

AK4M

INTEL Montevina

BLOCK DIAGRAM

Model

AK4M LV

AK4M VP

CPU
Penryn
u-FCPGA 478PIN

Thermal Sensor
GMT780-1

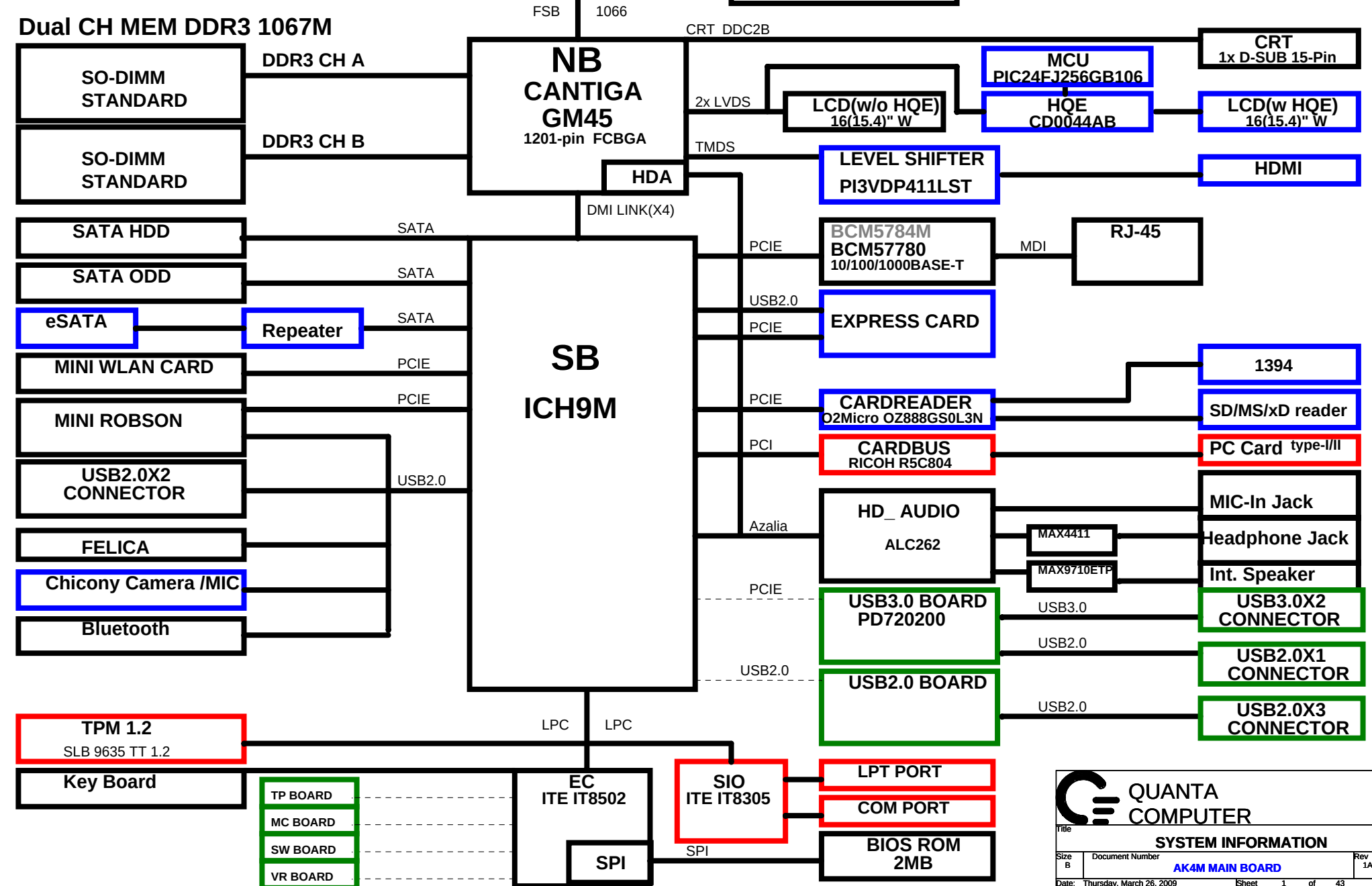
DC/DC & Charge

DC In

Battery

CLK Gen
ICS9LPR395

01

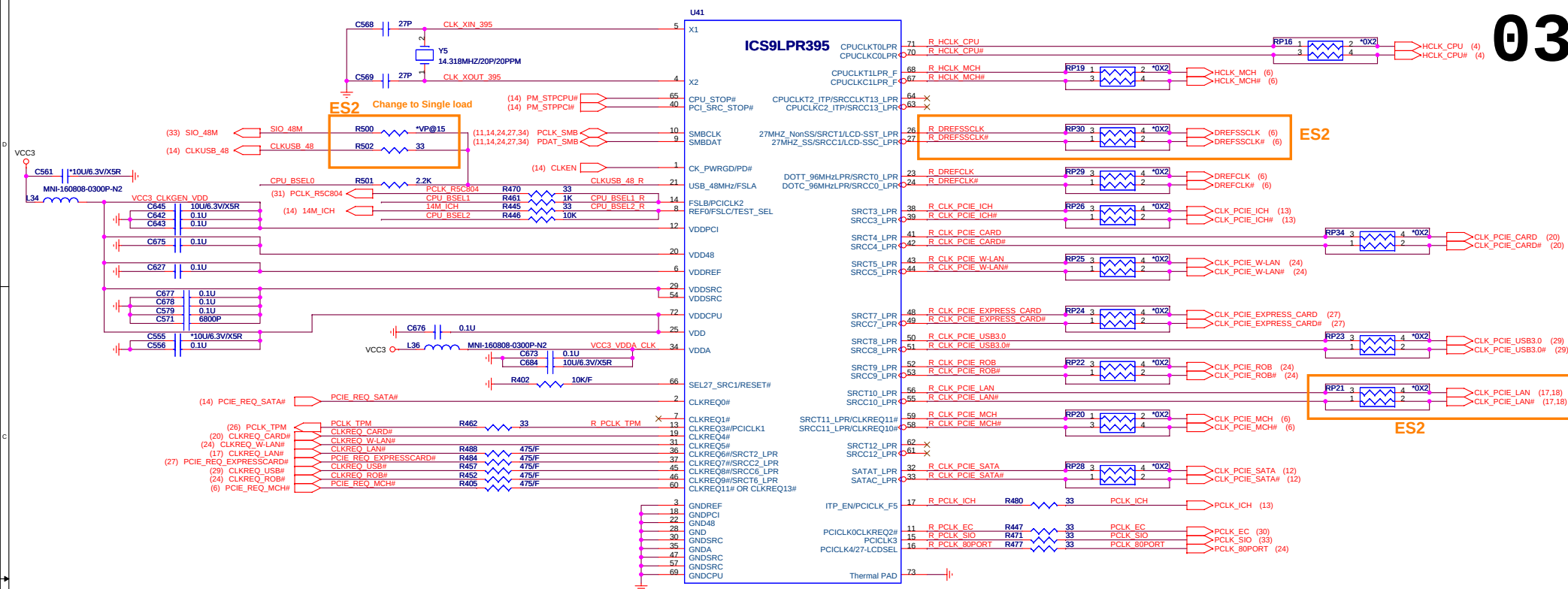


01. BLOCK DIAGRAM
02. PAGE LIST
03. CLOCK GENERATOR-ICS9LPR395
04. Pennyn CPU (1 of 2)
05. Pennyn CPU (2 of 2)
06. GMCH HOST & DMI (1 of 5)
07. GMCH DDR3 (2 of 5)
08. GMCH VIDEO (3 of 5)
09. GMCH POWER (4 of 5)
10. GMCH POWER 2 (5 of 5)
11. DDR3 SO-DIMM(204P)
12. ICH9-M HOST/SATA (1 of 4)
13. ICH9-M PCI E (2 of 4)
14. ICH9-M GPIO (3 of 4)
15. ICH9-M POWER (4 of 4)
16. HDMI
17. BCM5784M_LOM
18. BCM57780_LOM
19. CRT & LVDS
20. 4IN1 CARD/1394 888GS0L3N
21. SD_MS_XD SLOT
22. HD_ALC262
23. AUDIO AMP.
24. MINI PCI-E
25. SATA(HDD)/SATA(ODD)/eSATA
26. INT.KB/TOUCH-PAD/FAN/TPM
27. NEW CARD/BLUETOOTH
28. FELICA/CAMERA/SCREW HOLE
29. USB/BUZZER
30. EC_ITE8502
31. R5C804_PCI

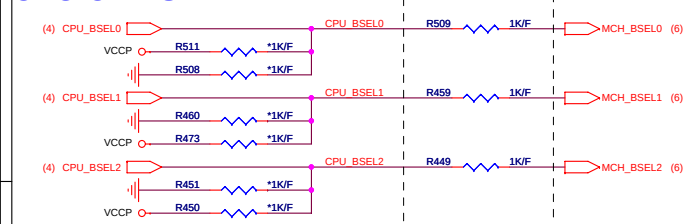
32. R5C804_CARDBUS
33. ITE8305 SUPER IO
34. CD0044AB(HQE)
35. MCU PIC24FJ256GB106
36. POWER +CPU_CORE (MAX17021)
37. POWER 3V & 5V (MAX17020)
38. POWER 1.5VSUS/VTM_MEM
39. POWER VCCP& 1.2V_HQE
40. CHARGER(ISL6251)
41. Battery connector
42. Discharge
43. CHANGE HISTORY

AK4M PWR Rails table:

Power Rails	Level	S3	S4	S5	Ctl Signal
15VPCU	15V	0	0	0	PWR DC/DC
5VPCU	5V	0	0	0	
3VPCU	3.3V	0	0	0	
RVCC3	3.3V	0	0	0	RVCC_ON
RVCC5	5V	0	0	0	LAN_WOL_EN_EC
VCC3_LAN	3.3V	0	0	0	
5VSUS	5V	0	X	X	
3VSUS	3.3V	0	X	X	SUSON
1.5VSUS	1.8V	0	X	X	
VTM_MEM	0.9V	X	X	X	
SMDDR_VREF	0.9V	X	X	X	HQE_POWER_ON
3V_HQE	3.3V	X	X	X	
1.2V_HQE	1.2V	X	X	X	
VCC5	5V	X	X	X	MAINON
VCC3	3.3V	X	X	X	
VCC1.8	1.8V	X	X	X	
VCC1.5	1.5V	X	X	X	
VCCP	1.05V	X	X	X	
VCC1.0_USB	1.0V	X	X	X	
CPU_CORE	By VID	X	X	X	VRON



CPU CLK SEL



FSC BSEL2	FSP BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
* 0	1	0	200.00	100	33.33	14.318	48	96	0.5 Down
0	1	1	166.66	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	200.00	100	33.33	14.318	48	96	0.5 Down

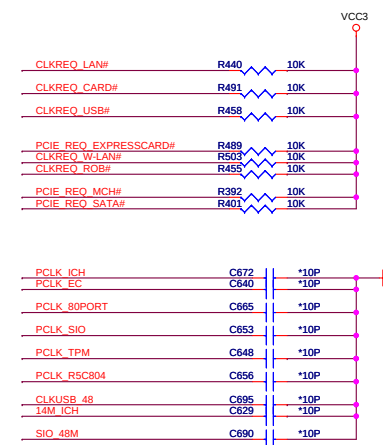
ITP_EN(PIN17)

* 0 : PIN63/64 SRC13/SRC13#

1 : ITP/ITP#

LCDSEL/27M Select Table

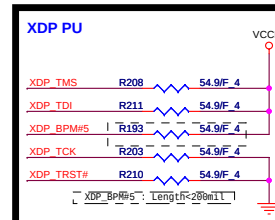
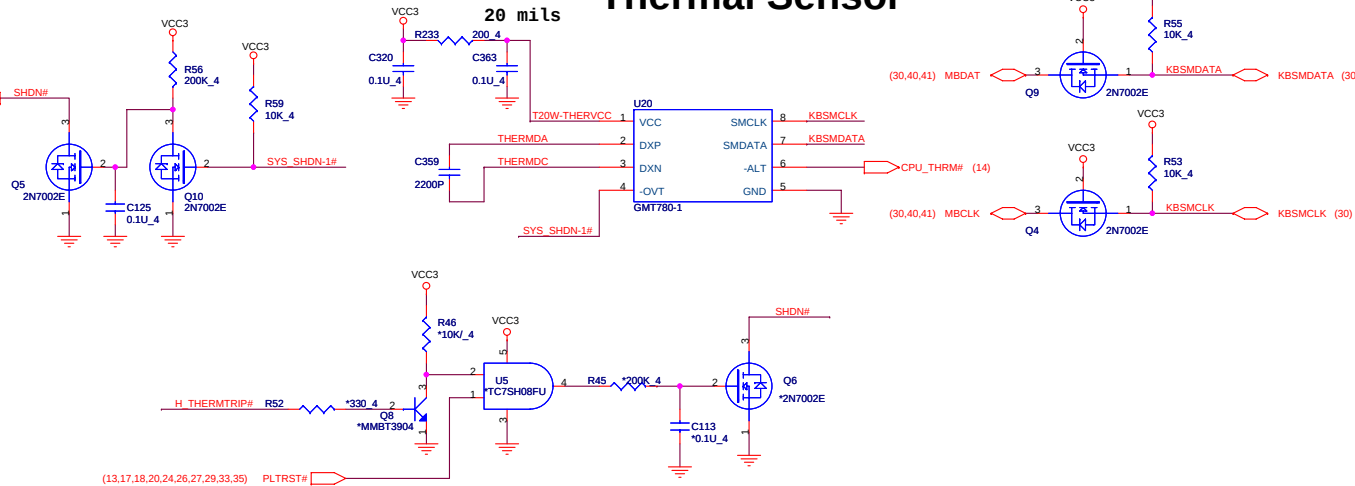
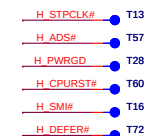
27 Select_SCR PIN16	SEL27_SRC1 PIN66	Dot96/SRC0 PIN 23/24	27MHz/SRC1/LCD PIN 26/27
0	0	SRC0	27MHZ (Ext Default)
* 1	0	DOT96	LCD (INT Default)
0	1	SRC0	SRC1
1	1	DOT96	SRC1

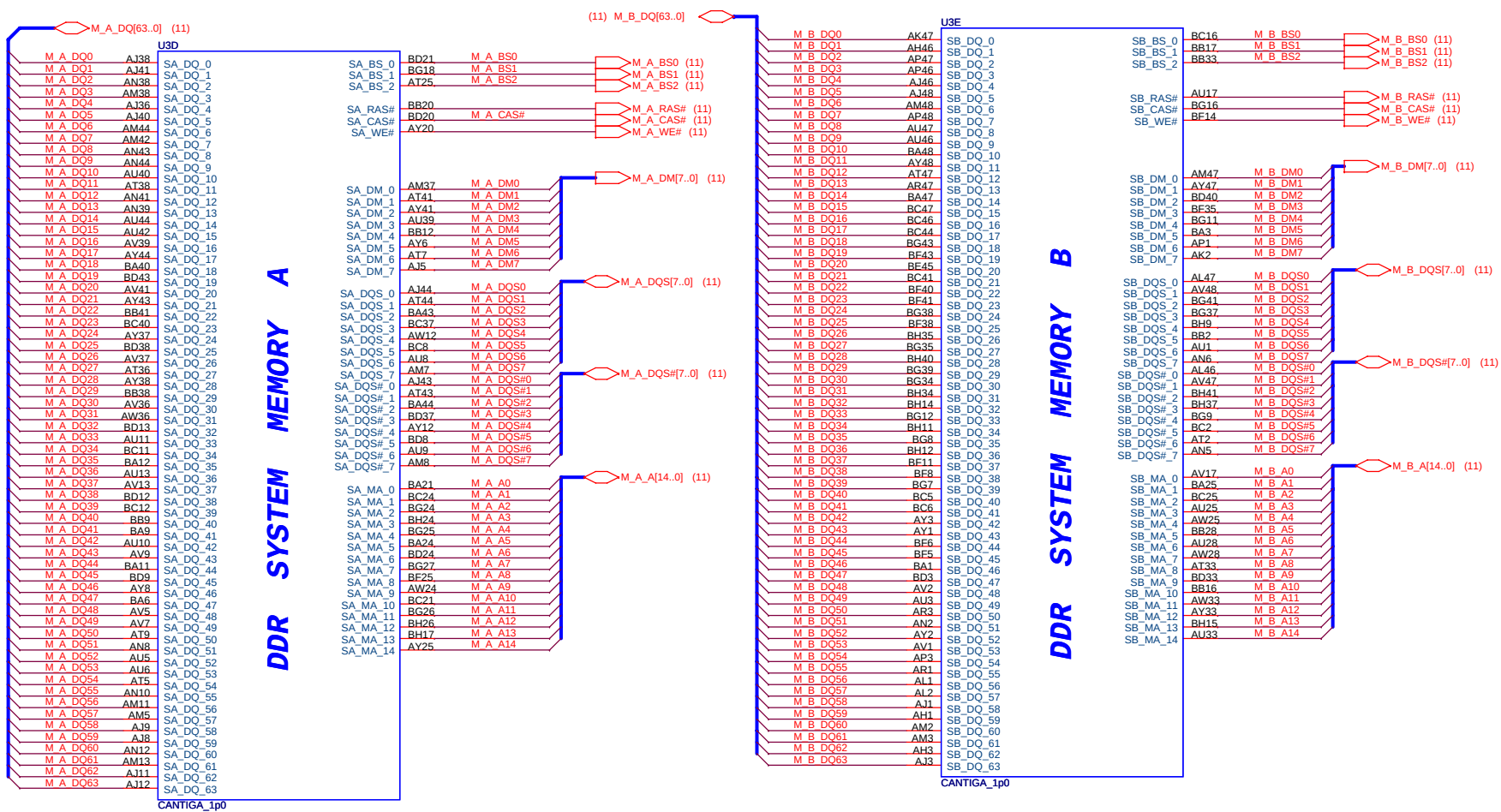
QUANTA
COMPUTER

CLOCK GENERATOR-ICS9LPR395

AK4M MAIN BOARD

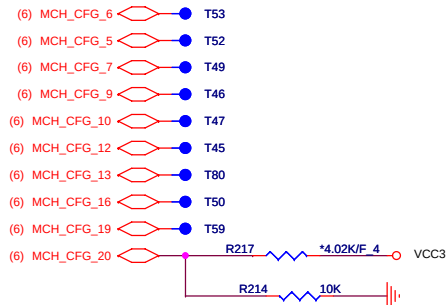
Date: Friday, March 13, 2009 Sheet 3 of 43

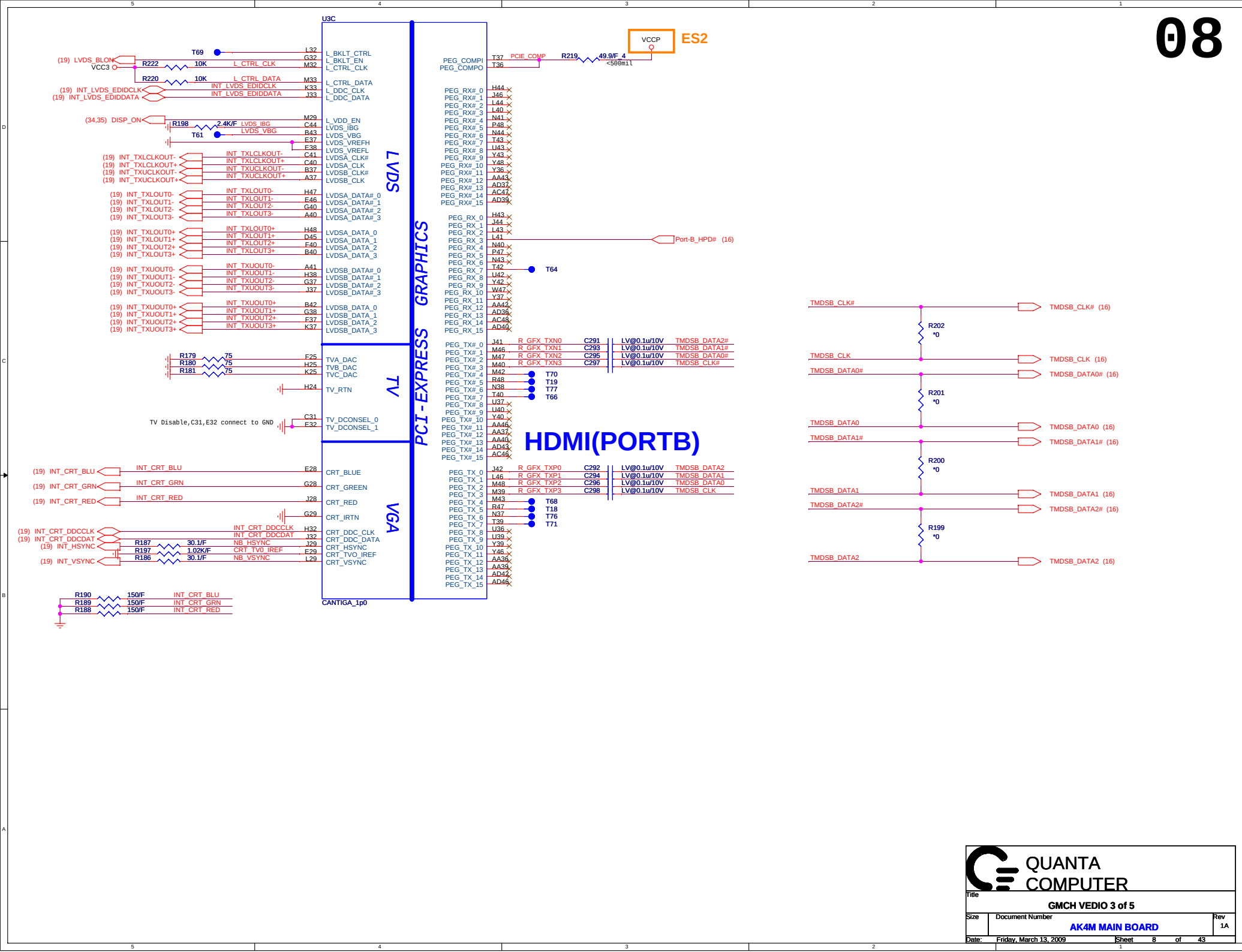


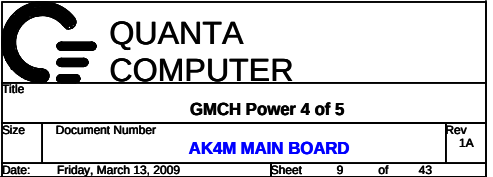


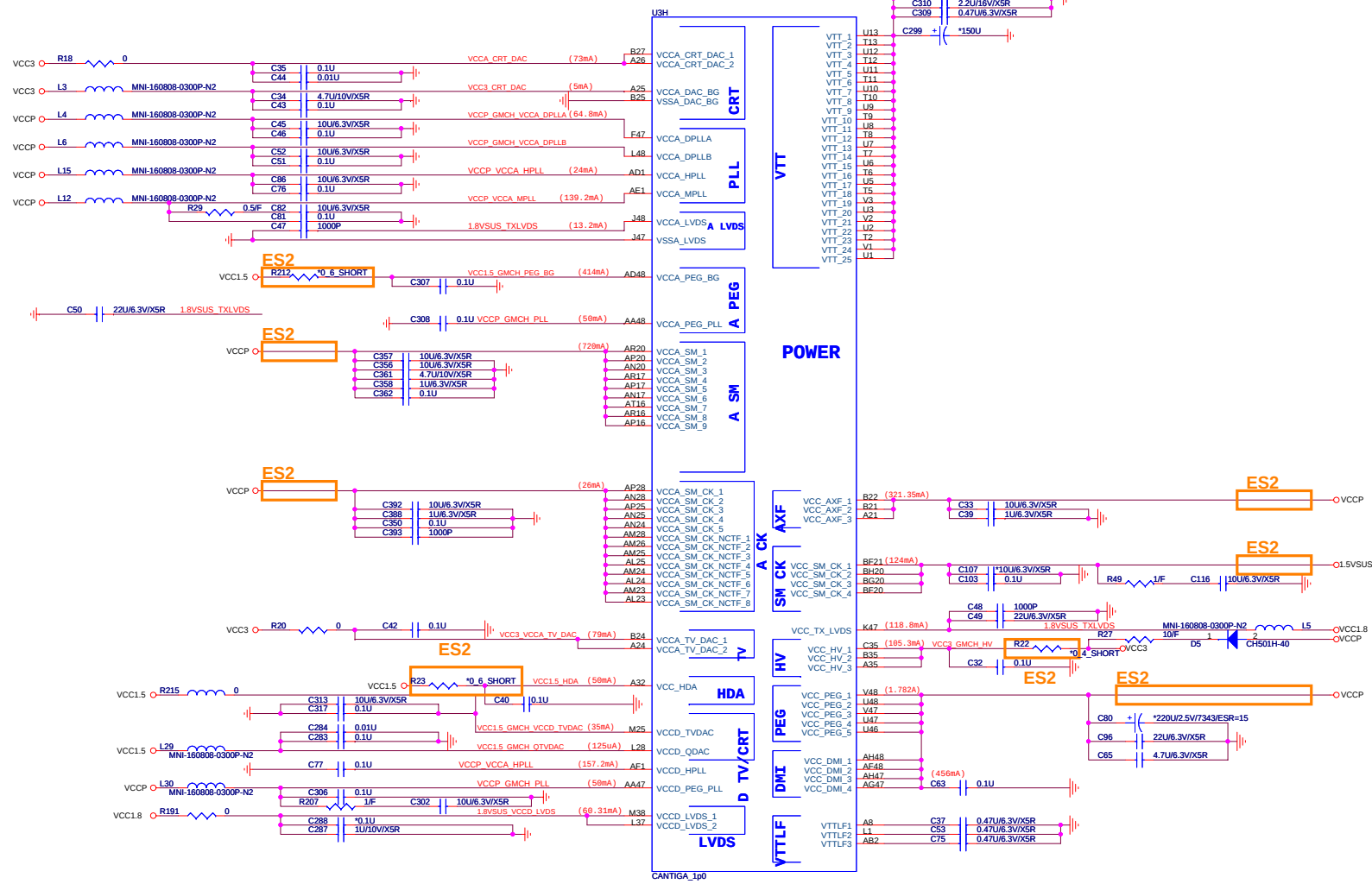
GMCH Strap pin description

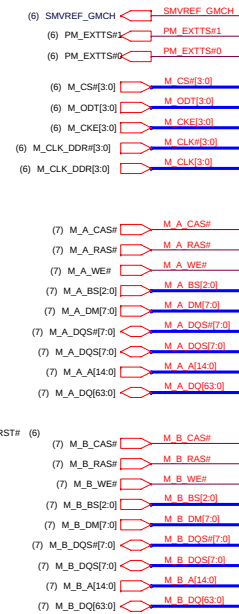
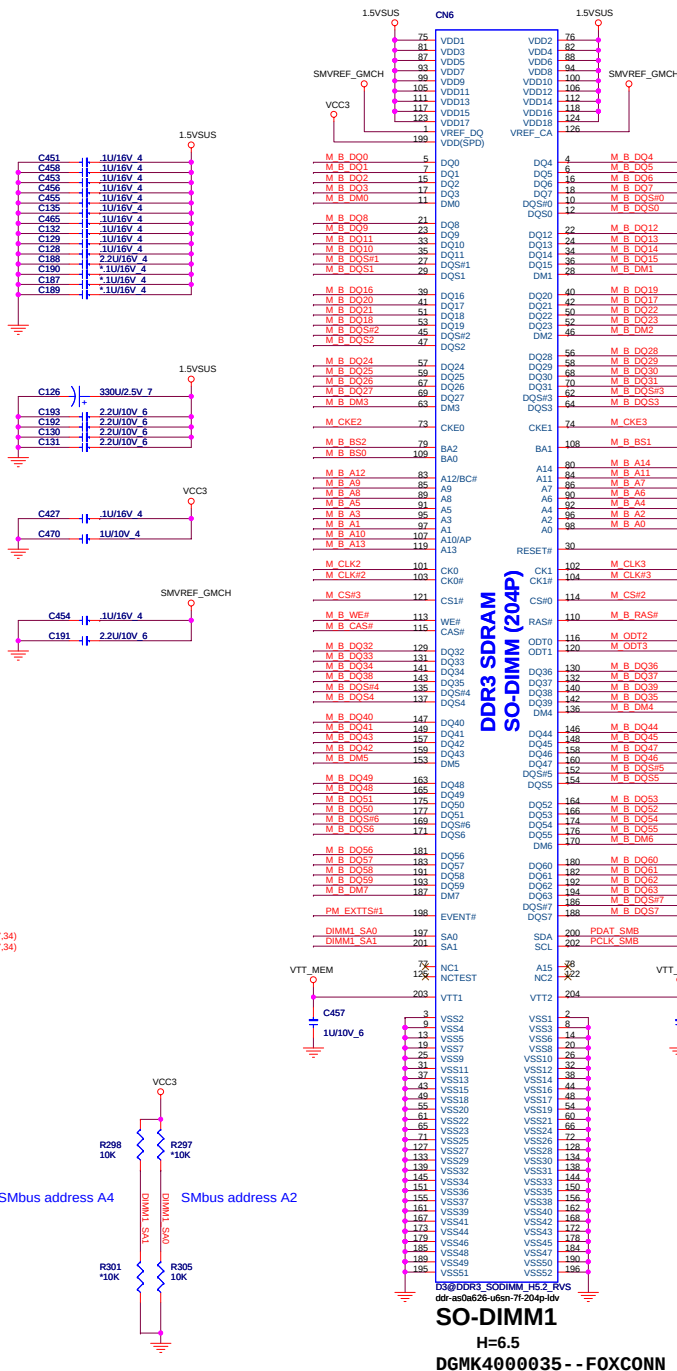
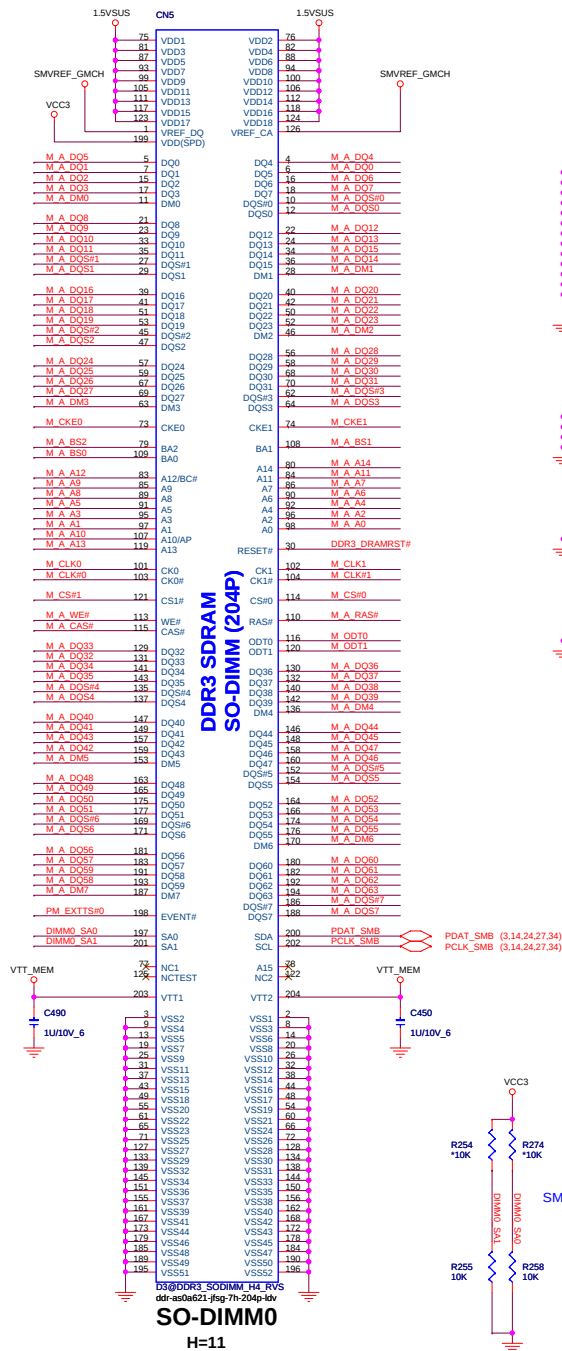
	Low	High
C6F5	DMIX2	* DMIX4
C6F6	ITPM HOST interface enable	* ITPM HOST interface disable
C6F7	AMT Fireware will use TLS cipher suite with no confidentiality	* AMT Fireware will use TLS cipher suite with confidentiality
C6F9	PCIe Graphics lan : Reverse Lane	* PCIe Graphics lan : Normal operation
C6F10	PCIe Loopback enable	* PCIe Loopback disable
C6F16	FSB Dynamic ODT Disabled	* FSB Dynamic ODT Enabled
C6F19	* DMI LANE Normal	DMI LANE Reversed
C6F20	* only SDVO/DP/HDMI or PCIe is operational	SDVO/DP/HDMI and PCIe are operation simultaneously via the PEG port
C6F[12:13]:XOR /ALLZ / Clock Un-gating	00 = Reserve 01 = XOR mode enabled 10 = All-Z mode enabled * 11 = Normal Operation(Default)	
Int.Pull-down : C6F 18,19,20		
Int.Pull-high : C6F C6F 3-17		

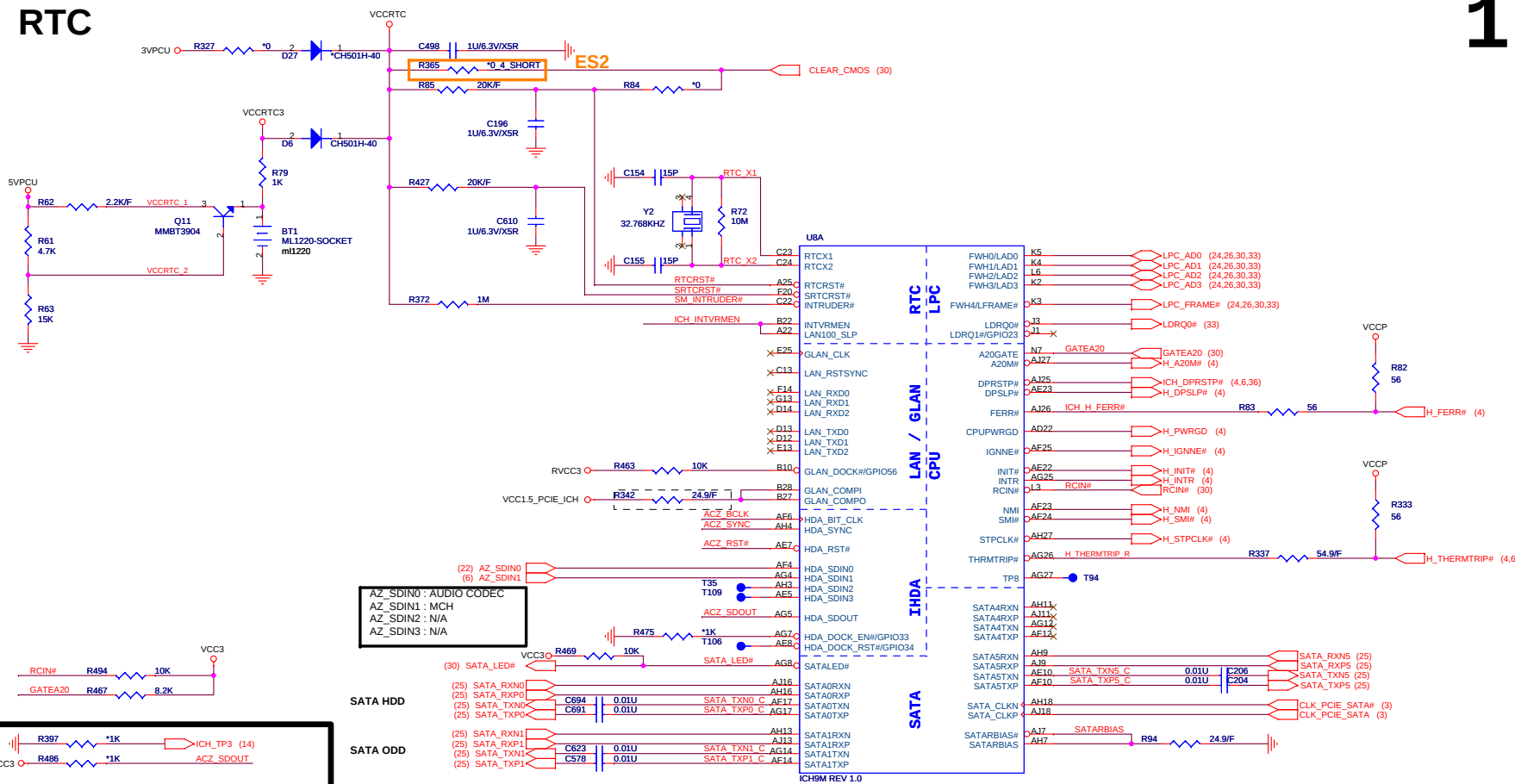












AZ_SDIN0 : AUDIO CODEC
AZ_SDIN1 : MCH
AZ_SDIN2 : N/A
AZ_SDIN3 : N/A

SATA HDD

SATA ODD

ICH9M REV 1.0

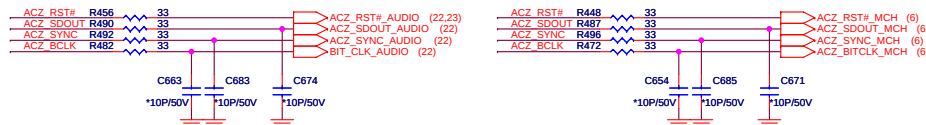
XOR Chain Entrance Strap

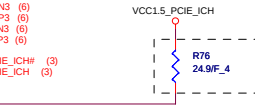
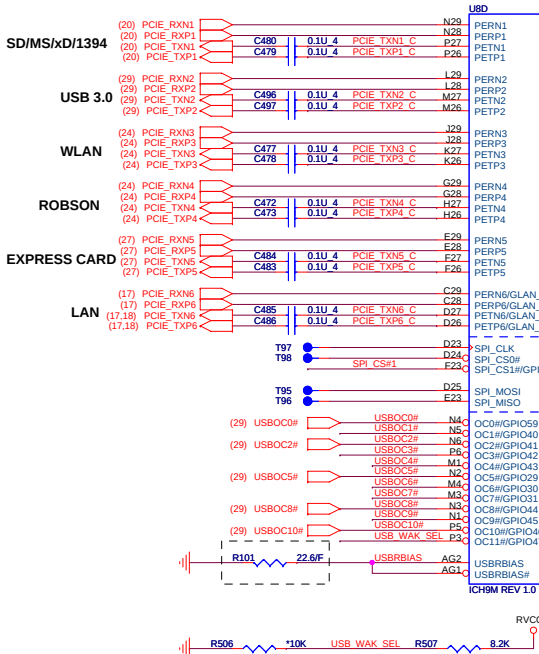
ICH_TP3	ACZ_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	* Normal operation
1	1	Set PCIe port config bit 1

Internal VRM Enable for Vccsus1_05, VccSus1_5, VccCL1_5, vccLAN1_05, vccCL1_05)

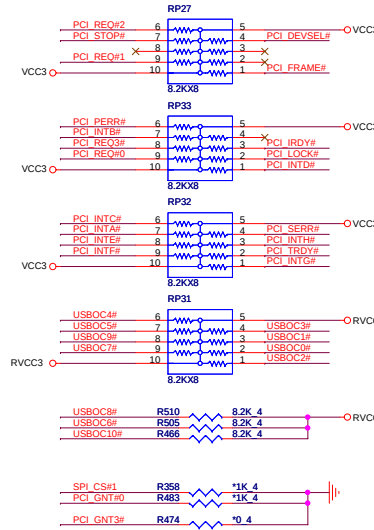
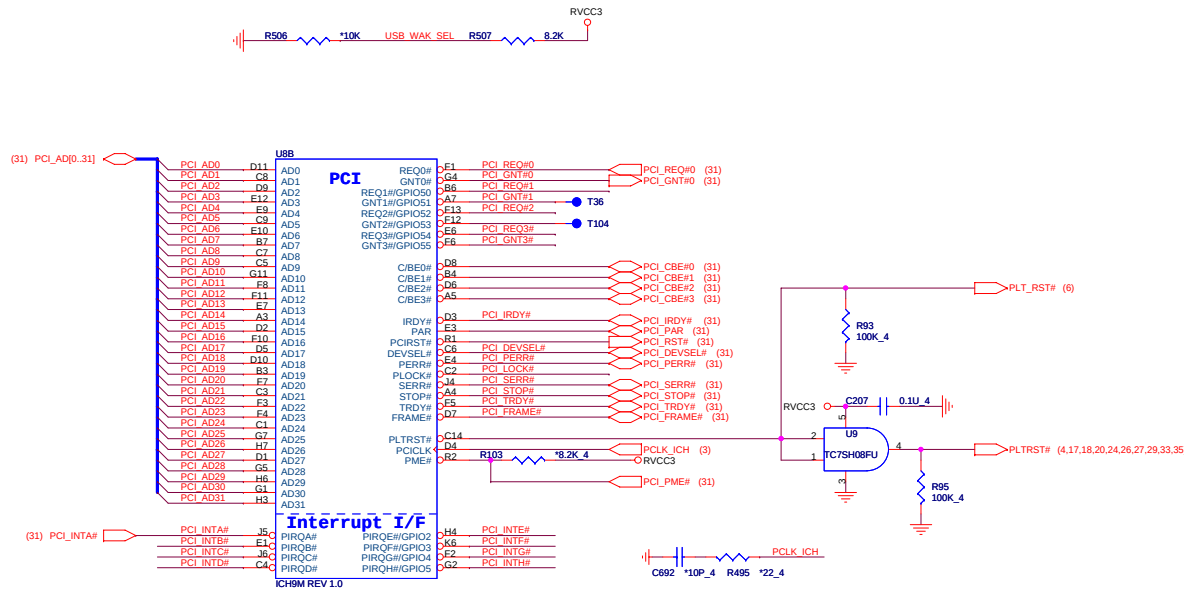
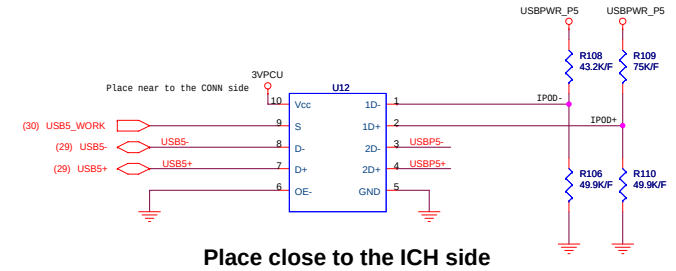
	INTVRMEN
Enable (default)	1
Disable	0

PLACE THESE PARTS NEAR ICH9M





USB	Function
PORT#0	USB (Debug)
PORT#1	ROBSON CARD
PORT#2	USB
PORT#3	FELICA
PORT#4	N/A
PORT#5	USB
PORT#6	BT
PORT#7	EXPRESS CARD
PORT#8	USB
PORT#9	MCU
PORT#10	USB
PORT#11	CAMERA



GPIO49 : NC
GPIO20 : Can't pull high.

A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default
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ICH9 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (default)

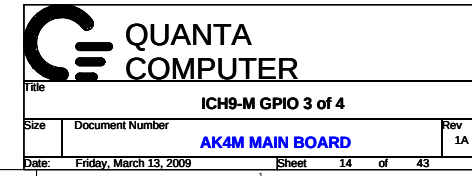
IRQ	Description
PIRQA	USB UHCI Controller #1,USB UHCI Controller #4
PIRQB	Audio, Modem ; SMBus
PIRQC	USB UHCI Controller #3, SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	INT LAN, option for Sd1,TCd,HPEt #0.1,2 ; i8412
PIRQF	option for Sd1,TCd,HPEt #0.1,2 ; i8412
PIRQG	option for Sd1,TCd,HPEt #0.1,2 ; i8412
PIRQH	USB EHCI Controller, option for Sd1,TCd,HPEt #0.1,2

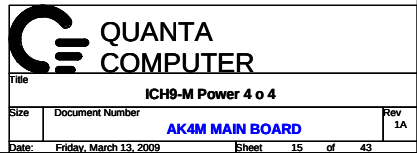


QUANTA
COMPUTER

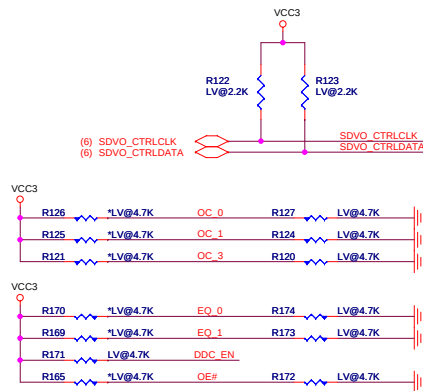
ICH9-M PCIe 2 of 4

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	AK4M MAIN BOARD	1A
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HDMI LEVEL SHIFT

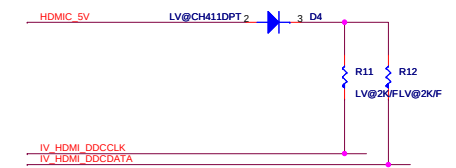
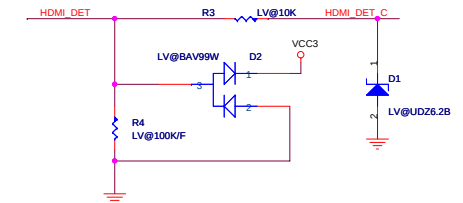
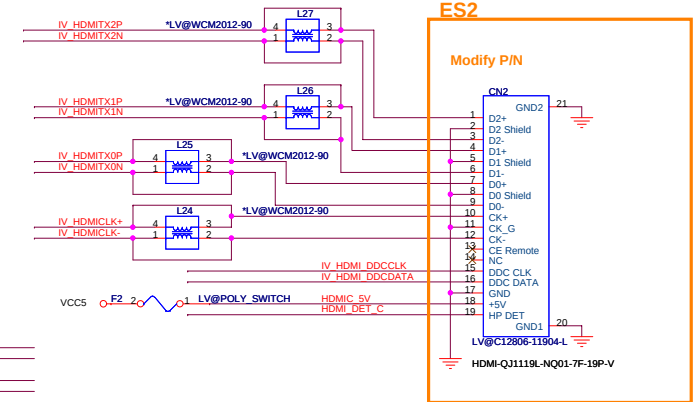
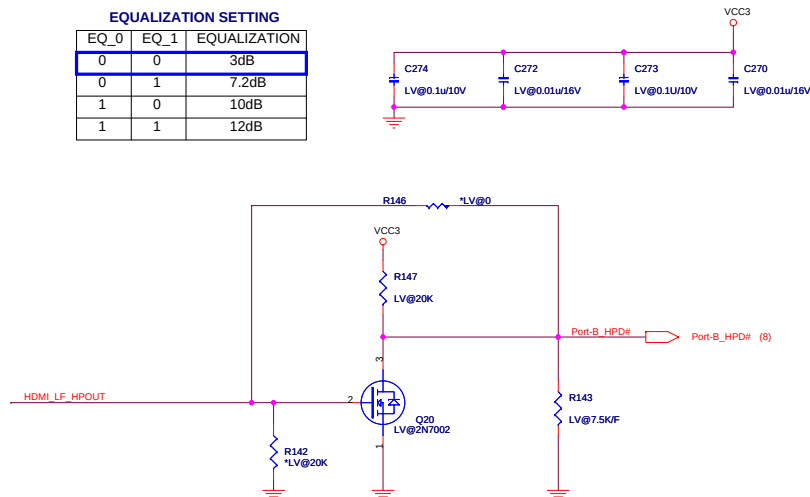


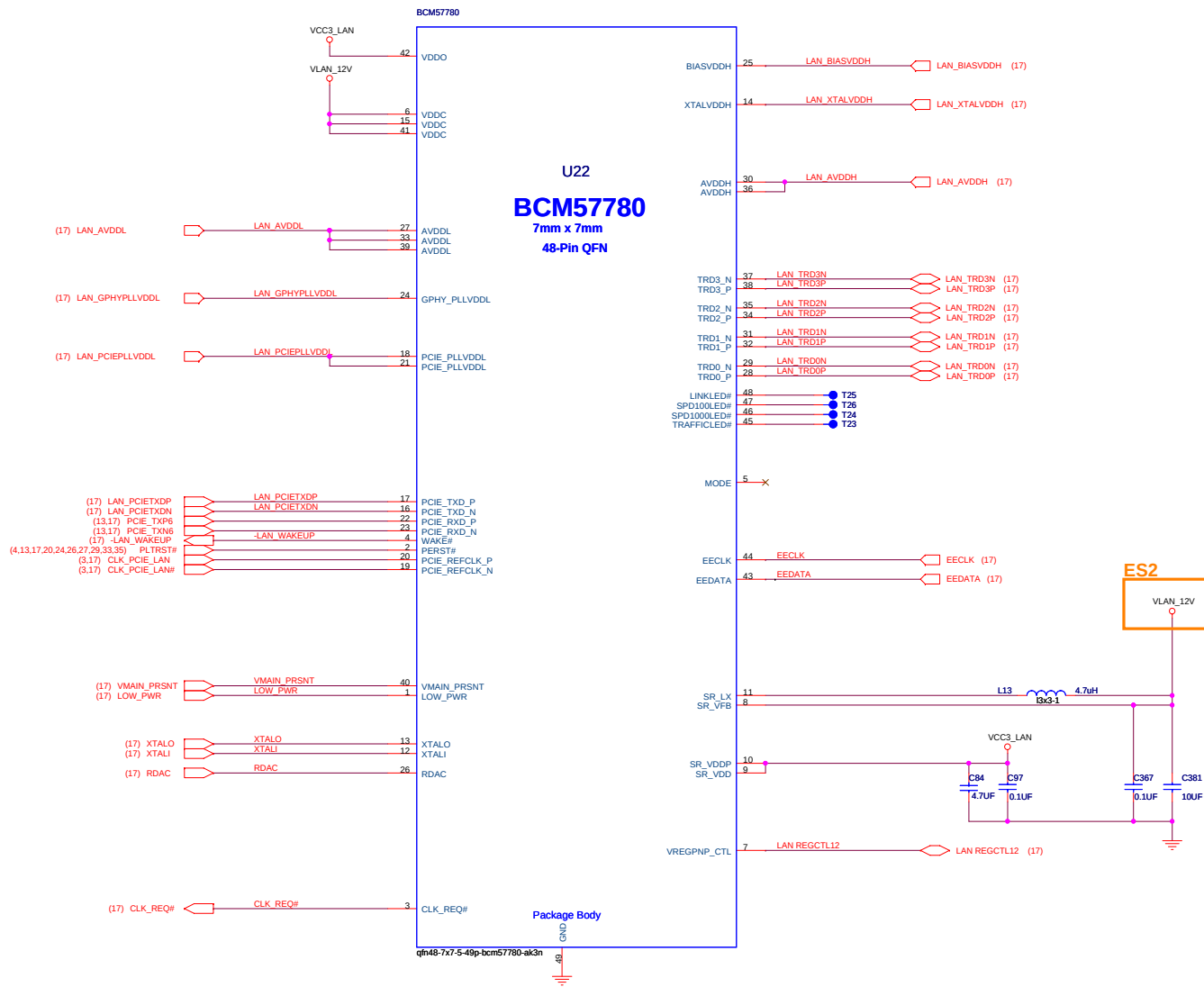
Vswing SETTING

OC_3	OC_2	OC_1	OC_0	Vswing(V)
0	0	0	0	0.5
0	0	0	1	0.6
0	0	1	0	0.75
0	0	1	1	1
1	0	0	0	0.4
1	0	0	1	0.4
1	0	1	0	0.4
1	0	1	1	0.4

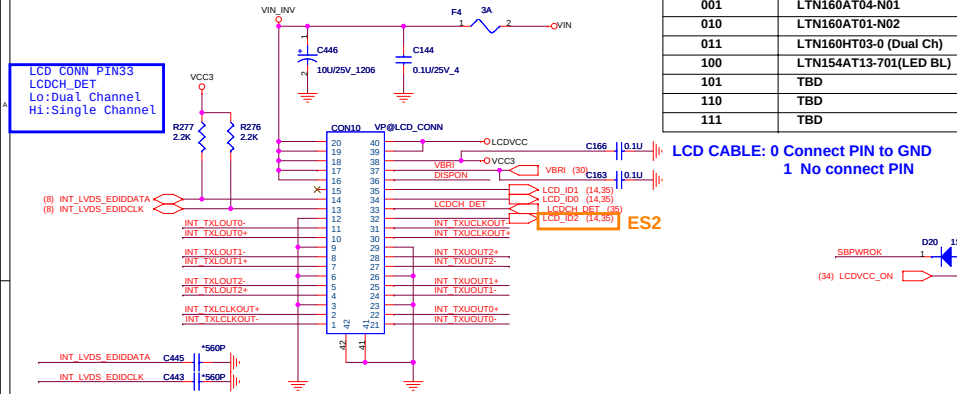
EQUALIZATION SETTING

EQ_0	EQ_1	EQUALIZATION
0	0	3dB
0	1	7.2dB
1	0	10dB
1	1	12dB

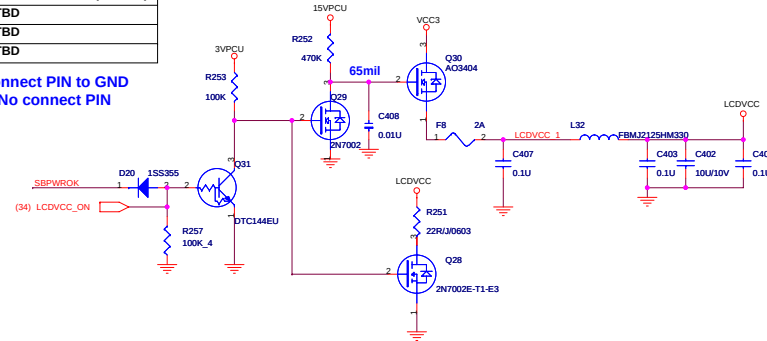




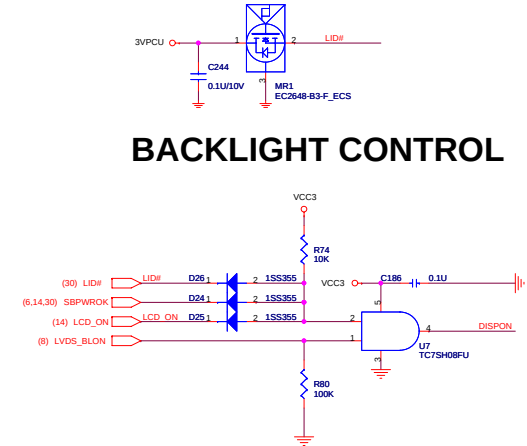
LVDS(w/o HQE)



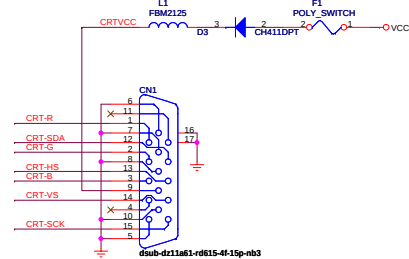
PANEL VCC CONTROL



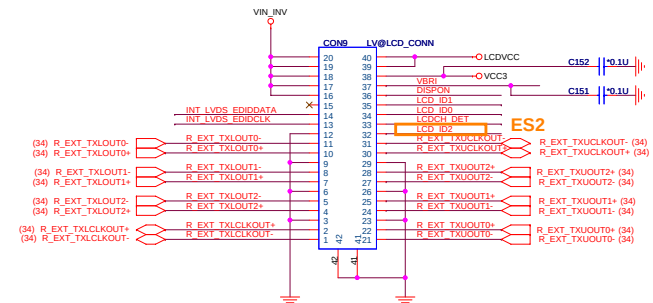
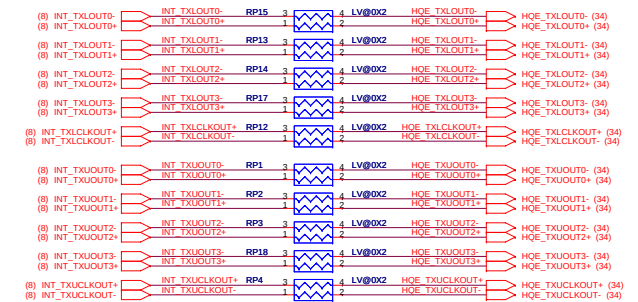
BACKLIGHT CONTROL



CRT CONNECTOR



LVDS(w HQE)



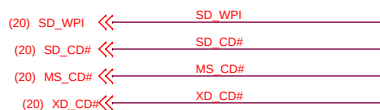
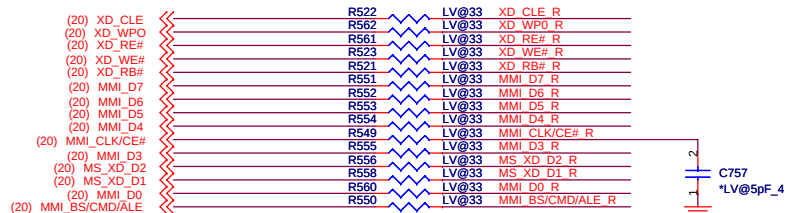
QUANTA
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CRT & LCD

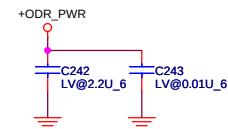
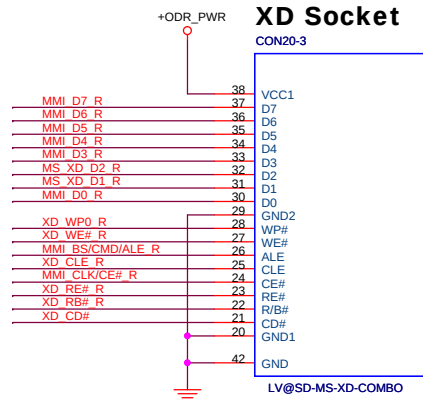
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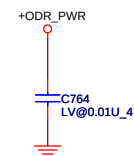
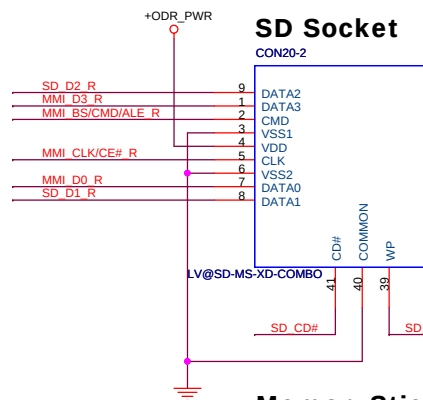
PLACE THESE PARTS NEAR OZ888GS0



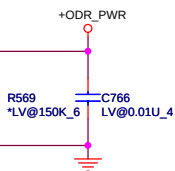
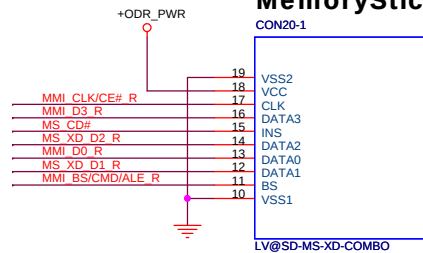
XD Socket



SD Socket

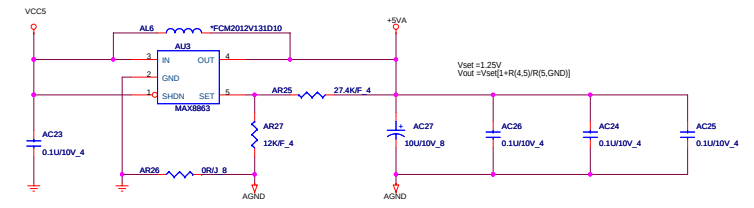
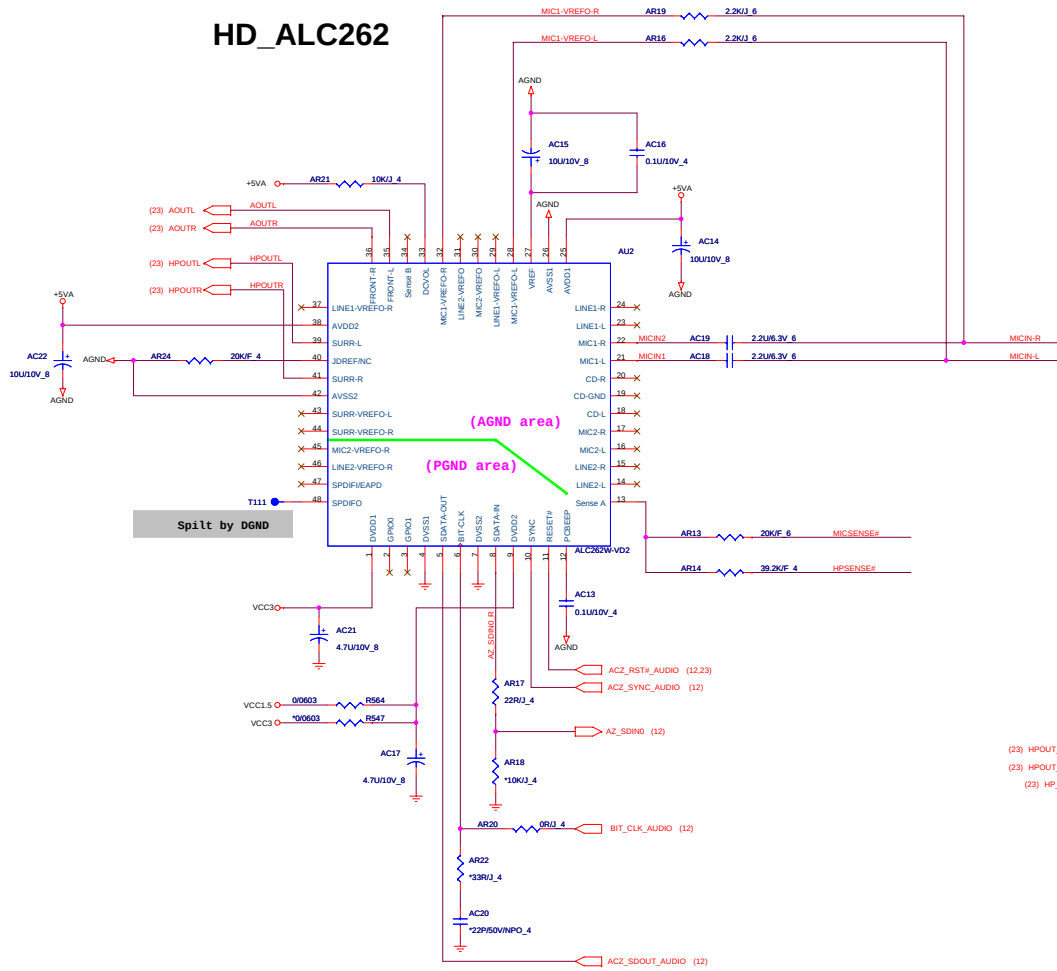


MemoryStick Socket



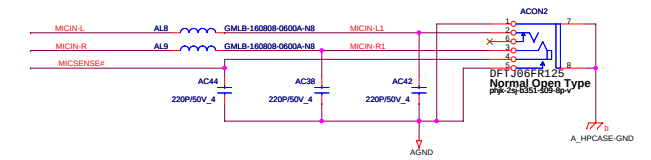
QUANTA
COMPUTER

HD_ALC262



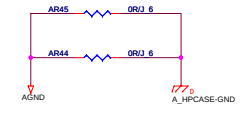
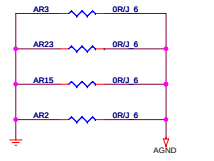
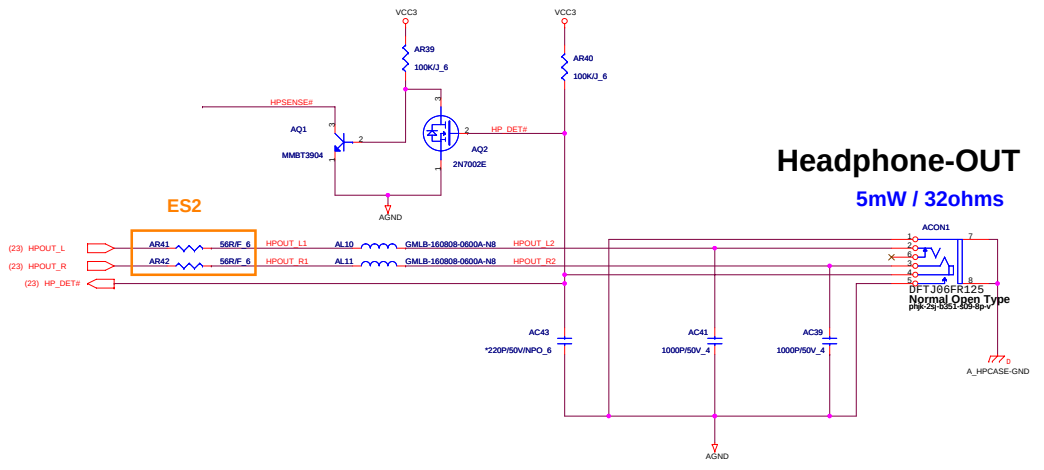
MIC-IN

Max. 100mVrms input for Mic-IN



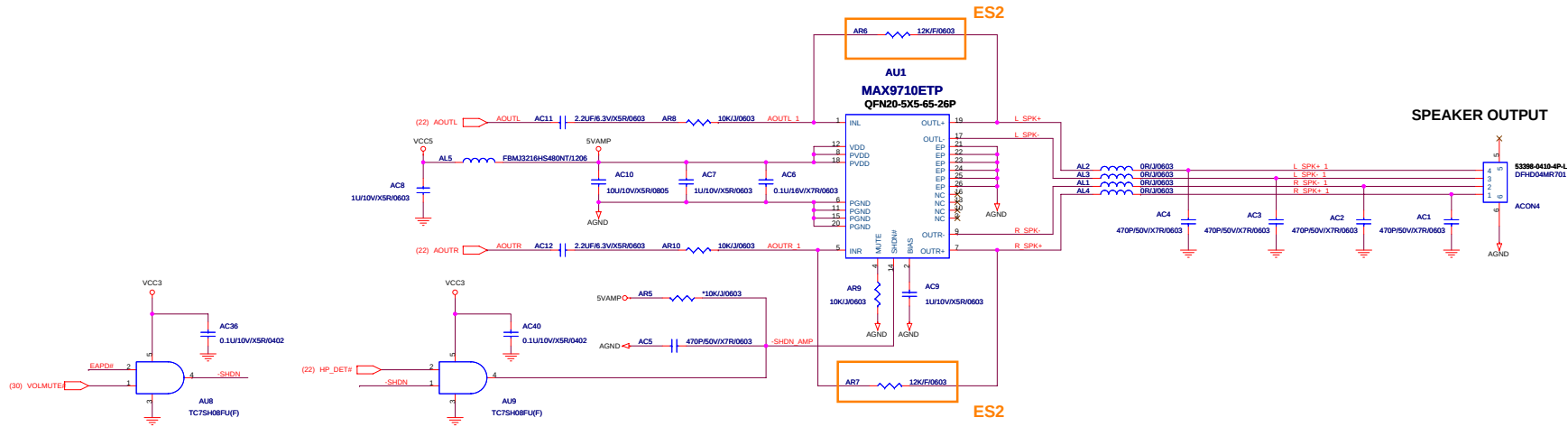
Headphone-OUT

5mW / 32ohms

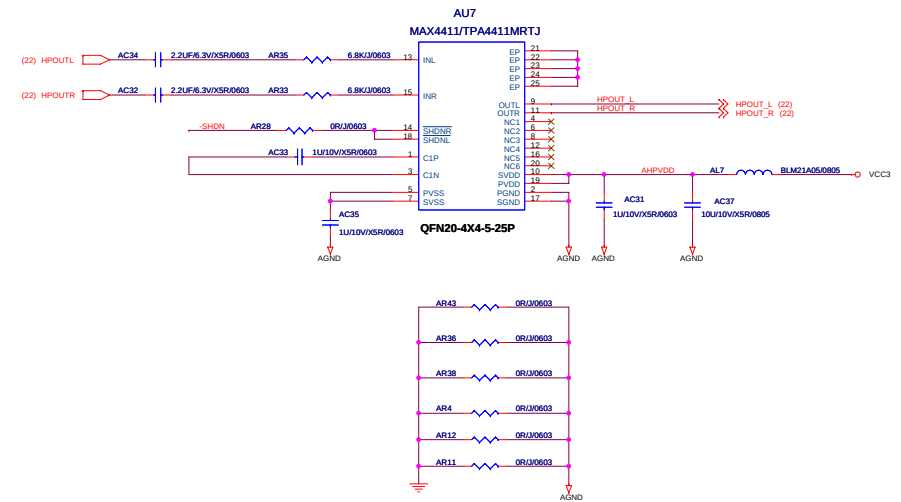
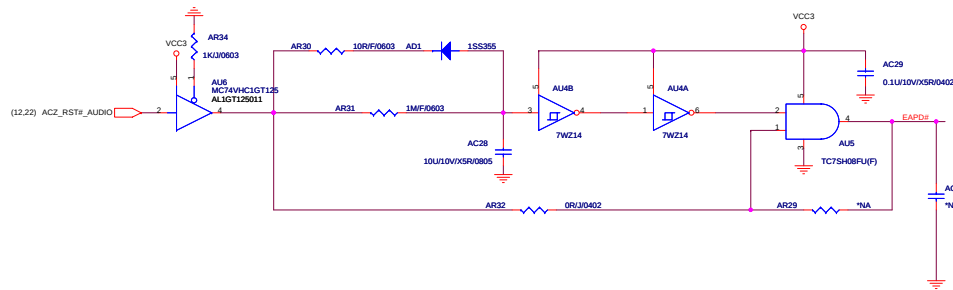


Place at CODEC bottom between the GND and AGND

AUDIO AMPLIFIER



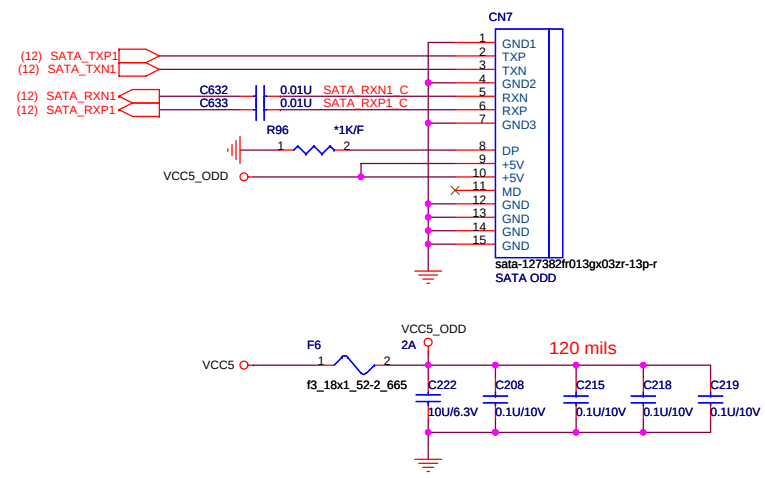
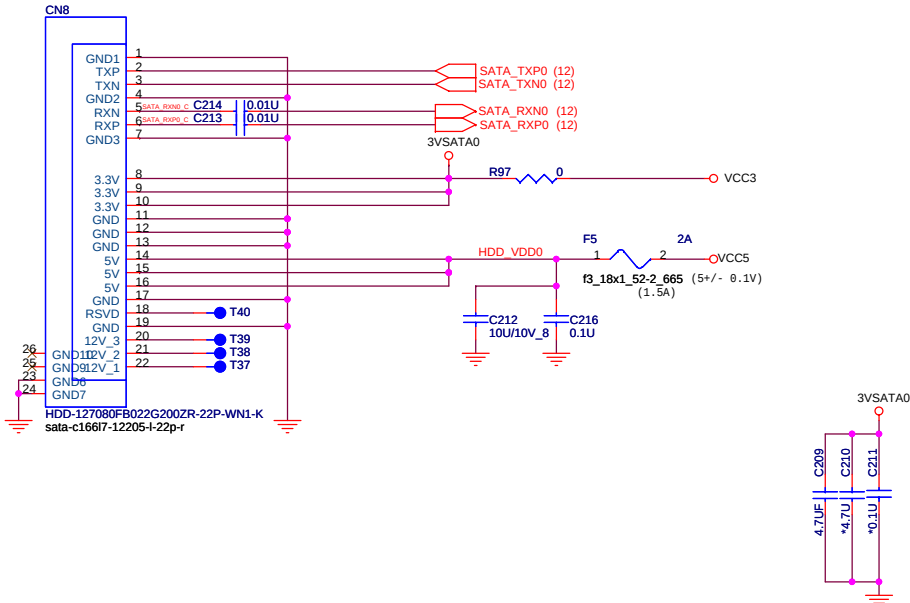
H.P AMPLIFIER



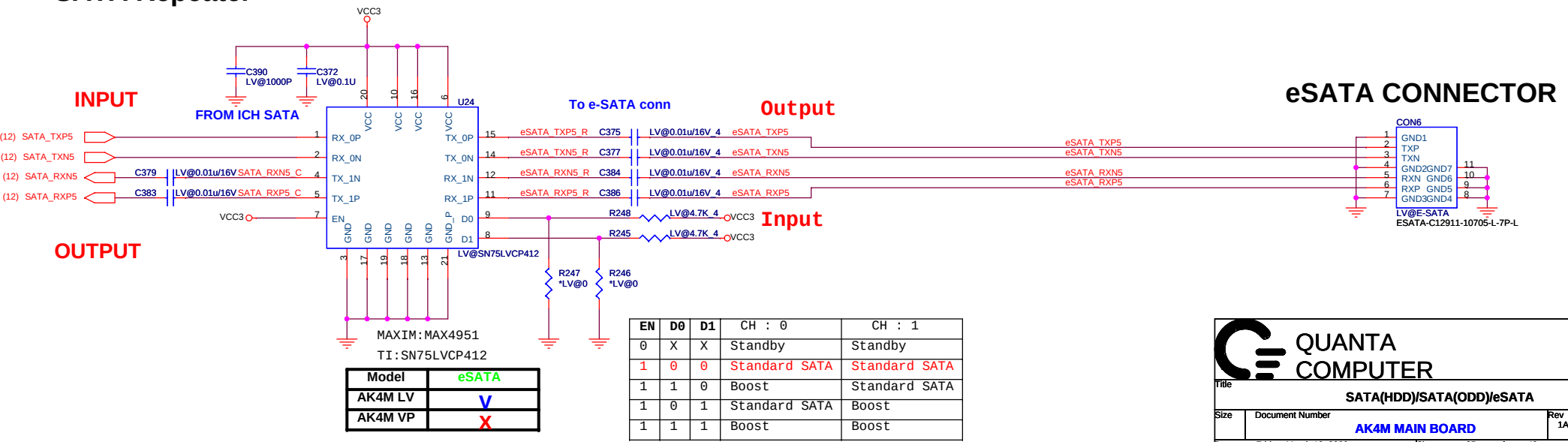
SATA HDD

SATA ODD

25



SATA Repeater



EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

QUANTA
COMPUTER

Title: **SATA(HDD)/SATA(ODD)/eSATA**

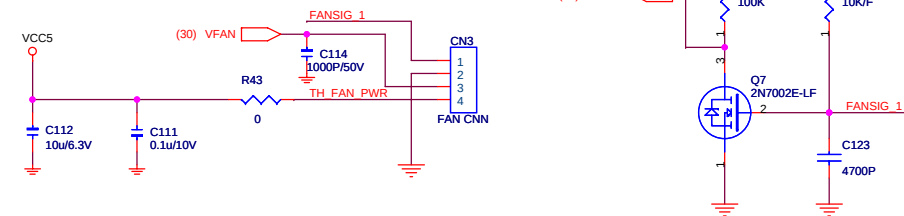
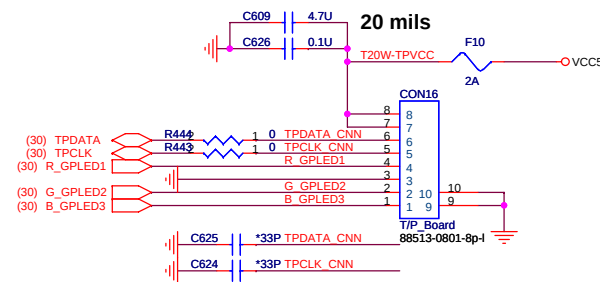
Size: **AK4M MAIN BOARD**

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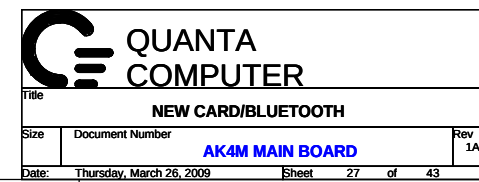
Sheet: **25** of **43**

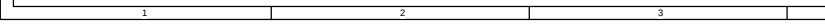
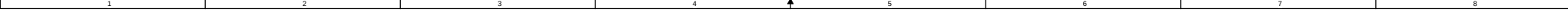
26

[illegible]

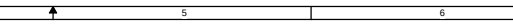
		I/O Address	
BADDR		Index	Data
0		2E	2F
1		4E	4F

27



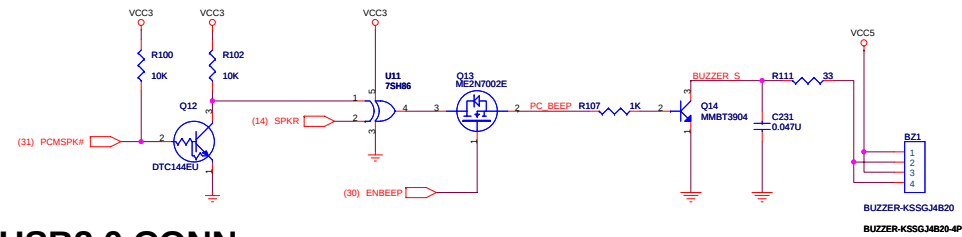


5

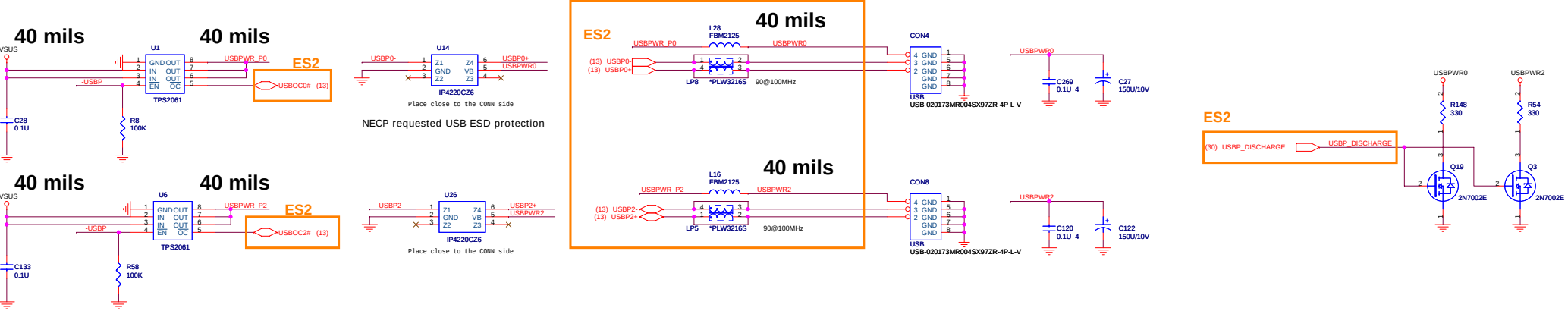


7	8
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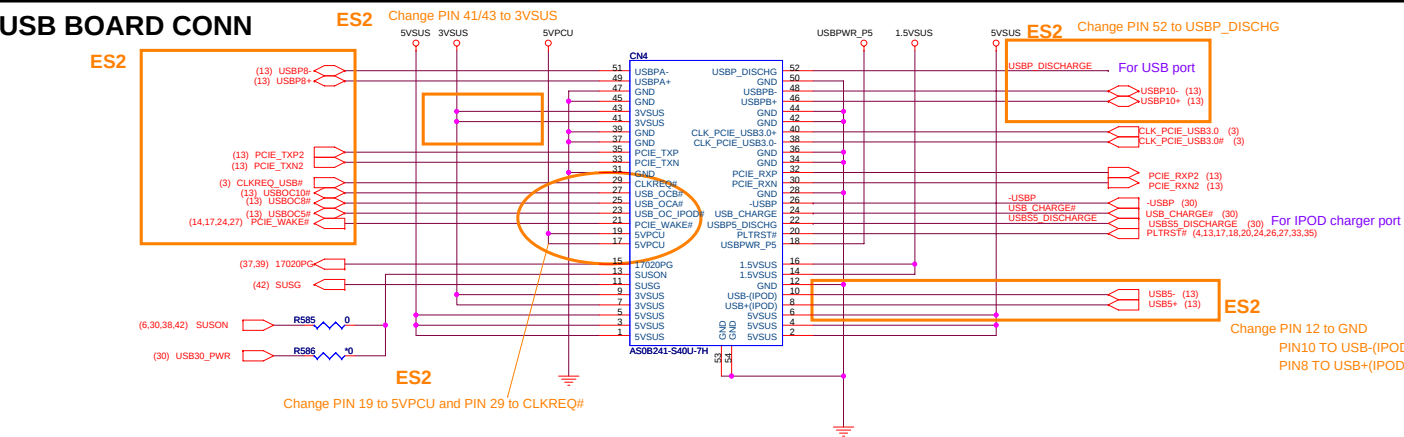
BUZZER



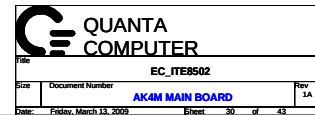
USB2.0 CONN

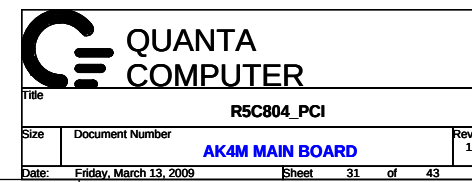


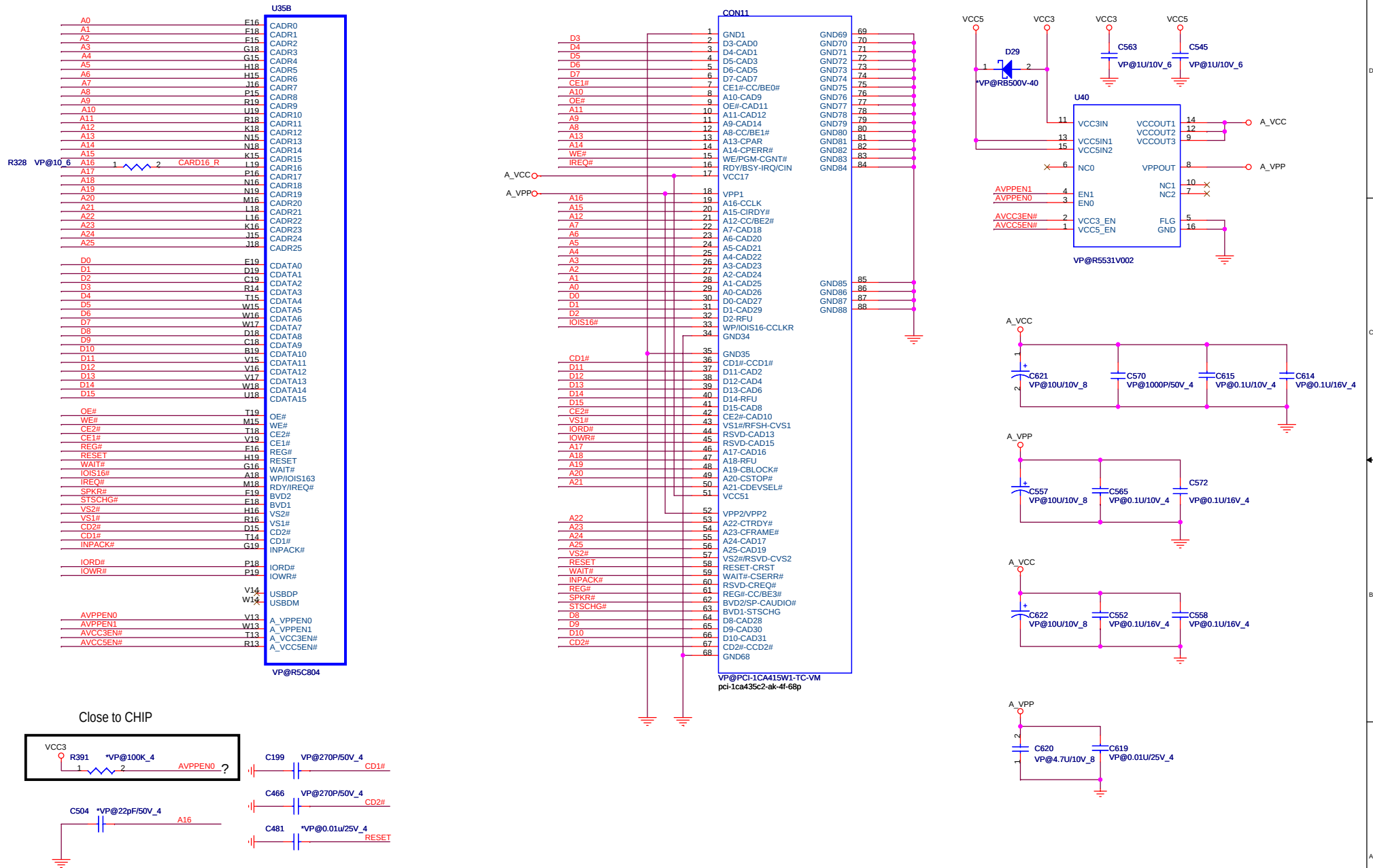
USB BOARD CONN



 QUANTA COMPUTER	
Title _____	
USB/BUZZER	
Size _____	Document Number AK4M MAIN BOARD
Date: Friday, March 13, 2009	Sheet 29 of 43 Rev 1A





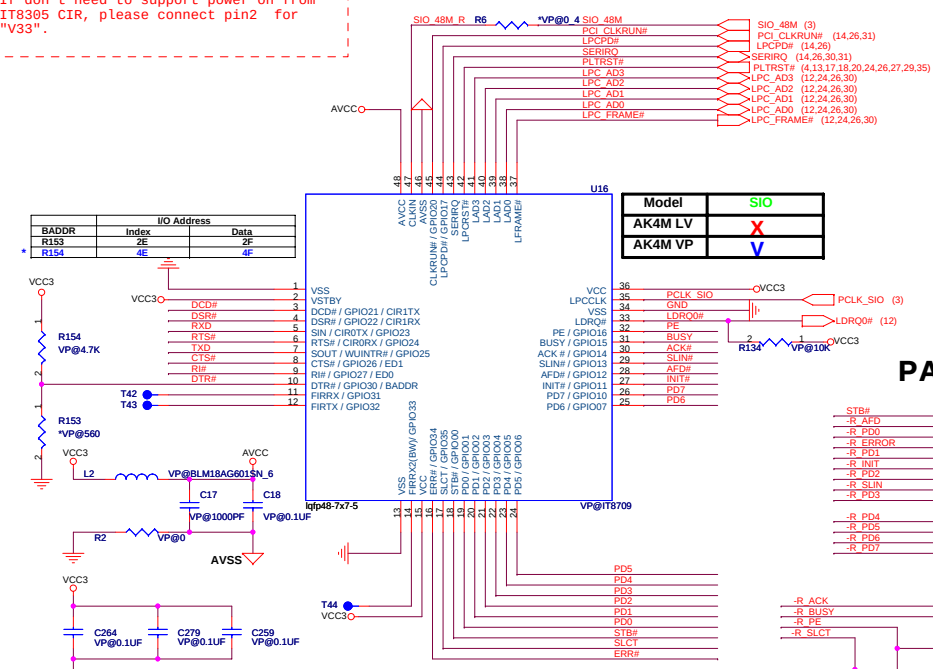


Note for pin 2:
If needs to support power on from IT8305
CIR, please connect pin2 for "VSTBY".
If don't need to support power on from
IT8305 CIR, please connect pin2 for
"V33".

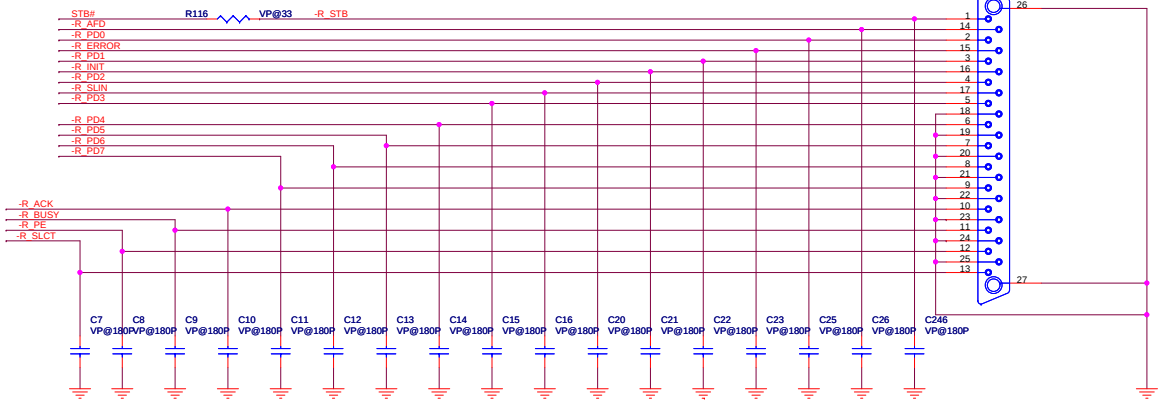
From External CLK for
14.318MHz(default) or
48MHz

ES2

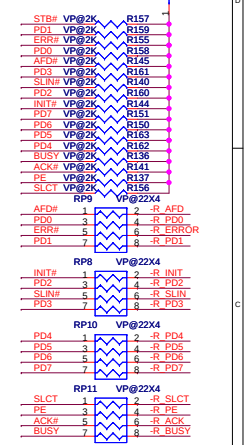
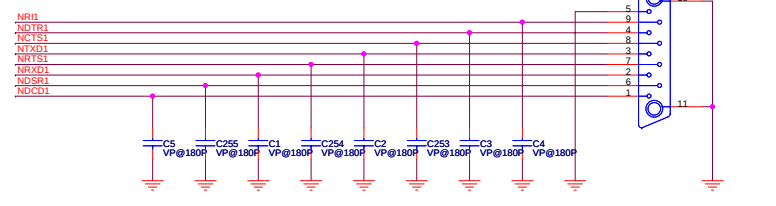
Check footprint and P/N



PARALLEL PORT



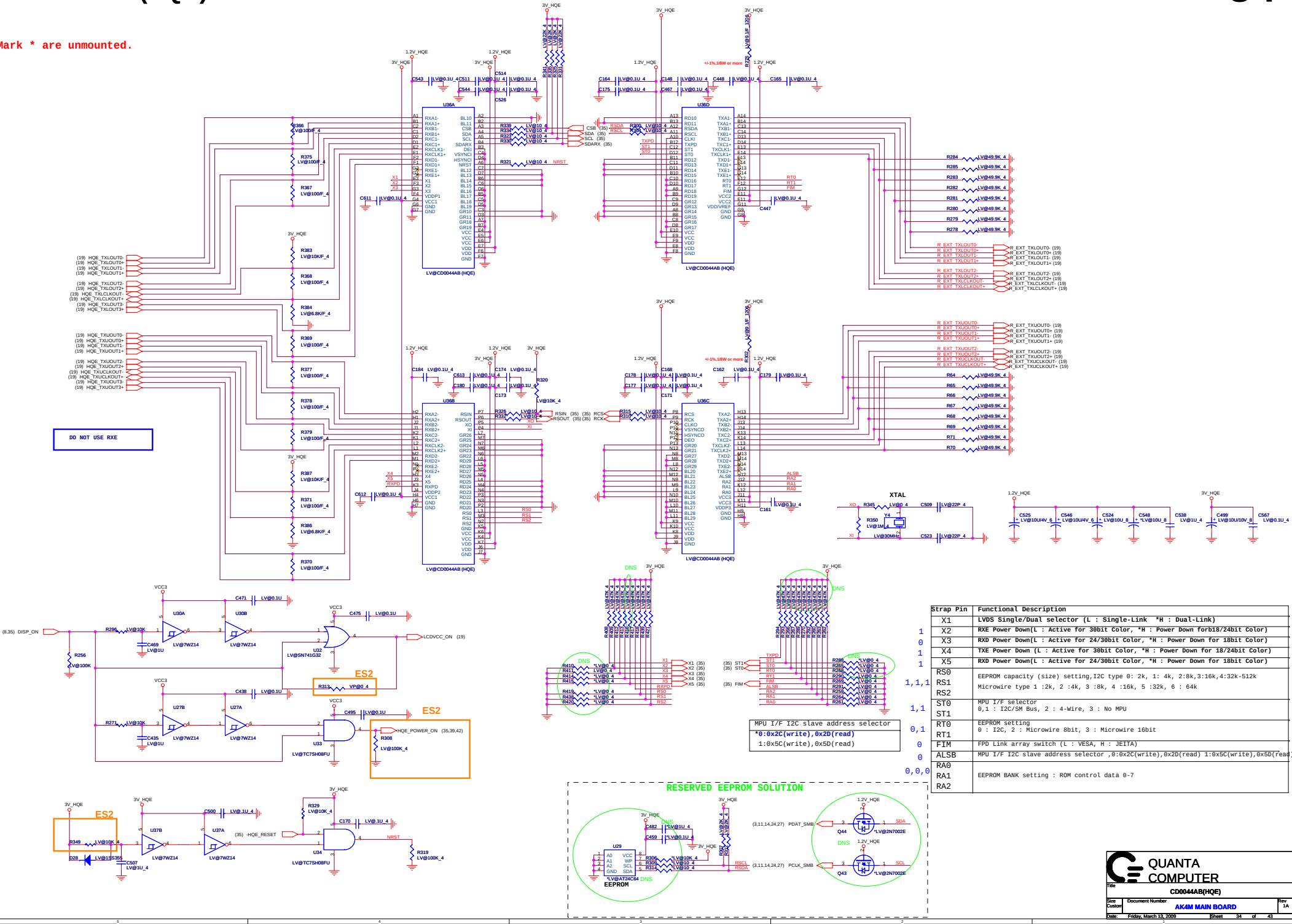
SERIAL PORT



QUANTA
COMPUTER

File: ITE8709 SUPER IO		
Size: Custom	Document Number: AK4M MAIN BOARD	Rev: 1A
Date: Thursday, March 26, 2009	Sheet: 33	of 43

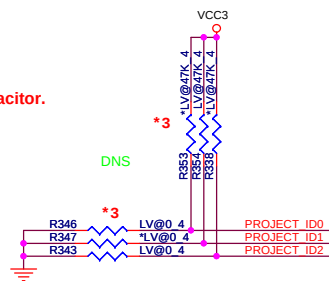
Mark * are unmounted.



*3: *** are unmounted.

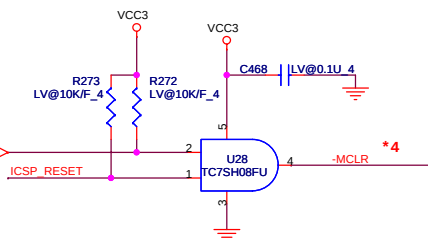
*4 are Low active signals.

*8: C80 must use the low ESR capacitor.



Project_ID[2,1,0]	Project name
000	AK4
001	AK4D
010	AK4M
011	TBD
100	TBD
101	TBD
110	TBD
111	TBD

MCU_RESET

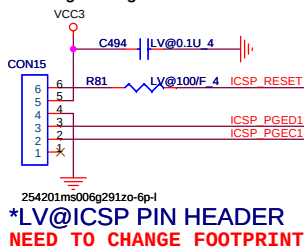


LCDCH_DET
Lo: Dual Channel
Hi: Single Channel

LCDCH_DET
L: Dual-Link
H: Single-Link

OUT_MODE
L: 18bitRGB
H: 24bitRGB

ICSP Programming HEADER



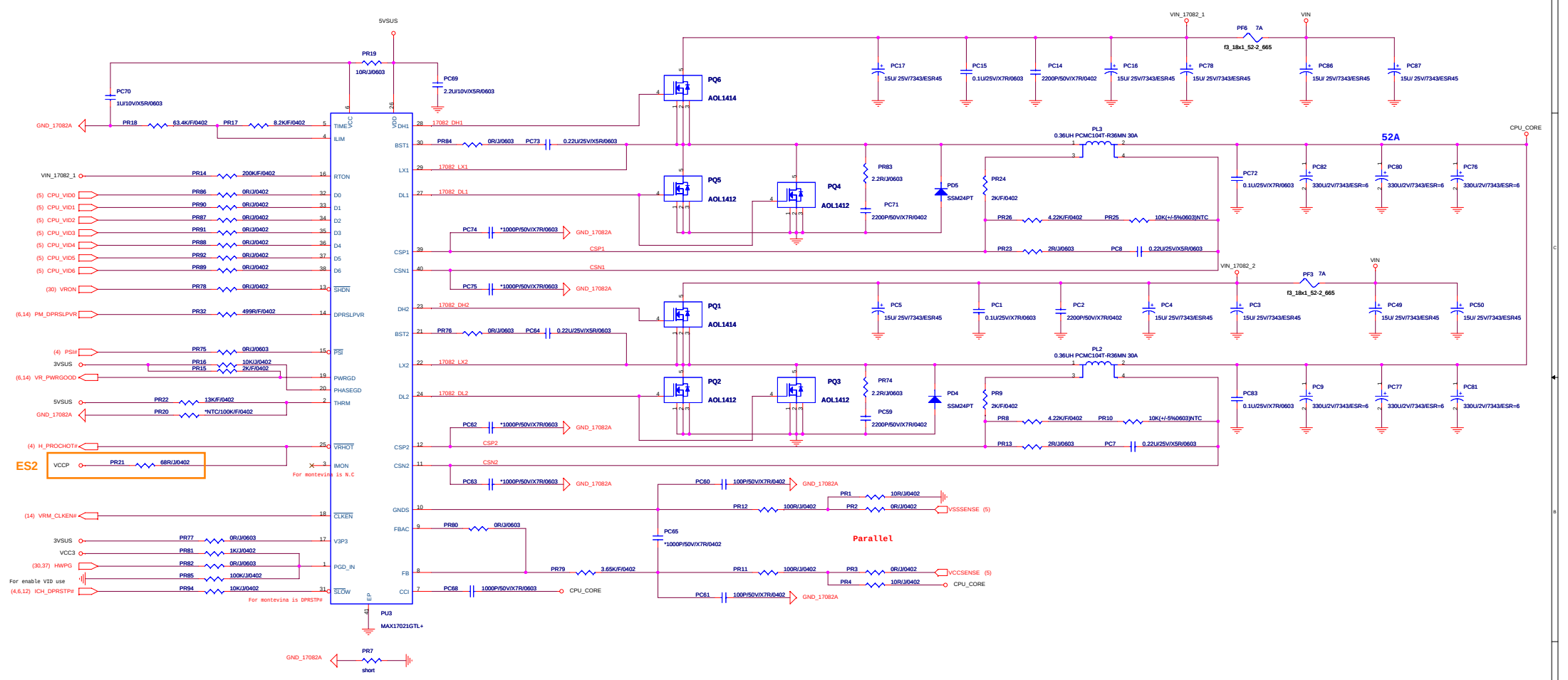
254201ms006g291zo-6p-l

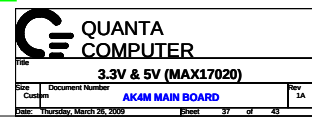
*LV@ICSP PIN HEADER
NEED TO CHANGE FOOTPRINT

LCD_ID[2,1,0]	LCD name
000	LTN160HT03-N01(Dual Ch)
001	LTN160AT04-N01
010	LTN160AT01-N02
011	LTN160HT03-0 (Dual Ch)
100	LTN154AT13-701(LED BL)
101	TBD
110	TBD
111	TBD

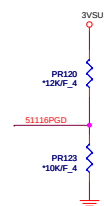
QUANTA
COMPUTER

Title	MCU PIC24FJ256GB106		
Size	Document Number	Rev	1A
Custom	AK4M MAIN BOARD		
Date:	Tuesday, March 24, 2009	Sheet	35 of 43

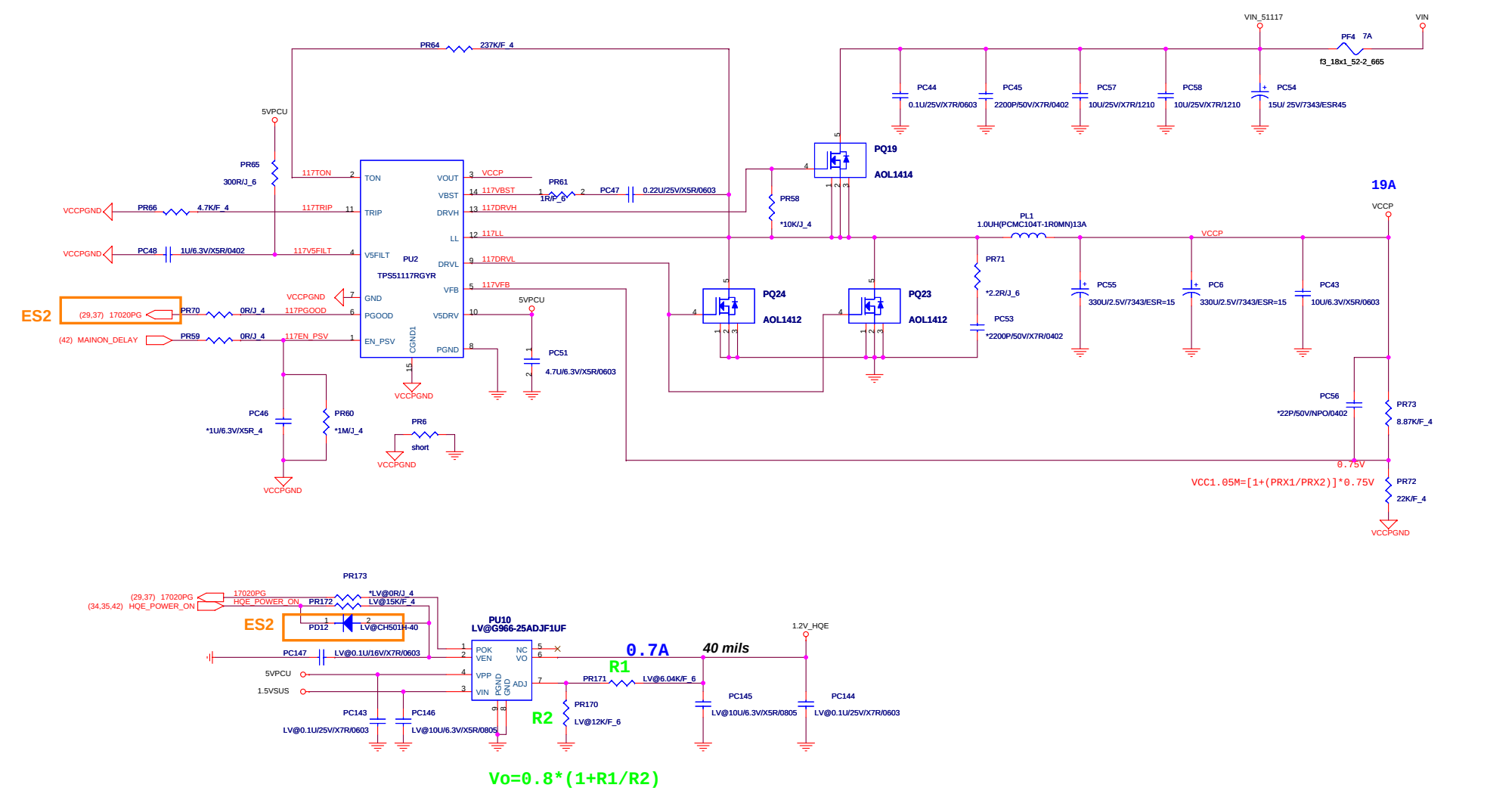


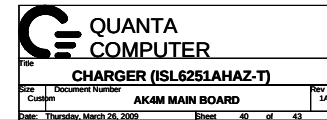


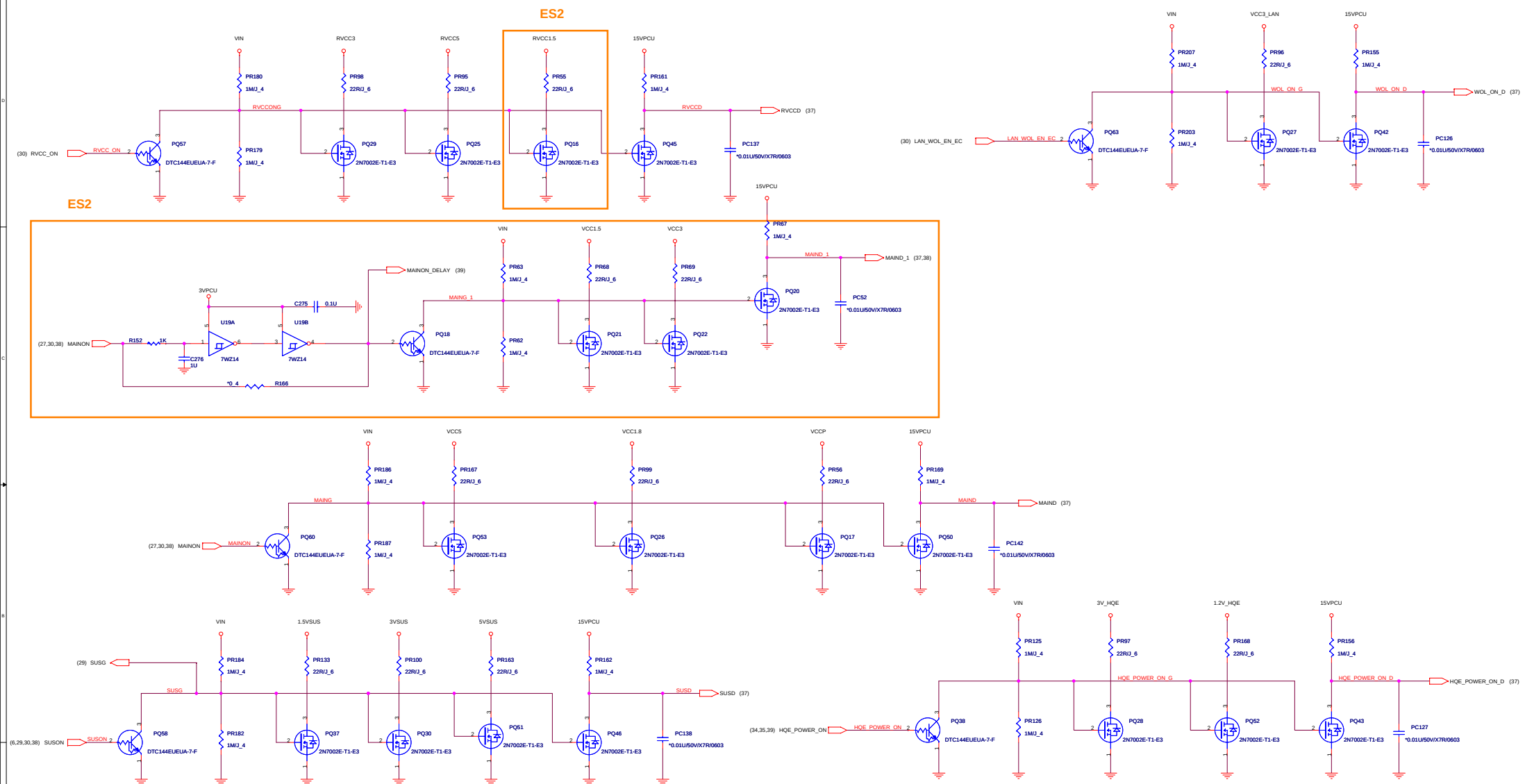
38



VCCP & 1.2V_HQE







CHANGE HISTORY

ES2
PAGE03:Del R500 to single load;exchange DREFSSCLK and CLK_PCIE_LAN for can not found LAN function
PAGE04:Del R5408 0 ohm for SMT request
PAGE06:Del R5275,R5298 0ohm,so change NET name;Add logic gate to control SM_PWROK;Del R5319 0ohm
PAGE08:Change VCCP_PCIE to VCCP
PAGE10:Del R5300,R5302,R5309,R5308,R5018,R5016,R5061,R5019,R5047 0ohm,Del Q5003
PAGE12:Del R5384 ohm
PAGE13:Change EXPRESS CARD to PORT#7
PAGE14:Del R5407,R5415,R5422 0ohm;Add GPIO LCD_ID2;Add LCD_ID2,H_PROCHOT_SB pull high;Add C650
PAGE15:Del R5429,R5426,L5021,L5020,R5139,R5431 for SMT request;Change 5VPCU,3VPCU to RVCC5,RVCC3
PAGE19:Add LCD_ID2
PAGE27:Change EXPCARD USB4 to USB7;Add Q49 for WAKE function;Del VCC3,R6385;Add logic gate to control RF_ON_BT
PAGE29:Change USBOC to 0,2;Change USBPWR to P0,P2;Change USB5_DISCHANGE to USBP_DISCHANGE;Change CN4 more pin define
PAGE30:Exchange CAP_LED,EC_BATLED;Change USB5_DISCHANGE to USBP_DISCHANGE;Del Q5084,Q5094,D5051,R6415;Change VCC5_LED to VCC3M_MINI
PAGE33:<1>Add Y1 oscillate 48Mhz for SUPER I/O
PAGE34:Change R349 to 10K;Add R313 to link LCDVCC_ON;Add R308 100K pull down
PAGE36:Change PR21 pull high to VCCP
PAGE37:Add PQ49 for RVCCD;Change PU9 to G1391T12U;Add PR153 100K ohm pull high for DDRPG;Add PD1
PAGE39:Change PU2-6 pin to 1702PG
PAGE40:Change PR199 to pull high 5VPCU;Change PU5 to G1391T12U
PAGE41:Add discharge circuit for MAIND_1
PAGE22: change AR41,AR42 to 56 ohm for NECP AUDIO team request
PAGE23: change AR6,AR7 to 12K for NECP AUDIO team request
PAGE24: change WLAN power supply from 3VSUS to VCC3.
PAGE42: Add discharge circuit for RVCC1.5
PAGE3: Add CAP 0.1U,1U for RICOH request
PAGE29: Change PIN8/10/12/41/43 of USB boad connector to improve USB(IPOD)signal quality
PAGE17: attach R6450 and remove R9109 for NECP request
PAGE17:No mount Q5060,R6463,C6239,C6239,C6240,Becuase BCM57780 internal has VR
PAGE18: Removing R9115/R6466 for NECP request
PAGE15:Change R105,R104 to 100 ohm &Mount C225,C224 unmount for VREF/VREF_SUS power sequence.
PAGE3-42:RENANE ALL PARTS
PAGE40:Add close battery connector for NECP request
PAGE40:Change PF9 location for NECP request
PAGE19:Change L19,L21,L23 to BLM18BA750SN1&Mount C251,C261,C265