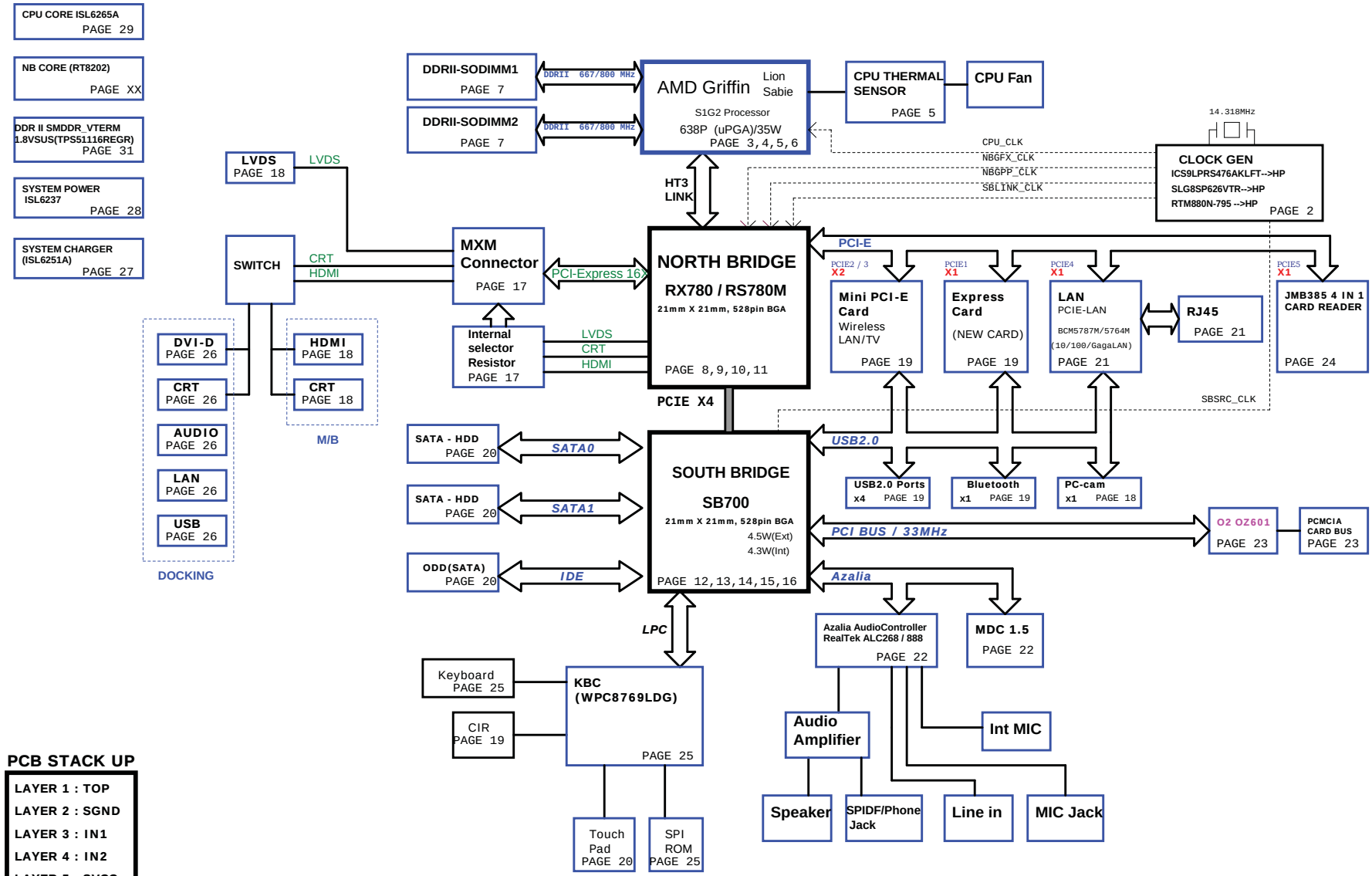
ZY7 SYSTEM BLOCK DIAGRAM

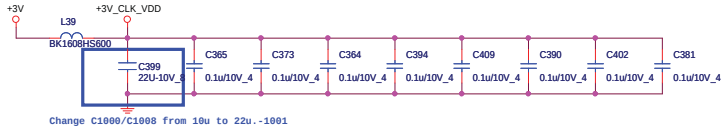


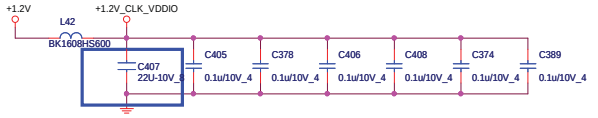
PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

Quanta Computer Inc.
PROJECT : ZY7
Size | Document Number: Block Diagram | Rev 1A
Date: Tuesday, November 27, 2007 | Sheet 1 of 35

CLK_GEN_SLG8SP628





ICS9LPRS480 P/N :

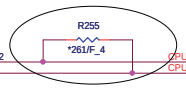
SLG8SP628 P/N : AL8SP628000

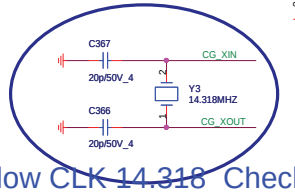
RTM880N-796 P/N : AL000880000

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

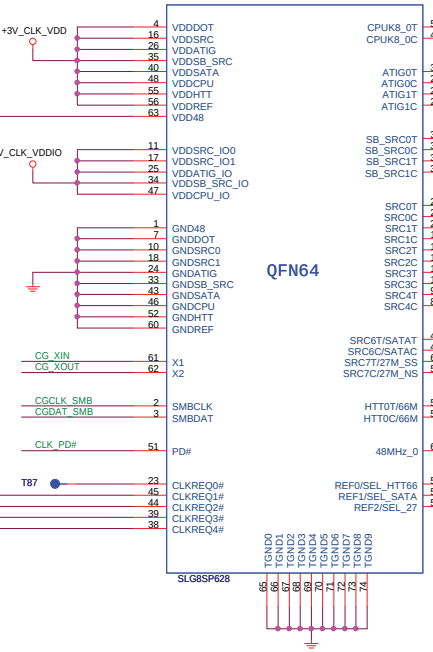
Place within 0.5" of CLKGEN

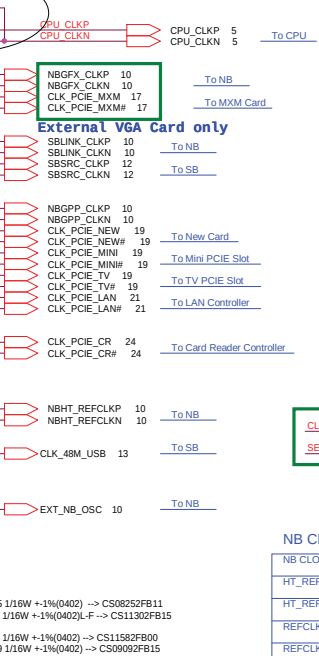
CHECK

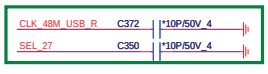




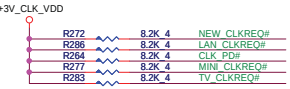
Follow CLK 14.318 Check 20p 11/19







Add for EMI.--1015



R1004/R1005 (value may change)

	NB_OSC
RX780	1.8V 82.5R/130R
RS780	1.1V 158R/90.9R

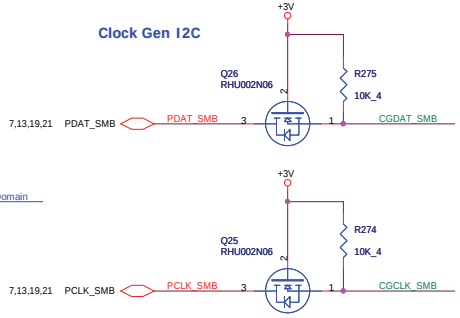
RES CHIP 82.5 1/16W +-1%(0402) --> CS08252FB11
RES CHIP 130 1/16W +-1%(0402)L-F --> CS11302FB15

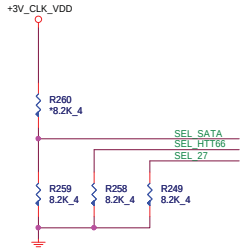
RES CHIP 158 1/16W +-1%(0402) --> CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) --> CS09092FB15

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

Clock Gen I2C





SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

Quanta Computer Inc.
PROJECT : ZY7

Size	Document Number	Rev
	CLOCK GENERATOR_SLG8SP628	1A

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8 HT_RXD#[15..0] HT_RXD#[15..0]
8 HT_RXD[15..0] HT_RXD[15..0]
8 HT_TXD[15..0] HT_TXD[15..0]
8 HT_TXD#[15..0] HT_TXD#[15..0]

PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

VLDT_RUN

U25A

HT LINK

D1	VLDT_A0		VLDT_B0	AE2	
D2	VLDT_A1		VLDT_B1	AE3	
D3	VLDT_A2		VLDT_B2	AE4	
D4	VLDT_A3		VLDT_B3	AE5	
HT_RXD0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	HT_TXD0
HT_RXD#0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	HT_TXD#0
HT_RXD1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	HT_TXD1
HT_RXD#1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	HT_TXD#1
HT_RXD2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	HT_TXD2
HT_RXD#2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	HT_TXD#2
HT_RXD3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	HT_TXD3
HT_RXD#3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	HT_TXD#3
HT_RXD4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	HT_TXD4
HT_RXD#4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	HT_TXD#4
HT_RXD5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	HT_TXD5
HT_RXD#5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	HT_TXD#5
HT_RXD6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	HT_TXD6
HT_RXD#6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	HT_TXD#6
HT_RXD7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	HT_TXD7
HT_RXD#7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	HT_TXD#7
HT_RXD8	E5	L0_CADIN_H8	L0_CADOUT_H8	AD4	HT_TXD8
HT_RXD#8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	HT_TXD#8
HT_RXD9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	HT_TXD9
HT_RXD#9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	HT_TXD#9
HT_RXD10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	HT_TXD10
HT_RXD#10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	HT_TXD#10
HT_RXD11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	HT_TXD11
HT_RXD#11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	HT_TXD#11
HT_RXD12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	HT_TXD12
HT_RXD#12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	HT_TXD#12
HT_RXD13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	HT_TXD13
HT_RXD#13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	HT_TXD#13
HT_RXD14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	HT_TXD14
HT_RXD#14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	HT_TXD#14
HT_RXD15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	HT_TXD15
HT_RXD#15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	HT_TXD#15
8 HT_CPU_UPCLK0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	HT_CPU_DWNCLK0 8
8 HT_CPU_UPCLK#0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	HT_CPU_DWNCLK#0 8
8 HT_CPU_UPCLK1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	HT_CPU_DWNCLK1 8
8 HT_CPU_UPCLK#1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	HT_CPU_DWNCLK#1 8
8 HT_CPU_UPCTL0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	HT_CPU_DWNCTL0 8
8 HT_CPU_UPCTL#0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	HT_CPU_DWNCTL#0 8
8 HT_CPU_UPCTL1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	HT_CPU_DWNCTL1 8
8 HT_CPU_UPCTL#1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	HT_CPU_DWNCTL#1 8

C519 4.7u/6.3V_6

Athlon 64 S1g2 SOCKET_638_PIN

Athlon 64 S1g2
Processor Socket
SOCKET_638_PIN

NO STUB for HT3

R135 *51_4
R133 *51_4

VLDT_RUN

HOLE27 MDC_HOLE
HOLE28 MDC_HOLE
HOLE11 MINI_HOLE
HOLE13 MINI_HOLE
HOLE9 CPU_HOLE
HOLE16 CPU_HOLE
HOLE19 CPU_HOLE
HOLE17 CPU_HOLE
HOLE8 MXM_HOLE
HOLE10 MXM_HOLE
HOLE20 MXM_HOLE
HOLE7 MXM_HOLE
HOLE6 MXM1_HOLE
HOLE21 MXM1_HOLE

HOLE14 *H-C295D118P2
HOLE5 *H-C295D118P2
HOLE2 *H-C295D118P2
HOLE23 *H-C295D118P2
HOLE4 *H-C295D118P2
HOLE35 *H-C295D118P2
HOLE25 *H-C295D118P2
HOLE24 *H-C295D118P2
ADOGND
HOLE32 *H-C295D118P2
HOLE34 *H-C295D118P2
HOLE33 *H-C295D118P2
HOLE1 *H-C295D118P2
HOLE15 *NONP_HOLE1
HOLE12 *NONP_HOLE2
HOLE3 *H-C295D118P2

HOLE26 ODD1_HOLE
HOLE30 ODD1_HOLE
HOLE31 HDD1_HOLE
HOLE29 HDD1_HOLE
HOLE22 HDD2_HOLE
HOLE18 HDD2_HOLE

+1.2V
VLDT_RUN
L50 FBJ3216HS800_1206
L54 FBJ3216HS800_1206

Note:on MCP77,(HT=+1.1V) and CPU(HT=+1.2V) and therefore cannot be connected to the same HT power rail.

80 ohm(4A)
C555 4.7u/6.3V_6
C560 4.7u/6.3V_6
C569 .22U_4
C527 .22U_4
C522 180P_4
C565 180P_4

LAYOUT: Place bypass cap on topside of board

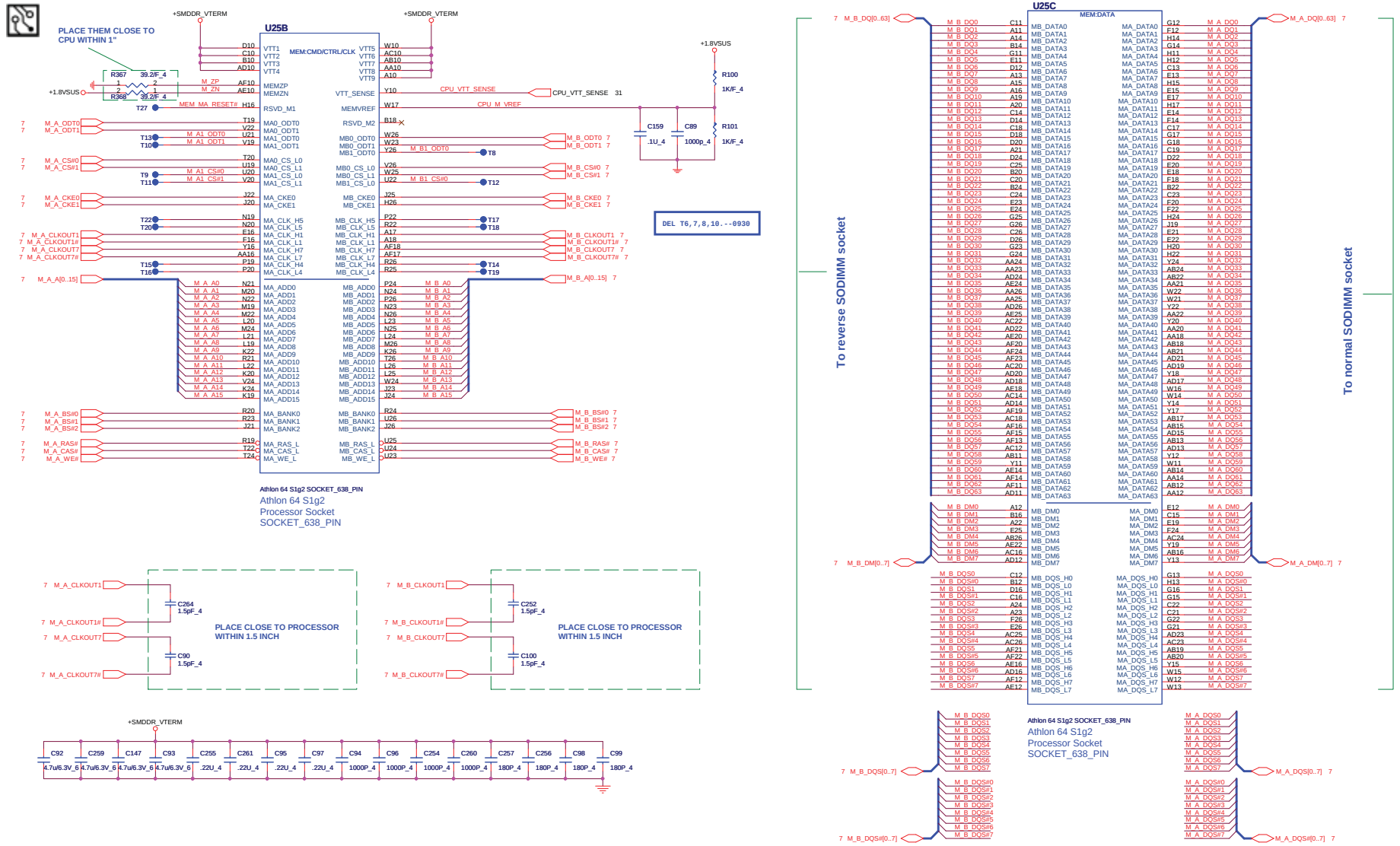
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

Quanta Computer Inc.
PROJECT : ZY7

Size	Document Number	Rev
	AMD Griffin HT I/F	1A
Date: Tuesday, November 27, 2007	Sheet 3 of 35	

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

Processor DDR2 Memory Interface



Quanta Computer Inc.	
PROJECT : ZY7	
Size	Document Number: AMD Griffin DDRII MEMORY I/F — Rev 1A
Date: Tuesday, November 27, 2007	Sheet 4 of 35

ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 390- (±5%) pulldown to VSS.

390 Ohm

Need Check .-1001

11/19

connect to CPU CORE power FB

place them to CPU within 1.5"

Keep trace from resisor to CPU within 0.6"
Keep trace from caps to CPU within 1.2"

DEL Pull H/L RES.--0930

route as differential as short as possible testpoint under package

Athlon 64 S1g2 Processor Socket SOCKET_638_PIN

connect to CPU CORE power controlier

VID Override Circuit

Add pull up

VFIX MODE

SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

HDT CONNECTOR

CPU H/W MONITOR

15 MIL

Address 98H

To SB GPIO

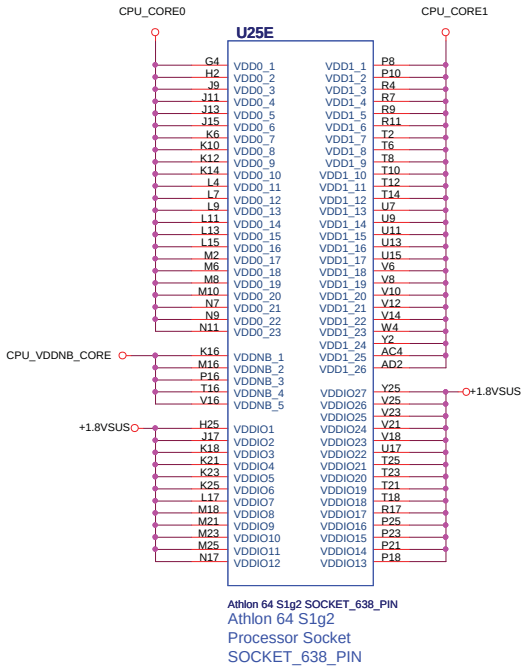
To FAN

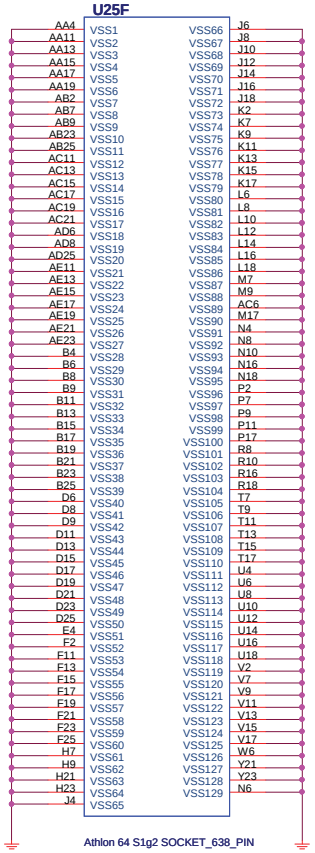
10 mil trace /
10 mil space

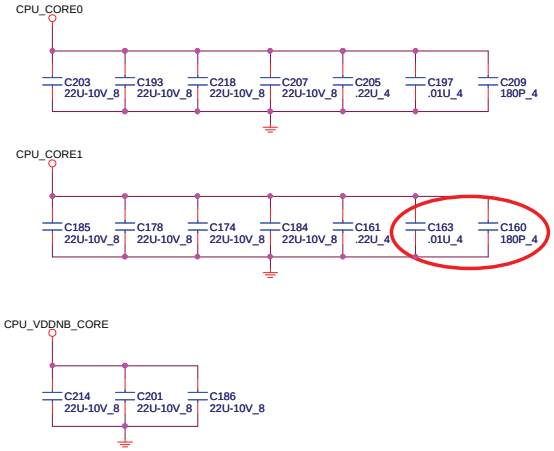
Quanta Computer Inc.
PROJECT : ZY7

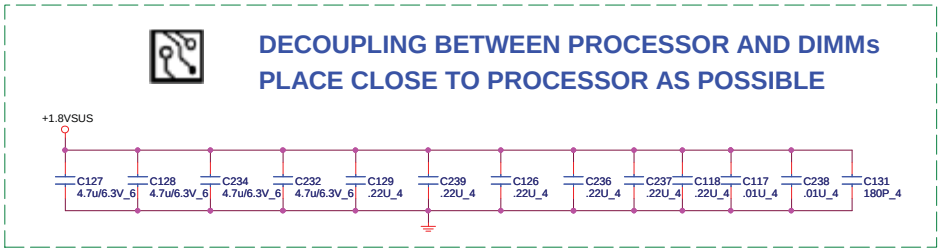
Size	Document Number	Rev
	AMD Griffin CTRL & DEBUG	1A
Date: Tuesday, November 27, 2007	Sheet 5 of 35	

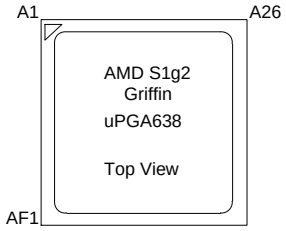
PROCESSOR POWER AND GROUND









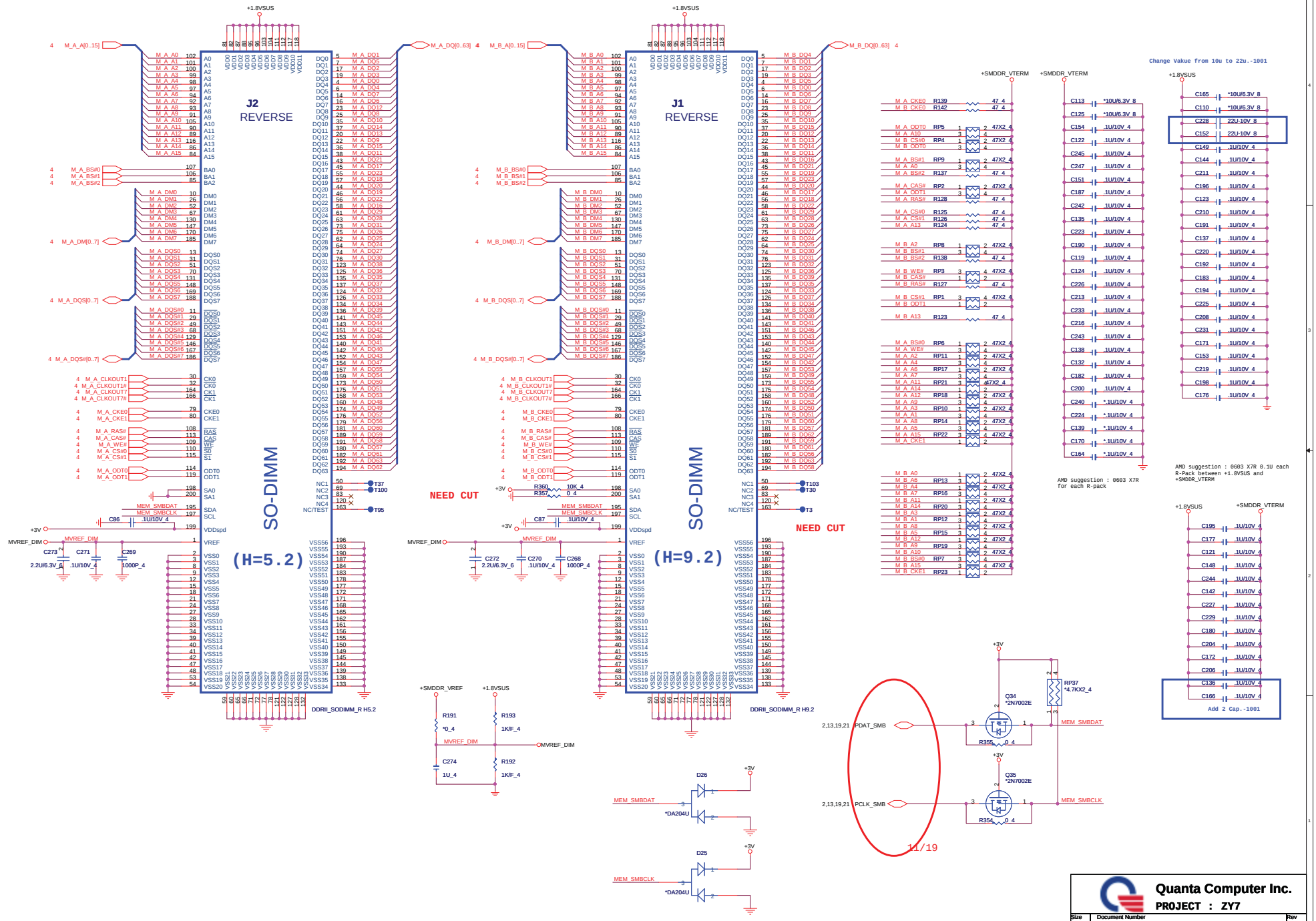


Quanta Computer Inc.

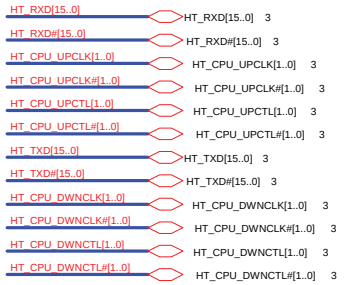
PROJECT : ZY7

Size	Document Number	Rev
	AMD Griffin PWR & GND	1A

Date: Tuesday, November 27, 2007 Sheet 6 of 35

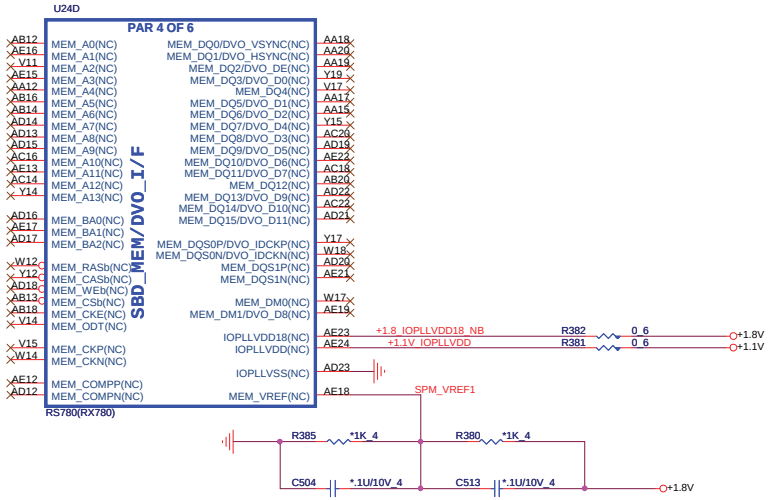


Quanta Computer Inc.
PROJECT : ZY7
Size | Document Number: DDR-II SODIMM*2 | Rev 1A
Date: Tuesday, November 27, 2007 | Sheet 7 of 35



signals	RS780	RX780
HT_TXCALP	R641 301ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R661 301 ohm 1%	R661 1.21k ohm 1%
HT_RXCALN		

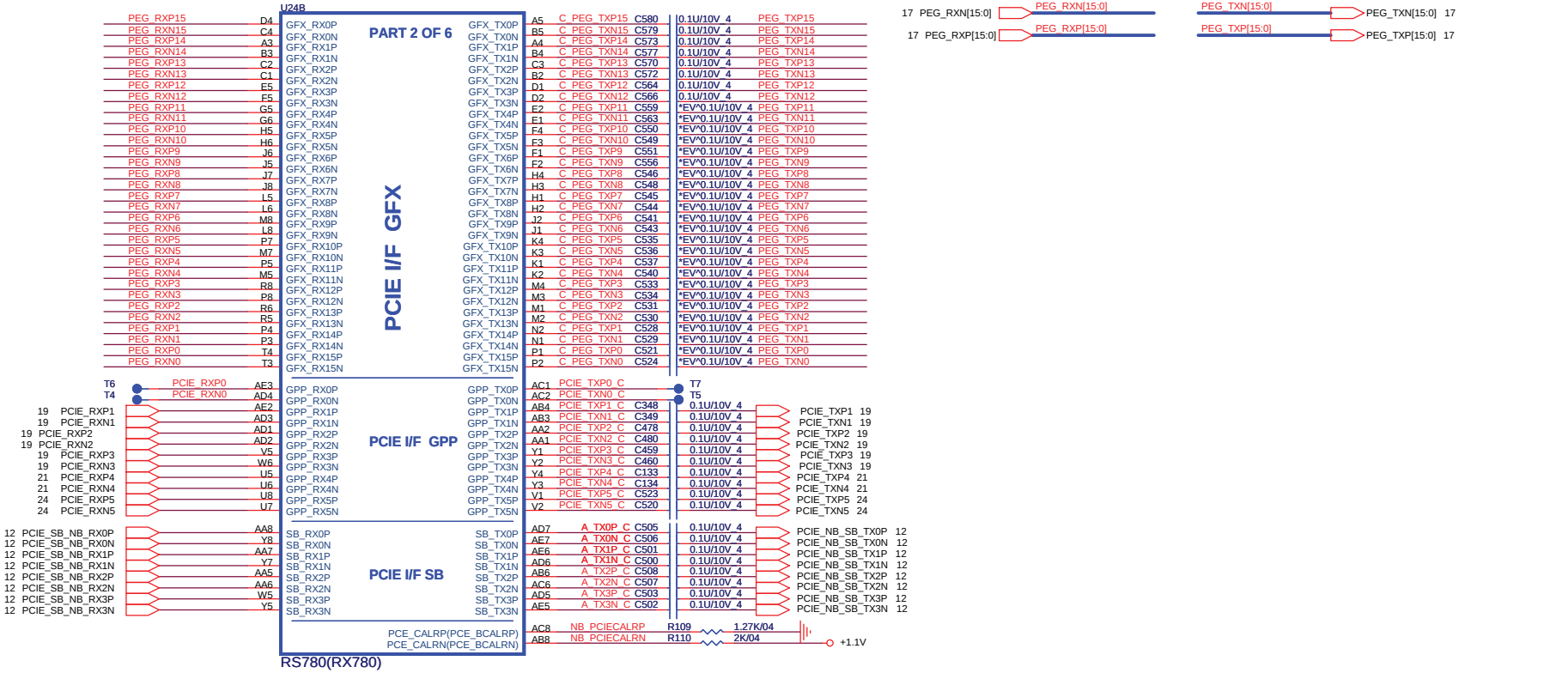
This block is for UMA RS780 only , RX780 can remove all component



Quanta Computer Inc.
PROJECT : ZY7

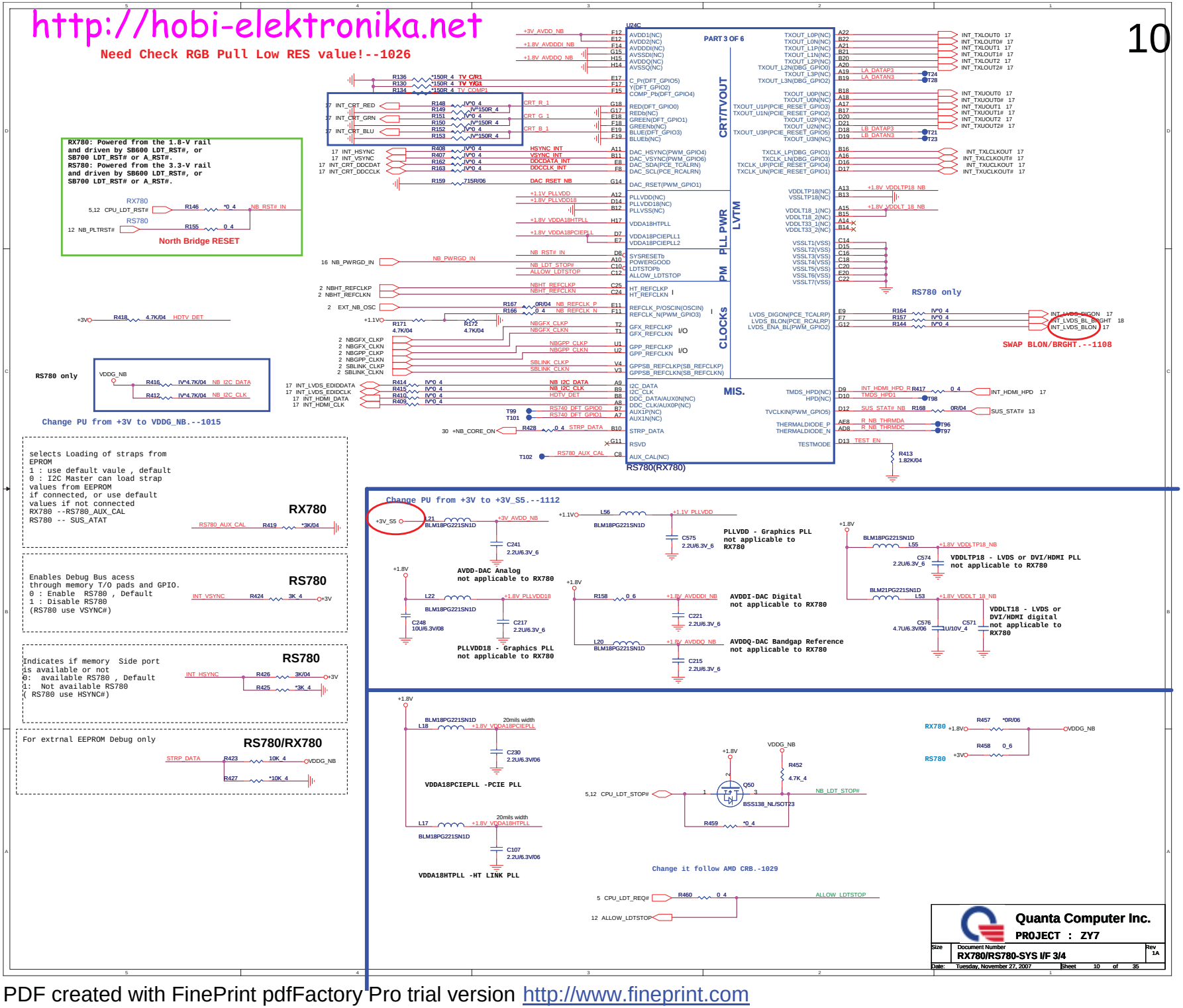
Size	Document Number	Rev
	RS740/RS780-HT LINK I/F 1/4	1A

Date: Tuesday, November 27, 2007 Sheet 8 of 35

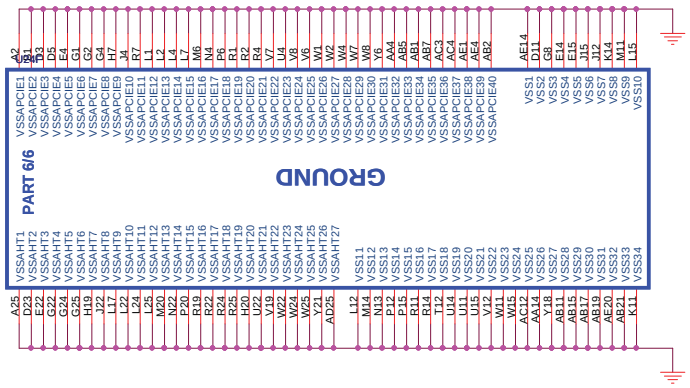


Quanta Computer Inc.		
PROJECT : ZY7		
Size	Document Number: RX780/RS780-PCIE I/F 2/4	Rev: 1A
Date: Tuesday, November 27, 2007	Sheet 9 of 35	

Need Check RGB Pull Low RES value!--1026

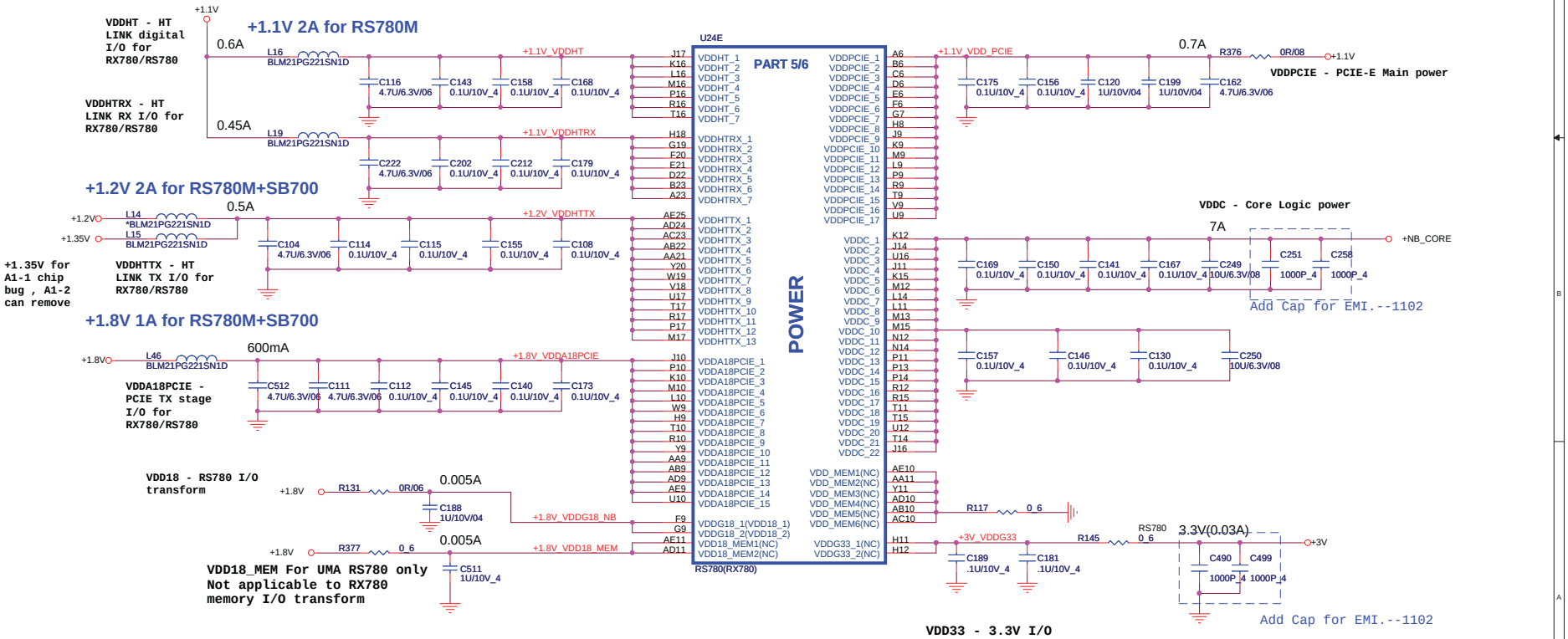


Quanta Computer Inc.
PROJECT : ZY7
Size | Document Number: RX780/RS780-SYS I/F 3/4 | Rev 1A
Date: Tuesday, November 27, 2007 | Sheet 10 of 35



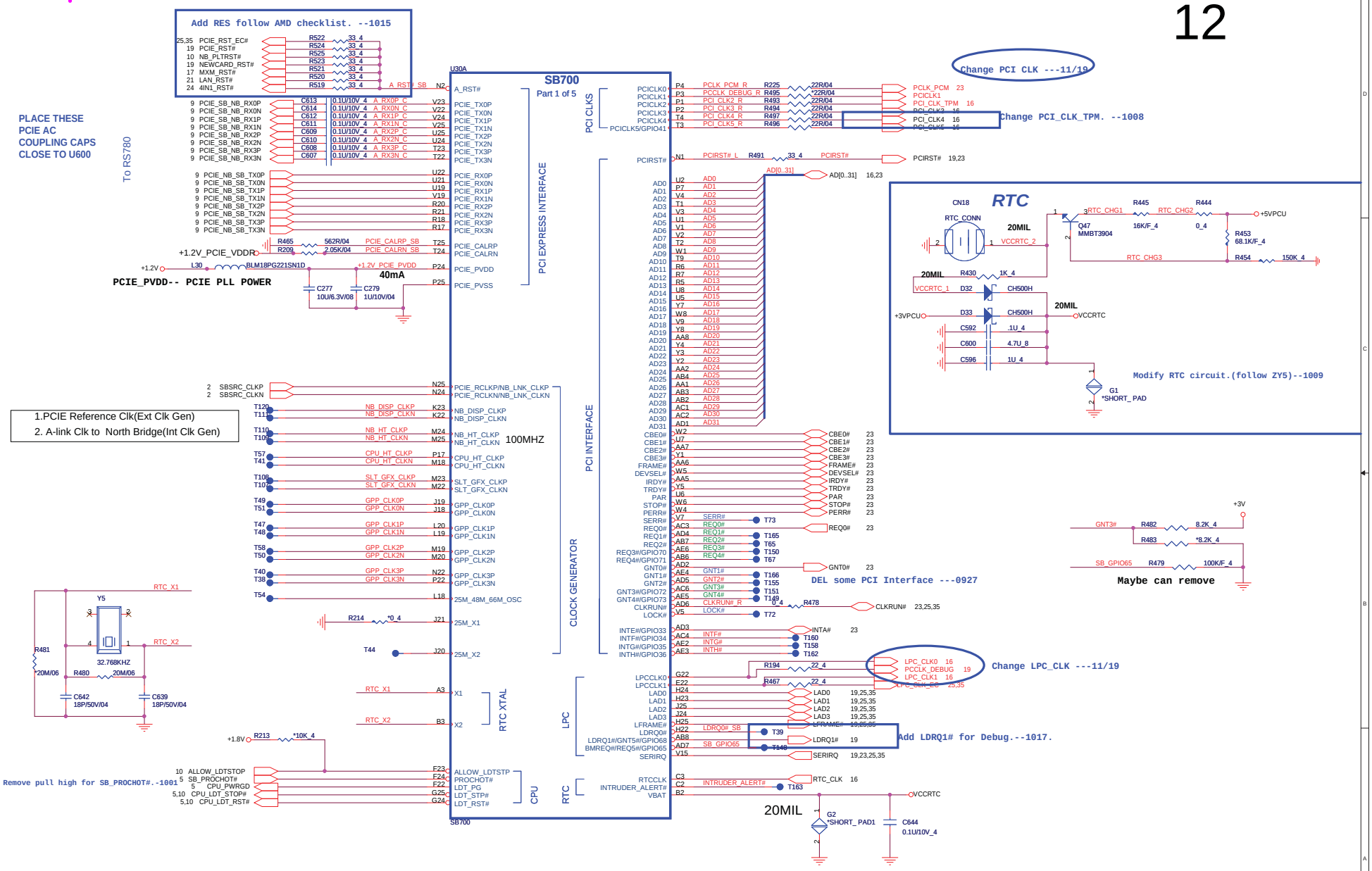
RX780/RS780 POWER DIFFERENCE TABLE

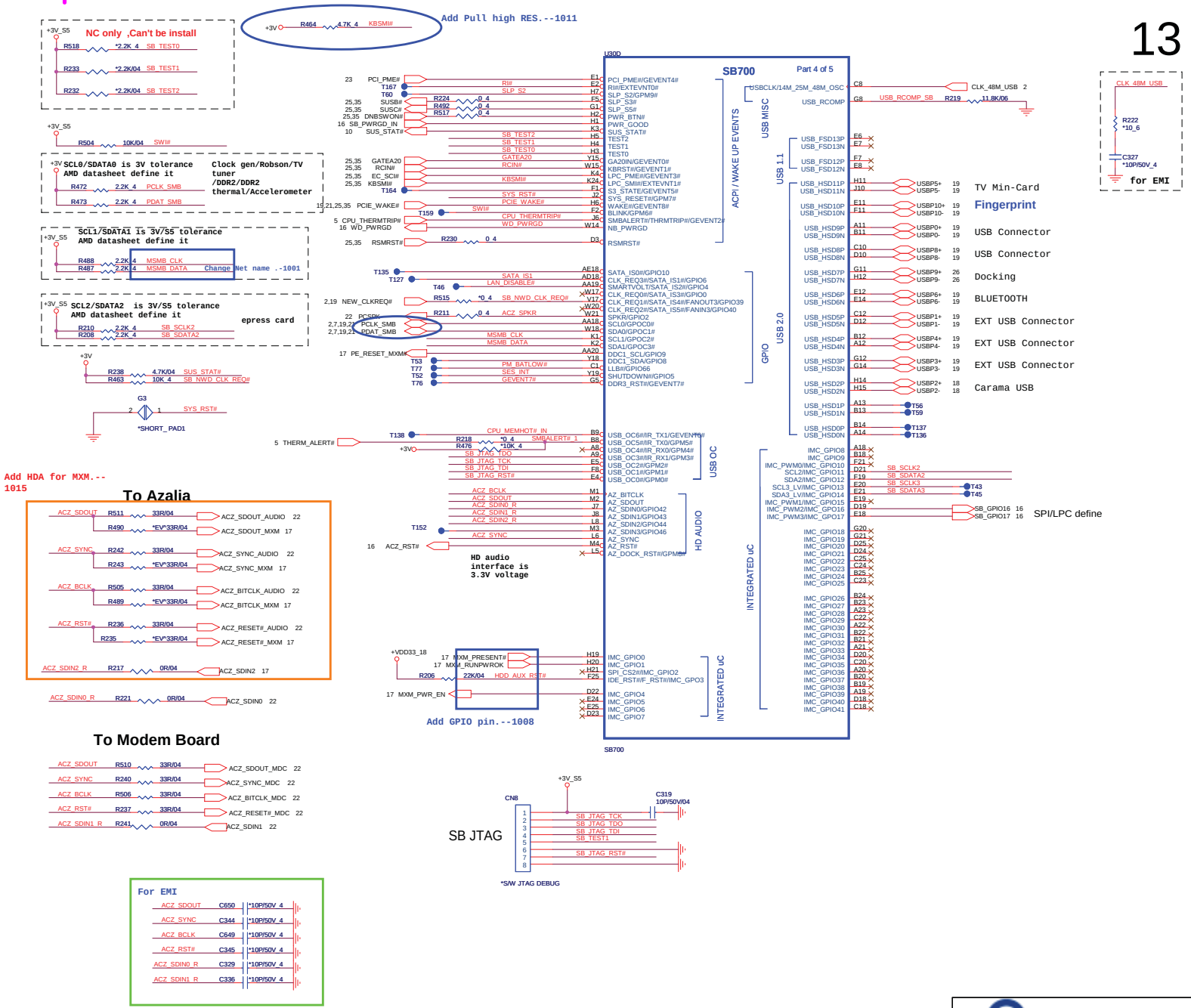
PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC



Quanta Computer Inc.
PROJECT : ZY7

Size	Document Number	Rev
	RX780/RS780-POWER 4/4	1A
Date: Tuesday, November 27, 2007	Sheet 11 of 35	





Quanta Computer Inc.	
PROJECT : ZY7	
Size	Document Number: SB700-ACPI/GPIO/USB 2/4 — Rev: 1A
Date: Tuesday, November 27, 2007	Sheet 13 of 35

SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO SB600

U30B

SB700
Part 2 of 5

SATA1

SATA2

SATA ODD

SERIAL ATA

ATA 66/100/133

SPI ROM

SATA PWR

HW MONITOR

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

Del RF_OFF#, EC will Control it----0925

DEL WAN_OFF# for ROBSON Portion----0925

DEL ACCLED_EN NET----0925

DEL BT_COMBO_EN# NET----0925

BOARD_ID0
BOARD_ID1
BOARD_ID2
BOARD_ID3
BOARD_ID4

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB700

NOTE:
R361 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

PLVDD_SATA-- SATA PLL POWER

XTLVDD_SATA-- SATA crystal power

Del CHIPSET_PCIE_SLOW_SB# Net----0925

Change from +3V to +3V_S5.--1012

AVDD--H/W monitor Analog power

5mA

77mA

1mA

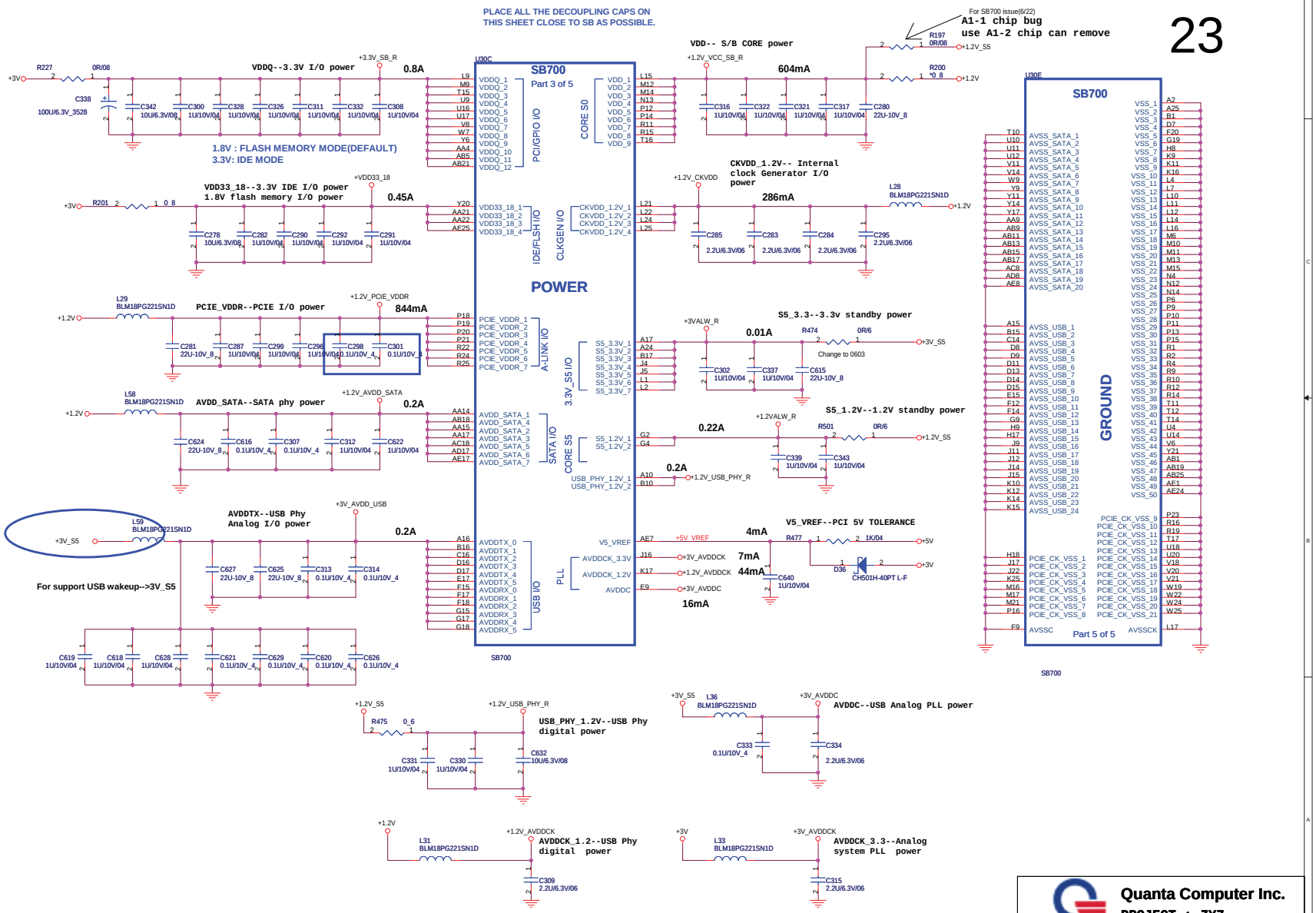
(1.2V @ 60mA)

(3.3V @ 1.2mA)

Place near ball

U9 TC7SH08FU

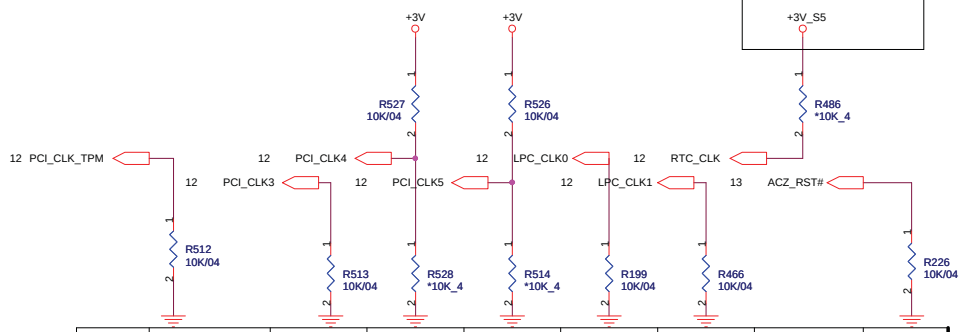
SB700



Quanta Computer Inc.
PROJECT : ZY7
Size | Document Number: SB700-PWR/DECOUPLING 4/4 | Rev: 1A
Date: Tuesday, November 27, 2007 | Sheet 15 of 35

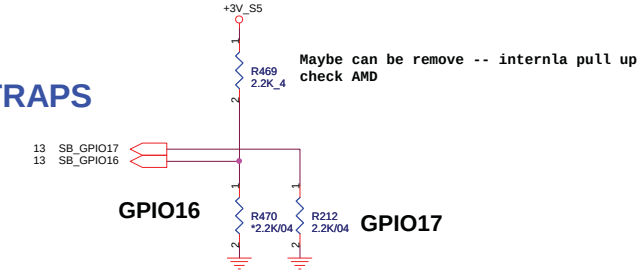
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#



	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT

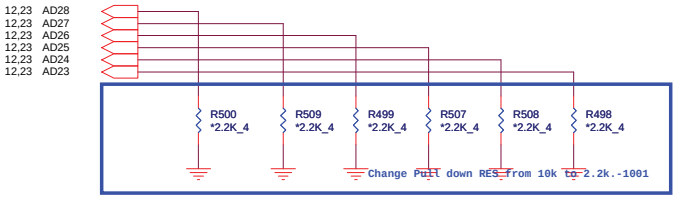
REQUIRED STRAPS



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

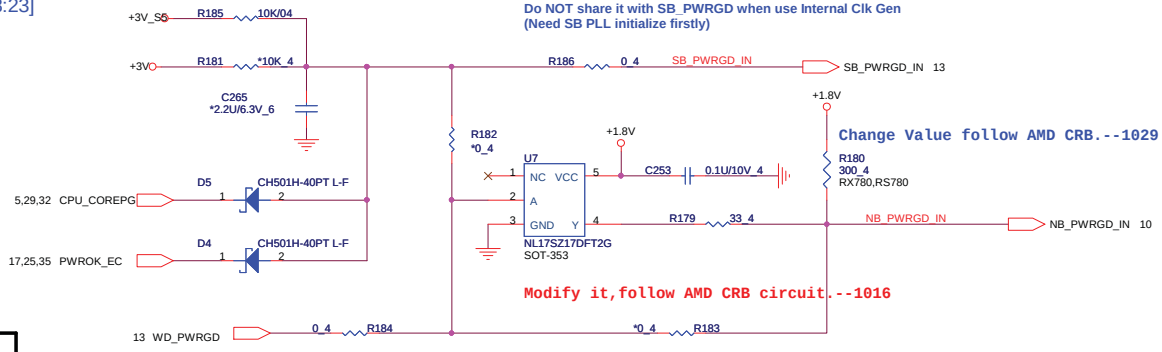
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



A11 no stuff R239,A12 Stuff R239,NO Stuff U11

NB/SB POWER GOOD CIRCUIT

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

Quanta Computer Inc.
PROJECT : ZY7

Size	Document Number	Rev
	SB700-STRAPS,PWRGD	1A
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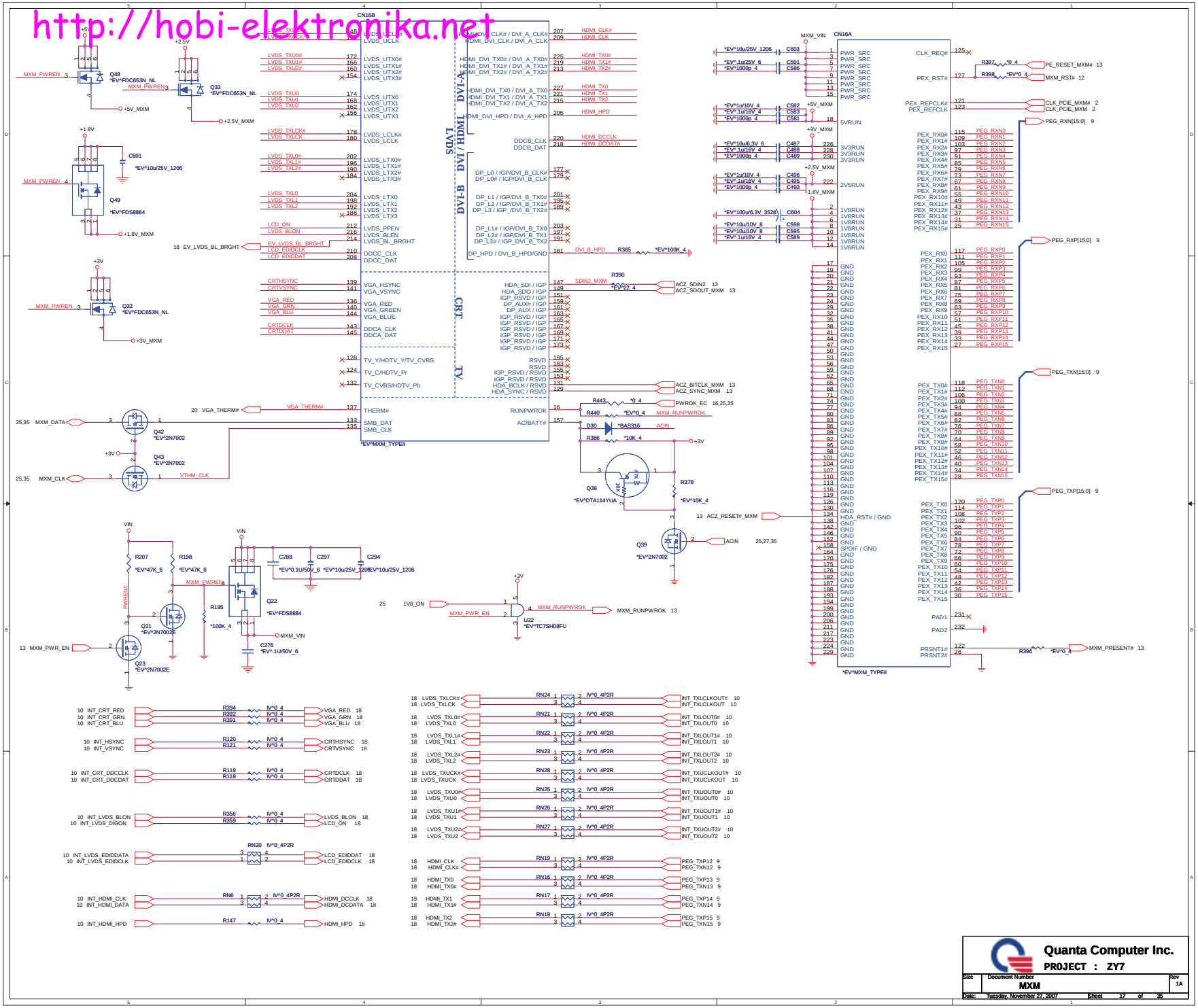
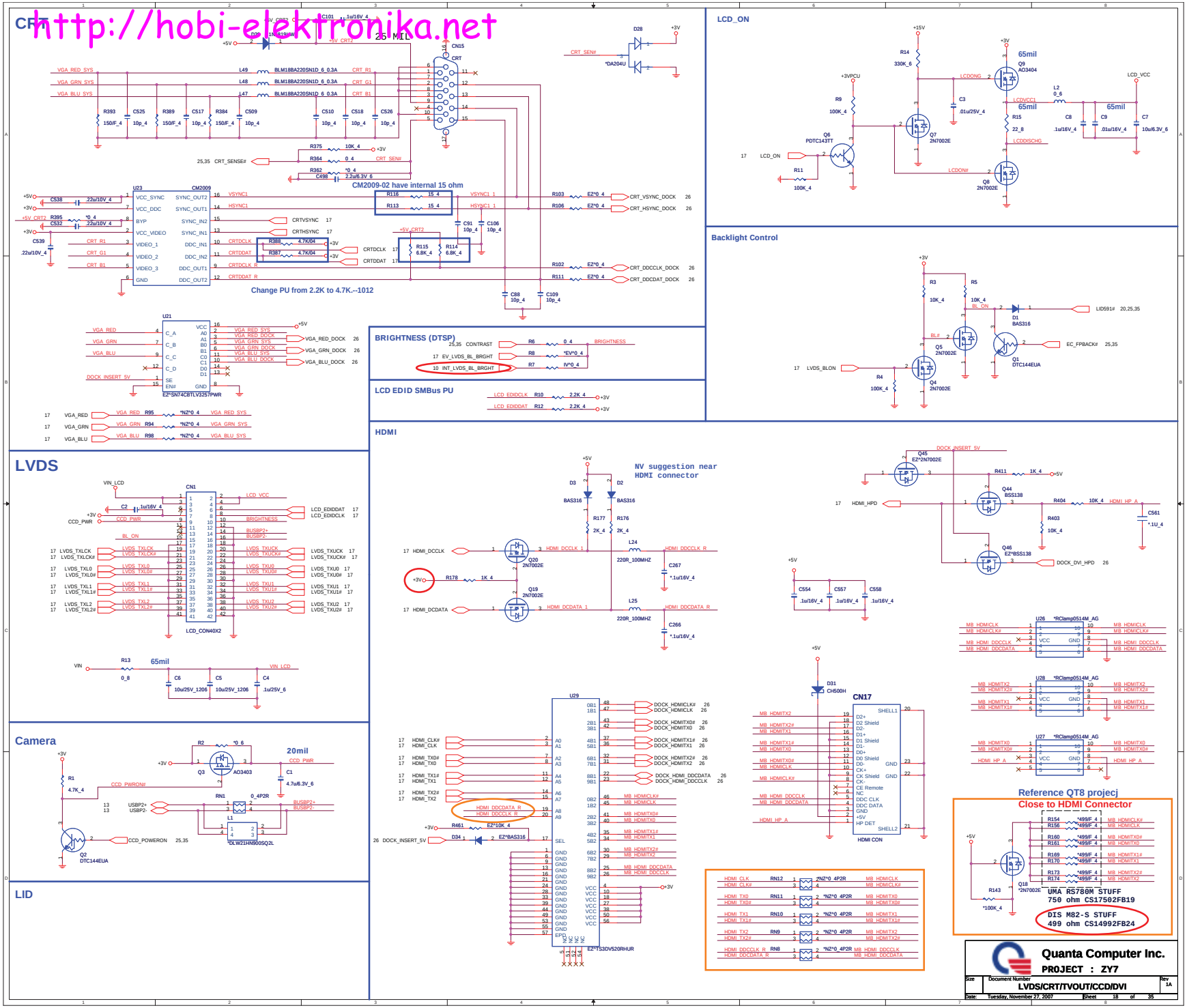
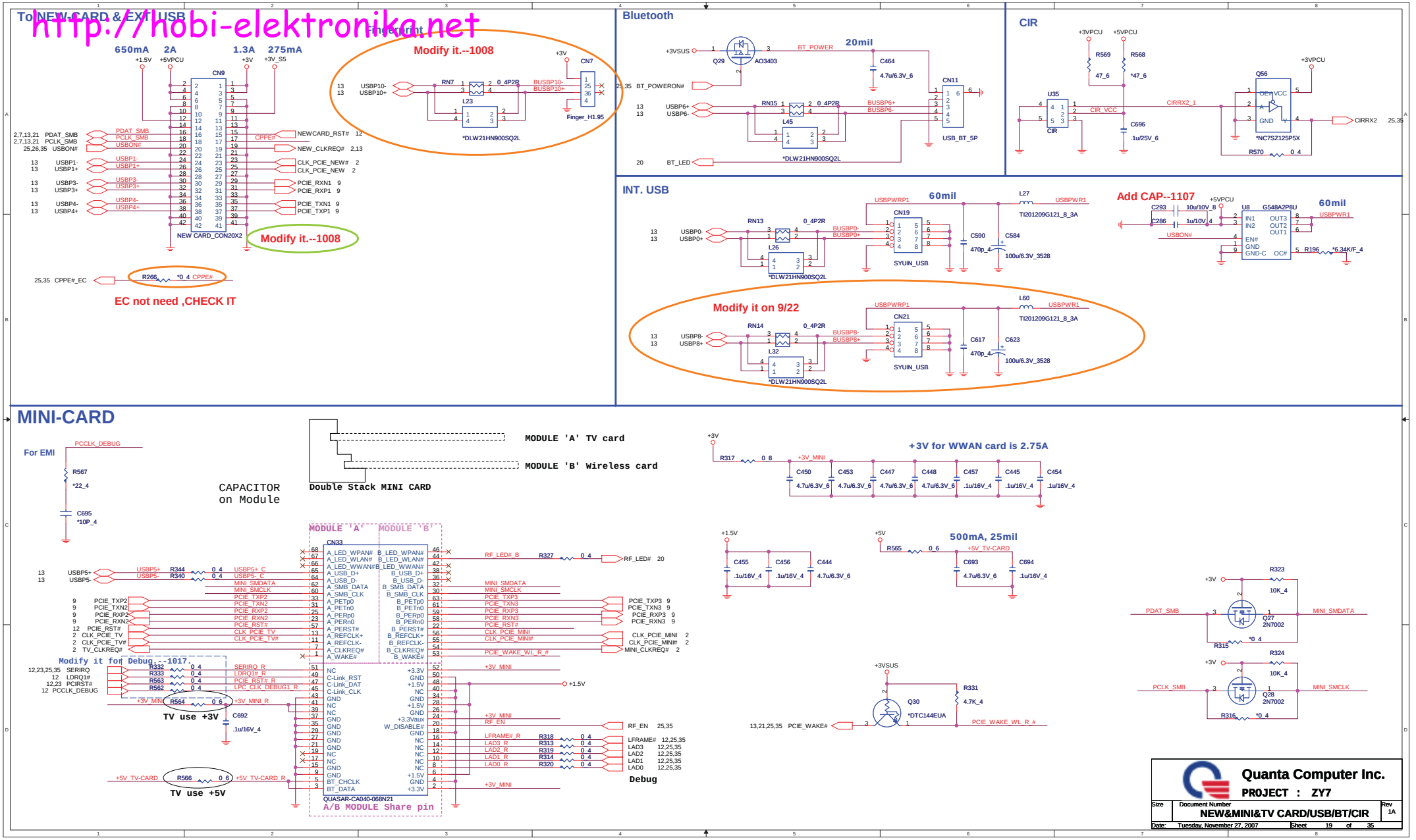
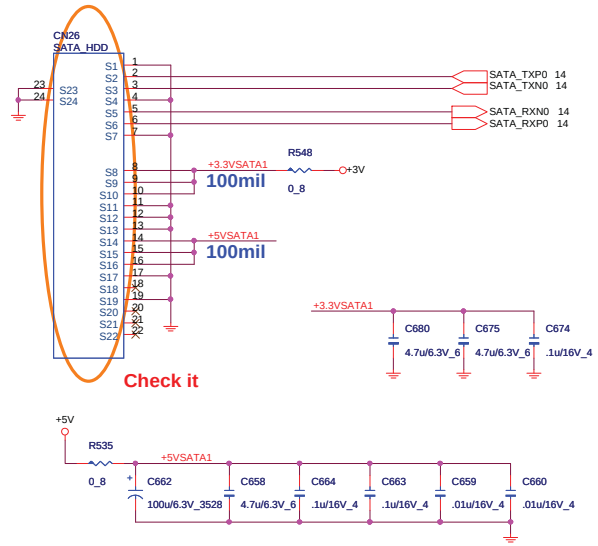


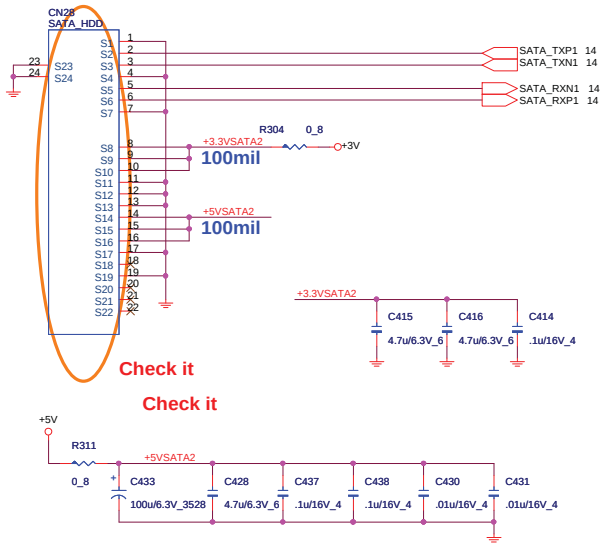




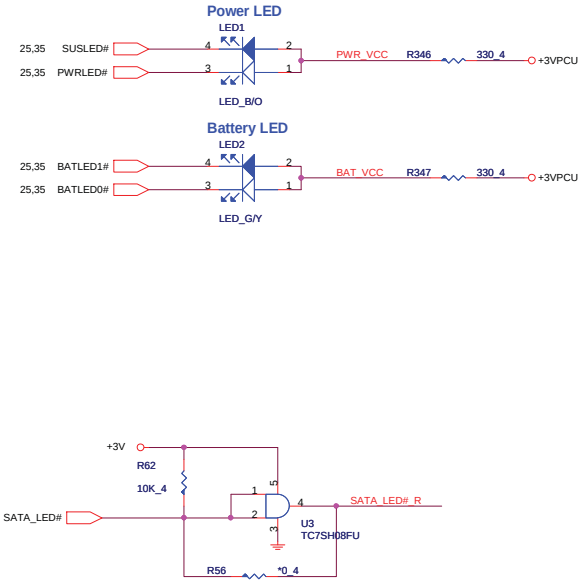
SATA1



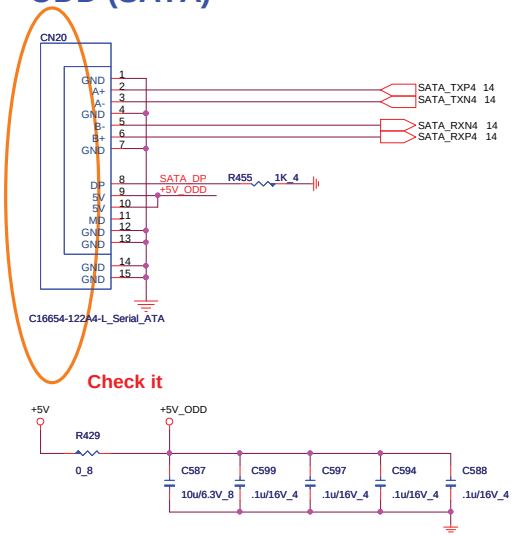
SATA2



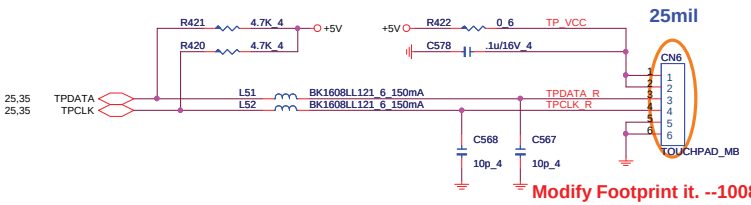
LED



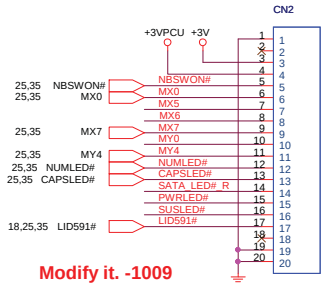
ODD (SATA)



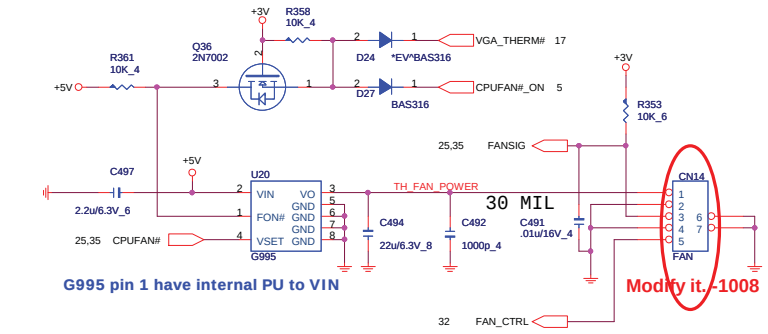
TP CONN



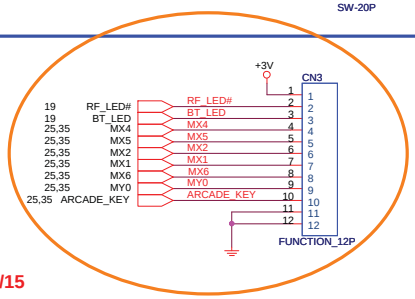
To Power/B



FAN



To Switch/B



Quanta Computer Inc.		
PROJECT : ZY7		
Size	Document Number: HDD/ODD/LED/SW/TP/FAN	Rev: 1A
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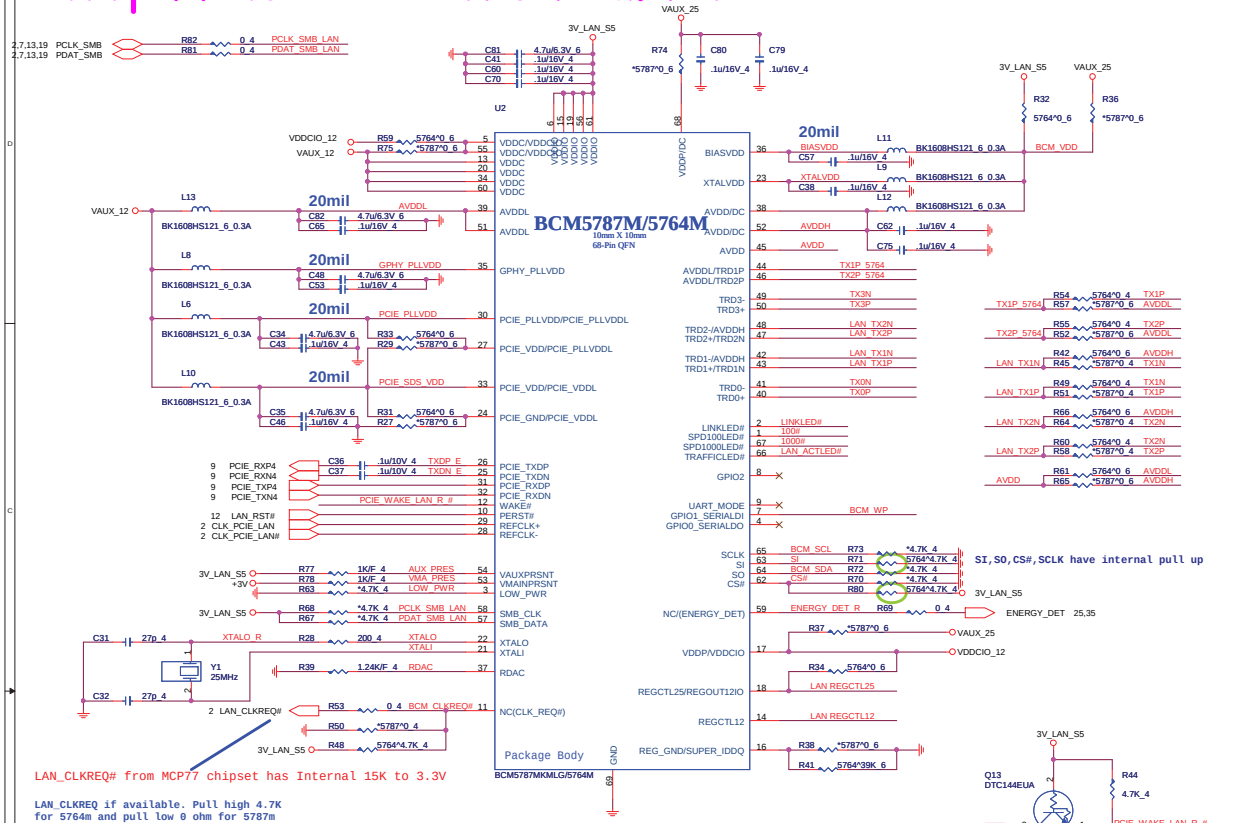
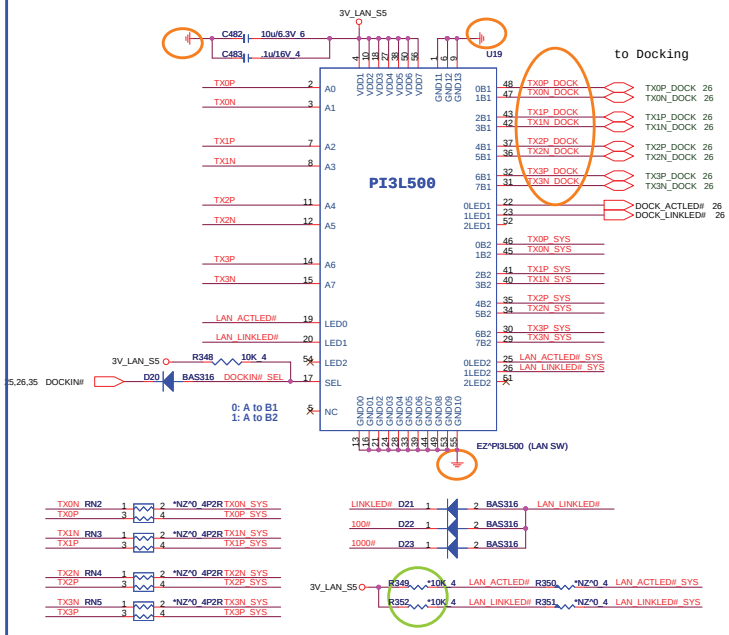
GigaLAN BCM5787M/5764M



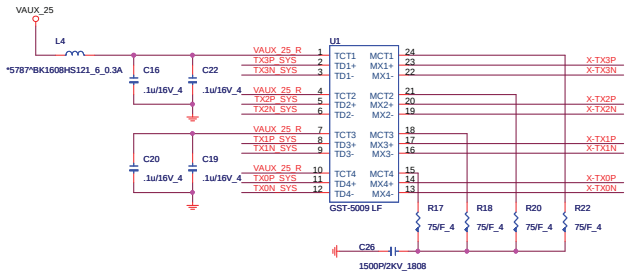
LAN SWITCH



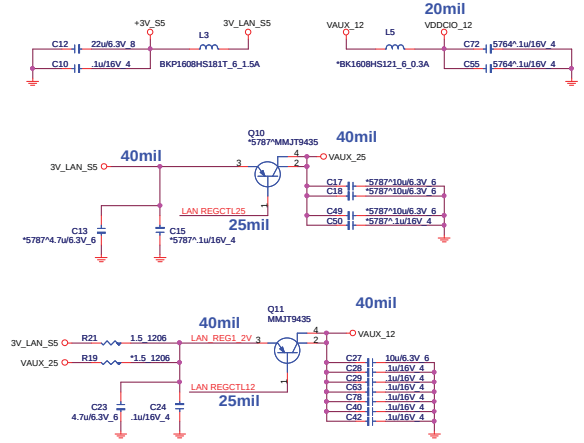
Transfomer

Source 1: DELTA LFE9249 DB0ZR1LAN11

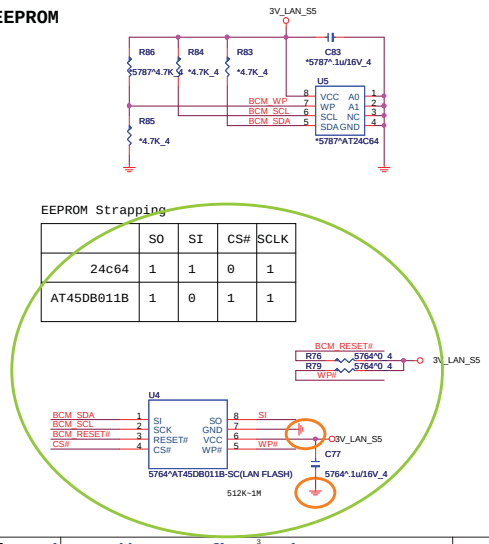
Source 2: Bothand GST5009 DBKN1NLAN03



LAN POWER



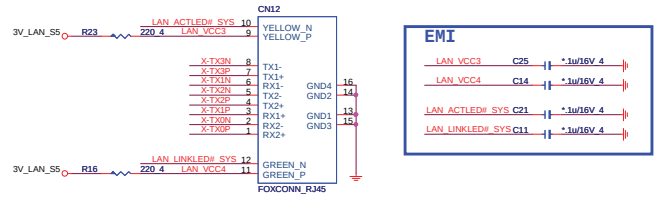
EEPROM



EEPROM Strapping

	SO	SI	CS#	SCLK
24c64	1	1	0	1
AT45DB011B	1	0	1	1

RJ45 connector



Quanta Computer Inc.

PROJECT : ZY7

Size	Document Number	Rev
	GigaLAN BCM5787M/5764M & RJ45	1A

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CODEC

ALC268/ALC888S-VC

Audio Amplifier

MAX9789A TQFN 32PIN

MUTE

SUBWOOFER

LINE OUT/SPDIF

Modify Footprint.-- 9/28

Normal OPEN Jack

TO DOCKING

ESD

LINE IN

Change value from 0 to 75 ohm.--1016

Normal OPEN Jack

MIC

Normal OPEN Jack

MDC

INT MIC.

Check Footprint it

SPEAKER

VR

Add PU +1.5V.--1016

60mil

Pls Close U19.

Add JP for EMI.--1112

Tied at one point only under the codec or near the codec

GAIN2	GAIN1	GAIN
0	0	6dB
1	0	10dB
0	1	15.6dB
1	1	21.6dB

Quanta Computer Inc.
PROJECT : ZY7
CODEC/AMP/MDC
Rev 1A
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http://hobi-elektronika.net

NOTE: IDSEL SELECTION!

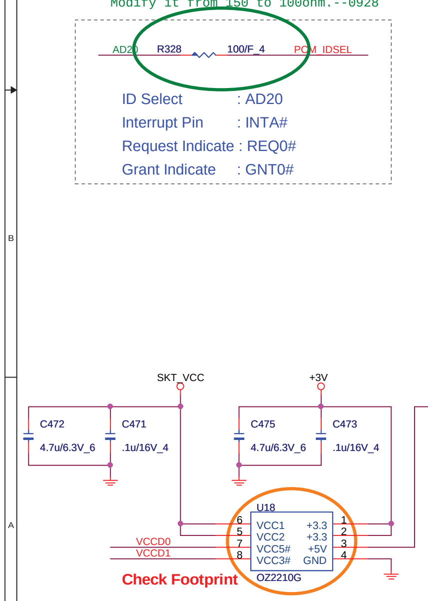
THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME. IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

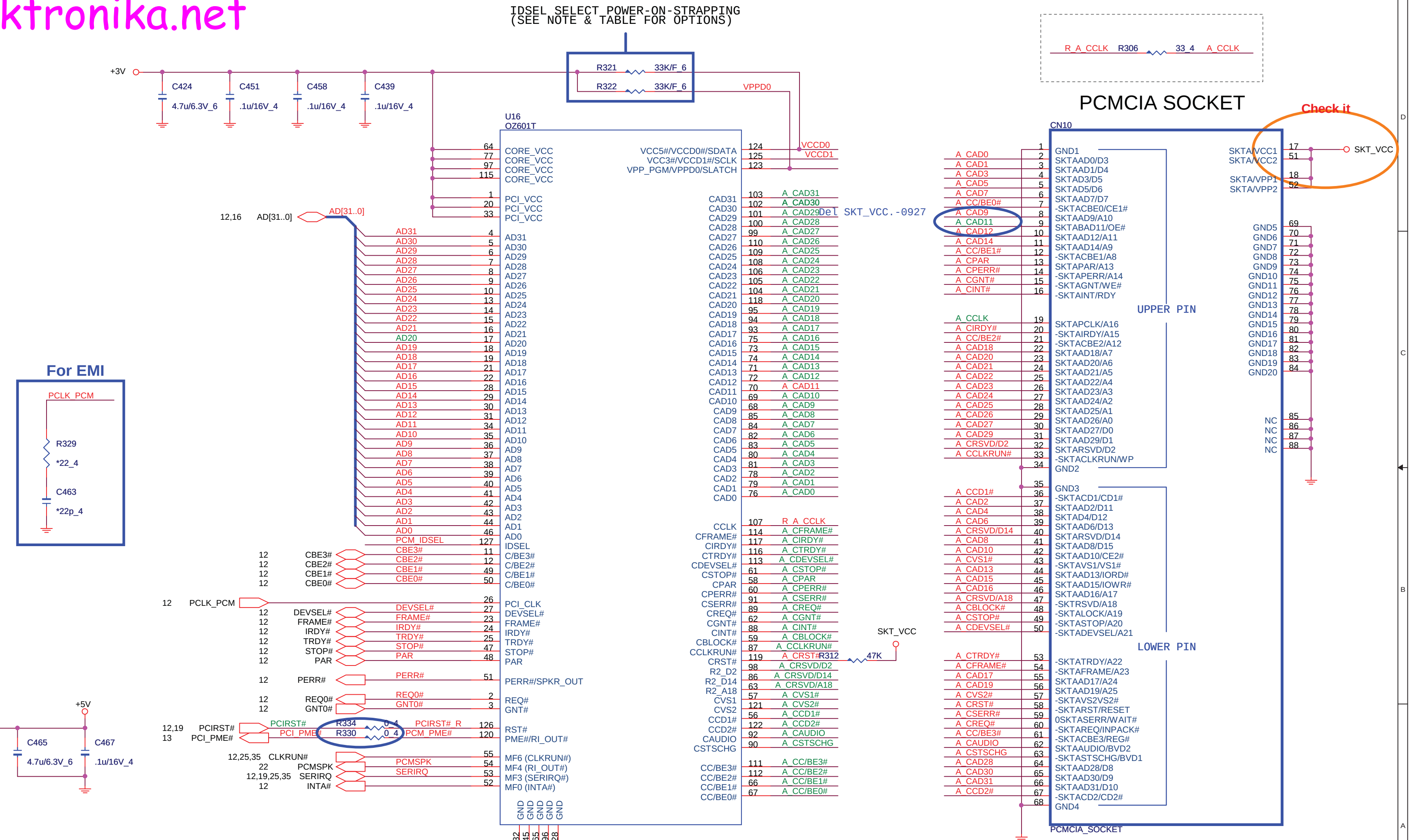
22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS. THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

Modify it from 150 to 100ohm.--0928





22K TO 47K PULL-UPS MUST BE PLACED ON INTA#, PME#, SERIRQ# & CLKRUN#.

Quanta Computer Inc.

PROJECT : ZY7

Size	Document Number	Rev
	PCMCIA(OZ601)	1A
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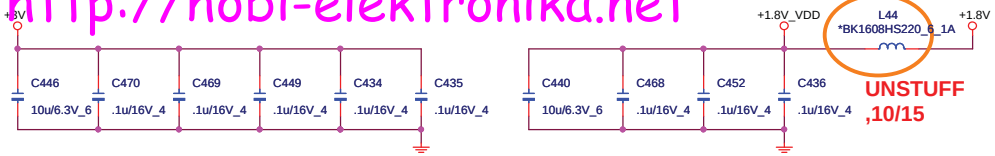
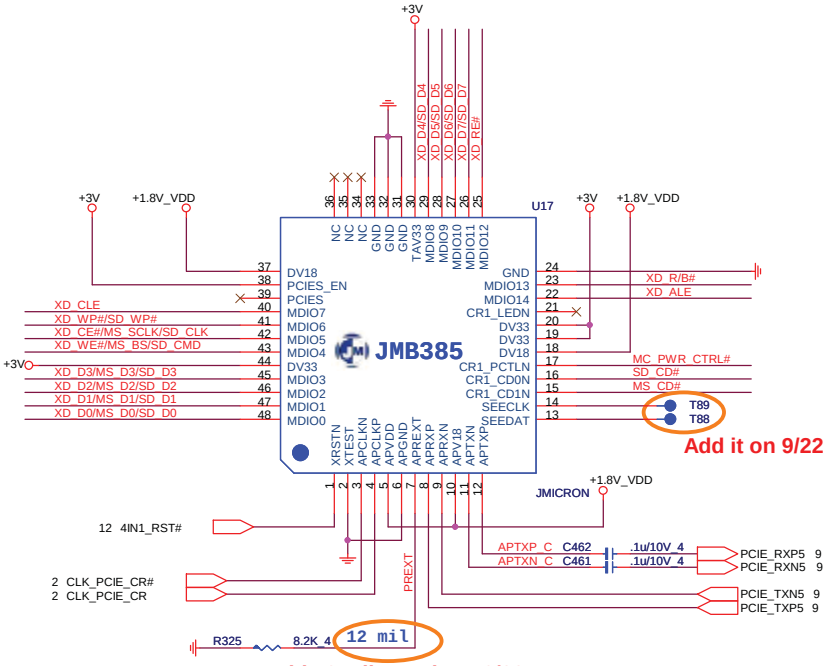
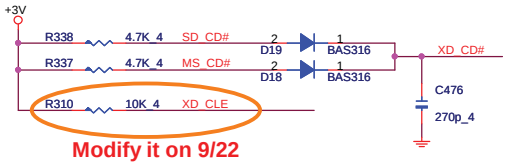
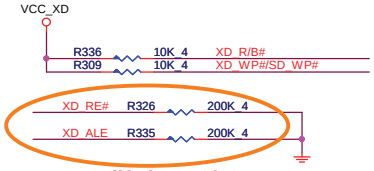
4 IN 1 CARD READER

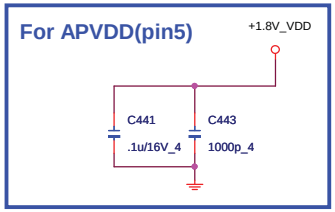


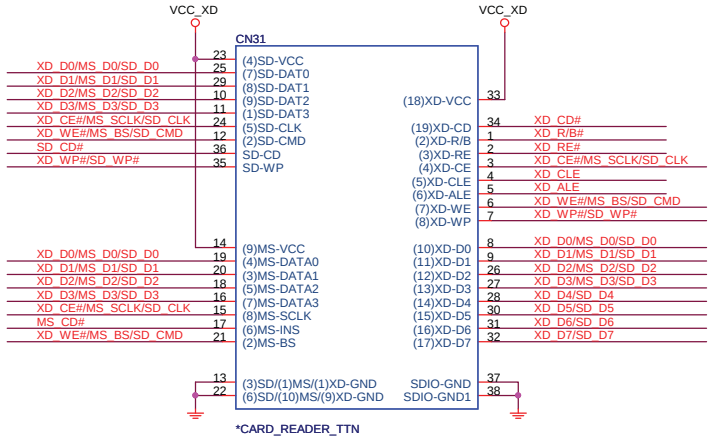


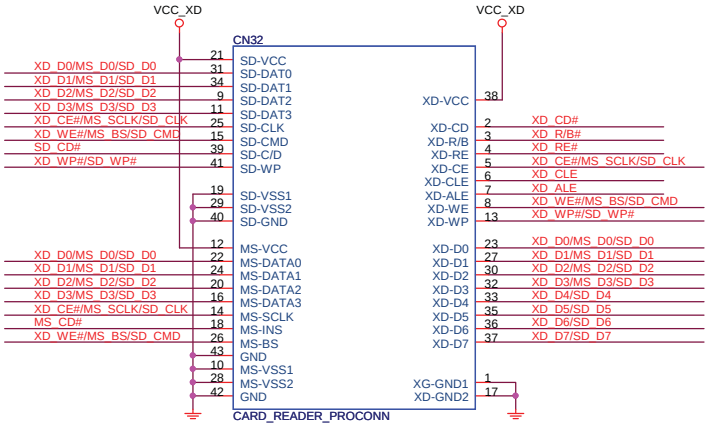




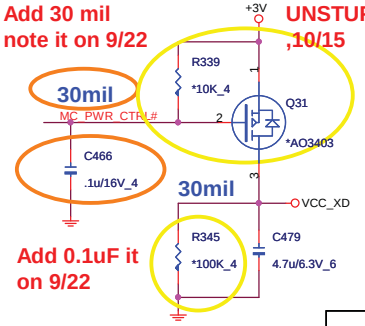
APVDD(pin5) must put C601/1000pF close to APVDD(pin5) (length must under 120mil) and trace width = 20mil, after C601, pls put one more 0.1uF for it.



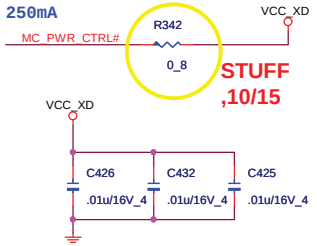




Memory Card Power Supply



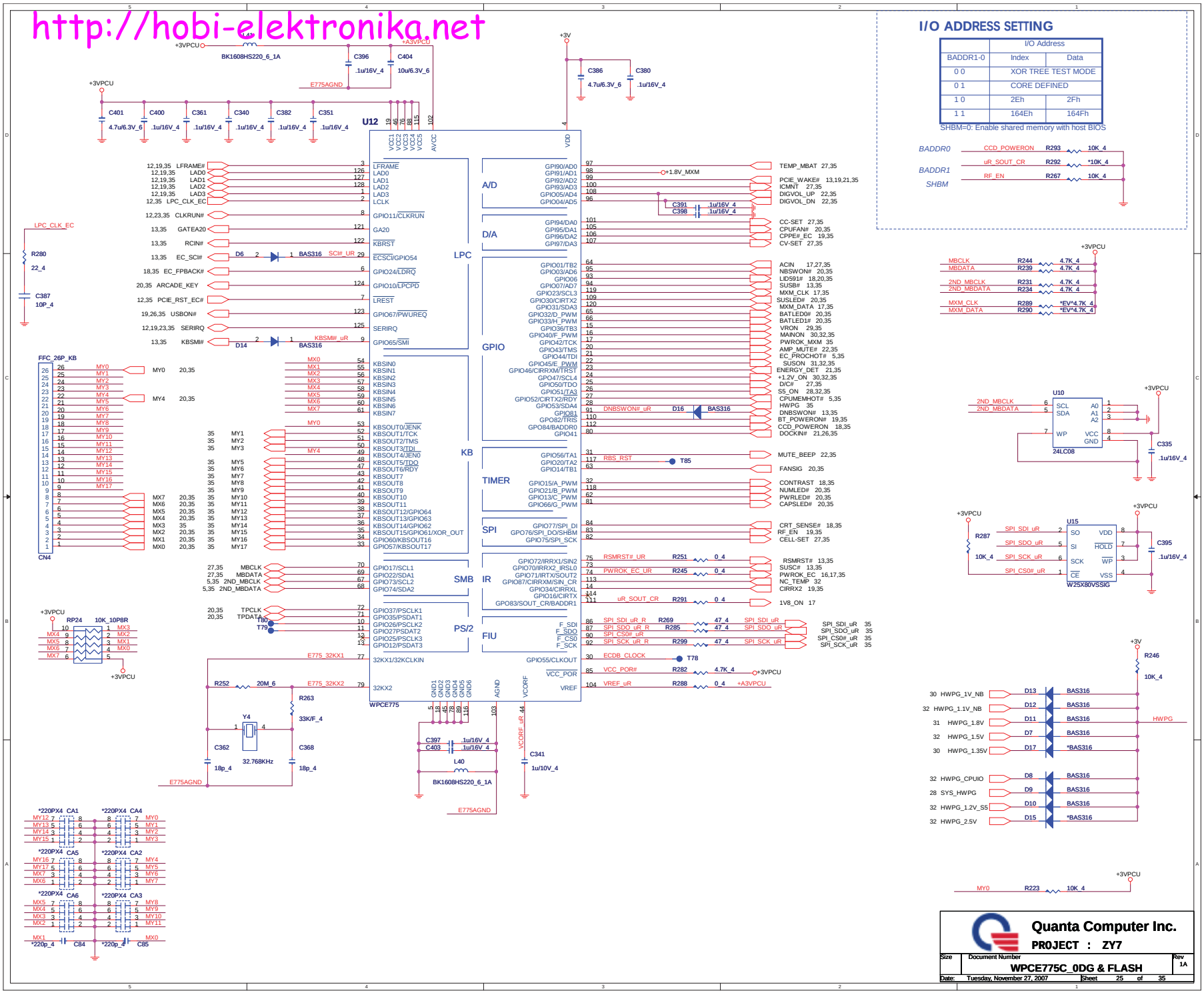
Use 0805 type and over 20 mils trace width on both side



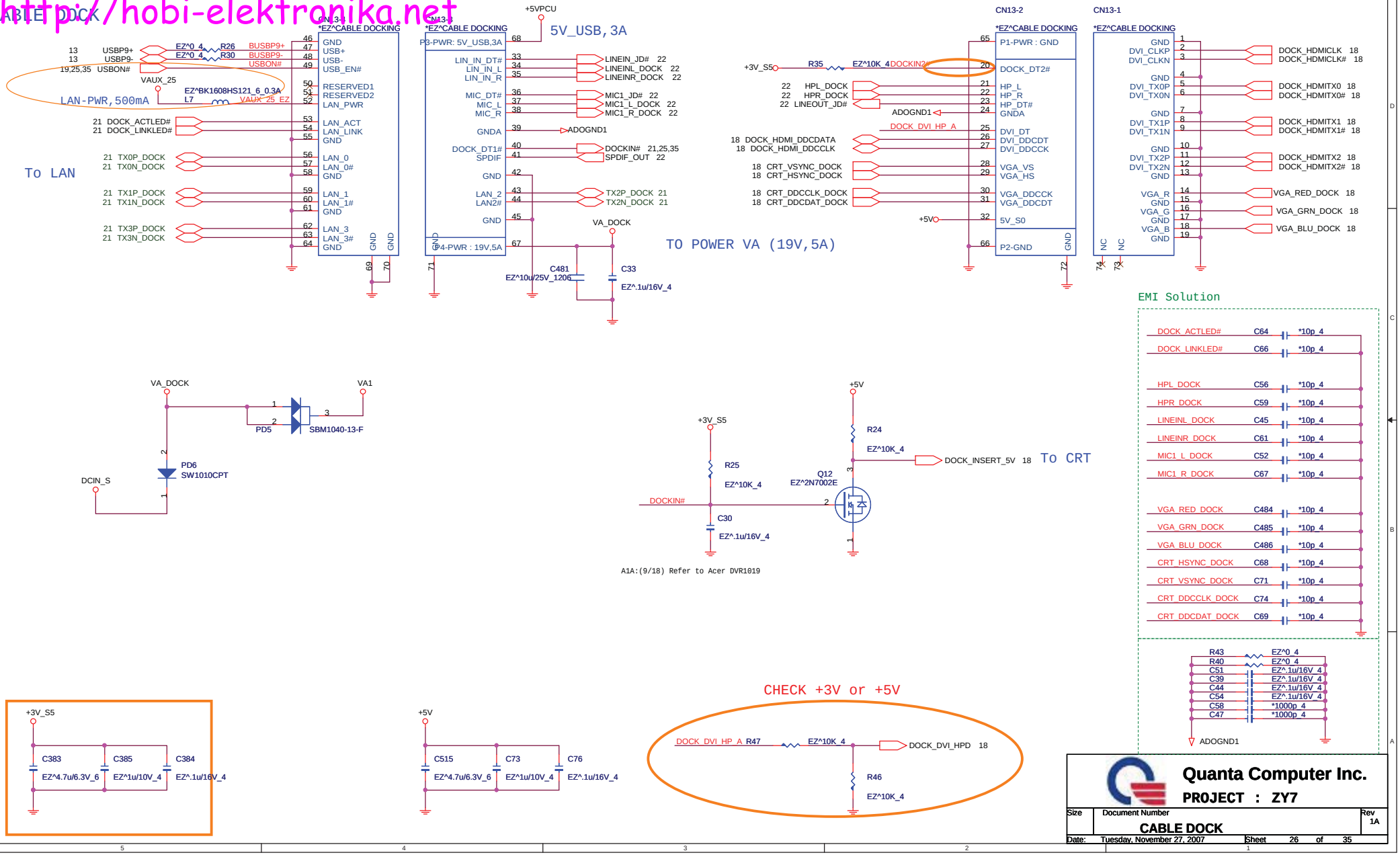
Quanta Computer Inc.

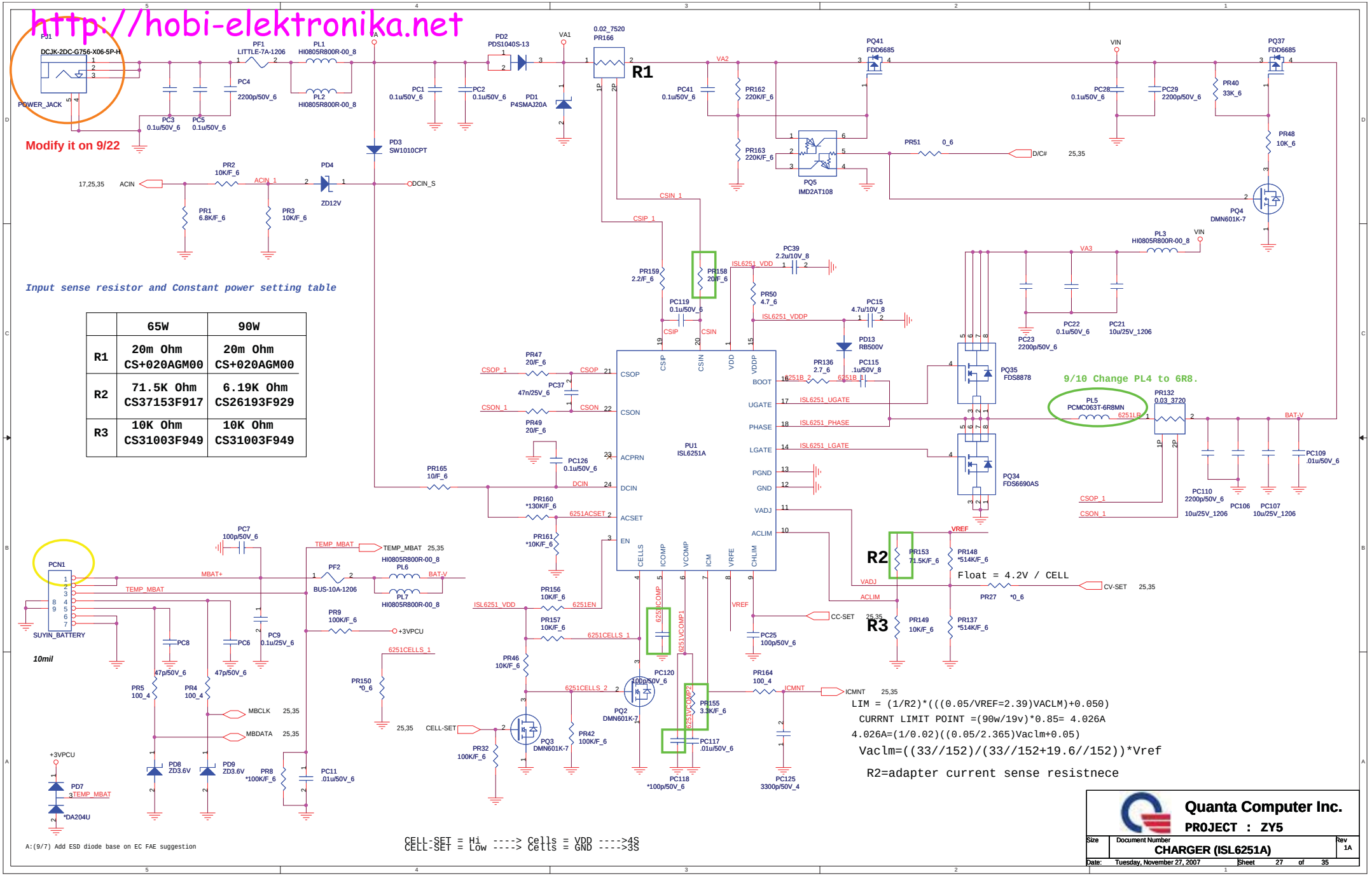
PROJECT : ZY7

Size	Document Number	Rev
	CARD READER JMB385	1A
Date: Tuesday, November 27, 2007	Sheet 24 of 35	

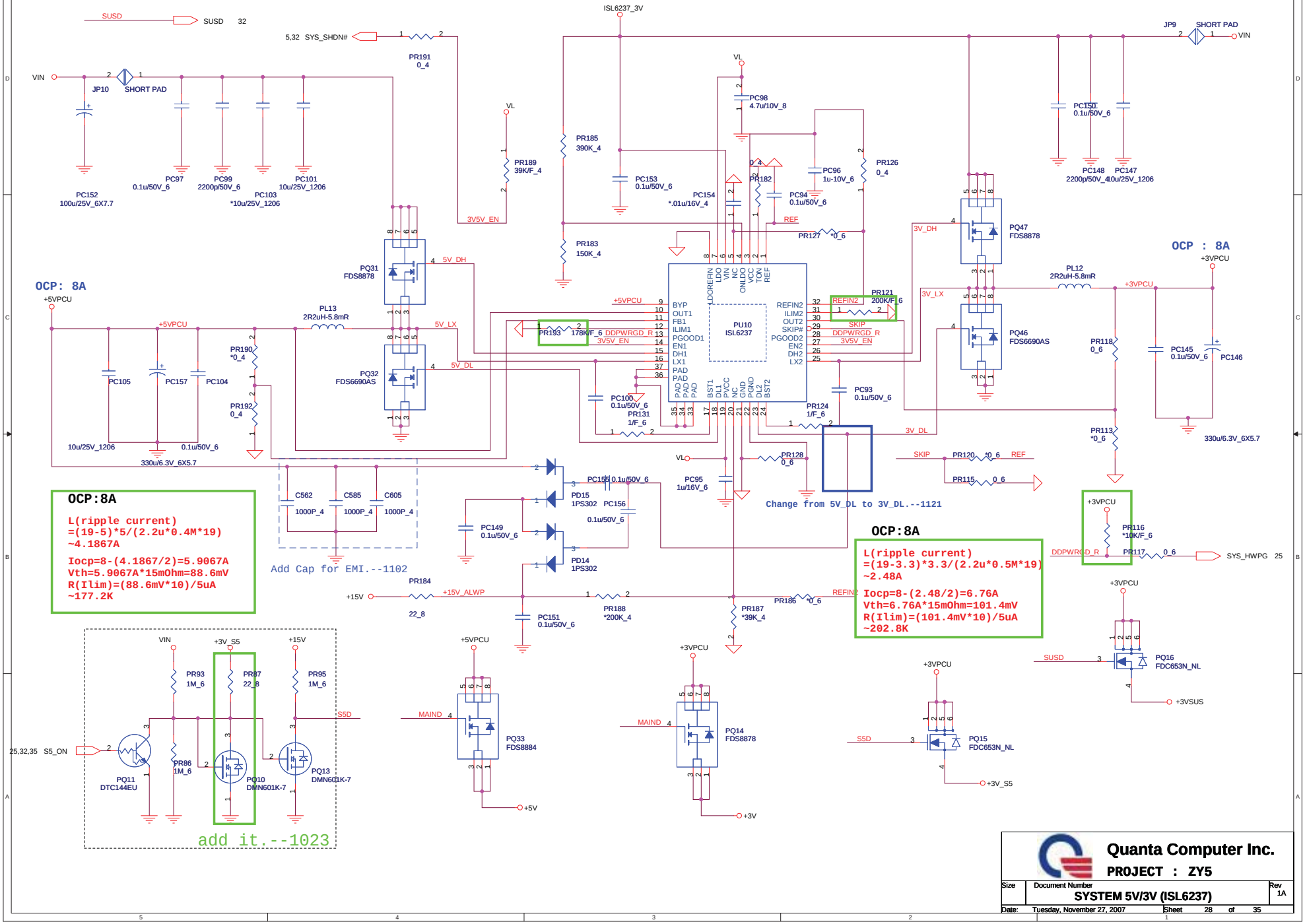


CABLE DOCK





	65W	90W
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	71.5K Ohm CS37153F917	6.19K Ohm CS26193F929
R3	10K Ohm CS31003F949	10K Ohm CS31003F949



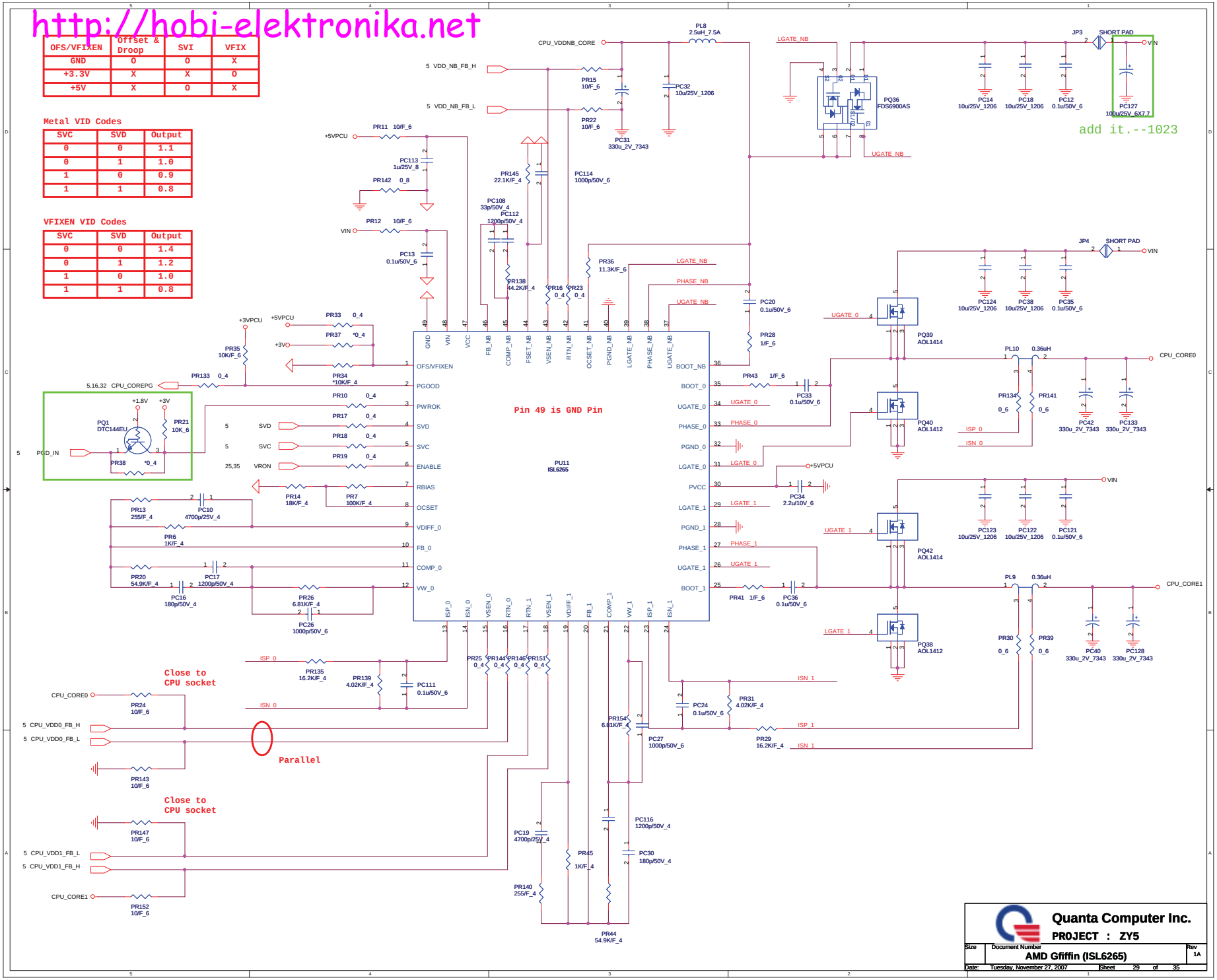
OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

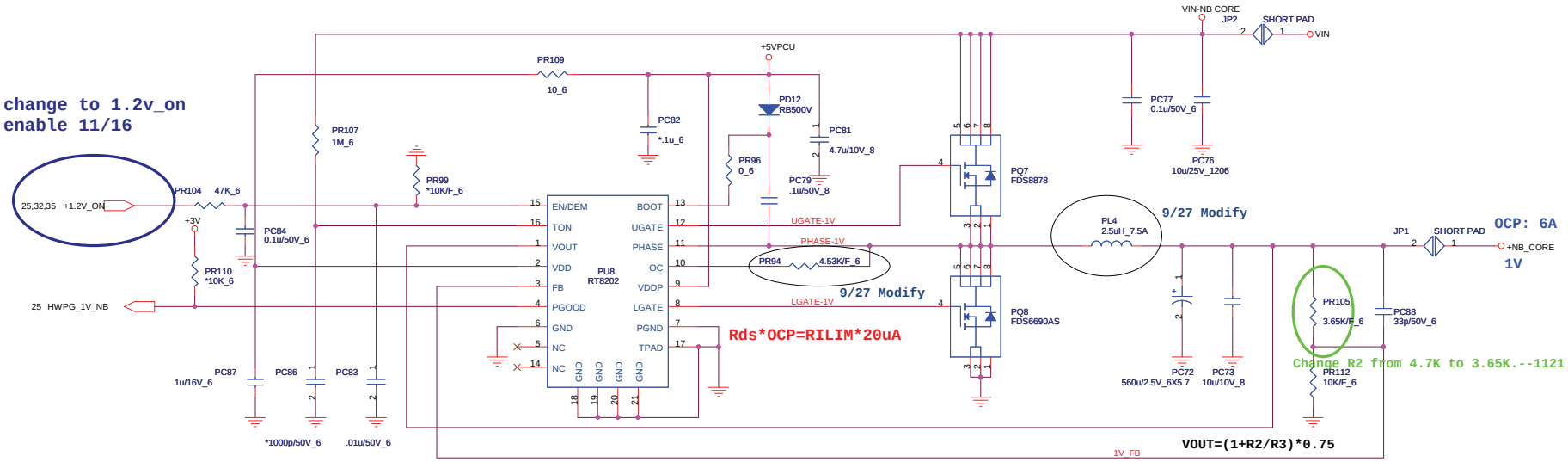
SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



Quanta Computer Inc.		
PROJECT : ZY5		
Size	Document Number: AMD Gfiffin (ISL6265)	Rev 1A
Date: Tuesday, November 27, 2007	Sheet 29 of 35	

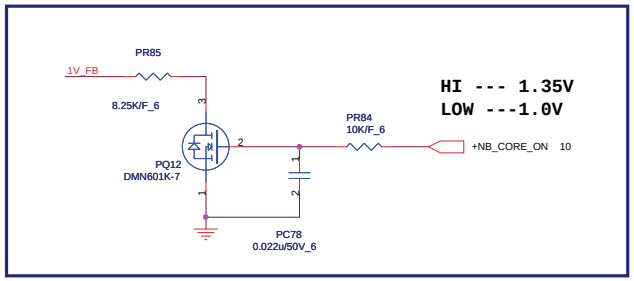


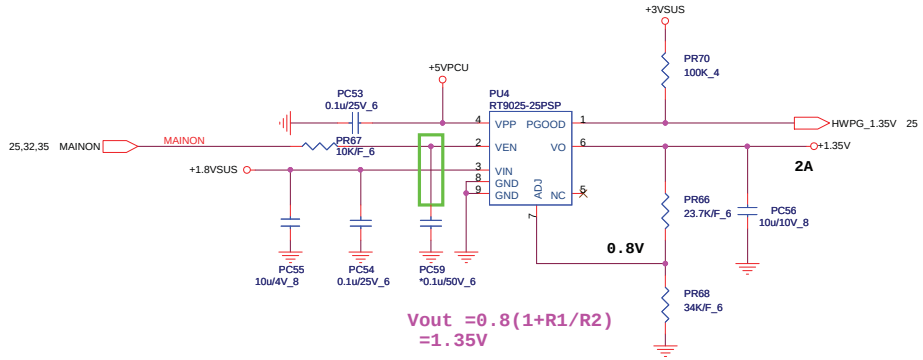
TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

6A OCP --- OC=4.53K
FDS6690AS Rds=15mOhm

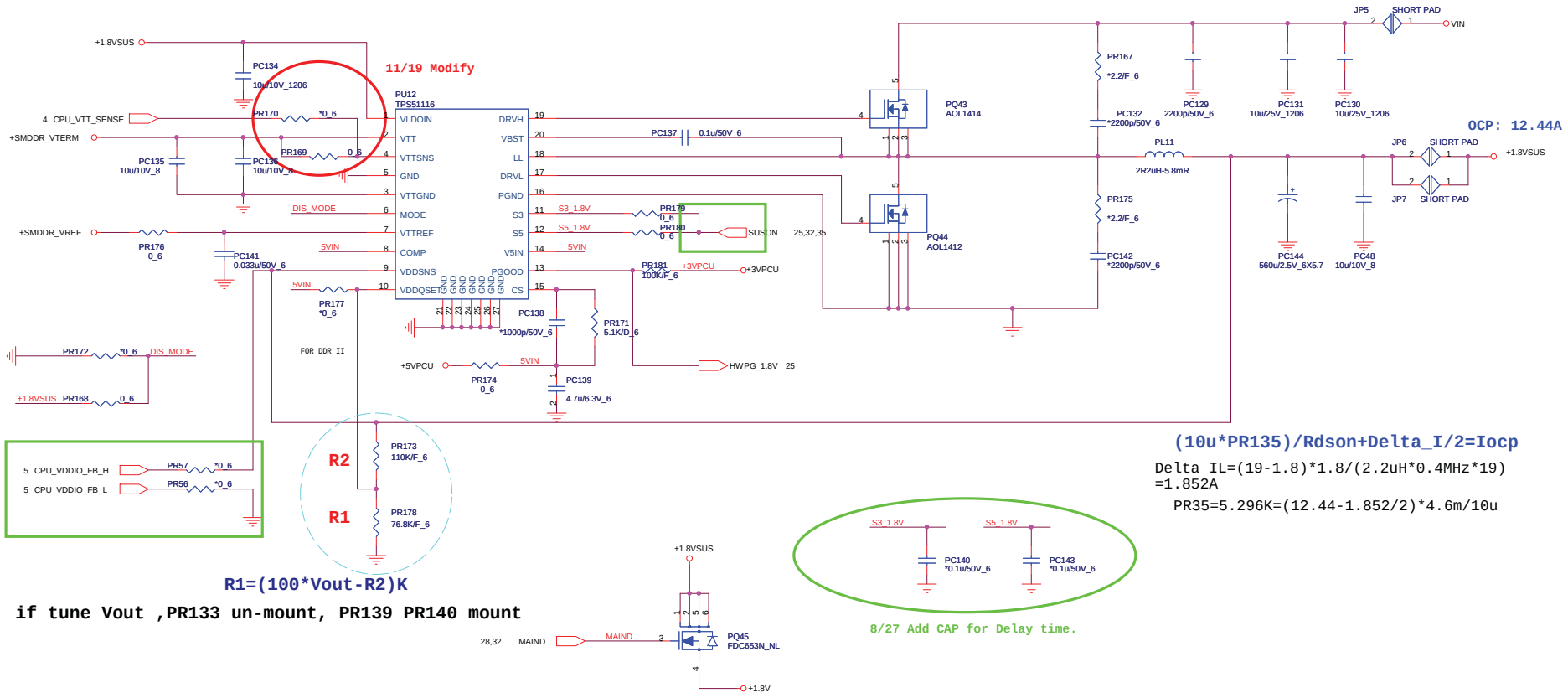
9/26 Addition





Quanta Computer Inc.
PROJECT : ZY7

Size	Document Number	Rev
	NB_CORE(RT8202)	1A
Date: Tuesday, November 27, 2007	Sheet 30 of 35	



Quanta Computer Inc.		
PROJECT : ZY5		
Size	Document Number: DDR 1.8V(TPS51116)	Rev: 1A
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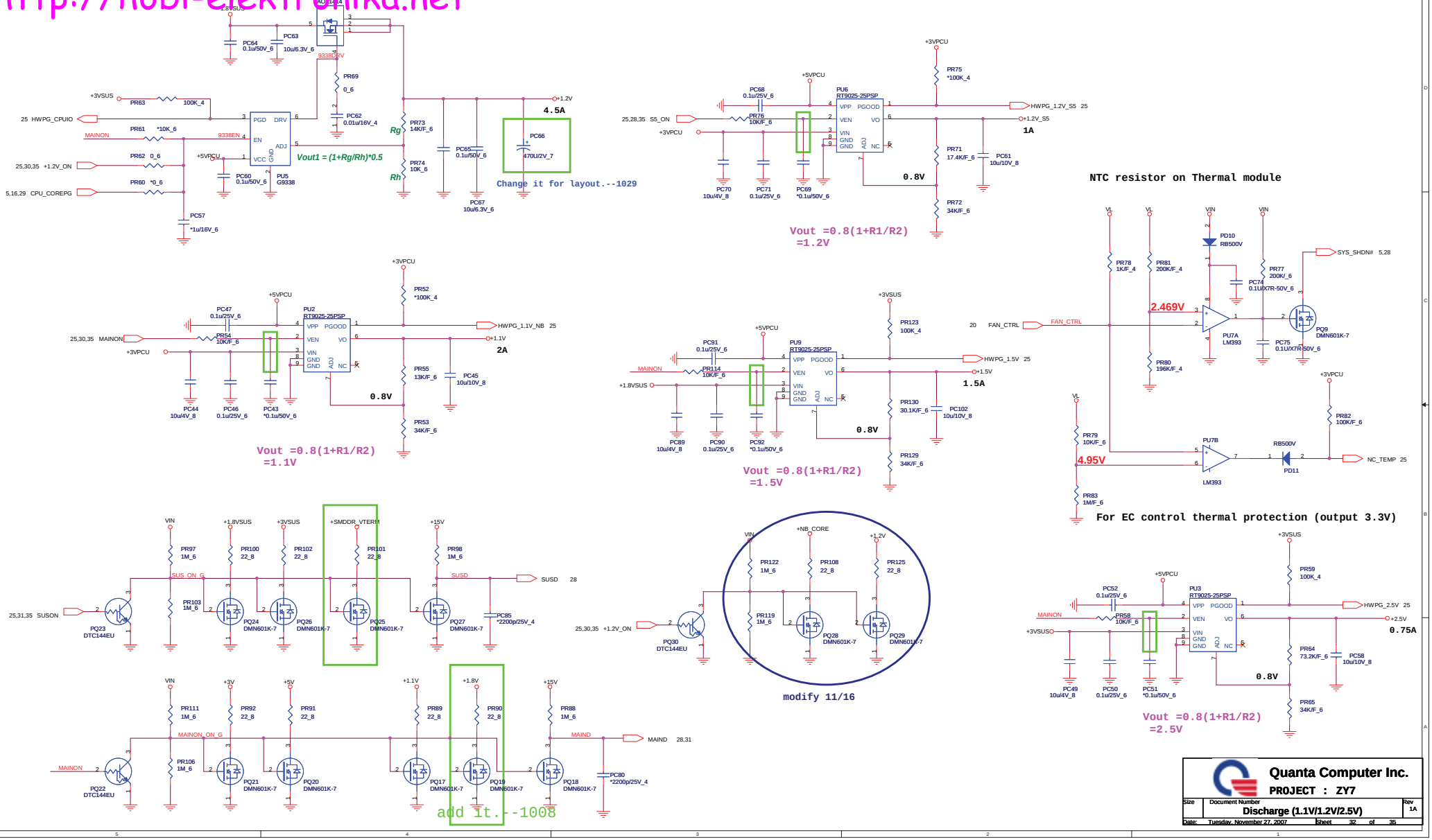

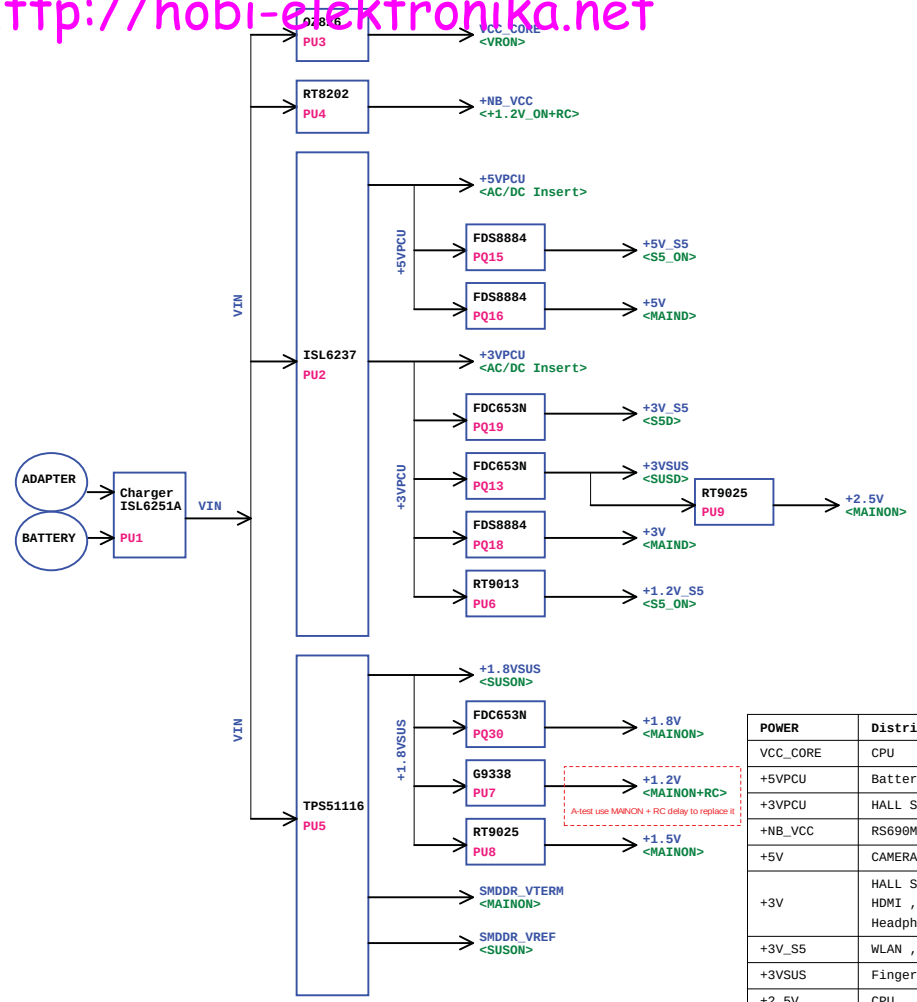

POWER	Distribution
VCC_CORE	CPU
+5VPCU	Battery LED , Power LED , USB , CIR , RTC
+3VPCU	HALL SENSOR , Battery LED , RF LED , kill SW , Jumper LED , KB , Power Board , EC , ID , SPI Flash , CIR
+NB_VCC	RS690M
+5V	CAMERA , Card Reader LED , ODD/HDD LED , Felica , T/P , T/sensor , CRT , HDMI , SB600 , CPU FAN , MXM , Headphone , EC , INT SPK AMP
+3V	HALL SENSOR , LCD PANEL , LVDS , WLAN , HD Decoder , NEW CARD , KB , KB LED , XD LED , Blue tooth , Touch sensor , Card Reader (OZ129) , ODD/HDD , HDMI , CRT , TVOUT , REQUIRED STRAPS , DEBUG STRAPS , SB600 , RS690M , DDR , CPU Thermal monitor , CPU FAN , CLK , MXM , VR , FM Tuner MDC , Headphone , EC , LAN , Codec(CX 20561)
+3V_S5	WLAN , NEW CARD , SB600 , MXM , LAN
+3VSUS	Finger print , SB600
+2.5V	CPU
+1.2V_S5	SB600
+1.8VSUS	SB600 , DDR , CPU , HDT
+1.8V	SB600 , LCD , LVDS , RS690M
+1.2V	SB600 , RS690M , CPU , WLAN , HD Decoder , NEW CARD
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR
+5V_S5	

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PROJECT : ZY5
Power Tree

CHANGE LIST

Model	REV	
ZY7 MB	1A	1.Copy RS780/SB700 circuit from QT8(0919).--0924 Page8:Change HT Link net.--0924 Page10:Change LVDS/HDMI net.--0924 Page20:Change ODD net name from SATA_TXP2 to SATA_TXP4--0925(Henri) Page20:del SATA1, SATA2 ODD(SATA)AC COUPLING--0925(Henri) Page14:del E-SATA portion.--0925(Henri) Page 14 Del RF_OFF#, EC will Control it----0925 Page 14 DEL WAN_OFF# for ROBSON Portion----0925 Page 14 DEL ACCLED_EN NET----0925 Page 14 DEL BT_COMBO_EN# NET----0925 Page 14 Del BT_OFF#, EC will Control it----0925 Page 14 Del CHIPSET_PCIE_SLOW_SB# Net----0925
	2B	
	2C	
	2D	

MODEL	ZY7	
	FROM	To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
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	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A

DOC NO.	PROJECT MODEL :	ZY7	APPROVED BY:		DATE:	2007/09/25
	PART NUMBER:		DRAWING BY:		REVISON:	3A

Title	<Title>	
Size: Custom	Document Number: <Doc>	Rev: <RevCode>
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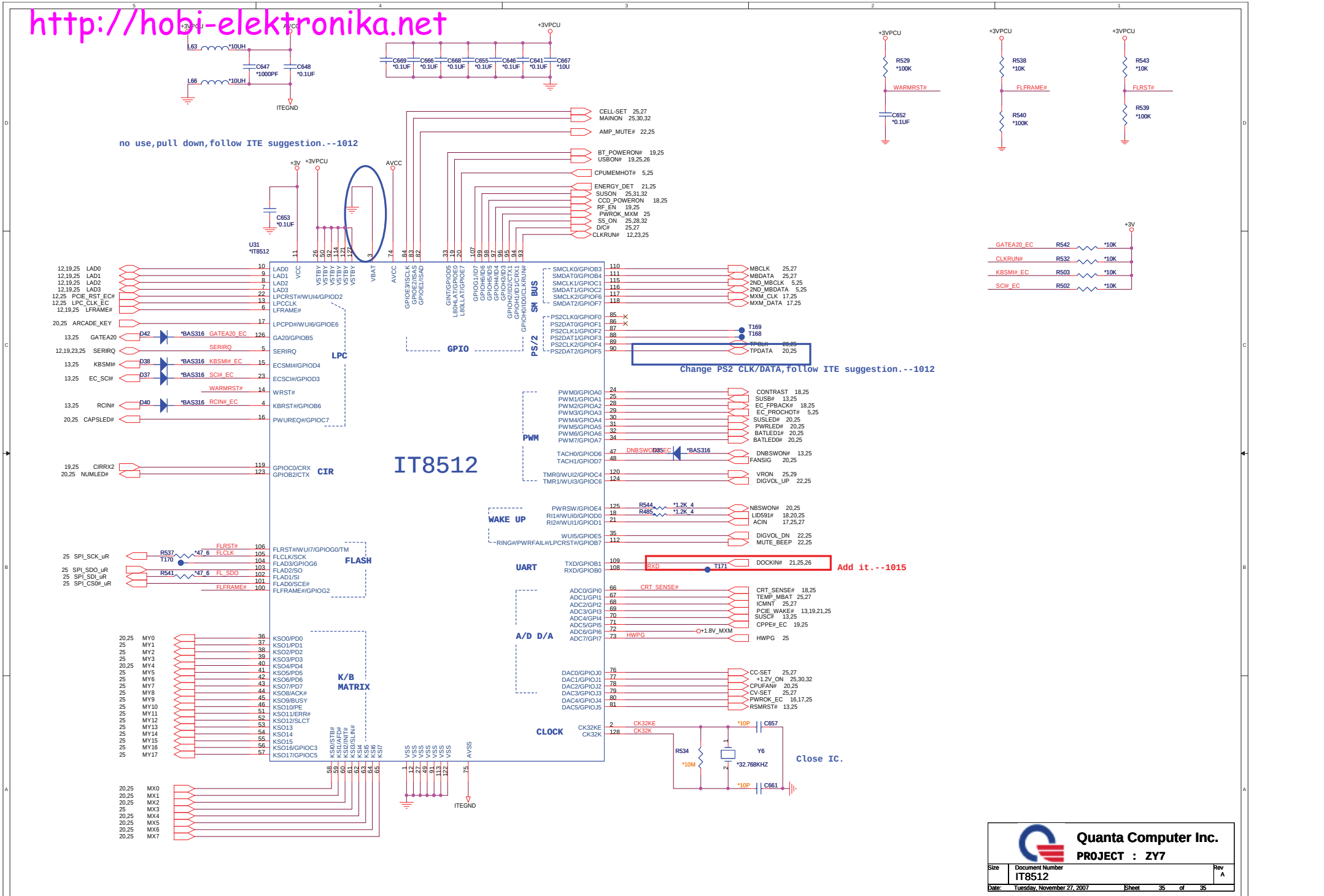
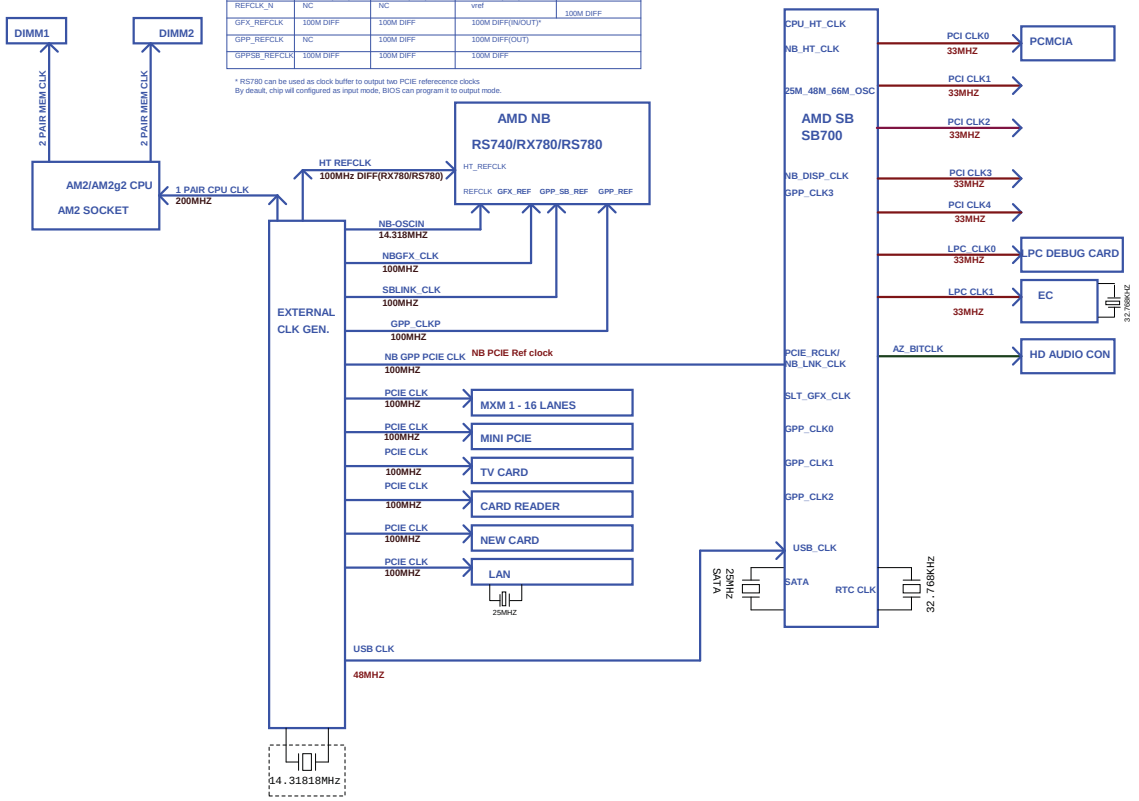


NB CLOCK INPUT TABLE

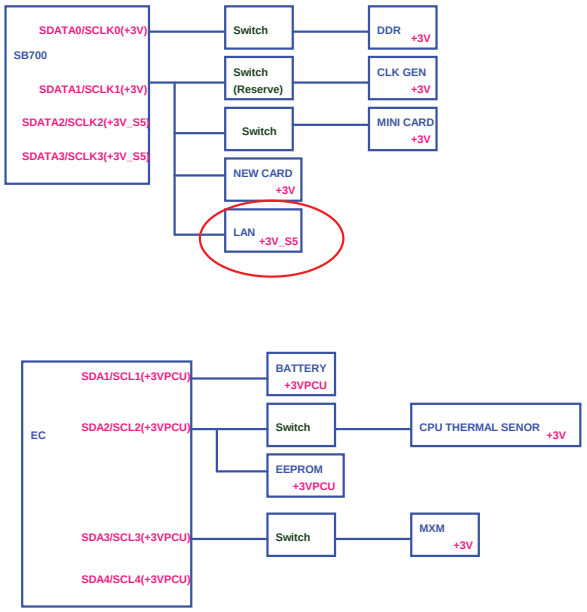
CLOCKS			
HT_REFCLKP	14M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V) 100M DIFF
REFCLK_N	NC	NC	vref 100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE refereence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

Clock distribution



SMBUS Table



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PROJECT : ZY7

Size	Document Number	Rev
	Clock/SMBUS	A

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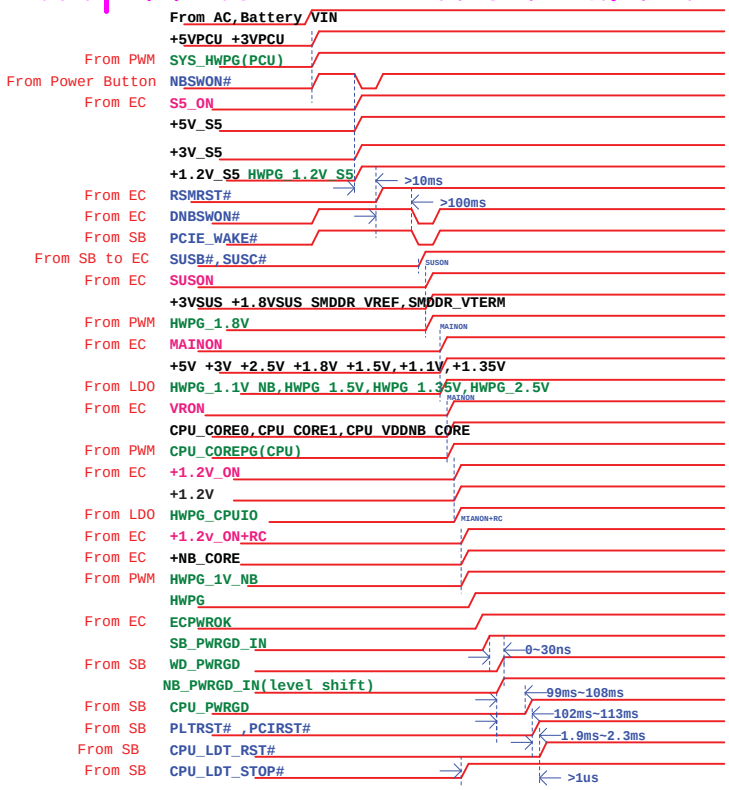
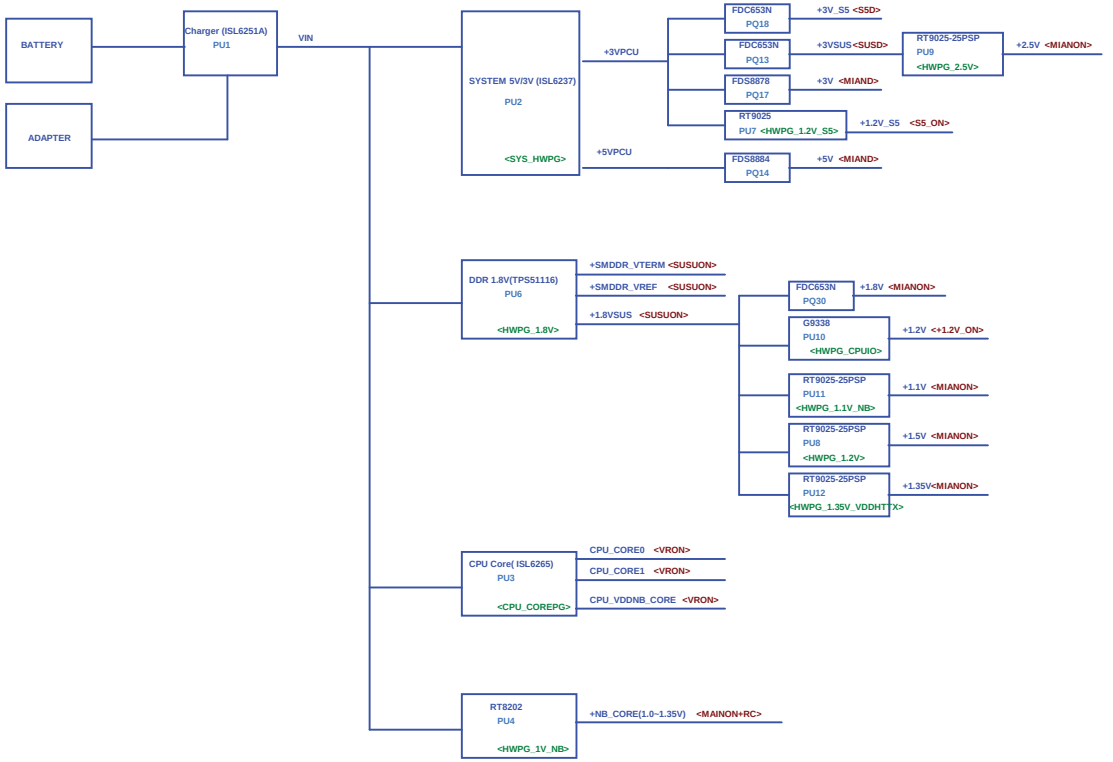


Power State / Voltage Rail Activity Summary

SYSTEM STATE	SLEEP STATE	PROCESSOR STATE	Description		RTC	ALWAYS	S5	SUS	RUN
G0	S0	C0	RUNNING		ON	ON	ON	ON	ON
G0	S0	C0	RUNNING	P-state transitions under OS control	ON	ON	ON	ON	ON
G0	S0	C1	RUNNING	HALT	ON	ON	ON	ON	ON
G0	S0	C2	RUNNING	Stop grant,caches snoopable	ON	ON	ON	ON	ON
G0	S0	C1E/C3	RUNNING	Stop grant, no LDTSTOP,not expected,cache snoops	ON	ON	ON	ON	ON
G0	S0	C1E/C3	RUNNING	Stop grant with LDTSTOP, cache not snoopable	ON	ON	ON	ON	ON
G1	S1	OFF	SLEEPING	Powered on suspend	ON	ON	ON	ON	ON
G1	S3	OFF	SLEEPING	Suspend to RAM	ON	ON	ON	ON	OFF
G2	S4	OFF	SLEEPING	Suspend to disk	ON	ON	ON	OFF	OFF
G2	S5	OFF	SOFT OFF		ON	ON	ON	OFF	OFF
G2/G3	S5 LOW	OFF	POWER BUTTON ONLY		ON	ON	OFF	OFF	OFF
G3		OFF	MECHANICAL OFF		ON	OFF	OFF	OFF	OFF



POWER	Distribution
VCC_CORE	CPU
+5VPCU	FINGERPRINT
+3VPCU	CIR,EC,SW/B,SUSLED,PWR LED,BAT LED,SPI FLASH
+1.1V	RS780
+NB_CORE	RS780
+5V	CRT,HDMI,DOCK,PCMCIA,AUDIO,HDD,ODD,FAN,TP,TV CARD,SB700,MXM
+3V	CPU,CLK GEN,SB700,RS780,MXM,DDR,DOCK,EC,CARD READER,PCMCIA,CODEC,LAN,HDD,NEW CARD,MINI CARD,LCD,CM2009,HDMI,CAMERA,CODEC,HEADPHONE,AMP
+3V_S5	DOCK,MDC,LAN,NEW CARD
+3VSUS	SUSLED,BT
+2.5V	CPU,MXM
+1.2V_S5	SB700
+1.8VSUS	CPU,SB700
+1.8V	CARD READER,RS780,SB700
+1.2V	SB600 , RS780 , CPU , CLK GEN
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR
+1.5V	NEW CARD,MINI CARD
+5V_S5	

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Power Sequence
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