PB2/PB2A BLOCK DIAGRAM 01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

PCI DEVICES IRQ ROUTING

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
R5C832	AD17	REQ0# / GNT0#	INT A/B#

CPU CORE MAX8736 PAG 40

SYSTEM POWER MAX8734 PAG 41

DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116) PAG 42

VCCP +1.5V AND GMCH 1.05V(TPS51124) PAG 43

VGACORE(1.025V)MAX1993 PAG 44

SYSTEM CHARGER(MAX8672) PAG 45,46

CPU Merom
478P (uPGA)/35W
PAG 3,4

CPU THERMAL SENSOR PAG 30

14.318MHz

CLOCK GEN
ICS9LPR363DGLF
64pinsTSSOP
PAG 2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

DDRII-SODIMM1 PAG 12,13
DDRII-SODIMM2 PAG 12,13
DDRII 533,667 MHz

NORTH BRIDGE
Crestline
PAG 5,6,7,8,9,10,11

PCI-Express 16X

NVDIA NB8X
NB8P-SE-256M
NB8M-SE-128M
P 15,16,17,18,19,20

HDMI CON PAG 25

CRT PORT PAG 24
DVI-I PORT PAG 24
LVDS(1 Channel)
LCD CNN PAG 25

DMI LINK

NBSRCCLK, NBSRCCLK#

SATA - HDD PAG 33
SATA0 150MB
PATA- CD-ROM PAG 33
PATA (66/100/133)

PCI BUS / 33MHz PAG 32

RICOH
RICOH 832
PAG 26~28

IEEE1394 PAG 27
Memory CardReader PAG 28

USB2.0 I/O PortsX4
0,1,2,3
USB2.0

Bluetooth 4
WebCam 6
Mini_PCI_E 7
TV Tune 8
Express Card 9

SOUTH BRIDGE
ICH-8M
PAG 20,21,22,23

PCI-E
Azalia

TV Tune

Mini PCI-E Card WLAN PAG 31

LAN Marvell M8039 PAG 32

Express Card PAG 28

E_SATA JMB360 PAG 33

E_SATA PAG 33

RJ45 PAG 32

INT-MIC PAG 35

CONEXANT CX20549 PAG 34

LPC

CIR
Flash PAG 38
SPI
Keyboard Touch Pad PAG 29

ITE8512
PAGE 38

FAN PAG 30

MAX9789A AUDIO Amplifier PAG 35

HP Jack / Speaker PAG 35

MDC DAA CX20548 PAG 37

MODEM RJ 11 PAG 37

MB PCB: DA0PB2MB8D0
SW/B PCB: DA0PB2PI8D0
USB/B PCB: DA0PB2TB8D0
TP/B PCB: DA0PB2TR8D0

USB:32PB2UB0000
TP:33PB2TB0000
SW:34PB2SB0000

256M
MB:31PB2MB0010/K0 PB2A/NB8P-SE Infineon
MB:31PB2MB0020/I0 PB2A/NB8P-SE Hynix
128M
MB:31PB2MB0000/L0 PB2/NB8M-SE Infineon
MB:31PB2MB0040/J0 PB2/NB8M-SE Hynix

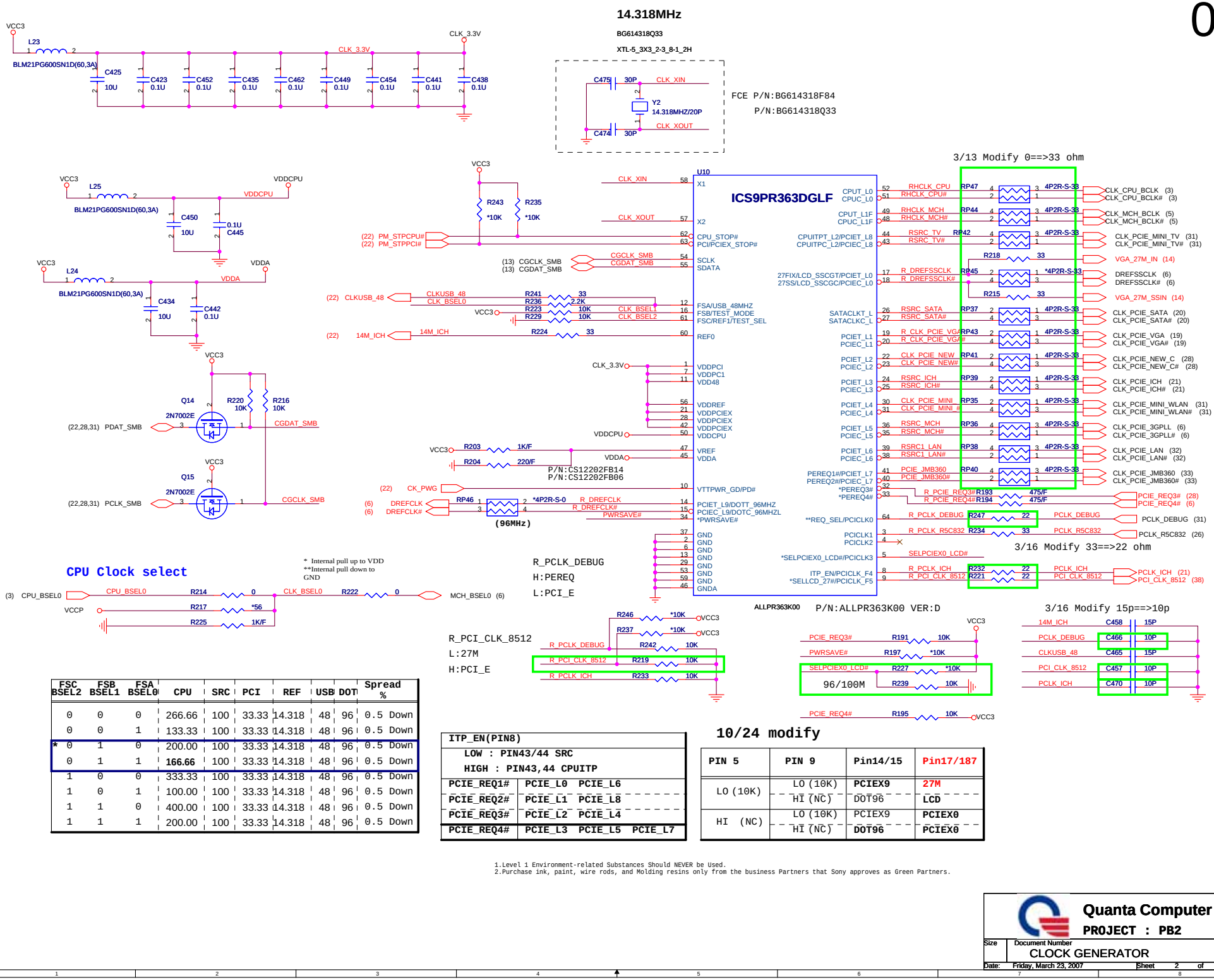
Voltage Rails

Voltage Rails	ON S0~S2	ON S3	ON S4	ON S5	Ctl Signal
VCC_CORE	X				VR_ON
VCCP	X				MAINON
SMDDR_VTERM	X				MAINON
VGACORE	X				MAINON
VGA1.2	X				MAINON
RVCC3	X	X	X		RVCCD
VCC1.25	X				MAINON
VCC1.5	X				MAINON
VCC1.8	X				MAIND
VCC2.5	X				MAINON
VCC3	X				MAIND
VCC5	X				MAIND
1.8VSUS	X	X			SUSON
3VSUS	X	X			SUSD
5VSUS	X	X			SUSD
3VPCU	X	X	X	X	8734LDO5
5VPCU	X	X	X	X	8734LDO5
15VPCU	X	X	X	X	5VPCU

Quanta Computer Inc.
PROJECT : PB2

Size	Document Number	Rev
	BLOCK DIAGRAM	A

Date: Friday, March 23, 2007 Sheet 1 of 46



FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
* 0	1	0	200.00	100	33.33	14.318	48	96	0.5 Down
0	1	1	**166.66**	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	200.00	100	33.33	14.318	48	96	0.5 Down

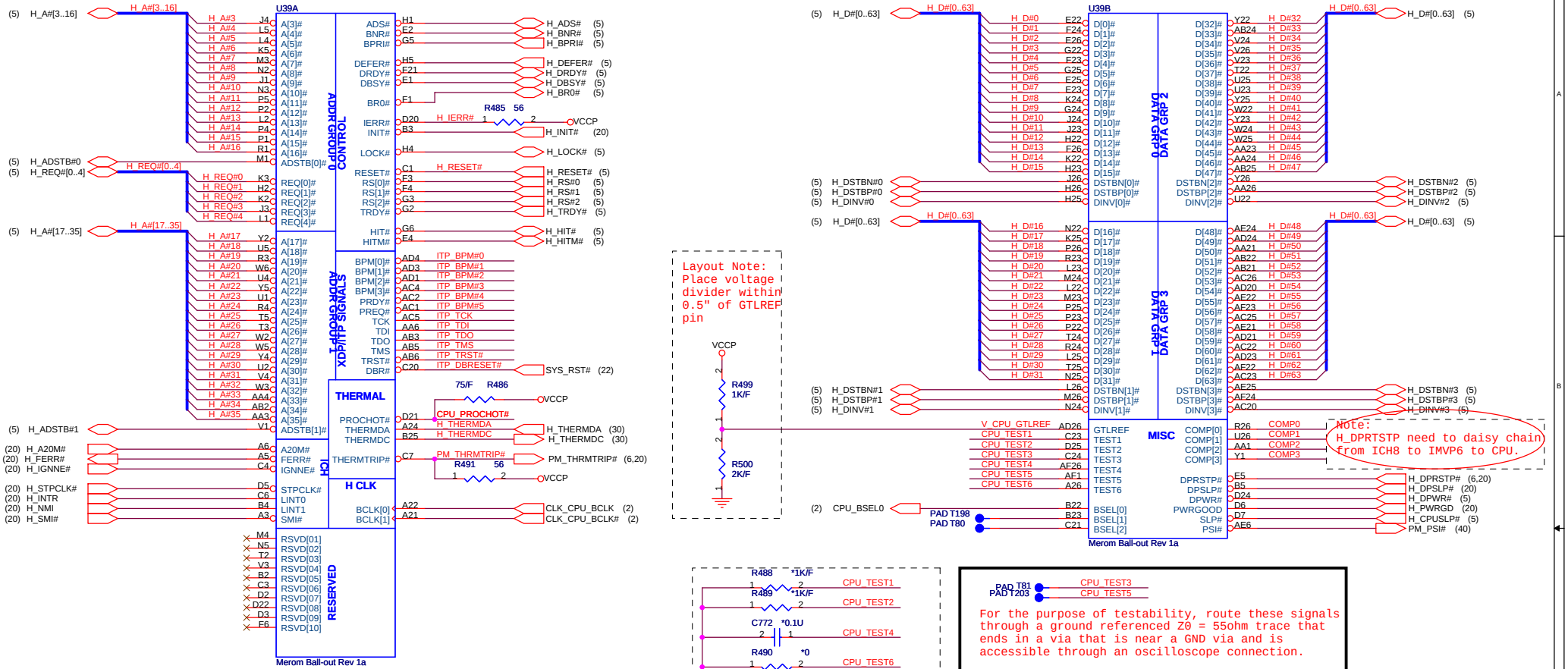
ITP_EN(PIN8)			
LOW : PIN43/44 SRC			
HIGH : PIN43,44 CPUITP			
PCIE_REQ1#	PCIE_L0	PCIE_L6	
PCIE_REQ2#	PCIE_L1	PCIE_L8	
PCIE_REQ3#	PCIE_L2	PCIE_L4	
PCIE_REQ4#	PCIE_L3	PCIE_L5	PCIE_L7

10/24 modify

PIN 5	PIN 9	Pin14/15	Pin17/187
LO (10K)	LO (10K)	PCIEX9	27M
	HI (NC)	DOT96	LCD
HI (NC)	LO (10K)	PCIEX9	PCIEX0
	HI (NC)	DOT96	PCIEX0

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : PB2
Size | Document Number: CLOCK GENERATOR | Rev A
Date: Friday, March 23, 2007 | Sheet 2 of 46



FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

ITP disable guidelines

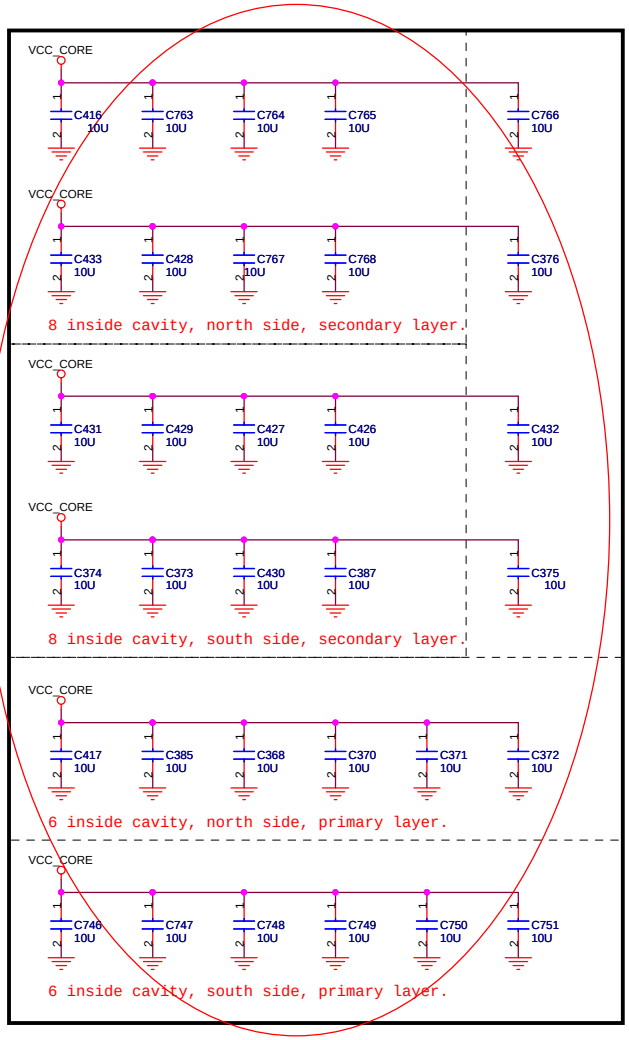
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

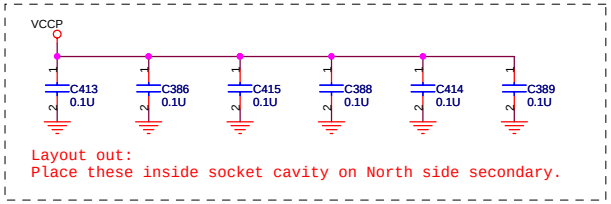
Note: Populate R5, R8, C372 & R430 when ITP connector is populated.

Quanta Computer Inc.
PROJECT : PB2

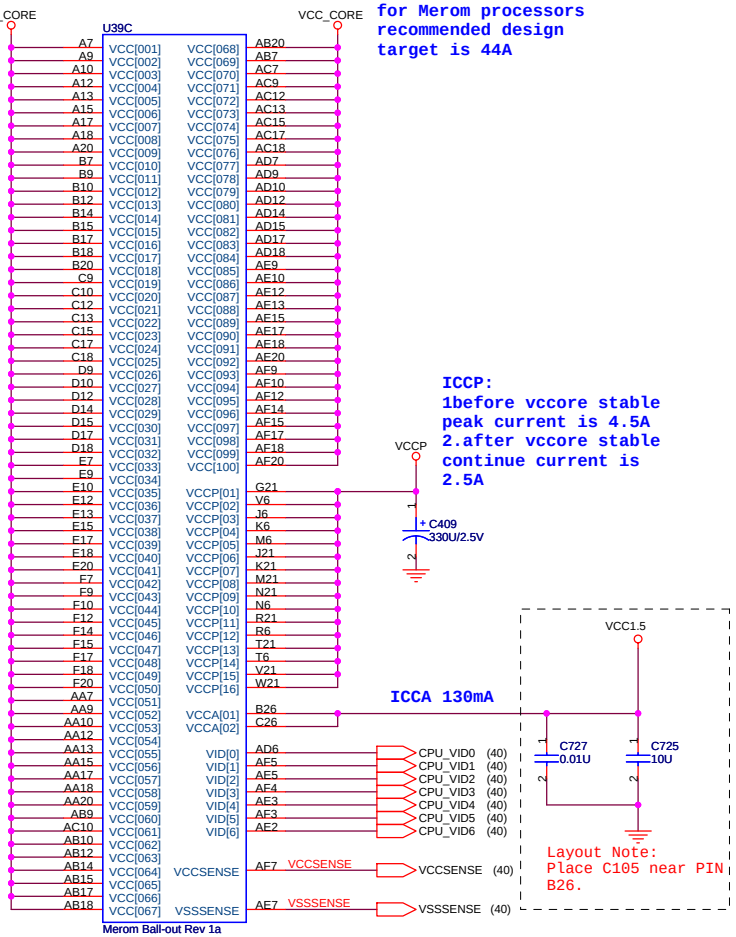
Size	Document Number	Rev
	CPU	A

Date: Friday, March 23, 2007 Sheet 3 of 46



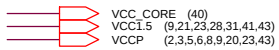


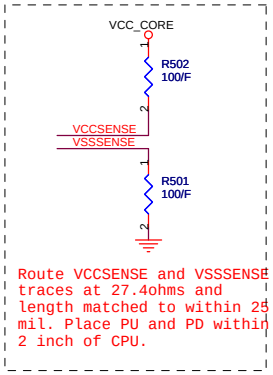
ICCODE:
for Merom processors
recommended design
target is 44A

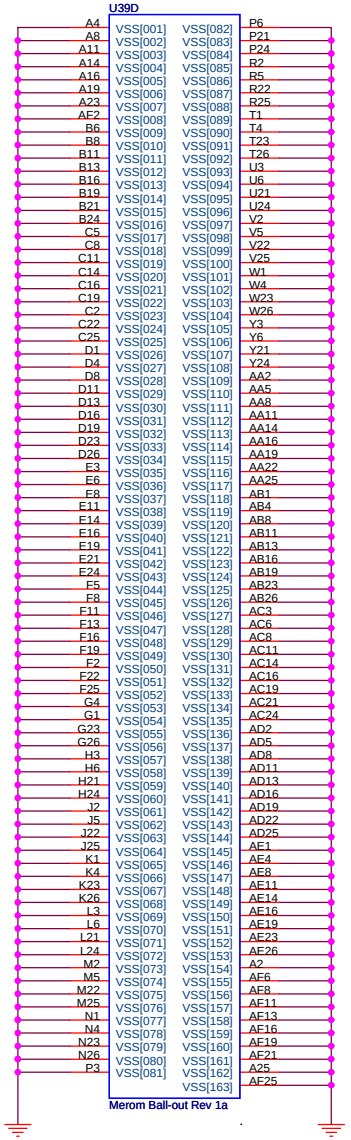


ICCP:
1before vccore stable peak current is 4.5A
2.after vccore stable continue current is 2.5A

ICCA 130mA

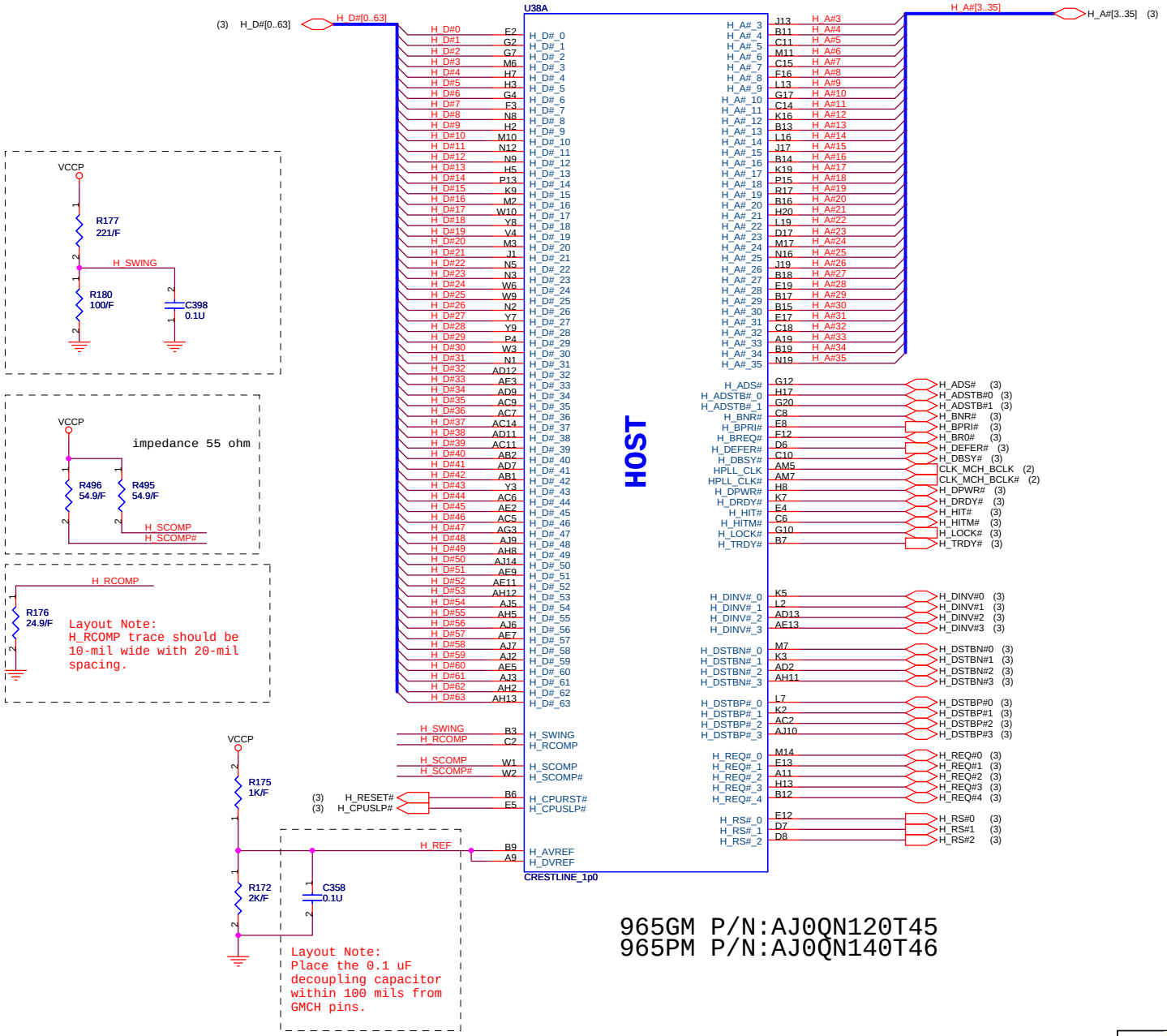






Quanta Computer Inc.
PROJECT : PB2

Size	Document Number	Rev
	CPU	A
Date: Friday, March 23, 2007	Sheet 4 of 46	



965GM P/N:AJ0QN120T45
965PM P/N:AJ0QN140T46

Quanta Computer Inc.		
PROJECT : PB2		
Size	Document Number NB	Rev A
Date: Friday, March 23, 2007	Sheet 5 of 46	

U38B

U38C

WW22 update
--- MA14 needs to be routed if customers are planning on using 2Gb technology and width=8 (by 8) DIMMs

CRESTLINE new pin define

Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minmize stub.

GMCH pwrok is 3.3v tolerant

<check list & CRB>
For Calero : 1.5K
For Cresstline:2.4K

IV&EV Dis/Enable setting

For 965GM TV disable

<FAE>
If no use can be NC

<check lisr & CRB>
For Calero : 255
For Cresstline:1.3K/F
For external VGA:0 ohm

<FAE>
Flexible and safe

IV&EV Dis/Enable setting

<check list>
HSYNC/VSYNC serial R place close to NB

In Crestline EDS Rev.1.0, Render Standby Voltage is not finalized yet(TBD), 1.05V for Graphic Voltage range(VCC_AXG) is between 0.9975V(min.) and 1.1025V(max.). Vgfx max at 1.1025V @ 8A (estimated)

only reserver AT3/5 not support IAMT,but design line suggest to connection these pin ,do not NC

CLKREQ# (MCH drives CLK_REQ# to control the PCI-E diff clk input itself)

<check list>
SDVO/PCIE/LVDS not implement
16 lanes NC

<check list>
For EV@
Connect to GND
CRT R/G/B
TV A/B/C
HSYNC/VSYNC

<check list>
For IV@
Connect to 150ohm
CRT R/G/B
TV A/B/C
Connect to 0ohm
HSYNC/VSYNC

<design guide>
If no use
DREFCLK PU and
DREFCLK# PD

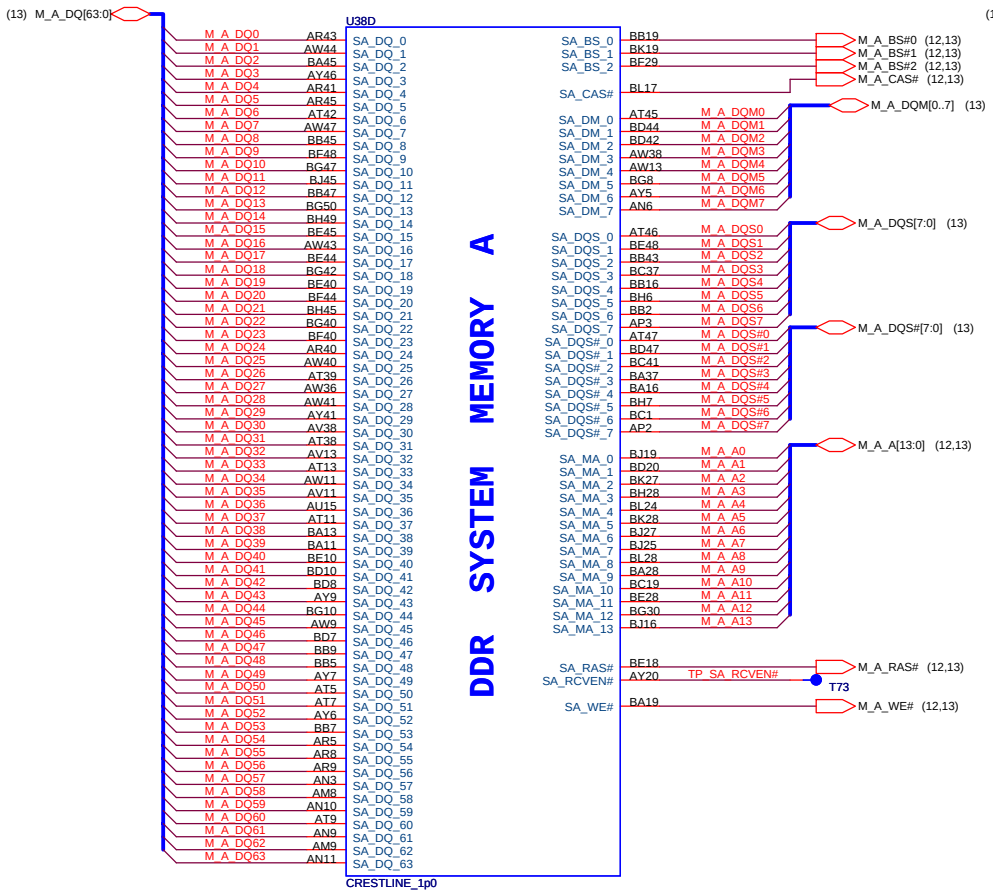
<FAE>
If no use DREFCLK PU and DREFCLK# PD

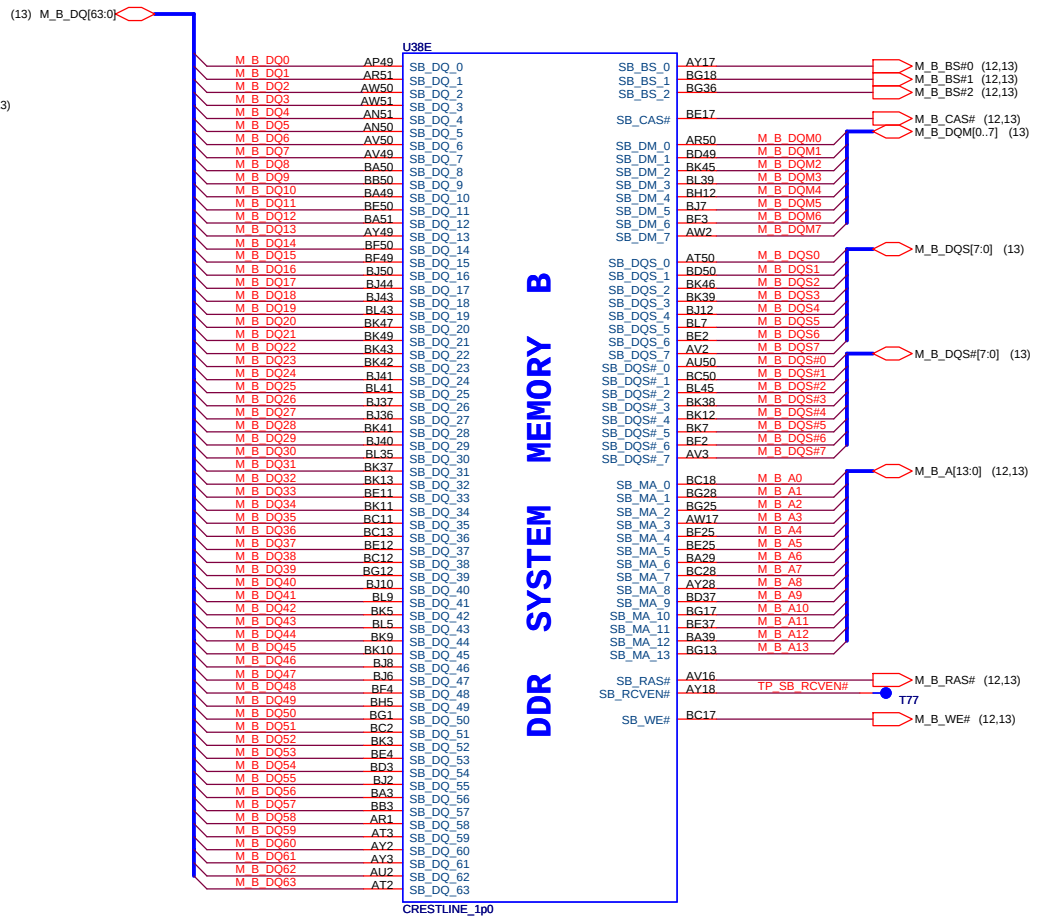
1.8VSUS (8,9,13,41,42)
VCC1.25 (9,23,43)
VCC3 (2,3,8,9,11,13,14,15,16,19,20,21,22,23,24,25,26,28,30,31,33,38,40,41)

Quanta Computer Inc.
PROJECT : PB2

Size	Document Number	Rev
	NB	A

Date: Friday, March 23, 2007 Sheet 6 of 46





Quanta Computer Inc.			
PROJECT : PB2			
Size	Document Number		Rev
	NB		A
Date: Friday, March 23, 2007		Sheet 7 of 46	

POWER

IVCCSM supply current 1 channel 1.615A 2 channel 3.318A

Ivcc (External GFX 1.310 A, integrate 1.572 A)

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity.

Ivcc_AXG Graphics core supply current 7.7A

C419 *330U/2.5V

R598 0

H=1.9mm

P/N:CH733LM8812

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity for VCC_AXG.

A test check when use external VGA can remove or not.. andrew

for IAMT power if not support need to connection to S0 power

Ivcc_AXM Controller supply current 540mA

Layout Note: Inside GMCH cavity.

Layout Note: Place close to GMCH edge.

Layout Note: Place C901 where LVDS and DDR2 taps.

Layout Note: Place on the edge.

GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

CRESTLINE_1p0

Quanta Computer Inc.	
PROJECT : PB2	
Size:	Document Number: NB — Rev: A
Date: Friday, March 23, 2007	Sheet 8 of 46

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V

CRT/TV Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TVC_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVDAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TVB_DAC	3.3V	GND	VCCSYNC	3.3V	GND

IV&EV Dis/Enable setting

+3V_VCCSYNC, VCC3, R141 *0, C298 *0.1U, R131 0

<FAE>
INT VGA disable
VCCSYNC connect
to GND

VCC3, L36 *BLM18PG181SN1, +VCCA_CRTDAC, R480 *0, +3V_VCCA_CRT_DAC

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

C722 *0.1U, R482 0

+3V_TV_DAC, R492 *0.03/F, +VCC_TVBG, R483 *0, +1.8VSUS_VCC_TX_LVDS

C726 *0.1U, R484 0

FB_120ohm+-25%_100mHz
200mA_0.2ohm DC

VCC1.25, L38 BLM11A121S, 50mA, +1.25V_VCCA_HPLL, C769 22U/10V, C756 0.1U

L39 BLM11A121S, 150mA, +1.25V_VCCA_MPLL, R494 0.5/F/0603, +VCCA_MPLL_L, C757 0.1U, C770 22U/10V

VCC1.25, L14 *0, 80mA, +1.25V_VCCA_DPLLA, C256 *470U/4V, C251 0.1U

10uH+-20%_100mA

L34 *0, 80mA, +1.25V_VCCA_DPLLB, C693 *470U/4V, C248 0.1U

0.1Caps should be placed 200 mils with in its pins.

IV&EV Dis/Enable setting

+1.8VSUS_VCC_TX_LVDS, 10mA, C716 *1000P, R476 0

VCC3, C252 0.1U, Ivcca_PEG_BG supply current 100mA

+1.25V_VCCD_PEG_PLL, 100mA, U51

VCC1.25, R178 0, +1.25V_VCCA_SM, C424 100U/6.3V-3528, C332 4.7U, C350 22U/6.3V, C410 22U/6.3V, C344 1U

VCC1.25, R152 0, +1.25V_VCCA_SM_CK, C300 22U/6.3V, C302 1U, C313 1U, C311 0.1U

VCC3, R151 *0, R149 0

+1.5V_VCCD_TVDAC, +1.5V_VCCD_TVDAC, R121 0, R146 0, R136 *0, +1.5V_VCCD_CRT, +1.5V_VCCD_TVDAC, +1.5V_VCCD_QDAC

VCC1.5, C284 0.1U, L18 *BLM18PG181SN1, +VCCD_TVDAC, C317 *0.1U

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

R159 0

+VCCA_MPLL_L, 250mA, C762 0.1U, C258 0.1U, +1.8V_VCCD_LVDS, 150mA

1.8VSUS, R100 *0, C259 *1U, C261 *10U, R107 0

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

+3V_TV_DAC, VCC3, L37 *BLM18PG181SN1, C732 *10U

22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.

IV&EV Dis/Enable setting

VCC1.25, L33 BLM21PG600SN1D(60.3A), 100mA, +1.25V_VCCD_PEG_PLL

FB_220ohm+-25%_100MHz_2A_0.1ohm DC

R464 1/F/0603, C685 10U/6.3V, C253 0.1U

U38H

CRESTLINE_1p0

CRT: VCCSYNC, VCCA_CRT_DAC_1, VCCA_CRT_DAC_2, VCCA_DAC_BG, VSSA_DAC_BG

PLL: VCCA_DPLLA, VCCA_DPLLB, VCCA_HPLL, VCCA_MPLL

LVDS: VCCA_LVDS, VSSA_LVDS

APEG: VCCA_PEG_BG, VSSA_PEG_BG, VCCA_PEG_PLL

ASM: VCCA_SM_1, VCCA_SM_2, VCCA_SM_3, VCCA_SM_4, VCCA_SM_5, VCCA_SM_7, VCCA_SM_8, VCCA_SM_9, VCCA_SM_10, VCCA_SM_11, VCCA_SM_NCTF_1, VCCA_SM_NCTF_2

ACK: VCCA_SM_CK_1, VCCA_SM_CK_2

TV/CRT: VCCA_TVA_DAC_1, VCCA_TVA_DAC_2, VCCA_TVB_DAC_1, VCCA_TVB_DAC_2, VCCA_TVC_DAC_1, VCCA_TVC_DAC_2

LVDS: VCCD_CRT, VCCD_TVDAC, VCCD_QDAC, VCCD_HPLL, VCCD_PEG_PLL, VCCD_LVDS_1, VCCD_LVDS_2

POWER

VTT: VTT_1 … VTT_22

AXD: VCC_AXD_1 … VCC_AXD_6, VCC_AXD_NCTF

AXF: VCC_AXF_1, VCC_AXF_2, VCC_AXF_3, VCC_DMI

SM CK: VCC_SM_CK_1 … VCC_SM_CK_4

HV: VCC_TX_LVDS, VCC_HV_1, VCC_HV_2

PEG: VCC_PEG_1 … VCC_PEG_5

DMI: VCC_RXR_DMI_1, VCC_RXR_DMI_2

VTTLF: VTTLF1, VTTLF2, VTTLF3

Ivcc_VTT FSB supply current 0.85A

C352 2.2U/6.3V, C761 4.7U, Place on the edge.

C361 0.1U, C760 4.7U, C418 220U/2.5V, Place on the edge.

+1.25V_AXD, R174 0, C324 1U, C339 220U/10V, Place caps close to VCC_AXD.

+1.25V_VCC_AXF, +1.25V_VCC_DMI, Ivcc_DMI supply current 100mA

+1.25V_VCC_DMI, R470 0, C710 0.1U

+1.8VSUS_VCC_SM_CK, 200mA

+1.8VSUS_VCC_TX_LVDS, 100mA, L35 *0, 1uH+-20%_300mA, C715 *1000P, C712 *220U/6.3V

IV&EV Dis/Enable setting

+3V_VCC_HV, C40, B40, C717 0.1U

+VCC_PEG, R542 0, C222 220U/2.5V, C268 10U/6.3V, 91uH+-20%_1.5A, Ivcc_PEG supply current 1.2A

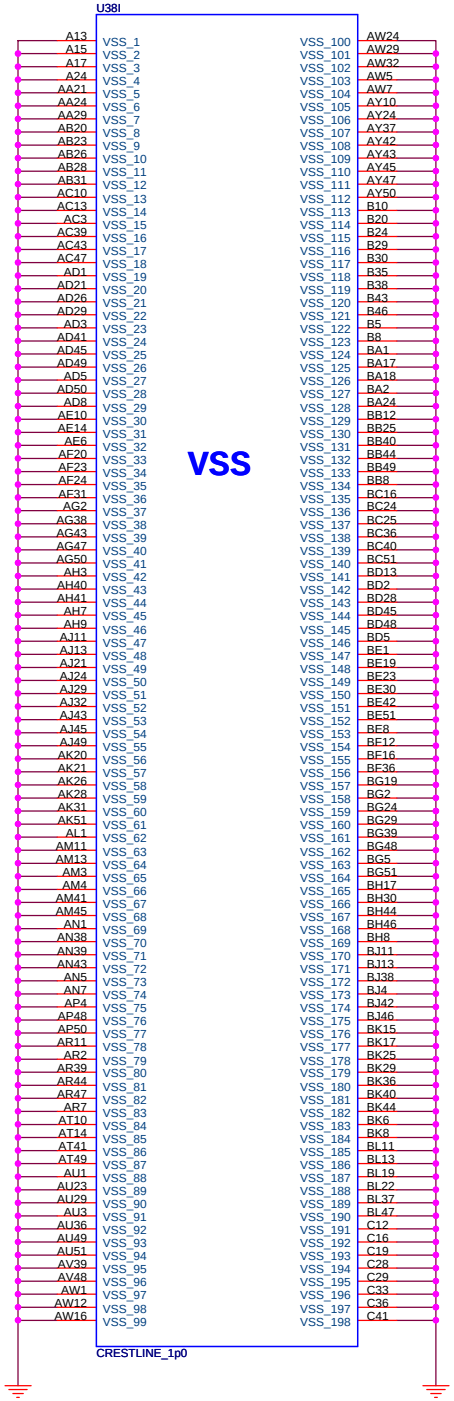
+VCC_RXR_DMI, R569 0, C227 220U/2.5V, C249 10U/6.3V, 91uH+-20%_1.5A, Ivcc_RX_DMI supply current 250mA

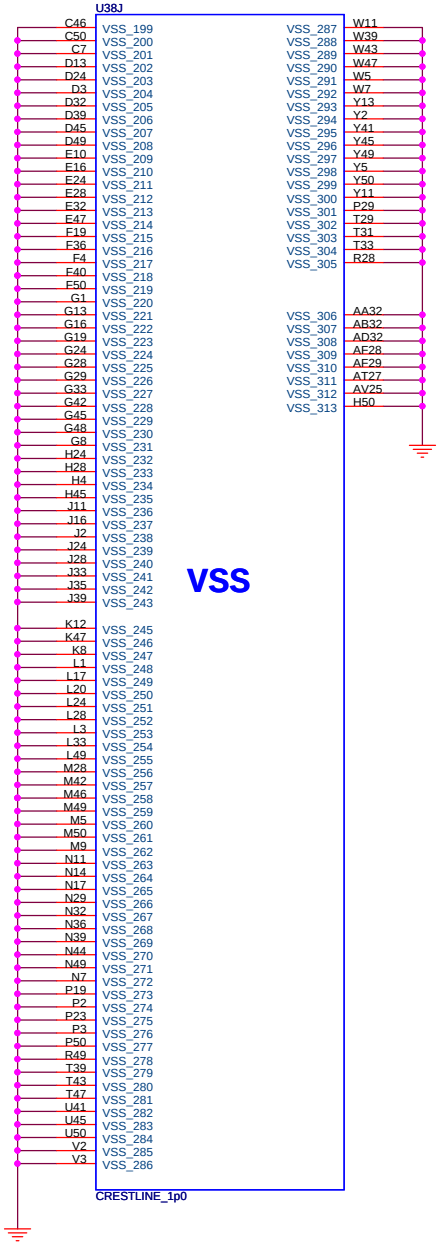
+VTTLF1, +VTTLF2, +VTTLF3, C758 0.47U/10V, C384 0.47U/10V, C742 0.47U/10V

+3V_VCC_HV, D7 CH751H-40HPT_NC, 40 mil wide, +3V_VCC_HV_L, R96 10, R478 0

VCC1.25, R158 0, +1.25V_VCC_AXF, C342 1U, C343 10U/6.3V, Place caps close to VCC_AXF

VCC1.25, L19 0, 1uH+-20%_300mA, +1.8VSUS_VCC_SM_CK, R163 1/F/0603, C334 22U/10V, C333 0.1U, +VCC_SM_CK_L, C330 10U/6.3V





Quanta Computer Inc.	
PROJECT : PB2	
Size:	Document Number: NB — Rev: A
Date: Friday, March 23, 2007	Sheet 10 of 46

Strap table

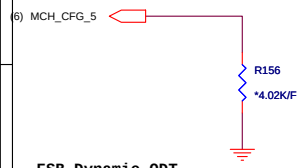
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

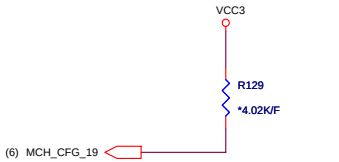
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

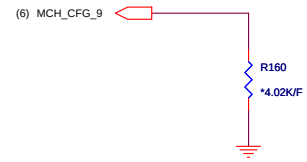


XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

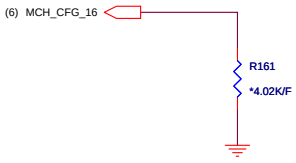


SDVO Present

Strap define at External DVI control page

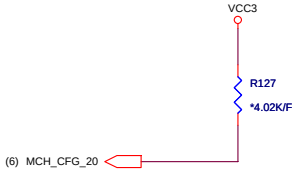
FSB Dynamic ODT

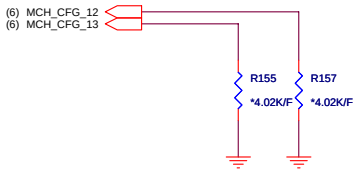
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port





Quanta Computer Inc.
PROJECT : PB2

Size	Document Number	Rev
	NB	A

Date: Friday, March 23, 2007 Sheet 11 of 46

DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

M_A_A[13..0] → M_A_A[13..0] (7,13)
SMDDR_VTERM → SMDDR_VTERM (42)

SMDDR_VTERM

C347	C408	C367	C337	C365	C353	C359	C338	C396	C335	C395	C366	C381
0.1U	0.1U	0.1U	0.1U	0.1U	0.1U	0.1U	0.1U	0.1U	0.1U	0.1U	0.1U	0.1U

(6,13) M_A_ODT0 — RP32: M_A_ODT0, M_A_A13 — RP17: M_A_A8, M_A_A5 — RP22: M_A_A3, M_A_A1 — 56X2 → SMDDR_VTERM

(6,13) M_A_CKE1 — RP13: M_A_CKE1, M_A_A11 — RP30: M_A_A10, (7,13) M_A_CAS# — RP18: M_A_A7, M_A_A6 — RP20: M_A_A2, M_A_A4 — 56X2 → SMDDR_VTERM

(7,13) M_A_RAS# — RP28: M_A_BS#1, M_A_A9 — RP14: M_A_A12, (7,13) M_A_WE# — RP26: M_A_BS#0 — 56X2 → SMDDR_VTERM

(6,13) SB_MA14 — R165 56 → SMDDR_VTERM

(6,13) SA_MA14 — R166 56

M_B_A[13..0] → M_B_A[13..0] (7,13)
1.8VSUS → 1.8VSUS (6,8,9,13,41,42)
VCC3 → VCC3 (2,3,6,8,9,11,13,14,15,16,19,20,21,22,23,24,25,26,28,30,31,33,38,40,41)

DDRII B CHANNEL

SMDDR_VTERM

C397	C379	C380	C341	C382	C394	C348	C357	C360	C404	C349	C403	C407
0.1U	0.1U	0.1U	0.1U	0.1U	0.1U	0.1U	0.1U	0.1U	0.1U	0.1U	0.1U	0.1U

Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

(7,13) M_B_BS#1 — RP23: M_B_A0, M_B_A3 — RP21: M_B_A1, M_B_A8 — RP16: M_B_A5 — 56X2 → SMDDR_VTERM

RP19: M_B_A4, M_B_A2 — RP12: M_B_A12, M_B_A9 — RP15: M_B_A7, M_B_A6 — (7,13) M_B_BS#2 — RP9 — (6,13) M_B_CKE0 — 56X2 → SMDDR_VTERM

(7,13) M_B_RAS# — RP27 — (6,13) M_B_CS#0 — RP25 — (7,13) M_B_BS#0 — (7,13) M_B_WE# — M_B_A10 — RP29 — (7,13) M_B_CAS# — 56X2 → SMDDR_VTERM

(6,13) M_A_CS#0 — RP24: M_A_A0, M_B_A13 — RP31: (6,13) M_B_ODT0, (6,13) M_B_ODT1, (6,13) M_B_CS#1 — RP33: M_ODT3 — RP34: (6,13) M_A_CS#1, (6,13) M_A_ODT1 — RP11: M_ODT1, (6,13) M_B_CKE1 — RP10: M_B_A11 — (6,13) M_A_CKE0, (7,13) M_A_BS#2 — 56X2 → SMDDR_VTERM

Quanta Computer Inc.
PROJECT : PB2

Size	Document Number	Rev
	DDR2	A

Date: Friday, March 23, 2007 Sheet 12 of 46

CGCLK_SMB
CGDAT_SMB
M_A_CKE[0..1]
M_A_CS#[0..1]
M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_CLK0
M_A_CLK0#
M_A_CLK1
M_A_CLK1#
M_A_BS#[0..2]
M_A_ODT[0..1]
M_A_DQM[0..7]
M_A_DQ[0..63]
M_A_DQS[0..7]
M_A_DQS#[0..7]
M_A_A[13..0]

M_B_CKE[0..1]
M_B_CS#[0..1]
M_B_RAS#
M_B_CAS#
M_B_WE#
M_B_CLK0
M_B_CLK0#
M_B_CLK1
M_B_CLK1#
M_B_BS#[0..2]
M_B_ODT[0..1]
M_B_DQM[0..7]
M_B_DQ[0..63]
M_B_DQS[0..7]
M_B_DQS#[0..7]
M_B_A[13..0]

VCC3
1.8VSUS

PC2100 DDR2 SDRAM SO-DIMM (200P)

DDR2-H=9.2
CN10A

CKEA 0,1
H 9.2

DDR2-H=5.2
CN9A

CKEB 0,1
H 5.2

SMBus address A4

SMBus address A0

PC2100 DDR2 SDRAM SO-DIMM (200P)

DDR2-H=9.2
CN10B

FOX P/N:DGMK0002610
TYCO P/N:DGMK0004205

C713 470P/50V
R97 0
R99 *10K/F
R477 *10K/F

PC2100 DDR2 SDRAM SO-DIMM (200P)

DDR2-H=5.2
CN9B

FOX P/N:DGMK00000C0
TYCO P/N:DGMK0000498

Place these Caps near So-Dimm1.

C738 2.2U/6.3V
C755 2.2U/6.3V
C735 2.2U/6.3V
C745 2.2U/6.3V
C741 2.2U/6.3V
C355 .1U/10V
C754 .1U/10V
C356 .1U/10V
C364 .1U/10V
C401 .1U/10V
C393 .1U/10V
C714 .1U/10V
C718 2.2U/6.3V
C436 2.2U/6.3V
C439 .1U/10V

SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

Place these Caps near So-Dimm2.

C744 2.2U/6.3V
C739 2.2U/6.3V
C743 2.2U/6.3V
C752 2.2U/6.3V
C734 2.2U/6.3V
C400 .1U/10V
C753 .1U/10V
C383 .1U/10V
C369 .1U/10V
C345 .1U/10V
C346 .1U/10V
C255 .1U/10V
C247 2.2U/6.3V
C437 2.2U/6.3V
C440 .1U/10V

SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm2
No Vias Between the Trace of PIN to CAP.

Quanta Computer Inc.
PROJECT : PB2

Size	Document Number	Rev
	DDR2	A
Date: Friday, March 23, 2007	Sheet 13 of 46	

YELLOW BLOCK is for G8X chip only

80mA

45mA

40mA

300mA

need add to 3v 120mA

40mA

40mA

NB8X:VCC1.8
G73:VCC2.5

Modify 09/27

NB8X:VGA1.2
G73:VCC2.5

YELLOW BLOCK is for G8X chip only

U31D

U_GPU_G3

OPTION SIGNAL FROM NB FOR UMA VGA

OPTION SIGNAL FROM Nvidia to VGA

G73 use 150/301 ohm
NB8X use 0 ohm

NB8P-SE P/N:AJB8PSE0T02
NB8M-SE P/N:AJB8MSE0T02

FOR IFPC VDD LEAKAGE CIRCIUT

Quanta Computer Inc.		
PROJECT : PB2		
Size	Document Number: VGA	Rev: A
Date: Friday, March 23, 2007	Sheet 14 of 46	

NB8M-SE:"0x0428" Please set to "1000"
NB8P-SE DevID "0x0425",
Set to "0101",R57 no stuff ,R445 and R446 stuff 2kohm

U31E

15mil

MIOA_VDDQ_0 MIOA_VDDQ_1 MIOA_VDDQ_2 MIOA_VDDQ_3 MIOA_VDDQ_4
MIOACAL_PU_GND MIOACAL_PD_VDDQ MIOA_VREF
MIOAD
MIOA_HSYNC MIOA_VSYNC MIOA_DE MIOA_CTL3 MIOA_CLKOUT MIOA_CLKOUT# MIOA_CLKIN

15mil

MIOB_VDDQ_0 MIOB_VDDQ_1 MIOB_VDDQ_2 MIOB_VDDQ_3 MIOB_VDDQ_4
MIOBCAL_PD_VDDQ MIOBCAL_PU_GND MIOB_VREF
MIOBD
MIOB_VSYNC MIOB_HSYNC MIOB_DE MIOB_CTL3 MIOB_CLKOUT MIOB_CLKOUT# MIOB_CLKIN

THERMAL GPIO
CLAMP I2CC_SCL I2CC_SDA GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO11 GPIO12

JTAG_TCK JTAG_TMS JTAG_TDI JTAG_TDO JTAG_TRST#
STRAP
ROM
RFU6 RFU7 RFU8 RFU9 RFU10 RFU11 RFU12 RFU13 RFU14 RFU15 RFU16 RFU17 RFU18 RFU19 RFU20
MEMSTRAPSEL0 MEMSTRAPSEL1 MEMSTRAPSEL2 MEMSTRAPSEL3
ROMCS# ROM_SI ROM_SO ROM_SCLK I2CH_SCL I2CH_SDA
BUFRST# STEREO SWAPRDY_A TESTMEMCLK TESTMODE

U_GPU_G3

MIOA_CKI T21

GREEN BLOCK can remove if use G8X

MIOBD7 pull down and MIOB_DE pull up from nvidia HANK recommend

9/28 modify

GFX_VID0
H : Low Voltage
L : Normal Voltage

VGACORECTL	G86
HI	1.15V
LO	1.2V

YELLOW BLOCK is for G8X chip only

GREEN BLOCK can remove if use G8X

P/N:AR0AT7RB013
U21 AT88SC0808C AR0AT7RB013
for HDMI function

PCI_DEVICE[3:0]	DESCRIPTION	
1000	NB8M-SE	G86-700-AX
0101	NB8P-SE	G86-770-AX
0111	NB8M-GS	G86-730-AX
others	Reserved	

12/14 modify

PCI_DEVICE[3:0]
Default are "0",can remove pull down resister from nvidia HANK recommend

RAM_CFG0 RAM_CFG1 RAM_CFG2 RAM_CFG3
PCI_DEVICE0 PCI_DEVICE1 PCI_DEVICE2 PCI_DEVICE3
SLOT_CLOCK_CFG
SUB_VENDOR

SHARE M/B SYSTEM BIOS, SUB VENDOR ID NEED PULL DOWN .

GPIO1 PULL DOWN strap can be remove from nvidia HANK recommend

NB8M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infineon
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

NB8P VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infineon
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infineon
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix

Boot Status

ACIN	GPIO12
H	H
L	L

1/24 modify
FOR BATTERY MODE FUNCTION
GFX_GPIO12=H ENABLE
GFX_GPIO12=L DISABLE

1/5 modify

Default are "0",can remove pull down resister from nvidia HANK recommend

VGA THERMAIL CIRCUIT

Quanta Computer Inc.
PROJECT : PB2

Size	Document Number	Rev
	VGA	A
Date: Friday, March 23, 2007	Sheet 15 of 46	

Channel C is available on G73M only

NB8M:
Stuff 5pcs 0.1u caps on FBVTT power rail

U31B

U31C

FBA

FBC

U_GPU_G3

PLACE NEAR GPU

PLACE NEAR GPU

C686 *220U/6.3V

GREEN BLOCK can remove if use G8X

YELLOW BLOCK is for G8X chip only

For EMI

15mil

For NB8M
Stuff 1k ohm on R407,R408
and 0.1u C659 For NB8M-SE

VREF = FBVDDQ * Rbot/(Rtop + Rbot)

stuff 40.2ohm on R43 and R41 for NB8M-SE

F_VREF2 filter can be remove from nvidia HANK recommend

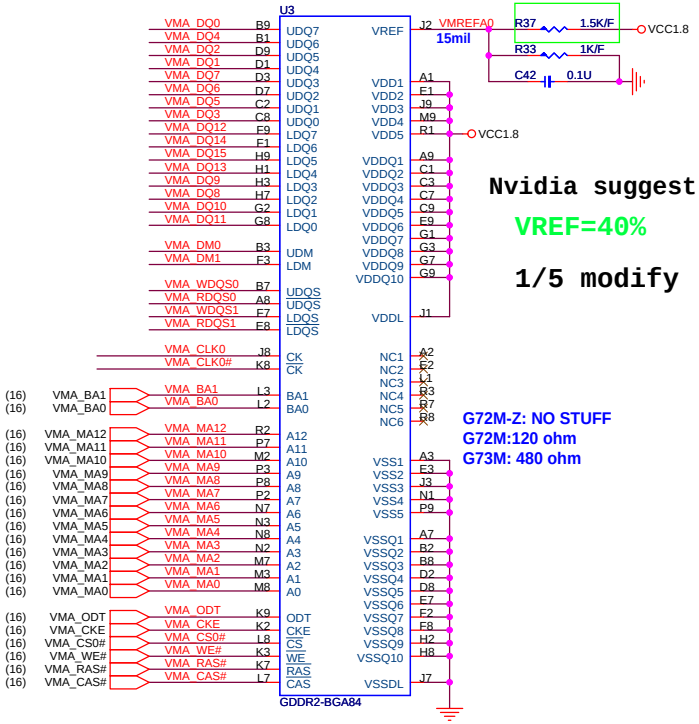
G70,G71: Stuff these parts
G72M,G73M : NC

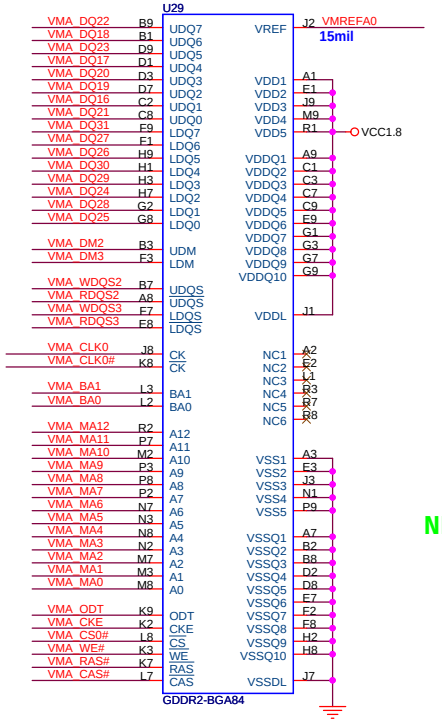
NB8M: use R438
NB8P: A02 use R438

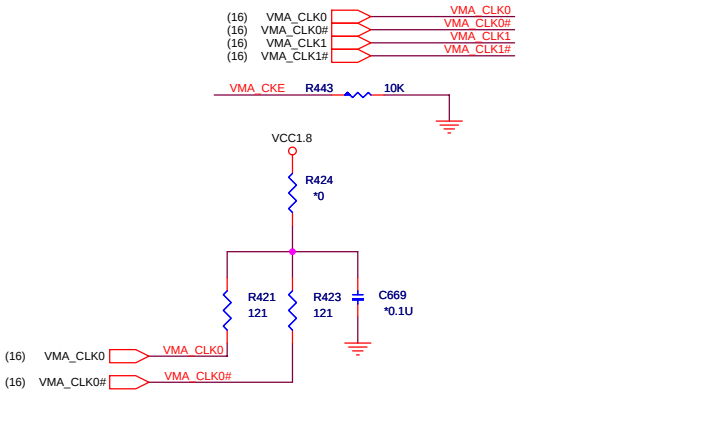
Modify 1/5

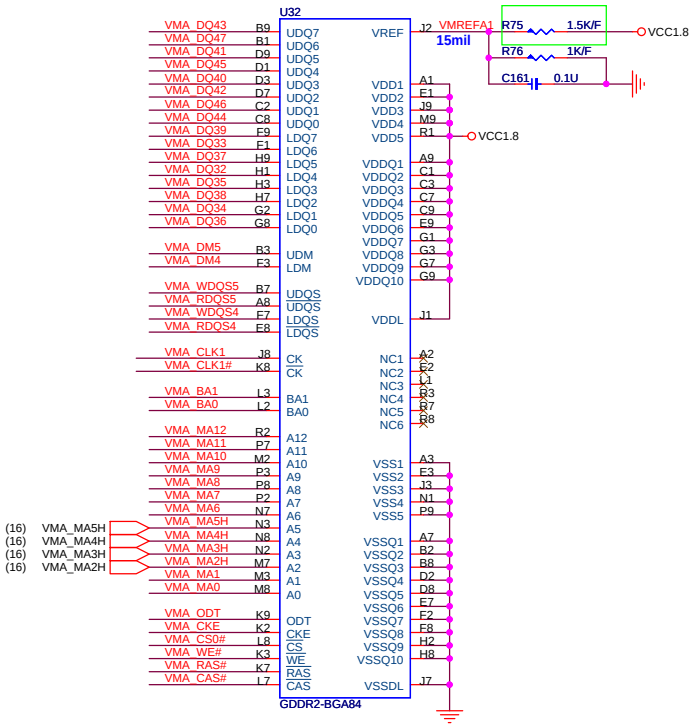
NB8M: use R23
NB8P: A02 use R23

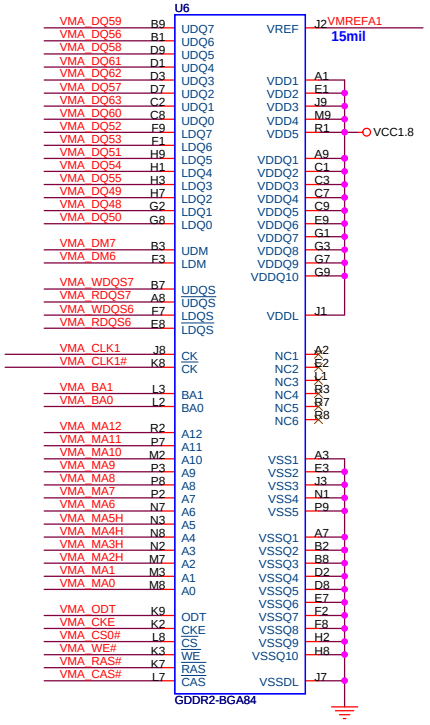
Quanta Computer Inc.		
PROJECT : PB2		
Size	Document Number: VGA	Rev: A
Date: Friday, March 23, 2007	Sheet 16 of 46	

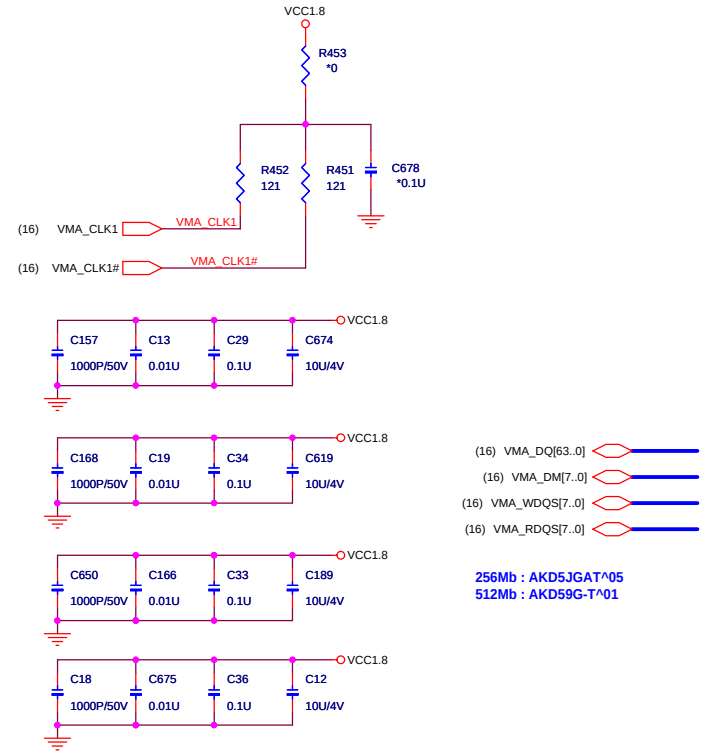










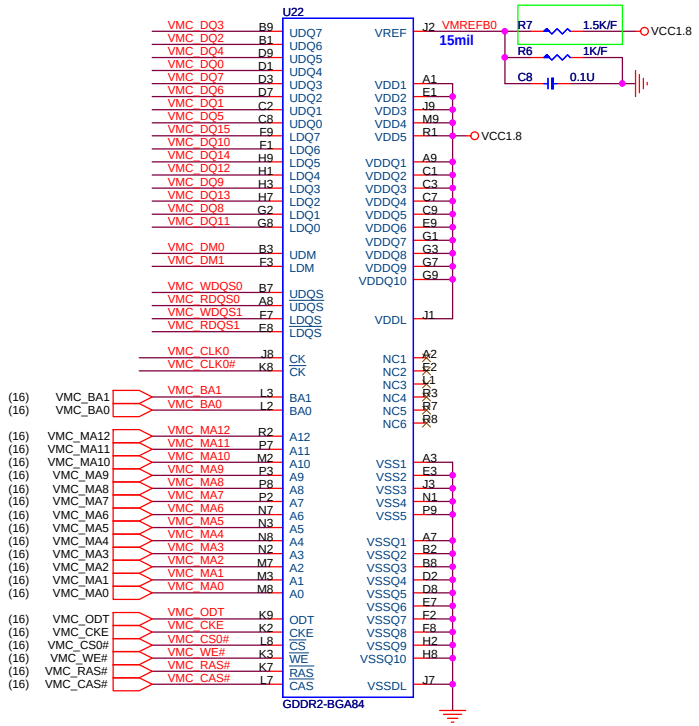


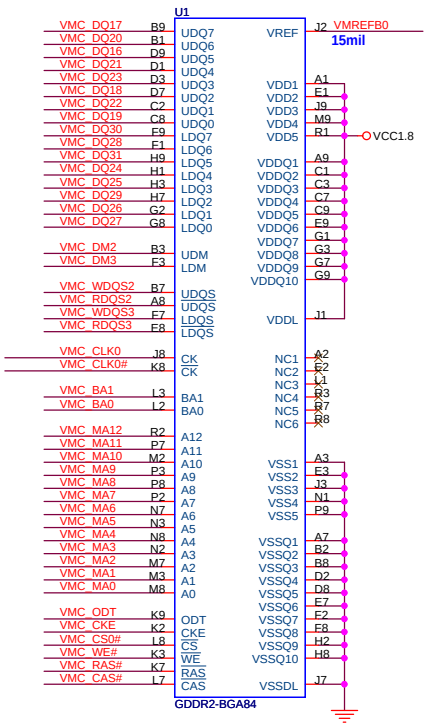
Quanta Computer Inc.

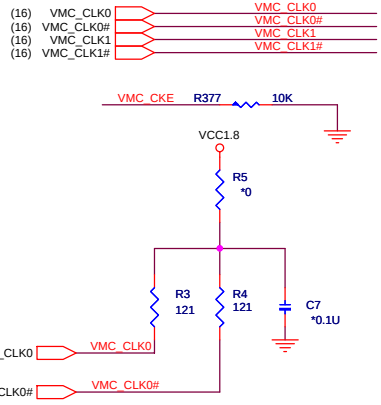
PROJECT : PB2

Size	Document Number	Rev
	VGA	A

Date: Friday, March 23, 2007 Sheet 17 of 46

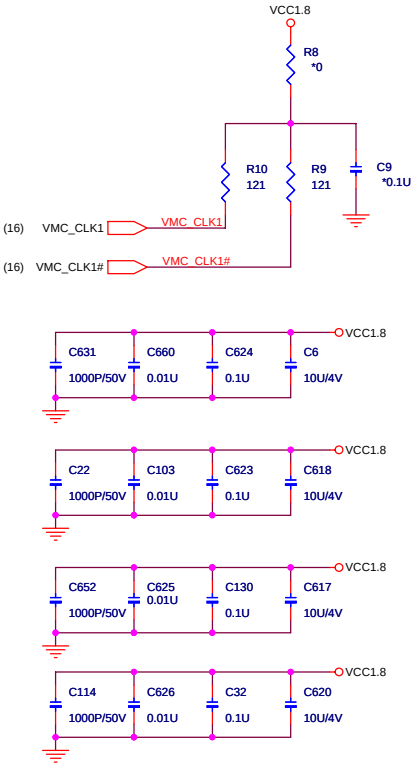




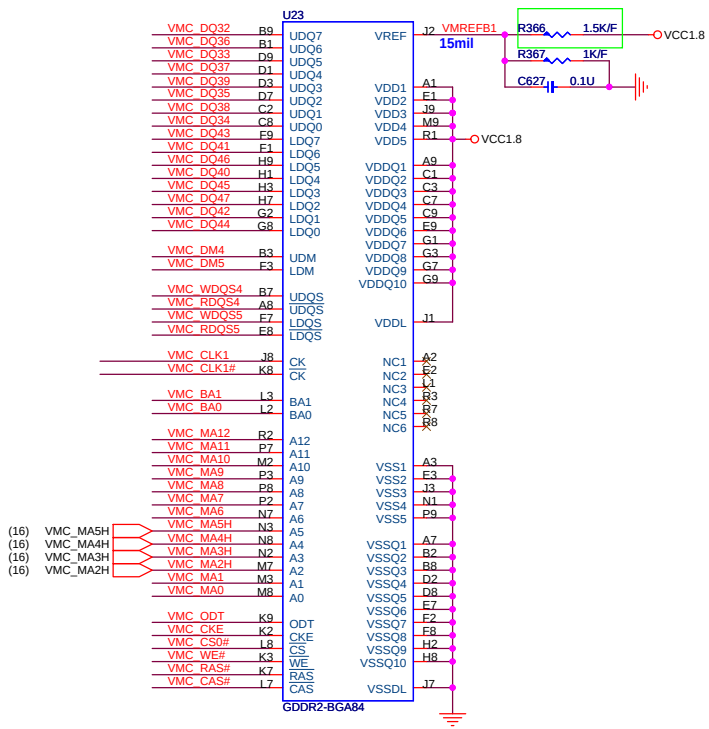


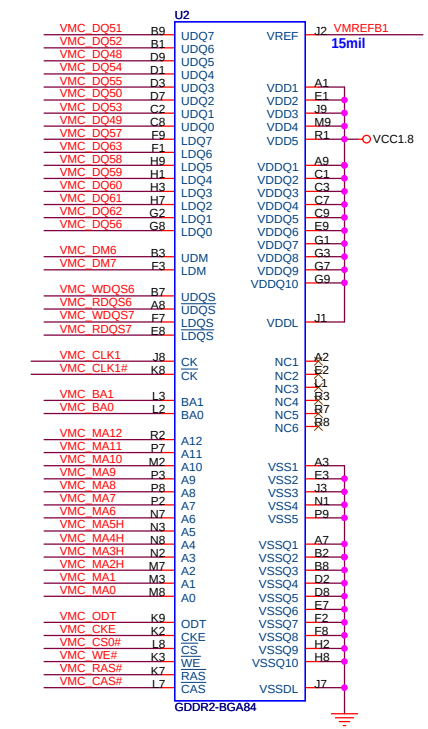
1/23 modify

Stuff 121 ohm on R3,R4,R9,R10



256Mb : AKD5JGAT^05
512Mb : AKD59G-T^01





Quanta Computer Inc.			
PROJECT : PB2			
Size	Document Number: VGA		Rev: A
Date: Friday, March 23, 2007		Sheet 18 of 46	

U31F

U_GPU_G3

U31A

PCIE

U_GPU_G3

500mA

1500mA

180mA

20mA

PLACE NEAR GPU

G8X Total power consumption
1.NVDD CORE POWER 1.2 - 1.0 -- 11.01A
2.PCIE VGA1.2V -- 1.75A
3.FBVDDQ 1.8V ----- 3.12A
4.VDD I/O 3.3V ---- 0.49A
5.PLL 2.5V ---

power up sequence

I/O 3.3V
NVCORE
1.8VFBDDQ
1.2V
2.5V

For 3.3V swing, we can remove R97, R104 and R98 and replace R? with 0 Ohm resistor.

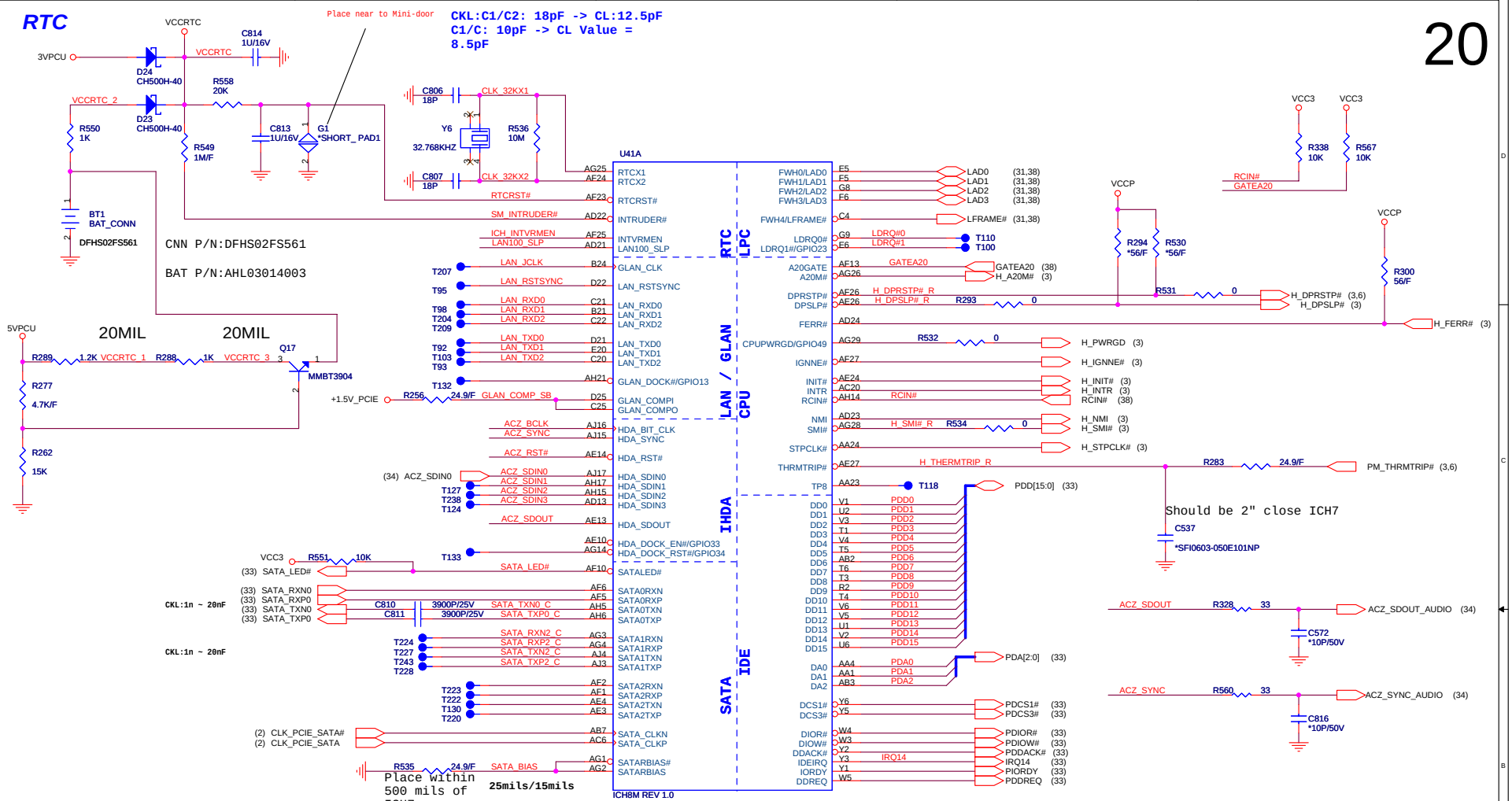
G73M: R58
NB8X: R54
10/24 modify

Quanta Computer Inc.
PROJECT : PB2

Size	Document Number	Rev
	VGA	A

Date: Friday, March 23, 2007 Sheet 19 of 46

RTC



ICH8M P/N:AJ0QM740T40

SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

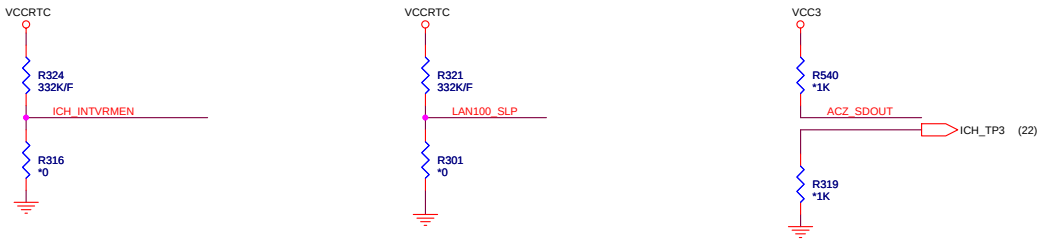
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1



Quanta Computer Inc.			
PROJECT : PB2			
Size	Document Number		Rev
	ICH8_M		A
Date: Friday, March 23, 2007		Sheet 20 of 46	

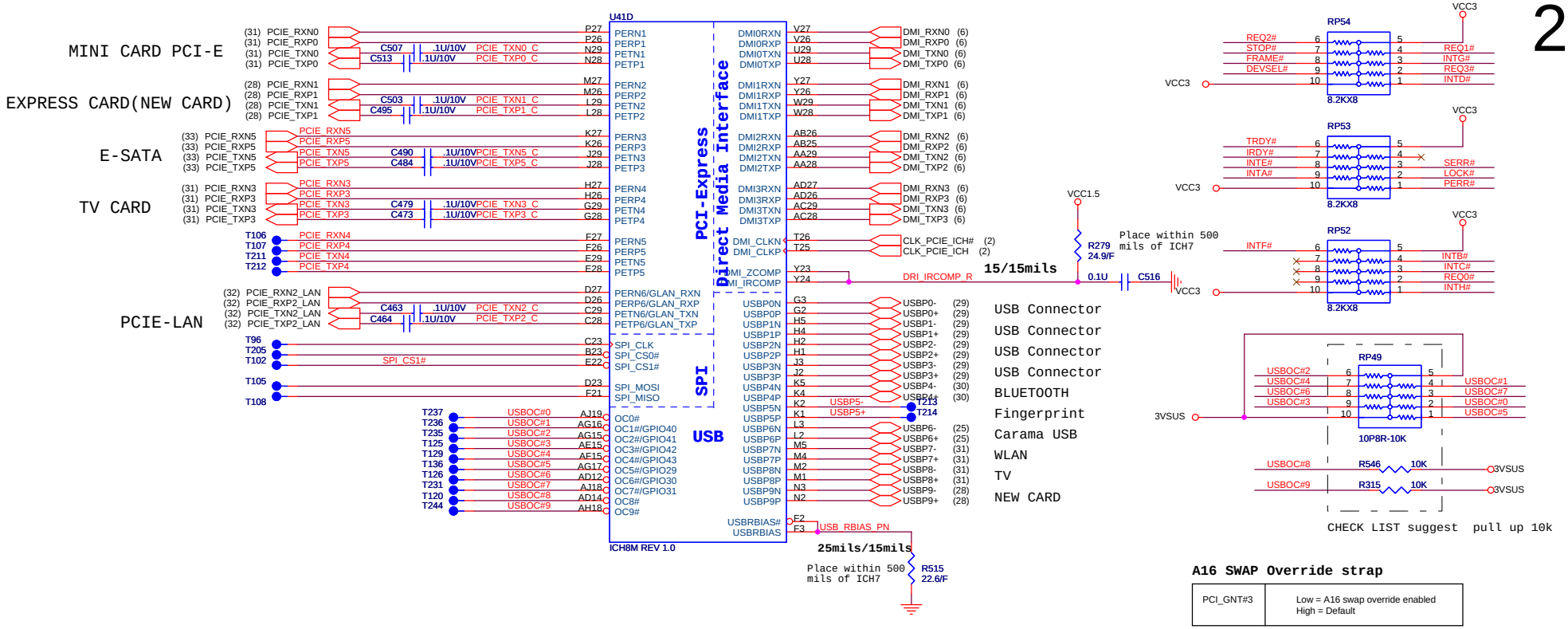
MINI CARD PCI-E

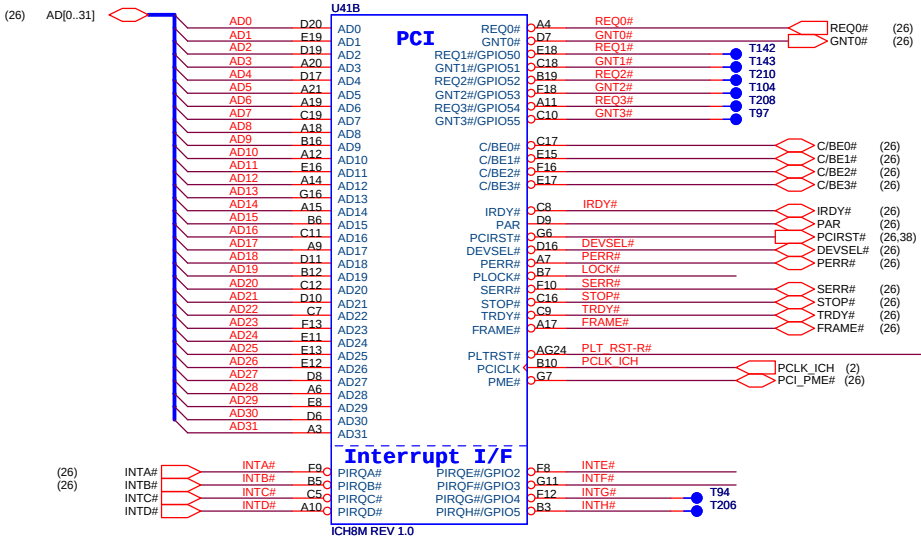
EXPRESS CARD(NEW CARD)

E-SATA

TV CARD

PCIE-LAN





A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

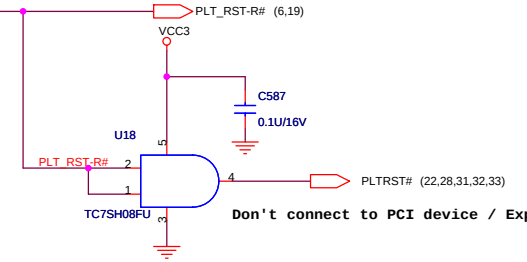
GNT3# R252 *1K

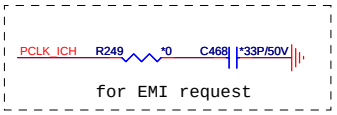
ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R257 *1K

GNT0# R251 *1K



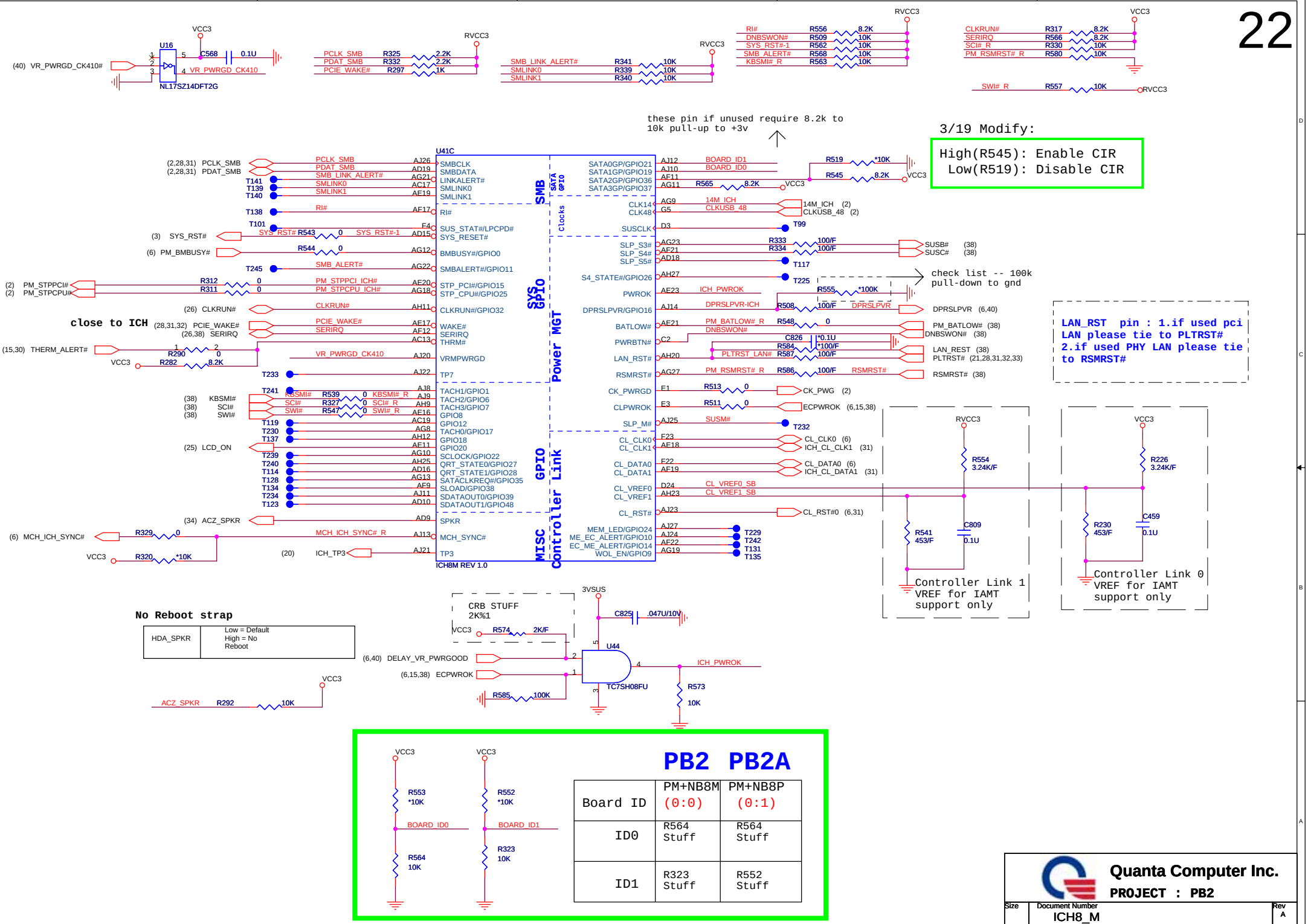


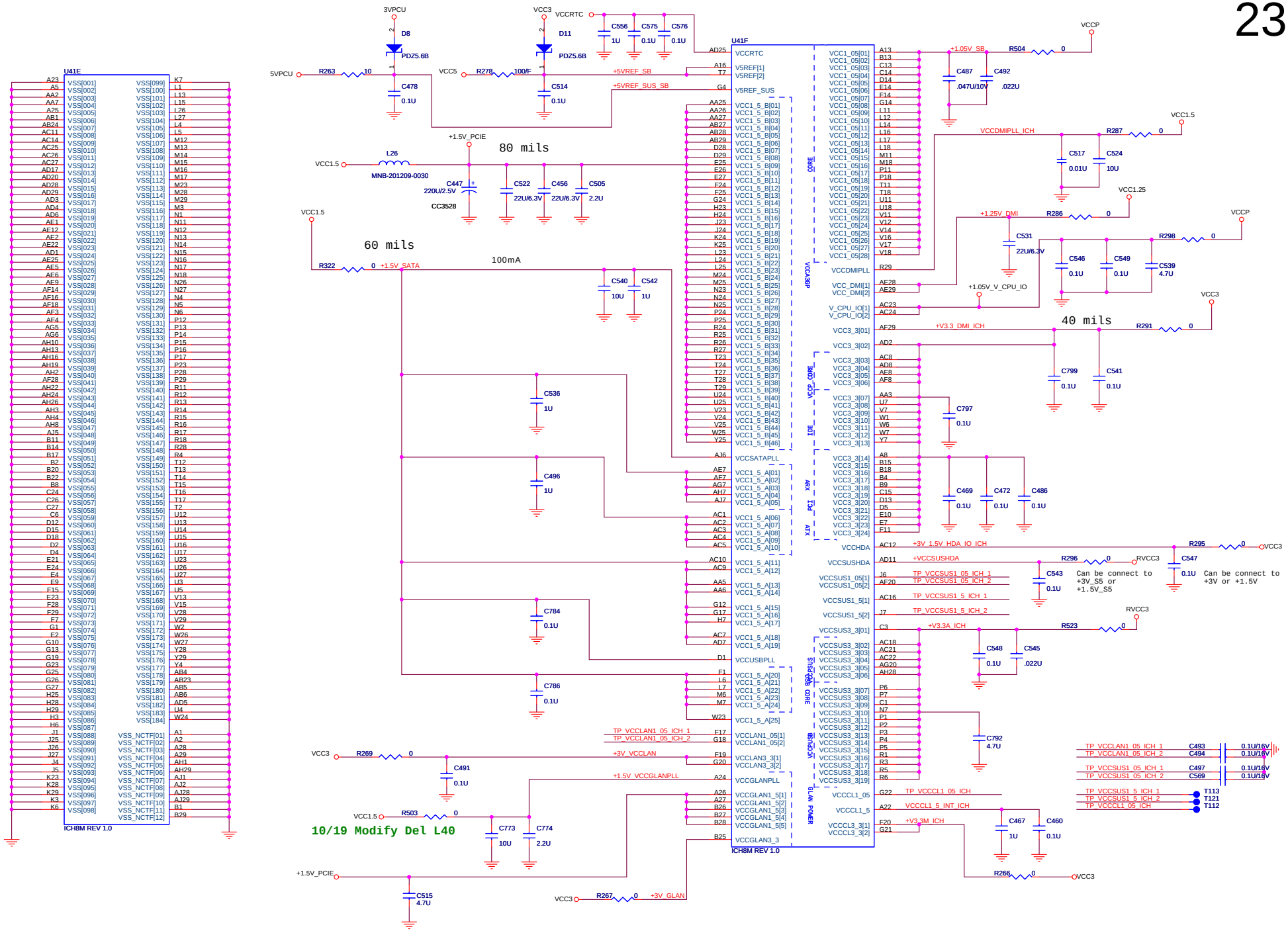
Quanta Computer Inc.

PROJECT : PB2

Size	Document Number	Rev
	ICH8_M	A

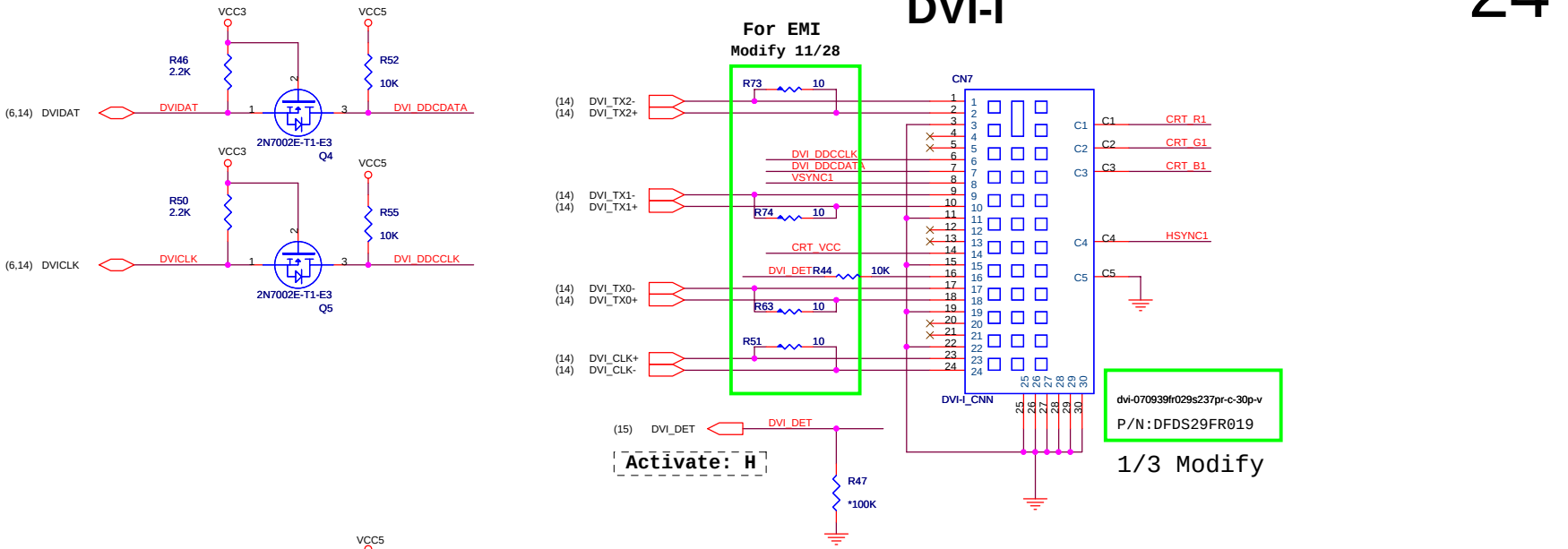
Date: Friday, March 23, 2007 Sheet 21 of 46

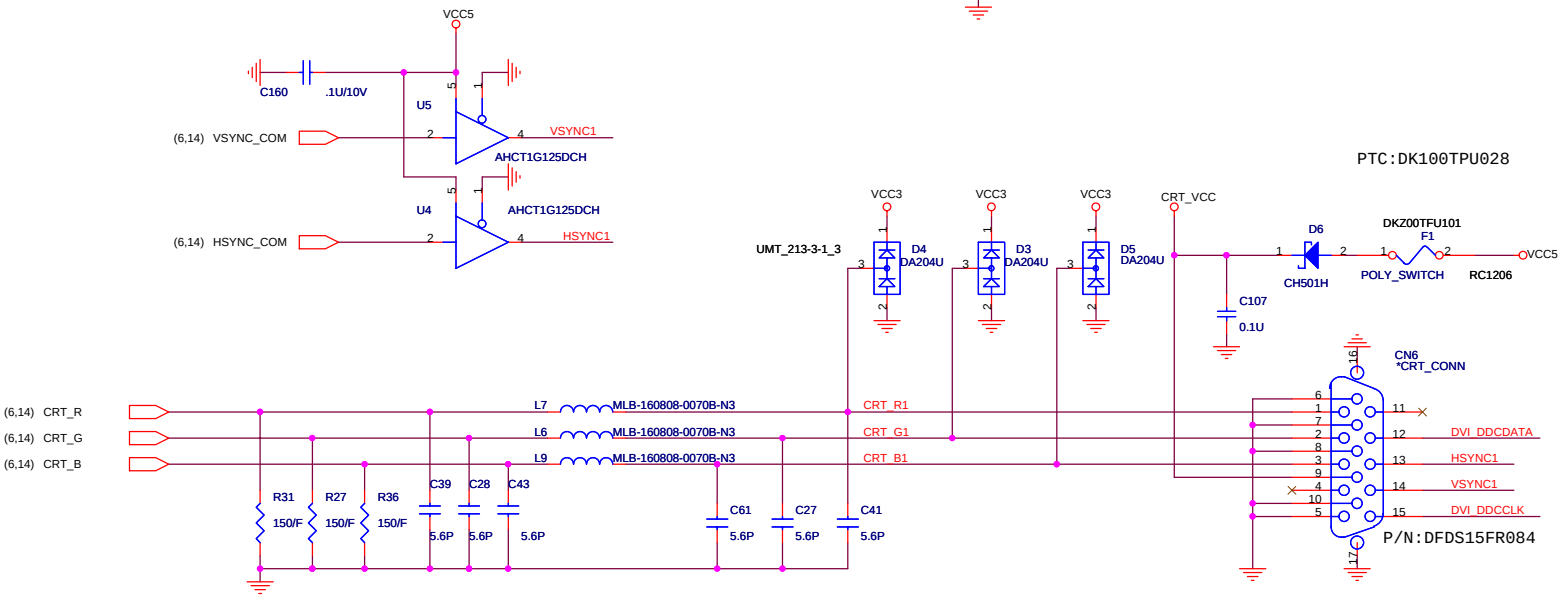

U16
NL17SZ14DFT2G
C568 0.1U
(40) VR_PWRGD_CK410#
VR_PWRGD_CK410
PCLK_SMB R325 2.2K
PDAT_SMB R332 2.2K
PCIE_WAKE# R297 1K
SMB_LINK_ALERT# R341 10K
SMLINK0 R339 10K
SMLINK1 R340 10K
RI# R556 8.2K
DNBSWON# R509 10K
SYS_RST#-1 R562 10K
SMB_ALERT# R568 10K
KBSMI#_R R563 10K
CLKRUN# R317 8.2K
SERIRQ R566 8.2K
SCI#_R R330 10K
PM_RSMRST#_R R580 10K
SWI#_R R557 10K
these pin if unused require 8.2k to 10k pull-up to +3v
3/19 Modify:
High(R545): Enable CIR
Low(R519): Disable CIR
U41C
ICH8M REV 1.0
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
close to ICH
check list -- 100k pull-down to gnd
LAN_RST pin : 1.if used pci LAN please tie to PLTRST#
2.if used PHY LAN please tie to RSMRST#
Controller Link 1 VREF for IAMT support only
Controller Link 0 VREF for IAMT support only
No Reboot strap
HDA_SPKR
Low = Default
High = No Reboot
CRB STUFF 2K%1
U44
TC7SH08FU
PB2 PB2A
Board ID
PM+NB8M (0:0)
PM+NB8P (0:1)
ID0
ID1
R564 Stuff
R323 Stuff
R552 Stuff
Quanta Computer Inc.
PROJECT : PB2
Size
Document Number
ICH8_M
Rev A
Date: Friday, March 23, 2007
Sheet 22 of 46



Quanta Computer Inc.			
PROJECT : PB2			
Size	Document Number		Rev
	ICH8_M		A
Date: Friday, March 23, 2007		Sheet 23 of 46	

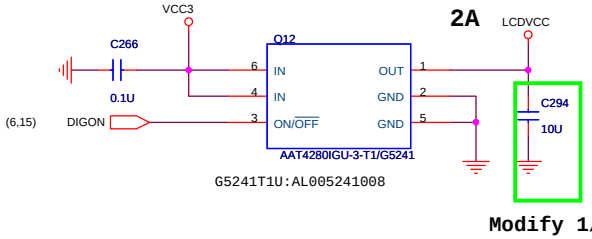
DVI-I





Quanta Computer Inc.		
PROJECT : PB2		
Size	Document Number: DVI/CRT	Rev: A
Date: Friday, March 23, 2007	Sheet 24 of 46	

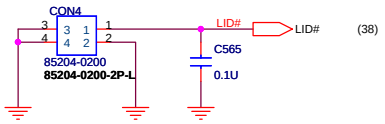
PANEL VCC CONTROL



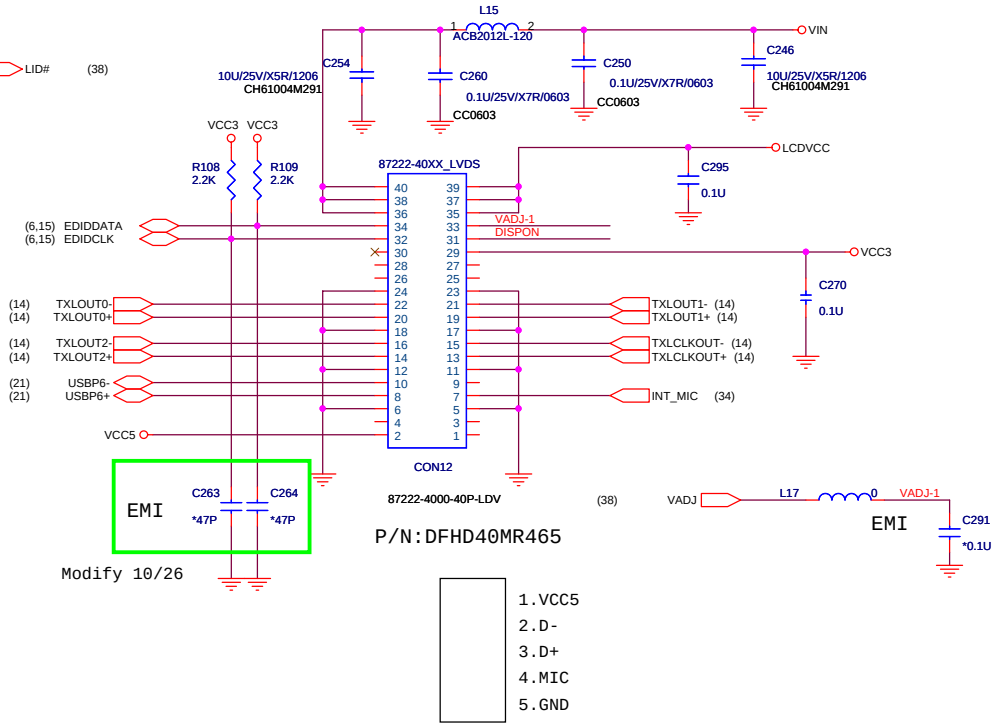
G5241T1U:AL005241008

Modify 1/24

LID



LCD CONNECTOR

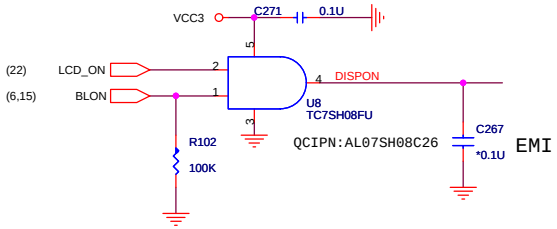


P/N:DFHD40MR465

Modify 10/26

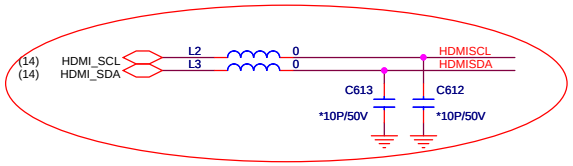
1.VCC5
2.D-
3.D+
4.MIC
5.GND

BACKLIGHT CONTROL

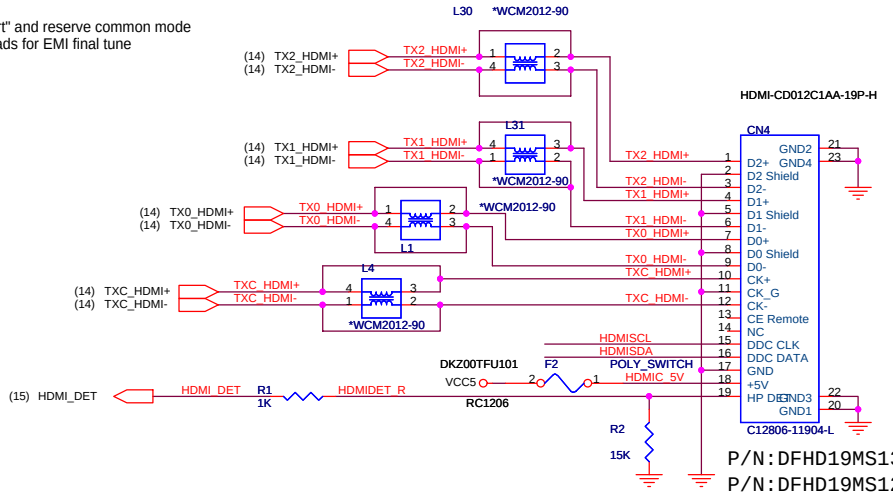


QCIPN:AL07SH08C26

DB "short" and reserve common mode choke pads for EMI final tune

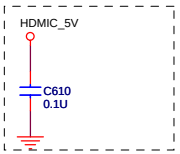


For HDMI Nvidia's PUN issue



P/N:DFHD19MS135 All
P/N:DFHD19MS127

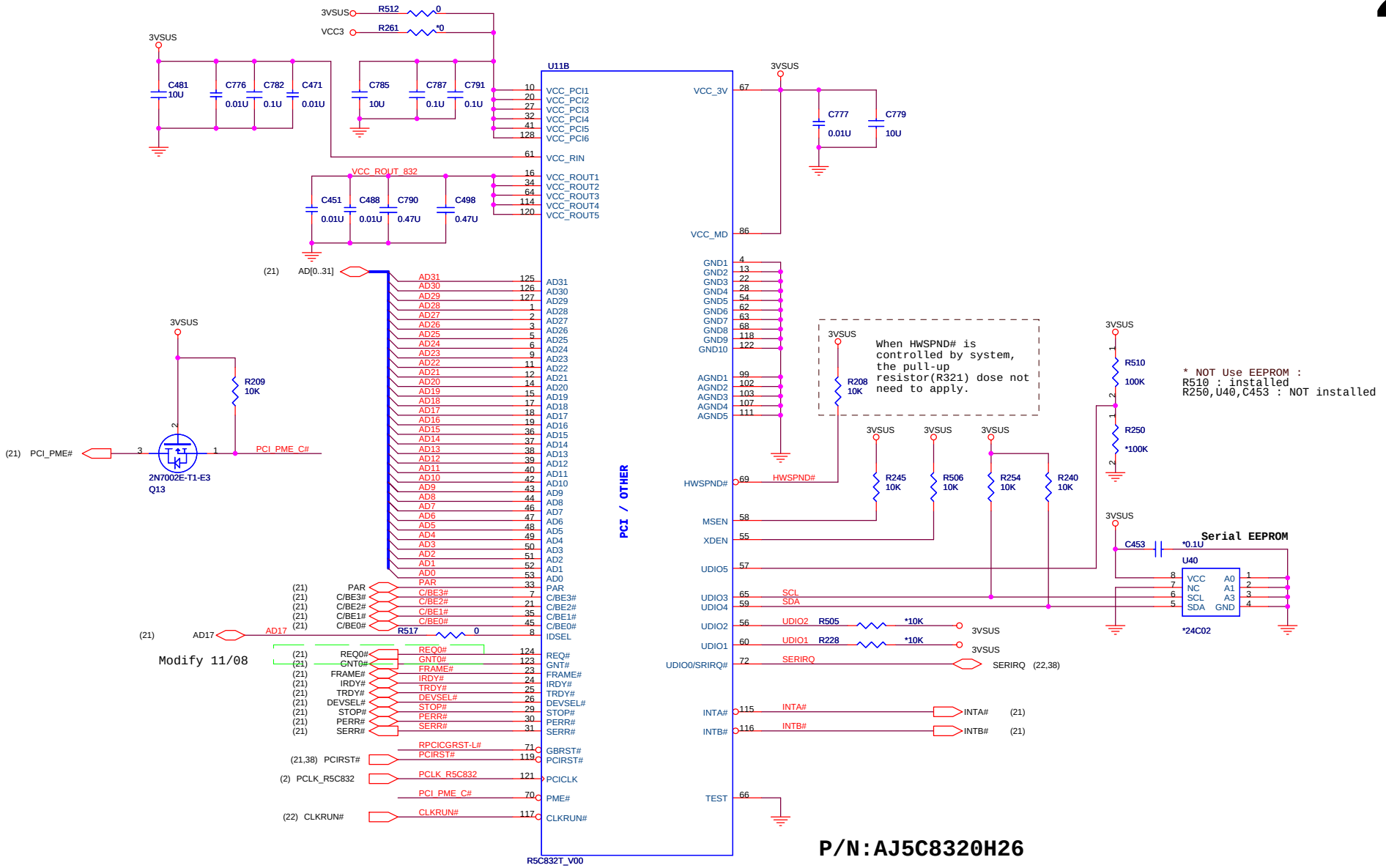
HDMI PORT



for EMI request

Quanta Computer Inc.
PROJECT : PB2

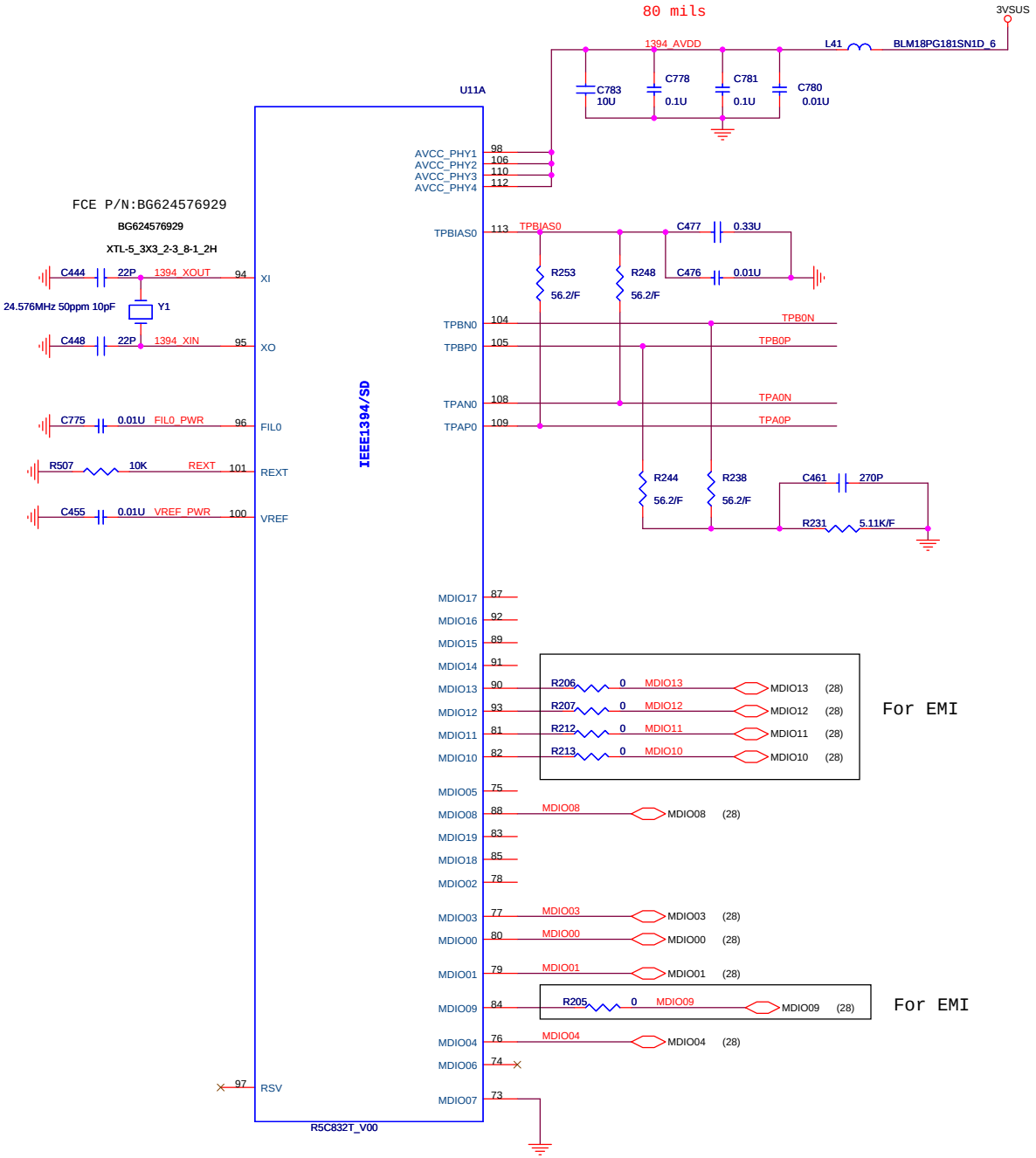
Size	Document Number	Rev
	LCD / HDMI	A
Date: Friday, March 23, 2007	Sheet 25 of 46	



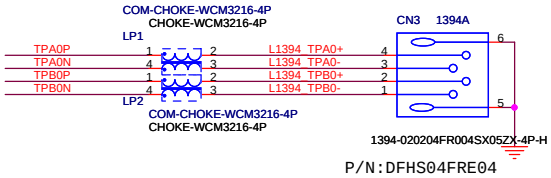
Quanta Computer Inc.
PROJECT : PB2

Size	Document Number	Rev
	R5C832	A

Date: Friday, March 23, 2007 Sheet 26 of 46



AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.



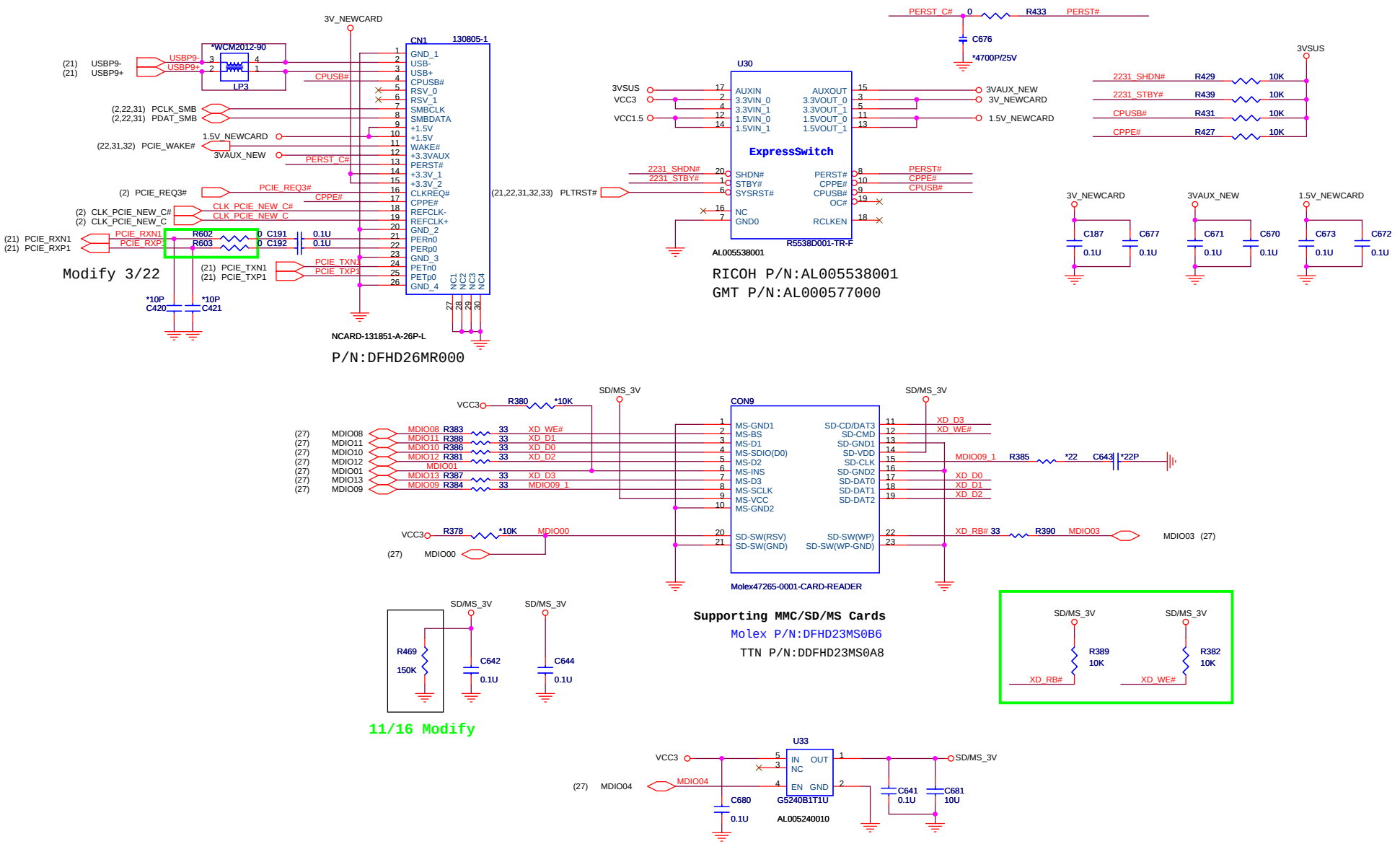
P/N:DFHS04FRE04

	Vendor ID	Device ID
1394	1180	0832
SD	1180	0822
MMC	1180	0843
MS	1180	0592
xD	1180	0852

Quanta Computer Inc.
PROJECT : PB2

Size	Document Number	Rev
	R5C832	A

Date: Friday, March 23, 2007 Sheet 27 of 46



Quanta Computer Inc.		
PROJECT : PB2		
Size	Document Number R5C832	Rev A
Date: Friday, March 23, 2007	Sheet 28 of 46	

PTC:DK100TPU028

USB Back

40 mils

DKZ00TFU101
F3
5VSUS
POLY_SWITCH
RC1206
USBVCC0
C257 0.1U
C265 100U/6.3V-3528

LP5
(21) USBP0-
(21) USBP0+
*WCM2012-90
C269 *47P/50V
C272 *47P/50V
40 mils
CON13
USB VERTICAL
DFHS04FRH14
P/N:DFHS04FRH14
D28 *DA204U
D27 *DA204U

INT KeyBoard

1/3 Modify

CON5
AFN240-A2G1T-24P-L
AFN240-A2G1T-24P-L-kw3
P/N:DFFC24FR181
Bot contact

220Px4 CP1
220Px4 CP2
220Px4 CP4
220Px4 CP3
220Px4 CP5
220Px4 CP6

RP50 10KX8
RP51 10KX8
RP48 10KX8

3/19 Modify

CIR

5VPCU
R468 *10K
(38) CIR_IN
R583
20 mlis
U45
VCC
OUT
GND
GND
IR-IRM-V538-TR1
IR-IRM-V538-TR1-3P-pb2
BEBK0076Z00
C829 10U
C828 0.1U

TOP
1 2 3
4

1/3 Modify

USB Right

5VSUS
120 mils
C593 10U
C590 0.1U
DFHS24FR536
87153-2401-24P-LDV
(21) USBP1-
(21) USBP1+
(21) USBP2-
(21) USBP2+
(21) USBP3-
(21) USBP3+
(34) HP-JD
(35) HPOUT_L
(35) HPOUT_R
(34) EXT_MIC_L
(34) EXT_MIC_R
(34) MIC1-JD
AGND
CON18

M/B
TOP VIEW
USB/B
TOP VIEW

SWITCH BOARD

11/06 Modify

(38) NUMLED#
3VPCU VCC5 5VPCU
C684 0.1U
C218 0.1U
C719 0.1U

30 mils
CON2
3VPCU
5VPCU
VCC5
(38) NBSWON#
(38) ECO
(38) RF_SW
(38) MODE_ON#
(38) SUSLED#
(38) ECO_LED#
(38) RF_LED#
(38) MODE_LED#
(38) CAPSLED#
(38) BATLED0#
(38) BATLED1#
(33) ODD_LED#
SW
AF720L-A2G1T-20P-L

Bot contact
P/N:DFFC20FR255

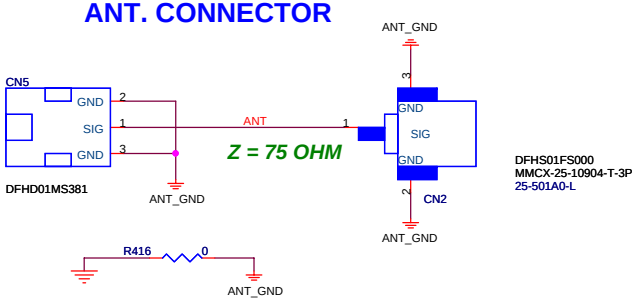
SW/B Blue: B Amber:A

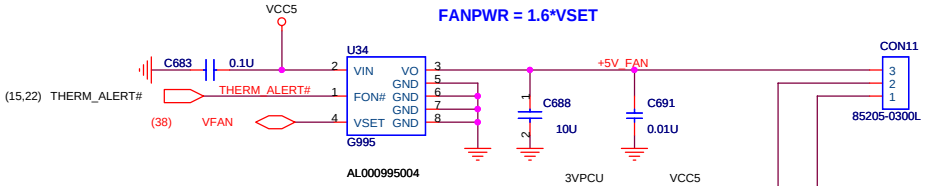
WIFI	Power	ECO	FUNC	NUM LED	CAP LED	BAT LED	ODD LED
B	B	B	B	B	B	B/A	B

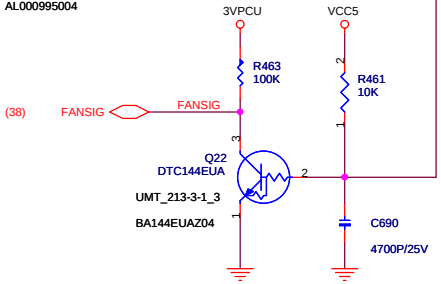
Quanta Computer Inc.	PROJECT : PB2	
Size	Document Number: K/B / USB	Rev: A
Date: Friday, March 23, 2007	Sheet 29 of 46	

FAN CONN

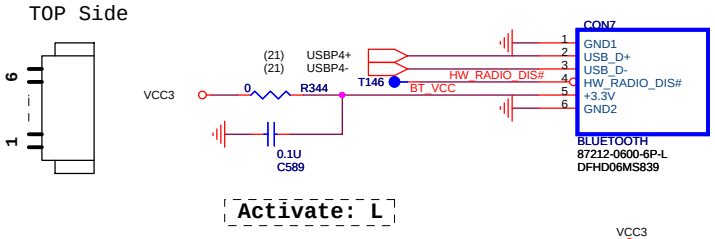
ANT. CONNECTOR

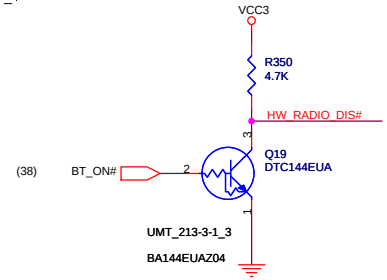




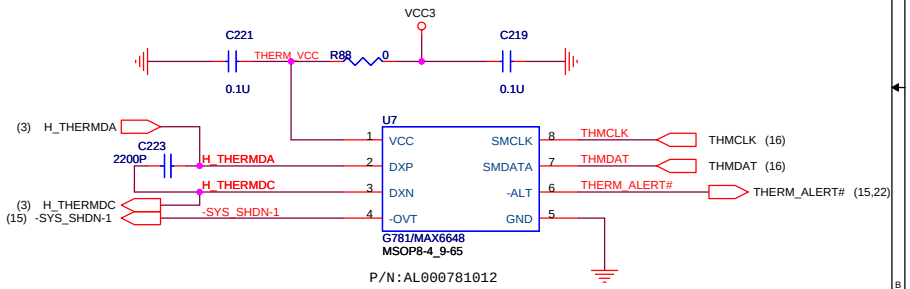


BT Connector

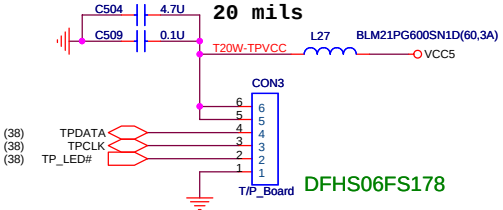


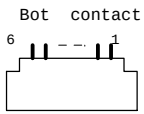


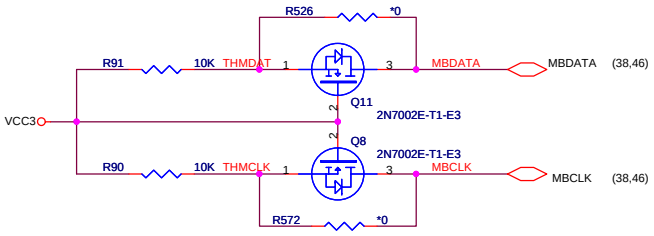
Thermal Senser

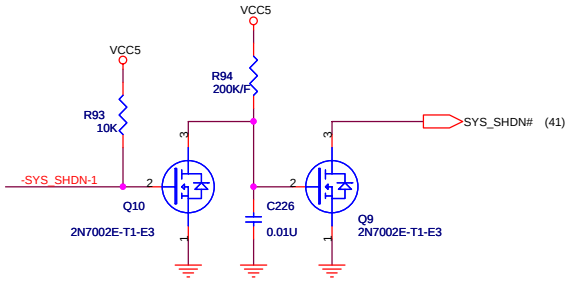


TOUCH PAD





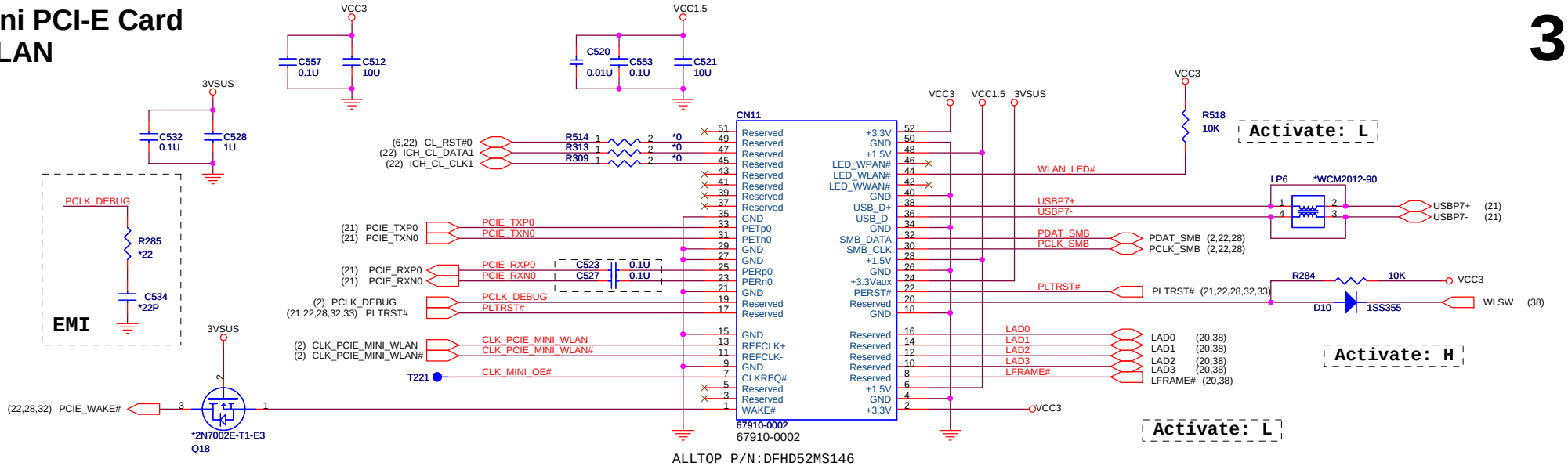




Quanta Computer Inc.
PROJECT : PB2

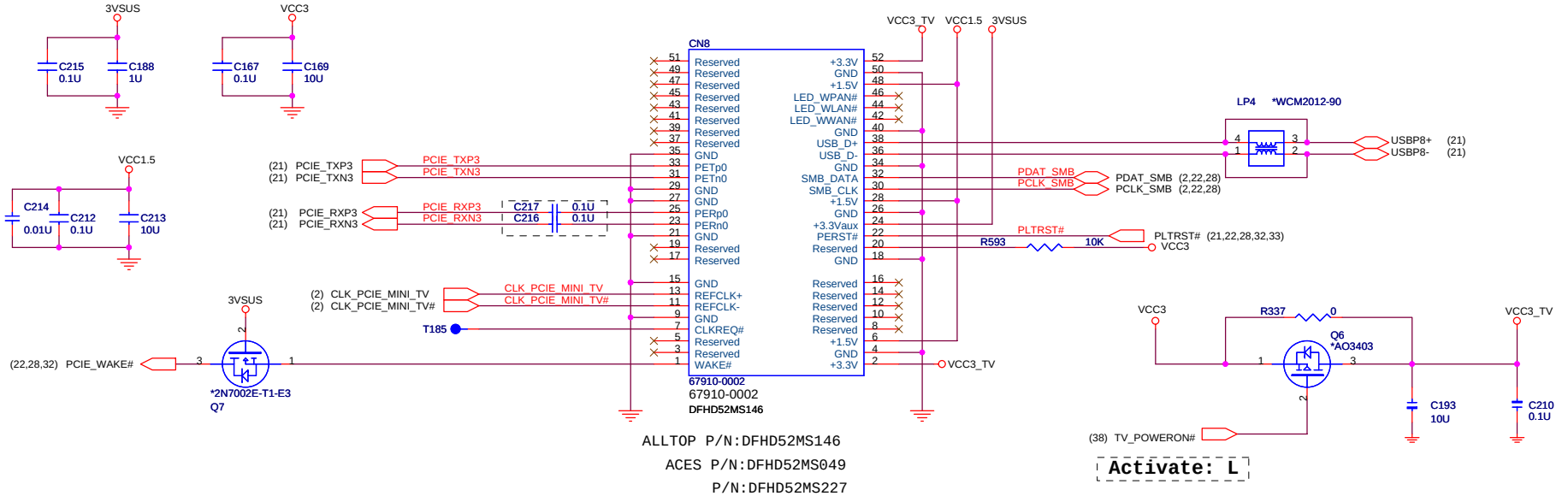
Size	Document Number	Rev
	FAN/BT/FG	A
Date: Friday, March 23, 2007	Sheet 30 of 46	

Mini PCI-E Card
WLAN



ALLTOP P/N:DFHD52MS146
ACES P/N:DFHD52MS049
P/N:DFHD52MS227

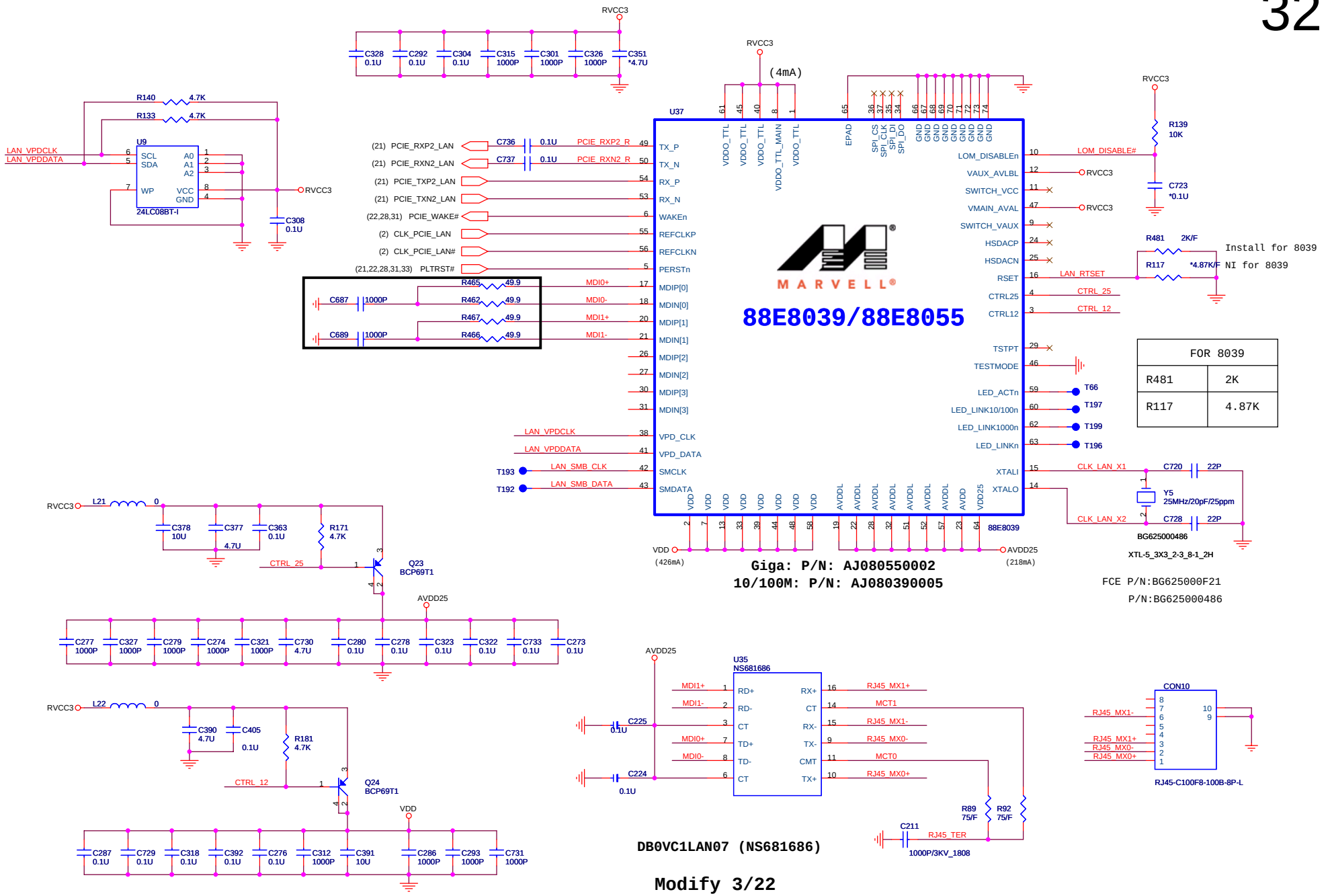
Mini PCI-E Card TV



ALLTOP P/N:DFHD52MS146
ACES P/N:DFHD52MS049
P/N:DFHD52MS227

Quanta Computer Inc.
PROJECT : PB2

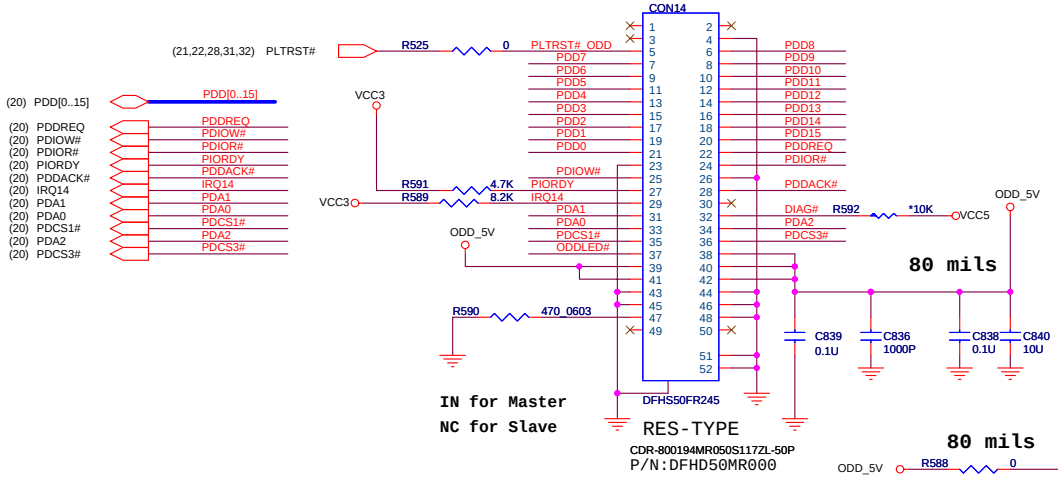
Size	Document Number	Rev
	WIRELESS/ TV	A
Date: Friday, March 23, 2007	Sheet 31 of 46	



Quanta Computer Inc.		
PROJECT : PB2		
Size	Document Number: Marvell 8039/55	Rev A
Date: Friday, March 23, 2007	Sheet 32 of 46	

CD-ROM CONNECTOR

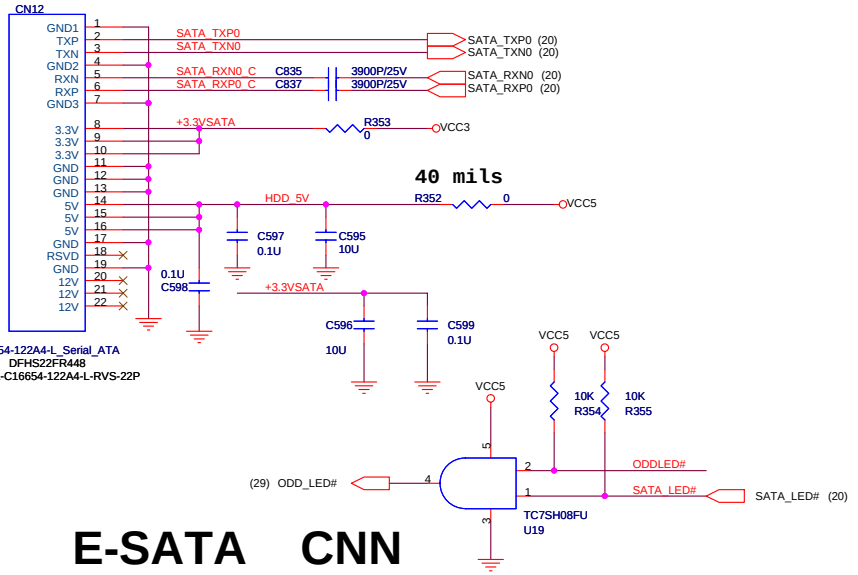
SMT TYPE CNN



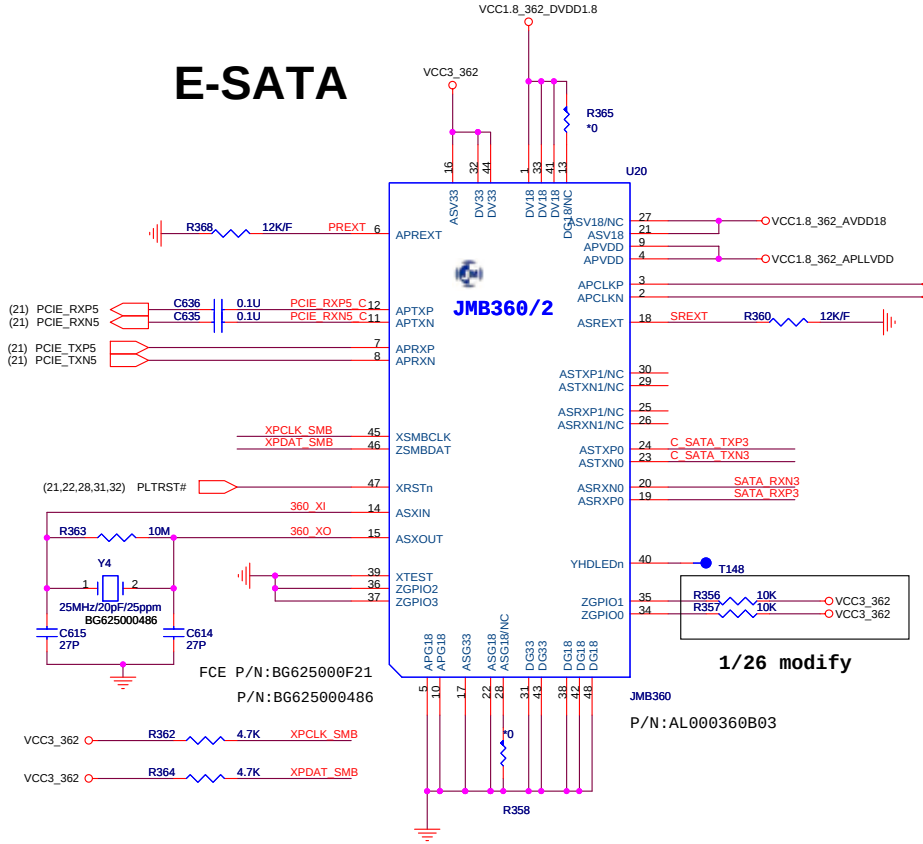
SATA HDD

10/19 Modify H=4.5mm

P/N:DFHS22FR448 REF: ZC3

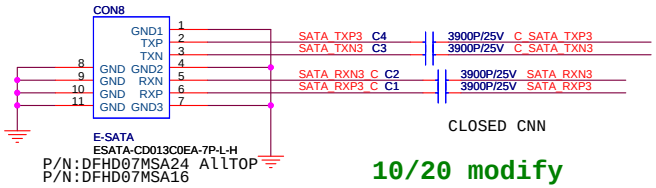


E-SATA



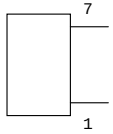
1/26 modify

E-SATA CNN

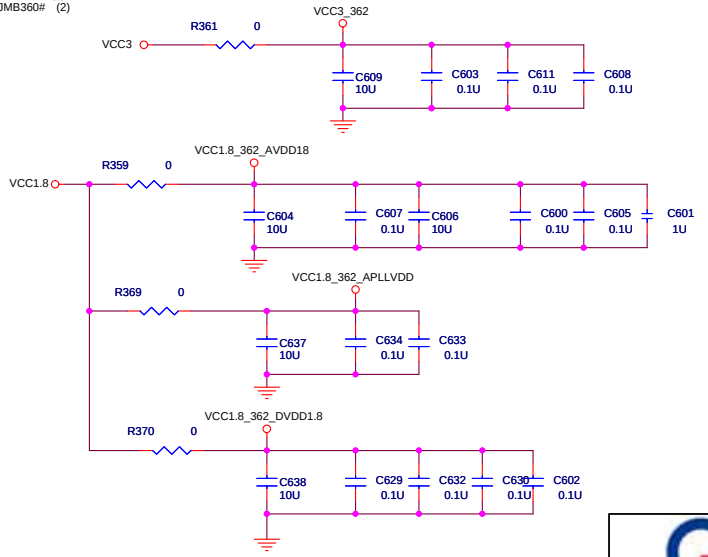


CLOSED CNN

Bottom Side



10/20 modify

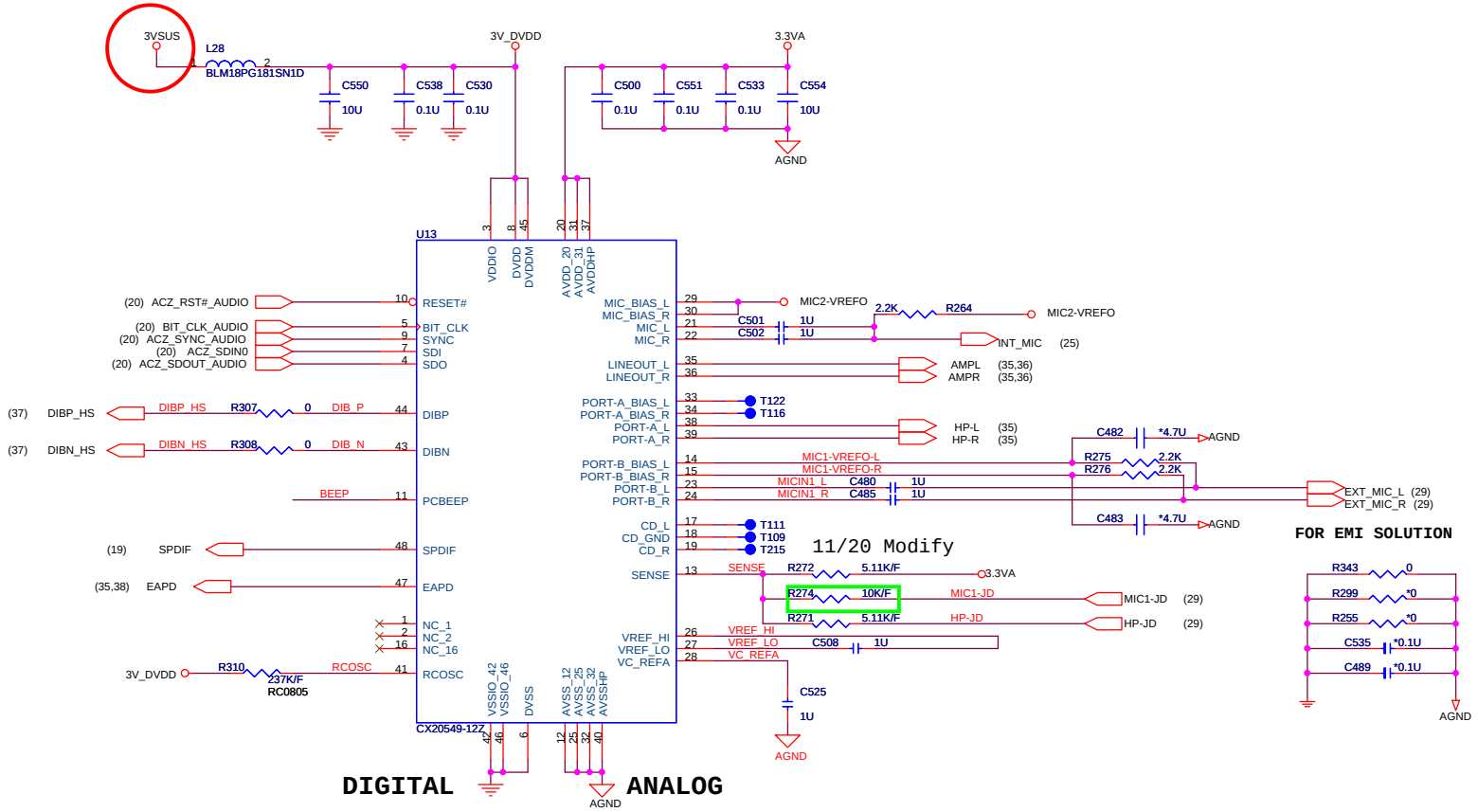


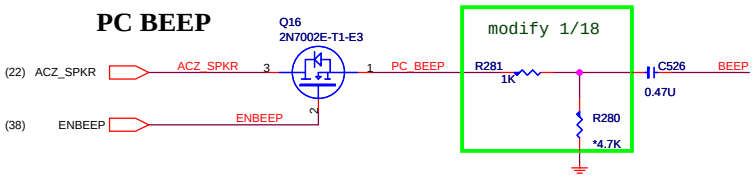
Quanta Computer Inc.

PROJECT : PB2

Size	Document Number	Rev
	ODD/SATA	A

Date: Friday, March 23, 2007 Sheet 33 of 46



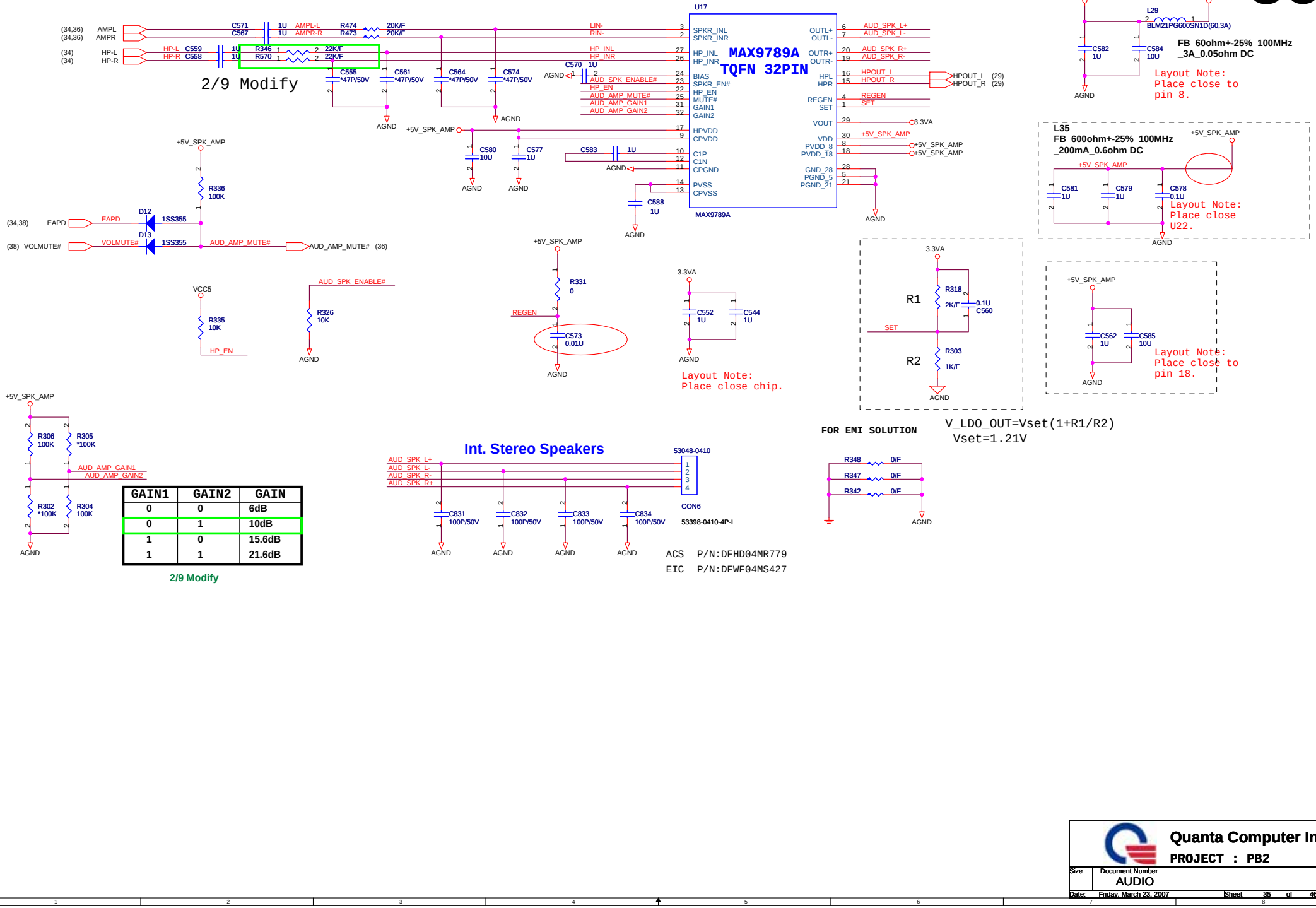


Quanta Computer Inc.
PROJECT : PB2

Size	Document Number	Rev
	AUDIO	A

Date: Friday, March 23, 2007 Sheet 34 of 46

AUDIO AMPLIFIER



Quanta Computer Inc.

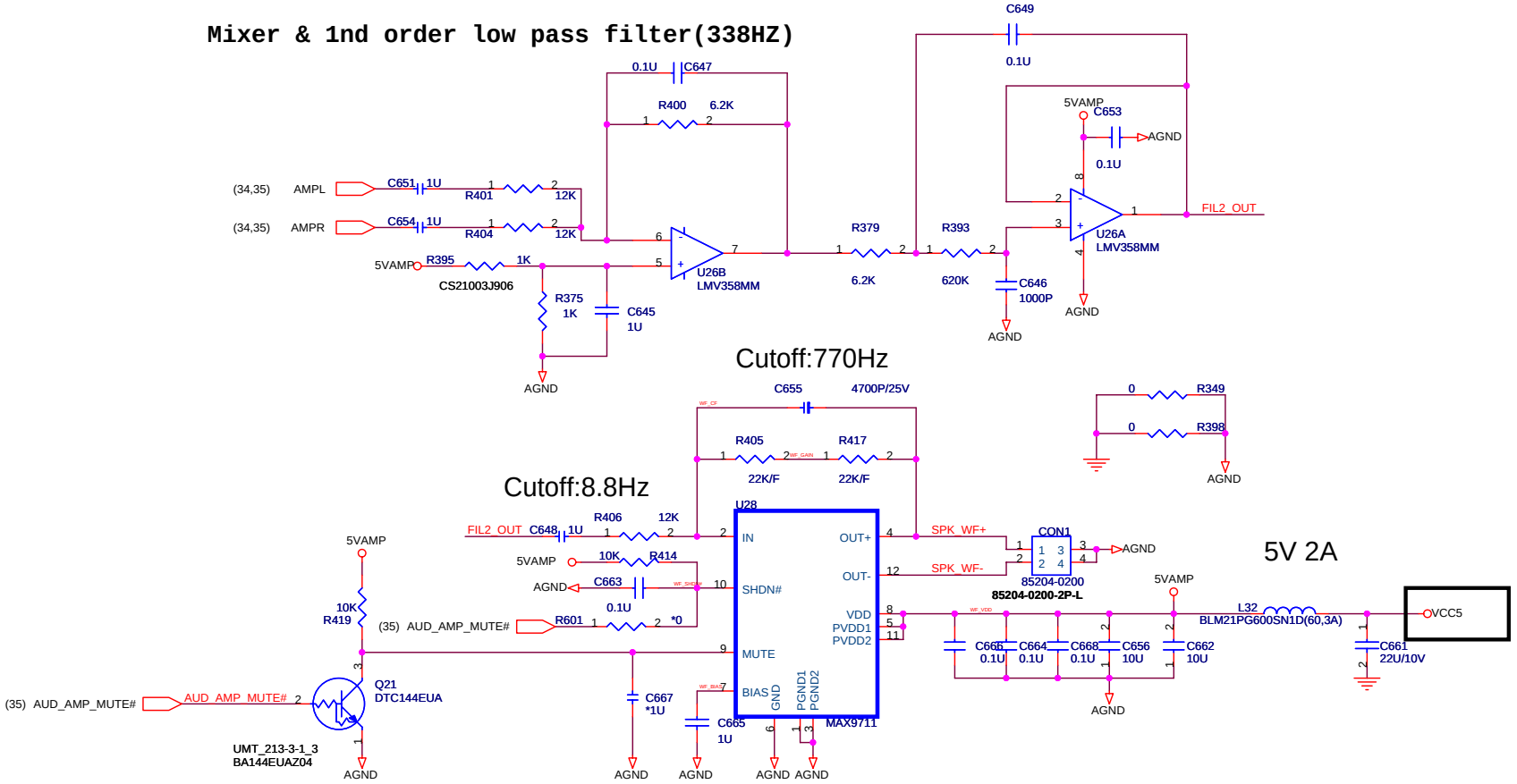
PROJECT : PB2

Size	Document Number	Rev
	AUDIO	A

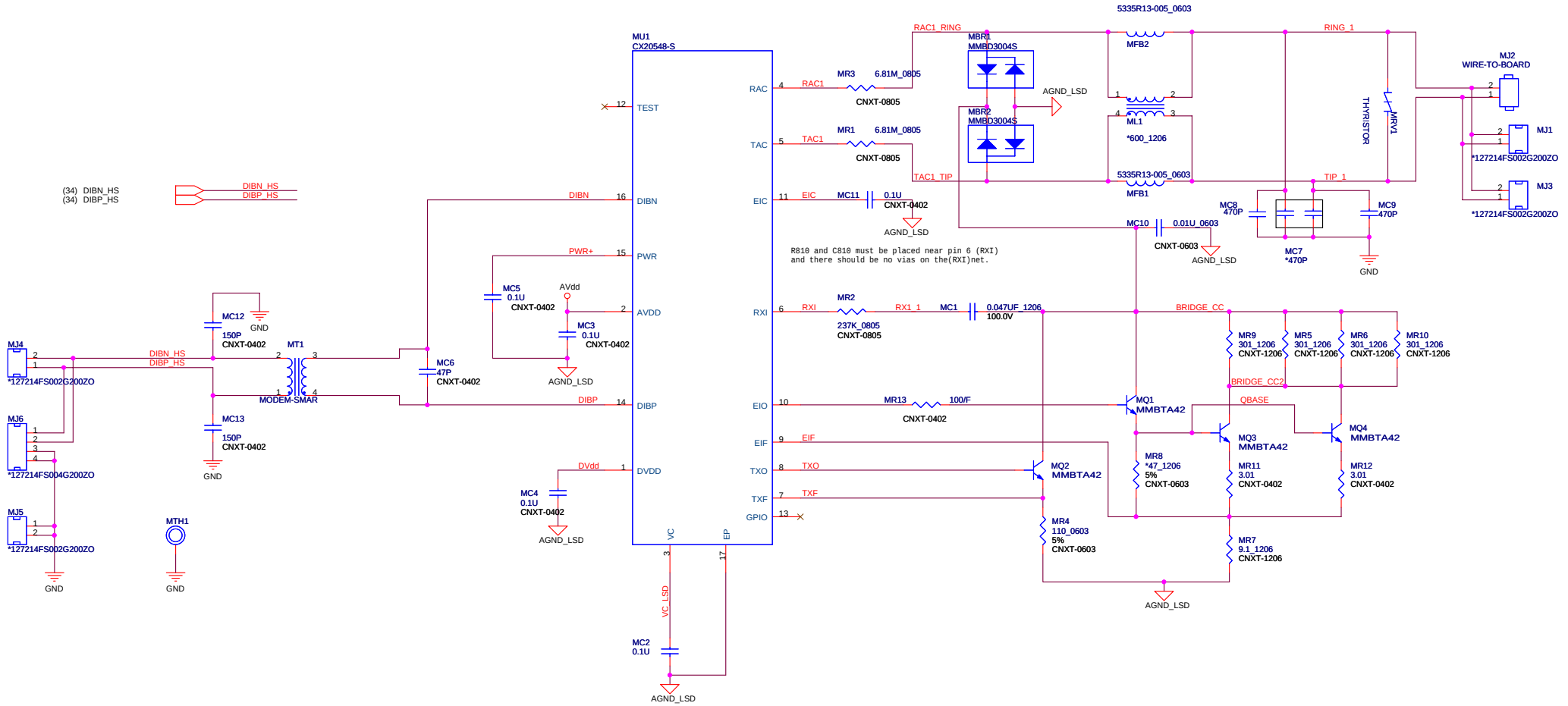
Date: Friday, March 23, 2007 Sheet 35 of 46

Mixer & 1nd order low pass filter(338HZ)

2nd order low pass filter(338HZ)



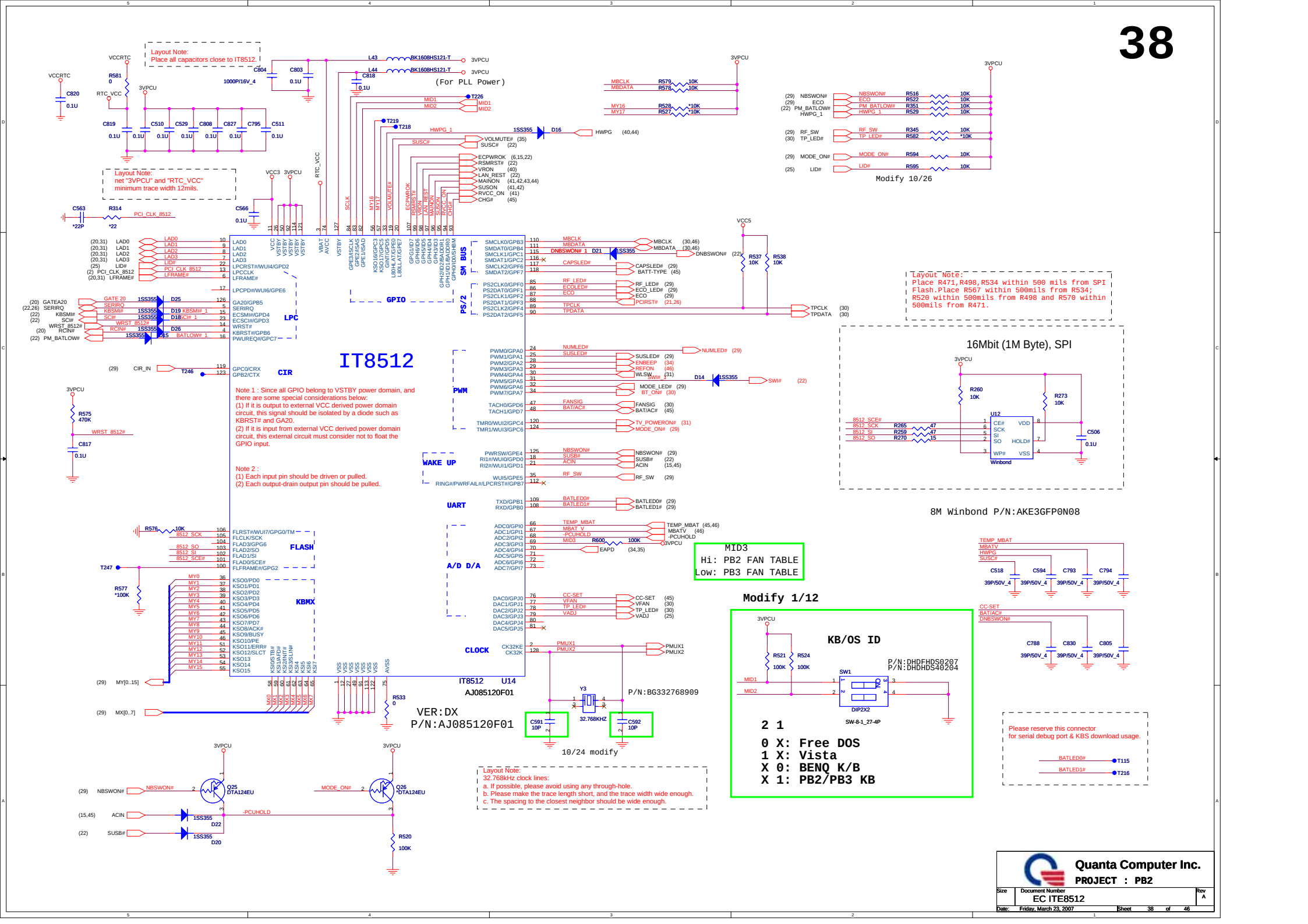
Quanta Computer Inc.		
PROJECT : PB2		
Size	Document Number: AUDIO	Rev: A
Date: Friday, March 23, 2007	Sheet 36 of 46	



Quanta Computer Inc.

PROJECT : PB2

Size	Document Number	Rev
	MOM	A
Date: Friday, March 23, 2007	Sheet 37 of 46	


IT8512
Layout Note:
Place all capacitors close to IT8512.
(For PLL Power)
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
Modify 10/26
Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534;
R520 within 500mils from R498 and R570 within 500mils from R471.
16Mbit (1M Byte), SPI
8M Winbond P/N:AKE3GFP0N08
MID3
Hi: PB2 FAN TABLE
Low: PB3 FAN TABLE
Modify 1/12
KB/OS ID
P/N:DHDFHDS0207
P/N:DHDHDS40204
2 1
0 X: Free DOS
1 X: Vista
X 0: BENQ K/B
X 1: PB2/PB3 KB
Please reserve this connector for serial debug port & KBS download usage.
Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.
VER:DX
P/N:AJ085120F01
P/N:BG332768909
10/24 modify
Quanta Computer Inc.
PROJECT : PB2
EC ITE8512
Friday, March 23, 2007
Sheet 38 of 46

CPU

H13 H19 H20

h-c276d197p2

h-c276d197p2 h-c276d197p2

H3 H2 H14

h-c315d118p2 h-c315d118p2 h-c315d118p2

H11 H6

h-c315d118p2 h-c315d118p2

h-tc276be276x276d118p2

h-tc276be276x276d118p2 h-tc276be276x276d118p2

H16 H9 H8

H15 H18 H27 H28 H22

h-c315d118p2 h-c315d118p2 h-c315d118p2 h-c315d118p2 h-c315d118p2

H25 H26 H29 H1 H23 H12

h-c315d118p2 h-c315d118p2 h-c315d118p2 h-c118d118n h-c118d118n h-c315d118p2

PCI_E

H4 H5 H24 H21

h-c236d150p2 h-c236d150p2 h-c236d150p2 h-c236d150p2

FAN

H7 H10

h-tc276be276x276d118p2 h-c236d150p2

For EMI

VCC5 VCC5 VCC5 VCC5

C5 0.1U C616 0.1U C622 0.1U C621 0.1U

VCC1.8 VCC1.8 VCC1.8 VCC1.8

VIN VIN VIN VCC5

C443 C586 C789 C309 0.1U

VCC5 VCC5 RVCC3 RVCC3

0.1U/25V/X7R/0603 0.1U/25V/X7R/0603 0.1U/25V/X7R/0603

PAD2 PAD15 PAD6 PAD14 PAD12 PAD1 PAD5 PAD8 PAD11 PAD3 PAD16

*EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91

PAD4 PAD7 PAD13 PAD9 PAD17 PAD18 PAD19 PAD20 PAD21 PAD22 PAD23 PAD24

*EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91 *EMIPAD142X91

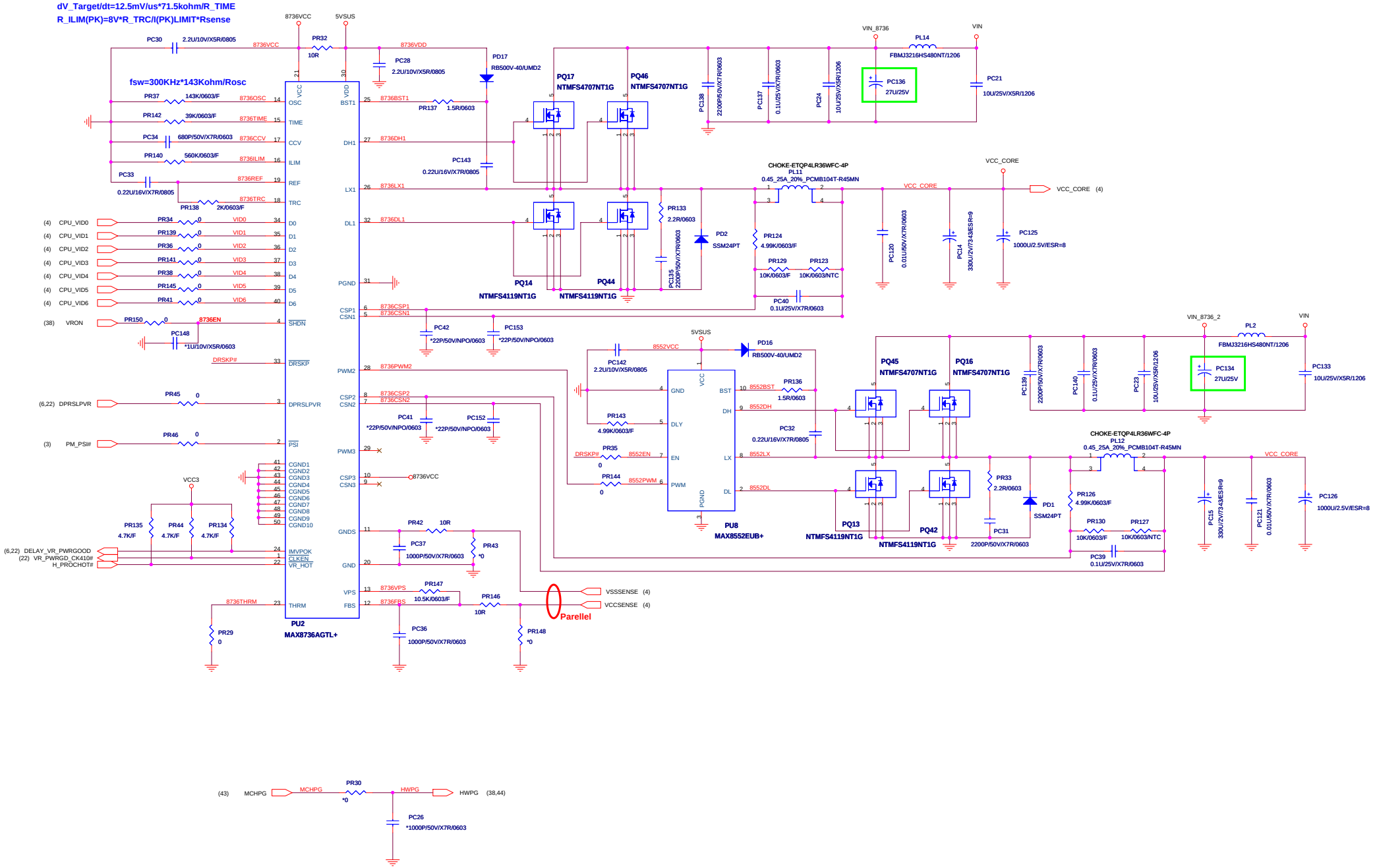
Quanta Computer Inc.

PROJECT : PB2

Size	Document Number	Rev
	EMI/SCREW	A

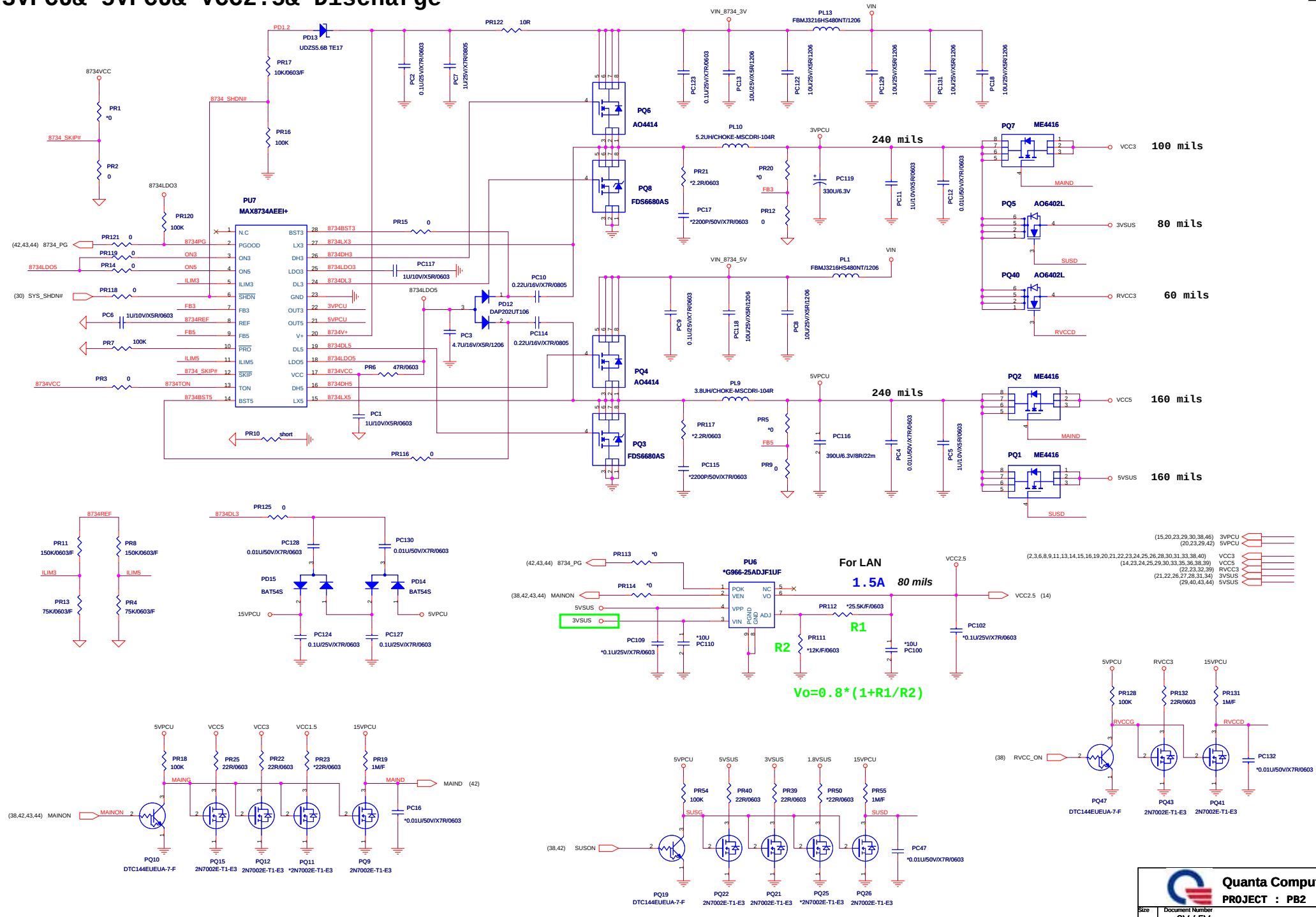
Date: Friday, March 23, 2007 Sheet 39 of 46

CPU CORE

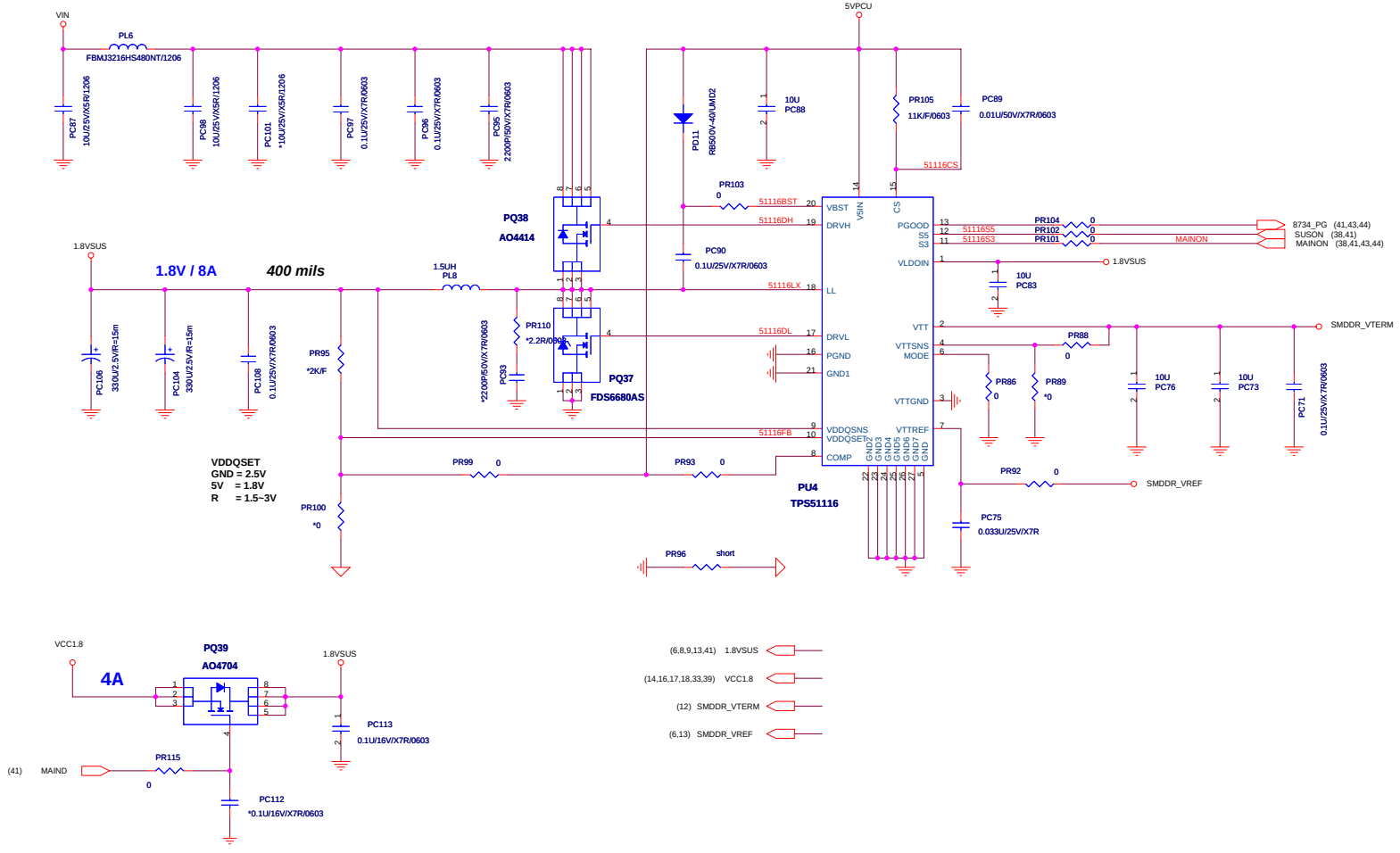


Quanta Computer Inc.			
PROJECT : PB2			
Size	Document Number		Rev
	CPU CORE		A
Date: Friday, March 23, 2007		Sheet 40 of 46	

3VPCU& 5VPCU& VCC2.5& Discharge

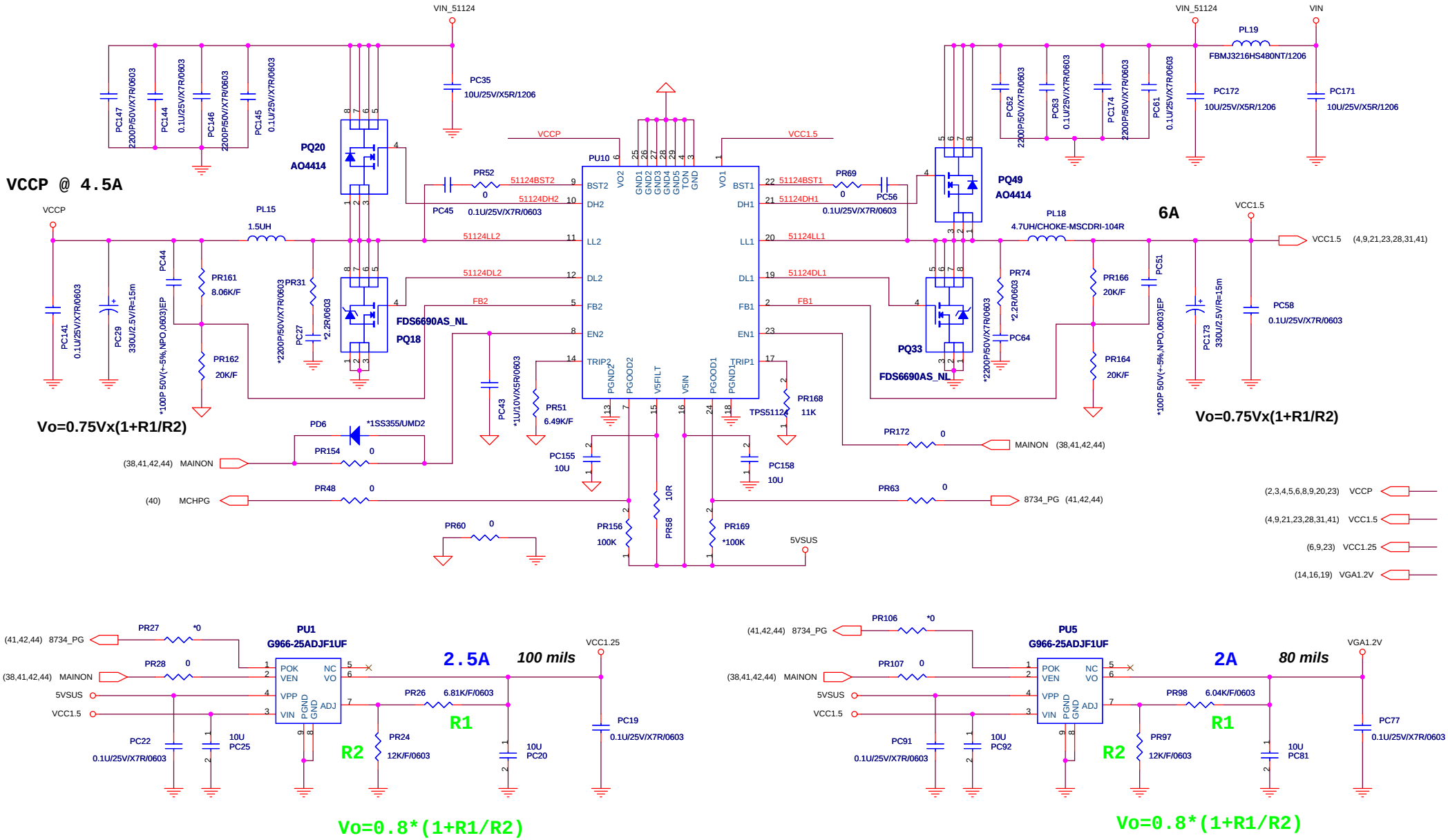


1.8VSUS & VCC1.8 & SMDDR_VTERM



Quanta Computer Inc.			
PROJECT : PB2			
Size	Document Number		Rev
	1.8VSUS /SMDDR_VTERM		A
Date: Friday, March 23, 2007		Sheet 42 of 46	

VCCP&VCC1.5V&VCC1.25&VGA1.2



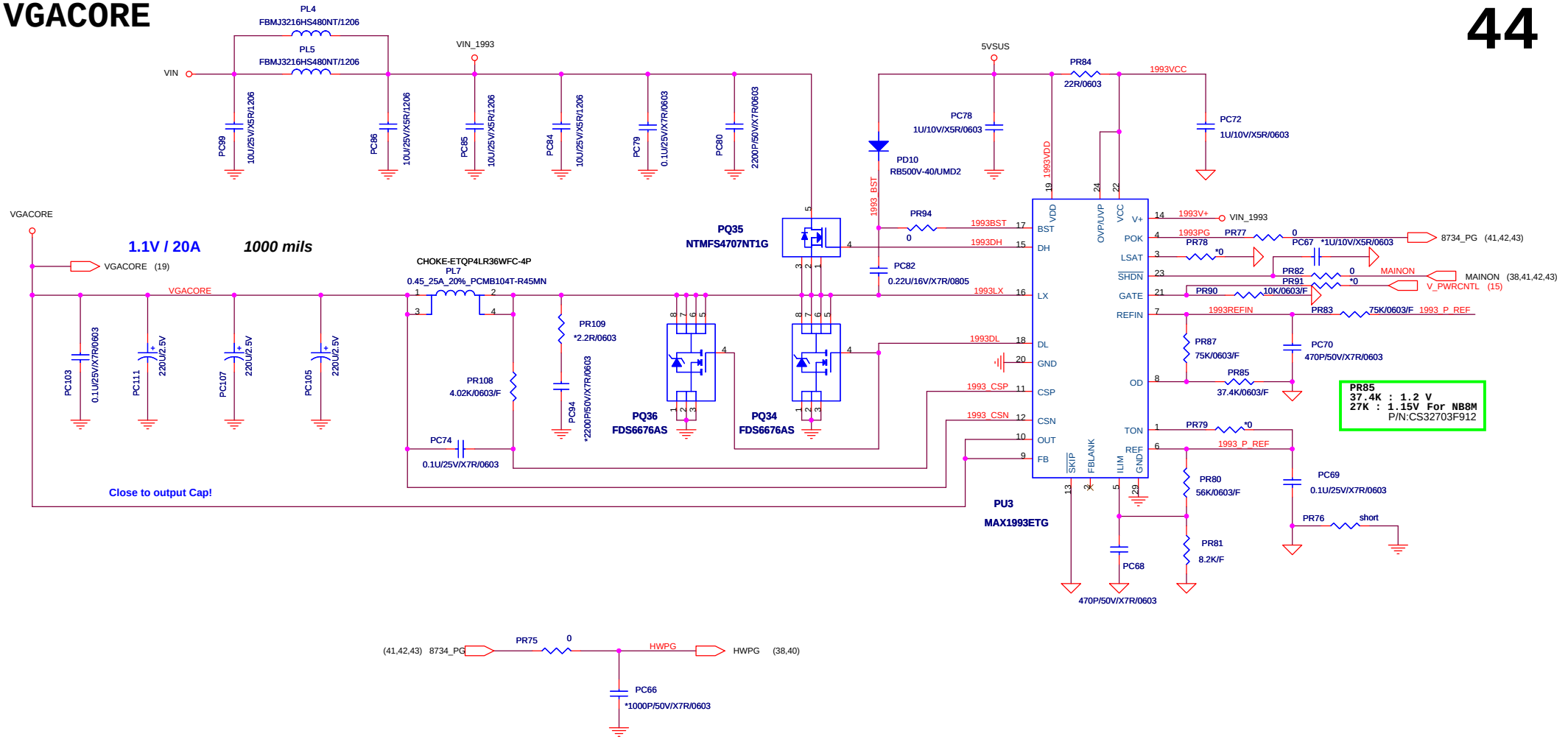
Quanta Computer Inc.

PROJECT : PB2

Size	Document Number	Rev
	VCCP(1.05V)/VCC1.5	A

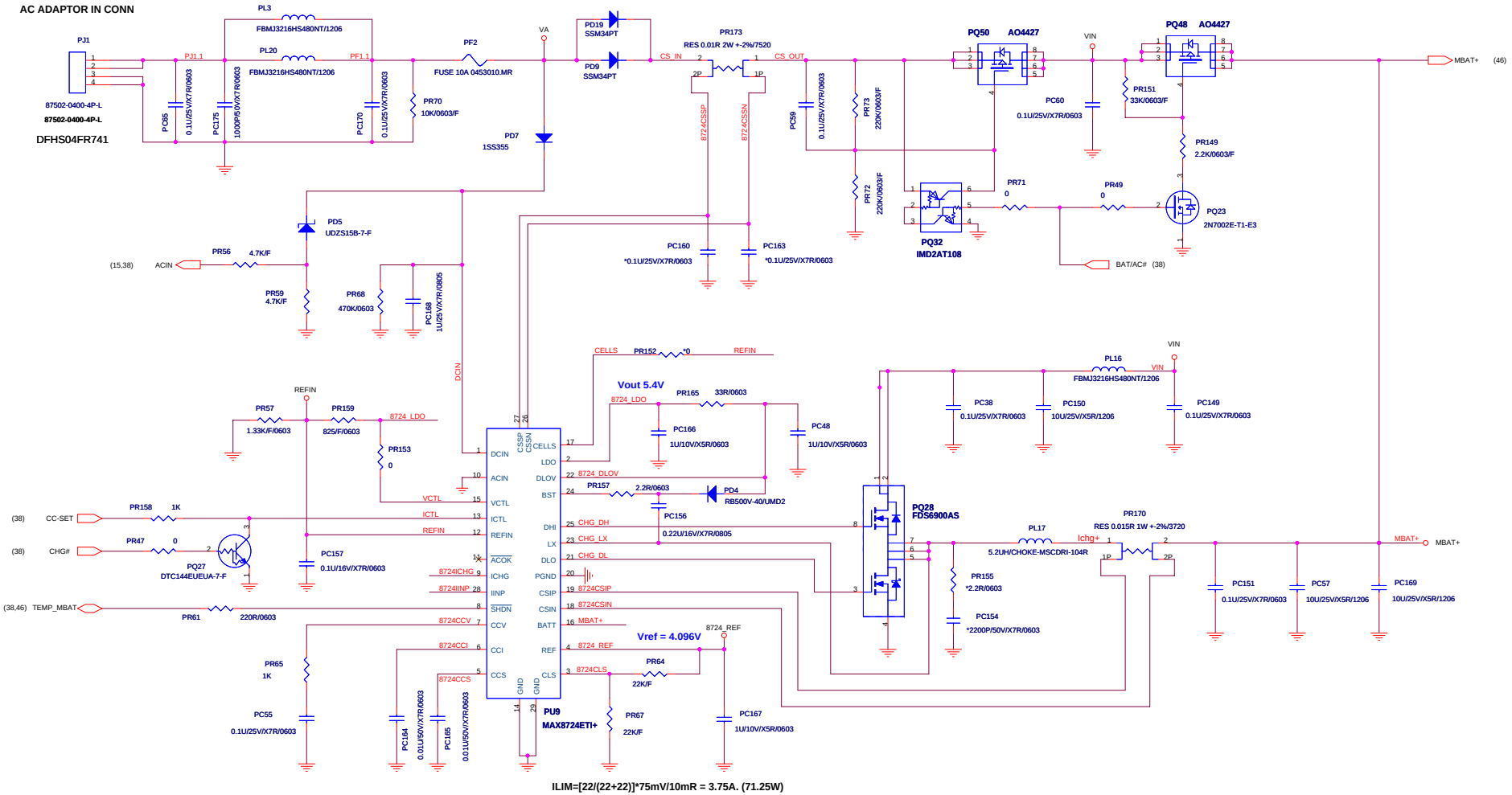
Date: Friday, March 23, 2007 Sheet 43 of 46

VGACORE



Quanta Computer Inc.		
PROJECT : PB2		
Size	Document Number: VGA_CORE	Rev: A
Date: Friday, March 23, 2007	Sheet 44 of 46	

Battery Charger



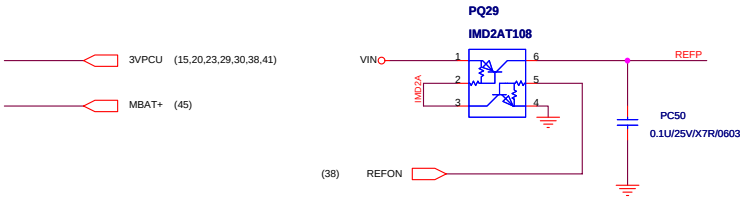
BATT-TYPE	
High	Low
Li-ion 4S2P Li-ion 4S1P Ni-MH 8S1P	Li-ion 3S2P

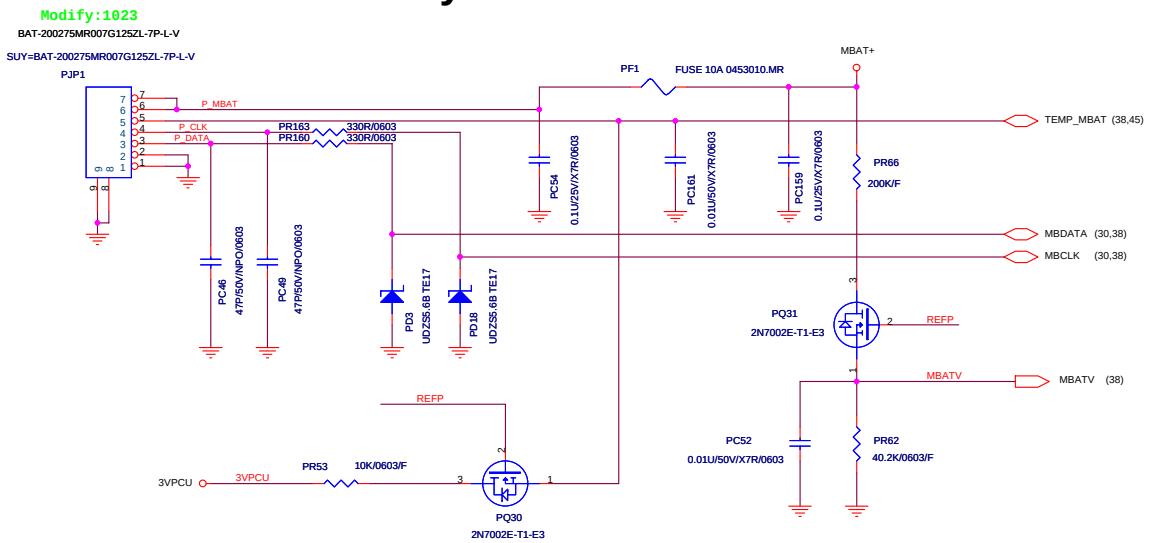
Quanta Computer Inc.
PROJECT : PB2

Size	Document Number	Rev
	BATTERY CHARGER	A

Date: Friday, March 23, 2007 Sheet 45 of 46

Battery Connector

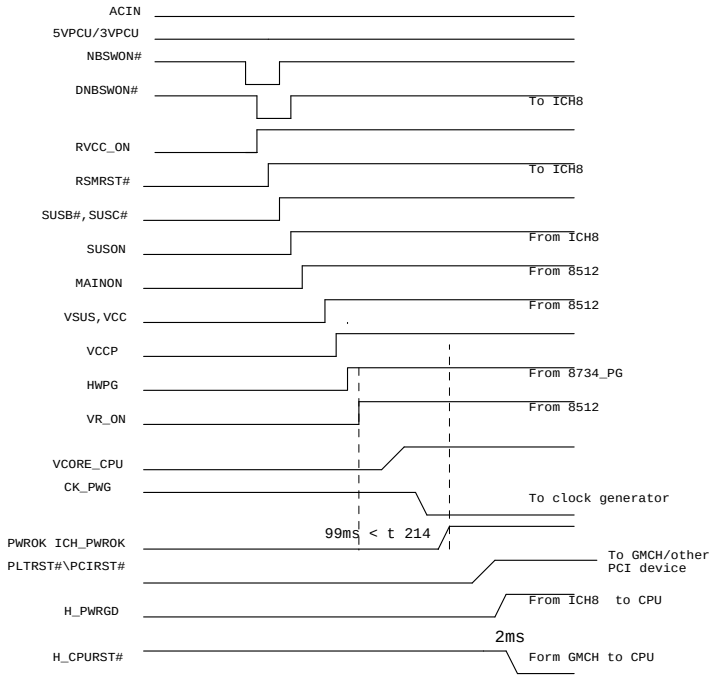




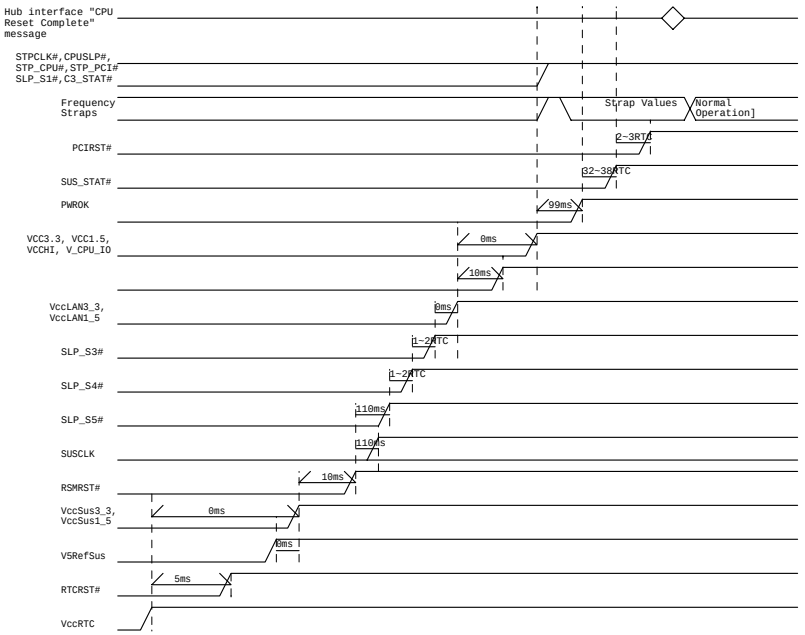
MBATV voltage :	
Li-ion 4S*P	16.8V*40.2/(200+40.2)= 2.812V 12.0V*40.2/(200+40.2)= 2.008V
Ni-MH 8S1P	8.0V*40.2/(200+40.2)= 1.34V

TEMP_MBAT voltage :		
	System Off	System On
Battery	0V	1.6V
Adapter	3.3V	3.3V
Battery+Adapter	1.6V	1.6V

ACIN POWER ON TIMING



Power Sequencing and Reset Signal Timings



Quanta Computer Inc.

PROJECT : PB2

Size	Document Number	Rev
	BATTERY CNN	A

Date: Friday, March 23, 2007 Sheet 46 of 46