R13J INTEL UMA/DISCRETE SYSTEM DIAGRAM

01

+3V/+5V S5 PG.30

+1.05V_VTT PG.31

CPU Core PG.32~33

DDR3 PG.34

VCCSA PG.35

Charge PG.36

Dis-Charge PG.37

+VGACORE PG.38

SODIMM1 Max. 4GB PG.12 — DDR3 Channel A

SODIMM2 Max. 4GB PG.13 — DDR3 Channel B

INTEL Sandy
37.5mm X 37.5mm
989pin PGA
TDP 35W
PG.2~5

PCI-E x8

Nvidia N12P-GV
23mm X 23mm
TDP 15W
PG.14~17

DDR3 800MHz

VRAM 64Mx16x4,64bit PG.18

HDMI PG.20

CRT PG.21

LVDS PG.19

FDI — DMI

HDD PG.22 — SATA0

ODD PG.22 — SATA1

INTEL PCH COUGAR POINT
PG.6~11

DP Port B

CRT

LVDS

PCI-E x 1 — LANE1 / LANE0

LAN RTL8165EH 10/100 PG.26

WLAN BT COMBO PG.29 — USB 2.0 PORT10

PCI-E x 1 — LANE2

Card Reader RTS5219 PG.23

KBC EnE KB3930QF A1 PG.28 — LPC

KB | TP | ROM | FAN

USB2.0 Ports X3 PG.25 — PORT0,1,8

Webcam PG.19 — PORT4

USB 2.0 — PORT13

BT Softbreeze PG.25

AUDIO CODEC IDT 92HD80Bx PG.24

Speaker PG.24

HP/MIC PG.25

Analog MIC PG.24

Stackup
TOP
GND
IN1
IN2
VCC
BOT

NB5

PROJECT : R13J
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Wednesday, September 28, 2011 Sheet 1 of 38

Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

02

U15A

DMI_TXN0 6 → B27 DMI_RX#[0]
DMI_TXN1 6 → B25 DMI_RX#[1]
DMI_TXN2 6 → A25 DMI_RX#[2]
DMI_TXN3 6 → B24 DMI_RX#[3]

DMI_TXP0 6 → B28 DMI_RX[0]
DMI_TXP1 6 → B26 DMI_RX[1]
DMI_TXP2 6 → A24 DMI_RX[2]
DMI_TXP3 6 → B23 DMI_RX[3]

DMI_RXN0 6 → G21 DMI_TX#[0]
DMI_RXN1 6 → E22 DMI_TX#[1]
DMI_RXN2 6 → F21 DMI_TX#[2]
DMI_RXN3 6 → D21 DMI_TX#[3]

DMI_RXP0 6 → G22 DMI_TX[0]
DMI_RXP1 6 → D22 DMI_TX[1]
DMI_RXP2 6 → F20 DMI_TX[2]
DMI_RXP3 6 → C21 DMI_TX[3]

DMI

FDI_TXN0 6 → A21 FDI0_TX#[0]
FDI_TXN1 6 → H19 FDI0_TX#[1]
FDI_TXN2 6 → E19 FDI0_TX#[2]
FDI_TXN3 6 → F18 FDI0_TX#[3]
FDI_TXN4 6 → B21 FDI1_TX#[0]
FDI_TXN5 6 → C20 FDI1_TX#[1]
FDI_TXN6 6 → D18 FDI1_TX#[2]
FDI_TXN7 6 → E17 FDI1_TX#[3]

FDI_TXP0 6 → A22 FDI0_TX[0]
FDI_TXP1 6 → G19 FDI0_TX[1]
FDI_TXP2 6 → E20 FDI0_TX[2]
FDI_TXP3 6 → G18 FDI0_TX[3]
FDI_TXP4 6 → B20 FDI1_TX[0]
FDI_TXP5 6 → C19 FDI1_TX[1]
FDI_TXP6 6 → D19 FDI1_TX[2]
FDI_TXP7 6 → F17 FDI1_TX[3]

FDI_FSYNC0 6 → J18 FDI0_FSYNC
FDI_FSYNC1 6 → J17 FDI1_FSYNC

FDI_INT 6 → H20 FDI_INT

FDI_LSYNC0 6 → J19 FDI0_LSYNC
FDI_LSYNC1 6 → H17 FDI1_LSYNC

Intel(R) FDI

eDP_COMP → A18 eDP_COMPIO
INT_eDP_HPD_Q → A17 eDP_ICOMPO
B16 eDP_HPD

C15 eDP_AUX
D15 eDP_AUX#

C17 eDP_TX[0]
F16 eDP_TX[1]
C16 eDP_TX[2]
G15 eDP_TX[3]

C18 eDP_TX#[0]
E16 eDP_TX#[1]
D16 eDP_TX#[2]
F15 eDP_TX#[3]

eDP

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

PCI EXPRESS* - GRAPHICS

PEG_ICOMPI J22 → PEG_COMP
PEG_ICOMPO J21
PEG_RCOMPO H22

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

PEG_RX#[0..7] 14 → K33 PEG_RX#0, M35 PEG_RX#1, L34 PEG_RX#2, J35 PEG_RX#3, J32 PEG_RX#4, H34 PEG_RX#5, H31 PEG_RX#6, G33 PEG_RX#7

PEG_RX#[0] J33 PEG_RX0
PEG_RX#[1] L35 PEG_RX1
PEG_RX#[2] K34 PEG_RX2
PEG_RX#[3] H35 PEG_RX3
PEG_RX#[4] H32 PEG_RX4
PEG_RX#[5] G34 PEG_RX5
PEG_RX#[6] G31 PEG_RX6
PEG_RX#[7] F33 PEG_RX7
PEG_RX#[8] E35
PEG_RX#[9] E33
PEG_RX#[10] F32
PEG_RX#[11] D34
PEG_RX#[12] E31
PEG_RX#[13] C33
PEG_RX#[14] B32
PEG_RX#[15]

PEG_RX[0..7] 14 → J33 PEG_RX0, L35 PEG_RX1, K34 PEG_RX2, H35 PEG_RX3, H32 PEG_RX4, G34 PEG_RX5, G31 PEG_RX6, F33 PEG_RX7

PEG_TX#[0] M29 C_PEG_TX#0
PEG_TX#[1] M32 C_PEG_TX#1
PEG_TX#[2] M31 C_PEG_TX#2
PEG_TX#[3] L32 C_PEG_TX#3
PEG_TX#[4] L29 C_PEG_TX#4
PEG_TX#[5] K31 C_PEG_TX#5
PEG_TX#[6] K28 C_PEG_TX#6
PEG_TX#[7] J30 C_PEG_TX#7
PEG_TX#[8] J28
PEG_TX#[9] H29
PEG_TX#[10] G27
PEG_TX#[11] E29
PEG_TX#[12] F27
PEG_TX#[13] D28
PEG_TX#[14] F26
PEG_TX#[15] E25

PEG_TX[0] M28 C_PEG_TX0
PEG_TX[1] M33 C_PEG_TX1
PEG_TX[2] M30 C_PEG_TX2
PEG_TX[3] L31 C_PEG_TX3
PEG_TX[4] L28 C_PEG_TX4
PEG_TX[5] K30 C_PEG_TX5
PEG_TX[6] K27 C_PEG_TX6
PEG_TX[7] J29 C_PEG_TX7
PEG_TX[8] J27
PEG_TX[9] H28
PEG_TX[10] G28
PEG_TX[11] E28
PEG_TX[12] F28
PEG_TX[13] D27
PEG_TX[14] E26
PEG_TX[15] D25

U15B

H_SNB_IVB# 7 → C26 SNB_IVB#
SNB_IVB# N.A at SNB EDS #27637 0.7v1
TP4 SKTOCC# → AN34 SKTOCC#

MISC

TP2 TP_CATERR# → AL33 CATERR#

Placement close to EC.

EC_PECI 28 → R386 43_4 H_PECI → AN33 PECI
C5164 47P/50V_4
H_PROCHOT#_R R146 56.2/F_4 H_PROCHOT# 28,32 → AL32 PROCHOT#
PM_THRMTRIP#_R R148 *0_4/S 9,28 → AN32 THERMTRIP#

THERMAL

PM_SYNC 6 → R377 *0_4/S PM_SYNC_R → AM34 PM_SYNC
H_PWRGOOD 9 → R378 *0_4/S H_PWRGOOD_R → AP33 UNCOREPWRGOOD
R384 10K_4
PM_DRAM_PWRGD_R V8 → SM_DRAMPWROK
CPU_PLTRST#_R → AR33 RESET#

PWR MANAGEMENT

CPU RESET#

U18 *74LVC1G07GW
+1.05V_VTT R404 *75/F_4
CPU_PLTRST# R400 *43_4
8,14,23,26,28,29 PLTRST#
+3VS5 C560 0.1U/10V_4
R401 750/F_4
R402 1.5K/F_4

SM_DRAMPWROK Processor Input.

+3VS5 R49 10K_4 → PM_DRAM_PWRGD_PU
U2 *74LVC1G07GW
C27 0.1U/10V_4
+1.5V_CPU
R40 200/F_4
PM_DRAM_PWRGD_C R42 130/F_4 PM_DRAM_PWRGD_R
R37 *39_4
R48 *0_4
PM_DRAM_PWRGD 6
R47 *0_4/S
R43 *3K/F_4
Q3 *2N7002
MAIN_ONG 4,37

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)

CLOCKS

BCLK A28 → CLK_CPU_BCLKP 8
BCLK# A27 → CLK_CPU_BCLKN 8
DPLL_REF_SSCLK A16 → CLK_DPLL_SSCLKP R5105 1K/F_4
DPLL_REF_SSCLK# A15 → CLK_DPLL_SSCLKN R5106 1K/F_4 +1.05V_VTT
for no support eDP , can disable it.

DDR3 MISC

SM_DRAMRST# → R8 CPU_DRAMRST#
SM_RCOMP[0] AK1 → SM_RCOMP_0 R143 140/F_4
SM_RCOMP[1] A5 → SM_RCOMP_1 R318 26.1/F_4
SM_RCOMP[2] A4 → SM_RCOMP_2 R316 200/F_4
SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

JTAG & BPM

PRDY# AP29 → XDP_PRDY#
PREQ# AP27 → XDP_PREQ#
TP12
TP11
CPU XDP
TCK AR26 → XDP_TCLK
TMS AR27 → XDP_TMS
TRST# AP30 → XDP_TRST#
TP8
TP10
TP13
TDI AR28 → XDP_TDI_R
TDO AP26 → XDP_TDO
TP39
TP7
R375 *1K_4 +3V
DBR# AL35 → XDP_DBRST#
XDP_DBRST# 6
BPM#[0] AT28 → XDP_BPM0 TP40
BPM#[1] AR29 → XDP_BPM1 TP41
BPM#[2] AR30 → XDP_BPM2 TP43
BPM#[3] AT30 → XDP_BPM3 TP42
BPM#[4] AP32 → XDP_BPM4 TP5
BPM#[5] AR31 → XDP_BPM5 TP45
BPM#[6] AT31 → XDP_BPM6 TP44
BPM#[7] AR32 → XDP_BPM7 TP46

DDR3 DRAM RESET

+1.5VSUS R311 1K_4
12,13 DDR3_DRAMRST# R312 1K_4
CPU_DRAMRST#_R
8 DRAMRST_CNTRL_PCH R315 *0_4/S
Q24 2N7002
C442 0.047U/10V_4
R314 4.99K/F_4
CPU_DRAMRST#

+1.05V_VTT 4,6,7,8,10,28,31,32,38
+1.5V_CPU 4
+3VS5 6,7,8,9,10,14,21,25,30,31,37,38
+3V 6,7,8,9,10,12,13,14,16,19,20,21,22,23,24,26,27,28,29,32,37,38

FDI disable (DIS only stuff)

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)

14 PEG_TX[0..7]

C_PEG_TX0	C483	0.1U/10V_4	PEG_TX0
C_PEG_TX1	C489	0.1U/10V_4	PEG_TX1
C_PEG_TX2	C492	0.1U/10V_4	PEG_TX2
C_PEG_TX3	C498	0.1U/10V_4	PEG_TX3
C_PEG_TX4	C501	0.1U/10V_4	PEG_TX4
C_PEG_TX5	C504	0.1U/10V_4	PEG_TX5
C_PEG_TX6	C508	0.1U/10V_4	PEG_TX6
C_PEG_TX7	C512	0.1U/10V_4	PEG_TX7

0.22uF AC coupling Caps for PCIE GEN1/2/3

14 PEG_TX#[0..7]

C_PEG_TX#0	C488	0.1U/10V_4	PEG_TX#0
C_PEG_TX#1	C490	0.1U/10V_4	PEG_TX#1
C_PEG_TX#2	C496	0.1U/10V_4	PEG_TX#2
C_PEG_TX#3	C500	0.1U/10V_4	PEG_TX#3
C_PEG_TX#4	C503	0.1U/10V_4	PEG_TX#4
C_PEG_TX#5	C507	0.1U/10V_4	PEG_TX#5
C_PEG_TX#6	C511	0.1U/10V_4	PEG_TX#6
C_PEG_TX#7	C517	0.1U/10V_4	PEG_TX#7

0.22uF AC coupling Caps for PCIE GEN1/2/3

DP & PEG Compensation

+1.05V_VTT R67 10K_4 INT_eDP_HPD_Q
+1.05V_VTT R319 24.9/F_4 eDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

+1.05V_VTT R85 24.9/F_4 PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)

+1.05V_VTT

H_PROCHOT#	R145	62_4
XDP_TDO	R155	51_4
XDP_TMS	R159	51_4
XDP_TDI_R	R403	51_4
XDP_PREQ#	R158	*51_4
XDP_TCLK	R156	51_4
XDP_TRST#	R163	51_4

NB5

PROJECT : R13J
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	1A

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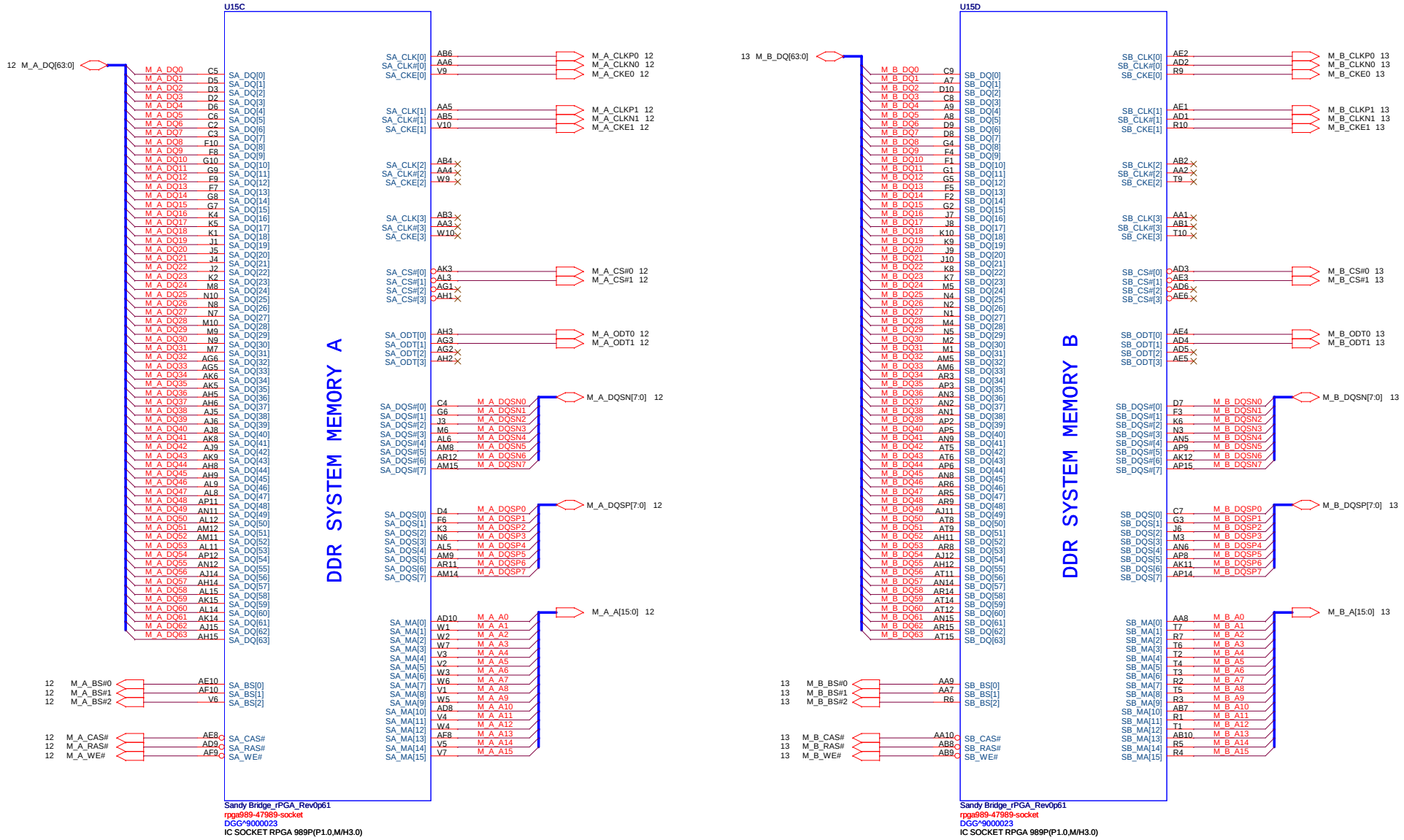
Sandy Bridge Processor (DDR3)



NB5

PROJECT : R13J

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 2/4 (DDR3 I/F)	1A

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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

04

U15F

SNB: 55A

+VCC_CORE

C493 22U/6.3VS_8 C521 10U/6.3VS_6 C516 22U/6.3VS_8
C42 22U/6.3VS_8 C36 22U/6.3VS_8 C174 22U/6.3VS_8
C509 22U/6.3VS_8 C172 22U/6.3VS_8 C263 22U/6.3VS_8
C300 22U/6.3VS_8 C39 22U/6.3VS_8 C502 22U/6.3VS_8
C177 22U/6.3VS_8 C527 *10U/6.3V_6S C33 22U/6.3VS_8
C151 22U/6.3VS_8 C286 22U/6.3VS_8 C283 22U/6.3VS_8
C237 22U/6.3VS_8 C242 22U/6.3VS_8 C163 22U/6.3VS_8
C535 *22U/6.3VS_8 C220 *22U/6.3VS_8 C447 22U/6.3VS_8
C173 22U/6.3VS_8 C515 10U/6.3VS_6 C270 22U/6.3VS_8
C450 22U/6.3VS_8 C451 22U/6.3VS_8 C542 *10U/6.3V_6S

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AE35 AE34 AE33 AE32 AE31 AE30 AE29 AE28 AE27 AE26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

SNB: 8.5A

+1.05V_VTT

AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12 E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

C145 22U/6.3VS_8 C147 22U/6.3VS_8 C482 22U/6.3VS_8
C260 22U/6.3VS_8 C180 22U/6.3VS_8 C166 22U/6.3VS_8
C146 *22U/6.3VS_8 C215 22U/6.3VS_8 C526 22U/6.3VS_8
C532 *22U/6.3VS_8 C200 *22U/6.3VS_8 C61 *22U/6.3VS_8
C491 22U/6.3VS_8 C66 *22U/6.3VS_8 C282 *22U/6.3VS_8
C167 *22U/6.3VS_8 C506 22U/6.3VS_8 C236 *22U/6.3VS_8
C513 *22U/6.3VS_8 C499 22U/6.3VS_8 C158 22U/6.3VS_8

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

+1.05V_VTT

+1.05V_VTT_40 R86 *0_4/S

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

VCC_SENSE AJ35 R136 100_4 +VCC_CORE
VSS_SENSE AJ34 VCC_SENSE 32
VSS_SENSE 32
R139 100_4

VCCIO_SENSE B10
VSSIO_SENSE A10 VSSP_SENSE
VCCP_SENSE 31
VSSP_SENSE 31

Trace Route to Power IC area.

+VCC_CORE 21,33
+VCC_GFX 33
+VCCSA 35
+1.05V_VTT 2,6,7,8,10,28,31,32,38
+1.5V_CPU 2
+1.5V_CPU 2
+1.5VSUS 2,10,12,13,21,34,38

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGQ^9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)

U15G

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

+VCC_GFX

SNB: 21.5A

C529 22U/6.3V_8 C264 22U/6.3V_8
C285 22U/6.3V_8 C299 22U/6.3V_8
C284 22U/6.3V_8 C530 22U/6.3V_8
C301 22U/6.3V_8 C238 22U/6.3V_8
C528 22U/6.3V_8 C239 22U/6.3V_8
C265 22U/6.3V_8 C531 22U/6.3V_8

AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

GRAPHICS

+1.8V

SNB: 1.5A

C449 10U/6.3V_8 C441 1U/6.3V_4 C443 1U/6.3V_4 + C440 *330U/2V_7343

B6 A6 A2
VCCPLL1 VCCPLL2 VCCPLL3

330uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.

1.8V RAIL

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGQ^9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)

SENSE LINES

VAXG_SENSE AK35
VSSAXG_SENSE AK34

R140 100_4 +VCC_GFX
VCC_AXG_SENSE 32
VSS_AXG_SENSE 32
R142 100_4

VREF

SM_VREF AL1

+VDDR_REF_CPU

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

R31 100K_4
Q2 2N7002
DDR_VTTREF 12,13,34
MAIND
MAIND 37

DDR3 -1.5V RAILS

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

SNB: 5A +1.5V_CPU

C297 10U/6.3V_6 C214 10U/6.3V_8 C289 10U/6.3V_6 C268 10U/6.3V_6
C190 10U/6.3V_6 C305 10U/6.3V_6 C576 *330U_2.5V_5.0x5.9_ESR10m

330uF x1, 10uF_8 x6 Socket BOT edge.

SA RAIL

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

SNB: 6A +VCCSA

C485 10U/6.3V_8 C448 10U/6.3V_8 C484 10U/6.3V_8 C445 *10U/6.3V_8

330uF x1, 10uF_8 x1 Socket BOT edge,
10uF_8 x2 Socket BOT cavity.

MISC

VCCSA_SENSE H23 VCCUSA_SENSE_R R82 *0_4/S VCCUSA_SENSE 35

FC_C22 C22 H_FC_C22 R77 10K_4
VCCSA_VID1 C24 VCCSA_SEL 35
R81 10K_4

+1.5V_CPU R310 *0_8/S +1.5V

40mile routing

Layout note: need routing together and ALERT need between CLK and DATA.

SVID CLK

Place PU resistor close to VR

R309 *54.9/F_4 +1.05V_VTT

H_CPU_SVIDCLK VR_SVID_CLK 32

SVID DATA

+1.05V_VTT +1.05V_VTT

Place PU resistor close to CPU R137 130/F_4

R308 *130/F_4 Place PU resistor close to VR

H_CPU_SVIDDAT VR_SVID_DATA 32

Place PU resistor close to CPU

SVID ALERT

C713 0.1U/10V_4

+1.05V_VTT R26 75/F_4

H_CPU_SVIDALRT# R25 43_4 VR_SVID_ALERT# 32

+1.5VSUS +1.5V_CPU +1.5VSUS

CPU VDDQ

Q36 AON7410

R185 220_8

C455 0.1U/10V_4
C452 0.1U/10V_4
C554 0.1U/10V_4
C558 0.1U/10V_4

Placement close to CPU.

MAIND

C438 *470P/50V_4

Q16 2N7002

MAIN_ONG 2,37

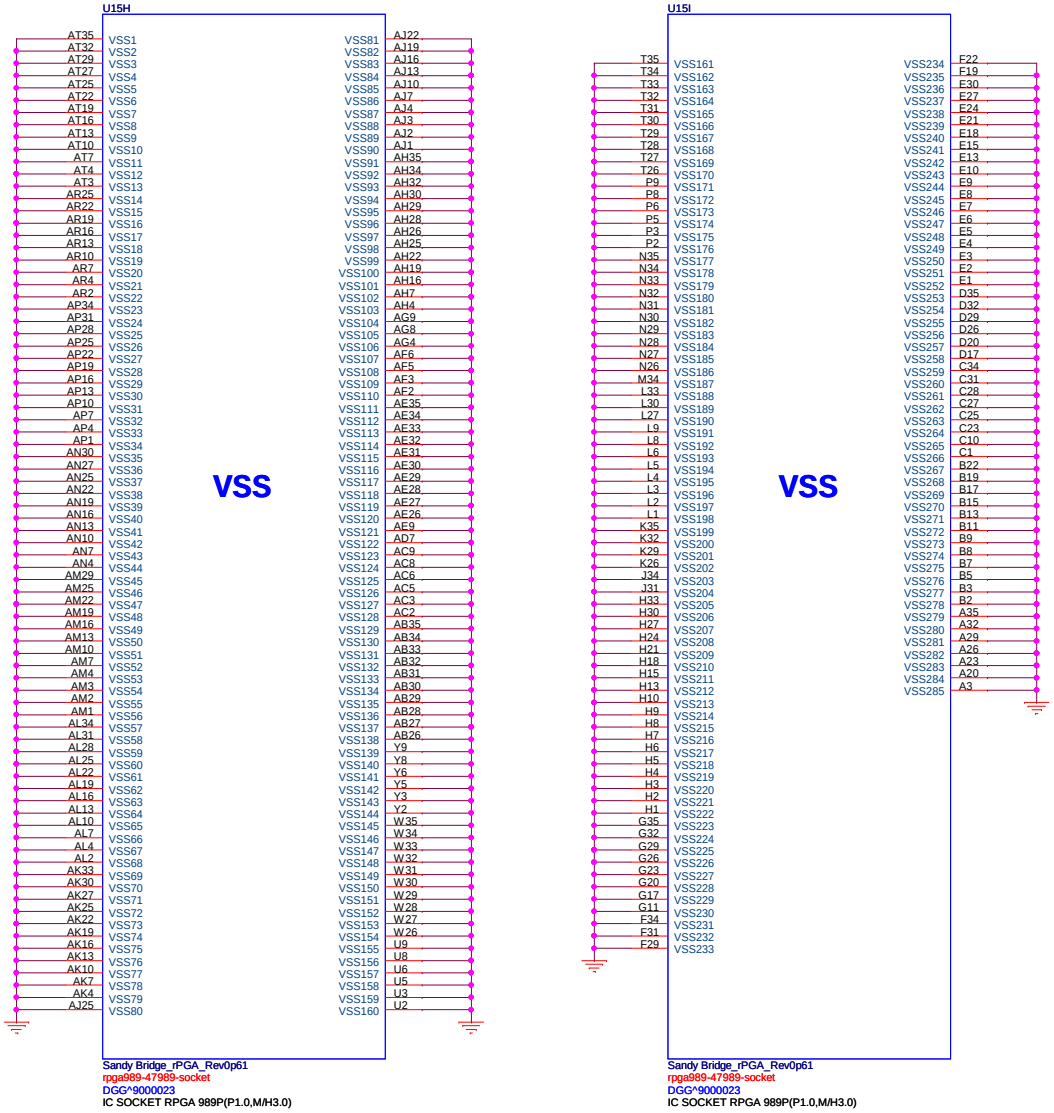
NB5

PROJECT : R13J
Quanta Computer Inc.

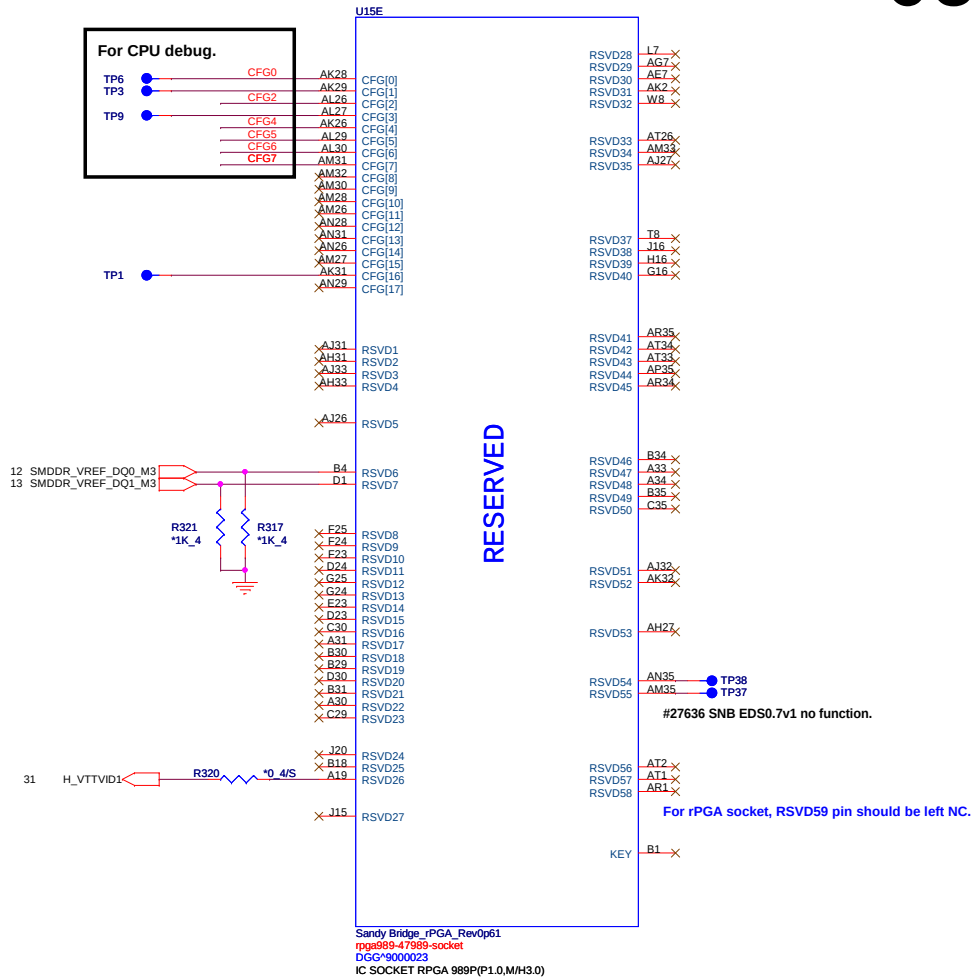
Size	Document Number	Rev
Custom	SNB 3/4 (POWER)	1A

Date: Wednesday, September 28, 2011 Sheet 4 of 38

Sandy Bridge Processor (GND)



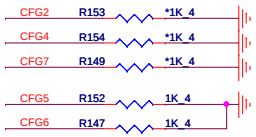
Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT : R13J
Quanta Computer Inc.

NB5

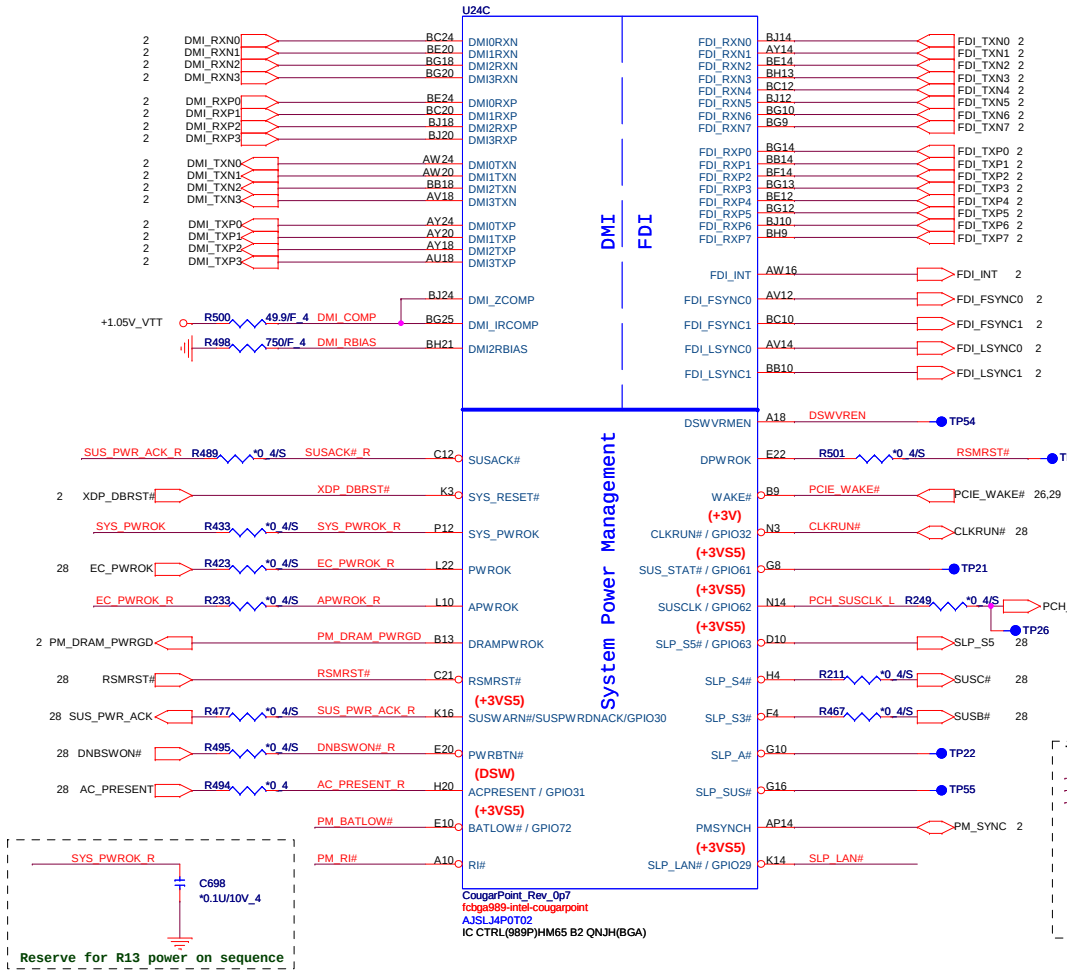
Size	Document Number	Rev
Custom	SNB 4/4 (GND)	1A

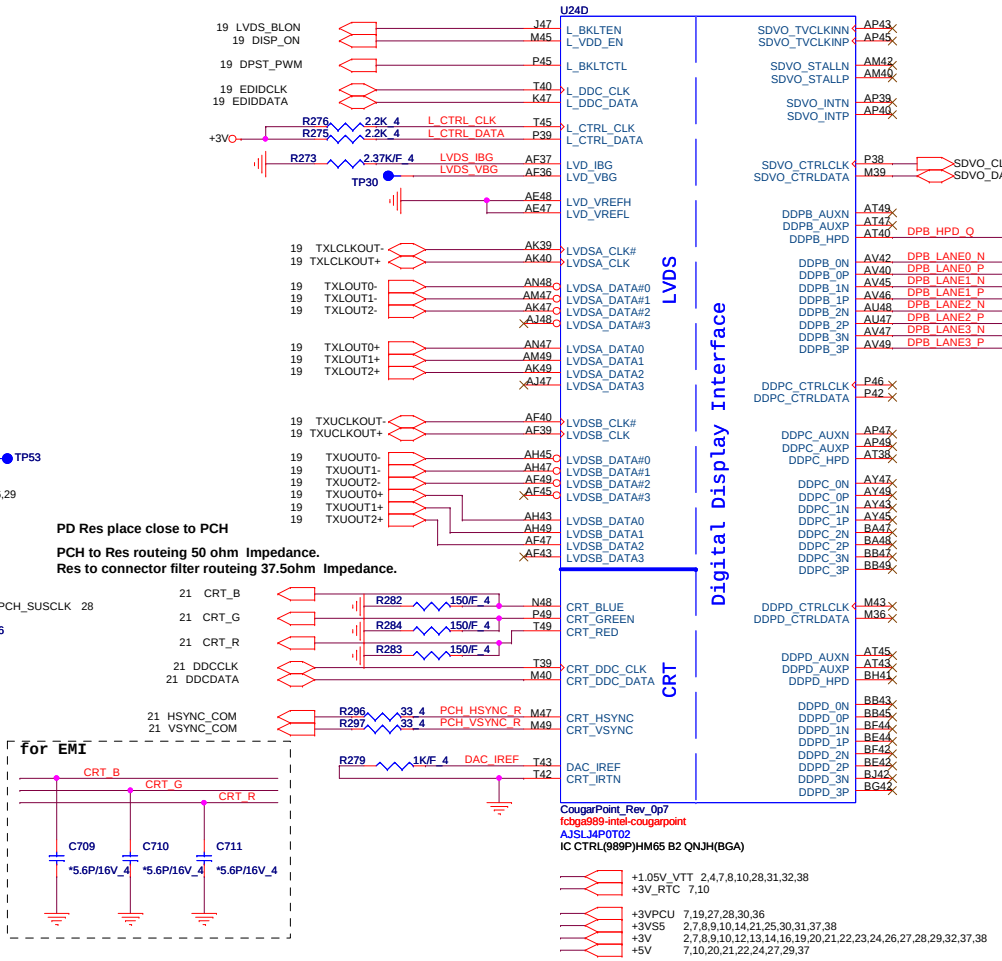
Date: Wednesday, September 28, 2011 | Sheet 5 of 38

Cougar Point (DMI,FDI,PM)

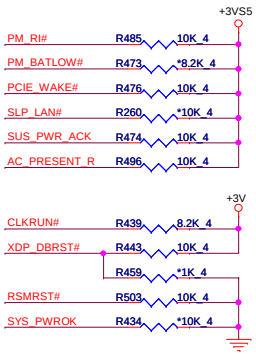
Cougar Point (LVDS,DDI)

06





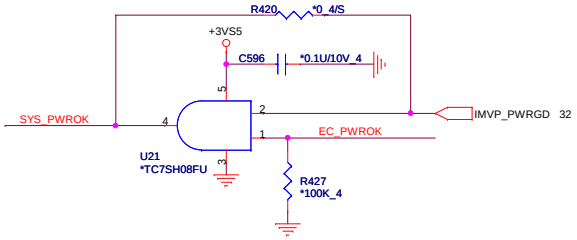
PCH Pull-high/low(CLG)

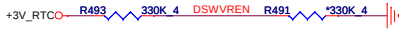


INT HDMI disable (DIS only remove)

INT HDMI Detect Function

System PWR_OK(CLG)





On Die DSW VR Enable
High = Enable (Default) Low = Disable

PROJECT : R13J

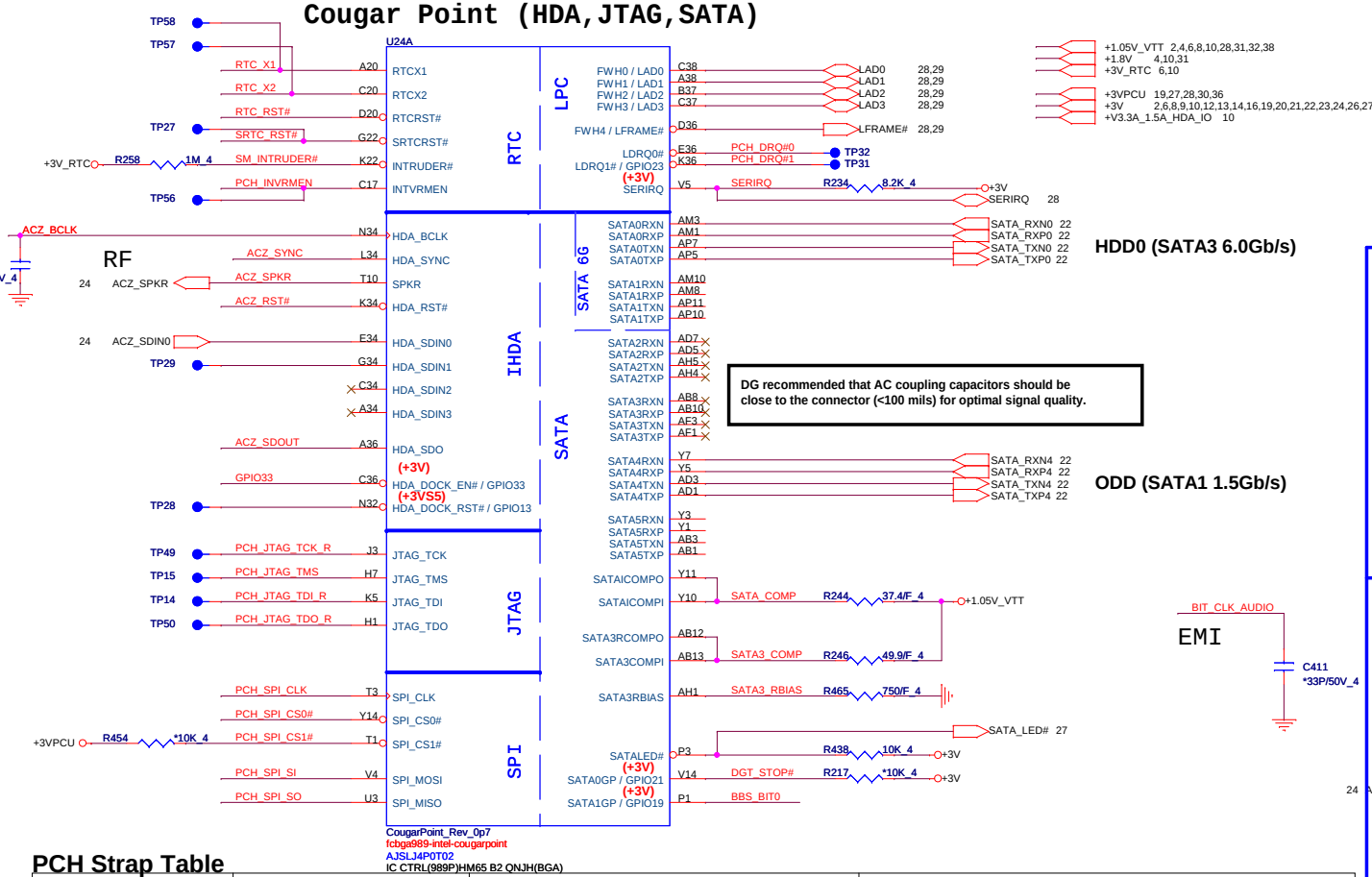
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A

Date: Wednesday, September 28, 2011 | Sheet 6 of 38

Cougar Point (HDA,JTAG,SATA)



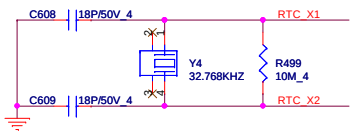
HDD0 (SATA3 6.0Gb/s)

ODD (SATA1 1.5Gb/s)

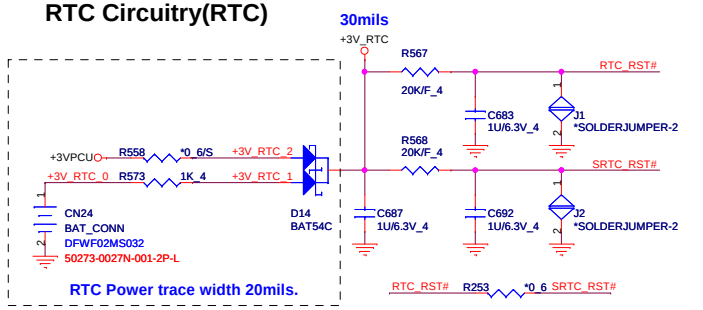
DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

EMI

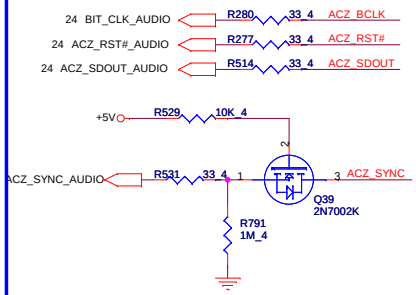
RTC Clock 32.768KHz



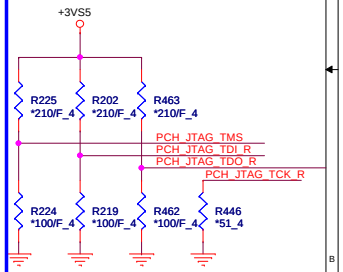
RTC Circuitry(RTC)



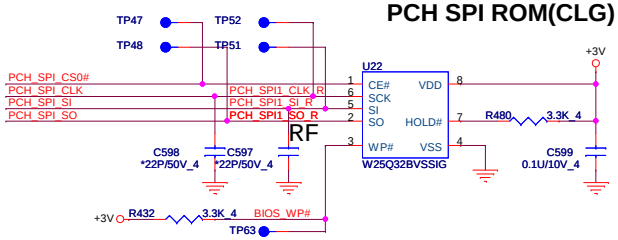
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR (Different from Calpella)	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R435 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V R522 *1K_4 R521 10K_4 PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R497 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R509 0_4 BIOS_WP#
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# GNT0# Boot Location: 1 1 SPI; 0 0 LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 (Different from Calpella)	Boot BIOS Selection 0 [bit-0]	PWROK		R455 *1K_4 BBS_BIT0 R523 *1K_4 BBS_BIT1 8
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R468 *1K_4 NV_ALE 8
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R470 2.2K_4 R469 4.7K_4 NV_CLE 8 H_SNB_IVB# 2 N.A at CPT EDS 0.7
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R278 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	28 GPIO33_E ACZ_SDOUT R510 *1K_4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R483 *1K_4 ICC_EN# 9
GPIO28 (Different from Calpella)	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R447 *1K_4 PLL_ODVR_EN 9
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R198 1K_4 +3V

PROJECT : R13J
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A

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07

Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)

PLTRST#(CLG)

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

SMBus/Pull-up(CLG)

MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

WLAN

LAN

Cardreader

Left_USB

Left_USB 2

Webcam

Right_USB

WLAN

Blue tooth

EMI

PCIE Clock

WLAN

LAN

GPU

Remove for UMA only.

UMA : Ra
S.G : Will control by NVIDIA GPIO

CLOCK TERMINATION for FCIM

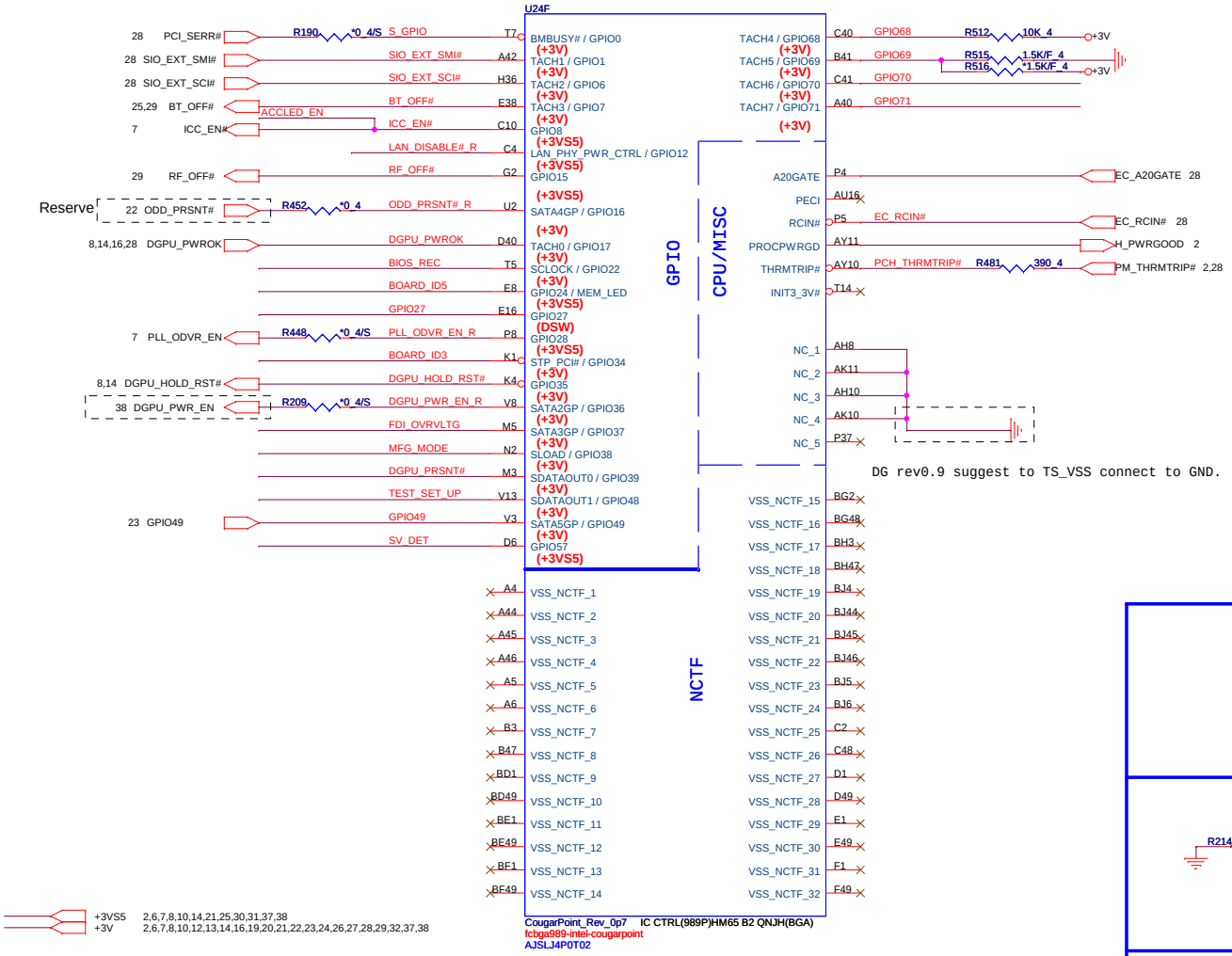
PROJECT : R13J
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 3/6 (PCIE/USB/CLK)	1A

Date: Wednesday, September 28, 2011 Sheet 8 of 38

Cougar Point (GPIO,VSS_NCTF,RSVD)

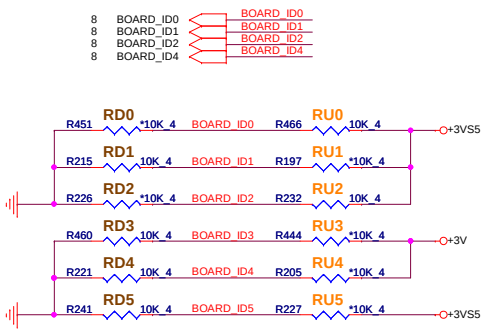


DG rev0.9 suggest to TS_VSS connect to GND.

+3VS5 2,6,7,8,10,14,21,25,30,31,37,38
+3V 2,6,7,8,10,12,13,14,16,19,20,21,22,23,24,26,27,28,29,32,37,38

BOARD ID SETTING

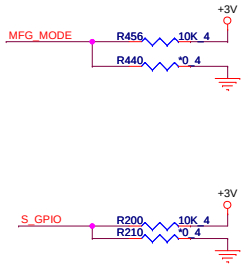
Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
R13 UMA	0	0	0	0	0	0
R13 DIS	0	0	0	0	0	1
R13 (1.1) DIS (AMD)	0	0	0	0	1	1
R13J (1.3) DIS (NVIDIA)	0	0	0	1	0	1
	0	0	0	0	0	0



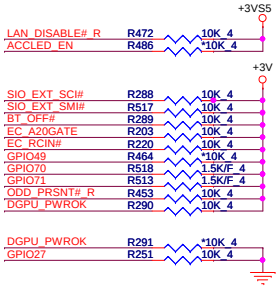
Clock Gen Power OK (CLG)

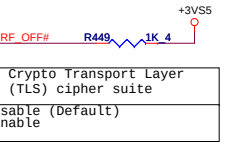
09

MFG-TEST

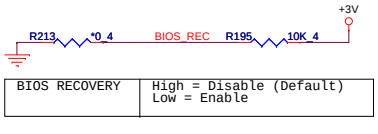


GPIO Pull-up/Pull-down(CLG)

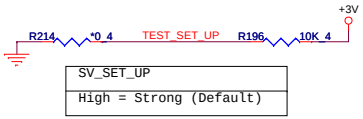




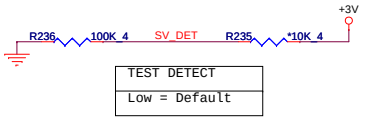
Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default) High = Enable



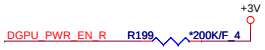
BIOS RECOVERY	High = Disable (Default) Low = Enable



SV_SET_UP
High = Strong (Default)



TEST DETECT
Low = Default



DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

GFX Present

	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

PROJECT : R13J
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A

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Cougar Point-M (POWER)

COUGAR POINT (POWER)

10

U24J

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | MISC | CPU | RTC | HDA

U24G

VCC CORE | CRT | LVDS | HVCMOS | DMI | VCCIO | FDI | NAND / SPI

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJSLJ4P0T02
IC CTRL(989P)HM65 B2 QNJH(BGA)

UMA Only, If have power noise issue then stuff it.

+1.05V_VTT 2,4,6,7,8,28,31,32,38
+1.5VSUS 2,4,12,13,21,34,38
+1.8V 4,7,31

+3V_RTC 6,7
+3VS5 2,6,7,8,9,14,21,25,30,31,37,38
+3V 2,6,7,8,9,12,13,14,16,19,20,21,22,23,24,26,27,28,29,32,37,38
+5VS5 19,25,30,31,32,33,34,35,37,38
+5V 6,7,20,21,22,24,27,29,37

PROJECT : R13J
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	1A

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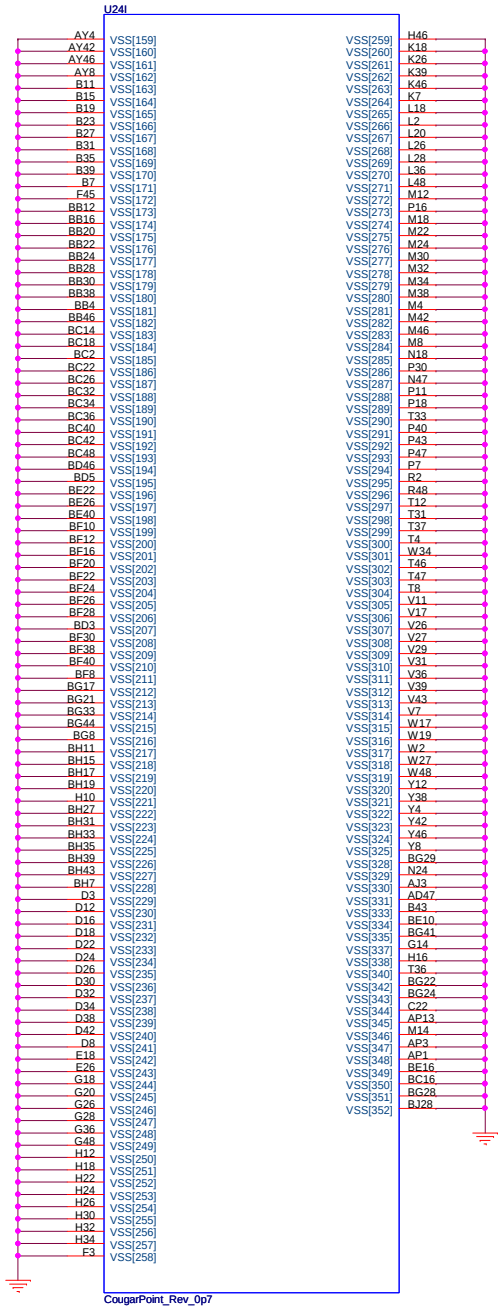
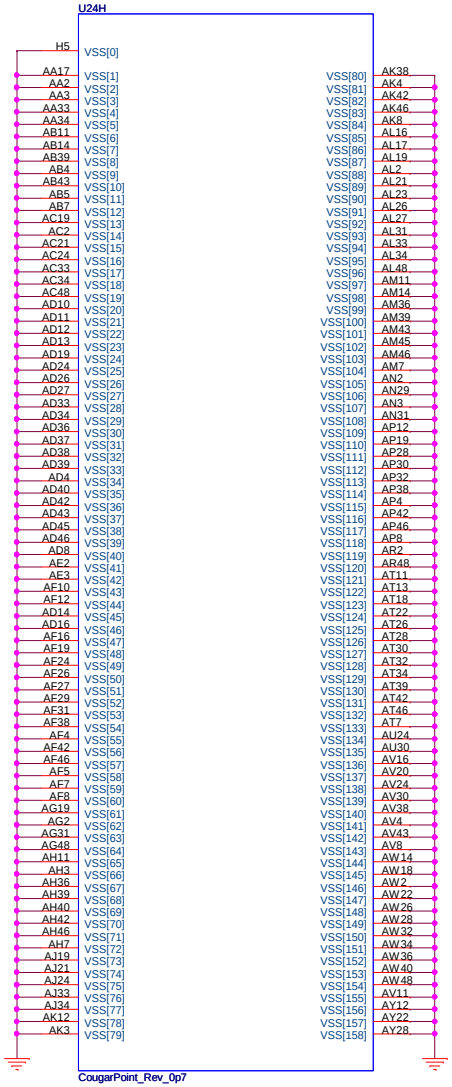
IBEX PEAK-M (GND)



IBEX PEAK-M (GND)



PROJECT : R13J

Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A

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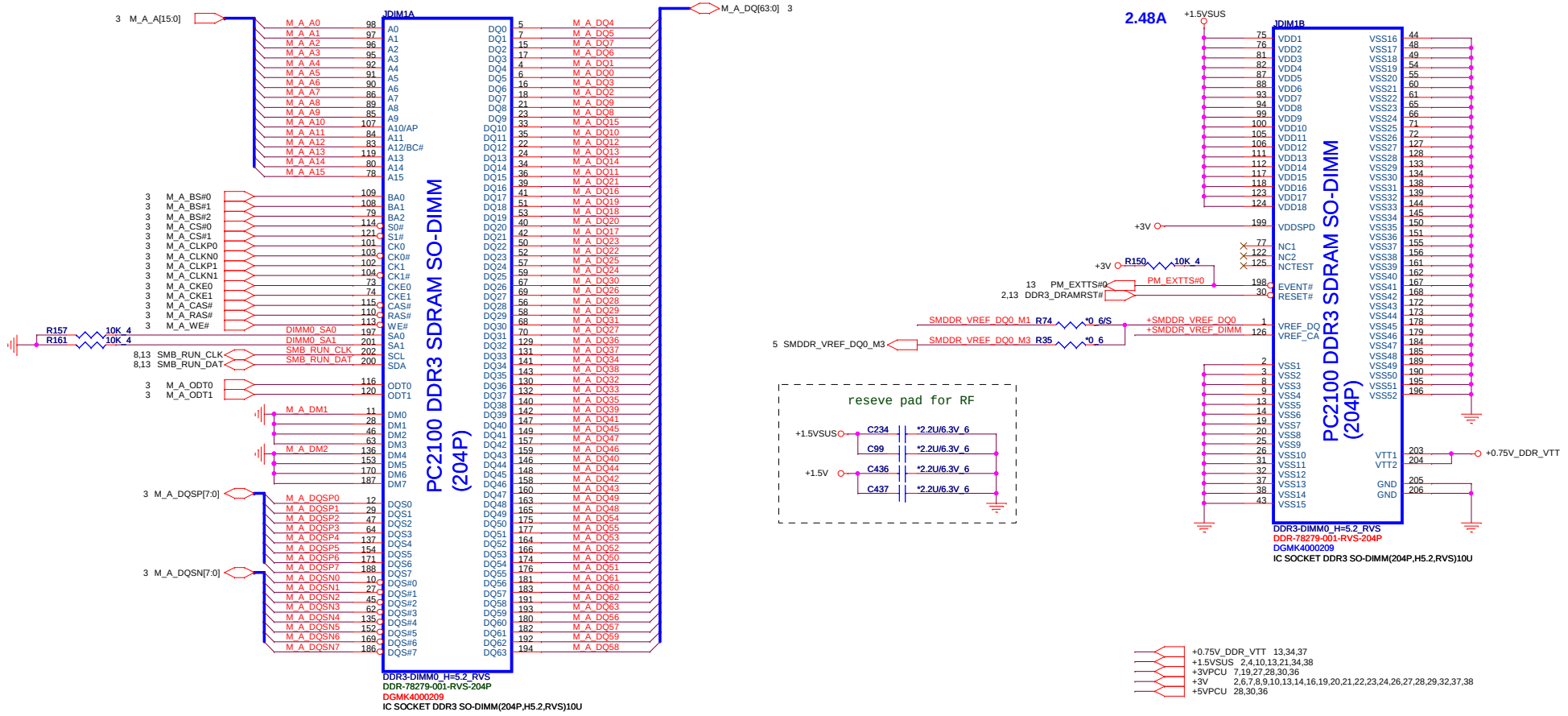
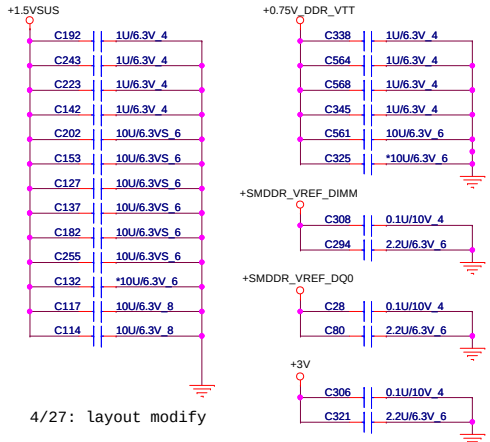


VREF DQ0 M2 Solution

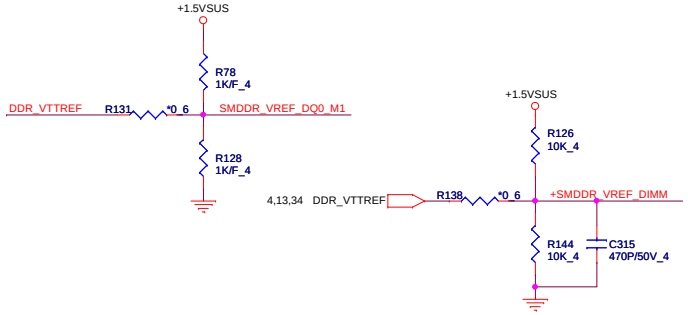
del M2 solution

Place these Caps near So-Dimm0.



4/27: layout modify

VREF DQ0 M1 Solution



NB5

PROJECT : R13J

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	1A

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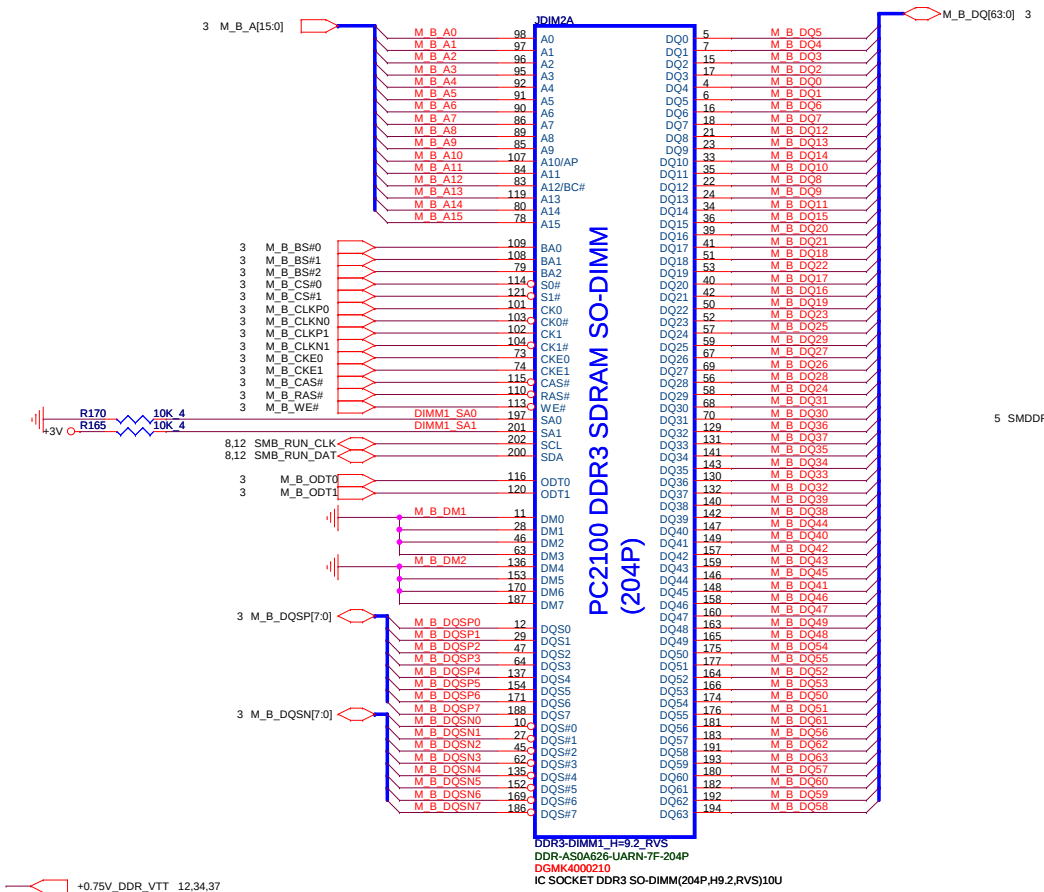
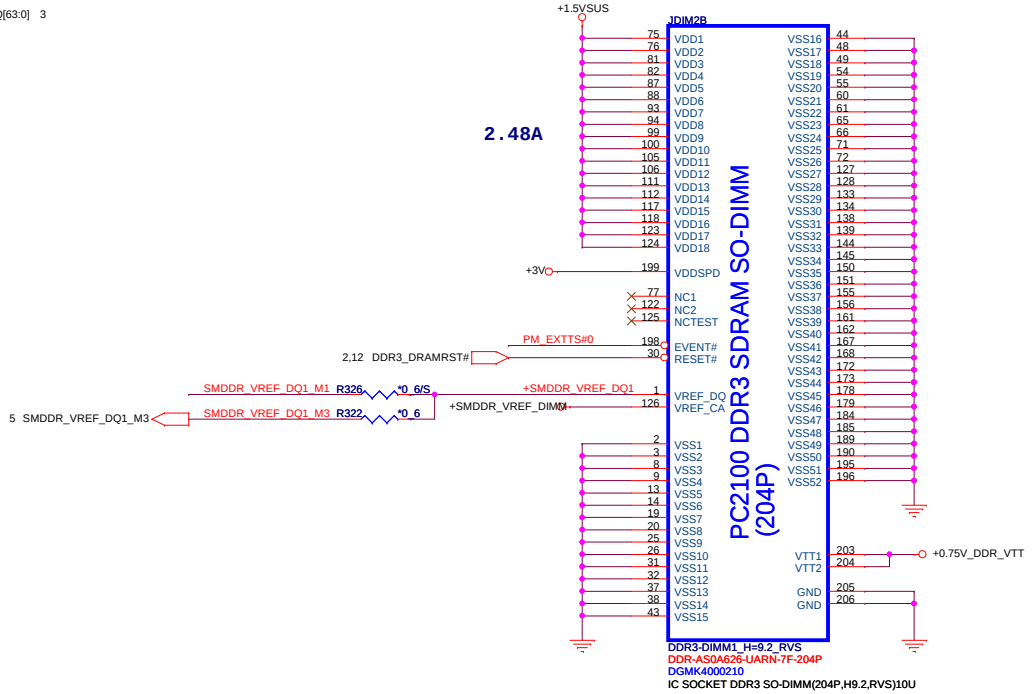
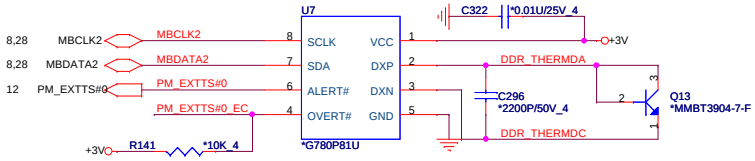
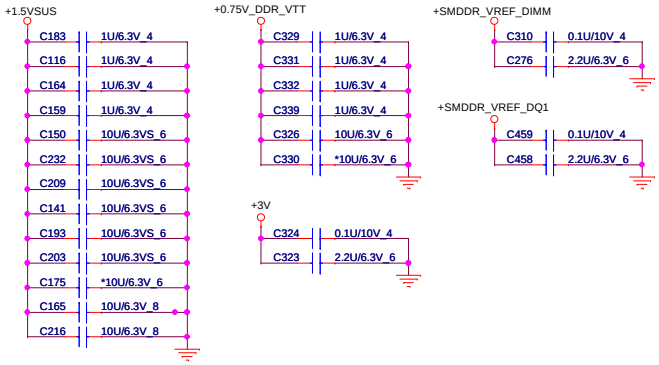




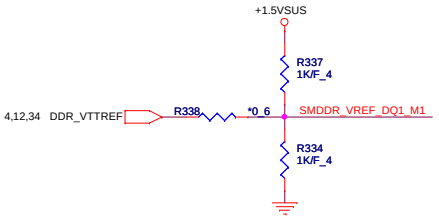
DDR3 Thermal Sensor



Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



del M2 solution

PROJECT : R13J

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	1A

NB5

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U5001A

PBGA533-NVIDIA-GEFORCE6250
N10M

1/13 PCI_EXPRESS

~ 500mA

1600mA

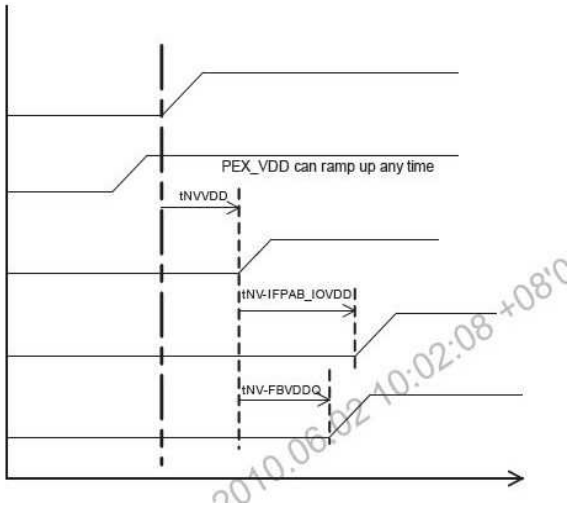
18.19A

120mA

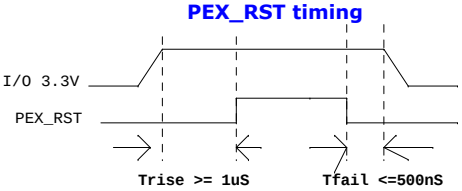
120mA

12~16 mils

power up sequence



PEX_RST timing



For DIS

For DIS

12/28 Nvidia to suggest R5009 not stuff and R5008 and Q5002 stuff.

PROJECT :	R13J
Quanta Computer Inc.	
Size: Custom	Document Number: N11M-GE2(PCIEI/F)
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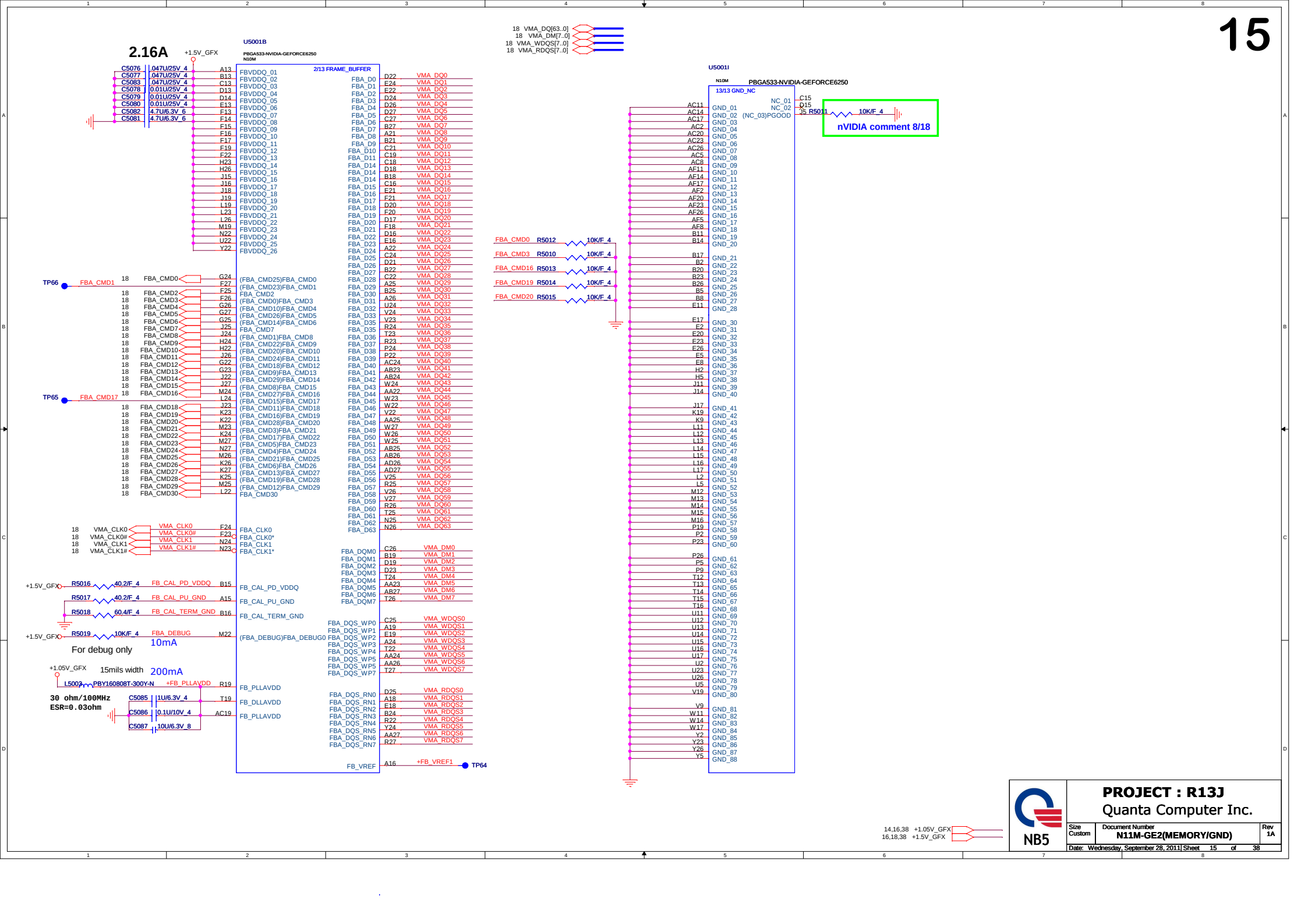
NB5


2.16A
+1.5V_GFX
U5001B
PBGA533-NVIDIA-GEFORCE6250
N10M
2/13 FRAME_BUFFER
C5076 .047U/25V_4
C5077 .047U/25V_4
C5083 .047U/25V_4
C5078 0.01U/25V_4
C5079 0.01U/25V_4
C5080 0.01U/25V_4
C5082 4.7U/6.3V_6
C5081 4.7U/6.3V_6
FBVDDQ_01 FBVDDQ_02 FBVDDQ_03 FBVDDQ_04 FBVDDQ_05 FBVDDQ_06 FBVDDQ_07 FBVDDQ_08 FBVDDQ_09 FBVDDQ_10 FBVDDQ_11 FBVDDQ_12 FBVDDQ_13 FBVDDQ_14 FBVDDQ_15 FBVDDQ_16 FBVDDQ_17 FBVDDQ_18 FBVDDQ_19 FBVDDQ_20 FBVDDQ_21 FBVDDQ_22 FBVDDQ_23 FBVDDQ_24 FBVDDQ_25 FBVDDQ_26
TP66 FBA_CMD1
TP65 FBA_CMD17
FBA_CMD0 FBA_CMD2 FBA_CMD3 FBA_CMD4 FBA_CMD5 FBA_CMD6 FBA_CMD7 FBA_CMD8 FBA_CMD9 FBA_CMD10 FBA_CMD11 FBA_CMD12 FBA_CMD13 FBA_CMD14 FBA_CMD15 FBA_CMD16 FBA_CMD18 FBA_CMD19 FBA_CMD20 FBA_CMD21 FBA_CMD22 FBA_CMD23 FBA_CMD24 FBA_CMD25 FBA_CMD26 FBA_CMD27 FBA_CMD28 FBA_CMD29 FBA_CMD30
VMA_CLK0 VMA_CLK0# VMA_CLK1 VMA_CLK1#
FBA_CLK0 FBA_CLK0* FBA_CLK1 FBA_CLK1*
R5016 40.2/F_4 FB_CAL_PD_VDDQ
R5017 40.2/F_4 FB_CAL_PU_GND
R5018 60.4/F_4 FB_CAL_TERM_GND
R5019 10K/F_4 FBA_DEBUG
For debug only
10mA
+1.05V_GFX 15mils width 200mA
L5002 PBY160808T-300Y-N +FB_PLLAVDD
30 ohm/100MHz
ESR=0.03ohm
C5085 1U/6.3V_4
C5086 0.1U/10V_4
C5087 10U/6.3V_8
FB_PLLAVDD FB_DLLAVDD FB_PLLAVDD
FBA_D0 FBA_D1 FBA_D2 FBA_D3 FBA_D4 FBA_D5 FBA_D6 FBA_D7 FBA_D8 FBA_D9 FBA_D10 FBA_D11 FBA_D12 FBA_D13 FBA_D14 FBA_D15 FBA_D16 FBA_D17 FBA_D18 FBA_D19 FBA_D20 FBA_D21 FBA_D22 FBA_D23 FBA_D24 FBA_D25 FBA_D26 FBA_D27 FBA_D28 FBA_D29 FBA_D30 FBA_D31 FBA_D32 FBA_D33 FBA_D34 FBA_D35 FBA_D36 FBA_D37 FBA_D38 FBA_D39 FBA_D40 FBA_D41 FBA_D42 FBA_D43 FBA_D44 FBA_D45 FBA_D46 FBA_D47 FBA_D48 FBA_D49 FBA_D50 FBA_D51 FBA_D52 FBA_D53 FBA_D54 FBA_D55 FBA_D56 FBA_D57 FBA_D58 FBA_D59 FBA_D60 FBA_D61 FBA_D62 FBA_D63
VMA_DQ0 VMA_DQ1 VMA_DQ2 VMA_DQ3 VMA_DQ4 VMA_DQ5 VMA_DQ6 VMA_DQ7 VMA_DQ8 VMA_DQ9 VMA_DQ10 VMA_DQ11 VMA_DQ12 VMA_DQ13 VMA_DQ14 VMA_DQ15 VMA_DQ16 VMA_DQ17 VMA_DQ18 VMA_DQ19 VMA_DQ20 VMA_DQ21 VMA_DQ22 VMA_DQ23 VMA_DQ24 VMA_DQ25 VMA_DQ26 VMA_DQ27 VMA_DQ28 VMA_DQ29 VMA_DQ30 VMA_DQ31 VMA_DQ32 VMA_DQ33 VMA_DQ34 VMA_DQ35 VMA_DQ36 VMA_DQ37 VMA_DQ38 VMA_DQ39 VMA_DQ40 VMA_DQ41 VMA_DQ42 VMA_DQ43 VMA_DQ44 VMA_DQ45 VMA_DQ46 VMA_DQ47 VMA_DQ48 VMA_DQ49 VMA_DQ50 VMA_DQ51 VMA_DQ52 VMA_DQ53 VMA_DQ54 VMA_DQ55 VMA_DQ56 VMA_DQ57 VMA_DQ58 VMA_DQ59 VMA_DQ60 VMA_DQ61 VMA_DQ62 VMA_DQ63
FBA_DQM0 FBA_DQM1 FBA_DQM2 FBA_DQM3 FBA_DQM4 FBA_DQM5 FBA_DQM6 FBA_DQM7
VMA_DM0 VMA_DM1 VMA_DM2 VMA_DM3 VMA_DM4 VMA_DM5 VMA_DM6 VMA_DM7
FBA_DQS_WP0 FBA_DQS_WP1 FBA_DQS_WP2 FBA_DQS_WP3 FBA_DQS_WP4 FBA_DQS_WP5 FBA_DQS_WP6 FBA_DQS_WP7
VMA_WDQS0 VMA_WDQS1 VMA_WDQS2 VMA_WDQS3 VMA_WDQS4 VMA_WDQS5 VMA_WDQS6 VMA_WDQS7
FBA_DQS_RN0 FBA_DQS_RN1 FBA_DQS_RN2 FBA_DQS_RN3 FBA_DQS_RN4 FBA_DQS_RN5 FBA_DQS_RN6 FBA_DQS_RN7
VMA_RDQS0 VMA_RDQS1 VMA_RDQS2 VMA_RDQS3 VMA_RDQS4 VMA_RDQS5 VMA_RDQS6 VMA_RDQS7
FB_VREF
+FB_VREF1
TP64
18 VMA_DQ[63..0]
18 VMA_DM[7..0]
18 VMA_WDQS[7..0]
18 VMA_RDQS[7..0]
FBA_CMD0 R5012 10K/F_4
FBA_CMD3 R5010 10K/F_4
FBA_CMD16 R5013 10K/F_4
FBA_CMD19 R5014 10K/F_4
FBA_CMD20 R5015 10K/F_4
U5001I
N10M
PBGA533-NVIDIA-GEFORCE6250
13/13 GND_NC
NC_01 NC_02 (NC_03)PGOOD
C15 D15 J5
R5011 10K/F_4
nVIDIA comment 8/18
GND_01 GND_02 GND_03 GND_04 GND_05 GND_06 GND_07 GND_08 GND_09 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16 GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_25 GND_26 GND_27 GND_28 GND_30 GND_31 GND_32 GND_33 GND_34 GND_35 GND_36 GND_37 GND_38 GND_39 GND_40 GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67 GND_68 GND_69 GND_70 GND_71 GND_72 GND_73 GND_74 GND_75 GND_76 GND_77 GND_78 GND_79 GND_80 GND_81 GND_82 GND_83 GND_84 GND_85 GND_86 GND_87 GND_88
14,16,38 +1.05V_GFX
16,18,38 +1.5V_GFX
NB5
PROJECT : R13J
Quanta Computer Inc.
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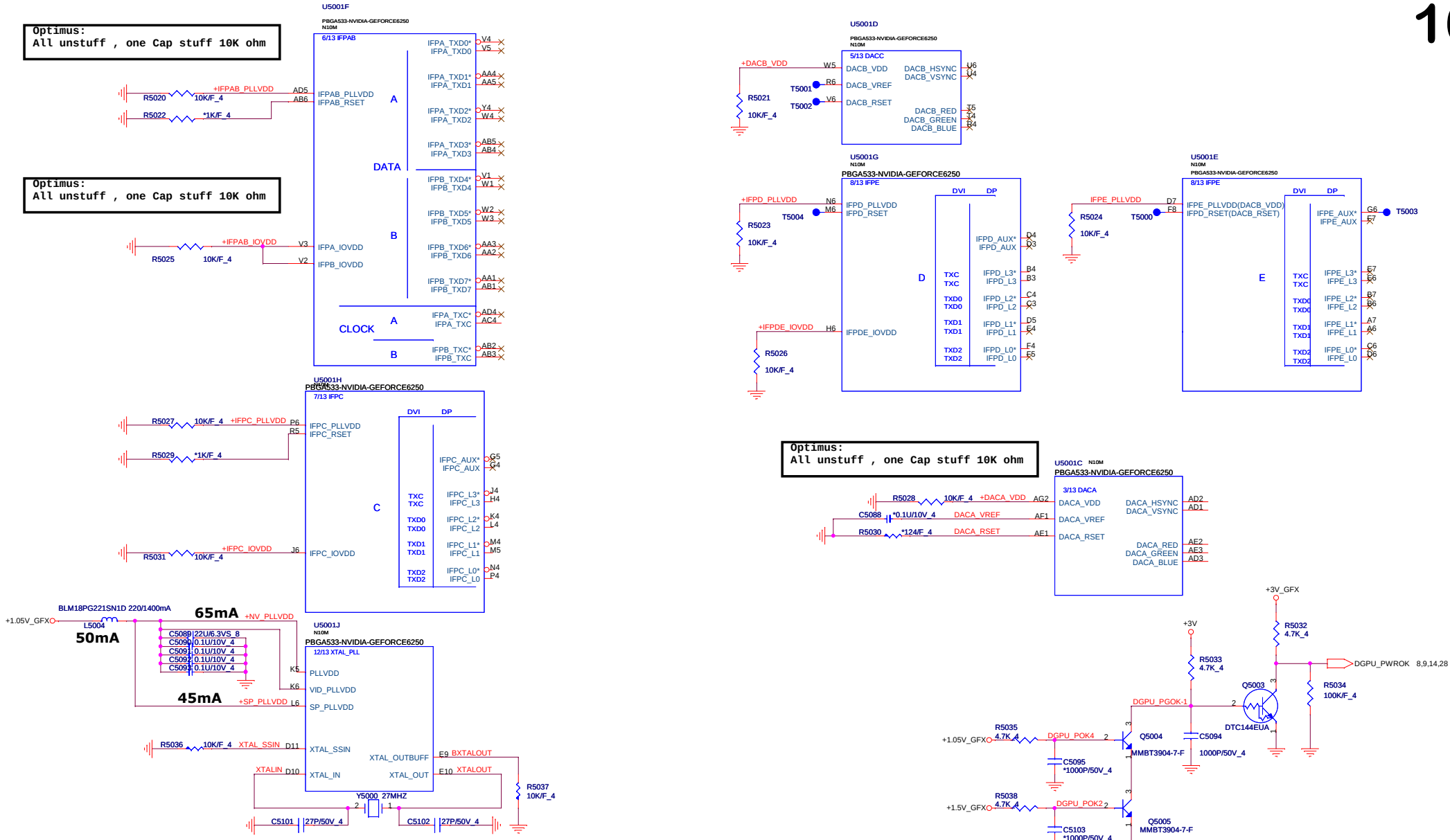
Optimus:
All unstuff , one Cap stuff 10K ohm

Optimus:
All unstuff , one Cap stuff 10K ohm



Optimus:
All unstuff , one Cap stuff 10K ohm

2,6,7,8,9,10,12,13,14,19,20,21,22,23,24,26,27,28,29,32,37,38 +3V
14,17,38 +3V_GFX
14,15,38 +1.05V_GFX

NB5

PROJECT : R13J
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N12P-GV(DISPLAY)	1A

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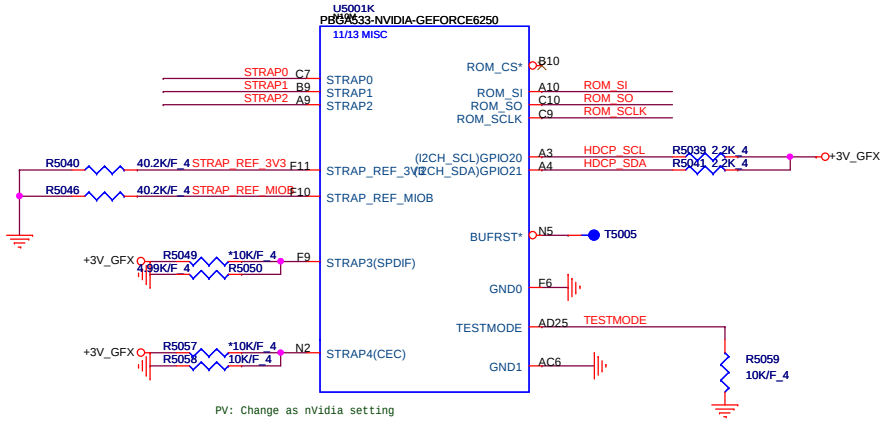
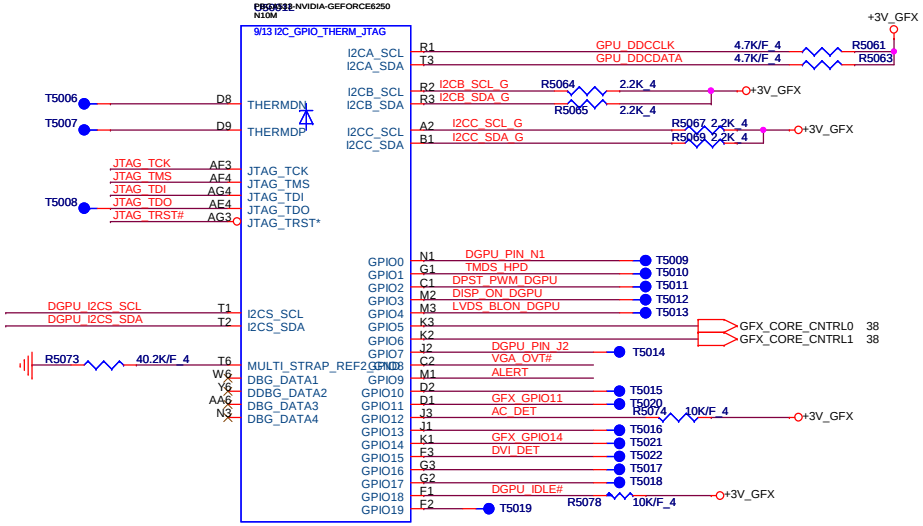
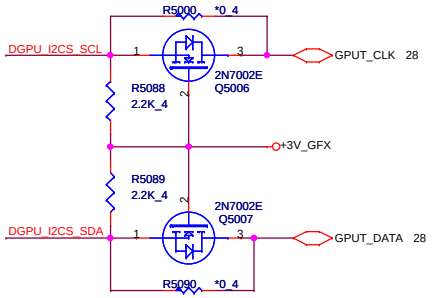
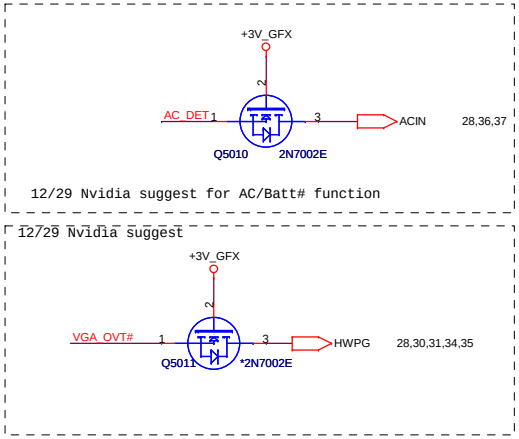



```
ROM_SI -> based on VRAM.

ROM_SO -> PU 10K

ROM_SCLK -> PU 5K

STRAP0 -> PU 45K

STRAP1 -> PD 35K

STRAP2 -> PD 5K

STRAP3 -> PD 5K

STRAP 4 -> PD 10K.
```







N12P-GV -> 0x17F

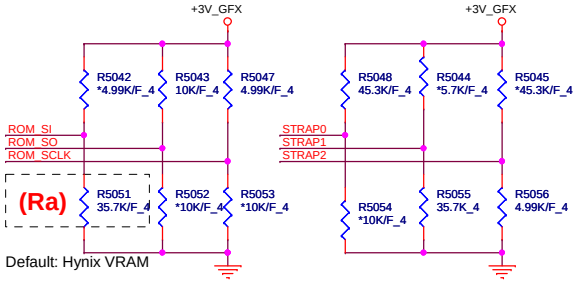
N12M-GE -> 0xA7A 1010 ->PU15K

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

17

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

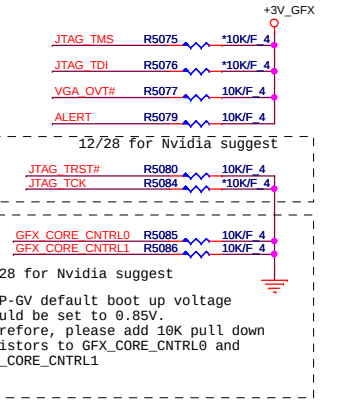


	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

VRAM Configuration Table

(Ra)

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	ROM_SI
0000		Reserved			
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix			PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung			PD 20K
0110	DDR3 128Mx16x4, 128bit, 1GB,900MHz	Hynix	H5TQ2G63BFR-11C	AKD5MGWTW07	PD 35K
0111	DDR3 128Mx16x4, 128bit, 1GB,900MHz	Samsung	K4W2G1646C-HC11	AKD5MGWT508	PD 45K
XXXX					
XXXX					



14,16,38 +3V_GFX

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	I-C-T
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	Memory VREF SELECT
11	I/O	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	THERM_LOAD_STEP_DOWN
14	OUT	N/A	THERM_LOAD_STEP_UP

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PROJECT : R13J
Quanta Computer Inc.

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Custom	N12P-GV(GPIO/STRAPS)	1A

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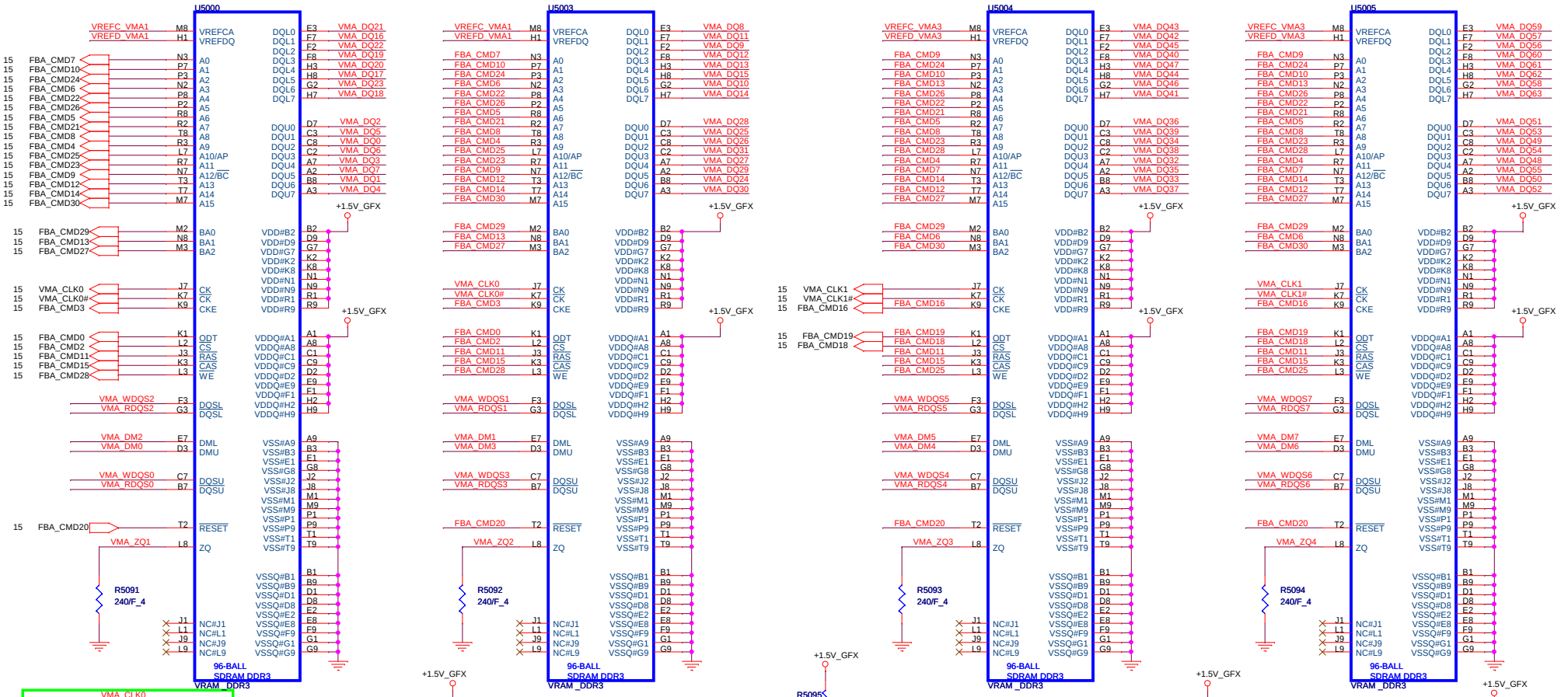
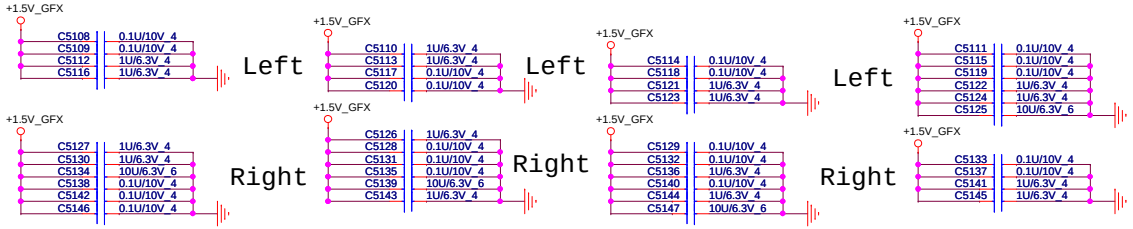
CHANNEL A: 256MB/512MB DDR3

15 VMA_DQ[63..0]
15 VMA_DM[7..0]
15 VMA_WDQS[7..0]
15 VMA_RDQS[7..0]





	QCI PN
Hynix 512MB	AKD5LZGTW00
Samsung 512MB	AKD5LGGT502
Hynix 1GB	AKD5MGWTW07
Samsung 1GB	AKD5MGWT508

15,16,38 +1.5V_GFX

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PROJECT : R13J
Quanta Computer Inc.

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Custom	DDR3 VRAM(BGA96)	1A

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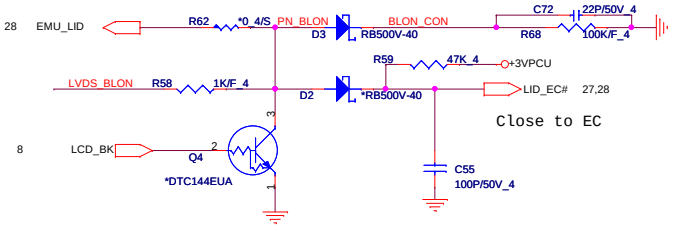
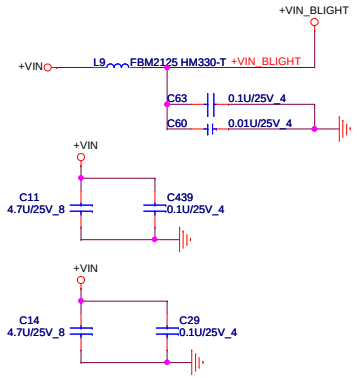
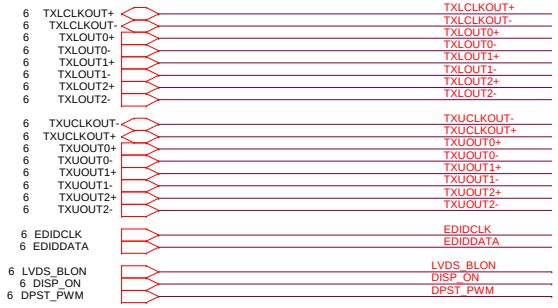
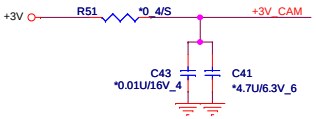
LID Switch



100mA



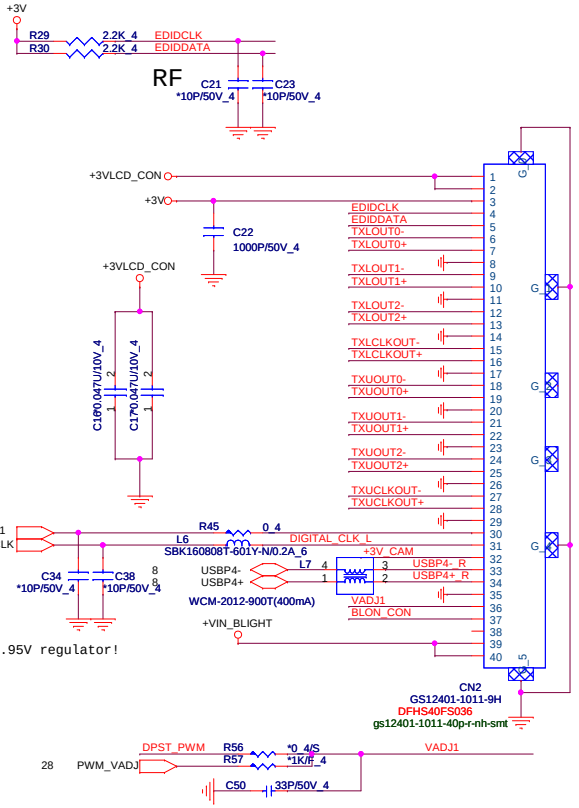




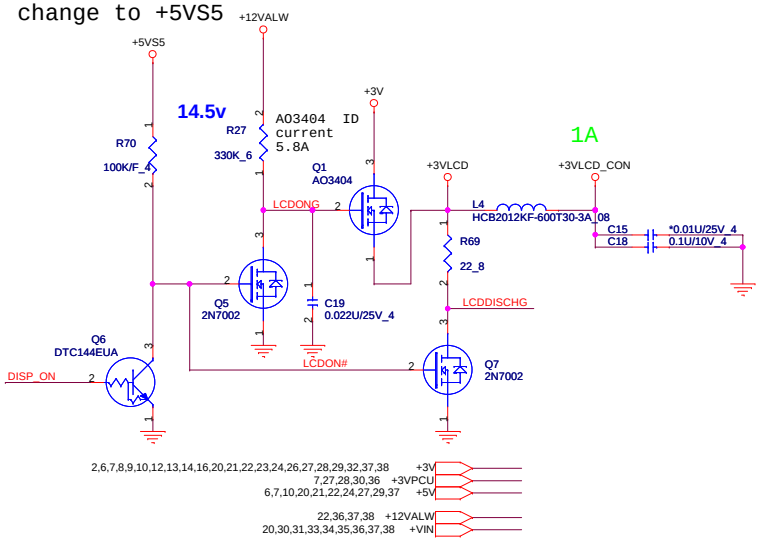
Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!

follow L7 location

DEL reserved Rester



change to +5VS5



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Quanta Computer Inc.

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Custom	LCD CONN/LID/CAM	1A

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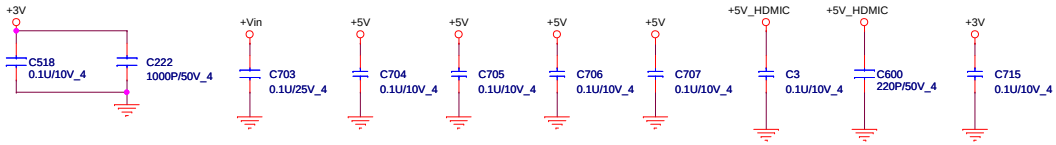
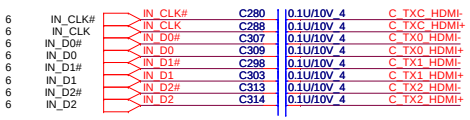
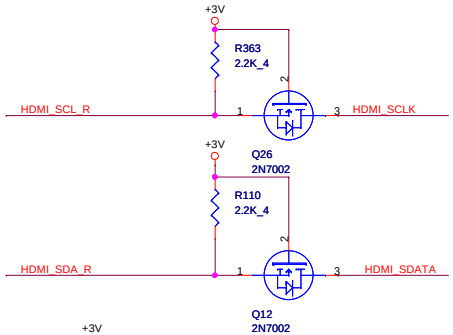
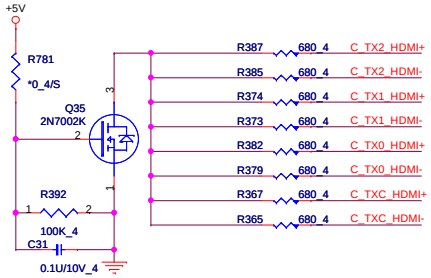


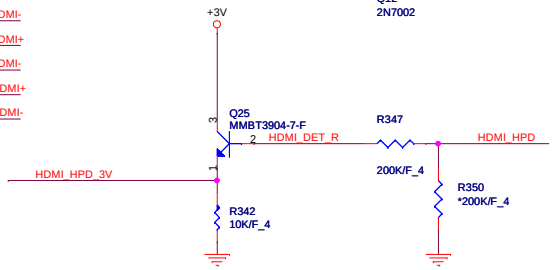
close to HDMI conn

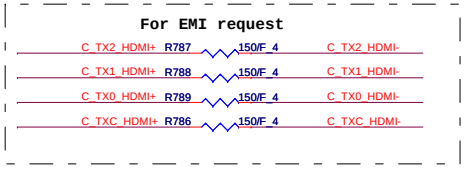


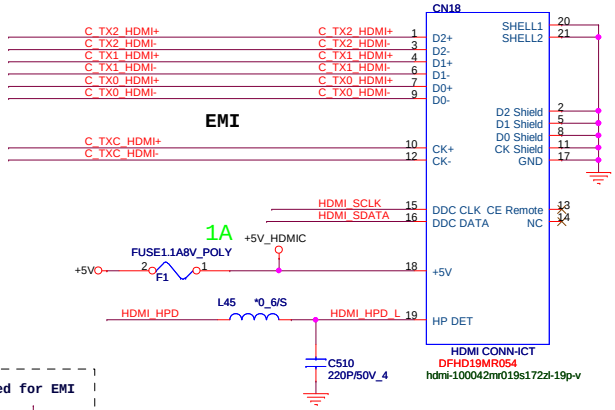
Close to HDMI Connector

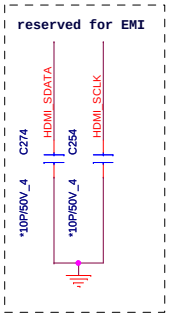


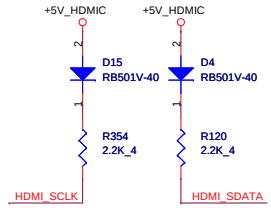












NB5	**PROJECT : R13J** Quanta Computer Inc.	
Size: Custom	Document Number: **HDMI CONN**	Rev: 1A
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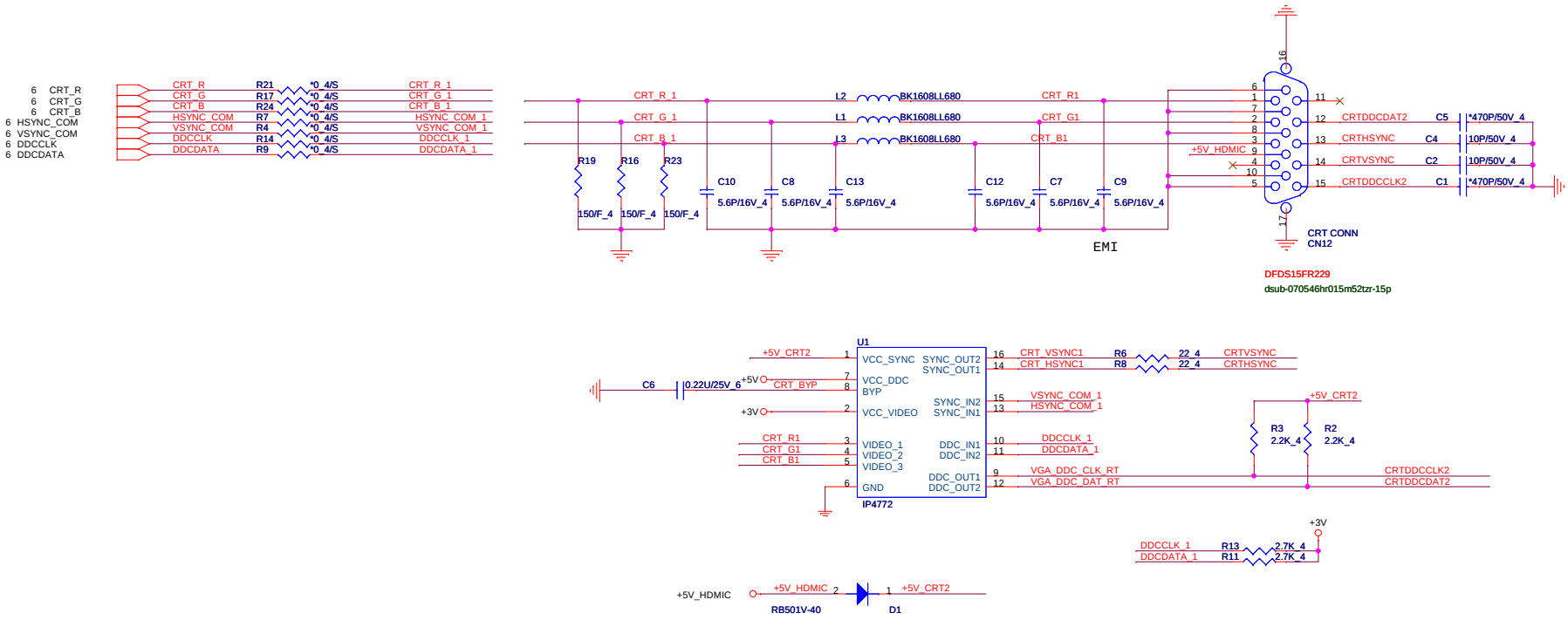
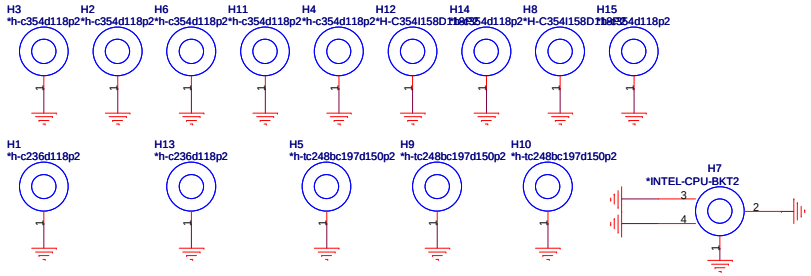
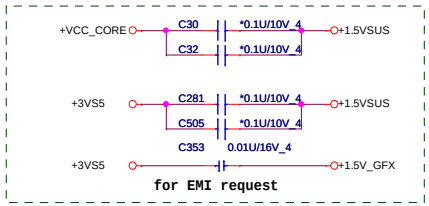
CRT PORT



HOLE





NB5	**PROJECT : R13J** Quanta Computer Inc.	
Size Custom	Document Number **CRT,Hole**	Rev 1A
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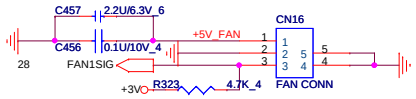
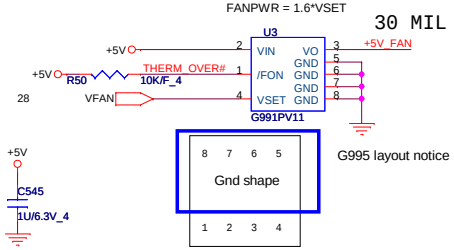
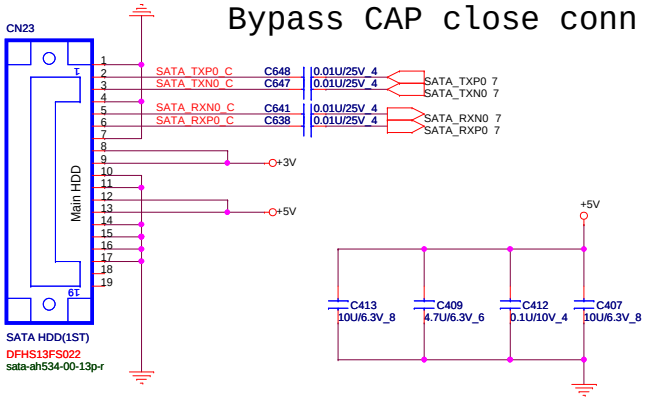
CPU FAN

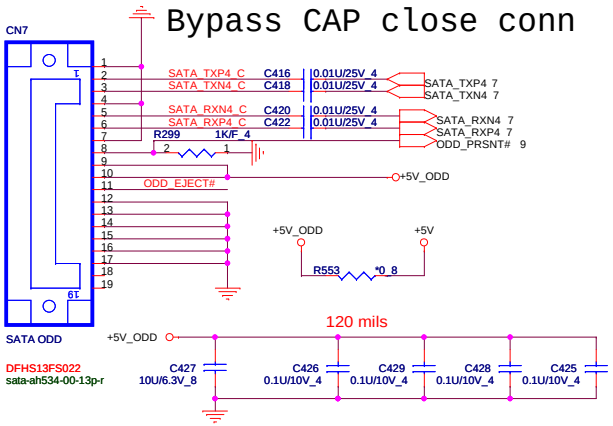


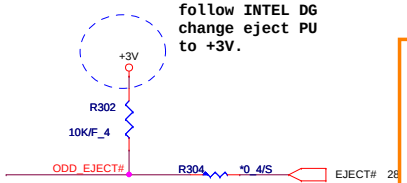


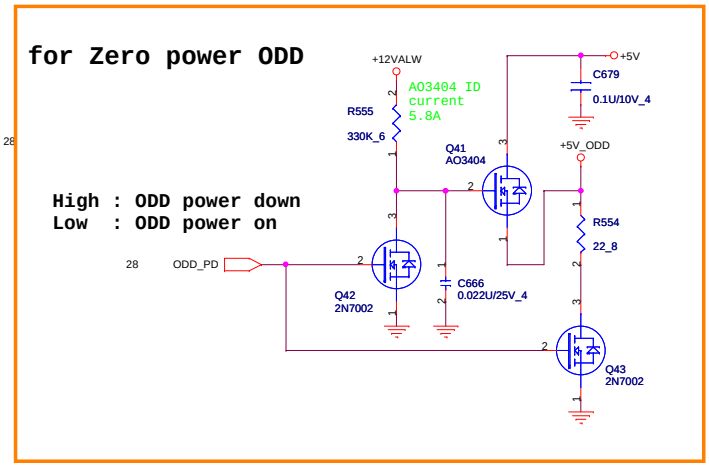
SATA HDD CONNECTOR



SATA ODD CONNECTOR







NB5	PROJECT : R13J Quanta Computer Inc.	
Size: Custom	Document Number: HDD/ODD/FAN	Rev: 1A
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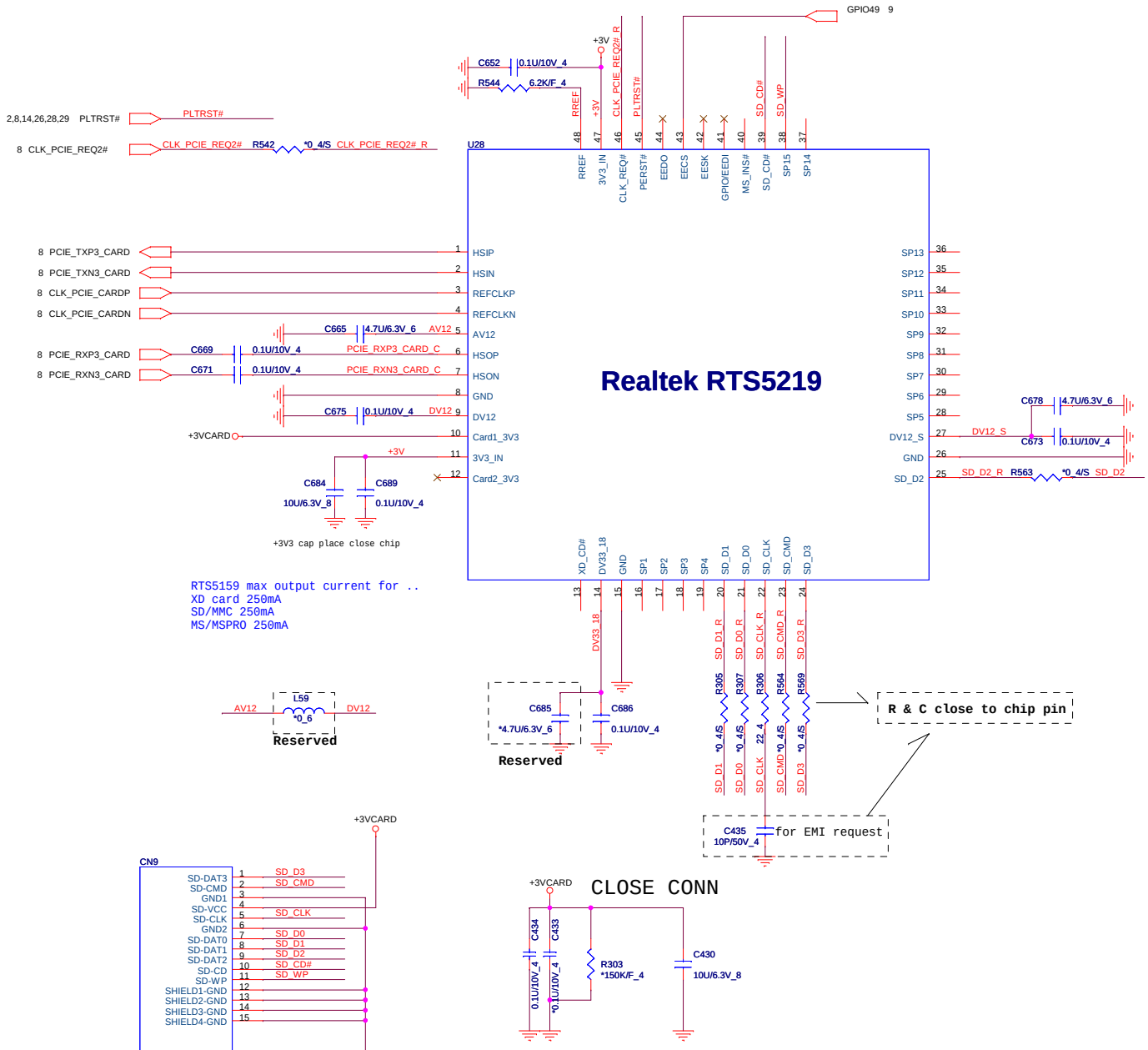

PROJECT : R13J
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5219 & CR SOCKET &HOLE	1A

NB5

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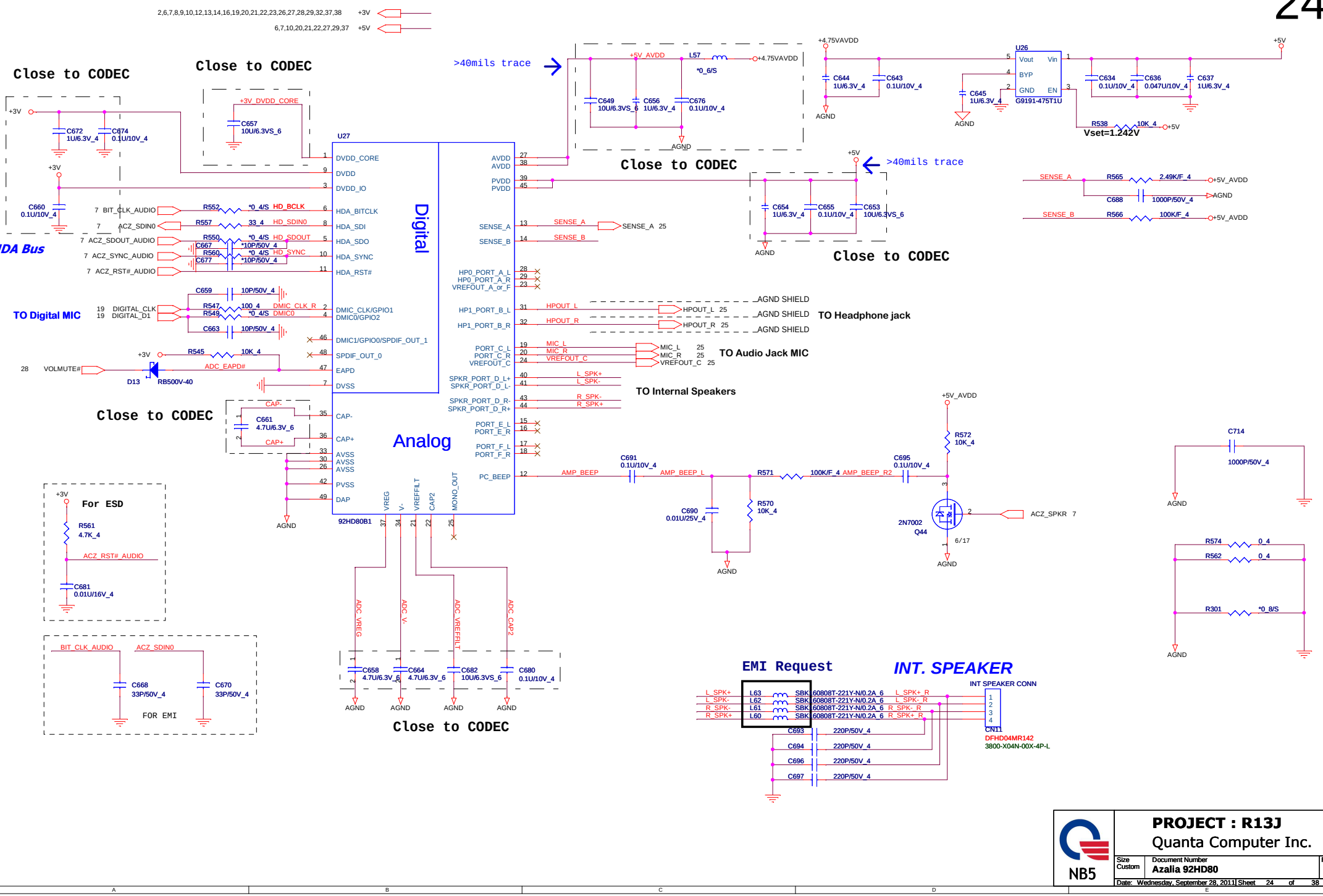
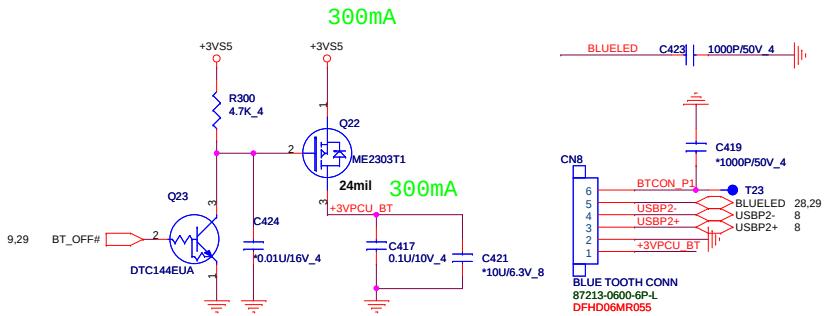
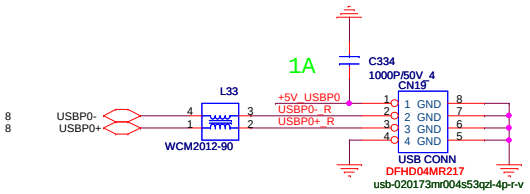


PROJECT : R13J	
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: Azalia 92HD80; Rev: 1A
Date: Wednesday, September 28, 2011	Sheet 24 of 38

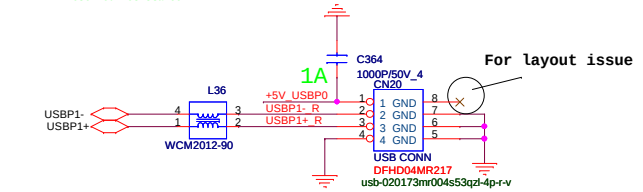
BLUETOOTH

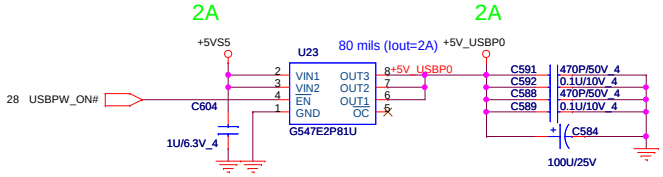


LEFT SIDE USBX2

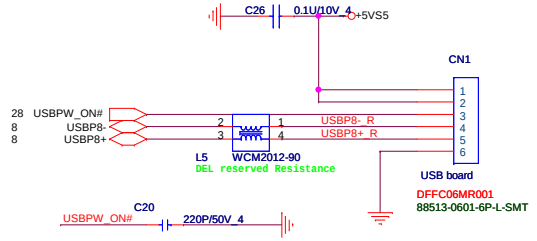


DEL reserved Resistance

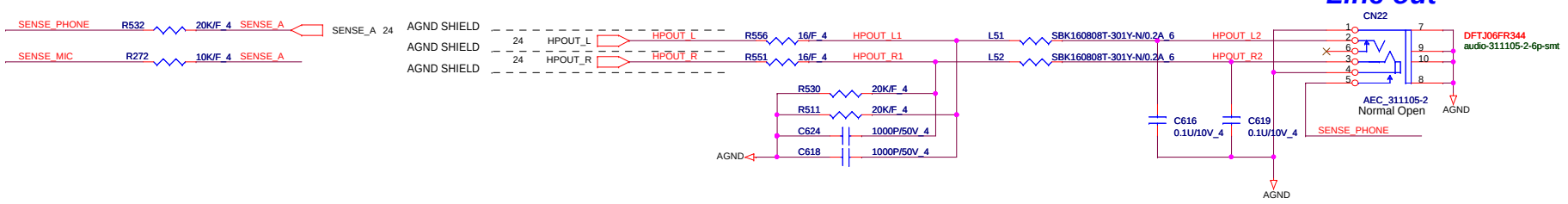




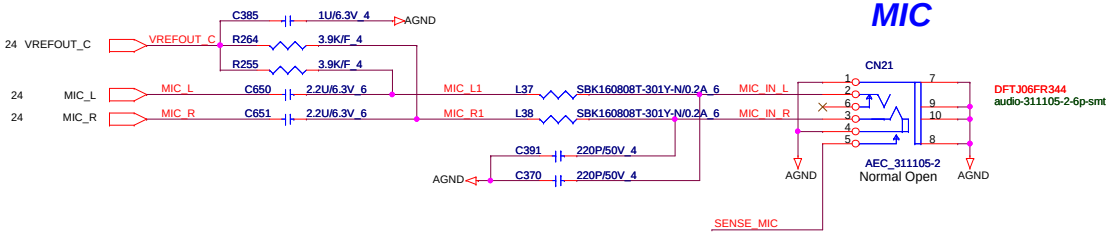
Right SIDE USBX1



Line out



MIC



NB5	**PROJECT : R13J** Quanta Computer Inc.	
	Size: Custom Document Number: **USB/BT/Audio JacK**	Rev: 1A
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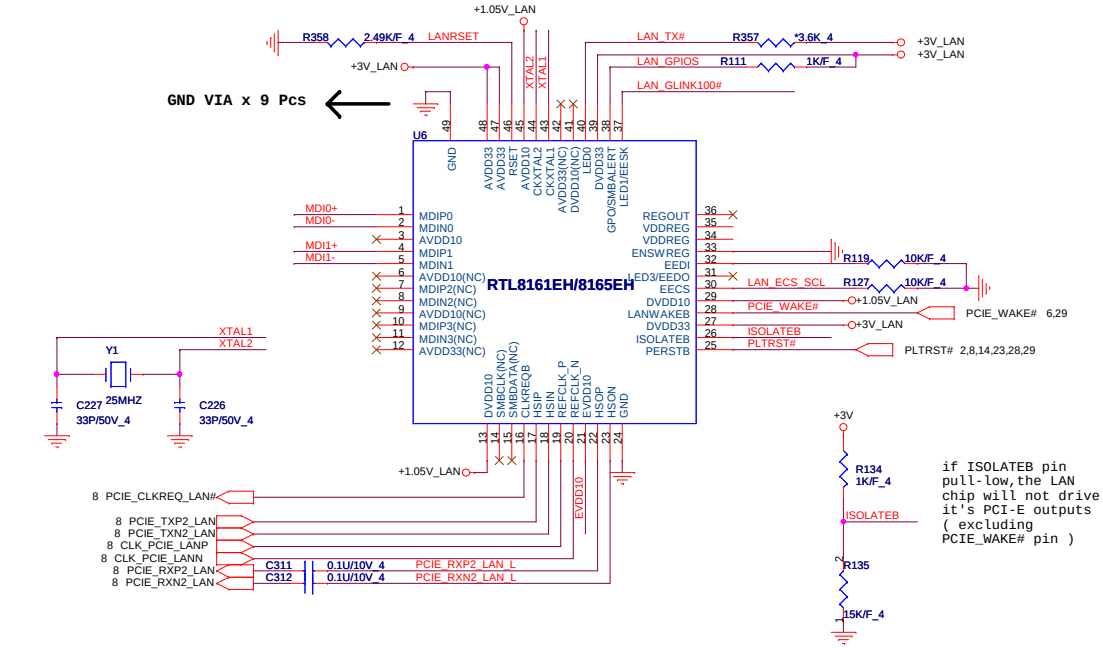
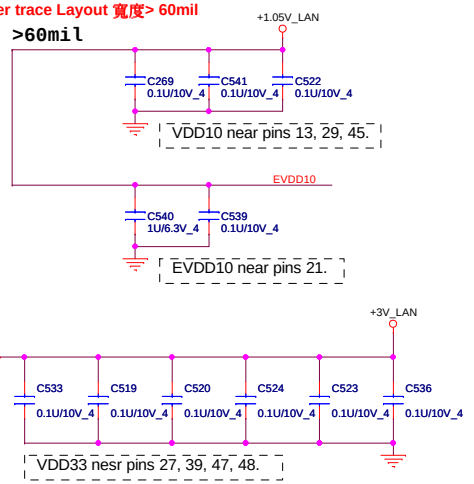
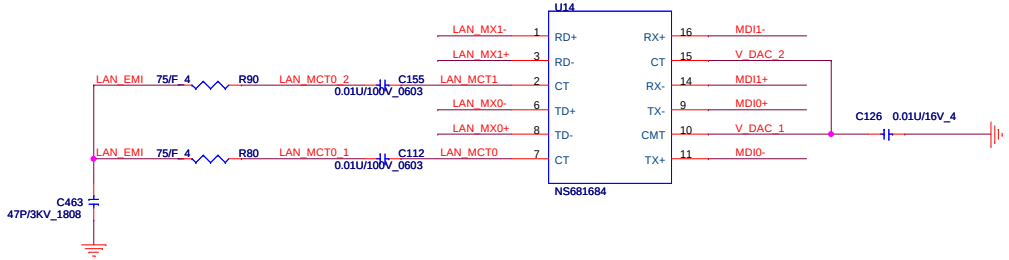


if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

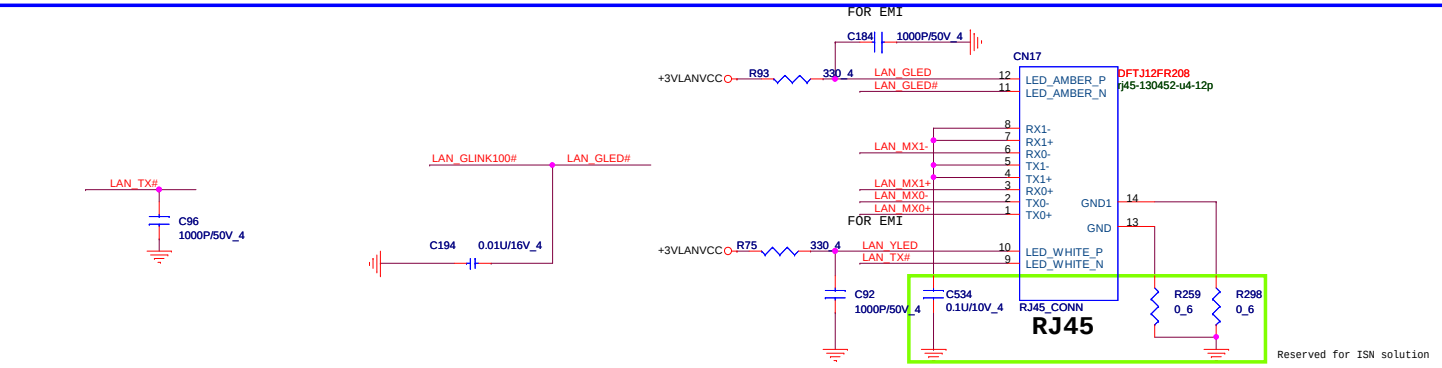
Power trace Layout 寬度> 60mil



Transformer for 10/100



Lan Con.



NB5	PROJECT : R13J Quanta Computer Inc.	
Size: Custom	Document Number: RTL8165EH	Rev: 1A
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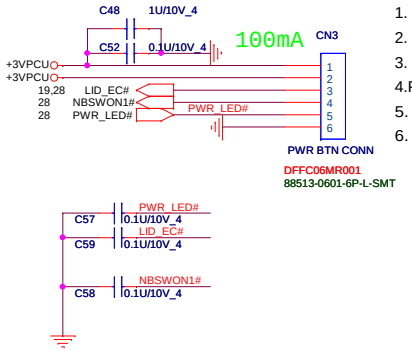
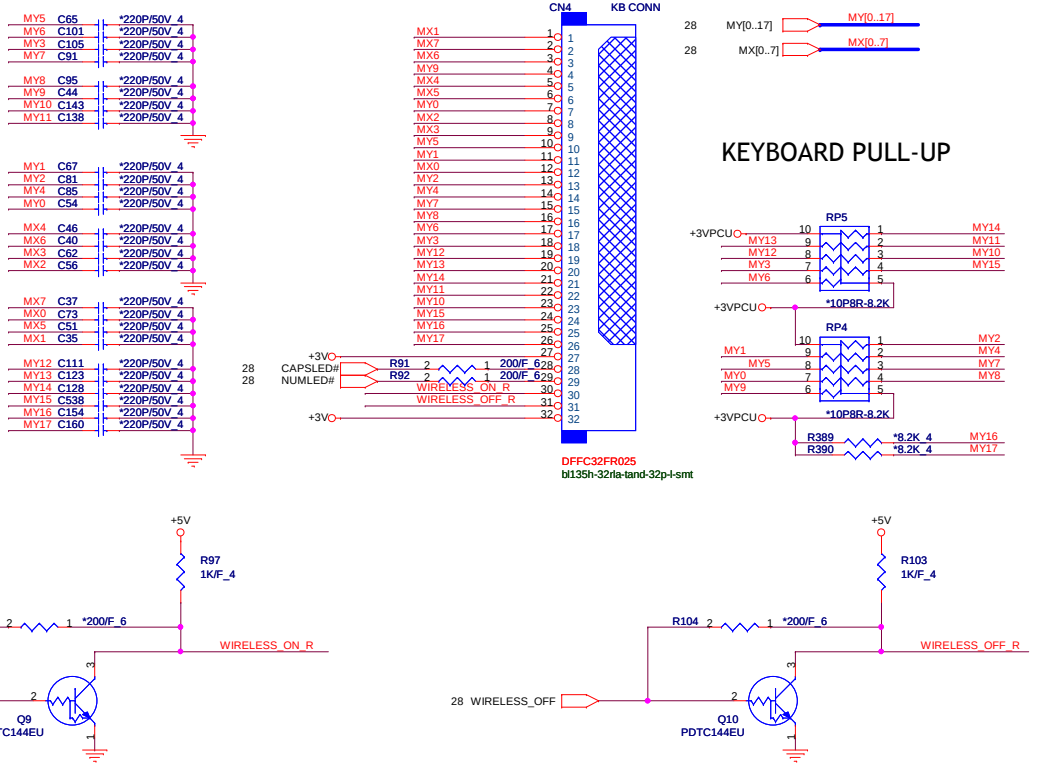
POWER BOTTON CONNECT



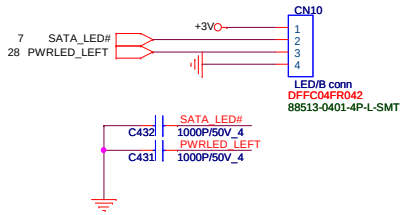
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

KEYBOARD Con.

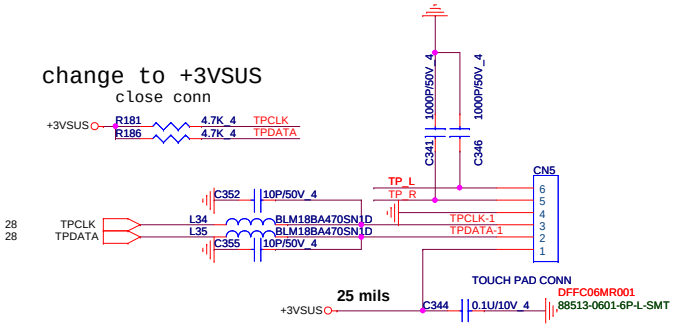


LED Con.

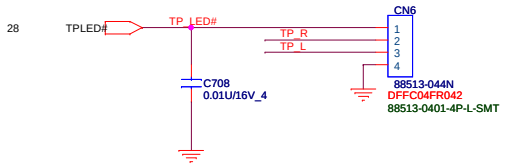
1. +3V
2. SATA_LED#
3. PWR_LED#
4.GND



TOUCH PAD Con.



To TOUCH PAD SW board



7,19,28,30,36 +3VPCU
6,7,10,20,21,22,24,29,37 +5V
29,37 +3VSUS
2,6,7,8,9,10,12,13,14,16,19,20,21,22,23,24,26,28,29,32,37,38 +3V

NB5

PROJECT : R13J

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A

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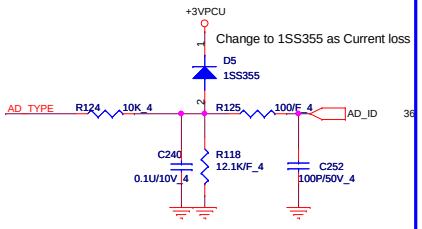
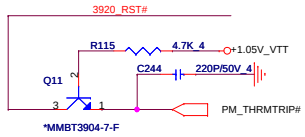
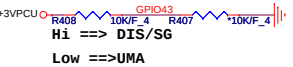
adapter Type check



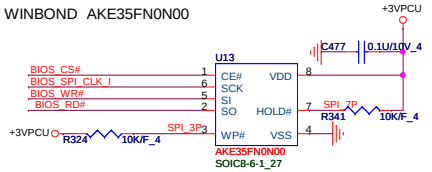


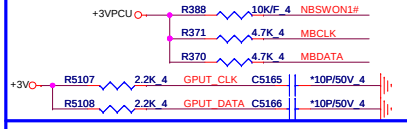
adapter select for EC

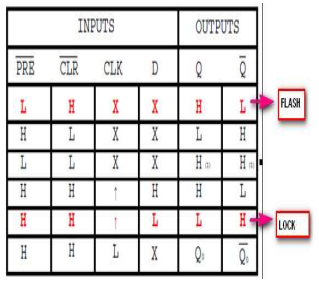


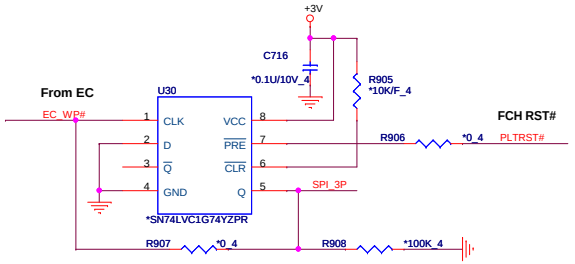
128K byte SPI EC ROM

Socket: DG008000031
EON AKE35FN0Q00
WINBOND AKE35FN0N00





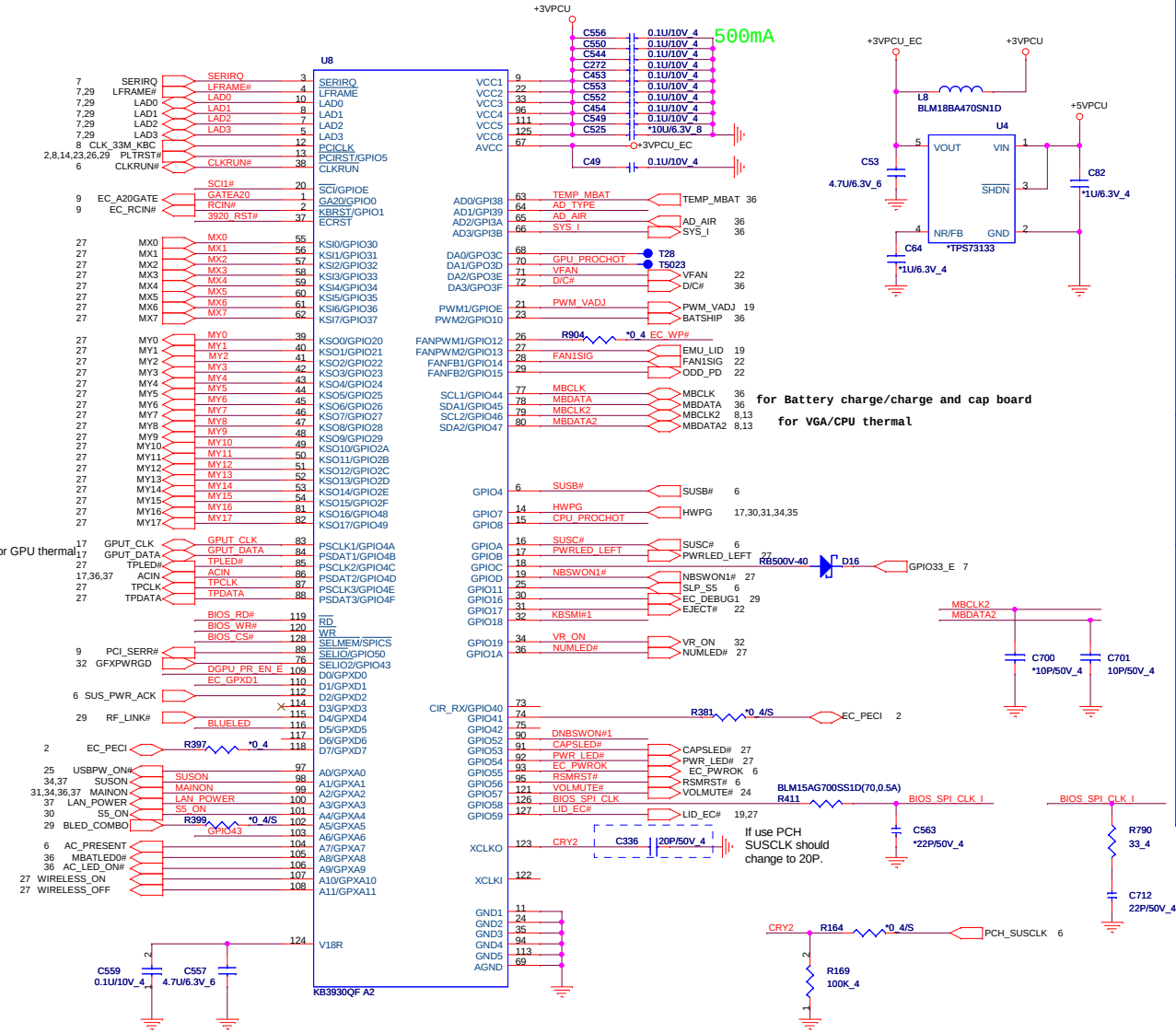


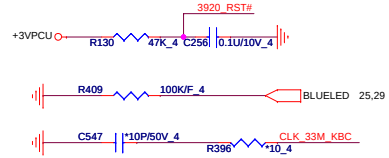


Change to RB500 as Current loss

Add Pin 117,103 for DSM,116 for Bluetooth

Delete T10 and tie pin 117 from Lan for DSM





2,4,6,7,8,10,31,32,38 +1.05V_VTT
2,6,7,8,9,10,12,13,14,16,19,20,21,22,23,24,26,27,29,32,37,38 +3V
7,19,27,30,36 +3VPCU
30,36 +5VPCU

PROJECT : R13J
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	EC (KB3926)/ROM	1A

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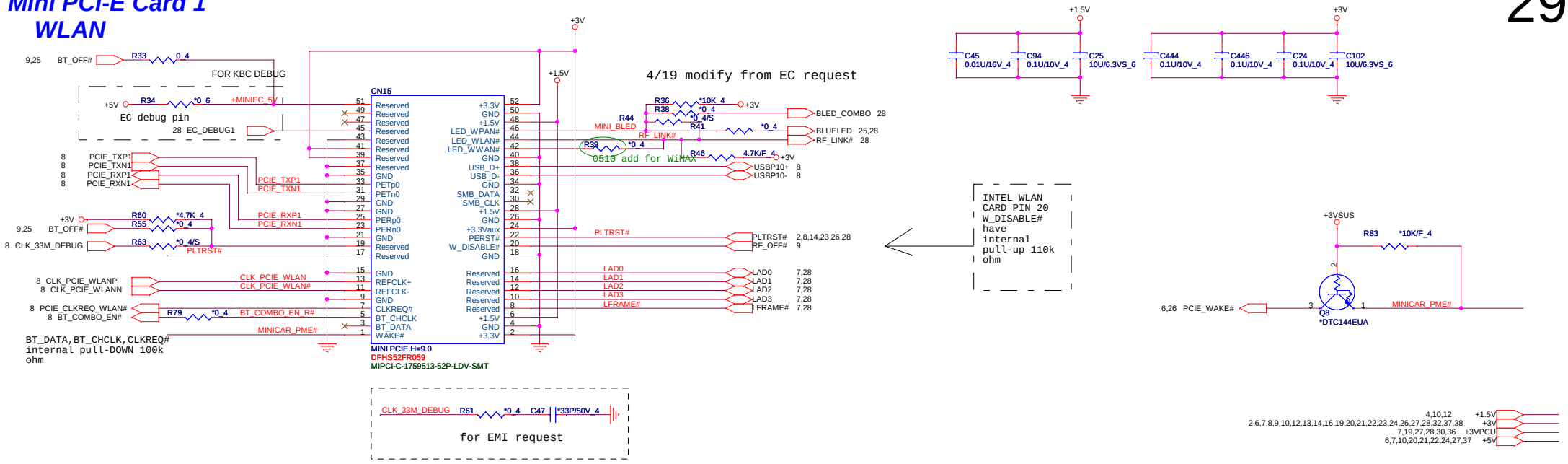
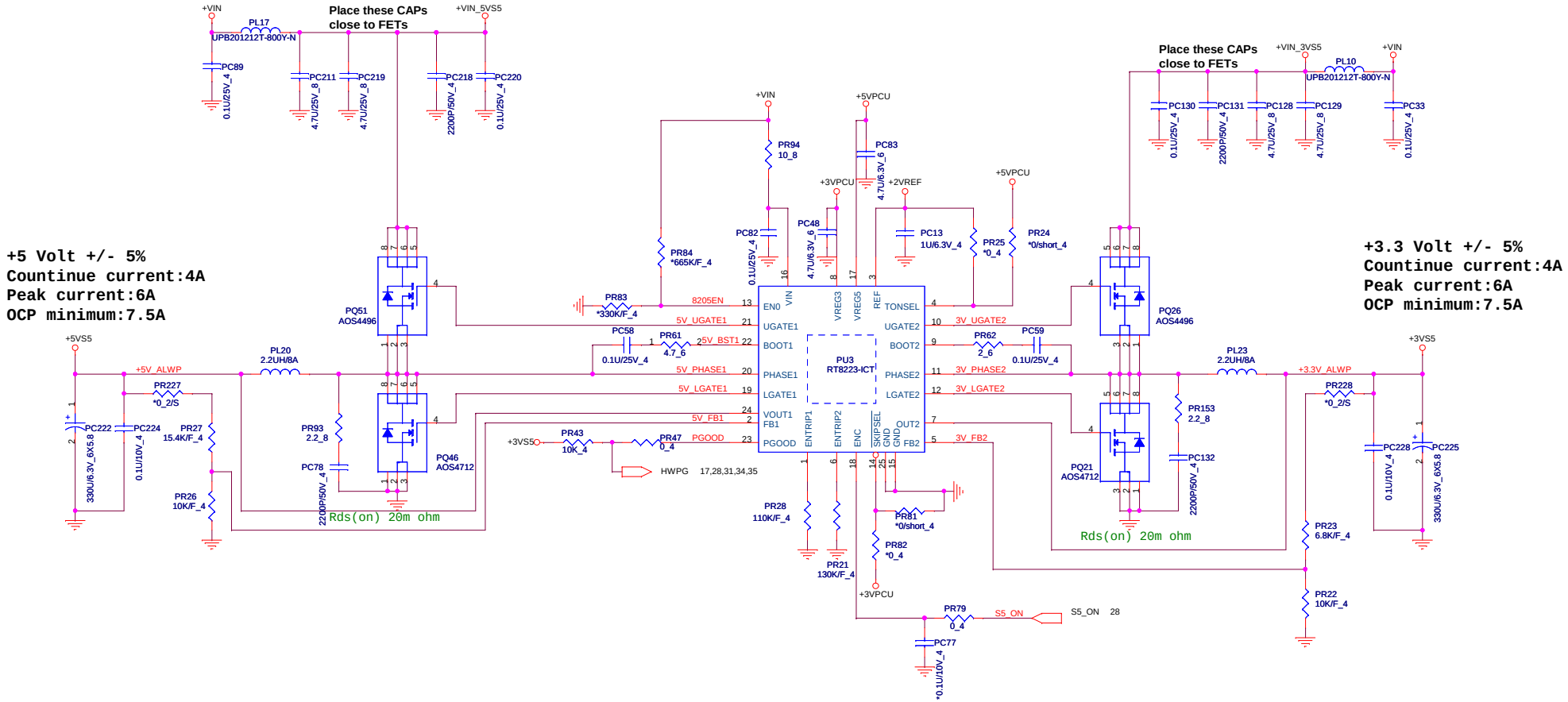
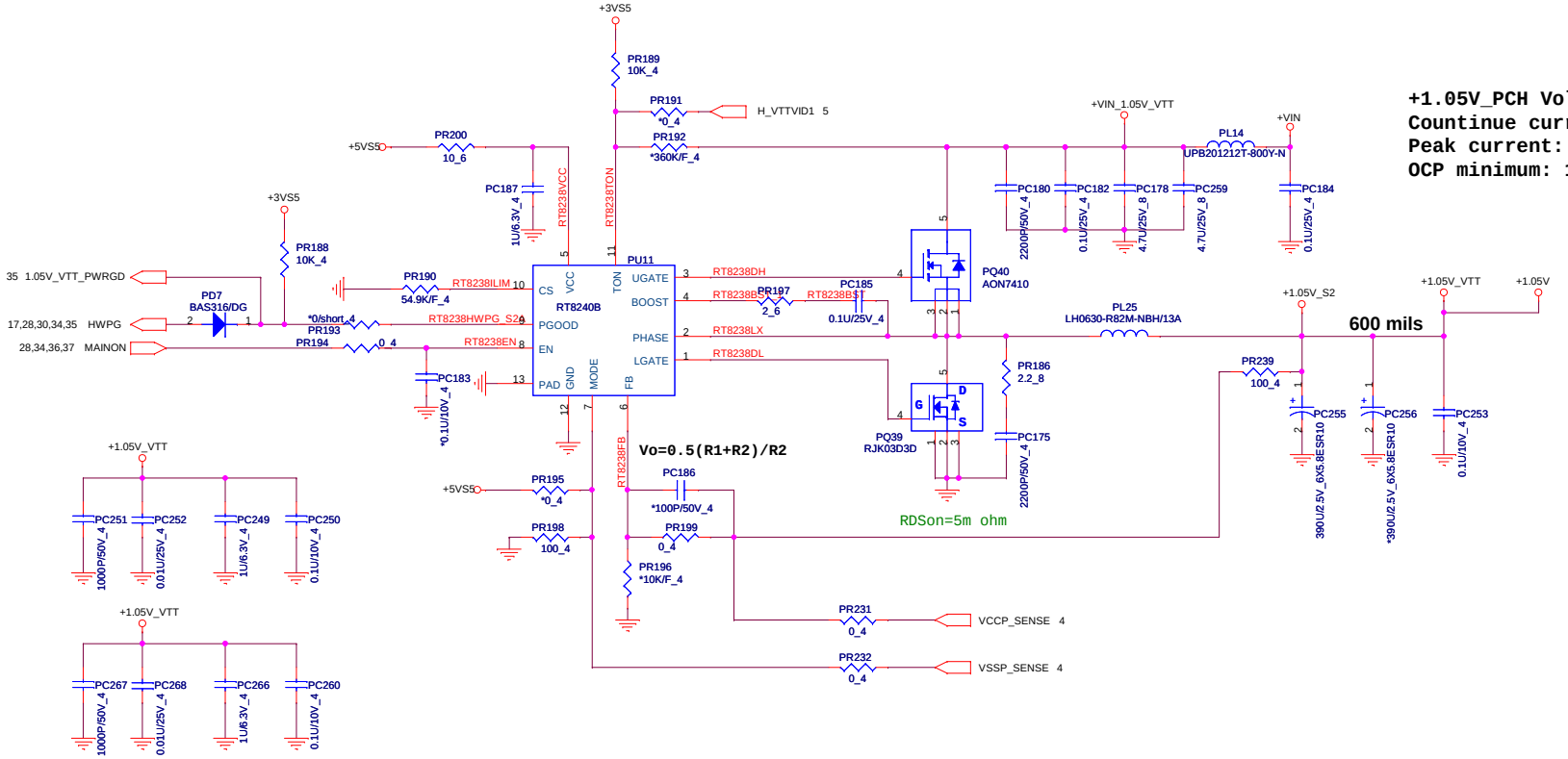
Mini PCI-E Card 1
WLAN



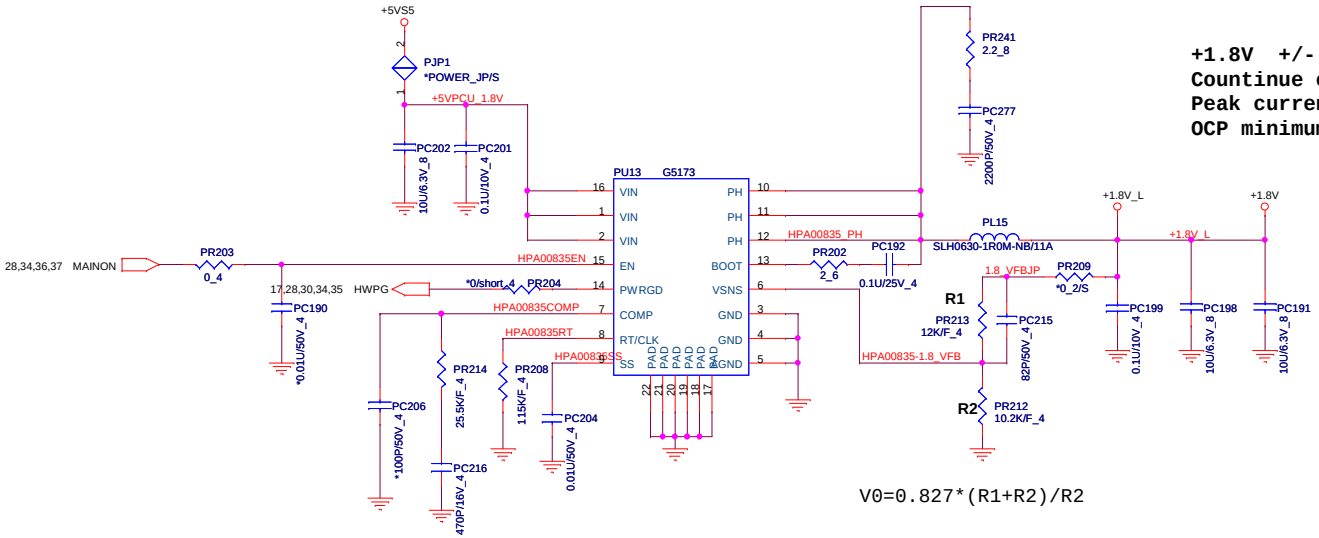
NB5	PROJECT : R13J Quanta Computer Inc.		
	Size: Custom	Document Number: MINI PCIE CONN X1	Rev: 1A
	Date: Wednesday, September 28, 2011	Sheet 29 of 38	



NB5	PROJECT : R13J Quanta Computer Inc.		
Size Custom	Document Number +5V/+3V (RT8206B)		Rev 1A
Date: Wednesday, September 28, 2011	Sheet 30 of 38		



+1.05V_PCH Volt +/- 5%
Countinue current:10A
Peak current: 12A
OCP minimum: 14.5A



+1.8V +/- 5%
Countinue current:1.5A
Peak current:2.5A
OCP minimum 4A

V0=0.827*(R1+R2)/R2

PROJECT : R13J
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1V VTT / PCH	1A

NB5

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1.Alert trace routing
between data and clock trace
2.Refer to ground
3.Keep out 20 mils

SV 35W CPU
VID1=1.05V
IccMax=54A
R_LL=1.9m ohm
OCP~60A

PV change
footprint 12/9

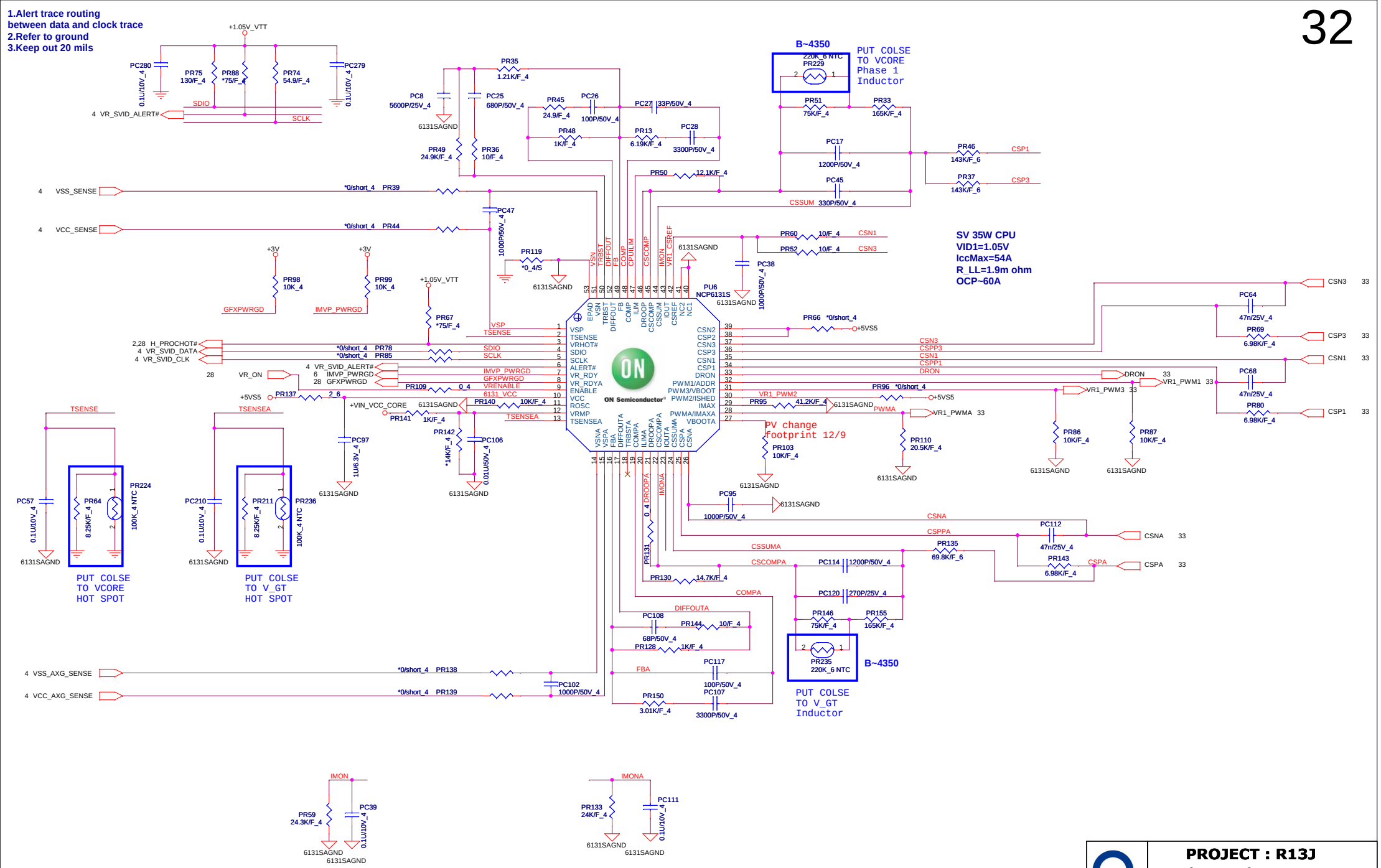
PUT COLSE
TO VCORE
HOT SPOT

PUT COLSE
TO V_GT
HOT SPOT

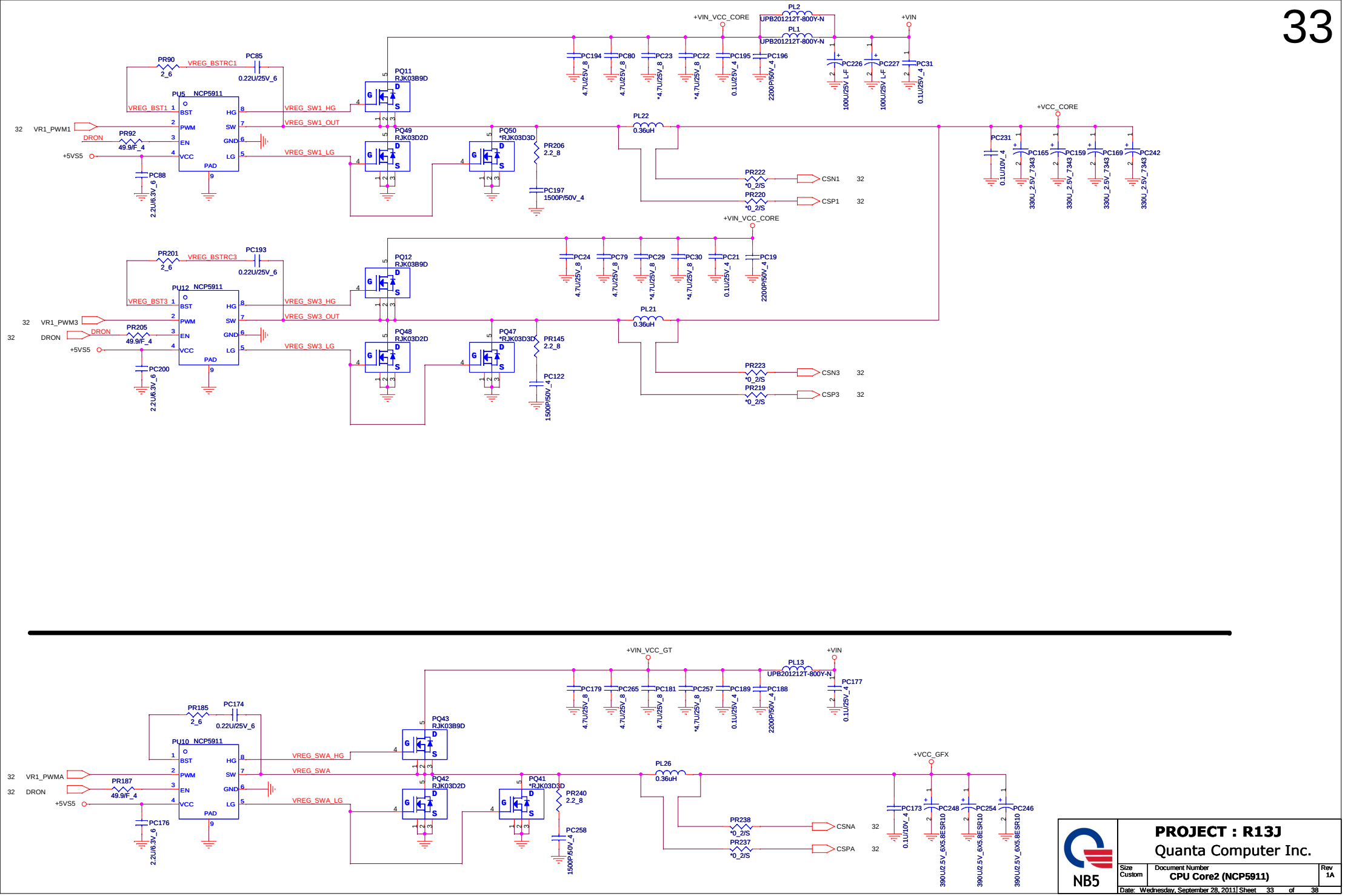
B~4350
PUT COLSE
TO VCORE
Phase 1
Inductor

B~4350
PUT COLSE
TO V_GT
Inductor

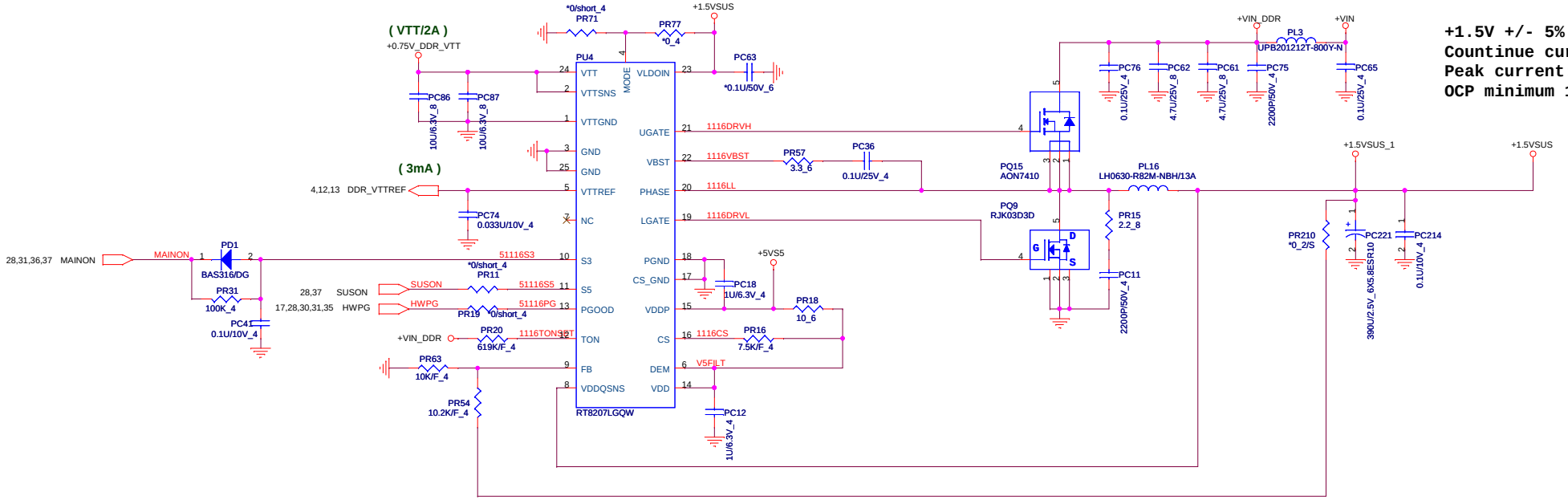
PU6
NCP6131S



NB5	PROJECT : R13J Quanta Computer Inc.		
	Size: Custom	Document Number: CPU Core1 (NCP6131S)	Rev: 1A
	Date: Wednesday, September 28, 2011	Sheet 32 of 38	



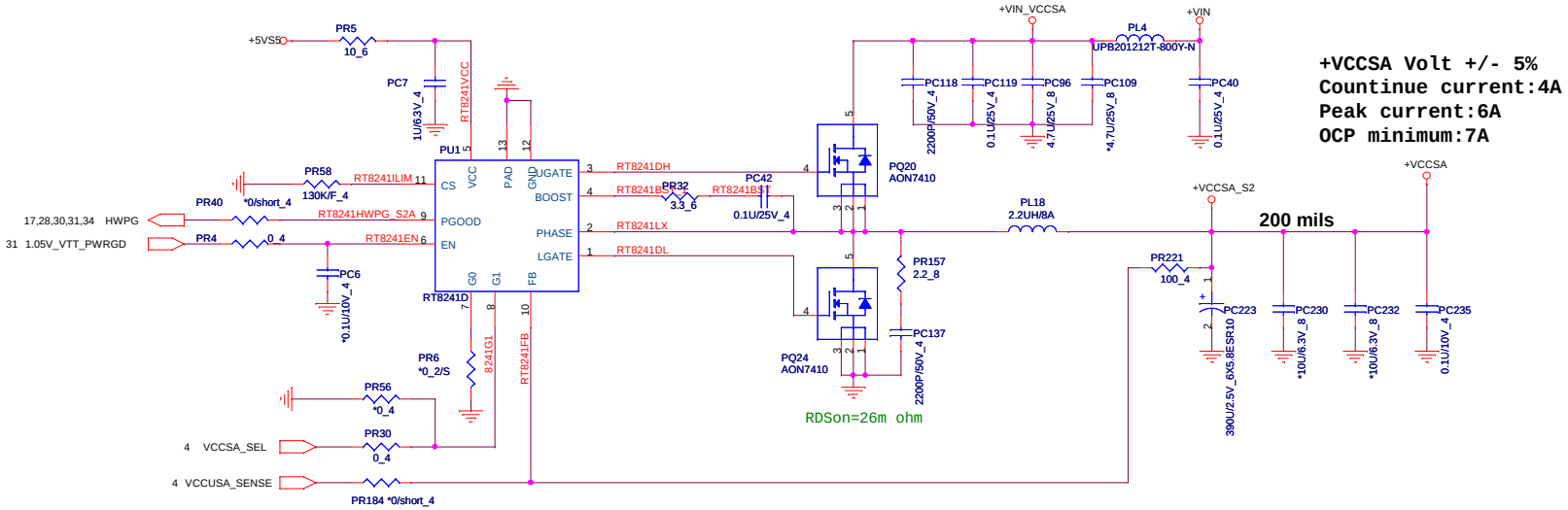
NB5	**PROJECT : R13J** Quanta Computer Inc.	
Size: Custom	Document Number: **CPU Core2 (NCP5911)**	Rev: 1A
Date: Wednesday, September 28, 2011	Sheet 33 of 38	



+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

2011_0217 modify for EE request cancel 1.0V_VGA

NB5	**PROJECT : R13J** Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 (RT8207)	Rev: 1A
Date: Wednesday, September 28, 2011	Sheet 34 of 38	



NB5	**PROJECT : R13J** Quanta Computer Inc.	
Size: Custom	Document Number: +1.1V VTT / PCH	Rev: 1A
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0916 for EMI

DC_JACK
90W
1025 change footprint for EE request

Do Not add test pad on BATDIS_G signal

Place this ZVS close to Diode away +VIN

0922 for EMI

To PWR LED

Place this ZVS close to Far-Far away +VIN

0922 for EMI

Place this cap close to EC

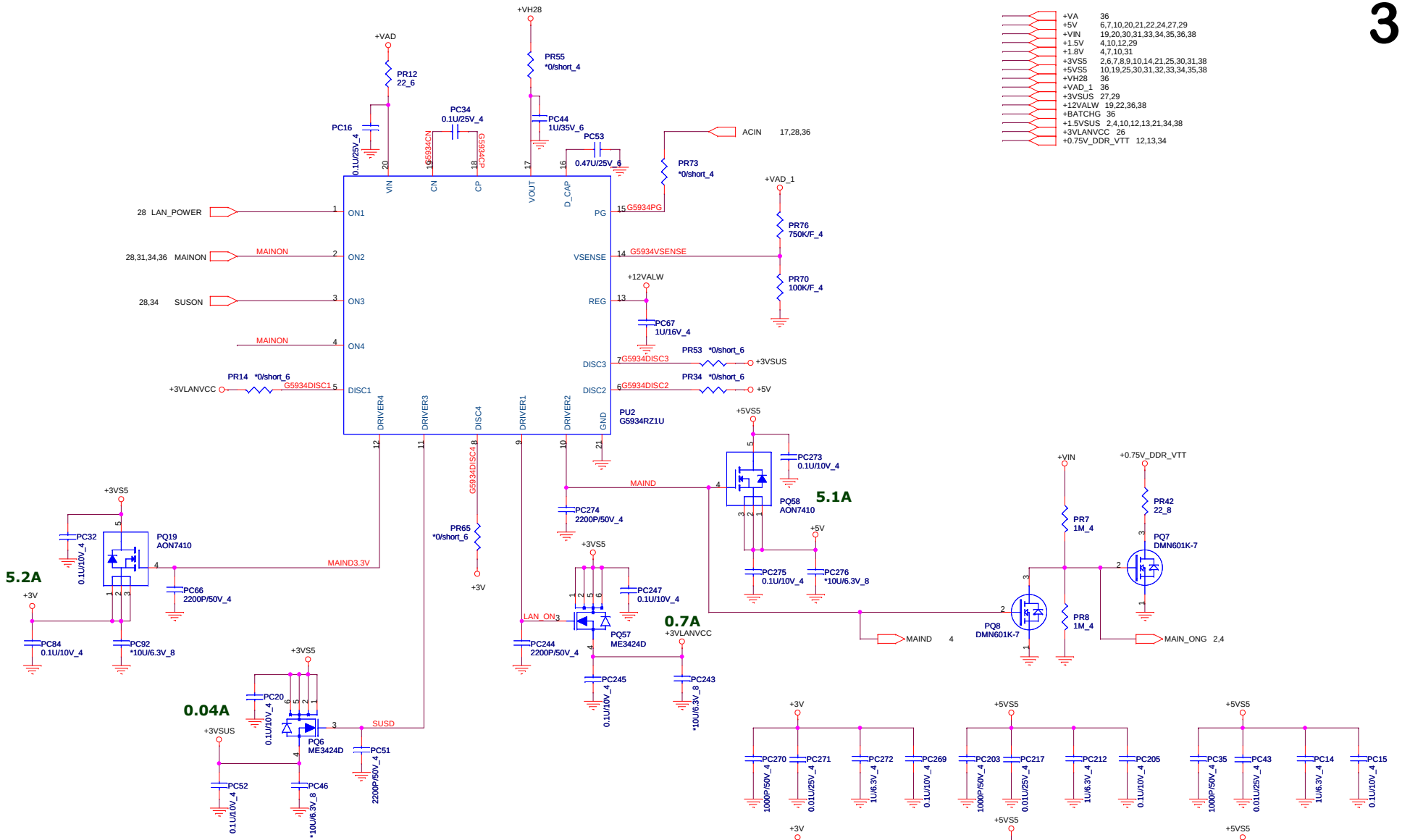
Place this cap close to EC

Place this cap close to EC

Place this cap close to EC

+VA
+VH28 37
+VAD_1 37
+3VPCU 7,19,27,28,30
+5VPCU 28,30
+BATCHG

NB5	PROJECT : R13J Quanta Computer Inc.		
	Size: Custom	Document Number: Charger (OZ8681)	Rev: 1A
	Date: Wednesday, September 28, 2011	Sheet 36 of 38	



PROJECT : R13J

Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	1A

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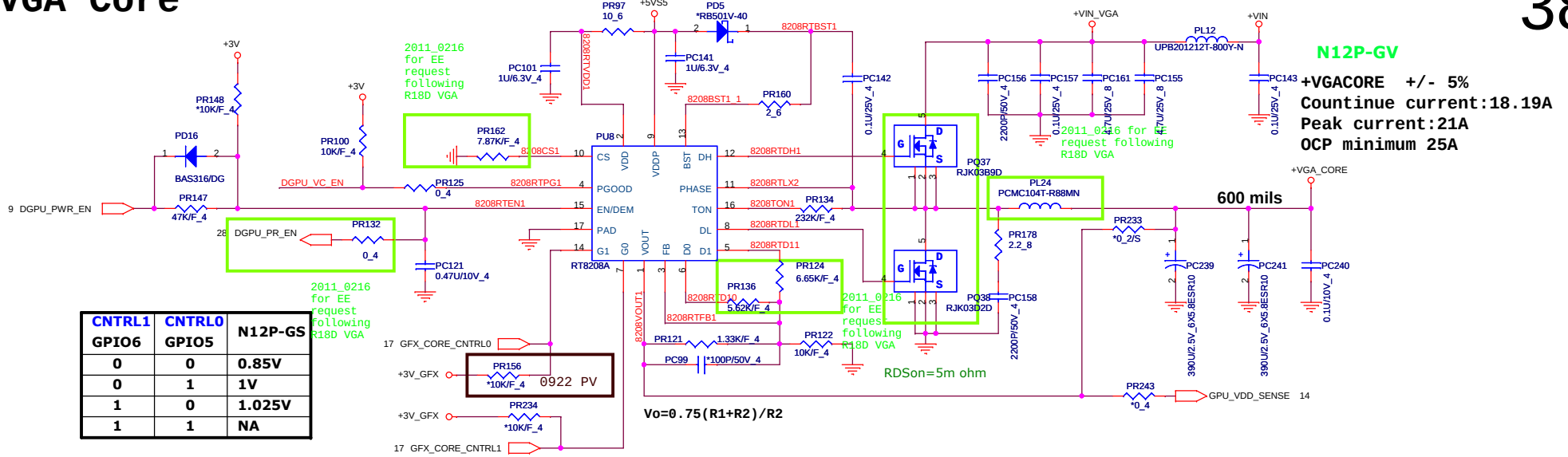
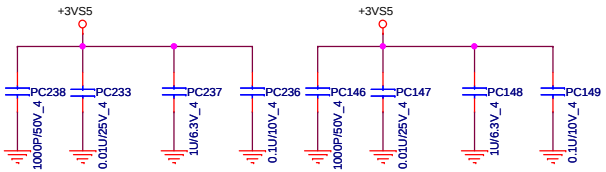
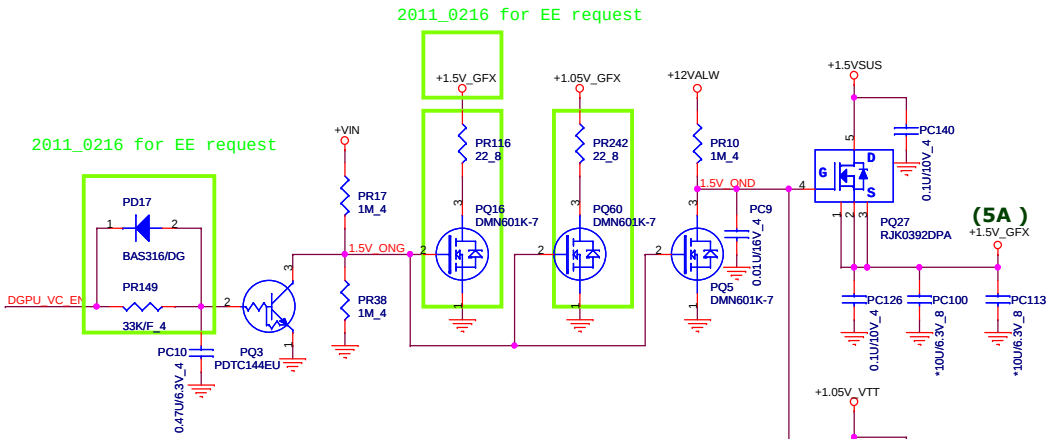
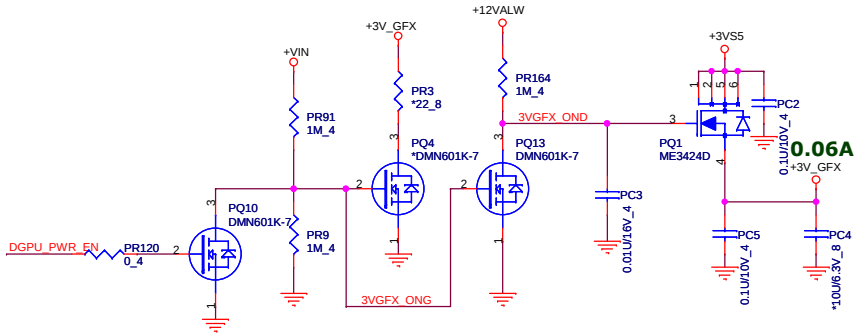
VGA Core



CNTRL1 GPIO6	CNTRL0 GPIO5	N12P-GS
0	0	0.85V
0	1	1V
1	0	1.025V
1	1	NA







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