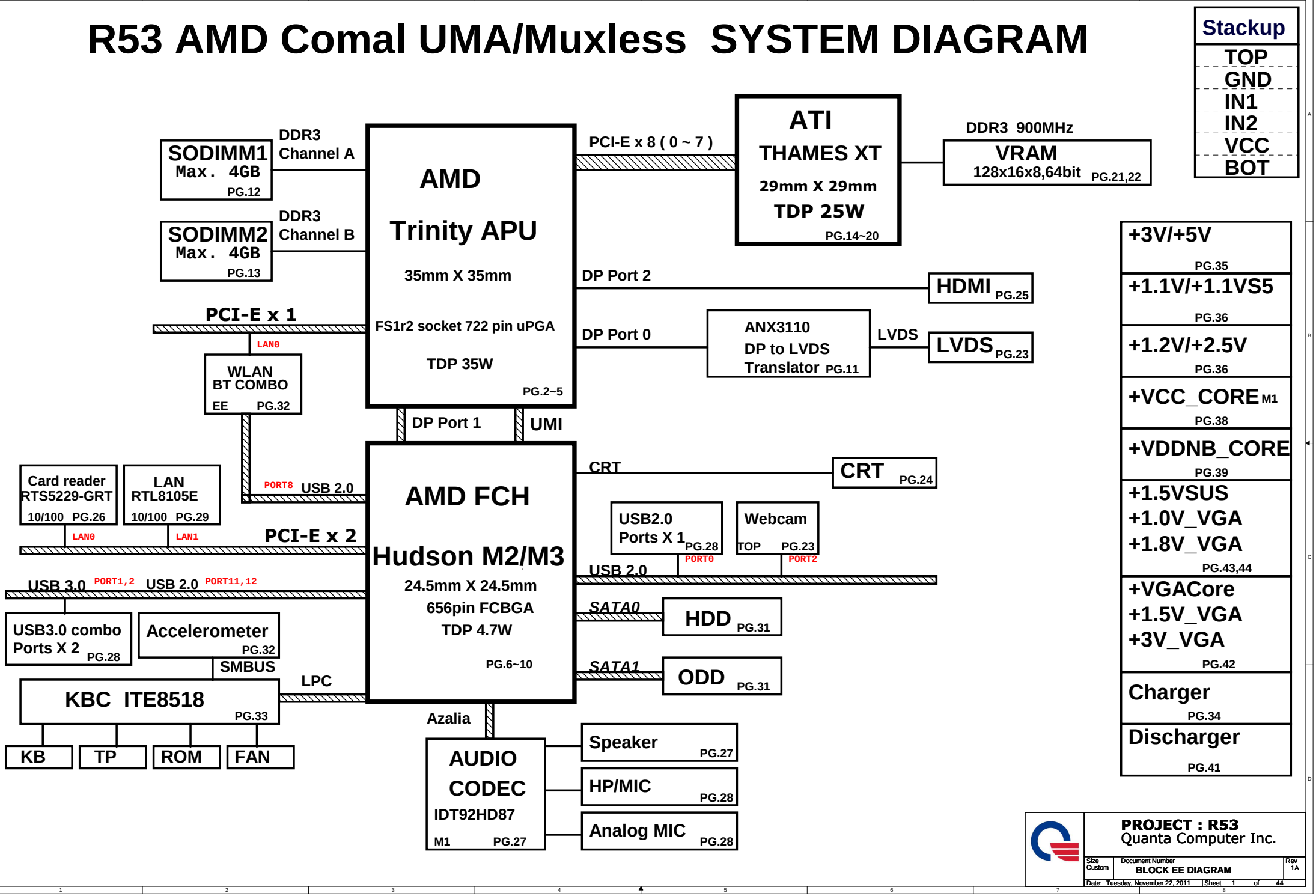
R53 AMD Comal UMA/Muxless SYSTEM DIAGRAM



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK EE DIAGRAM	1A

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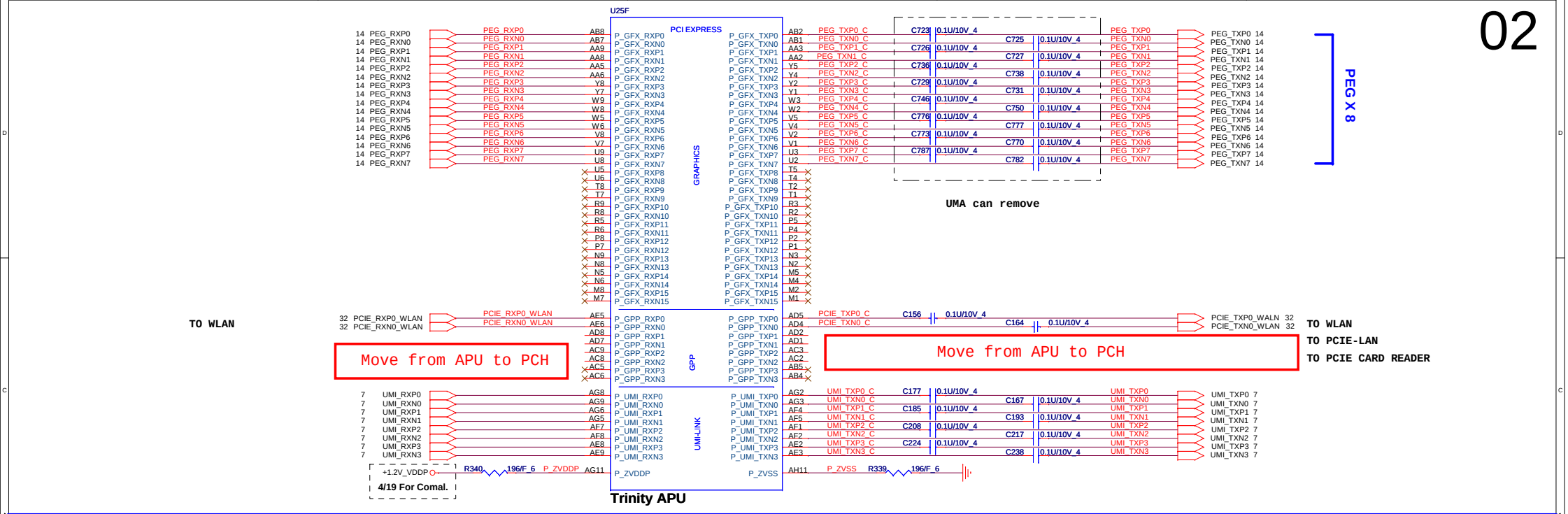
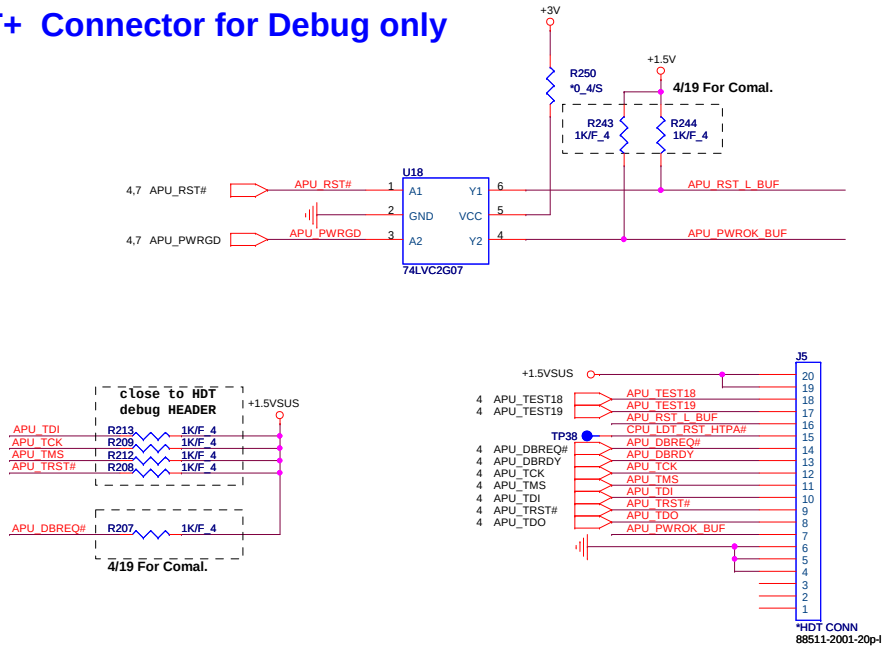


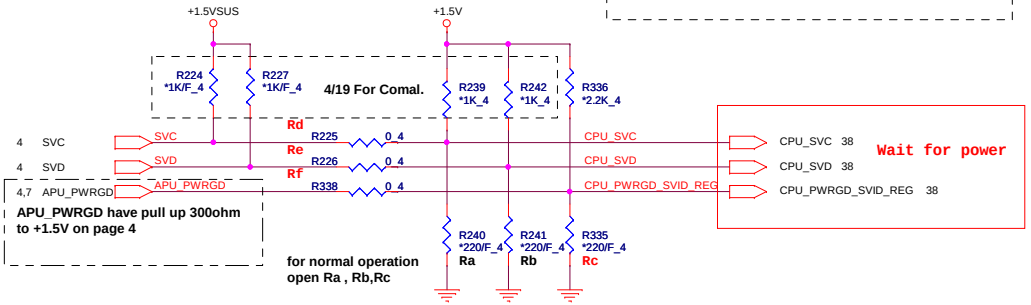
HDT+ Connector for Debug only



VID Override Circuit

	BOOT VOLTAGE		
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

Note:
To override VID,Remove Rd, Re, Rf, install Rc
set VID via SVC & SVD option RES.



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Llano PCIE/UMI/GPP	1A
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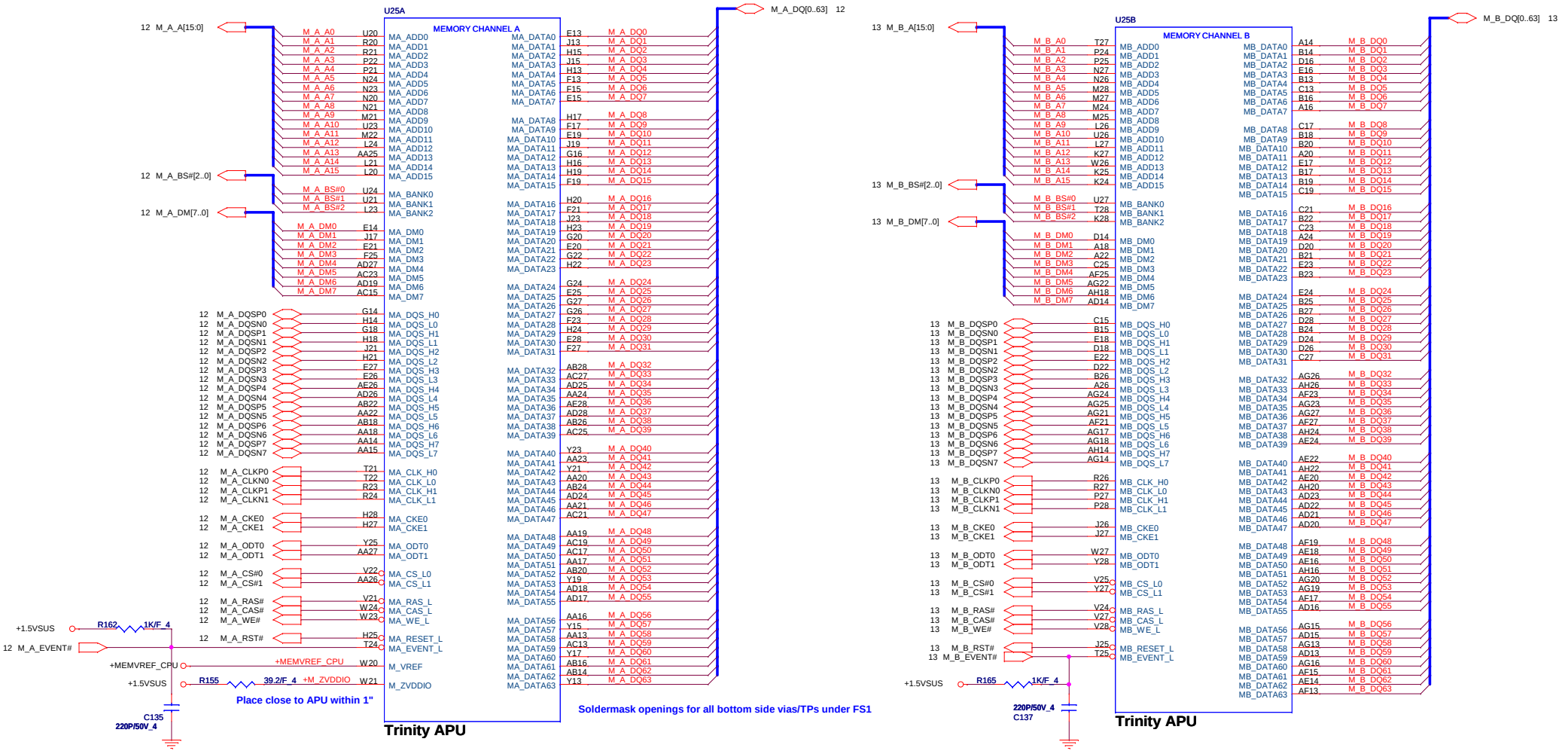

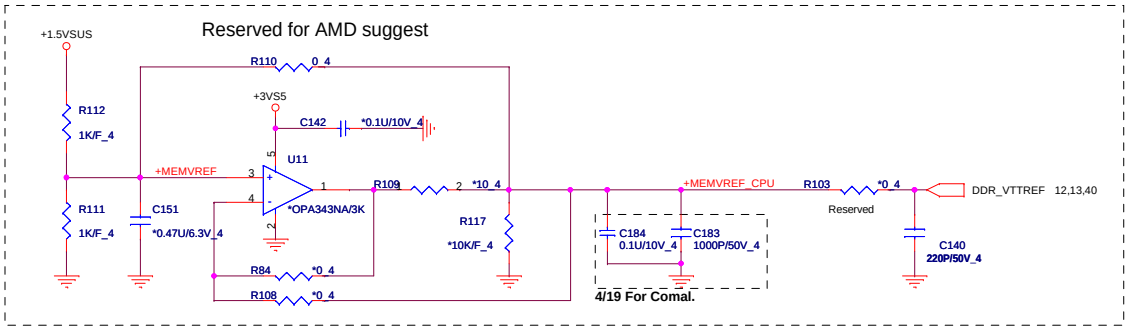

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Llano DDR3 MEM I/F	1A
Date: Monday, November 14, 2011	Sheet 3 of 44	

Place caps with APU < 1 inch
route PCIE as 85ohm +/- 10%

DP0 output to
eDP to LVDS converter

Display port power 1.5V min 1.2v max : 1.65v

DP1 output to Hudson-M2
for VGA translator interface

4/19 HDMI change to DP2 for Comal.

DP2 output to
HDMI connector

note --HDMI P&N can not swap

Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal,
close to APU.

Trinity APU

LVDS

VGA

HDMI

Display port power 1.5V min 1.2v max : 1.65v

SI,AMD no concern
so remove TP10,
TP17,TP18,TP16,TP23

To AMD HDT

M_TEST CONNECTION TBD

7/8 For Comal.

TEST35 PU FOR INTERNAL
TEST35 PD FOR CUSTOMER

DMAACTIVE_L controls
entry and exit from the
sleep and power states

AMD internal test only

FS1R1 signals is for detect CPU TYPE and protect it.
FS1R1 CPU this pin is N.C
FS1R2 CPU this pin is LOW
can remove it at MP

4/19 For Comal.

SI , PU SUS power
meet AMD design

Add R49 for verify this solution

APU_PROCHOT# 可以當 input or output
當Low 時CPU 會降 P - STATE

to EC reserve only

reserve for leakage current verify

Thermal

THERMTRIP# shutdown temperature 125度C

ADD VGA TEMP_ FAIL function is active Hi

over 120 degree C= Low

When 100K-NTC 100 C=6.164K
Thermal Trip = 120 C

PROJECT : R53
Quanta Computer Inc.
R23

Size	Document Number	Rev
	Llano Display/Misc	1A
Monday, November 14, 2011	Sheet	of

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

SI , change to 22u for improve +VDDNB_CORE transient

4/19 For Comal.

+VDDNB_CORE

C821 22U/6.3VS_8 C818 22U/6.3VS_8 C452 22U/6.3VS_8

C408 0.22U/10V_4 C465 0.22U/10V_4 C466 180P/50V_4 C468 180P/50V_4 C467 180P/50V_4

4/19 For Comal.

+VDDNB_CAP

C346 22U/6.3VS_8 C380 22U/6.3VS_8 C397 180P/50V_4

SI , change to 22u for AMD ACE dynamic test,

36A

Maximum IDDspike 50A

+VCC_CORE

U25D

VDD_1 F8, VDD_2 H6, VDD_3 J1, VDD_4 J14, VDD_5 P6, VDD_6 P10, VDD_7 J16, VDD_8 J18, VDD_9 J9, VDD_10 K19, VDD_11 K3, VDD_12 K17, VDD_13 M3, VDD_14 K6, VDD_15 V10, VDD_16 V18, VDD_17 V3, VDD_18 F3, VDD_19 L18, VDD_20 V6, VDD_21 W1, VDD_22 T18, VDD_23 Y14, VDD_24 AA1, VDD_25 AB6, VDD_26 AC1, VDD_27 R1, VDD_28 P3, VDD_29 K10, VDD_30 H3, VDD_31 M19

VDD_33 R11, VDD_34 T10, VDD_35 H8, VDD_36 G1, VDD_37 U11, VDD_38 W11, VDD_39 W13, VDD_40 W15, VDD_41 W17, VDD_42 W19, VDD_43 AB3, VDD_44 AD3, VDD_45 AD6, VDD_46 AE1, VDD_47 L1, VDD_48 Y6, VDD_49 M6, VDD_50 N11, VDD_51 N1, VDD_52 T3, VDD_53 T6, VDD_54 U19, VDD_55 U1, VDD_56 Y16, VDD_57 Y18, VDD_58 Y3, VDD_59 D4, VDD_60 F4, VDD_61 AF6, VDD_62 AF3, VDD_63 L11

C229 22U/6.3V_8 C271 22U/6.3V_8 C250 22U/6.3V_8 C669 22U/6.3V_8 C260 22U/6.3V_8

C286 22U/6.3V_8 C715 22U/6.3V_8 C267 22U/6.3V_8 C266 22U/6.3V_8 C259 22U/6.3V_8

4/19 For Comal.

C307 0.22U/10V_4 C306 0.22U/10V_4 C234 180P/50V_4 C239 180P/50V_4 C293 0.01U/25V_4 C304 0.01U/25V_4 C290 0.01U/25V_4

25A

Maximum IDDNBspike 33A

+VDDNB_CORE

VDDNB_1 C8, VDDNB_2 D10, VDDNB_3 B8, VDDNB_4 B12, VDDNB_5 C9, VDDNB_6 A9, VDDNB_7 A10, VDDNB_8 A8, VDDNB_9 A11, VDDNB_10 E10, VDDNB_11 E11, VDDNB_12 C10

VDDNB_13 C11, VDDNB_14 C12, VDDNB_15 D9, VDDNB_16 D8, VDDNB_17 D12, VDDNB_18 D11, VDDNB_19 B11, VDDNB_20 A12, VDDNB_21 B10, VDDNB_22 E12, VDDNB_23 B9

+VDDNB_CAP

VDDNB_CAP K13, VDDNB_CAP K12

DECOUPLING between PROCESSOR and DIMMs Across VDDIO and VSS split

+1.5VSUS

C207 0.22U/10V_4 C194 0.22U/10V_4 C195 180P/50V_4 C275 180P/50V_4

2.8A Up to DDR3-1333 @ 1.50V VDDIO

+1.5VSUS

C242 0.22U/10V_4 C349 0.22U/10V_4 C255 0.22U/10V_4 C400 0.22U/10V_4 C285 0.22U/10V_4 C338 0.22U/10V_4

4/19 For Comal.

C190 180P/50V_4

VDDIO_1 H26, VDDIO_2 K20, VDDIO_3 J28, VDDIO_4 K23, VDDIO_5 K26, VDDIO_6 L22, VDDIO_7 L25, VDDIO_8 L28, VDDIO_9 M20, VDDIO_10 M23, VDDIO_11 M26, VDDIO_12 N22, VDDIO_13 N25, VDDIO_14 N28, VDDIO_15 P20, VDDIO_16 P23, VDDIO_17 P26, VDDIO_18 AA28

VDDIO_19 T23, VDDIO_20 T26, VDDIO_21 U22, VDDIO_22 U25, VDDIO_23 U28, VDDIO_24 Y26, VDDIO_25 T20, VDDIO_26 R28, VDDIO_27 R25, VDDIO_28 R22, VDDIO_29 V20, VDDIO_30 V23, VDDIO_31 V26, VDDIO_32 W22, VDDIO_33 W25, VDDIO_34 W28, VDDIO_35 Y24, VDDIO_36 G28

+1.5VSUS

4/19 For Comal.

C399 22U/6.3VS_8 C192 22U/6.3VS_8 C403 22U/6.3VS_8 C402 22U/6.3VS_8 C323 4.7U/6.3V_6 C310 4.7U/6.3V_6 C210 4.7U/6.3V_6 C398 4.7U/6.3V_6

If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

+1.2V_VDDP

VDDP = 5A

+1.2V R334 *0_8/S +1.2V_VDDP

4/19 For Comal.

C707 22U/6.3VS_8 C674 10U/6.3V_8 C689 10U/6.3V_8 C679 10U/6.3V_8

C683 0.22U/6.3V_4 C684 0.22U/6.3V_4 C682 180P/50V_4 C685 180P/50V_4

VDDP AH6, VDDP AH5, VDDP AH4, VDDP AH3, VDDP AH7

VDDA AB10

VDDR = 3.3A (Up to DDR3-1333 @ 1.5V)

+1.2V

+1.2V_VDDR_B R333 *0_8/S

C673 10U/6.3V_8 C671 10U/6.3V_8 C676 10U/6.3V_8

C680 0.22U/6.3V_4 C203 0.22U/10V_4 C675 1000P/50V_4 C678 180P/50V_4 C681 180P/50V_4

VDDR AG10, VDDR AH8, VDDR AH9, VDDR AH10

VDDA= 0.75A

+2.5V L17 PBY160808T-221Y-N(220,2A) +2.5V_VDDA

C204 4.7U/6.3V_6 C216 0.22U/10V_4 C226 3300P/50V_4

Trinity APU

EMI suggestion

+VCC_CORE

C96 470P/50V_4 C98 *470P/50V_4 C97 *470P/50V_4

U25E

VSS_1 J20, VSS_2 L4, VSS_3 R7, VSS_4 W18, VSS_5 A15, VSS_6 AB17, VSS_7 AC22, VSS_8 AE21, VSS_9 AF24, VSS_10 AH23, VSS_11 AH25, VSS_12 R7, VSS_13 C14, VSS_14 C16, VSS_15 C2, VSS_16 C20, VSS_17 C22, VSS_18 C24, VSS_19 C26, VSS_20 C28, VSS_21 D13, VSS_22 D15, VSS_23 D17, VSS_24 D19, VSS_25 D23, VSS_26 D25, VSS_27 D27, VSS_28 E4, VSS_29 F9, VSS_30 F14, VSS_31 F16, VSS_32 F18, VSS_33 F20, VSS_34 F22, VSS_35 F26, VSS_36 F28, VSS_37 G13, VSS_38 G15, VSS_39 G17, VSS_40 G19, VSS_41 G21, VSS_42 G23, VSS_43 G25, VSS_44 G4, VSS_45 J22, VSS_46 J24, VSS_47 J4, VSS_48 J7, VSS_49 K11, VSS_50 K14, VSS_51 K9, VSS_52 AC11, VSS_53 L19, VSS_54 L7, VSS_55 M11, VSS_56 AF11, VSS_57 V19, VSS_58 V9, VSS_59 W16, VSS_60 W4, VSS_61 W7, VSS_62 Y11, VSS_63 Y20, VSS_64 Y22, VSS_65 Y9, VSS_66 A17, VSS_67 A13, VSS_68 K16, VSS_69 F24, VSS_70 G8, VSS_71 H7, VSS_72 J8

VSS_75 A19, VSS_76 A21, VSS_77 A23, VSS_78 A25, VSS_79 A7, VSS_80 AA4, VSS_81 AA7, VSS_82 AB13, VSS_83 AB15, VSS_84 AB19, VSS_85 AB21, VSS_86 AB23, VSS_87 AB25, VSS_88 AB27, VSS_89 AB9, VSS_90 AC14, VSS_91 AC16, VSS_92 AC18, VSS_93 AC20, VSS_94 AC24, VSS_95 AC26, VSS_96 AC28, VSS_97 AC4, VSS_98 AC7, VSS_99 AD9, VSS_100 AE13, VSS_101 AE15, VSS_102 AE17, VSS_103 M9, VSS_104 N10, VSS_105 N4, VSS_106 N7, VSS_107 R10, VSS_108 R4, VSS_109 T11, VSS_110 T9, VSS_111 U10, VSS_112 U18, VSS_113 U4, VSS_114 U7, VSS_115 V11, VSS_116 AE19, VSS_117 AE23, VSS_118 AE25, VSS_119 AE27, VSS_120 AE4, VSS_121 AE7, VSS_122 AF14, VSS_123 AF16, VSS_124 AF18, VSS_125 AF20, VSS_126 AF22, VSS_127 AF26, VSS_128 AF28, VSS_129 AF9, VSS_130 AG4, VSS_131 AG7, VSS_132 AH13, VSS_133 AH15, VSS_134 AH17, VSS_135 AH19, VSS_136 AH21, VSS_137 P9, VSS_138 C18, VSS_139 D21, VSS_140 W14, VSS_141 P11, VSS_142 C7, VSS_143 E8, VSS_144 K18, VSS_145 W12

Trinity APU

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Llano POWER/GND	1A

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NC,no install by default

R462 *2.2K_4 FCH_TEST0
R463 *2.2K_4 FCH_TEST1
R469 *2.2K_4 FCH_TEST2

+3V
R295 2.2K_4 CGCLK_SMB
R287 2.2K_4 CGDAT_SMB
to DDR3 SMBUS
SI2 , change power rail from +3V to +3VS5
+3VS5
R468 *1K_4
J6 1 2 SYS_RST#
*SOLDERJUMPER-2
SYS_RST# internal 10K pull up

GEVENT0# internal pull Hi 8.2K to +3V
GEVENT1# internal pull Hi 8.2K to +3V
GEVENT23# internal pull Hi 8.2K to +3V
GEVENT5# internal pull Hi 8.2K to +3VS5
PCIE_WAKE# no need to pull
Hi resistor from check list

CLK_REQ2# internal pull Hi 8.2K to +3V
CLK_REQ3# internal pull Hi 8.2K to +3V
CLK_REQ4# internal pull Hi 8.2K to +3V

+3VS5
R301 10K/F_4 SCL3
R298 10K/F_4 SDA3
R290 2.2K_4 SCL2
R296 2.2K_4 SDA2
R464 2.2K_4 SCL1
R465 2.2K_4 SDA1
R284 *4.7K_4 FCH_THERMTRIP#
C582 *0.01U/25V_4
R272 10K/F_4 DNBSWON#

SI2 , HP request Image sensor SMBUS reserve to FCH

This pin is used to power down VGA DAC regulators when CRT no connected

GEVENT16# internal pull Hi 8.2K to +3VS5
GEVENT15# internal pull Hi 8.2K to +3VS5

To Azalia

ACZ_SDOUT_R R454 33_4 ACZ_SDOUT_AUDIO 27
ACZ_SYNC_R R481 33_4 ACZ_SYNC_AUDIO 27
ACZ_BCLK_R R450 33_4 BIT_CLK_AUDIO 27
ACZ_RST#_R R479 33_4 ACZ_RST#_AUDIO 27
ACZ_SDIN0 ACZ_SDIN0 27

Pure UMA can remove
CLK_REQ# already internal pull up 8.2K
44 VGA_REQ 1 2 CLKREQ1#
D10 RB501V-40

remove PCIE_RST2# from AMD recommend

TP45 TP98 PCIE_RST2# RI#
33 SUSB# SUSC#
33 SUSC#
33 DNBSWON#
10 FCH_PWRGD
SUSB# SUSC# DNBSWON# FCH_PWRGD

4/19 For Comal.
TP51 FCH_TEST0 FCH_TEST1 FCH_TEST2
33 EC_A20GATE
33 EC_RCIN#
EC_A20GATE EC_RCIN#
TP50 FCH_PME#
33 SIO_EXT_SMI#
33 SIO_EXT_SCI#
SIO_EXT_SMI# SYS_RST#
R447 *0_4/S GEVENT5#
29,32 PCIE_WAKE# PCIE_WAKE#
C879 *100P/50V_4
4 FCH_THERMTRIP#
FCH_THERMTRIP#
R286 10K/F_4 WD_PWRGD
33 RSMRST# RSMRST#
26 PCIE_CARD_CLKREQ#
29 PCIE_LAN_CLKREQ#
PCIE_CARD_CLKREQ# PCIE_LAN_CLKREQ#

27 ACZ_SPKR
12,13 CGCLK_SMB
12,13 CGDAT_SMB
30 SCL1
30 SDA1
32 PCIE_MINI_CLKREQ#
R505 *0_4/S FCH_GPIO66
CGCLK_SMB CGDAT_SMB SCL1 SDA1 PCIE_MINI_CLKREQ#
CLKREQ1#

LLB# Not Implemented ,left unconnected.
TP94 LLB#
TP64 SMARTVOLT2
9 VGA_POWER_DOWN
R283 0_4 VGA_PD
TP49 GBE_LED0
Remove Card EECS function form Vendor mail
SI
TP63

TP93 TP97 ODD_PLUGIN#
31 ODD_PLUGIN#
31 ODD_DA#_FCH
ODD_DA#_FCH
4/19 For Comal.
TP48 TP99 FCH_JTAG_TCK
TP95 FCH_JTAG_TDI
TP46 FCH_JTAG_RST#
For Zero ODD

HD audio interface is +3V_S5 voltage
R484 *10K/F_4 ACZ_BCLK_R
R476 *10K/F_4 ACZ_SDOUT_R
R467 *10K/F_4 ACZ_SDIN0
R470 *10K/F_4 ACZ_SDIN1
R466 *10K/F_4 ACZ_SDIN2_R
ACZ_SDIN3_R
ACZ_SYNC_R
ACZ_RST#_R

TP60 TP59
32 BT_COMBO_OFF# BT_COMBO_OFF#
14 VGA_RSTB VGA_RSTB
33 VGA_ON_SB VGA_ON_SB

U34A
HUDSON-M3
Part 4 of 5
Hudson-M2-A13

PCIE_RST2#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
PME#/GEVENT3#
LPC_SMI#/GEVENT23#
LPC_PD#/GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
WD_PWRGD
RSMRST#
ACPI / WAKE UP EVENTS

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#/VGA_PD
GBE_LED0/GPIO183
SPI_HOLD#/GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#
GPIO

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#
USB OC

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
HD AUDIO

PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192

KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/XDB0/GPIO223
KSO_15/XDB1/GPIO224
KSO_16/XDB2/GPIO225
KSO_17/XDB3/GPIO226
EMBEDDED CTRL

USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB MISC
USB 1.1

USB_HSD13P USB_HSD13N
USB_HSD12P USB_HSD12N
USB_HSD11P USB_HSD11N
USB_HSD10P USB_HSD10N
USB_HSD9P USB_HSD9N
USB_HSD8P USB_HSD8N
USB_HSD7P USB_HSD7N
USB_HSD6P USB_HSD6N
USB_HSD5P USB_HSD5N
USB_HSD4P USB_HSD4N
USB_HSD3P USB_HSD3N
USB_HSD2P USB_HSD2N
USB_HSD1P USB_HSD1N
USB_HSD0P USB_HSD0N
USB 2.0

USBSS_CALRP
USBSS_CALRN
USB_SS_TX3P USB_SS_TX3N
USB_SS_RX3P USB_SS_RX3N
USB_SS_TX2P USB_SS_TX2N
USB_SS_RX2P USB_SS_RX2N
USB_SS_TX1P USB_SS_TX1N
USB_SS_RX1P USB_SS_RX1N
USB_SS_TX0P USB_SS_TX0N
USB_SS_RX0P USB_SS_RX0N
USB 3.0

SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208

USB_RCOMP_SB R494 11.8K/F_6
USBP6+ USBP6- → USBP12+ 28, USBP12- 28 — Left side USB Combo 3.0/2.0.
USBP5+ USBP5- → USBP11+ 28, USBP11- 28 — Left side USB Combo 3.0/2.0.
USBP8+ 32, USBP8- 32 — WLAN Min-Card
USBP7+ USBP7- → TP104 TP101
USBP2+ 23, USBP2- 23 — Camera USB
USBP0+ 28, USBP0- 28 — Right side USB 2.0 Connector
R496 1K/F_4, R495 1K/F_4 +FCH_VDD_11_SSUSB_S
USB 3.0 Not Implemented: left unconnected.
USBP3+ USBP3- → USB30_TX2+ 28, USB30_TX2- 28
USB30_RX2+ 28, USB30_RX2- 28
USB30_TX1+ 28, USB30_TX1- 28
USB30_RX1+ 28, USB30_RX1- 28
EC_PWM2 → EC_PWM2 10
No need for GPIO200

SCL3 of a TSI-capable APU's thermal bus,Pulled up to APU_VDDIO. Resistor value verified in the relevant APU design guide.

PROJECT : R53
Quanta Computer Inc.
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HUDSON-M3

Part 1 of 5

U34E

Place these PICE AC coupling cap close to FCH

SI , PCIE port change from port 2 to port 0

SI , change to 22Ω & 47Ω for Rise/Fall time issue

Pure UMA can remove

Note: CLK_FCH_SRCP/N is 100MHZ SSC

Note: CLK_PCIE_TRAVISP/N is 100MHZ non-SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_PCIE_VGAP/N is 100MHZ SSC

Note: GPP_CLK(0:8)P/N is 100MHZ SSC capable

SI , AMD request test point

Add G-sensor signal

SI2 , change R497 value from 220 ohm to 120 ohm

SI , change for EMI

FCH PROCHOT#--- (input 0.8V threshold) When it isasserted, it can generate SCI or SMI to OS/BIOS

PV change to short-pad

LDT_STP# let is NC from schematic recommend

S5_CORE_EN is necessary to connect enable pin of +3VPCU/+5VPCU regulator for S5+ mode implementation

INTRUDER_ALERT# Left not connected (FCH has 50-kohm internal pull-up to VBAT).

USE GROUND GUARD FOR 32K_X1 AND 32K_X2

Hudson-M2-A13

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U34D

HUDSON-M3

Part 5 of 5

GROUND

VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58 VSS_59 VSS_60 VSS_61 VSS_62 VSS_63 VSS_64

VSS_65 VSS_66 VSS_67 VSS_68 VSS_69 VSS_70 VSS_71 VSS_72 VSS_73 VSS_74 VSS_75 VSS_76 VSS_77 VSS_78 VSS_79 VSS_80 VSS_81 VSS_82 VSS_83 VSS_84 VSS_85 VSS_86 VSS_87 VSS_88 VSS_89 VSS_90 VSS_91 VSS_92 VSS_93 VSS_94 VSS_95 VSS_96 VSS_97 VSS_98 VSS_99 VSS_100 VSS_101 VSS_102 VSS_103 VSS_104 VSS_105 VSS_106 VSS_107 VSS_108 VSS_109 VSS_110 VSS_111 VSS_112 VSS_113 VSS_114 VSS_115 VSS_116 VSS_117 VSS_118 VSS_119 VSS_120 VSS_121 VSS_122 VSS_123 VSS_124 VSS_125 VSS_126 VSS_127 VSS_128

VSSAN_HWM VSSXL VSSPL_SYS

VSSPL_DAC VSSAN_DAC VSSANQ_DAC VSSIO_DAC EFUSE

Hudson-M2-A13

PLACE SATA AC COUPLING CAPS CLOSE TO HUDSON-M2/M3

SATA HDD

SATA ODD

SATA_TXP0 SATA_TXN0 SATA_RXN0 SATA_RXP0 SATA_TXP1 SATA_TXN1 SATA_RXN1 SATA_RXP1

U23 *MC74VHC1G08DFT2G

C577 *0.1U/10V_4

SATA_LED# SB_SATA_LED# R288 0_4

PLACE SATA_CAL RES VERY CLOSE TO BALL OF HUDSON-M2/M3

R313 1K/F_4 R303 931/F_4 SATA_CALRP SATA_CALRN +1.1V_AVDD_SATA

4/19 For Comal.

R294 *220/F_6 SB_SATA_LED# +3V

SATA_ACT#/GPIO67 SATA_X1 SATA_X2

Integrated Clock Mode: Leave unconnected.

Add GPIO for G-sensor LED control

GPIO52 internal pull Hi 8.2K to +3V
GPIO53 internal pull Hi 8.2K to +3V
GPIO54 internal pull Hi 8.2K to +3V
GPIO56 internal pull Hi 8.2K to +3V
GPIO57 internal pull Hi 8.2K to +3V
GPIO58 internal pull Hi 8.2K to +3V

RF_OFF# BT_OFF# BT_COMBO_EN# ODD_PWR LCD_BK TP102

FANOUT0/GPIO52 FANOUT1/GPIO53 FANOUT2/GPIO54 FANIN0/GPIO56 FANIN1/GPIO57 FANIN2/GPIO58

TEMPIN0 TEMPIN1 TEMPIN2 TEMPIN3

TEMPIN0/GPIO171 TEMPIN1/GPIO172 TEMPIN2/GPIO173 TEMPIN3/TALERT#/GPIO174

R281 10K/F_4 R276 10K/F_4 R485 10K/F_4 R277 10K/F_4

TEMP(0 - 3)
Temp Monitor Not Implemented
10-KΩ 5% pull-up to +3VS5
or 10-KΩ 5% pull-down

U34B

HUDSON-M3

Part 2 of 5

SATA_TX0P SATA_TX0N SATA_RX0N SATA_RX0P SATA_TX1P SATA_TX1N SATA_RX1N SATA_RX1P SATA_TX2P SATA_TX2N SATA_RX2N SATA_RX2P SATA_TX3P SATA_TX3N SATA_RX3N SATA_RX3P SATA_TX4P SATA_TX4N SATA_RX4N SATA_RX4P SATA_TX5P SATA_TX5N SATA_RX5N SATA_RX5P

NC6 NC7 NC8 NC9 NC10 NC11 NC12 NC13

SERIAL ATA

HW MONITOR

SD CARD

SD_CLK/SCLK_2/GPIO73 SD_CMD/SLOAD_2/GPIO74 SD_CD#/GPIO75 SD_WP/GPIO76 SD_DATA0/SDATI_2/GPIO77 SD_DATA1/SDATO_2/GPIO78 SD_DATA2/GPIO79 SD_DATA3/GPIO80

GBE LAN

GBE_COL GBE_CRS GBE_MDCK GBE_MDIO GBE_RXCLK GBE_RXD3 GBE_RXD2 GBE_RXD1 GBE_RXD0 GBE_RXCTL/RXDV GBE_RXERR GBE_TXCLK GBE_TXD3 GBE_TXD2 GBE_TXD1 GBE_TXD0 GBE_TXCTL/TXEN GBE_PHY_PD GBE_PHY_RST# GBE_PHY_INTR

GBE_COL R280 *10K/F_4 GBE_CRS R451 *10K/F_4 GBE_MDIO R456 *10K/F_4 +3VS5

6/7 for Comal.

GBE_RXERR R452 *10K/F_4

ICT need TP2675 size test point

GBE_PHY_INTR R455 10K/F_4 +3VS5

SPI ROM

SPI_DI/GPIO164 SPI_DO/GPIO163 SPI_CLK/GPIO162 SPI_CS1#/GPIO165 ROM_RST#/SPI_WP#/GPIO161

SPI_SI SPI_SO SPI_CLK SPI_CS0# FCH_SPI_WP

TP47 TP40 TP41 TP43 TP39

EC_BIOS_CS# EC_BIOS_SPI_CLK_I EC_BIOS_WR# EC_BIOS_RD# SPI_WP

VGA DAC

VGA_RED VGA_GREEN VGA_BLUE VGA_HSYNC/GPO68 VGA_VSYNC/GPO69 VGA_DDC_SDA/GPO70 VGA_DDC_SCL/GPO71 VGA_DAC_RSET AUX_VGA_CH_P AUX_VGA_CH_N AUXCAL

L30 FCH_CRT_R R503 *0_4/S FCH_CRT_RED 24

L32 FCH_CRT_G R510 *0_4/S FCH_CRT_GRE 24

M29 FCH_CRT_B R509 *0_4/S FCH_CRT_BLU 24

M28 FCH_CRT_HSYNC 24
N30 FCH_CRT_VSYNC 24

M33 FCH_DDCDAT 24
N32 FCH_DDCCLK 24

K31 VGA_DAC_REST R314 715/F_4

V28 APU_DP_AUXP 4
V29 APU_DP_AUXN 4

U28 AUXCAL R317 100/F_4 +FCH_VDDAN_11_MLDAC

VGA MAINLINK

ML_VGA_L0P ML_VGA_L0N ML_VGA_L1P ML_VGA_L1N ML_VGA_L2P ML_VGA_L2N ML_VGA_L3P ML_VGA_L3N ML_VGA_HPD/GPIO229

T31 APU_DP_TXP0 4
T33 APU_DP_TXN0 4
T29 APU_DP_TXP1 4
T28 APU_DP_TXN1 4
R32 APU_DP_TXP2 4
R30 APU_DP_TXN2 4
P29 APU_DP_TXP3 4
P28 APU_DP_TXN3 4

C29 VGA_HPD R311 *10K/F_4 +FCH_VDDAN_33_DAC_R

VIN0/GPIO175 VIN1/GPIO176 VIN2/SDATI_1/GPIO177 VIN3/SDATO_1/GPIO178 VIN4/SLOAD_1/GPIO179 VIN5/SCLK_1/GPIO180 VIN6/GBE_STAT3/GPIO181 VIN7/GBE_LED3/GPIO182

N2 SIDE_PORT_ID0
M3 SIDE_PORT_ID1
L2 SIDE_PORT_ID2
N4 BOARD_ID0
P1 BOARD_ID1
P3 BOARD_ID2
M1 BOARD_ID3
M5 BOARD_ID4

NC1 NC2 NC3 NC4 NC5

VIN(0 - 7)
Voltage Monitor Not Implemented
10-KΩ 5% pull-up to +3VS5
or 10-KΩ 5% pull-down

Hudson-M2-A13

Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023

FCH SPI ROM

SPI_CLK C880 *22P/50V_4 EMI

SI , change power rail from +3V to +3VS5

R486 10K/F_4 C881 *0.1U/10V_4 R473 *10K/F_4

U33 *MX25L1605DM2I-12G

R487 0_4 SPI_CS0# R472 0_4 SPI_CLK R471 0_4 SPI_SO R489 0_4 SPI_SI R493 *0_4

*10K/F_4 R491 +3V

R place close to PCH

FCH_CRT_R R502 150/F_4
FCH_CRT_G R501 150/F_4
FCH_CRT_B R504 150/F_4

FCH_VGA_HPD R506 *0_4 VGA_HPD

Reserve for debug

VGA Hot-plug

SI , Q23,Q41 change to dual type MOS Q50

R508 1K/F_4 R500 100K/F_4

Q50B Q50A 2N7002DW-7-F Dual

VGA_HPD R309 100K/F_4

ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port

+3VS5 R444 10K/F_4 BOARD_ID0 R445 *10K/F_4
R442 *10K/F_4 BOARD_ID1 R443 10K/F_4
R449 *10K/F_4 BOARD_ID2 R448 10K/F_4
R440 *10K/F_4 BOARD_ID3 R460 10K/F_4
R438 *10K/F_4 BOARD_ID4 R439 10K/F_4
R446 10K/F_4 SIDE_PORT_ID0 R459 *10K/F_4
R441 10K/F_4 SIDE_PORT_ID1 R461 *10K/F_4
R437 *10K/F_4 SIDE_PORT_ID2 R457 10K/F_4

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Quanta Computer Inc.

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PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

SI, add for leakage issue

R539 0_8 Q46 *AO3416

+3V

+3.3V_VDDIO

VDDQ--3.3V I/O power 102mA

C589 0.1U/10V_4 C570 22U/6.3V5_8 C586 0.1U/10V_4 C581 0.1U/10V_4 C585 0.1U/10V_4

33,34,36,40,41 MAINON

M2 chipset need to connect to GND
M3 remove

+FCH_VDDAN_33_DAC_R

+FCH_VDDPL_33_MLDAC

+VDDPL_3.3V

47mA

+VDDPL_33_SYS 20mA

+VDDPL_33_DAC 20mA

30mA

R291 *0_4 +FCH_VDDPL_33_SSUSB_S 11mA

+FCH_VDDPL_33_SUSB_S 14mA

+FCH_VDDPL_33_PCIE 11mA

+FCH_VDDPL_33_SATA 12mA

L52 PBY160808T-221Y-N(220,2A) TRACE WIDTH >=15mil

C638 2.2U/6.3V_4 C639 *0.1U/10V_4

L54 PBY160808T-221Y-N(220,2A) TRACE WIDTH >=15mil

C641 2.2U/6.3V_4 C632 *0.1U/10V_4

NOTE : LDO_CAP
A11 stepping : C will install 1nf cap
A12 stepping : C will let it to NC

C635 *1000P/50V_4 +LDO_CAP

+FCH_VDDAN_11_MLDAC +FCH_VDDAN_11_DAC

VDDAN_11_ML -- UMI 1.1V analog power

+FCH_VDDAN_11_ML

7mA

226mA

C609 0.1U/10V_4 C617 1U/6.3V_4 C631 4.7U/6.3V_6 C613 0.1U/10V_4

VDDPL_33_USB_S : USB PHY PLL analog power

L53 PBY160808T-221Y-N(220,2A) +VDDPL_3.3V

C640 2.2U/6.3V_4 C615 0.1U/10V_4

+3V_AVDD_USB L67 PBY160808T-221Y-N(220,2A) +FCH_VDDPL_33_SUSB_S

C885 2.2U/6.3V_4 C886 1U/6.3V_4

VDDAN_33_USB_S : USB PHY I/O analog power

+3V_AVDD_USB TRACE WIDTH >=50mil 470mA

+3VS5 L68 PBY160808T-221Y-N(220,2A)

C574 0.1U/10V_4 C583 10U/6.3V_8 C887 10U/6.3V_8 C567 1U/6.3V_4 C575 1U/6.3V_4

VDDAN_11_USB_S : USB PHY PLL analog power

+1.1VS5 L70 PBY160808T-221Y-N(220,2A) +FCH_VDDAN_11_USB_S

C979 0.1U/10V_4

SI , AMD SR tool review need one more 0.1u

C572 2.2U/6.3V_4 140mA

C587 0.1U/10V_4 TRACE WIDTH >=20mil

VDDCR_11_USB_S : USB PHY core power

+1.1VS5 L69 PBY160808T-221Y-N(220,2A) +FCH_VDDCR_11_USB_S 42mA

TRACE WIDTH >=15mil

C573 0.1U/10V_4 C579 0.1U/10V_4 C888 10U/6.3V_8

SI , AMD SR tool review

M3 chipset need to stuff for support USB3.0

+FCH_VDD_11_SSUSB_S

+1.1VS5 L48 PBY160808T-221Y-N(220,2A) R293 *0_8/S +FCH_VDDAN_11_SSUSB_S_R 282mA

VDDAN_11_SSUSB_S : USB3.0 PHY PLL analog power

R289 *0_4 R300 *0_8/S +FCH_VDDCR_11_SSUSB_S 424mA

M2 chipset need to connect to GND M3 remove

C605 1U/6.3V_4 C607 0.1U/10V_4 C606 0.1U/10V_4 C604 1U/6.3V_4 C627 10U/6.3V_8 C630 1U/6.3V_4 C629 0.1U/10V_4 C628 0.1U/10V_4

VDDCR_11_SSUSB_S : USB3.0 PHY core power

M3 chipset need to stuff for support USB3.0

if support Modem wake up should be change pull hi to S5 power

+3VS5 +FCH_VDDPL_33_SSUSB_S

L50 PBY160808T-221Y-N(220,2A) M3 chipset need to stuff for support USB3.0

C633 2.2U/6.3V_6 C634 0.1U/10V_4

+3V +VDDIO_AZ

R477 *0_4/S

VDDIO_AZ_S -- HD Audio Interface I/O power

C563 2.2U/6.3V_4

U34C

HUDSON-M3 Part 3 of 5

PCI/GPIO I/O

AB17 VDDIO_33_PCIGP_1
AB18 VDDIO_33_PCIGP_2
AE9 VDDIO_33_PCIGP_3
AD10 VDDIO_33_PCIGP_4
AG7 VDDIO_33_PCIGP_5
AC13 VDDIO_33_PCIGP_6
AB12 VDDIO_33_PCIGP_7
AB13 VDDIO_33_PCIGP_8
AB14 VDDIO_33_PCIGP_9
AB16 VDDIO_33_PCIGP_10

CORE S0

T14 VDDCR_11_1
T17 VDDCR_11_2
T20 VDDCR_11_3
U16 VDDCR_11_4
U18 VDDCR_11_5
V14 VDDCR_11_6
V17 VDDCR_11_7
V20 VDDCR_11_8
Y17 VDDCR_11_9

H24 VDDPL_33_SYS
V22 VDDPL_33_DAC
U22 VDDPL_33_ML
T22 VDDAN_33_DAC
L18 VDDPL_33_SSUSB_S
D7 VDDPL_33_USB_S
AH29 VDDPL_33_PCIE
AG28 VDDPL_33_SATA

CLKGEN I/O

H26 VDDAN_11_CLK_1
J25 VDDAN_11_CLK_2
K24 VDDAN_11_CLK_3
L22 VDDAN_11_CLK_4
M22 VDDAN_11_CLK_5
N21 VDDAN_11_CLK_6
N22 VDDAN_11_CLK_7
P22 VDDAN_11_CLK_8

LDO_CAP M31

VDDPL_11_DAC V21

MAIN LINK EXPRESS

Y22 VDDAN_11_ML_1
Y23 VDDAN_11_ML_2
Y24 VDDAN_11_ML_3
Y25 VDDAN_11_ML_4

AB24 VDDAN_11_PCIE_1
Y21 VDDAN_11_PCIE_2
AE25 VDDAN_11_PCIE_3
AD24 VDDAN_11_PCIE_4
AB23 VDDAN_11_PCIE_5
AA22 VDDAN_11_PCIE_6
AE26 VDDAN_11_PCIE_7
AG27 VDDAN_11_PCIE_8

GBE LAN

AB10 VDDIO_33_GBE_S

AB11 VDDCR_11_GBE_S_1
AA11 VDDCR_11_GBE_S_2

AA9 VDDIO_GBE_S_1
AA10 VDDIO_GBE_S_2

SERIAL ATA

AA21 VDDAN_11_SATA_1
Y20 VDDAN_11_SATA_4
AB21 VDDAN_11_SATA_2
AB22 VDDAN_11_SATA_3
AC22 VDDAN_11_SATA_5
AC21 VDDAN_11_SATA_6
AA20 VDDAN_11_SATA_7
AA18 VDDAN_11_SATA_8
AB20 VDDAN_11_SATA_9
AC19 VDDAN_11_SATA_10

USB

G7 VDDAN_33_USB_S_1
H8 VDDAN_33_USB_S_2
J8 VDDAN_33_USB_S_3
K8 VDDAN_33_USB_S_4
K9 VDDAN_33_USB_S_5
M9 VDDAN_33_USB_S_6
M10 VDDAN_33_USB_S_7
N9 VDDAN_33_USB_S_8
N10 VDDAN_33_USB_S_9
M12 VDDAN_33_USB_S_10
N12 VDDAN_33_USB_S_11
M11 VDDAN_33_USB_S_12

U12 VDDAN_11_USB_S_1
U13 VDDAN_11_USB_S_2

T12 VDDCR_11_USB_S_1
T13 VDDCR_11_USB_S_2

3.3V_S5 I/O

N18 VDDIO_33_S_1
L19 VDDIO_33_S_2
M18 VDDIO_33_S_3
V12 VDDIO_33_S_4
V13 VDDIO_33_S_5
Y12 VDDIO_33_S_6
Y13 VDDIO_33_S_7
W11 VDDIO_33_S_8

G24 VDDXL_33_S

N20 VDDCR_11_S_1
M20 VDDCR_11_S_2

J24 VDDPL_11_SYS_S

M8 VDDAN_33_HWM_S

AA4 VDDIO_AZ_S

USB SS

P16 VDDAN_11_SSUSB_S_1
M14 VDDAN_11_SSUSB_S_2
N14 VDDAN_11_SSUSB_S_3
P13 VDDAN_11_SSUSB_S_4
P14 VDDAN_11_SSUSB_S_5

N16 VDDCR_11_SSUSB_S_1
N17 VDDCR_11_SSUSB_S_2
P17 VDDCR_11_SSUSB_S_3
M17 VDDCR_11_SSUSB_S_4

POWER

Hudson-M2-A13

1007mA for M3
902mA for M2

+1.1V_VDDCR VDDCR-- S/B CORE power

TRACE WIDTH >=100mil +1.1V

C588 0.1U/10V_4 C597 0.1U/10V_4 C598 1U/6.3V_4 C590 1U/6.3V_4 C591 10U/6.3V_8

+1.1V_CKVDD

340mA

VDDAN_11_CLK-- Internal clock Generator I/O power

TRACE WIDTH >=30mil

C626 1U/6.3V_4 C618 1U/6.3V_4 C622 0.1U/10V_4 C624 0.1U/10V_4 C916 22U/6.3VS_8

Reserve for VDDAN_11_CL leakage current issue

R514 0_8 Q42 *AO3416 L72 BLM18PG181SN1D(180,1.5A)_6 +1.1V

MAINON 33,34,36,40,41

+1.1V_PCIE_VDDR

1088mA

VDDAN_11_PCIE --PCIE/UMI analog power

TRACE WIDTH >=100mil

L56 BLM18PG181SN1D(180,1.5A)_6 +1.1V

C610 0.1U/10V_4 C620 0.1U/10V_4 C621 1U/6.3V_4 C623 1U/6.3V_4 C642 22U/6.3VS_8

+1.1VS5

VDDPL_11_SYS_S : System Clock Gen PLLs analog power

+VDDPL_1.1V L47 PBY160808T-221Y-N(220,2A)

C608 2.2U/6.3V_4 C614 0.1U/10V_4

+1.1V_AVDD_SATA

1337mA

VDDAN_11_SATA--SATA PHY analog/IO power

TRACE WIDTH >=50mil

L45 BLM18PG181SN1D(180,1.5A)_6 +1.1V

C596 1U/6.3V_4 C611 1U/6.3V_4 C599 0.1U/10V_4 C595 0.1U/10V_4 C600 22U/6.3VS_8

if support USB 3.0 wake up should be change pull hi to S5 power

VDDAN_33_HWM_S -- Hardware monitor interface I/O power

+VDDAN_3.3V_HWM

+3VS5 L66 PBY160808T-221Y-N(220,2A)

C878 2.2U/6.3V_4 C566 0.1U/10V_4

+VDDIO_3.3V

59mA

VDDIO_33_S-- 3.3v S5 I/O power

TRACE WIDTH >=20mil +3VS5

C593 *0.1U/10V_4 C576 2.2U/6.3V_4 C594 1U/6.3V_4 C584 1U/6.3V_4 C603 1U/6.3V_4 C580 1U/6.3V_4

if support USB 3.0 wake up should be change pull hi to S5 power

5mA

VDDXL_33_S-- 25MHZ XTAL IO power

+VDDXL_3.3V

VDDCR_1.1_S-- 1.1V S5 Core power

L49 PBY160808T-221Y-N(220,2A) +3VS5

C625 *0.1U/10V_4 C612 2.2U/6.3V_4

187mA

+VDDCR_1.1V +1.1VS5

TRACE WIDTH >=15mil

C601 1U/6.3V_4 C616 2.2U/6.3V_4

70mA

+VDDPL_1.1V

12mA

+VDDAN_3.3V_HWM

26mA

+VDDIO_AZ

Trace width >=20 mil

This circuit is for switch DAC and UMI analog power

32 mA Max

+3V Q25 AO3404 +FCH_VDDAN_33_DAC_R

+FCH_VDDAN_33_DAC L71 PBY160808T-221Y-N(220,2A)

C915 2.2U/6.3V_4 C914 0.1U/10V_4

+12VALW R315 330K_6 +FCH_VGA_PWR_EN

VGA will power down when CRT no insert

6 VGA_POWER_DOWN VGA_POWER_DOWN

Q24 ME2N7002E

VGA_PD is generated from FCH

R282 2.2K_4 C569 1U/6.3V_4 C637 0.022U/25V_4

+1.1V Q26 AO3404

+FCH_VDDAN_33_DAC_R +FCH_VDDPL_33_MLDAC

R511 *0_8/S

C901 2.2U/6.3V_4 C893 0.1U/10V_4

233 mA Max

+VDDAN_11_MLDAC L55 PBY160808T-221Y-N(220,2A) +FCH_VDDAN_11_MLDAC

SI2 , remove discharge circuit

SI , reserve for leakage issue

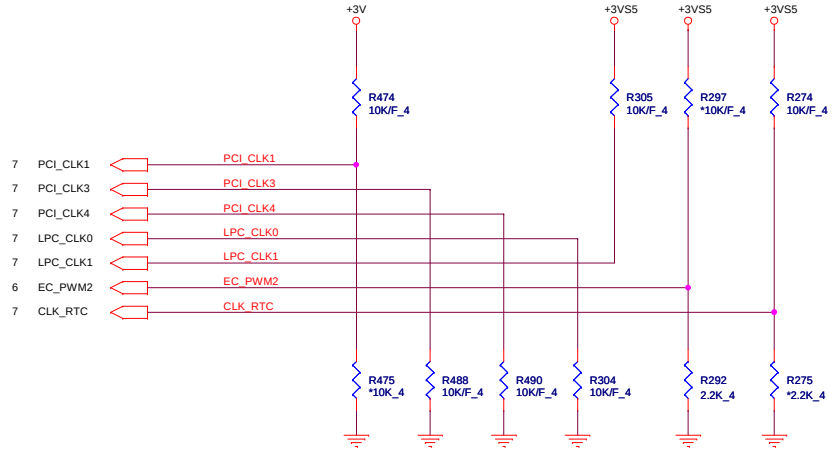
PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hudson-M3 POWER/GND	1A

Date: Friday, November 11, 2011 Sheet 9 of 44

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

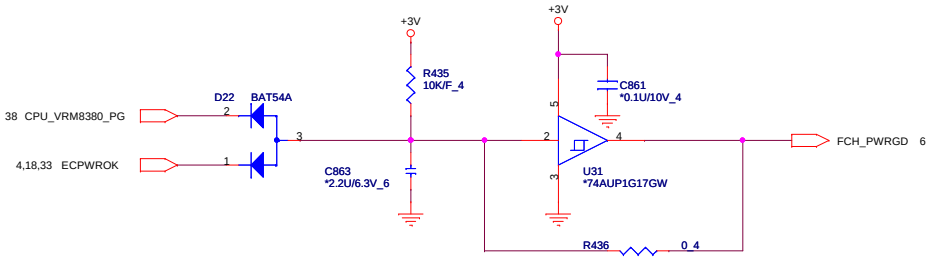
	--------	PCI_CLK1	--------	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE ENABLED
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE DISABLED DEFAULT

DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH PWRGD



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hudson-M3 STRAP/PWRGD	1A
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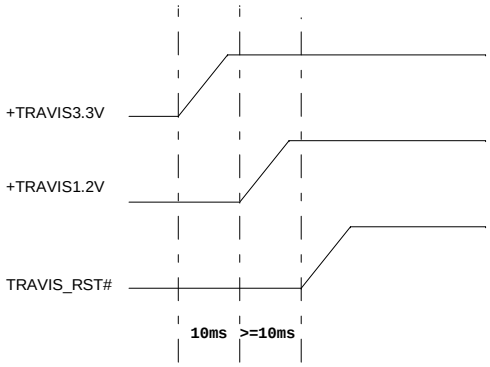
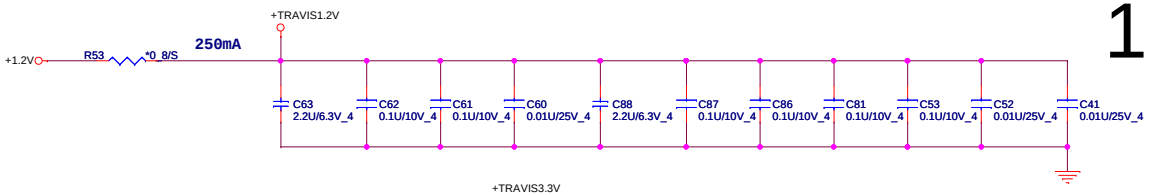
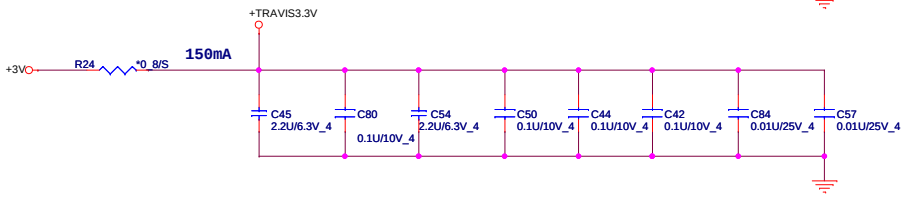
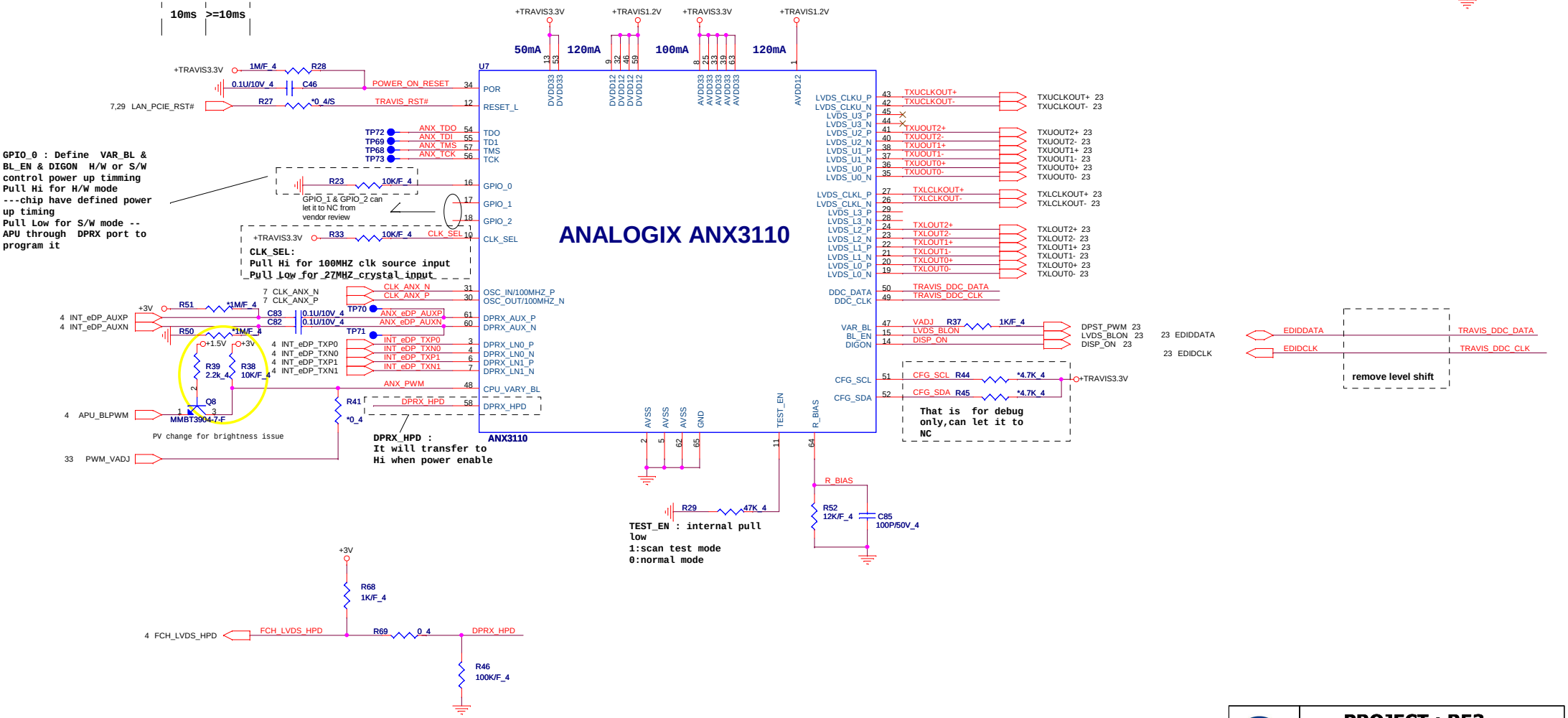
ANX3110 Power Up Sequence

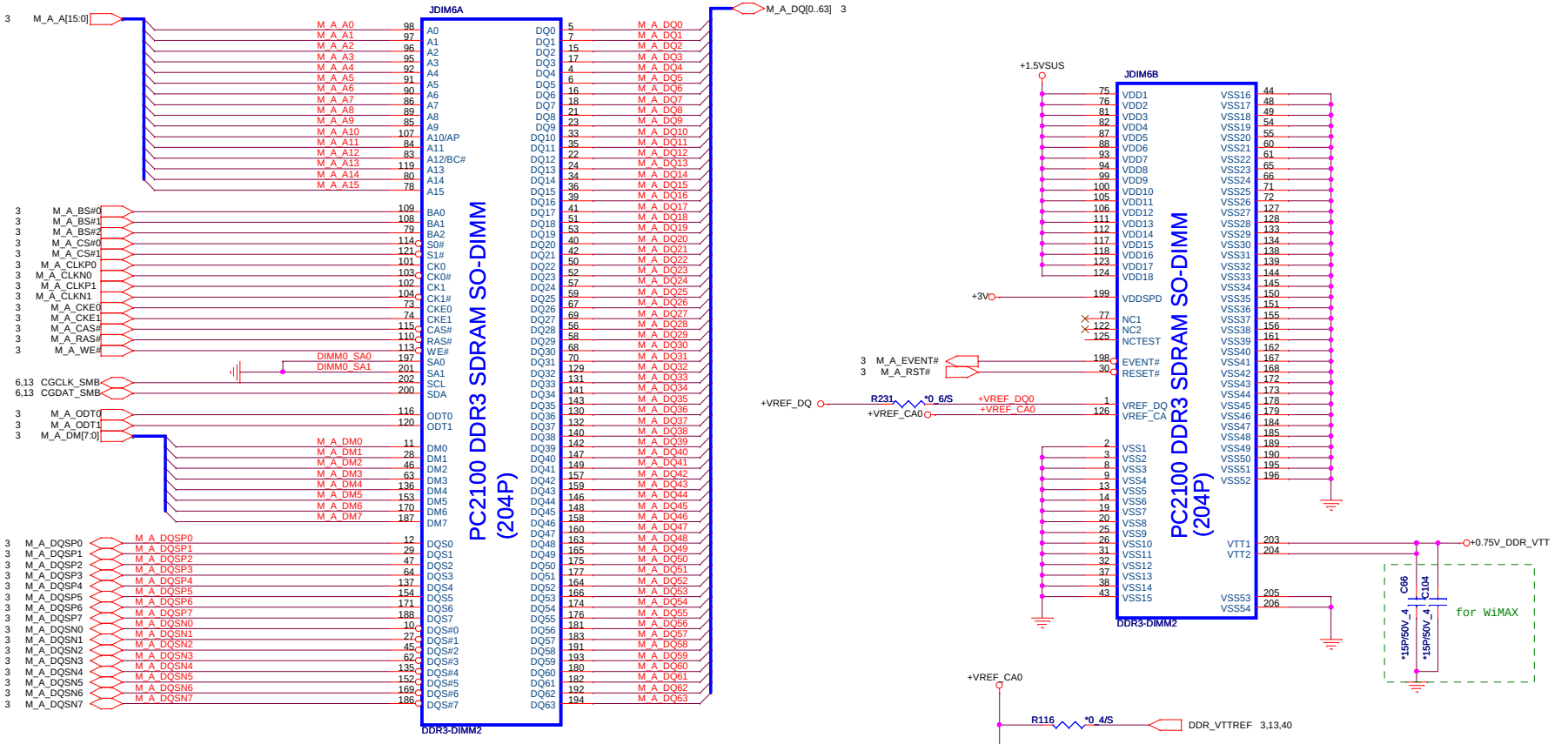




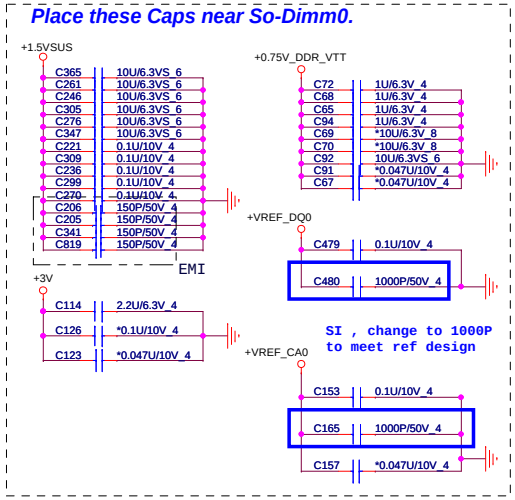


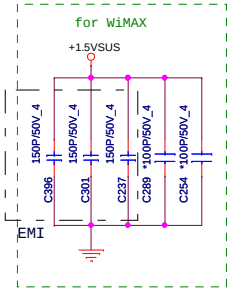


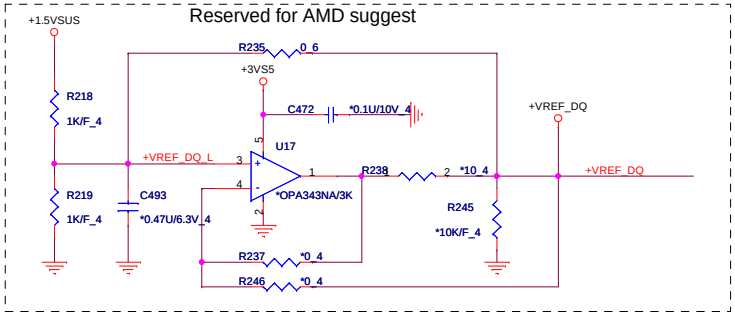
PROJECT : R53 Quanta Computer Inc.		
Size: Custom	Document Number: ANX3110	Rev: 1A
Date: Friday, November 11, 2011	Sheet 11 of 44	



H9．2mm







13,40 +0.75V_DDR_VTT
2,3,4,5,13,40,41,44 +1.5VSUS
2,4,6,8,9,10,11,13,14,18,23,24,25,26,27,28,29,30,31,32,33,41,42,44 +3V

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-0	1A
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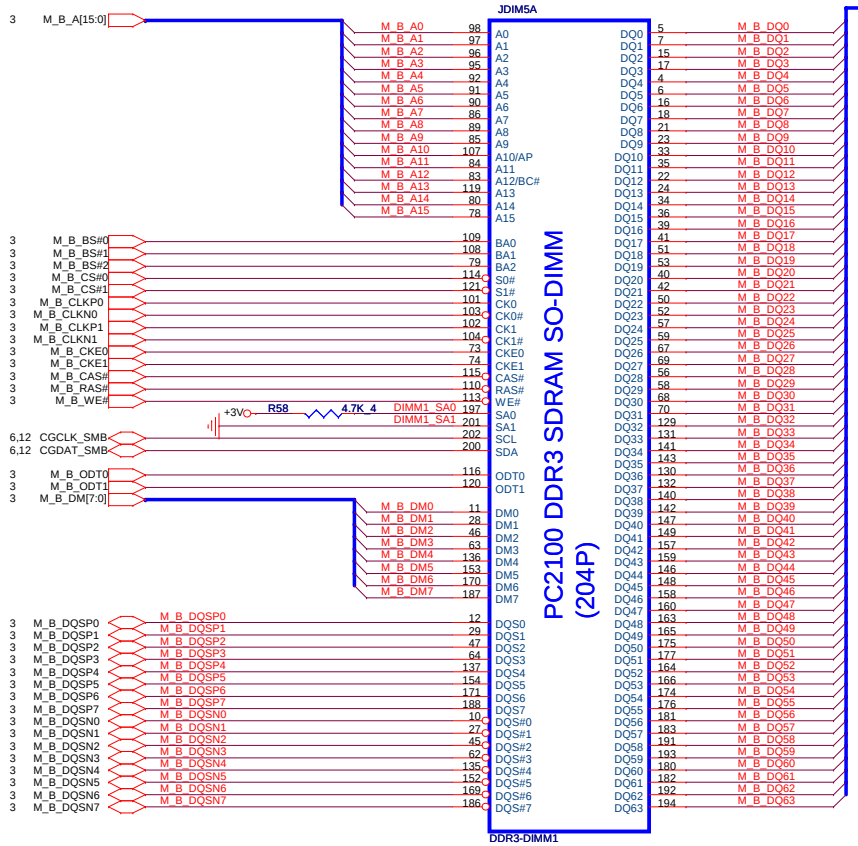
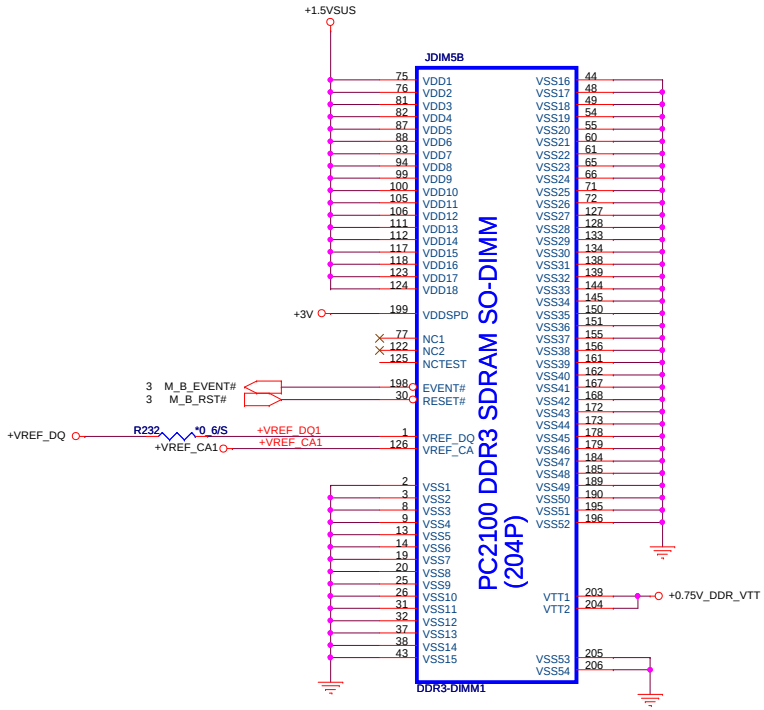
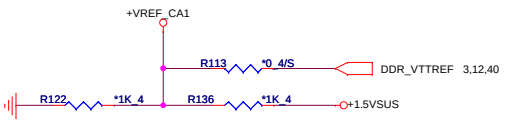
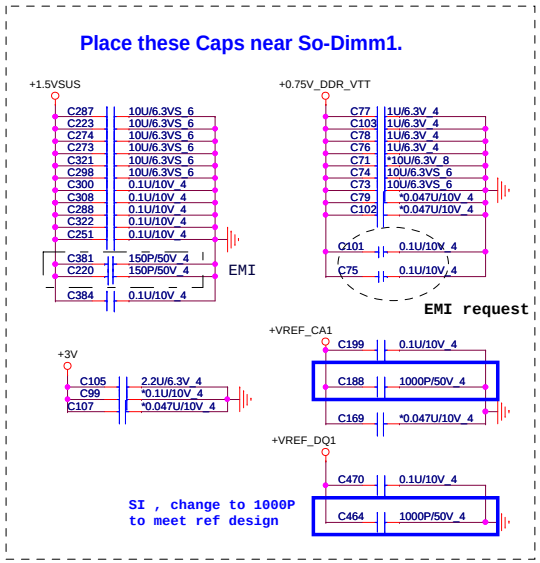






H5.2mm



12,40 +0.75V_DDR_VTT
2,3,4,5,12,40,41,44 +1.5VSUS
2,4,6,8,9,10,11,12,14,18,23,24,25,26,27,28,29,30,31,32,33,41,42,44 +3V

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1	1A

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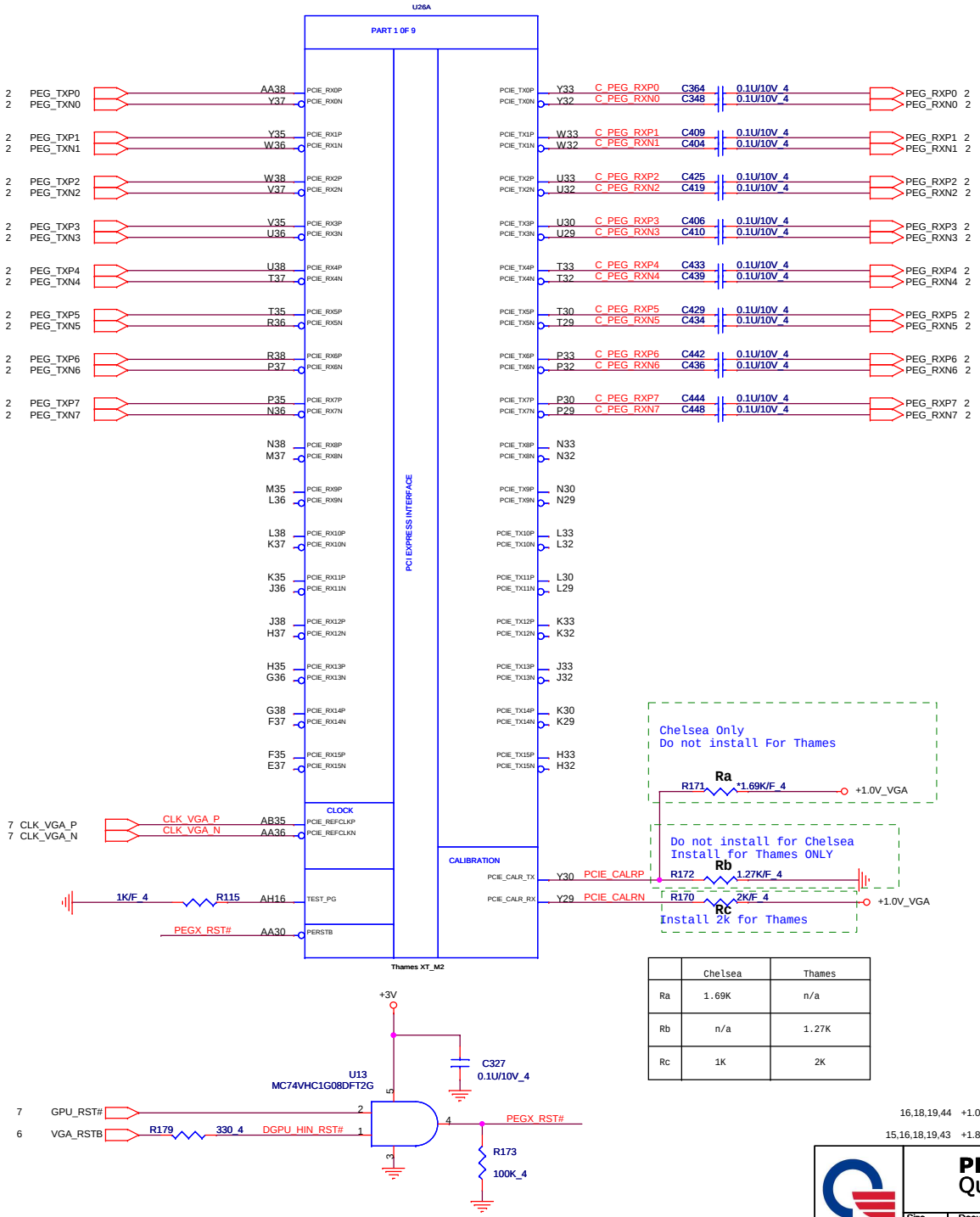


	Chelsea	Thames
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K

16,18,19,44 +1.0V_VGA → +1.0V_VGA
15,16,18,19,43 +1.8V_VGA → +1.8V_VGA

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Chelsea_PCIE_Interface	1A

Date: Monday, November 14, 2011 Sheet 14 of 44

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix- D die	64Mx16 *8, 900Mhz	H5TQ1G63DFR-11C
0001	Micron- G die	64Mx16 *8, 900Mhz	MT41J64M16JT-107G:G
0010	Samsung- G die	64Mx16 *8, 900Mhz	K4W1G1646G-BC11
0011	Hynix- D die	128Mx16 *8, 900Mhz	H5TQ2G63DFR-11C
0100	Micron- D die	128Mx16 *8, 900Mhz	MT41J128M16HA-107G:D
0101	Samsung- C die	128Mx16 *8, 900Mhz	K4W2G1646C-HC11
0110			
0111			
1000			
1001			
1010			
1011			
1100			
1101			
1110			
1111			

GPIO16 GPIO20 GPIO15

Thames-XT	PWRCNTL 2	PWRCNTL 1	PWRCNTL 0	VGA CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V

Memory ID

Access to SMBBus ans SDA/SCL is mandatory on all designs
Add test points on SMBBus and SDA/SCL for debug

Reserve for AMD debug only

GPIO22(ROMCS#)
3-k external pull up is required
if an external BIOS ROM chip is used. Must be unconnected if no external BIOS ROM chip is used

GPIO29, GPIO30 are NC on Thames

Thames INSTALL, do not install for Chelsea
PS_0 should be tied to GND on Thames

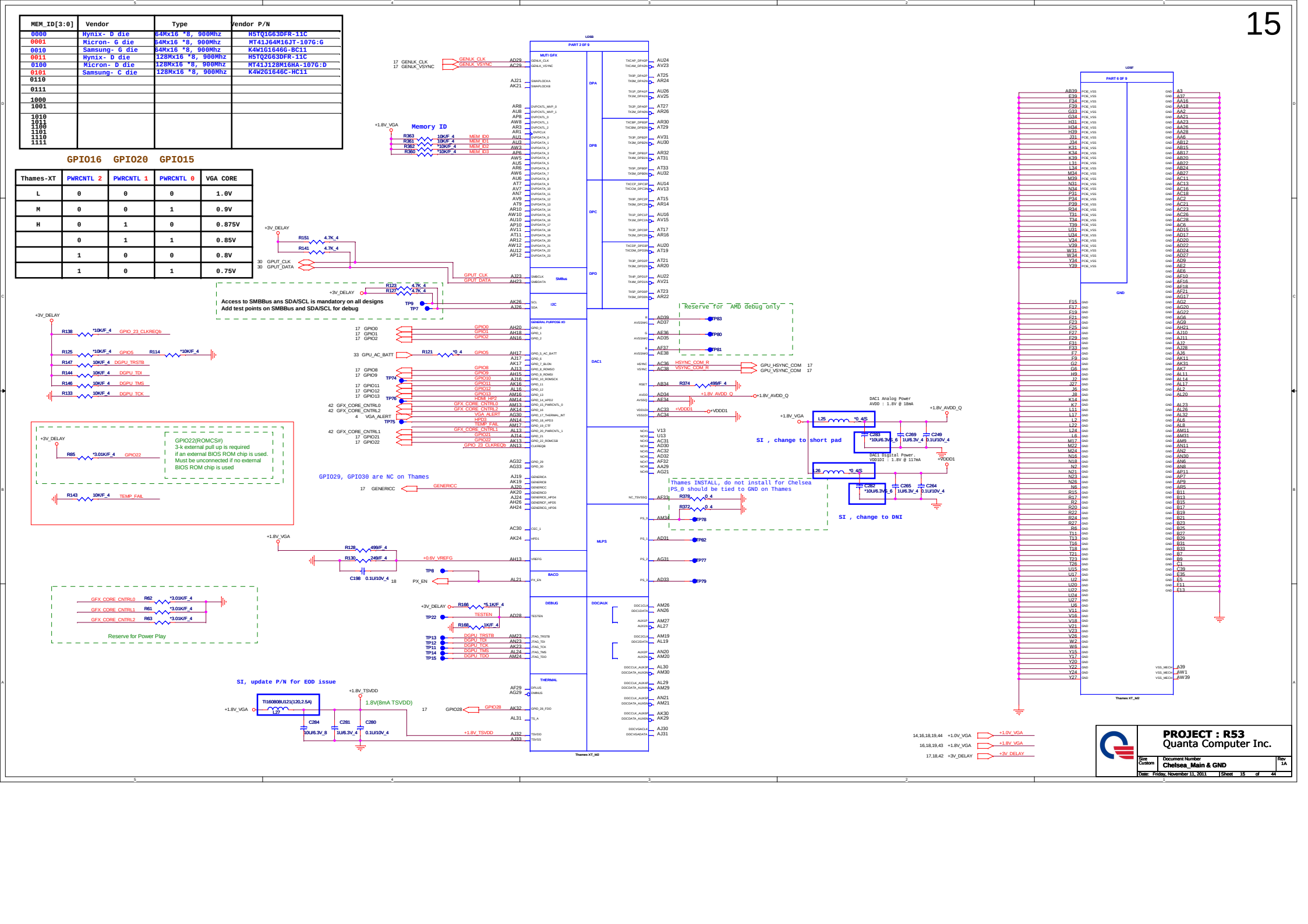
SI , change to short pad

SI , change to DNI

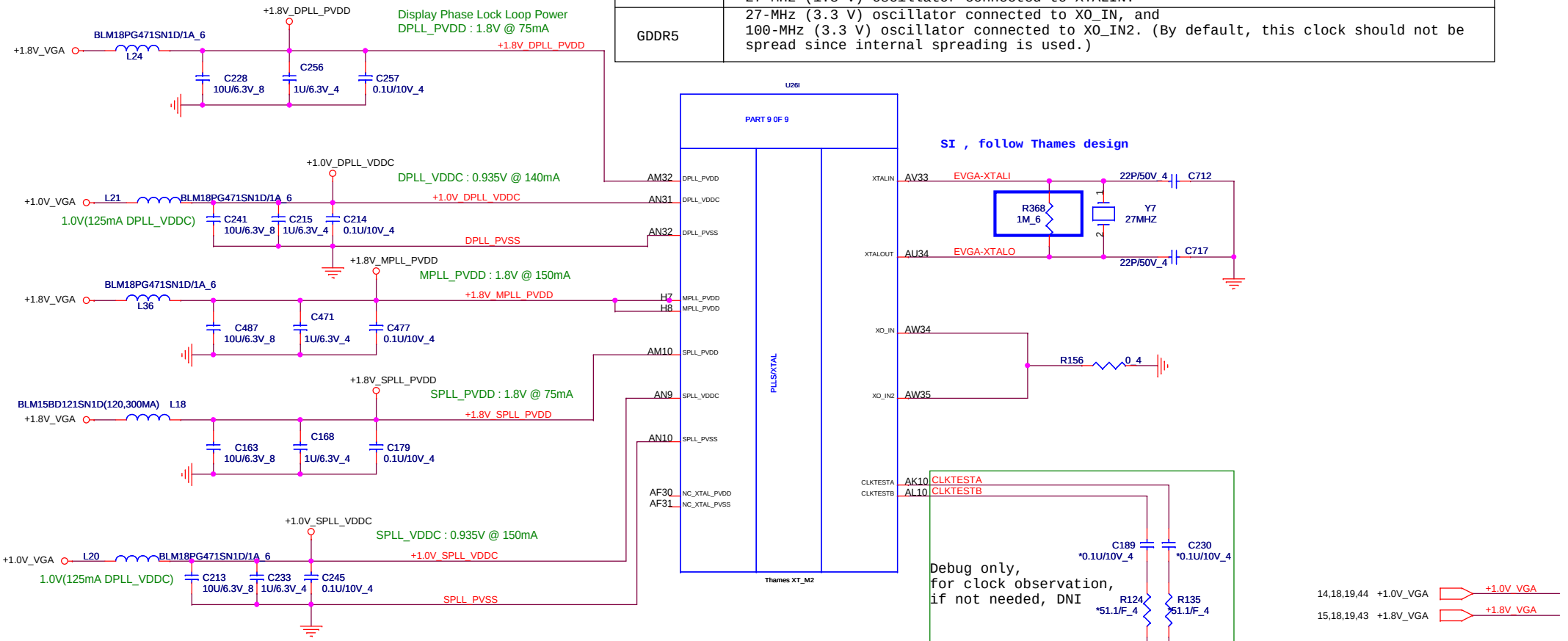
Reserve for Power Play

SI, update P/N for EOD issue

1.8V(8mA TSVDD)



Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Chelsea_XTAL	1A

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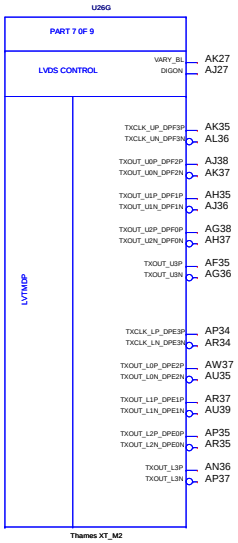
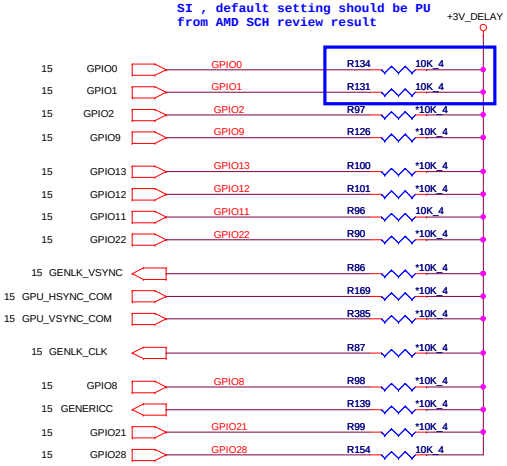


CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

SI , default setting should be PU from AMD SCH review result

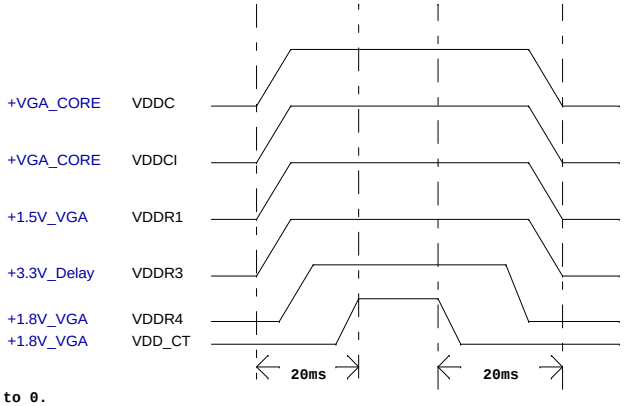


Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

Power Up/Down Sequence



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Chelsea_LVDS / STRAP	1A
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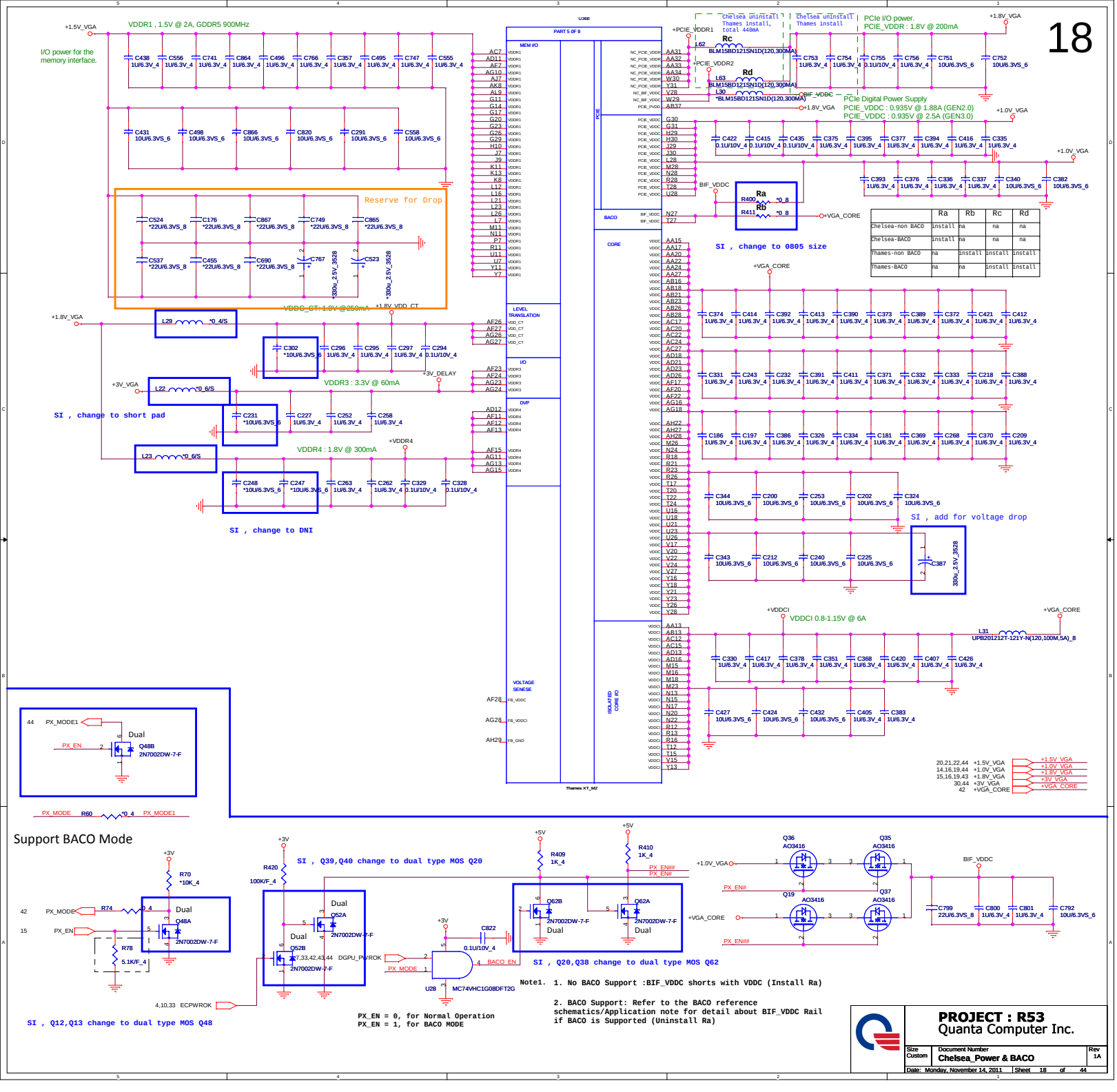

	Ra	Rb	Rc	Rd
Chelsea-non BACO	install	na	na	na
Chelsea-BACO	install	na	na	na
Thames-non BACO	na	install	install	install
Thames-BACO	na	na	install	install

Note1. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Chelsea_Power & BACO	1A
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For Thames a dedicated BEAD is required
for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

For Thames a dedicated BEAD is required
for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10

U26H

PART 8 0F 9

DP_VDDR

DP_VDDC

DP GND

CALIBRATION

Thames XT_M2

DP/TMDS/LVDS Transmitter Power
HDMI mode: 1.8V@237mA per port
DP mode: 1.8V@188mA per port

+1.8V_VGA

DPAB_VDD18

L59 *0_4/S

C709 *10U/6.3VS_6 | C711 1U/6.3V_4 | C714 0.1U/10V_4

AN24 DP_VDDR
AP24 DP_VDDR
AP25 DP_VDDR
AP26 DP_VDDR
AU28 DP_VDDR
AV29 DP_VDDR

+1.8V_VGA

DPCD_VDD18

L57 *0_4/S

C699 *10U/6.3VS_6 | C708 1U/6.3V_4 | C702 0.1U/10V_4

AP20 DP_VDDR
AP21 DP_VDDR
AP22 DP_VDDR
AP23 DP_VDDR
AU18 DP_VDDR
AV19 DP_VDDR

+1.8V_VGA

DPEF_VDD18

L61 *0_4/S

C732 *10U/6.3VS_6 | C728 1U/6.3V_4 | C733 0.1U/10V_4

AH34 DP_VDDR
AJ34 DP_VDDR
AF34 DP_VDDR
AG34 DP_VDDR
AM37 DP_VDDR
AL38 DP_VDDR

SI , change to short pad

SI , change to DNI

R150 150/F_4 AW28 DPAB_CALR

R365 150/F_4 AW18 DPCD_CALR

R377 150/F_4 AM39 DPEF_CALR

DP_VDDC AP31
DP_VDDC AP32
DP_VDDC AN33
DP_VDDC AP33

DP_VDDC AP13
DP_VDDC AT13
DP_VDDC AP14
DP_VDDC AP15

DP_VDDC AL33
DP_VDDC AM33
DP_VDDC AK33
DP_VDDC AK34

DP_VSSR AN27
DP_VSSR AP27
DP_VSSR AP28
DP_VSSR AW24
DP_VSSR AW26
DP_VSSR AN29
DP_VSSR AP29
DP_VSSR AP30
DP_VSSR AW30
DP_VSSR AW32
DP_VSSR AN17
DP_VSSR AP16
DP_VSSR AP17
DP_VSSR AW14
DP_VSSR AW16
DP_VSSR AN19
DP_VSSR AP18
DP_VSSR AP19
DP_VSSR AW20
DP_VSSR AW22
DP_VSSR AN34
DP_VSSR AP39
DP_VSSR AR39
DP_VSSR AU37
DP_VSSR AF39
DP_VSSR AH39
DP_VSSR AK39
DP_VSSR AL34
DP_VSSR AV27
DP_VSSR AR28
DP_VSSR AV17
DP_VSSR AR18
DP_VSSR AN38
DP_VSSR AM35

DPAB_VDD10

DP/TMDS/LVDS Transmitter Power
0.935V@222mA per port

+1.0V_VGA

*0_4/S L60

C722 0.1U/10V_4 | C721 1U/6.3V_4 | C720 *10U/6.3VS_6

DPCD_VDD10

DP/TMDS/LVDS Transmitter Power
0.935V@222mA per port

+1.0V_VGA

*0_4/S L58

C710 0.1U/10V_4 | C706 1U/6.3V_4 | C700 *10U/6.3VS_6

SI , change to short pad

DPEF_VDD10

DP/TMDS/LVDS Transmitter Power
0.935V@222mA per port

+1.0V_VGA

*0_4/S L28

C279 0.1U/10V_4 | C278 1U/6.3V_4 | C277 *10U/6.3VS_6

SI , change to DNI

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Chelsea_DP Powers	1A
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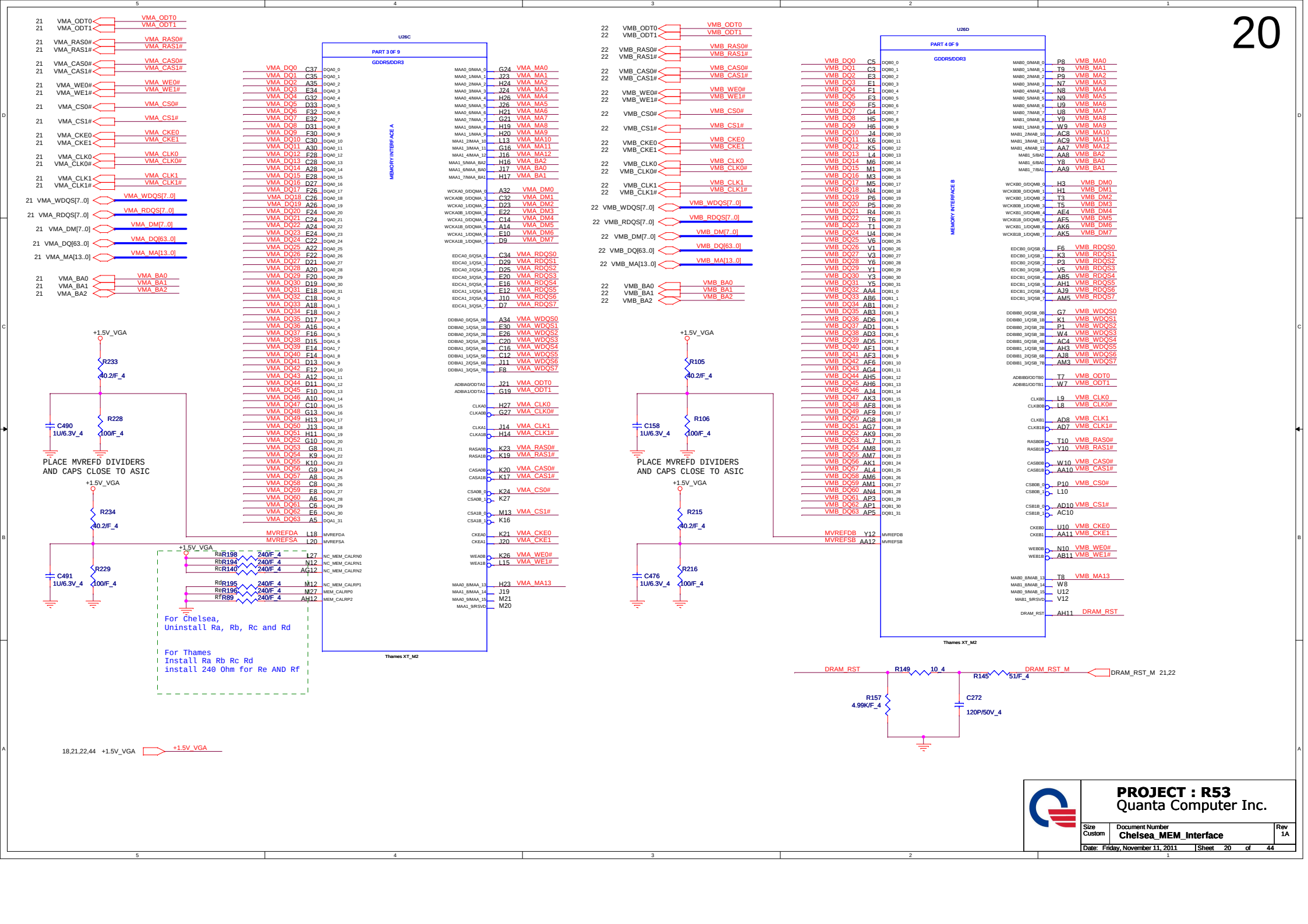

PROJECT : R53	
Quanta Computer Inc.	
Size: Custom	Document Number: Chelsea_MEM_Interface
Rev: 1A	
Date: Friday, November 11, 2011	Sheet 20 of 44

CHANNEL A: 256MB/512MB DDR3

Vendor	QCI PN	B/S PN
Hynix D(Vega)	AKD5LZWTW02	AKD5LZWTW08
Micron G die	AKD5EGSTL00	AKD5LZSTL10
SAMSUNG G die	AKD5EGGT500	AKD5EGGT502
Hynix B(Vega)	AKD5MGWTW00	AKD5MGWTW07
SAMSUNG C die	AKD5MGWT500	AKD5MGWT508

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM-A (DDR3 BGA96)	3A

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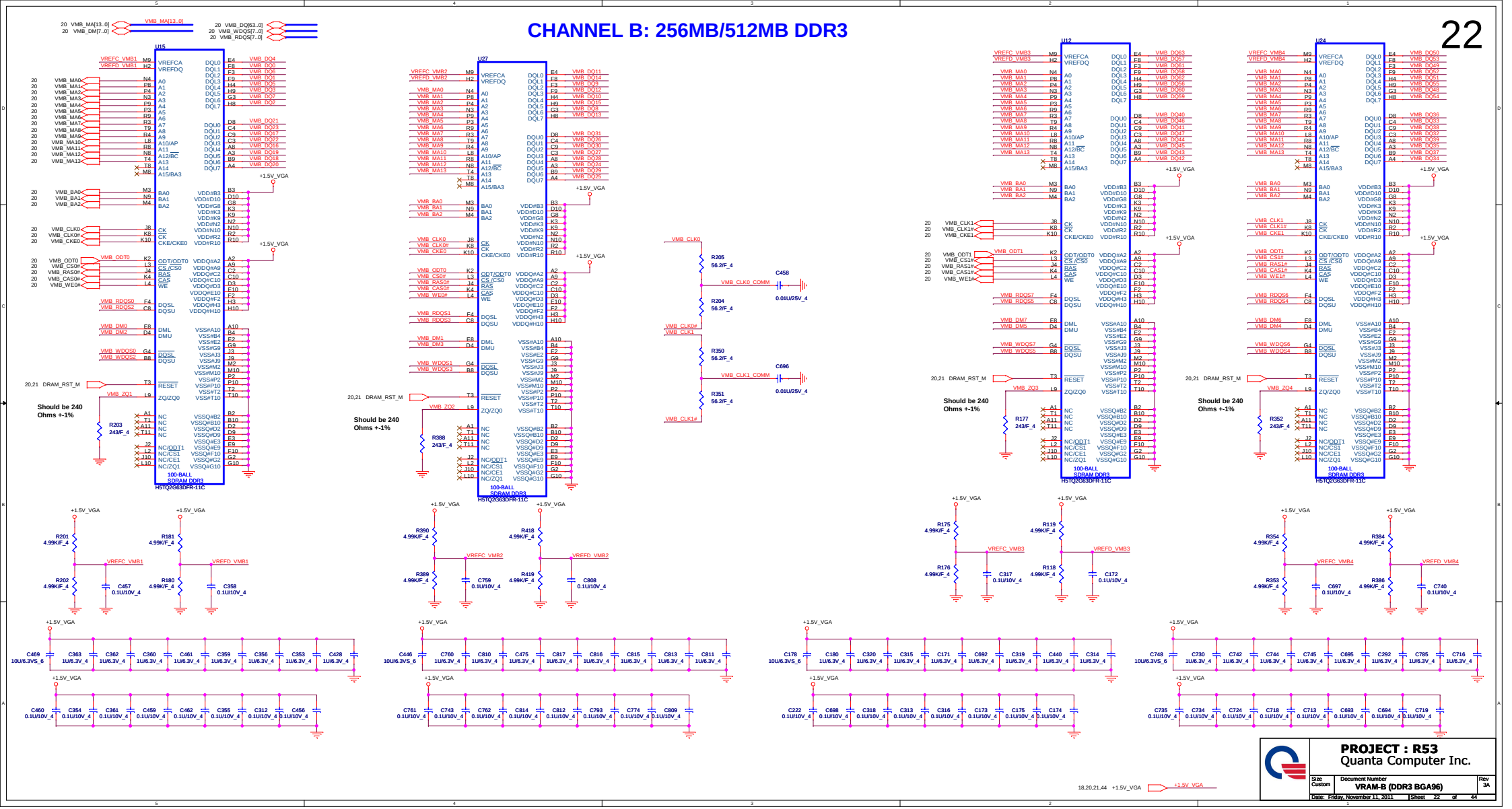
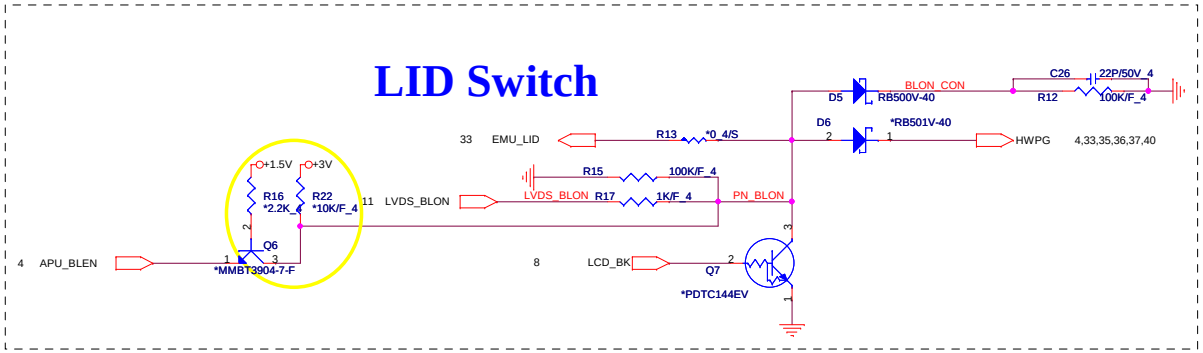
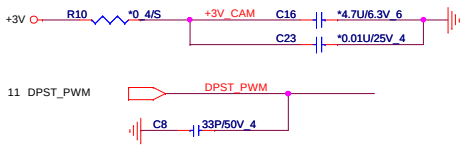
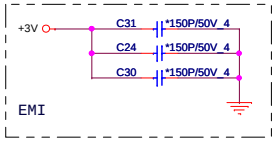
CHANNEL B: 256MB/512MB DDR3

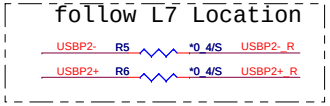


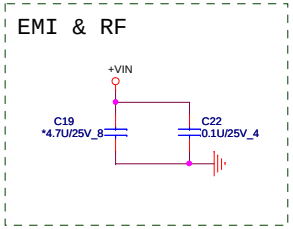
LID Switch

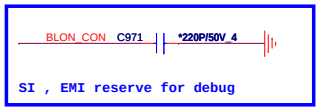


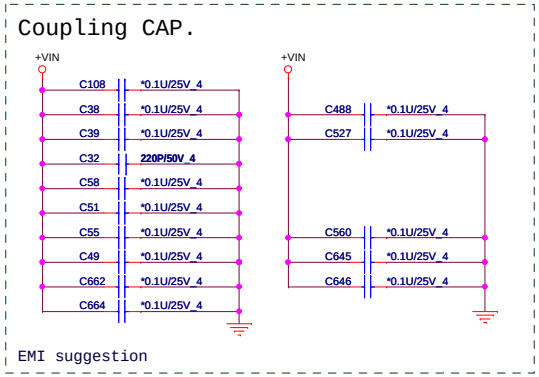


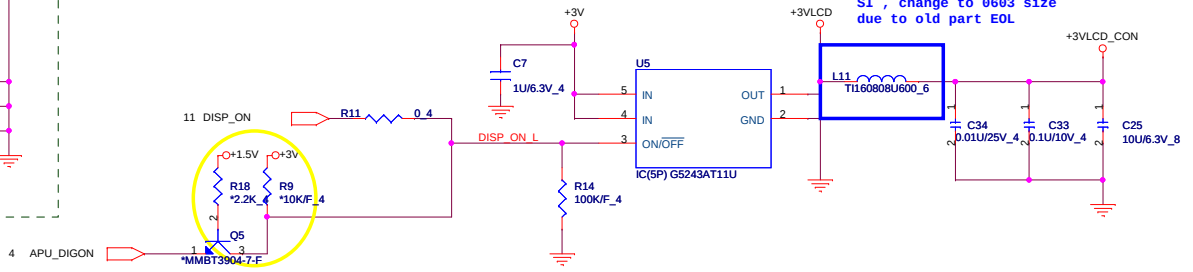


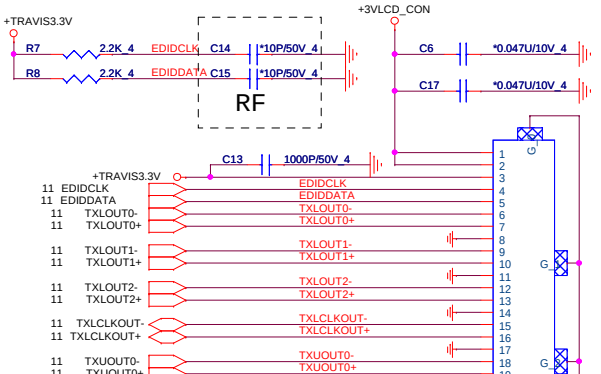












4,7,30,33,34,35 +3VPCU
2,4,6,8,9,10,11,12,13,14,18,24,25,26,27,28,29,30,31,32,33,41,42,44 +3V
9,34,41,44 +12VALW
34,35,36,37,39,40,41,42,44 +VIN

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Quanta Computer Inc.

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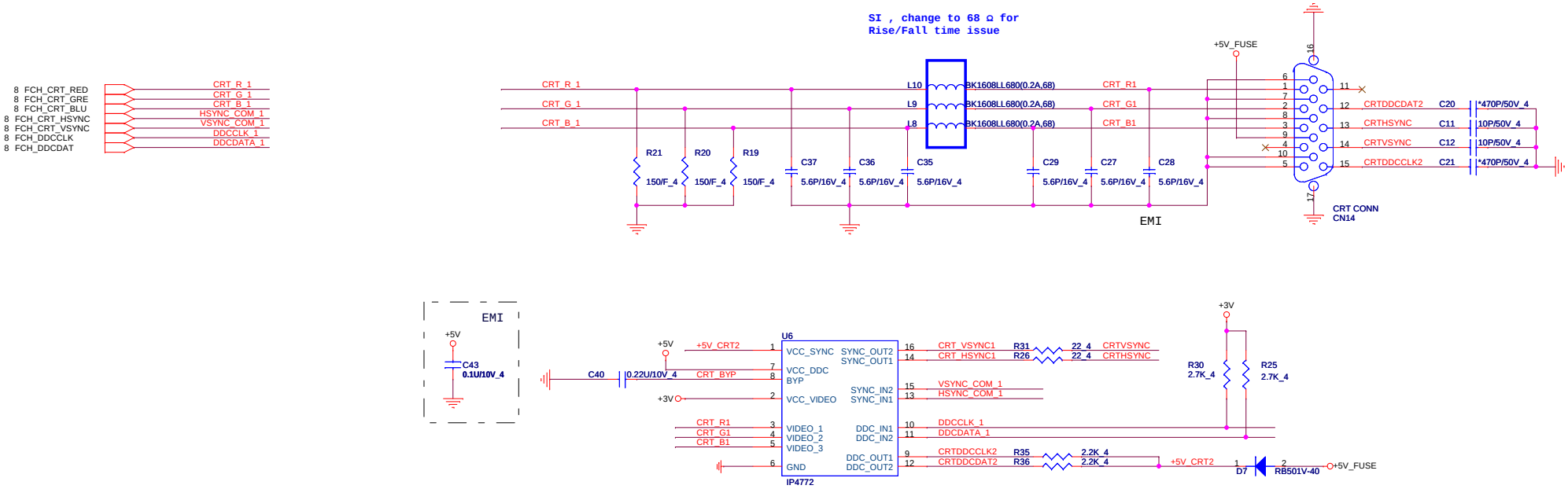
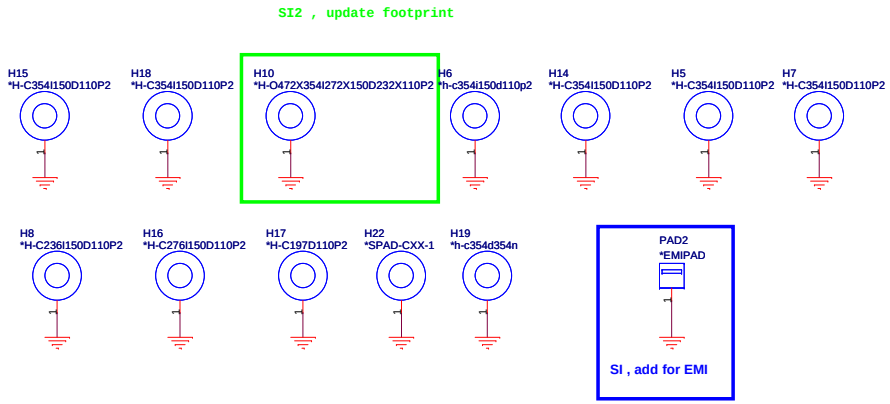
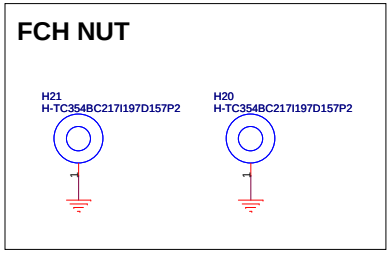
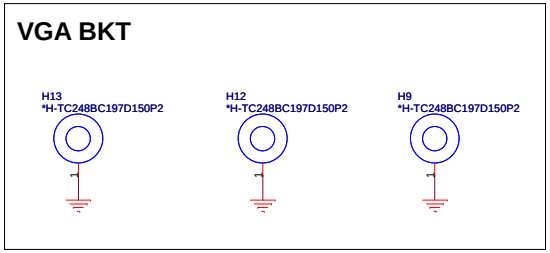
CRT PORT

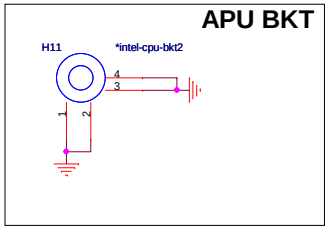


HOLE









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Quanta Computer Inc.

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Custom	CRT,Hole	1A
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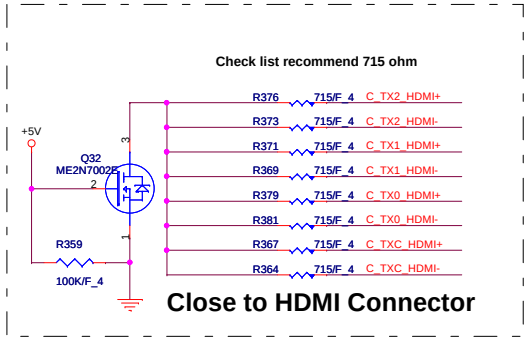
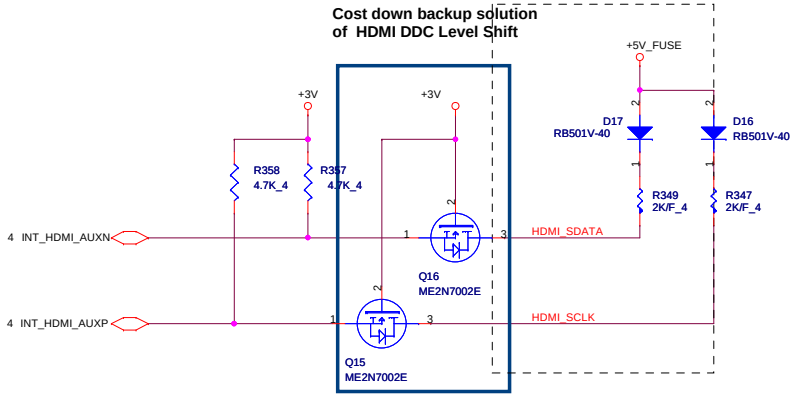
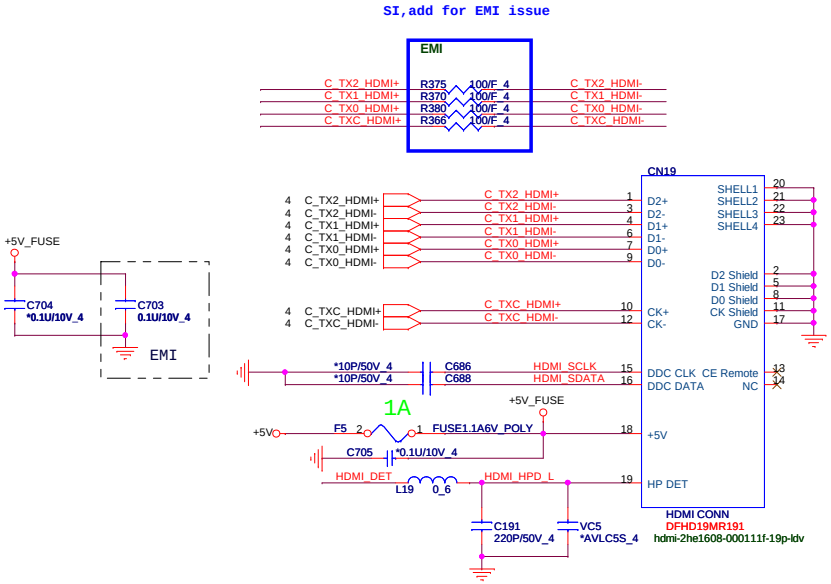
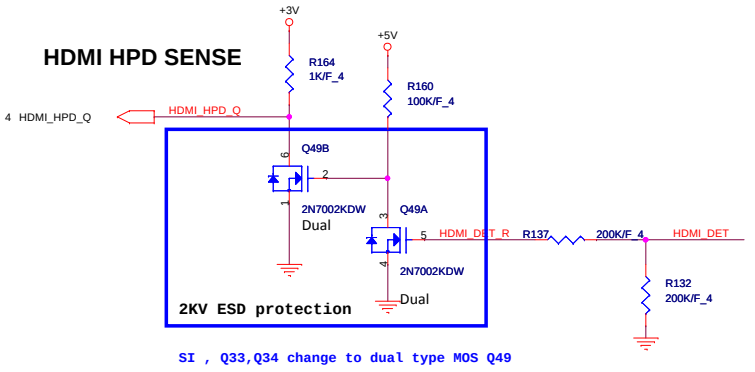
HDMI PORT









SI , Q33,Q34 change to dual type MOS Q49

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI CONN	1A

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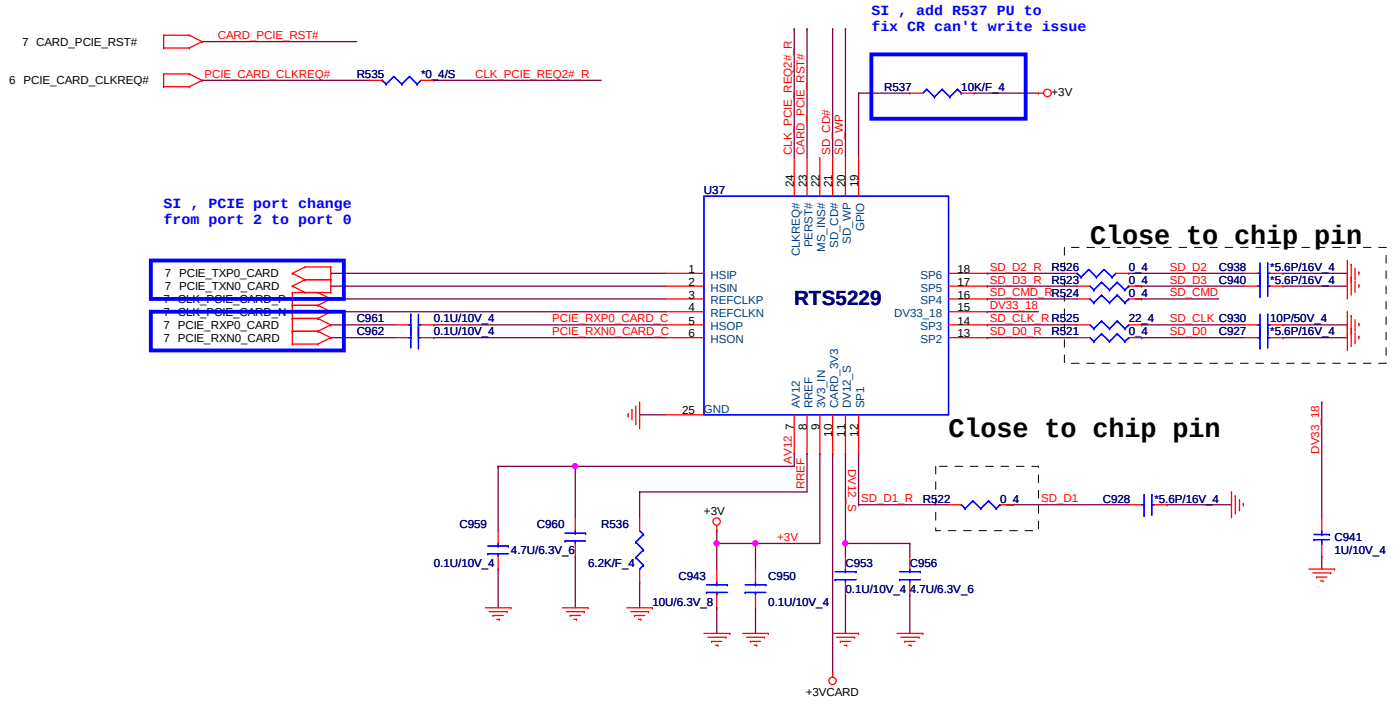

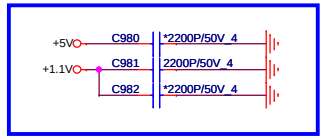

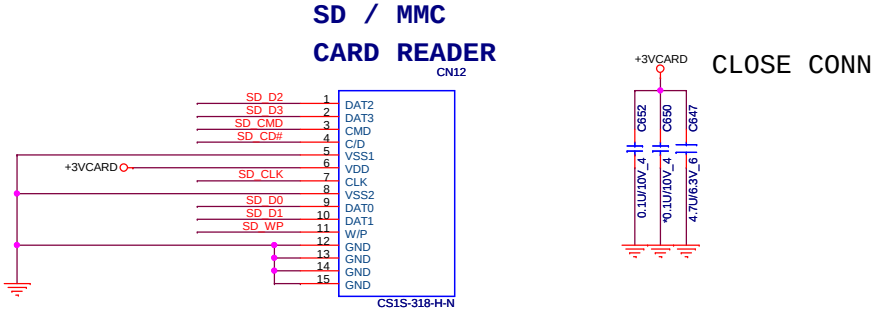

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5219 & CR SOCKET &HOLE	1A

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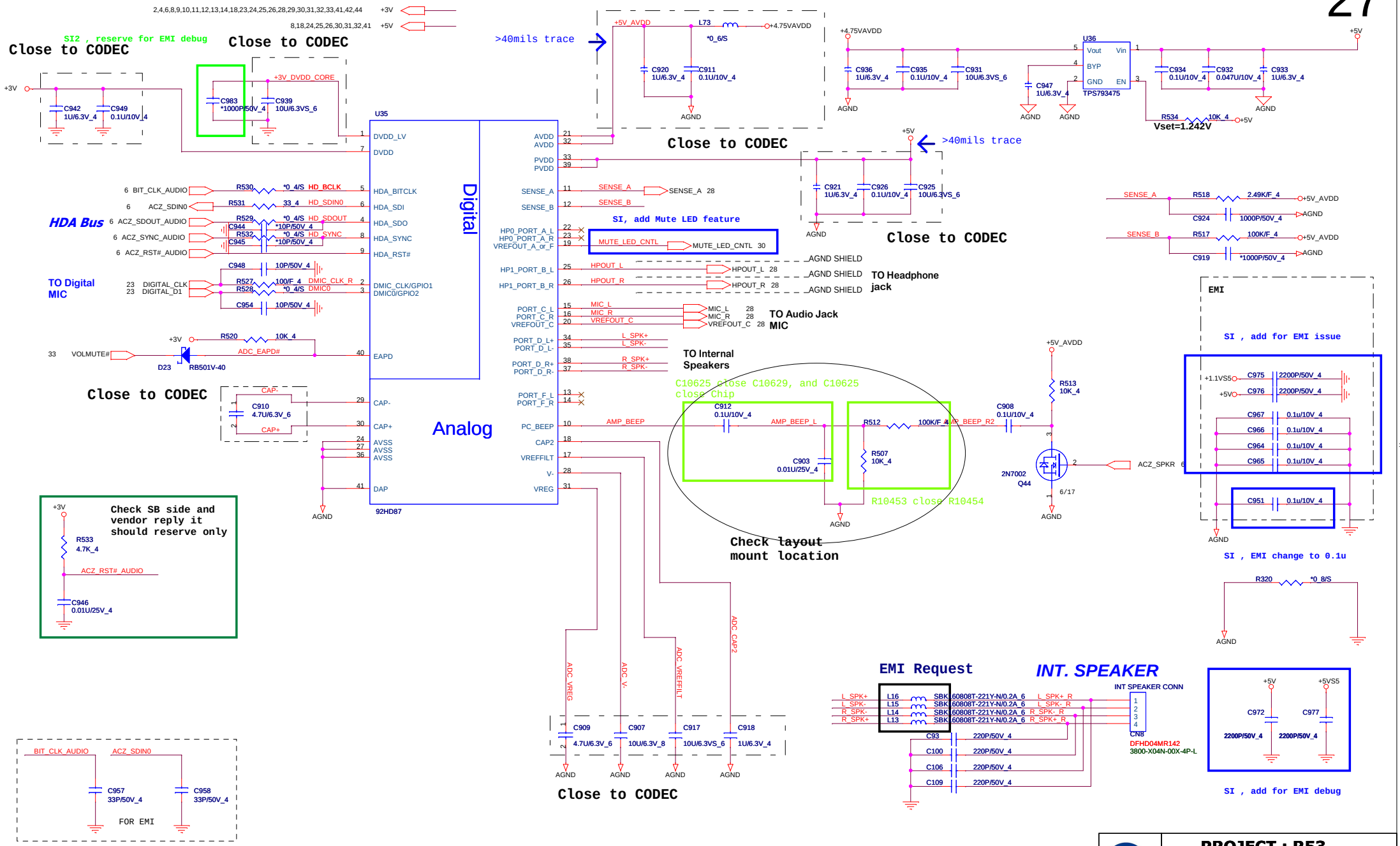

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Size	Document Number	Rev
Custom	Azalia 92HD80	1A

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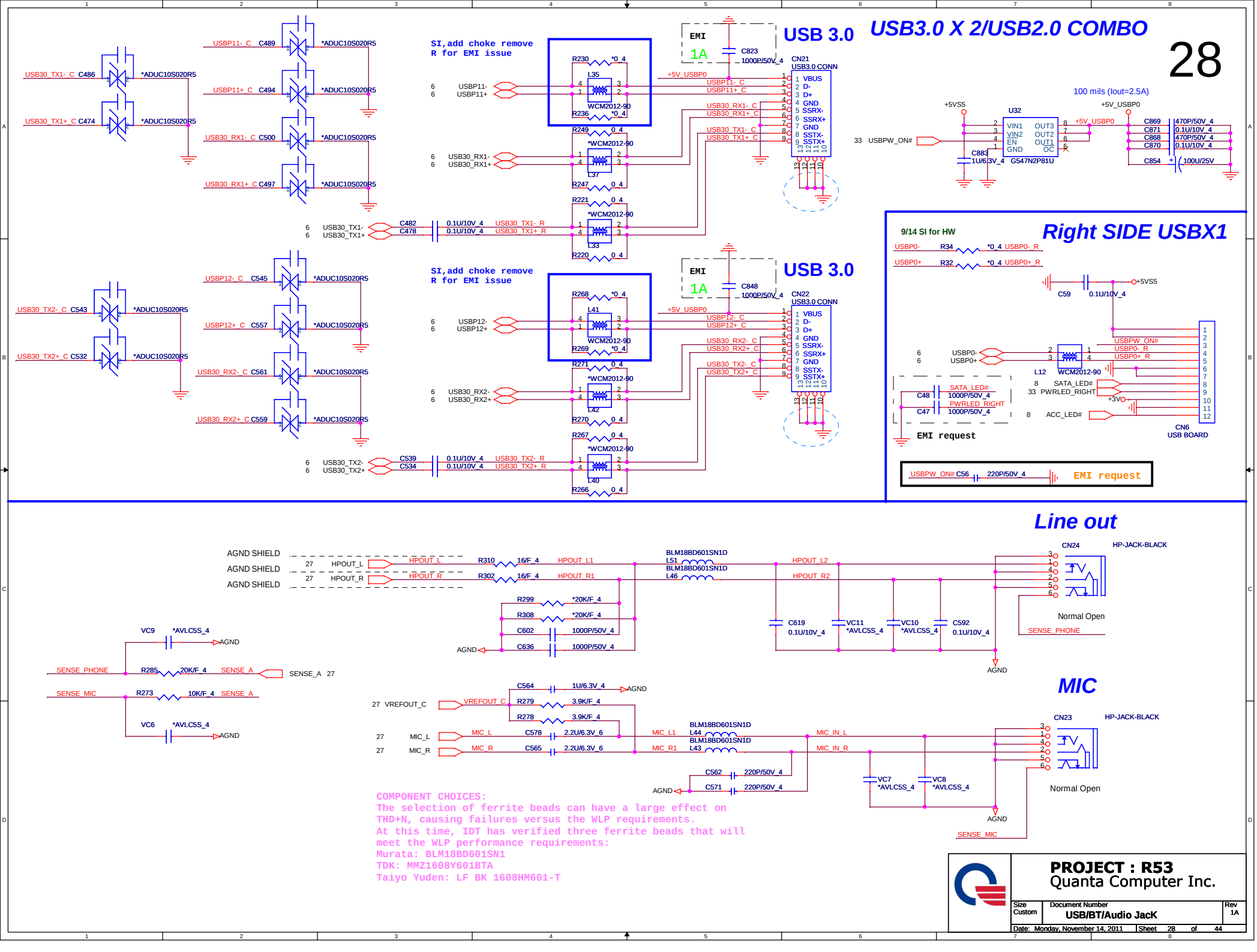
USB 3.0
USB3.0 X 2/USB2.0 COMBO
28
SI,add choke remove R for EMI issue
EMI
1A
C823 1000P/50V_4
CN21 USB3.0 CONN
VBUS
D-
D+
GND
SSRX-
SSRX+
GND
SSTX-
SSTX+
USB30_TX1- C C486
USB30_TX1+ C C474
USB30_RX1- C C500
USB30_RX1+ C C497
USBP11- C C489
USBP11+ C C494
*ADUC10S020R5
R230 *0_4
L35 WCM2012-90
R236 *0_4
R249 0_4
*WCM2012-90
L37
R247 0_4
R221 0_4
*WCM2012-90
L33
R220 0_4
C482 C478 0.1U/10V_4
USB30_TX1- R
USB30_TX1+ R
+5V_USBP0
USBP11- C
USBP11+ C
USB30_RX1- C
USB30_RX1+ C
USB30_TX1- C
USB30_TX1+ C
100 mils (Iout=2.5A)
+5VS5
U32
VIN1
VIN2
EN
GND
OUT3
OUT2
OUT1
OC
G547N2P81U
C883 1U/6.3V_4
33 USBPW_ON#
C869 470P/50V_4
C871 0.1U/10V_4
C868 470P/50V_4
C870 0.1U/10V_4
C854 100U/25V
USB 3.0
USB30_TX2- C C543
USB30_TX2+ C C532
USB30_RX2- C C561
USB30_RX2+ C C559
USBP12- C C545
USBP12+ C C557
R268 *0_4
L41 WCM2012-90
R269 *0_4
R271 0_4
*WCM2012-90
L42
R270 0_4
R267 0_4
*WCM2012-90
L40
R266 0_4
C539 C534 0.1U/10V_4
USB30_TX2- R
USB30_TX2+ R
C848 1000P/50V_4
CN22 USB3.0 CONN
USBP12- C
USBP12+ C
USB30_RX2- C
USB30_RX2+ C
USB30_TX2- C
USB30_TX2+ C
Right SIDE USBX1
9/14 SI for HW
USBP0- R34 *0_4 USBP0- R
USBP0+ R32 *0_4 USBP0+ R
C59 0.1U/10V_4
+5VS5
USBP0-
USBP0+
L12 WCM2012-90
USBPW_ON#
USBP0- R
USBP0+ R
SATA_LED#
PWRLED_RIGHT
ACC_LED#
C48 1000P/50V_4
C47 1000P/50V_4
+3VO
CN6 USB BOARD
EMI request
USBPW_ON# C56 220P/50V_4
EMI request
Line out
AGND SHIELD
HPOUT_L
HPOUT_R
R310 16/F_4
R302 16/F_4
HPOUT_L1
HPOUT_R1
BLM18BD601SN1D
L51
L46
HPOUT_L2
HPOUT_R2
R299 *20K/F_4
R308 *20K/F_4
C602 1000P/50V_4
C636 1000P/50V_4
C619 0.1U/10V_4
VC11 *AVLC5S_4
VC10 *AVLC5S_4
C592 0.1U/10V_4
CN24 HP-JACK-BLACK
Normal Open
SENSE_PHONE
VC9 *AVLC5S_4
R285 20K/F_4
SENSE_A
SENSE_MIC
R273 10K/F_4
VC6 *AVLC5S_4
MIC
C564 1U/6.3V_4
VREFOUT_C
R279 3.9K/F_4
R278 3.9K/F_4
MIC_L
MIC_R
C578 2.2U/6.3V_6
C565 2.2U/6.3V_6
MIC_L1
MIC_R1
L44
L43
MIC_IN_L
MIC_IN_R
C562 220P/50V_4
C571 220P/50V_4
VC7 *AVLC5S_4
VC8 *AVLC5S_4
CN23 HP-JACK-BLACK
Normal Open
COMPONENT CHOICES:
The selection of ferrite beads can have a large effect on THD+N, causing failures versus the WLP requirements.
At this time, IDT has verified three ferrite beads that will meet the WLP performance requirements:
Murata: BLM18BD601SN1
TDK: MMZ1608Y601BTA
Taiyo Yuden: LF BK 1608HM601-T
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Quanta Computer Inc.
Size Custom
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For EMI 0 ~ 22 ohm

R72 10_4 LAN_XTAL1 XTAL1
Y5 25MHz XTAL2
C130 33P/50V_4
C129 33P/50V_4

+3VLANVCC
+3V_LAN
C127 0.1U/10V_4
C134 0.1U/10V_4
C131 0.1U/10V_4
C148 0.1U/10V_4

GND VIA x 9 Pcs

+1.05V_LAN
R71 2.49K/F_4 LANRSET
+3V_LAN
LAN_TX#
LAN_GPIOS R73 1K/F_4 +3V_LAN
LAN_GLINK100#

U10 RTL8105E
GND AVDD33 AVDD33 RSET AVDD10 CKXTAL2 CKXTAL1 AVDD33 DVDD10(NC) LED1 DVDD33 GPO/SMBALERT LED1/EESK
MDI0+ MDI0- MDI1+ MDI1-
MDIP0 MDIN0 AVDD10 MDIP1 MDIN1 AVDD10(NC) MDIP2(NC) MDIN2(NC) AVDD10(NC) MDIP3(NC) MDIN3(NC) AVDD33(NC)
REGOUT VDDREG VDDREG ENSWREG EEDI LED3/EEDO EECS DVDD10 LANWAKEB DVDD33 ISOLATEB PERSTB
LAN_GLINK10# R82 10K/F_4
LAN_ECS_SCL R80 10K/F_4
+1.05V_LAN
PCIE_WAKE# → PCIE_WAKE# 6,32
+3V_LAN
ISOLATEB
LAN_PCIE_RST# → LAN_PCIE_RST# 7,11
DVDD10 SMBCLK(NC) SMBDATA(NC) CLKREQB HSIP HSIN REFCLK_P REFCLK_N DVDD10 HSOP HSON GND

U9 NS681684
LAN_MX0+ LAN_MX0- LAN_MCT1 LAN_MX1+ LAN_MX1- LAN_MCT0
TD+ TD- CT RD+ RD- CT
TX+ CMT TX- RX- CT RX+
MDI0+ V_DAC2 MDI0- MDI1- V_DAC1 MDI1+
75_4 R47 C89 0.01U/100V_0603
75_4 R48 C90 0.01U/100V_0603
C64 10P/3KV_1808
C95 0.01U/25V_4

+1.05V_LAN
PCIE_LAN_CLKREQ# R107 *0_4/S
LAN_CLKRQ
PCIE_TXP1_LAN
PCIE_TXN1_LAN
CLK_PCIE_LANP
CLK_PCIE_LANN
PCIE_RXN1_LAN_L C161 0.1U/10V_4 → PCIE_RXN1_LAN 7
PCIE_RXP1_LAN_L C160 0.1U/10V_4 → PCIE_RXP1_LAN 7
+1.05V_LAN

+3V
R104 1K_4
ISOLATEB
R94 15K/F_4

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

IND SMD 4.7UH +-20% 680MA(CBC2518T4R7M)
CV-4707MZ00

Power trace Layout 寬度> 60mil
>60mil

+1.05V_LAN
C112 1U/6.3V_4
C159 0.1U/10V_4
C149 0.1U/10V_4
C132 0.1U/10V_4
C145 0.1U/10V_4

+1.05V_LAN
C146 0.1U/10V_4
C155 0.1U/10V_4
C125 0.1U/10V_4
C115 0.1U/10V_4

LAN_GLINK100# LAN_GLED#
LAN_TX# LAN_YLED#
Link
C764 *1000P/50V_4
C789 *1000P/50V_4

RJ45
CN20
+3V_LAN R405 330_4 C791 1000P/50V_4
LAN_YLED LAN_YLED#
LED_AMBER_P LED_AMBER_N
LAN_MX1-
LAN_MX1+ LAN_MX0- LAN_MX0+
RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+
GND1 C797 180P/50V_4
GND C757 180P/50V_4
+3V_LAN R391 330_4
LAN_GLED LAN_GLED#
LED_WHITE_P LED_WHITE_N
RJ45_CONN
C779 180P/50V_4
C758 1000P/50V_4

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POWER BOTTON CONNECT

SI , reserve for Lid
+3VPCU noise

100mA

C963 *4.7U/6.3V_6
C122 1U/6.3V_4
C121 0.1U/10V_4
+3VPCU

33 LID_EC#
33 NBSWON1#
33 PWR_LED#
PWR_LED#

CN7
PWR BTN CONN

1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

SI , contact to +3VPCU

C117 PWR_LED# 0.1U/10V_4
C119 LID_EC# 0.1U/10V_4

SI , delete C120 for QB button drop

C118 NBSWON1# 0.1U/10V_4

SI , delete G5 for space save

KEYBOARD Con.

MY5 C141 220P/50V_4
MY6 C166 220P/50V_4
MY3 C170 220P/50V_4
MY7 C154 220P/50V_4
MY8 C162 220P/50V_4
MY9 C124 220P/50V_4
MY10 C211 220P/50V_4
MY11 C201 220P/50V_4
MY1 C143 220P/50V_4
MY2 C147 220P/50V_4
MY4 C150 220P/50V_4
MY0 C136 220P/50V_4
MX4 C128 220P/50V_4
MX6 C116 220P/50V_4
MX3 C139 220P/50V_4
MX2 C138 220P/50V_4
MX7 C113 220P/50V_4
MX0 C144 220P/50V_4
MX5 C133 220P/50V_4
MX1 C110 220P/50V_4
MY12 C182 220P/50V_4
MY13 C187 220P/50V_4
MY14 C196 220P/50V_4
MY15 C219 220P/50V_4
MY16 C235 220P/50V_4
MY17 C244 220P/50V_4

33 MY[0..17] MY[0..17]
33 MX[0..7] MX[0..7]

SI , mount for EMI

CN9
MX1 MX7 MX6 MY9 MX4 MX5 MY0 MX2 MX3 MY5 MY1 MX0 MY2 MY4 MY7 MY8 MY6 MY3 MY12 MY13 MY14 MY11 MY10 MY15 MY16 MY17
KB CONN

SI2 , for mute LED issue

33 CAPSLED#
+3V
R541 10K/F_4
27 MUTE_LED_CNTL
C984 *220P/50V_4
Q47 2N7002
R392 *10K/F_4

SI, add Mute LED feature

R152 200/F_6 CAPSLED# R
R153 200/F_6 MUTE_LED_CNTL_R
WIRELESS_ON_R
WIRELESS_OFF_R

SI2 , reserve for EMI

+5V
R159 1K/F_4
R158 *200/F_6
WIRELESS_ON_R
33 WIRELESS_ON
Q17 PDTC144EU

R161 1K/F_4
R163 *200/F_6
WIRELESS_OFF_R
33 WIRELESS_OFF
Q18 PDTC144EU

KEYBOARD PULL-UP

RP6 *10P8R-8.2K
+3VPCU
MY13 MY12 MY3 MY6 MY14 MY11 MY10 MY15

RP5 *10P8R-8.2K
+3VPCU
MY1 MY5 MY0 MY9 MY2 MY4 MY7 MY8

R142 *8.2K_4 MY16
R148 *8.2K_4 MY17

TOUCH PAD Con.

TP_LED# C970 *220P/50V_4
SMB_ACC_DAT C968 *220P/50V_4
SMB_ACC_CLK C969 *220P/50V_4

+5VS5
C973 *220P/50V_4
C974 *220P/50V_4
C978 *2200P/50V_4

SI , EMI reserve for debug

change to +3VSUS
close conn

+3VSUS
R254 4.7K_4 TPCLK
R251 4.7K_4 TPDATA

33 TPCLK
33 TPDATA
C509 10P/50V_4
L39 BLM18BA470SN1D/0.3A_6
L38 BLM18BA470SN1D/0.3A_6
C501 10P/50V_4

33 TPLED#
TP_LED#
TPCLK-1
TPDATA-1
SMB_ACC_DAT
SMB_ACC_CLK

CN11
TOUCH PAD CONN
DFFC08FR026
50503-0080n-001-8p-l

25 mils

+3VSUS
C492 0.1U/10V_4

Q51A 2N7002KDW
Dual
15 GPUT_CLK
SMB_ACC_CLK
SMB_ACC_CLK 33
R263 4.7K_4
+3V_VGA
+3VSUS
R262 4.7K_4
SMB_ACC_DAT 33
15 GPUT_DATA
SMB_ACC_DAT
Dual
Q51B 2N7002KDW
2KV ESD protection

SI , Q21,Q22 change to dual type MOS Q51

4,7,33,34,35 +3VPCU
8,18,24,25,26,27,31,32,41 +5V
32,41 +3VSUS
2,4,6,8,9,10,11,12,13,14,18,23,24,25,26,27,28,29,31,32,33,41,42,44 +3V

Q64A *2N7002KDW
Dual
SMB_ACC_CLK
SCL1 6
+3VSUS
SMB_ACC_DAT
SDA1 6
Dual
Q64B *2N7002KDW

SI2 , HP request Image sensor
SMBUS reserve to FCH

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/SW/TP	1A

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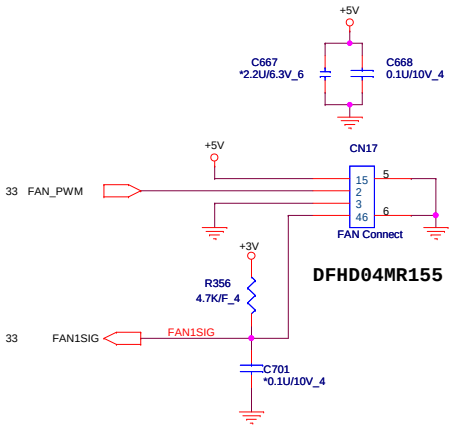
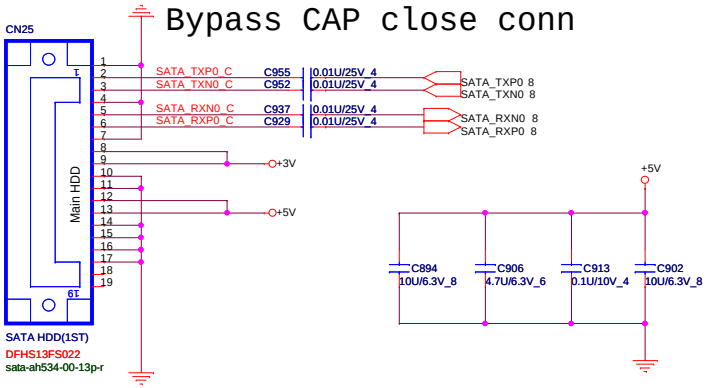
CPU FAN



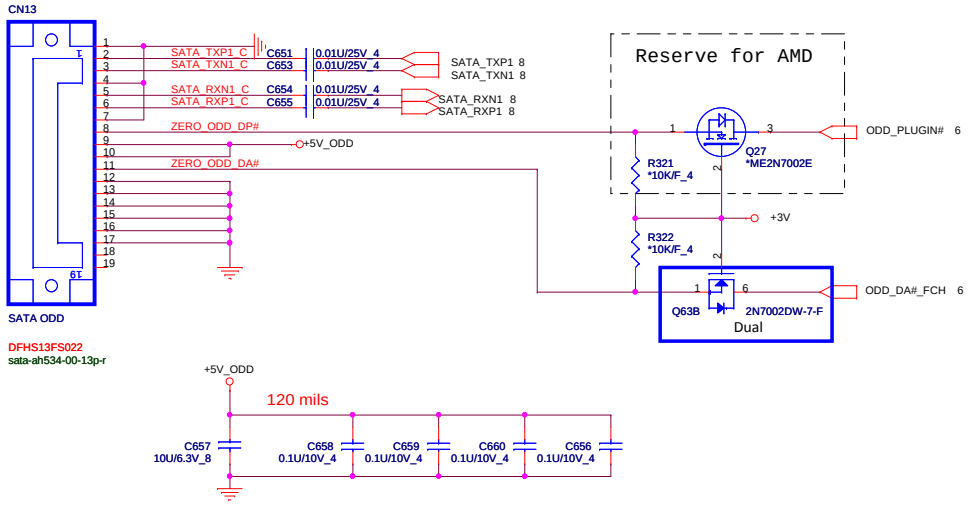
SATA HDD CONNECTOR

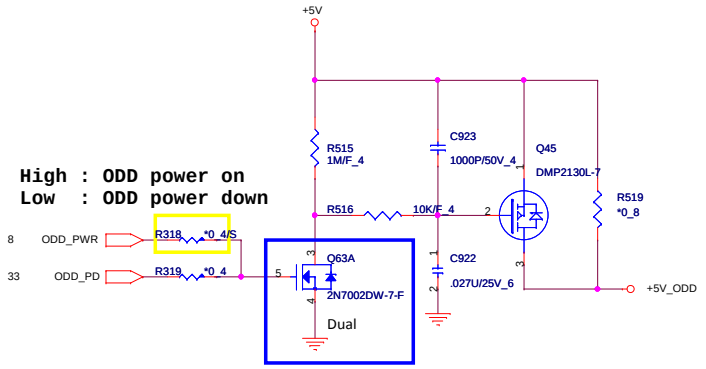
Bypass CAP close conn



SATA ODD CONNECTOR

SATA ODD





SI , Q28,Q43 change to dual type MOS Q63

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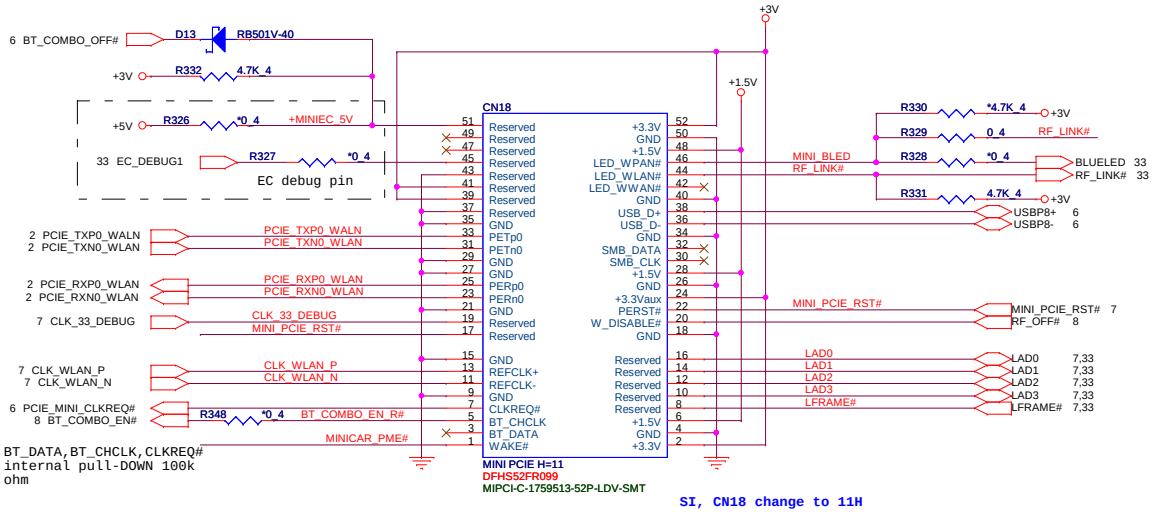
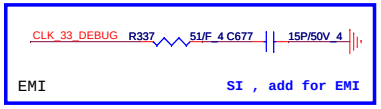
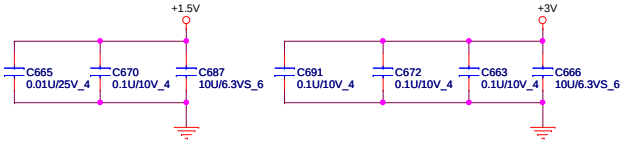
Mini PCI-E Card 1 WLAN

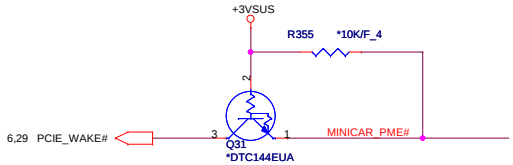


SI, CN18 change to 11H



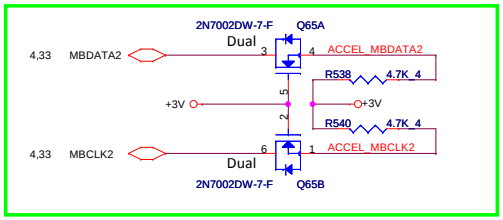


INTEL WLAN CARD PIN 20 W_DISABLE# have internal pull-up 110k ohm

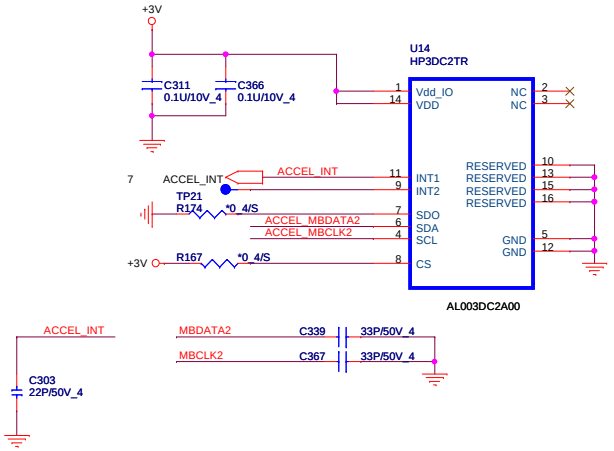


2,4,11,23,38,41 +1.5V
2,4,6,8,9,10,11,12,13,14,18,23,24,25,26,27,28,29,30,31,33,41,42,44 +3V
4,7,30,33,34,35 +3VPCU
8,18,24,25,26,27,30,31,41 +5V

Accelerometer Sensor



SI2 , add for avoid leakage from SUS power



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Size	Document Number	Rev
Custom	MINI PCIE & G-sensor	1A
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ITE pin 100 , 104 , 106 default can not pull up to +3VPCU it will cause chip into test mode

+3VPCU CAP close to EC pin

Smart adapter Type check

Change to 1SS355 as Current loss

D18 1SS355

Change to RB500 as Current loss

500mA

SI , del QB button PU resistor R392

SI2,change to +3VS5 for leakage issue

For +VIN noise

Vender	Size	P/N
AMIC	4M	AKE39F-0800
EON	4M	AKE39ZN0Q02
Socket		DFHS08FS023

4M SPI EC ROM

U20 EN25Q32B-104HIP AKE39ZN0Q02 SOIC8-8-1_27

SI , add for EMI

128K byte SPI EC ROM

U19 *DFHS08FS023 SOIC8-6-1_27

ICT need TP2675 size test point

TP place on top lay for ICT request

Adapter select

Hi ==> DIS/SG
Low ==>UMA

Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W

IT8518E/HX

AJ085180F04

SI, remove NUMLED#

Add TP SMBUS signal

Add G-sensor SMBUS signal

For GPU thermal protection

for Battery charge/discharge

for CPU themal protection

SI , drop QB button feature

from power button

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Size	Document Number	Rev
Custom	EC (KB3926)/ROM	1A

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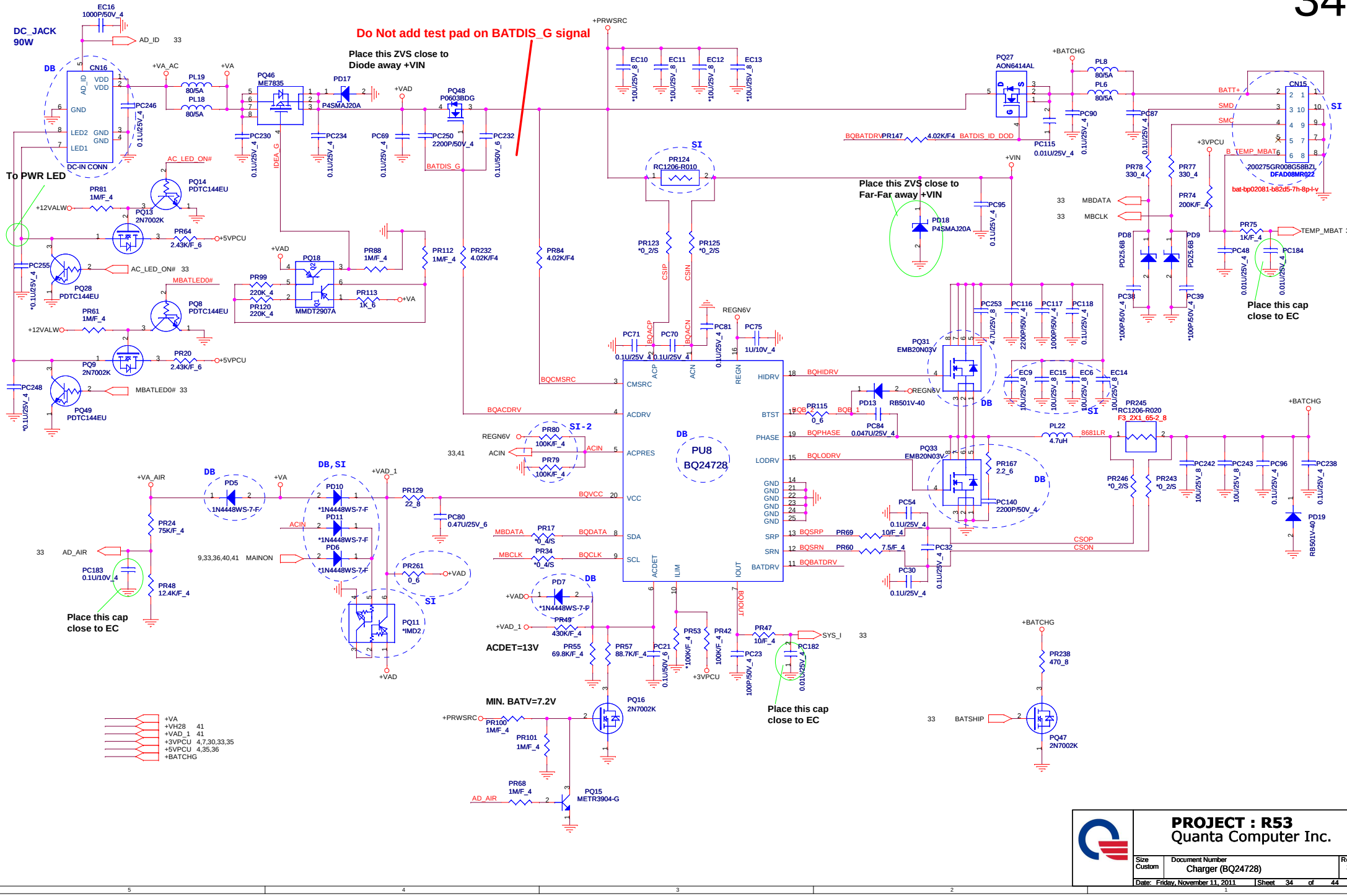
DC_JACK
90W
DB
CN16
DC-IN CONN
To PWR LED
Do Not add test pad on BATDIS_G signal
Place this ZVS close to
Diode away +VIN
Place this ZVS close to
Far-Far away +VIN
Place this cap
close to EC
Place this cap
close to EC
Place this cap
close to EC
ACDET=13V
MIN. BATV=7.2V
PU8
BQ24728
SI-2
DB,SI
+PRWSRC
+BATCHG
+VIN
+VA
+VAD
+3VPCU
+5VPCU
+12VALW
REGN6V
SYS_I
BATSHIP
PROJECT : R53
Quanta Computer Inc.
Charger (BQ24728)
Size Custom
Rev 1A
Date: Friday, November 11, 2011
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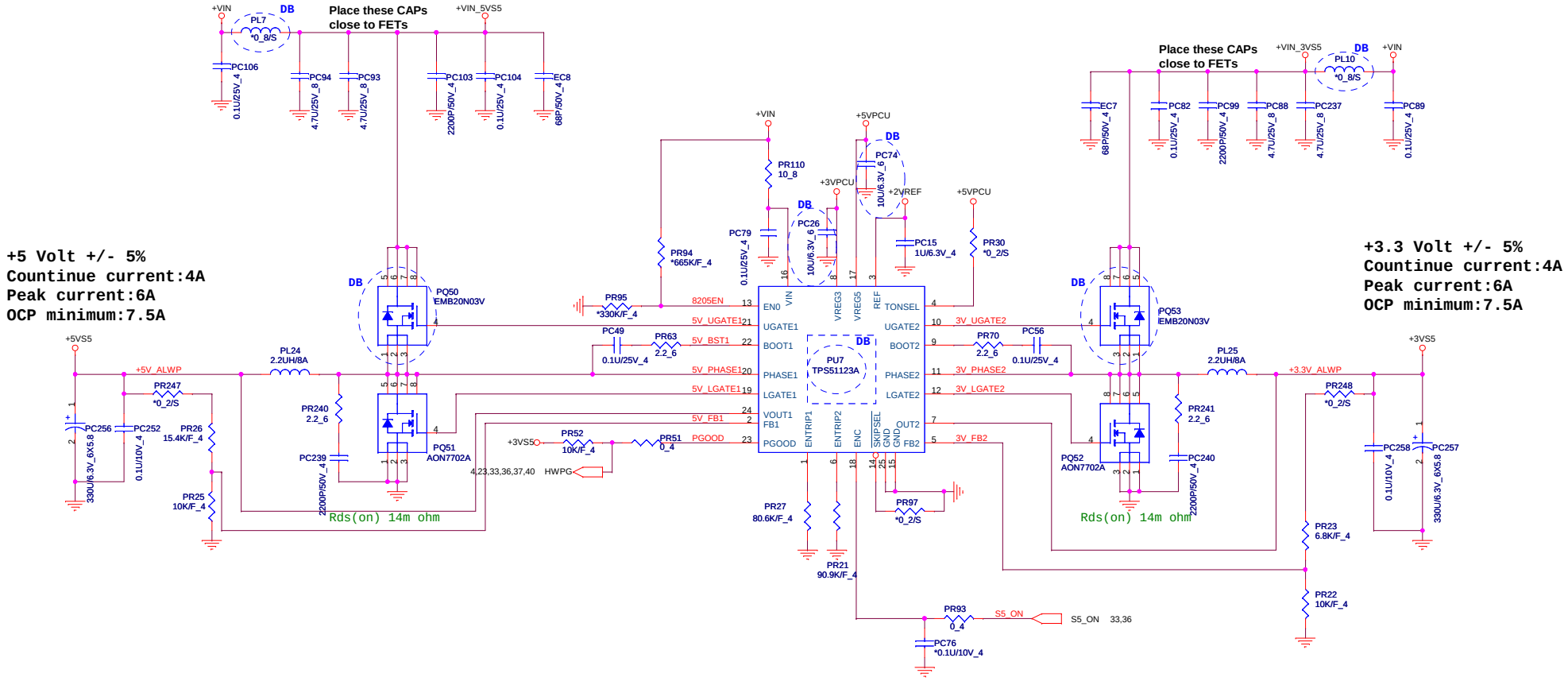
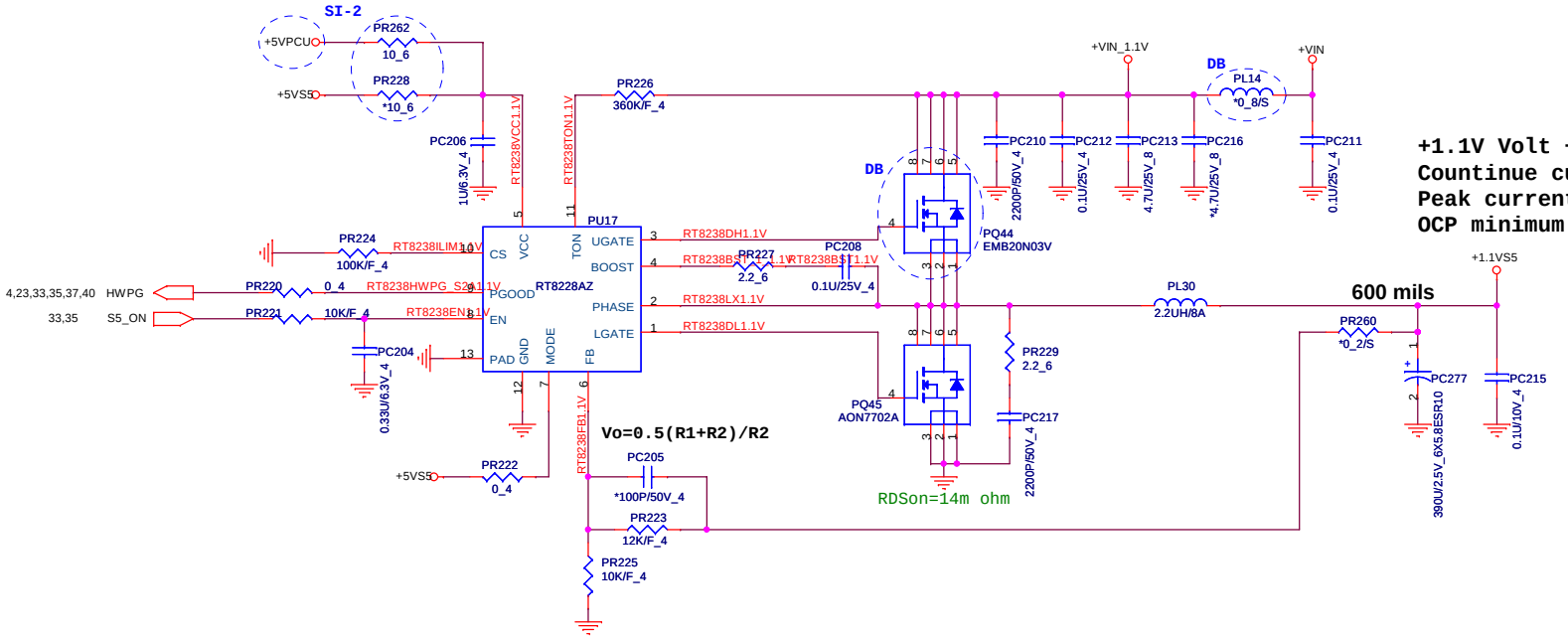
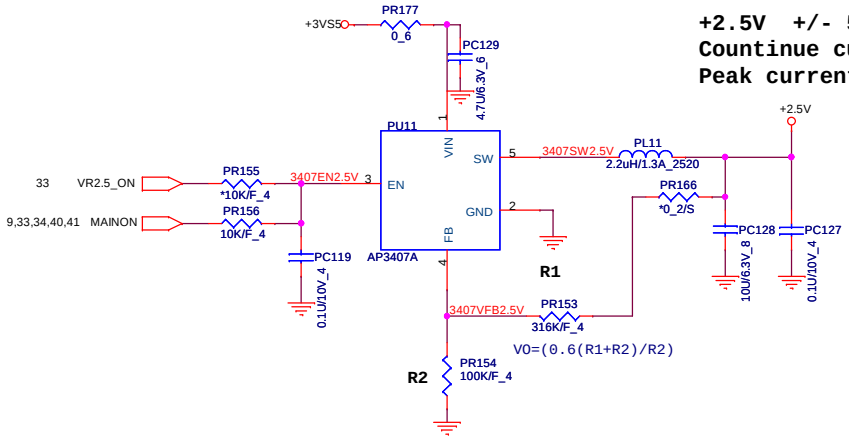

+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A
Place these CAPs close to FETs
Place these CAPs close to FETs
PU7 TPS51123A
PQ50 EMB20N03V
PQ51 AON7702A
PQ52 AON7702A
PQ53 EMB20N03V
Rds(on) 14m ohm
Rds(on) 14m ohm
DB for prevent interference



+1.1V Volt +/- 5%
Countinue current:5A
Peak current: 6.5A
OCP minimum:7.5A



+2.5V +/- 5%
Countinue current:0.3A
Peak current:0.75A

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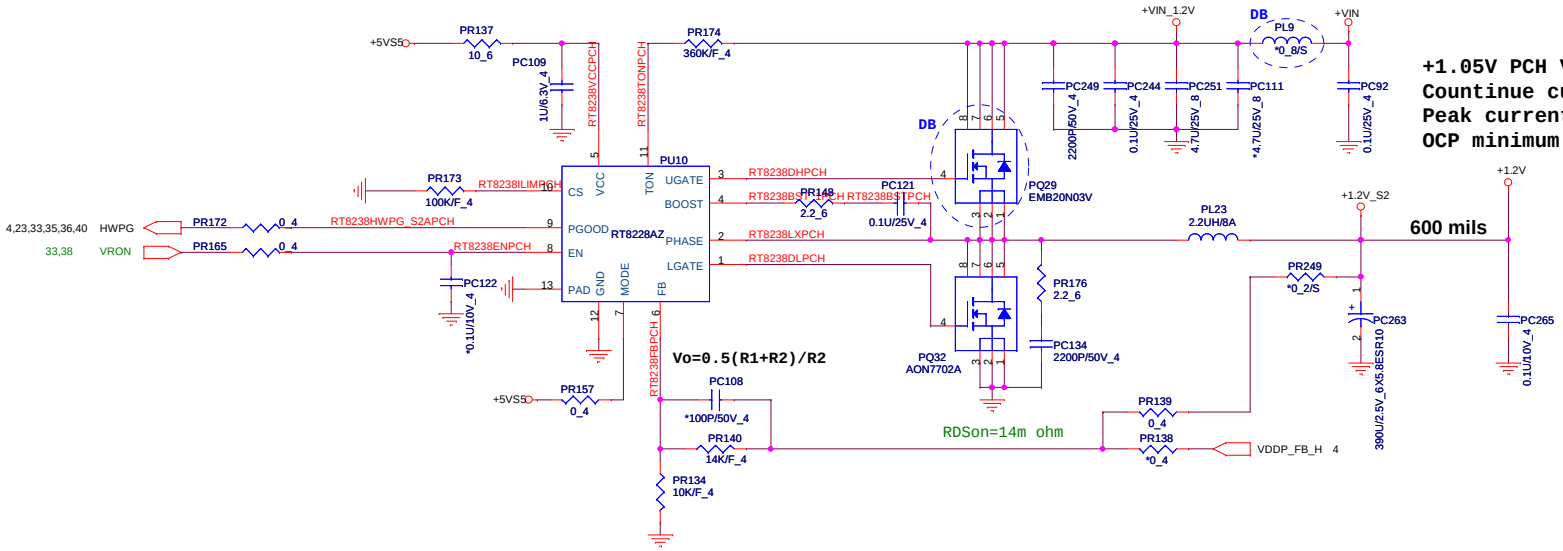
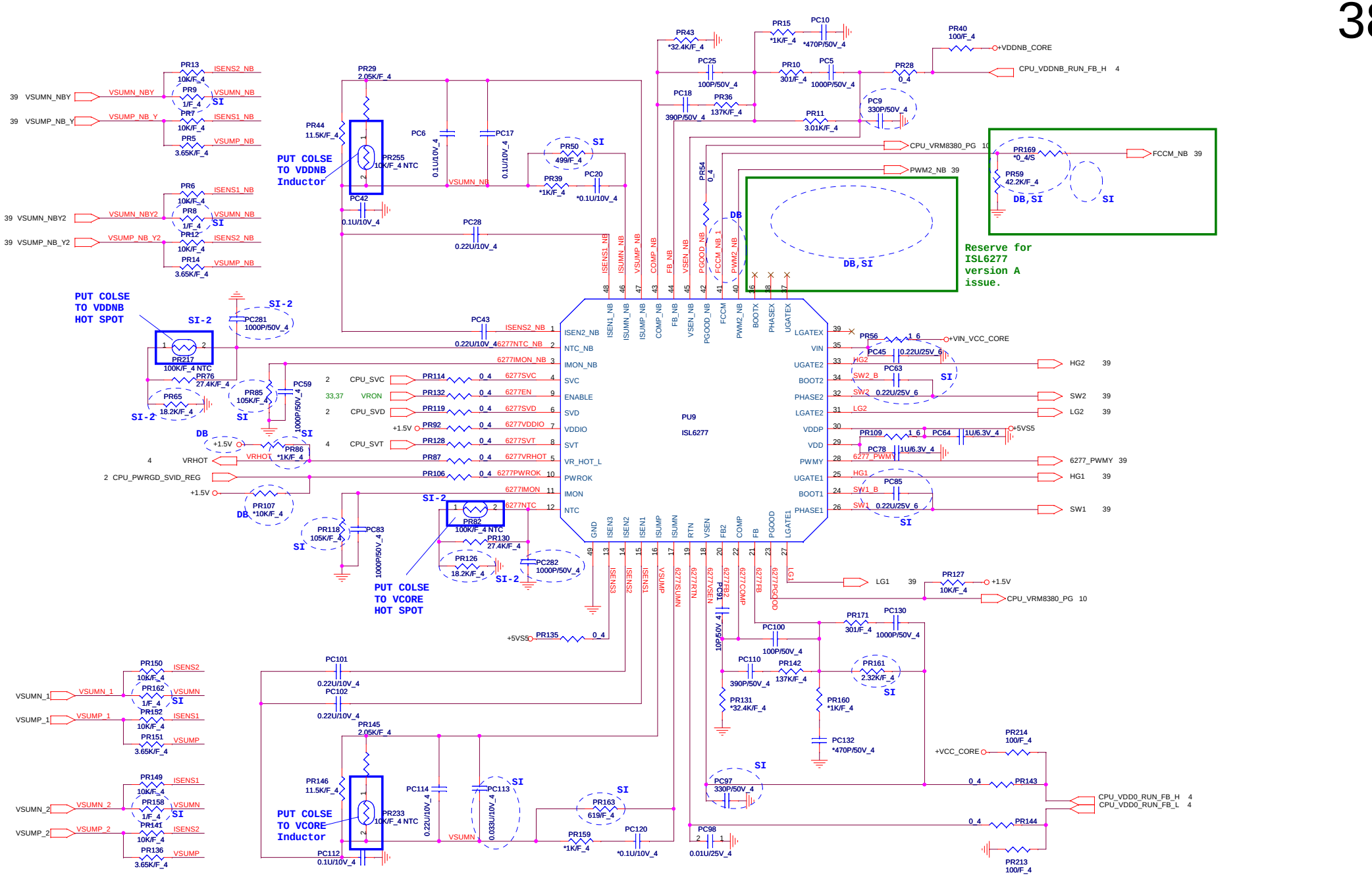
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1VS5 (RT8228)/2.5V	1A
Date: Friday, November 11, 2011	Sheet 36 of 44	



PROJECT : R53	
Quanta Computer Inc.	
Size: Custom	Document Number: +1.2V (RT8228)
Rev: 1A	
Date: Friday, November 11, 2011	Sheet 37 of 44


PU9
ISL6277
Reserve for ISL6277 version A issue.
PUT COLSE TO VDDNB Inductor
PUT COLSE TO VDDNB HOT SPOT
PUT COLSE TO VCORE HOT SPOT
PUT COLSE TO VCORE Inductor
DB
SI
SI-2
DB,SI
ISEN2_NB
NTC_NB
IMON_NB
SVC
ENABLE
SVD
VDDIO
SVT
VR_HOT_L
PWROK
IMON
NTC
LGATEX
VIN
UGATE2
BOOT2
PHASE2
LGATE2
VDDP
VDD
PWMY
UGATE1
BOOT1
PHASE1
GND
ISEN3
ISEN2
ISEN1
ISUMP
ISUMN
RTN
VSEN
FB2
COMP
FB
PGOOD
LGATE1
+VDDNB_CORE
+VIN_VCC_CORE
+VCC_CORE
+5VS5
+1.5V
CPU_VDDNB_RUN_FB_H
CPU_VRM8380_PG
CPU_VDD0_RUN_FB_H
CPU_VDD0_RUN_FB_L
PROJECT : R53
Quanta Computer Inc.
Size Custom
Document Number ISL6277
Rev A
Date: Friday, November 11, 2011
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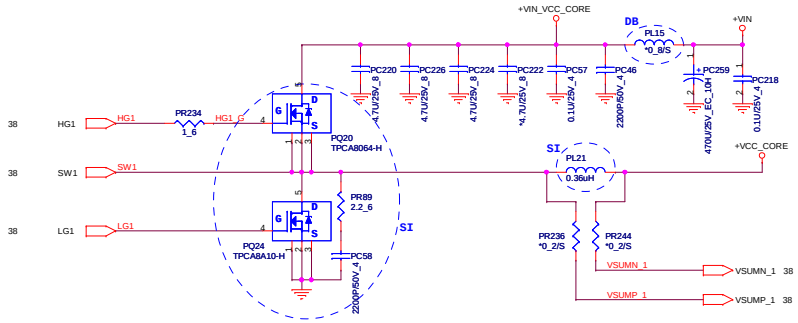
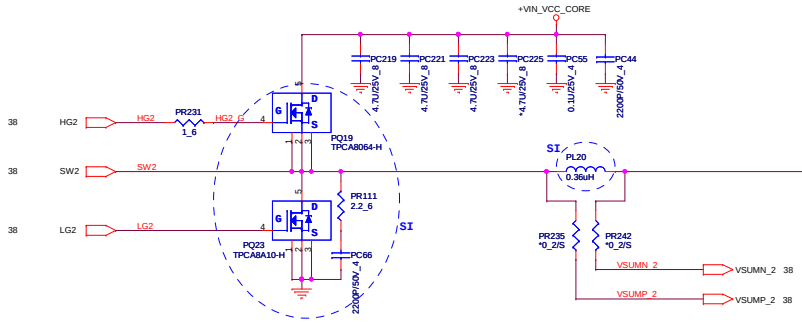
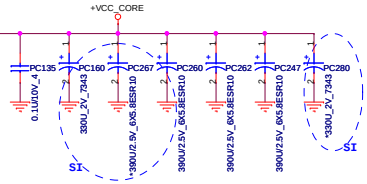
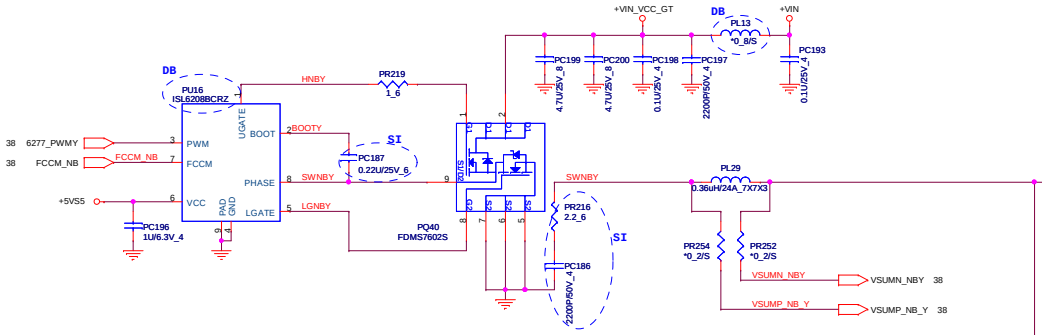
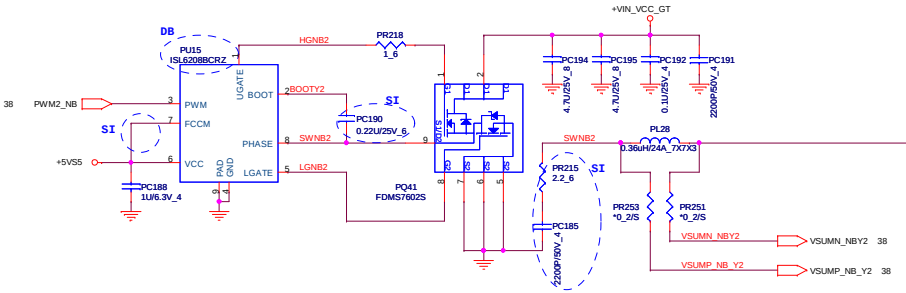




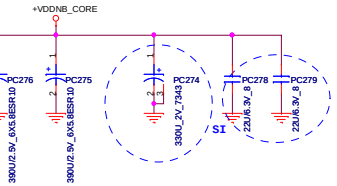
CPU CORE Volt
Countinue current:36A
Peak current:50A
OCP minimum:60A







VDDNB Volt
Countinue current:25A
Peak current:33A
OCP minimum:40A



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Size	Document Number	Rev
Custom	ISL6208	1A
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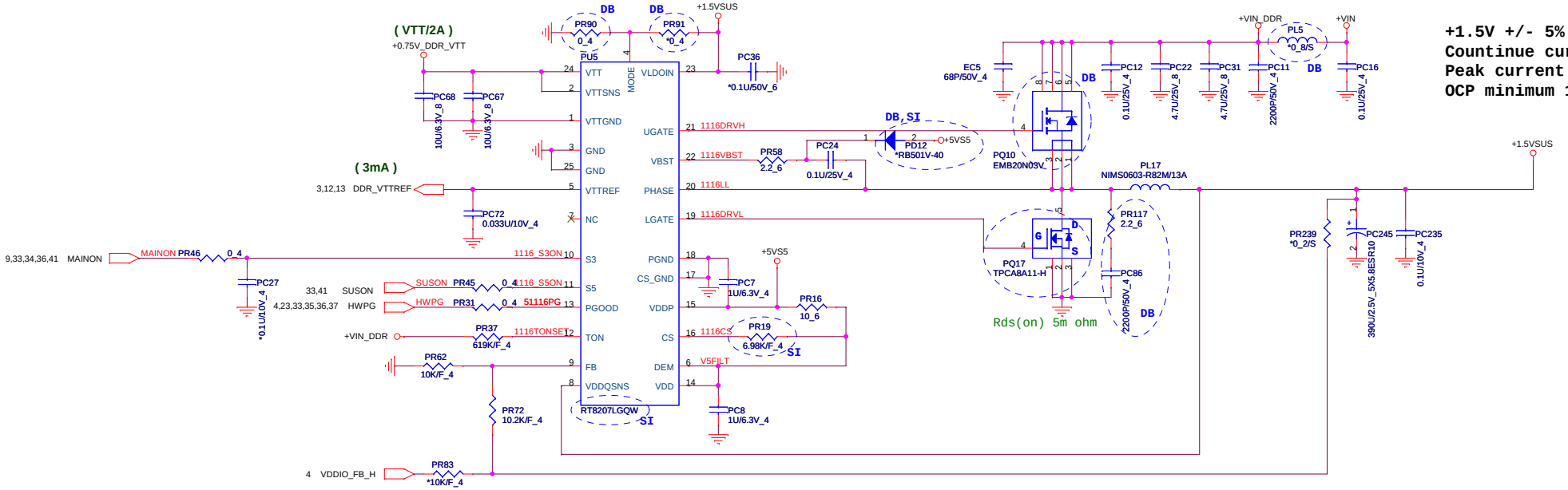

+1.5V +/- 5%
Countinue current:10A
Peak current:12A
OCP minimum 15A

Size: Custom	Document Number: DDRIII(G5616)	Rev: 1A
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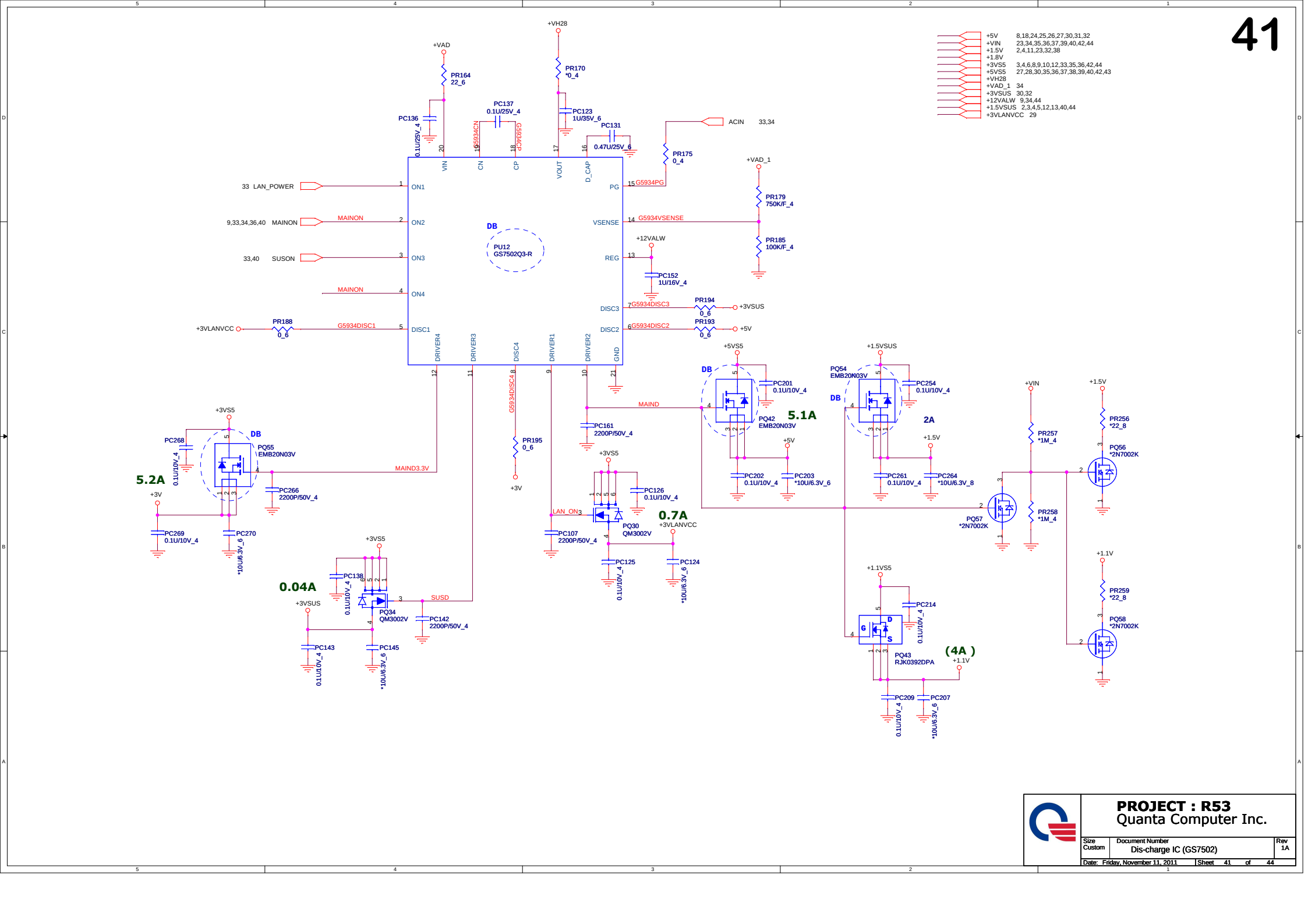

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (GS7502)	1A

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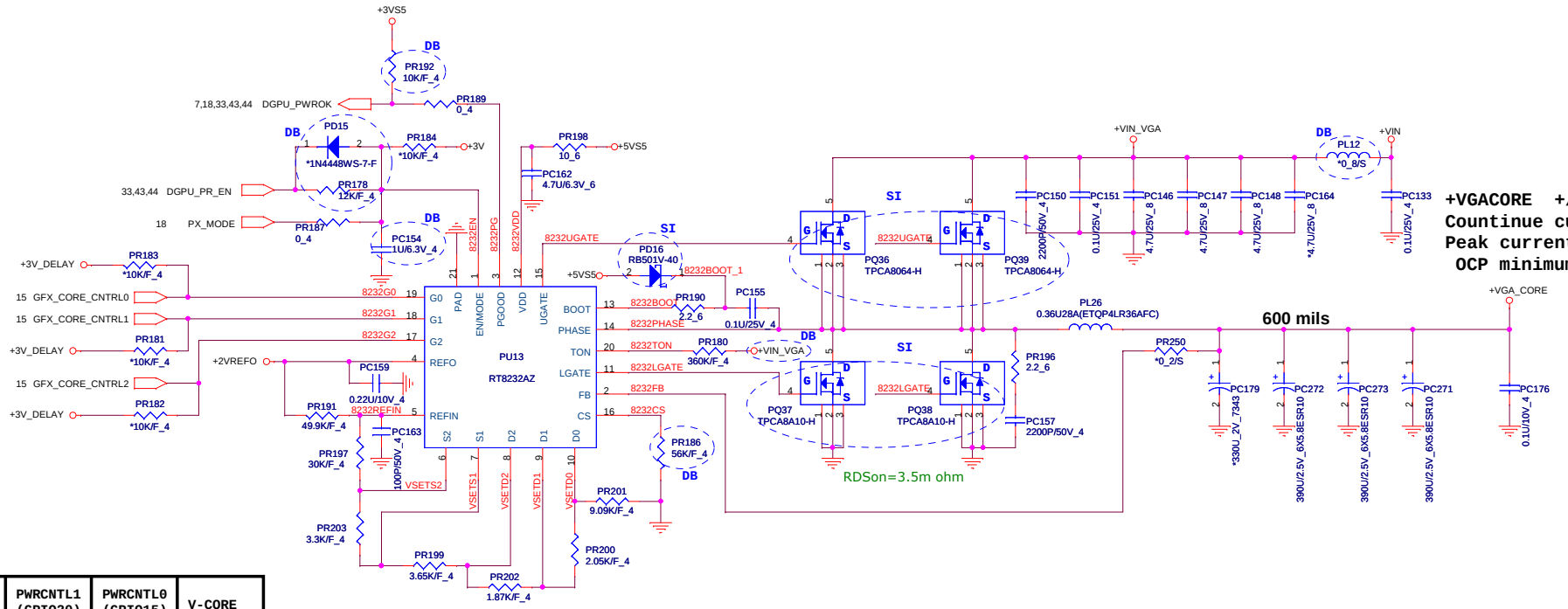
VGA Core



+VGACORE +/- 5%
Countinue current:20A
Peak current:23A
OCP minimum 33A

Symour-XT	PWRCNTL2 (GPIO16)	PWRCNTL1 (GPIO20)	PWRCNTL0 (GPIO15)	V-CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V

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Size	Document Number	Rev
Custom	+VGACORE (RT8232AZ)	1A

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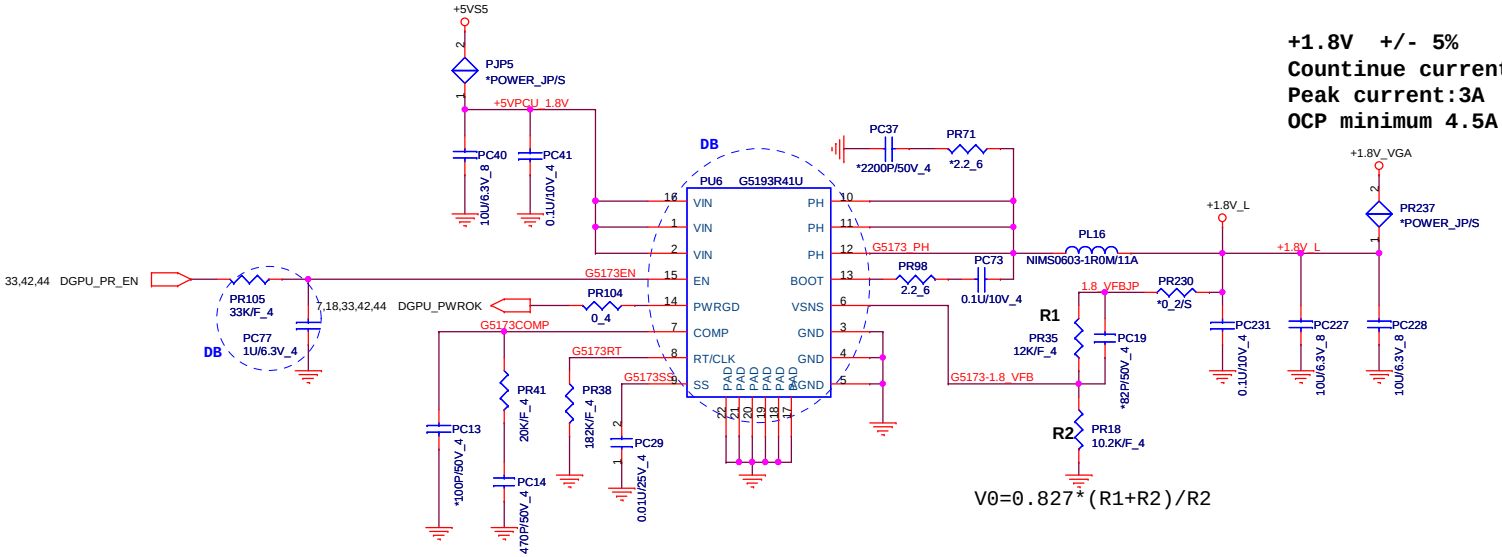
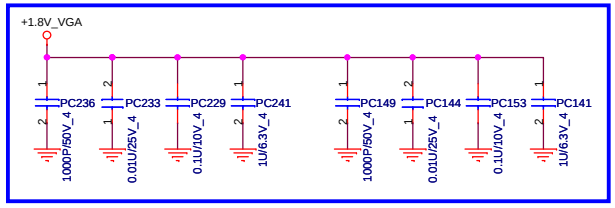


+1.8V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A

DB for prevent interference



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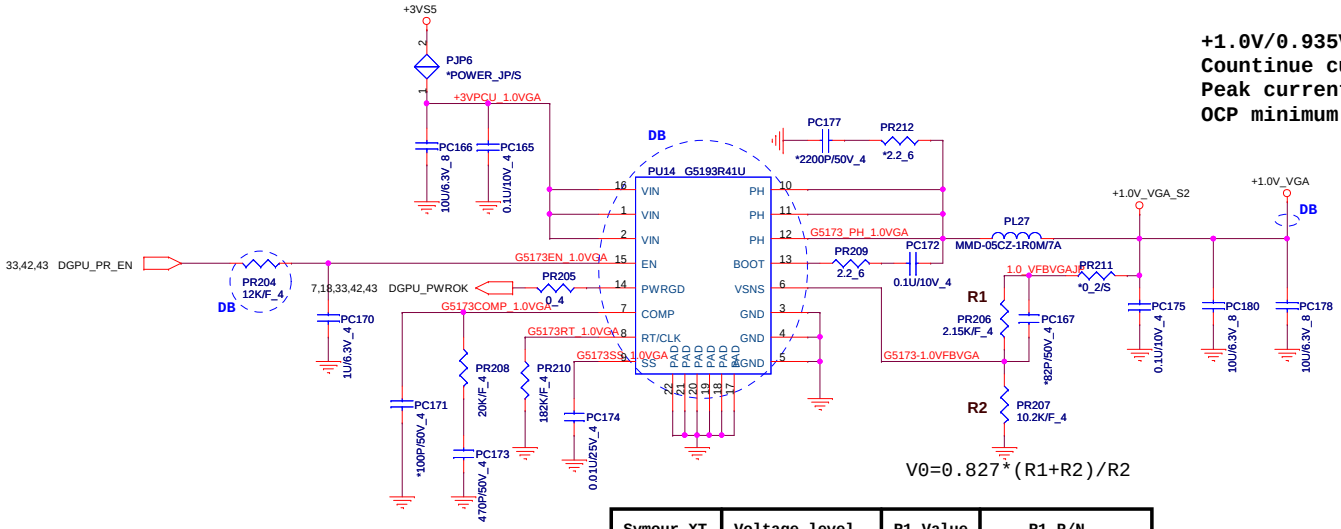
Size	Document Number	Rev
Custom	+1.8V_VGA (G5193)	1A
Date: Friday, November 11, 2011	Sheet 43 of 44	

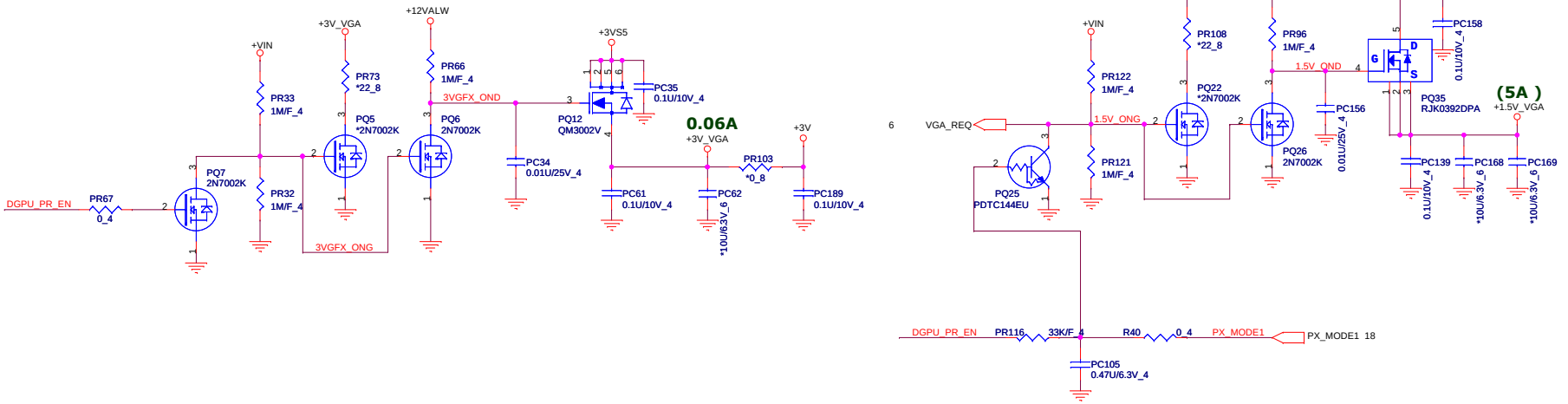
+1.0V/0.935V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A

+3V 2,4,6,8,9,10,11,12,13,14,18,23,24,25,26,27,28,29,30,31,32,33,41,42
+VIN 23,34,35,36,37,39,40,41,42
+3VS5 3,4,6,8,9,10,12,33,35,36,41,42
+5VS5 27,28,30,35,36,37,38,39,40,41,42,43
+3V_VGA 18,30
+12VALW 9,34,41
+1.5VSUS 2,3,4,5,12,13,40,41
+1.5V_VGA 18,20,21,22



V0=0.827*(R1+R2)/R2

Symour-XT	Voltage level	R1 Value	R1 P/N
17W	1.0V	2.15K	CS22152FB07
25W	0.935V	1.37K	CS21372FB19



PROJECT : R53
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Size	Document Number	Rev
Custom	+1.0V_VGA (G5193)	1A
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