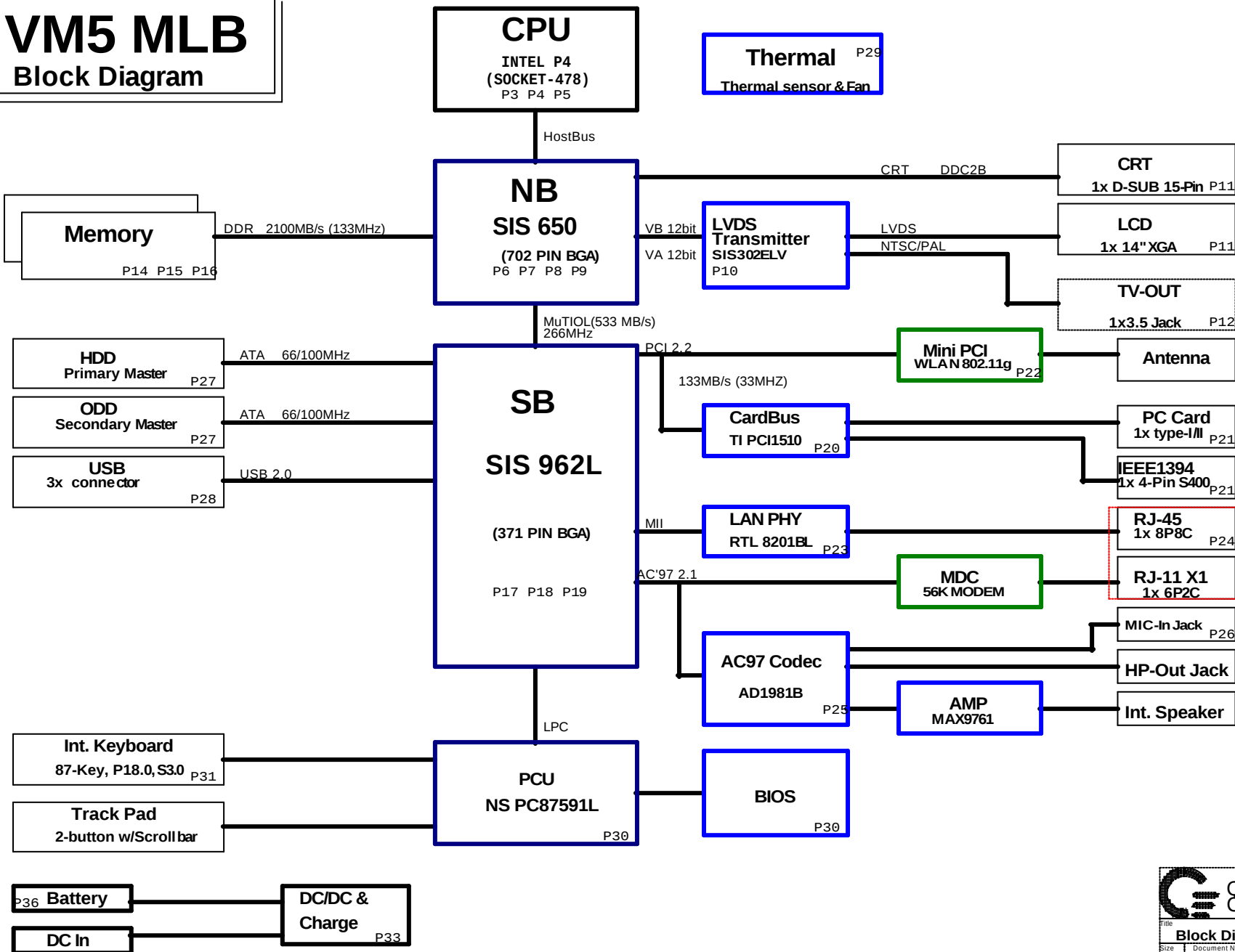


VM5 MLB

Block Diagram

01



Page List

01 Block Diagram
02 Page List
03-CELERON-1/3
04-CELERON-2/3
05-CELERON-3/3

06-NB-SIS650-1/4
07-NB-SIS650-2/4
08-NB-SIS650-3/4
09-NB-SIS650-4/4
10-LVDS Interface

11-CRT Port & LCD Connector
12-Hardware Trap
13-Clock generator
14-DDR Terminator
15-DDR SODIMMX2

16-DDR SDRAM(on board)
17-SB-SIS962L-1/3
18-SB-SIS962L-2/3
19-SB-SIS962L-3/3
20-PCI1510GVF

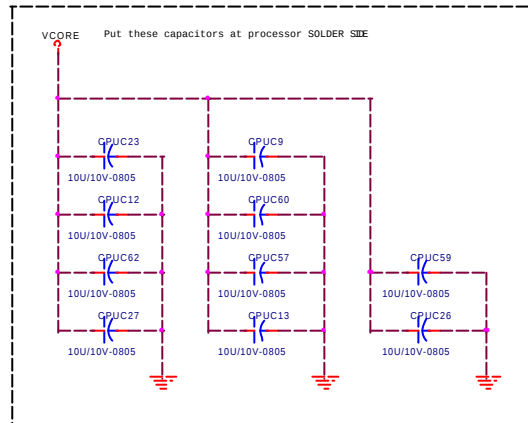
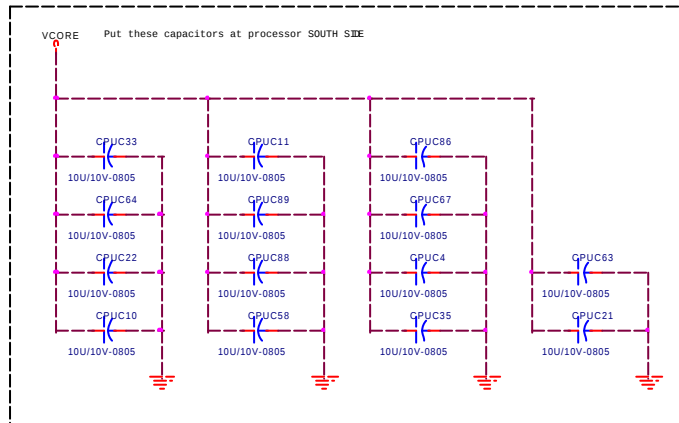
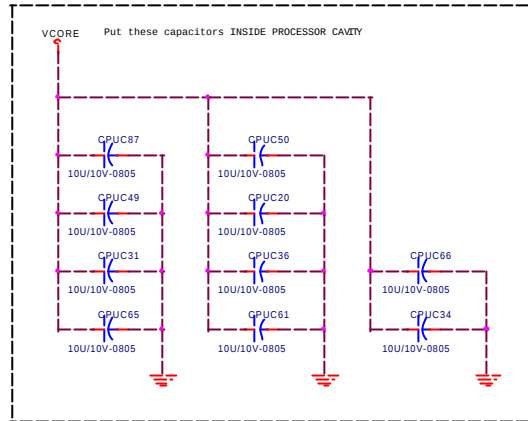
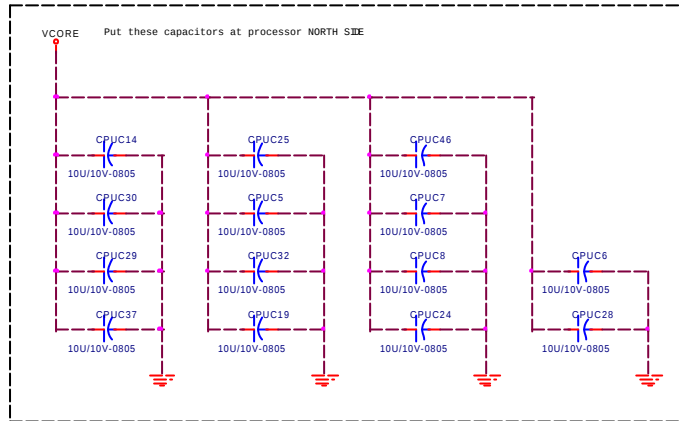
21-PCMCIA SOCKET & POWER
22-Mini PCI & MDC
23-LAN Phy. RTL8201
24-TP and Lan Connector(CK)
25-Audio CODE

26-Audio AMP
27-HDD,ODD Connector
28-USB Connector
29-RTC & Thermal IC,FAN
30-PCU-87591 & BIOS

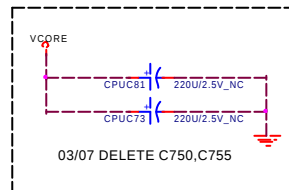
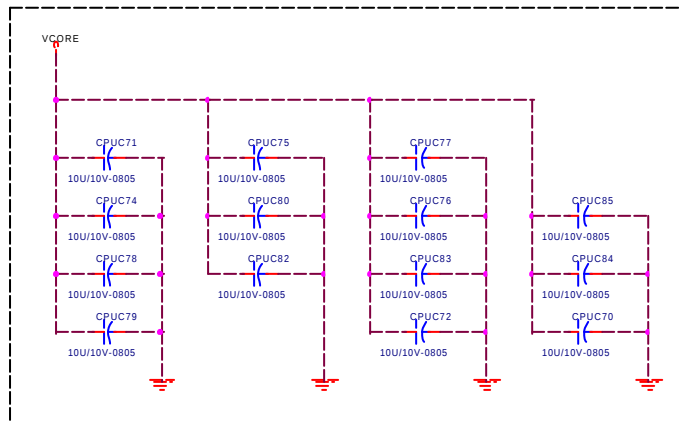
31-Internal K/B & Screw
32-PCI Bus Glue Logic
33- DC/DC 3V/5V
34- 2.5/1.8VSUS & DDRVTT
35- DC/DC VCORE

36- BATTERY CHARGER
37- BATTERY CONNECTOR

		QUANTA COMPUTER	
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P.S. Choose X7R/X5R components instead of Y5V for all 10uF_1206 capacitors on this page.



Title		SOCKET 478 -3	Rev	1A
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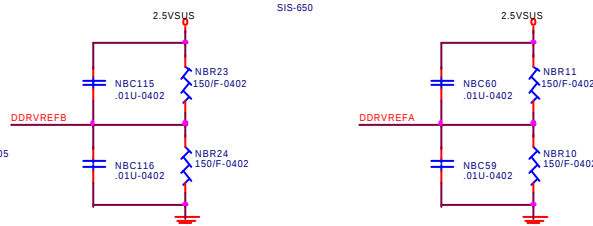
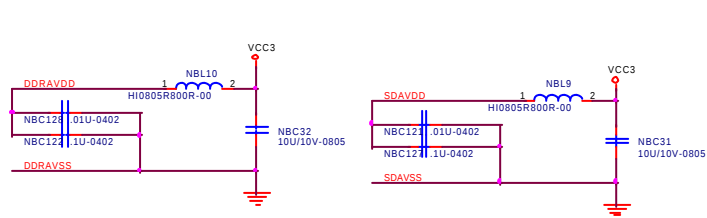
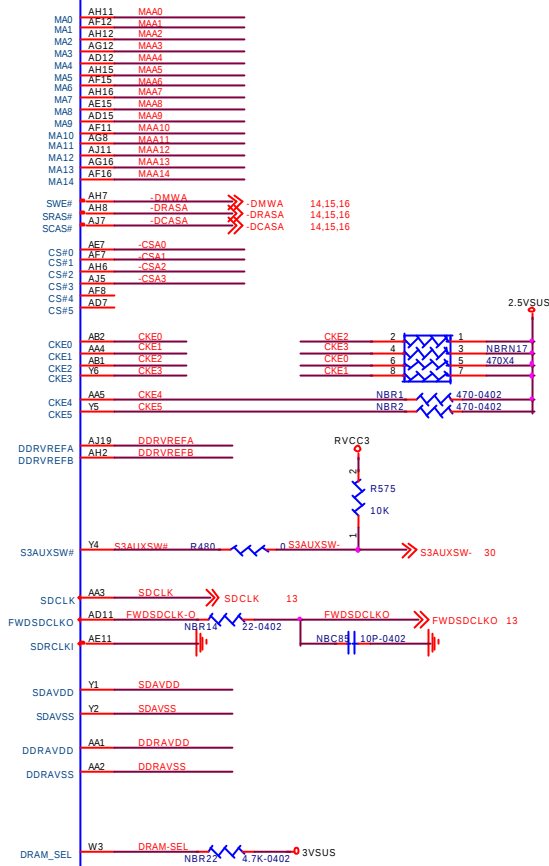
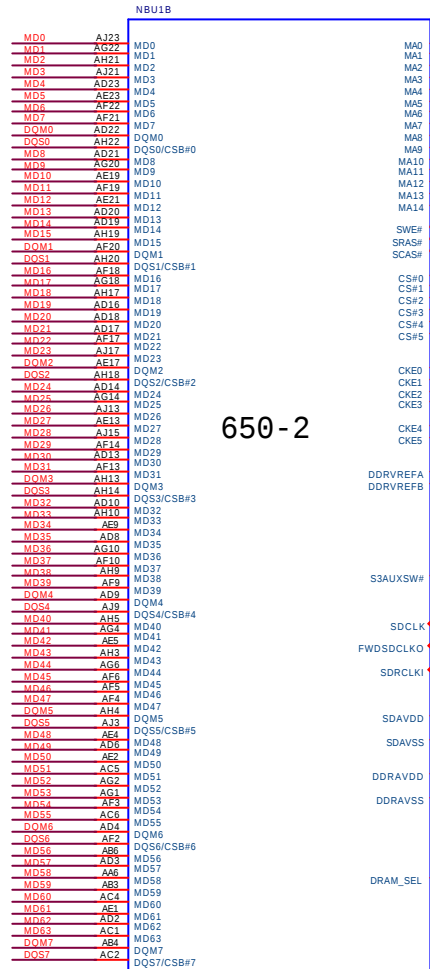
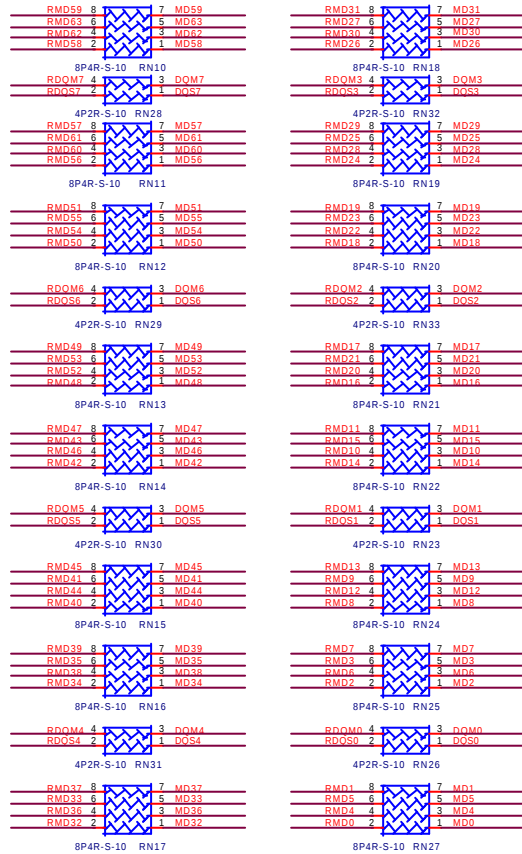
AGP

650-1

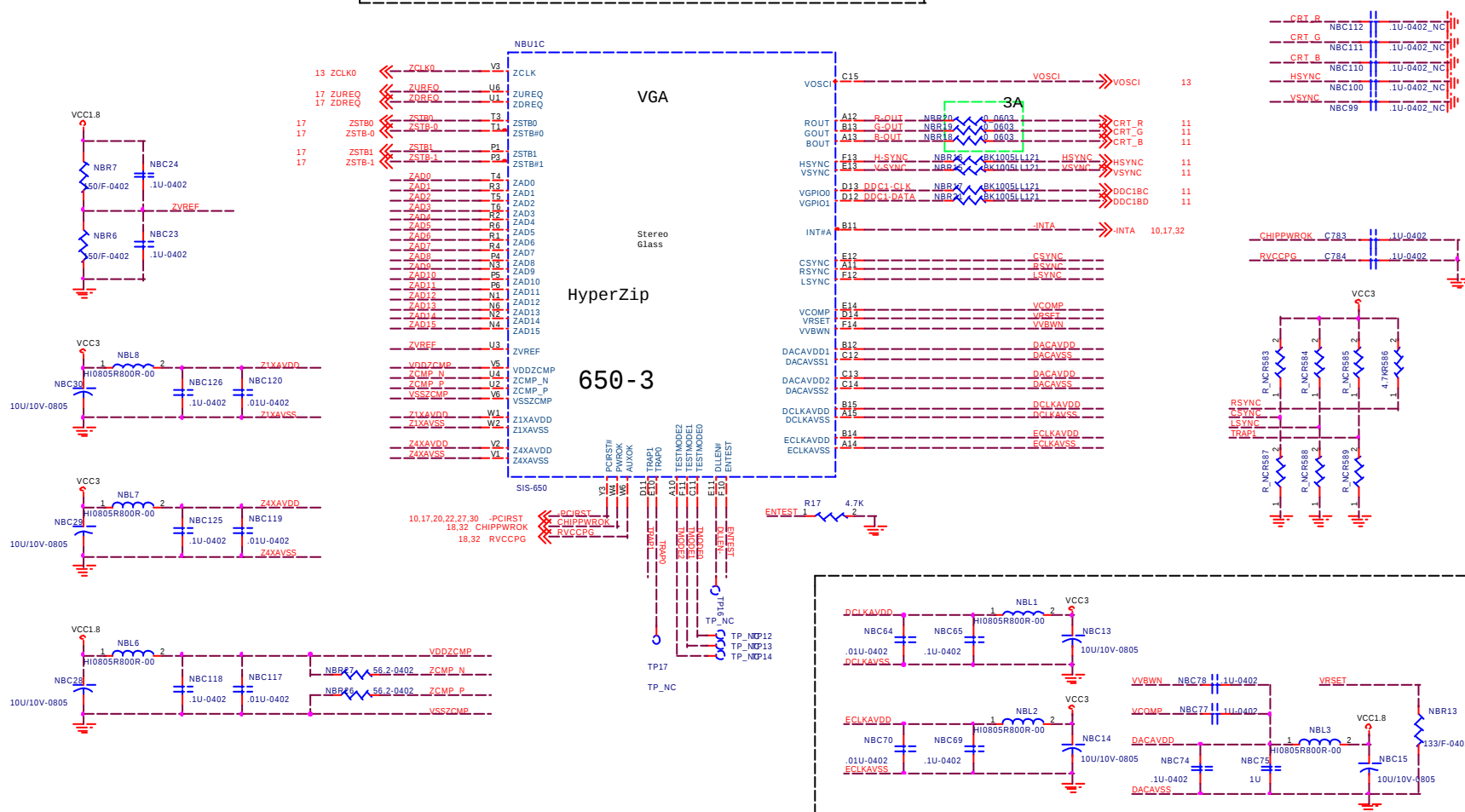
HOST



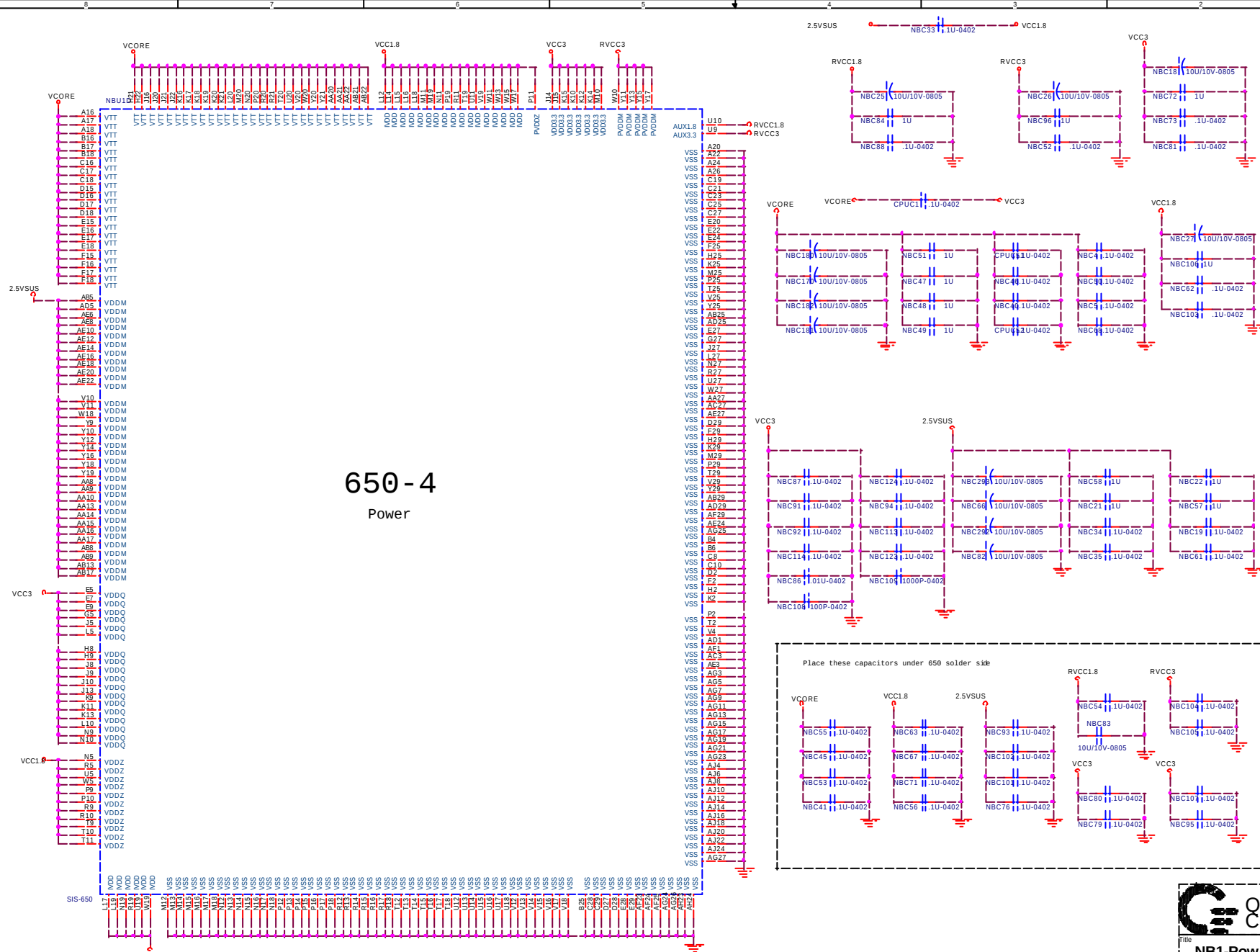
Title			Rev
NB1-HOST/AGP			1A
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Custom	VM5 Main Board		
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NB Hardware Trap Table				embedded pull-low (30-50K Ohm)
	0	1	Default	
DCLEN	enable PLT	disable PLT	0	yes
WDRSEL	WDR	WDR	0	yes
TRAP0	enable	disable	1 (000)	yes
TRAP1	enable	disable	0	yes
CSYNC	enable VB	enable VB	0	
ESYNC	enable VGA interrupt	enable VGA interrupt	1	
LSYNC	enable same link	enable same link	0	



Title NB1-HyperZip/VGAMisc.			
Size Custom	Document Number VM5 Main Board	Rev 1/	
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302ELV/302LV



Title
LVDS interface

Size Document Number

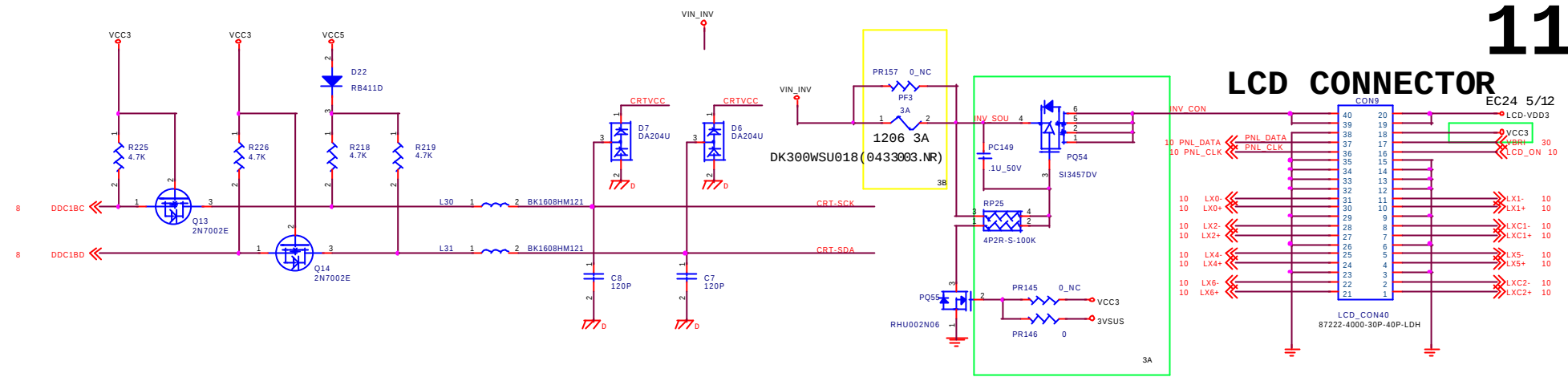
Custom VM5 Main Board

Rev
2A

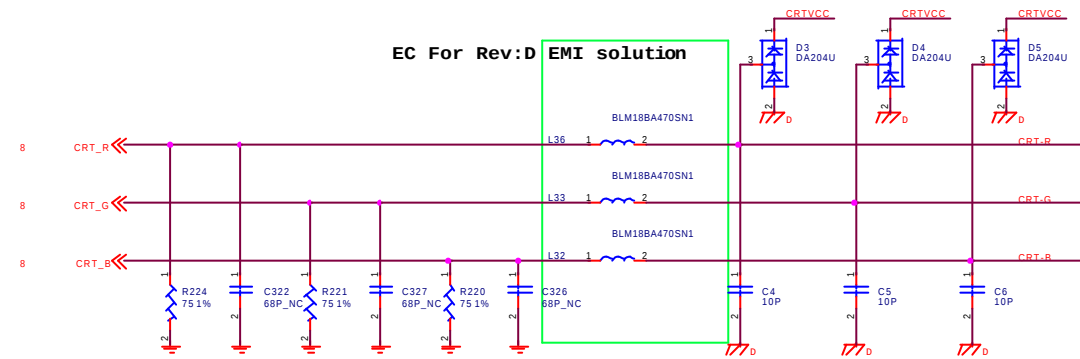
Date: Thursday, April 22, 2004

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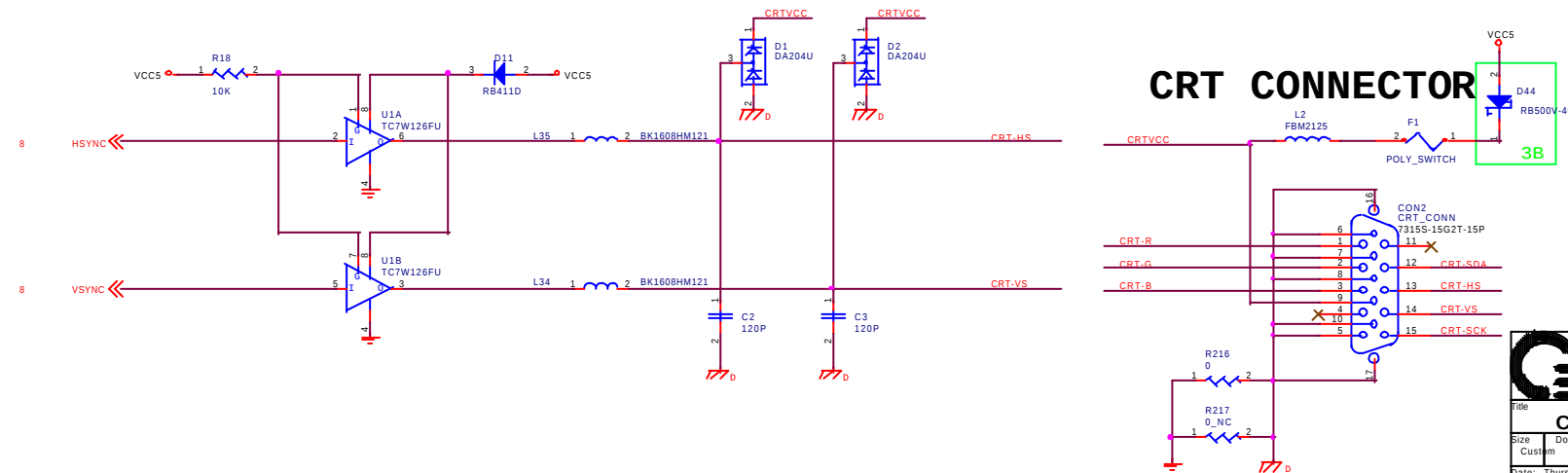
LCD CONNECTOR



EC For Rev:D EMI solution

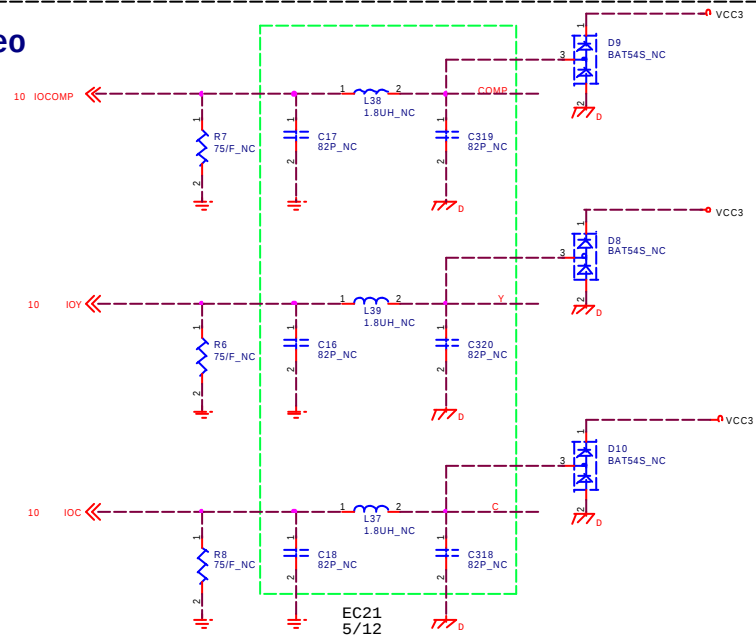


CRT CONNECTOR

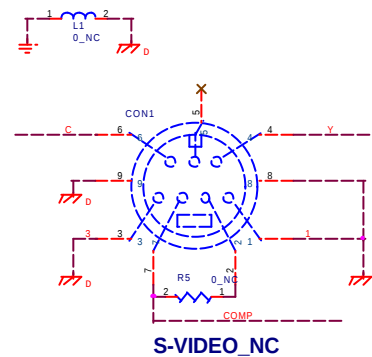


Title			CRT PORT		
Size			Document Number		
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Date			Rev		
Thursday, April 22, 2004			3A		

S-video

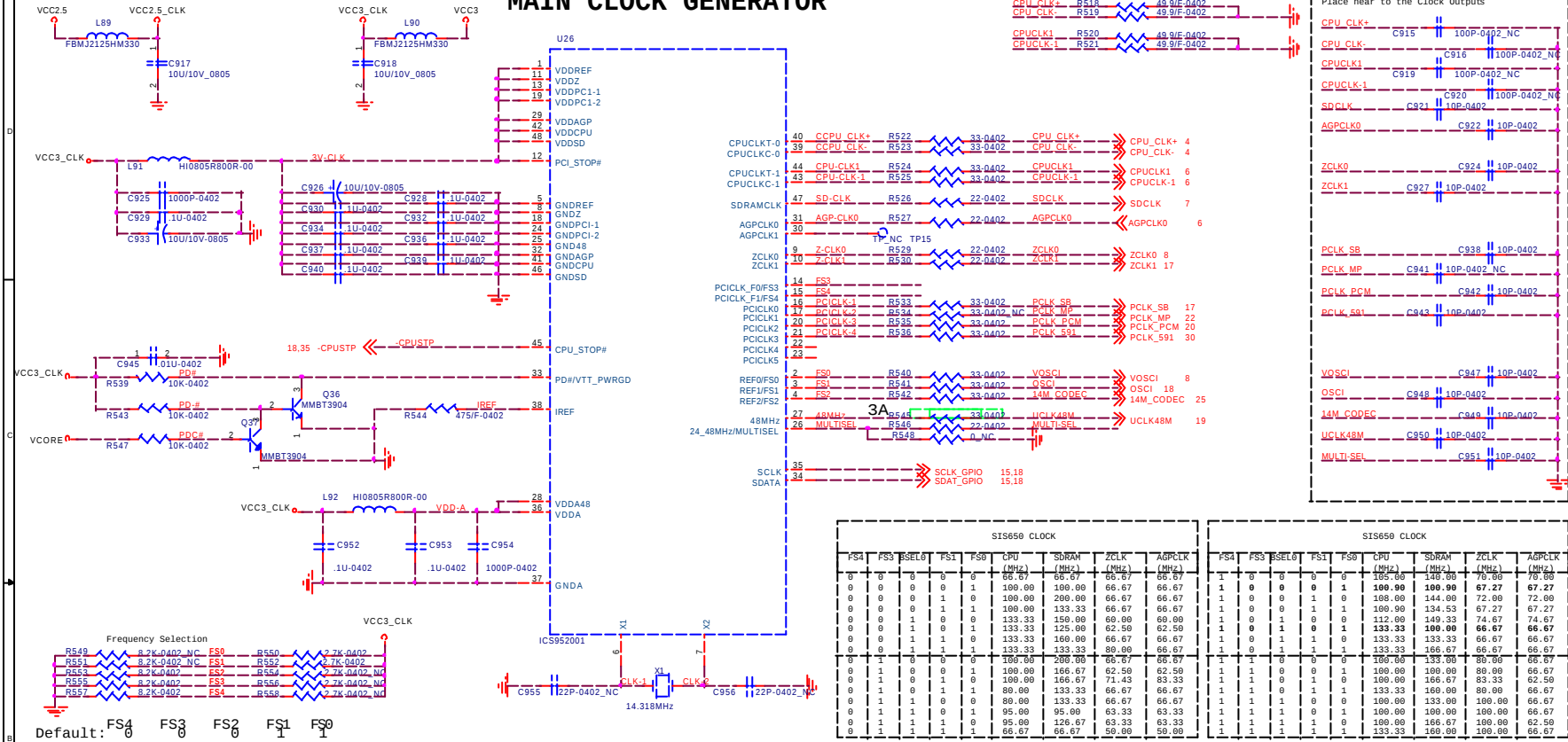


No Stuff for all S_Video Parts



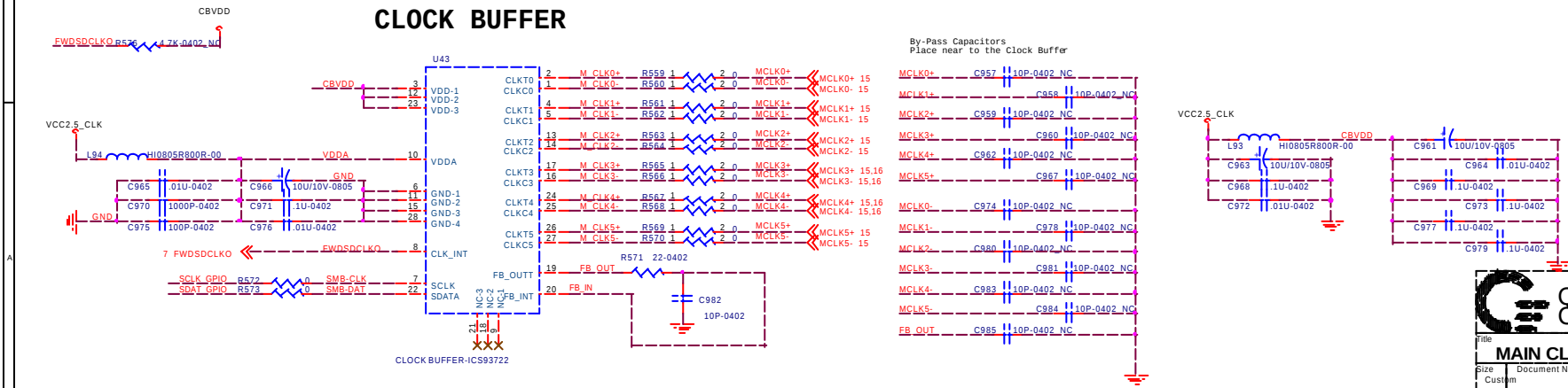
QUANTA COMPUTER	
Hardware Trap & TV-OUT	
Title	Document Number
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VM5 Main Board	
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MAIN CLOCK GENERATOR



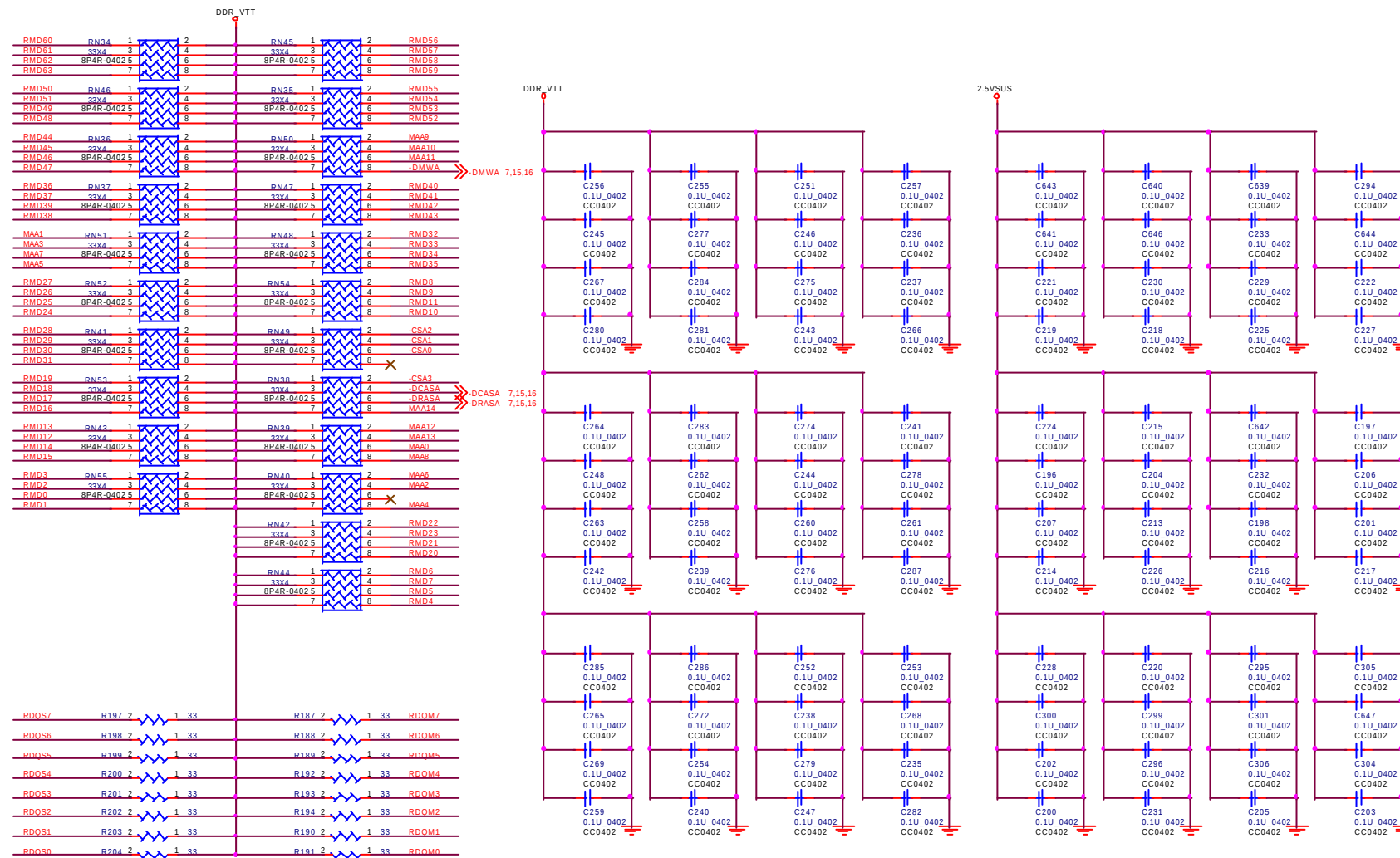
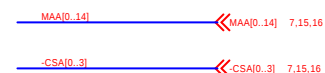
SIS650 CLOCK											
FS4	FS3	BSEL0	FS1	FS0	CPU (MHz)	SDRAM (MHz)	ZCLK (MHz)	AGPCLK (MHz)	FS4	FS3	BSEL0
0	0	0	0	0	66.67	66.67	66.67	66.67	1	0	0
0	0	0	0	1	100.00	100.00	66.67	66.67	1	0	1
0	0	0	1	0	100.00	200.00	66.67	66.67	1	0	0
0	0	0	1	1	100.00	133.33	66.67	66.67	1	0	1
0	0	1	0	0	133.33	150.00	60.00	60.00	1	1	0
0	0	1	0	1	133.33	125.00	62.50	62.50	1	1	1
0	0	1	1	0	133.33	160.00	66.67	66.67	1	0	1
0	0	1	1	1	133.33	133.33	80.00	66.67	1	1	1
0	1	0	0	0	100.00	200.00	66.67	66.67	1	1	0
0	1	0	0	1	100.00	166.67	62.50	62.50	1	1	1
0	1	0	1	0	100.00	166.67	71.43	83.33	1	0	0
0	1	0	1	1	80.00	133.33	66.67	66.67	1	1	1
0	1	1	0	0	80.00	133.33	66.67	66.67	1	1	0
0	1	1	0	1	95.00	95.00	63.33	63.33	1	1	1
0	1	1	1	0	95.00	126.67	63.33	63.33	1	1	1
0	1	1	1	1	66.67	66.67	50.00	50.00	1	1	1

CLOCK BUFFER



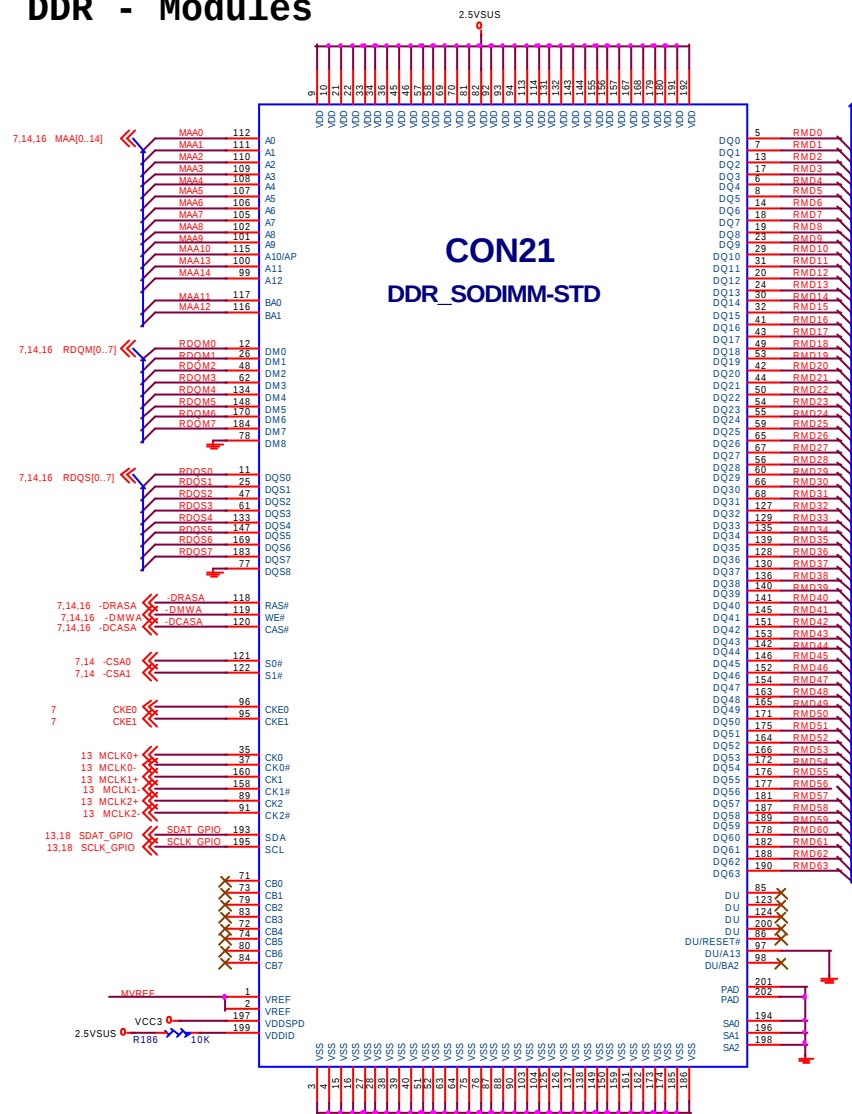
DDR TERMINATOR

14

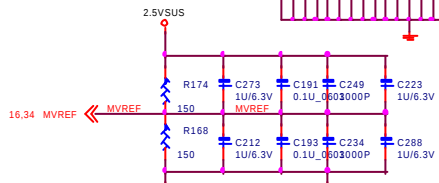
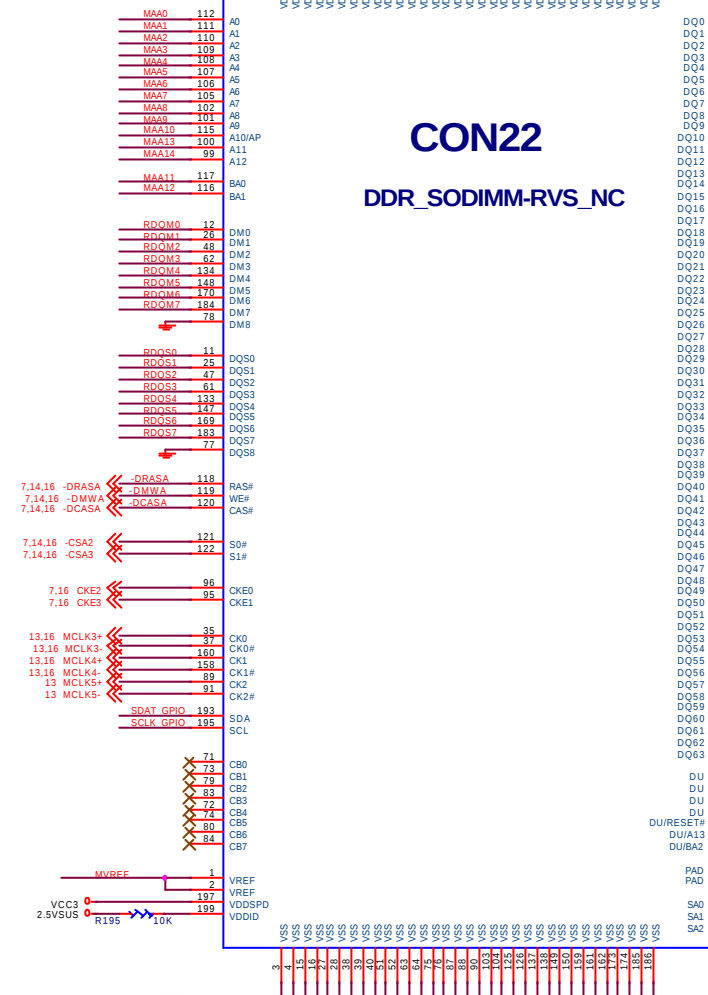


DDR - Modules

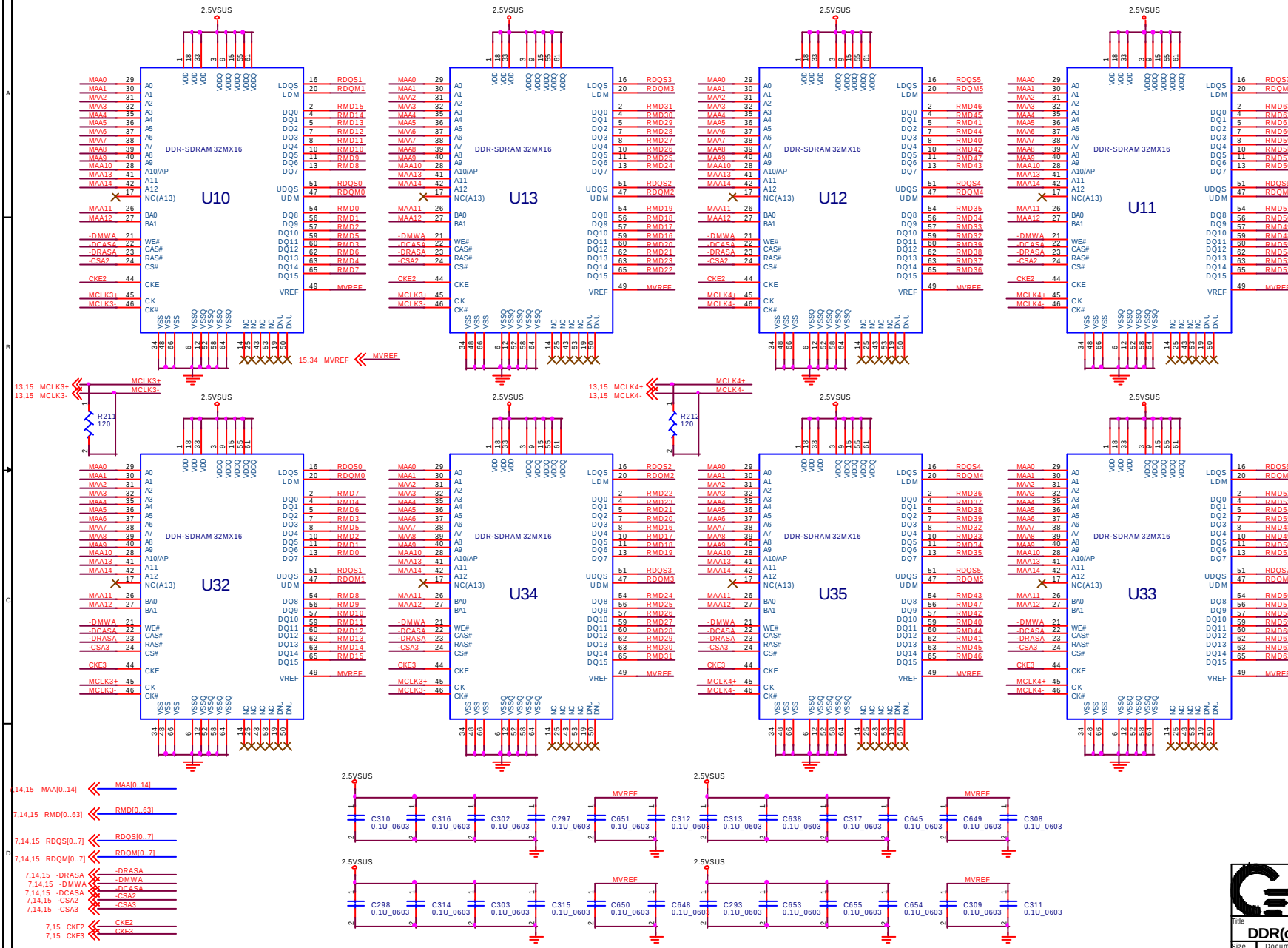
15



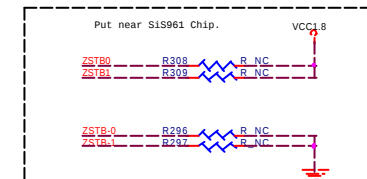
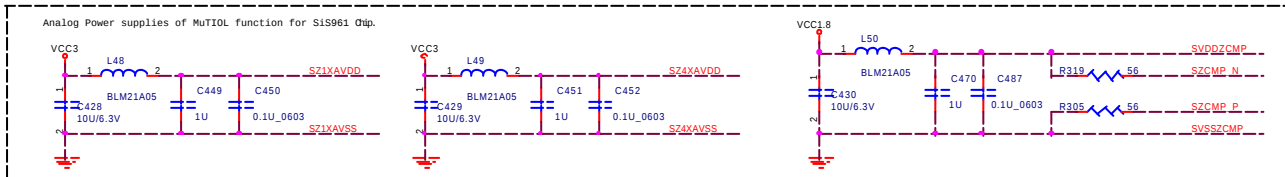
RMD[0..63] >> RMD[0..63] 7.14.16

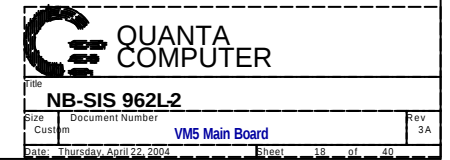


Title		
Memory - SODIMM		
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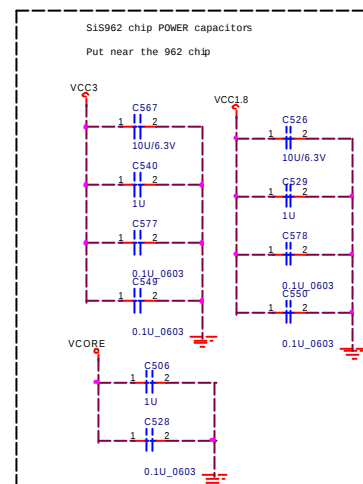
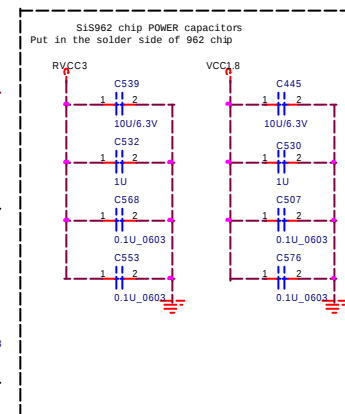
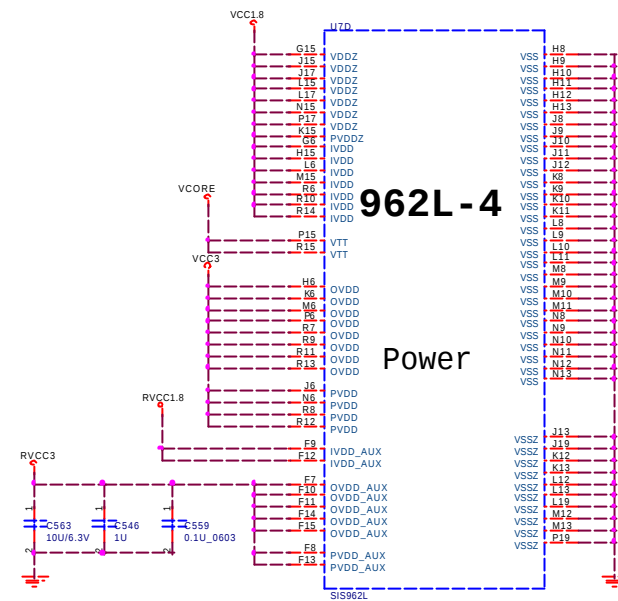
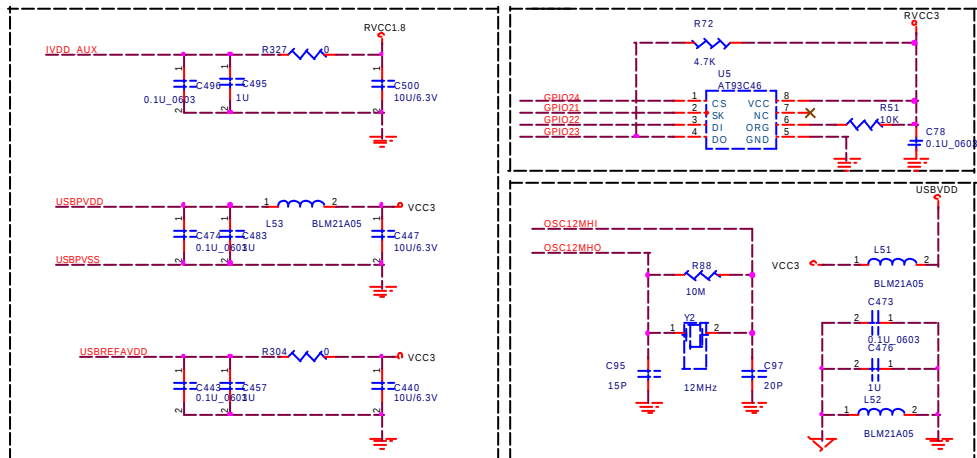
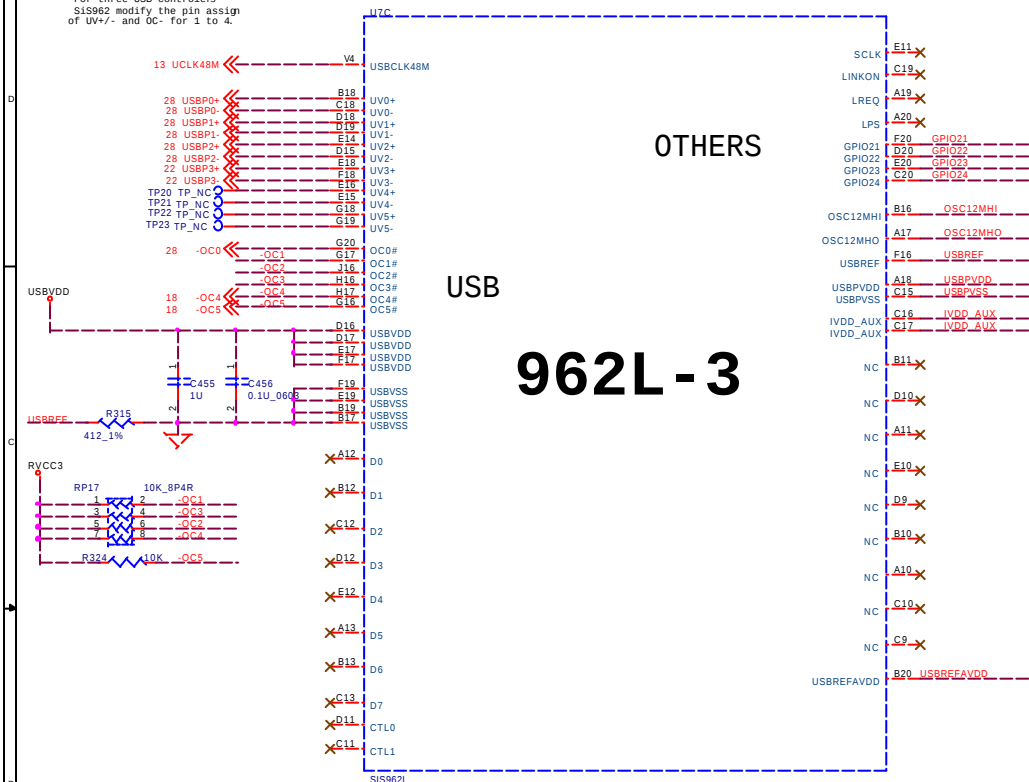


Title			DDR(on board)
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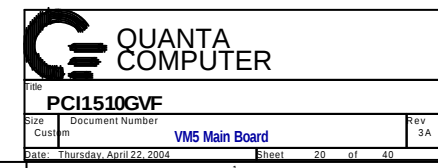




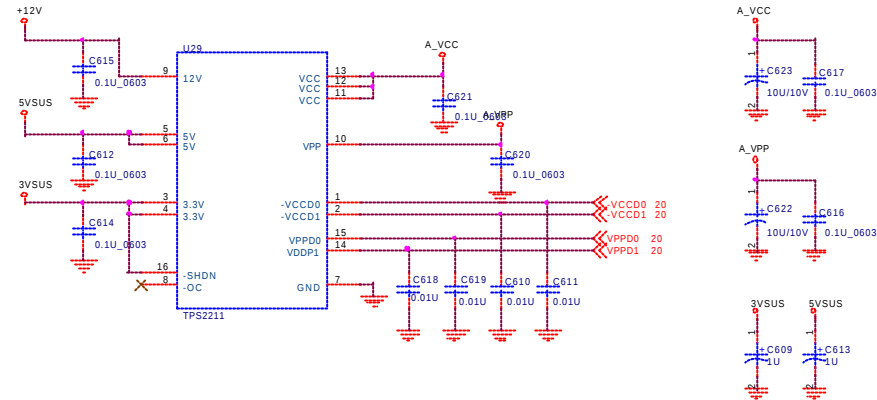
For three USB controllers
SiS962 modify the pin assign
of UV+/- and OC- for 1 to 4.



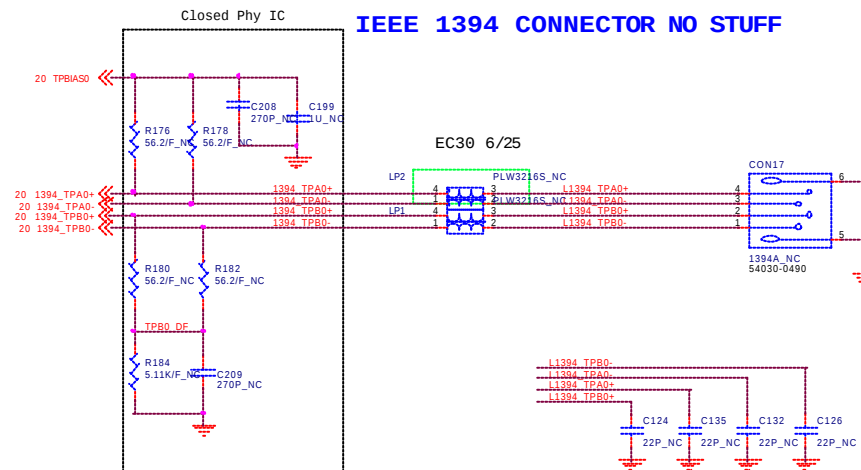
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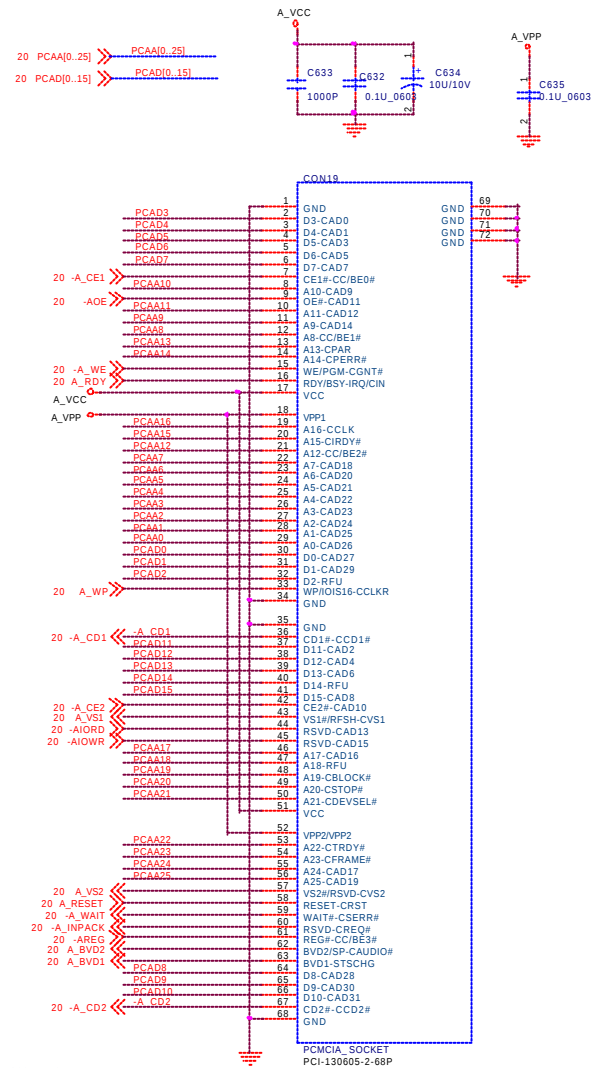
PCMCIA POWER SWITCH



IEEE 1394 CONNECTOR NO STUFF



PCMCIA SOCKET



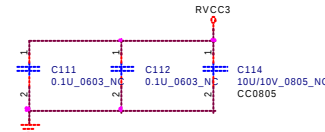
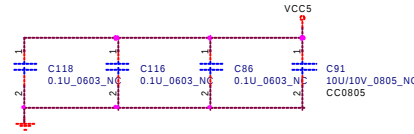
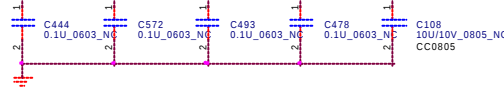
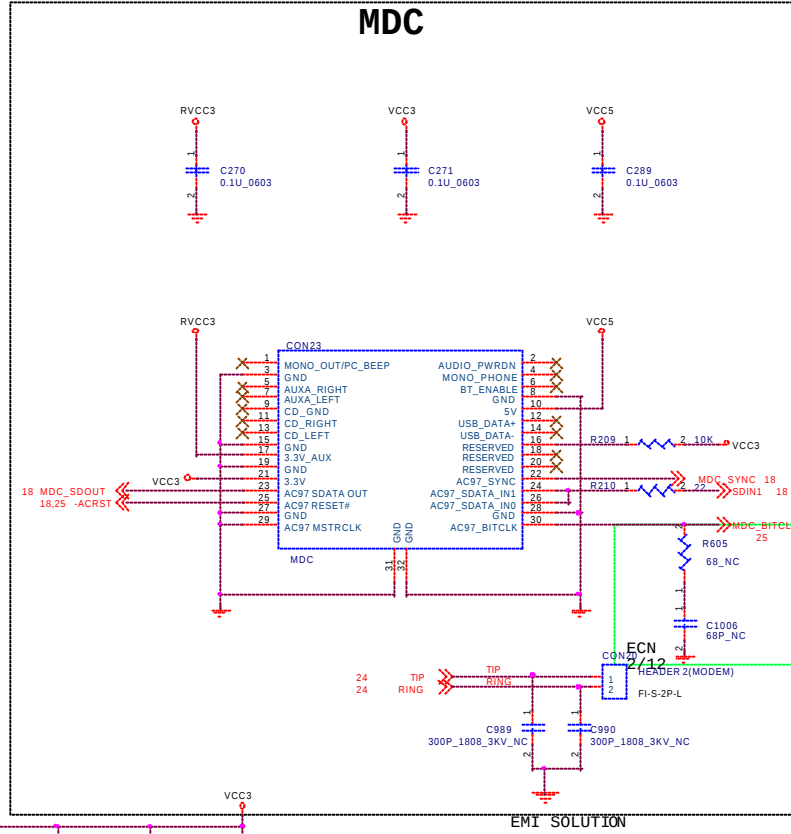
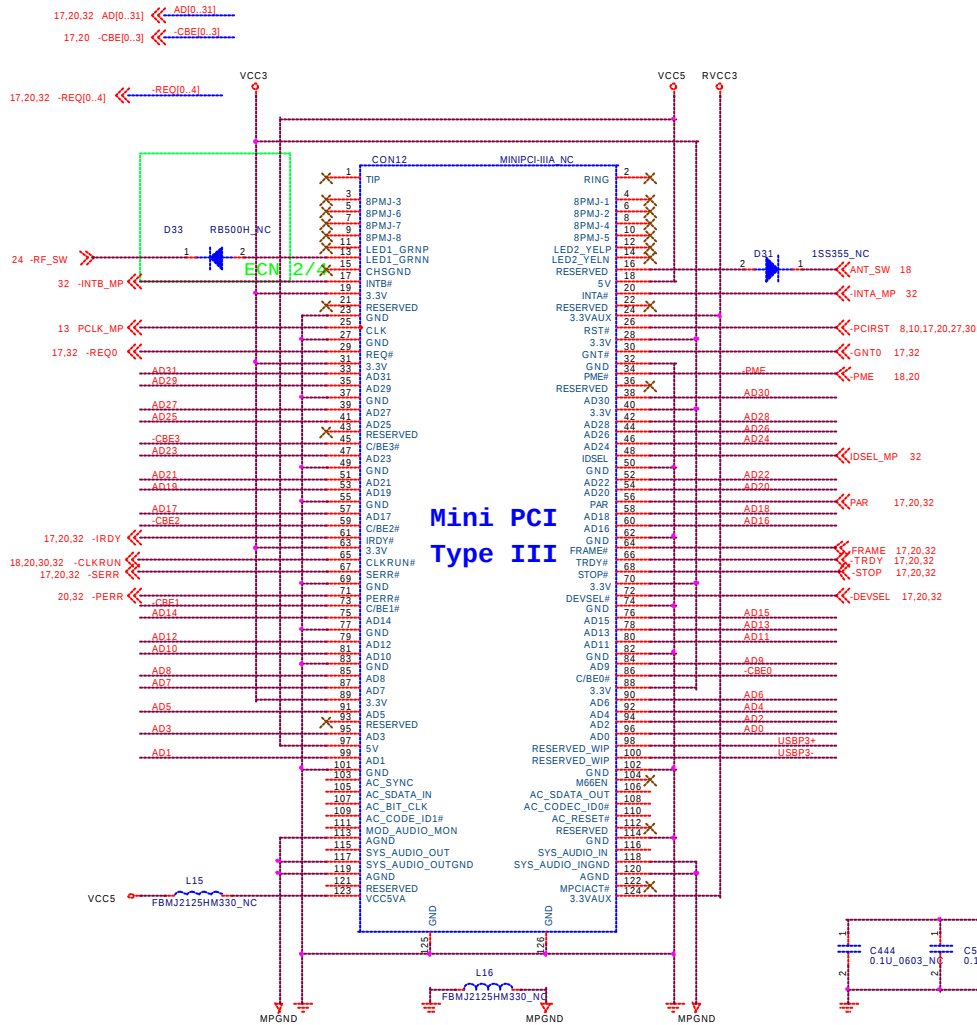
Title **PCMCIA SOCKET&POWER**

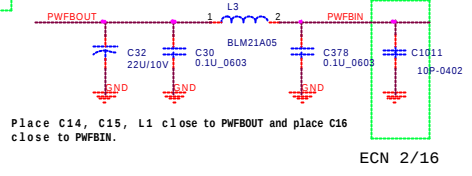
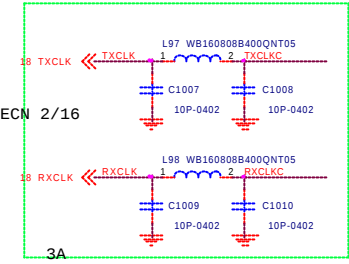
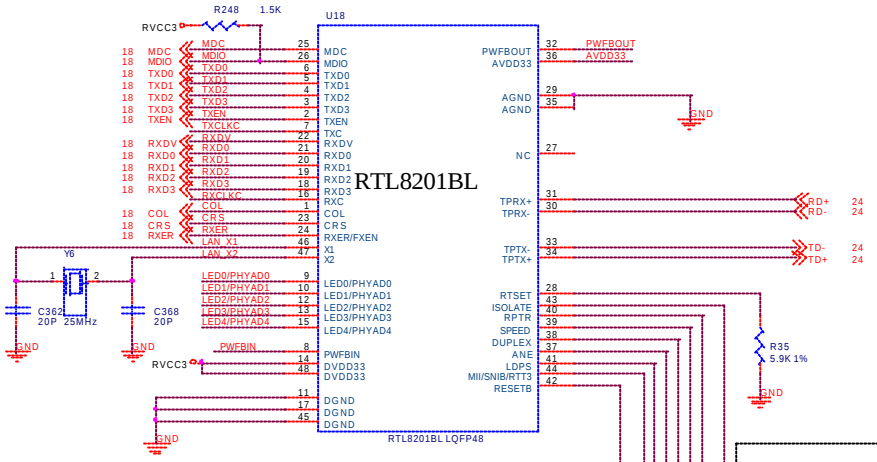
Size	Document Number
Custom	

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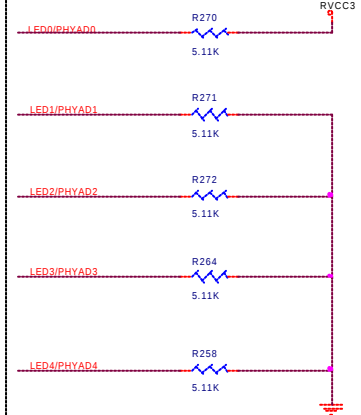




Place C14, C15, L1 close to PWFBOUT and place C16 close to PWFBIN.

ECN 2/16

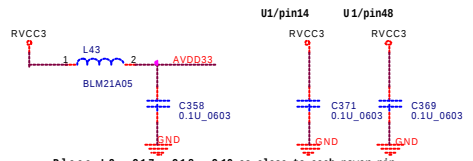
This schematic sets PHY address to 00001b. You could set PHY address from 00001b to 11111b. But the LED polarity must match the respective PHYAD setting. Refer to datasheet's detailed description.



LED0	LED1	LED2	LED3	LED4
Link	Dupx	10Act	100Act	COL

Hardwire Configuration network:

- This configuration shows
Enable: Auto negotiation, Full duplex, 100Mbps,
Link Down Power Saving, MII interface
Disable: I isolate, Repeater mode
- These seven configuration pins could be connected to VDD or GND directly.

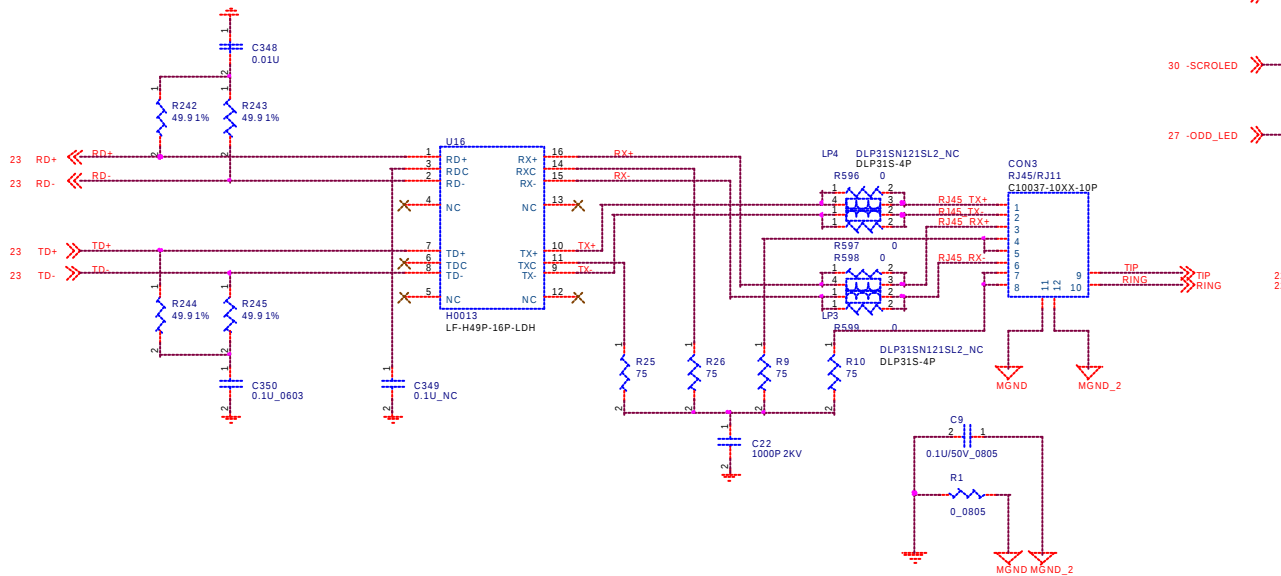
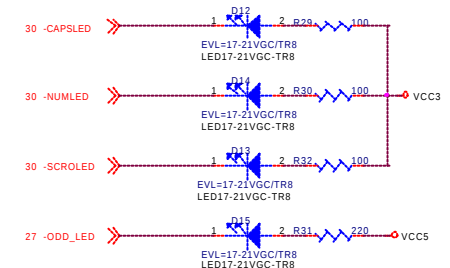
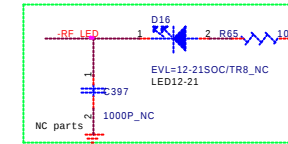
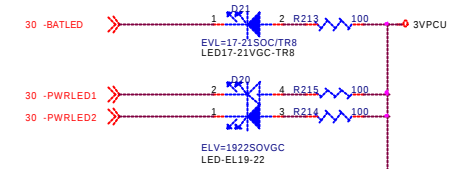
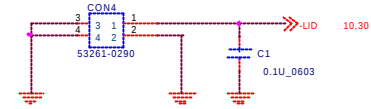
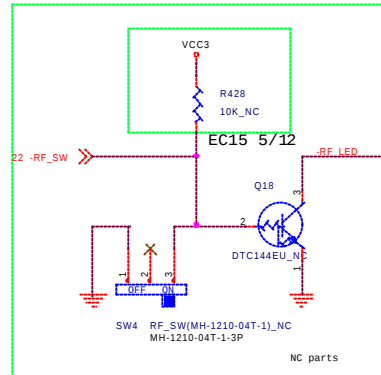
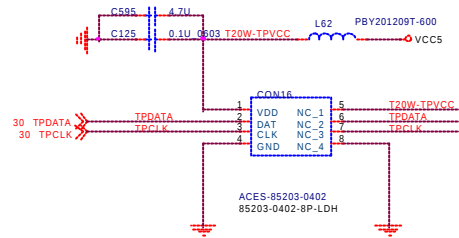


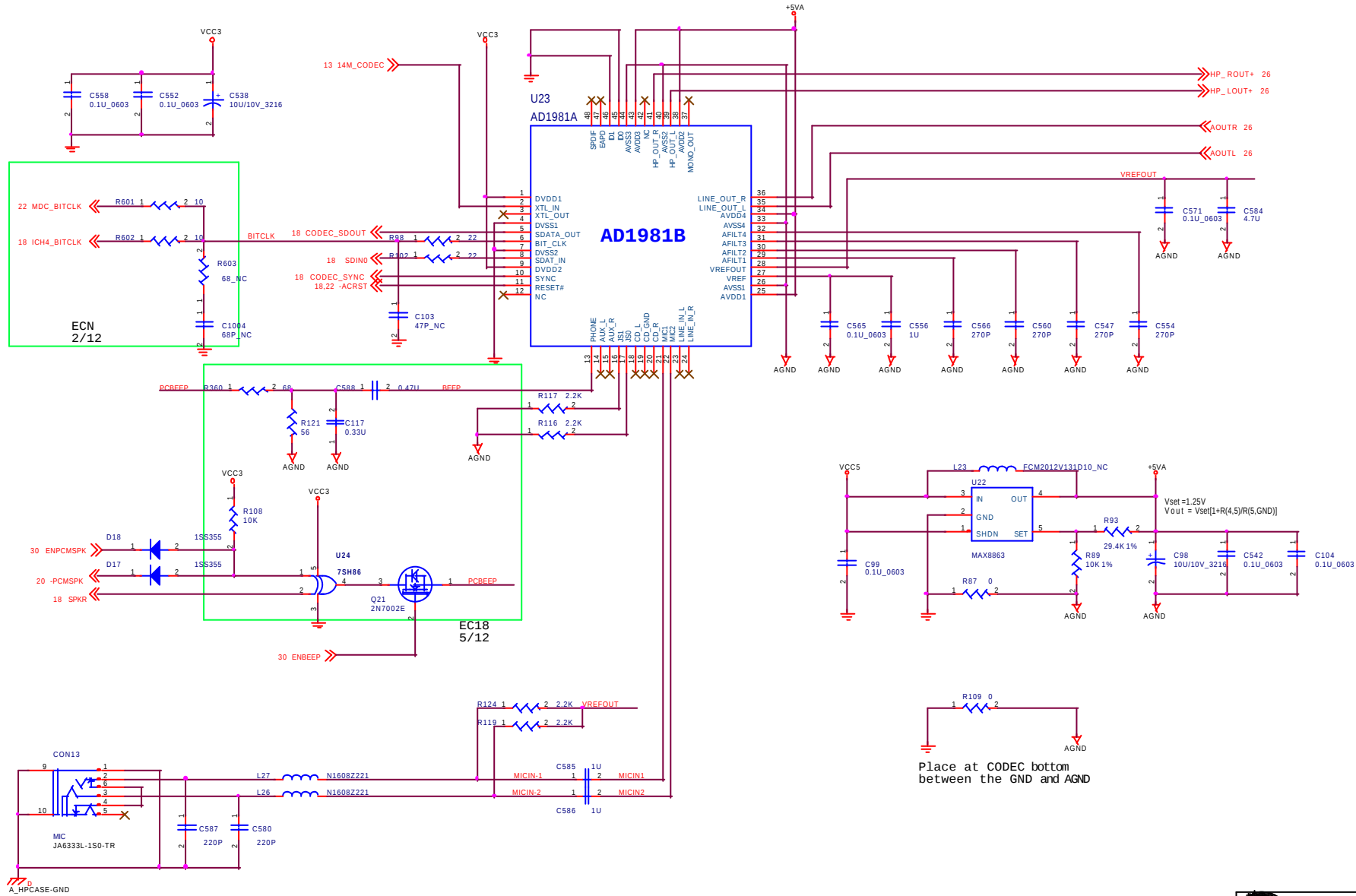
Place L2, C17, C18, C19 as close to each power pin as possible.



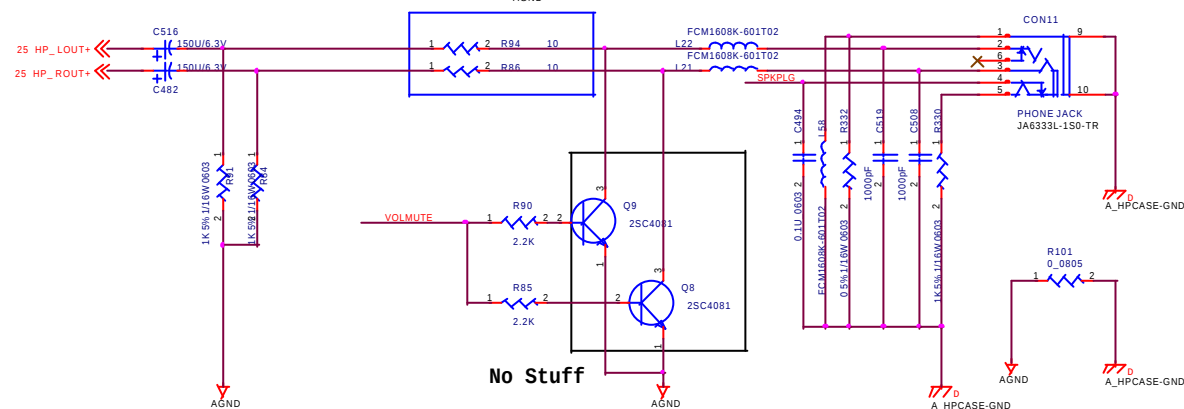
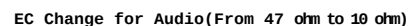
Title		LAN PHY RTL8201BL	
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TOUCHPAD BOARD CON





Place at CODEC bottom
between the GND and AGND



17 IDEDA0 IDEDA0
17 IDEDA15 IDEDA15
17 IDEDA2 IDEDA2
17 IDEDA1 IDEDA1

17 IDEDA4 IDEDA4
17 IDEDA5 IDEDA5
17 IDEDA6 IDEDA6
17 IDEDA7 IDEDA7

17 IDEDA8 IDEDA8
17 IDEDA11 IDEDA11
17 IDEDA9 IDEDA9
17 IDEDA10 IDEDA10

17 IDEDA12 IDEDA12
17 IDEDA13 IDEDA13
17 IDEDA3 IDEDA3
17 IDEDA14 IDEDA14

17 IDECS-A0 IDECS-A0
17 IDESA0 IDESA0
17 IDECS-A1 IDECS-A1
17 IDESA1 IDESA1

17 IDESA2 IDESA2
17 IDEREQA IDEREQA
17 IDEIOW-A IDEIOW-A
17 IDEIOR-A IDEIOR-A
17 ICHRDYA ICHRDYA
17 IDACK-A IDACK-A
17 IDEIRQA IDEIRQA

17 IDEDB13 IDEDB13
17 IDEDB12 IDEDB12
17 IDEDB3 IDEDB3
17 IDEDB2 IDEDB2

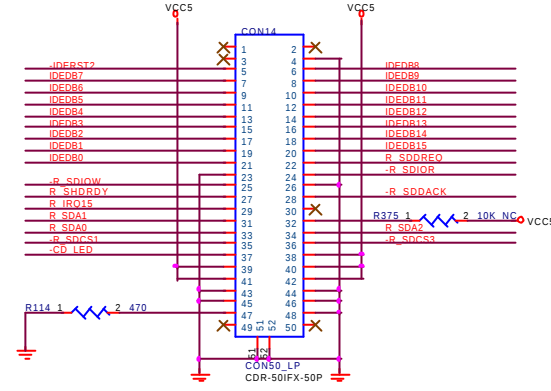
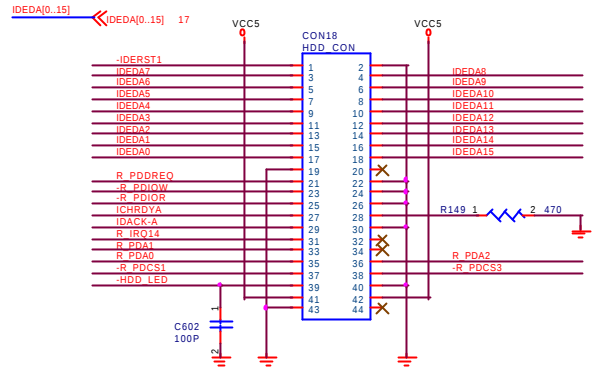
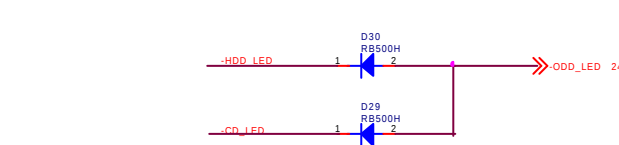
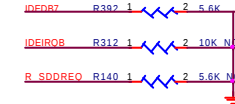
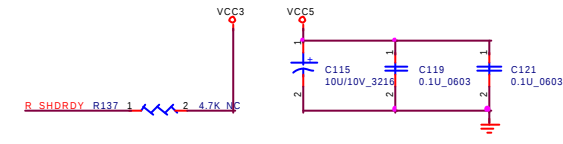
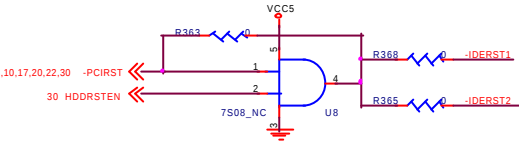
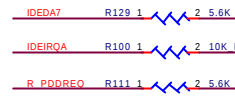
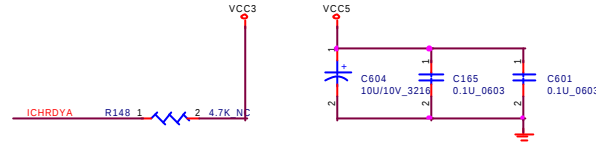
17 IDEDB6 IDEDB6
17 IDEDB5 IDEDB5
17 IDEDB4 IDEDB4
17 IDEDB7 IDEDB7

17 IDEDB8 IDEDB8
17 IDEDB9 IDEDB9
17 IDEDB10 IDEDB10
17 IDEDB11 IDEDB11

17 IDEDB0 IDEDB0
17 IDEDB15 IDEDB15
17 IDEDB1 IDEDB1
17 IDEDB14 IDEDB14

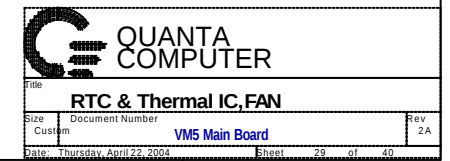
17 IDECS-B0 IDECS-B0
17 IDECS-B1 IDECS-B1
17 IDESB0 IDESB0
17 IDESB1 IDESB1

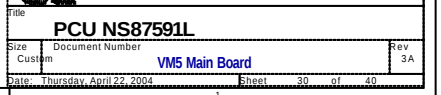
17 IDESB2 IDESB2
17 IDEIORB IDEIORB
17 IDEIOW-B IDEIOW-B
17 IDEIOR-B IDEIOR-B
17 ICHRDYB ICHRDYB
17 IDACK-B IDACK-B
17 IDEREQB IDEREQB





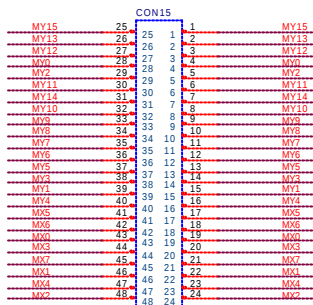
Fan



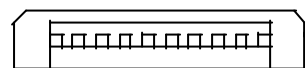


Int. keyboard

$\text{MX}[0..7] \gg \text{MX}[0..7] \quad 30$
 $\text{MY}[0..15] \gg \text{MY}[0..15] \quad 30$

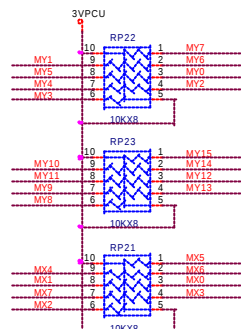
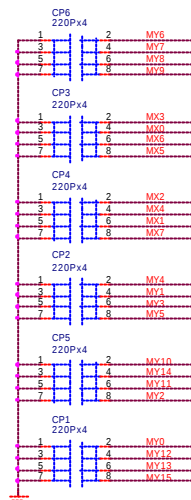


52610-24
52610-24-48P-RUH

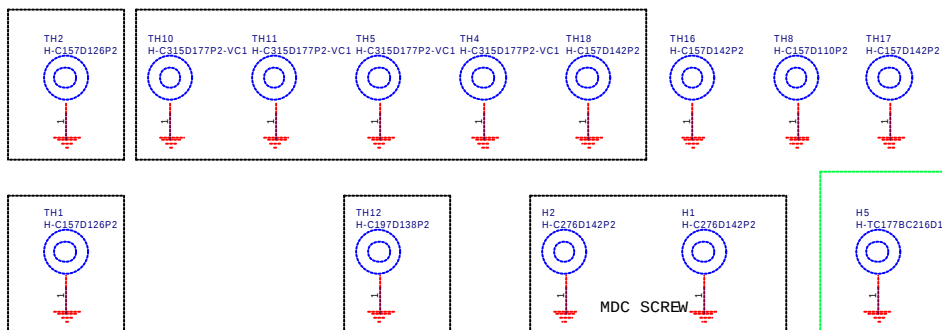


1

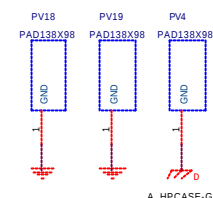
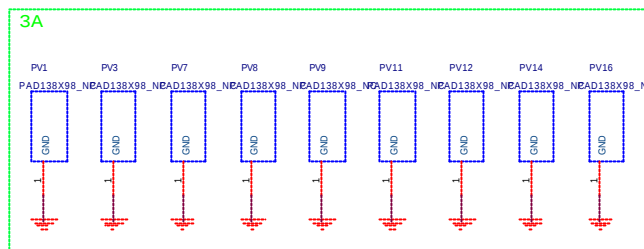
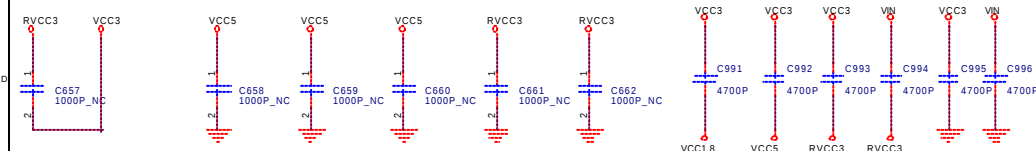
24



Screw

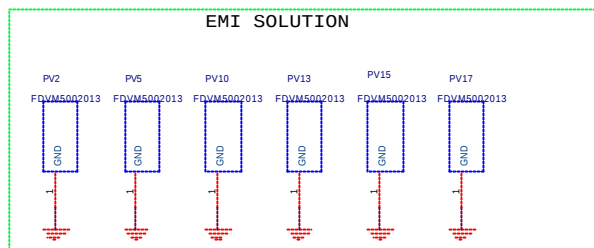


ECN 2/4

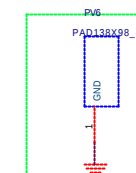


A HPCASE-GND

EMI SOLUTION

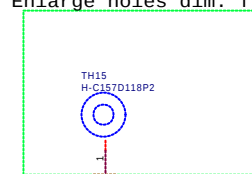


Change P/N

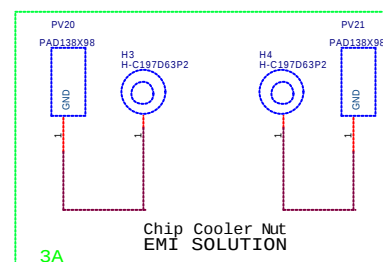
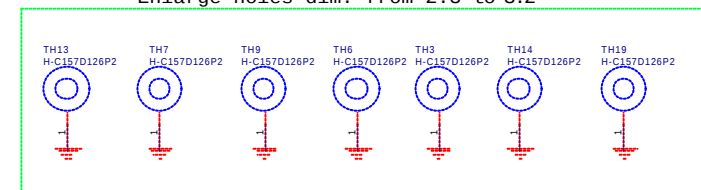


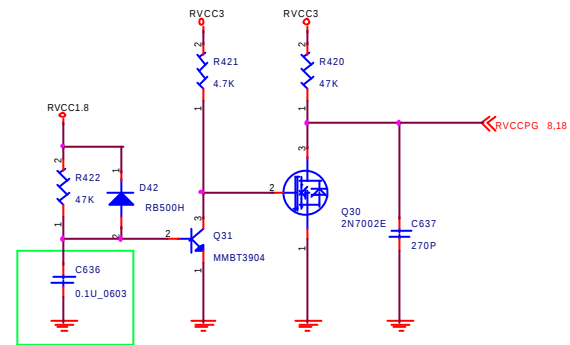
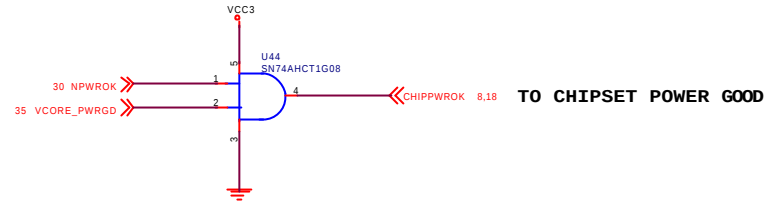
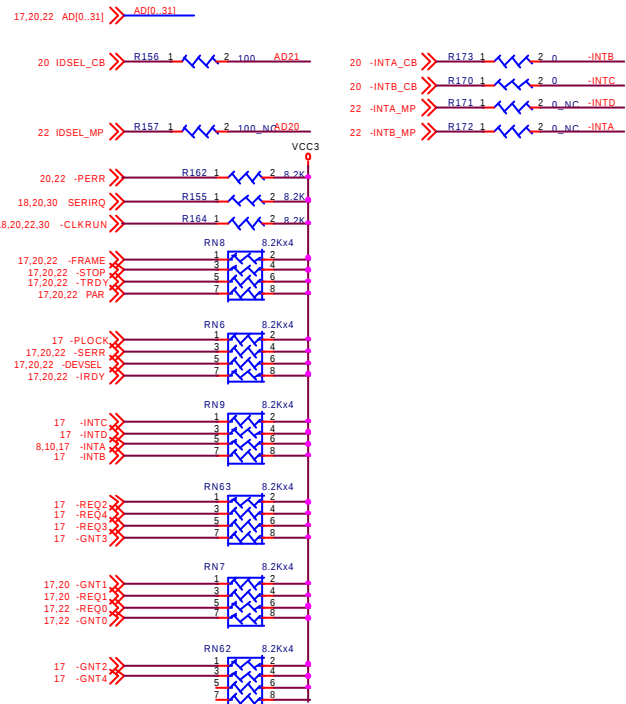
3B

Enlarge holes dim. from 2.8 to 3.0



Enlarge holes dim. from 2.8 to 3.2

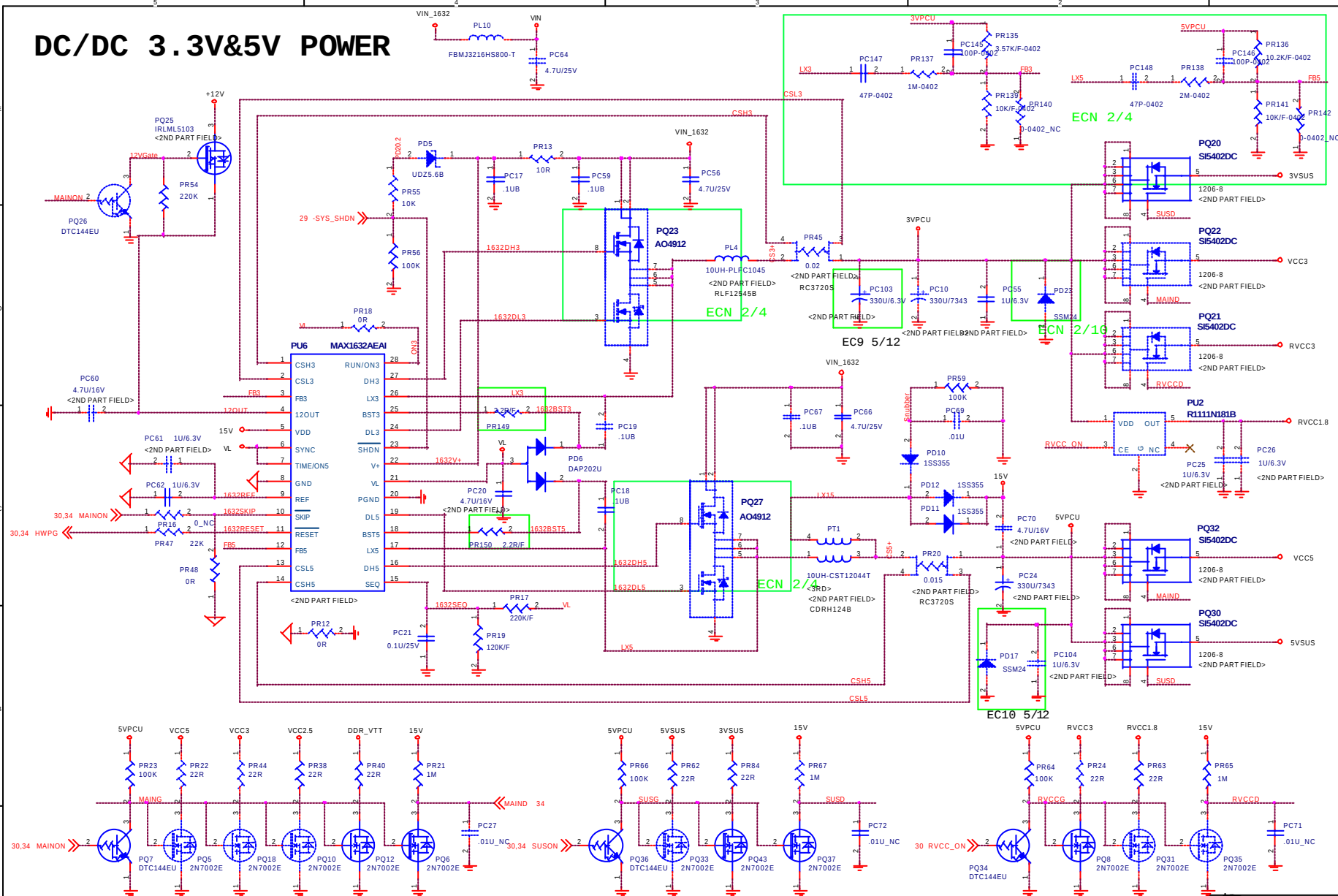




EC8 5/12

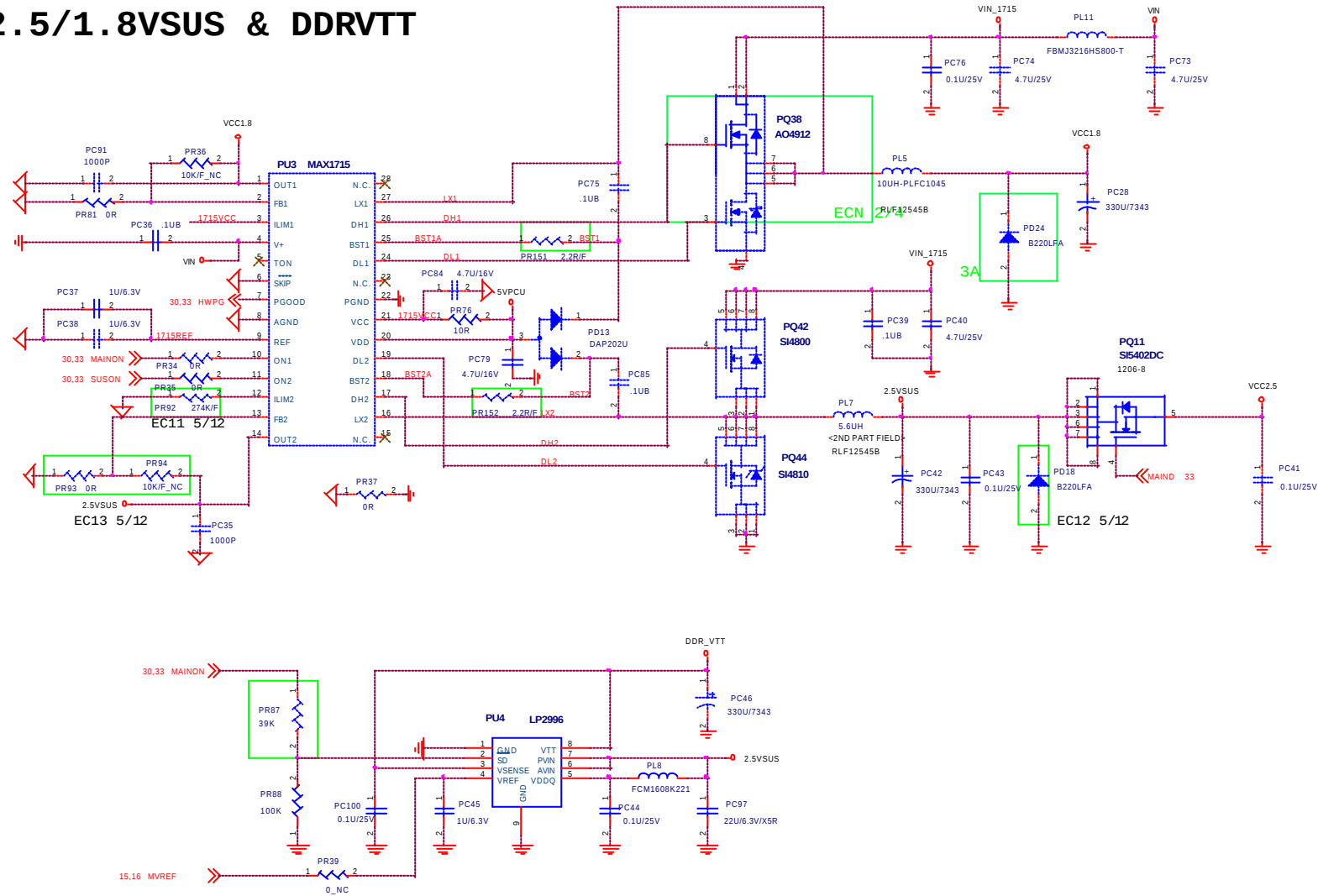
DC/DC 3.3V&5V POWER

33

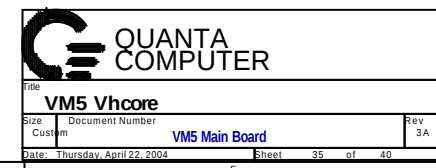


Title		DC/DC 3V&5V
Size	Document Number	VM5 Main Board
Custom		Rev 2A
Date	Thursday, April 22, 2004	Sheet 33 of 40

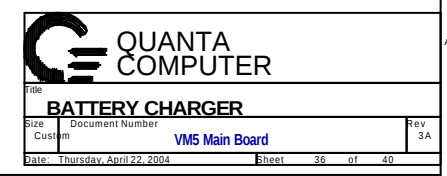
2.5/1.8VSUS & DDRVTT



DC/DC 2.5/1.8/1.5VSUS		
Size	Document Number	Rev
Custom	VM5 Main Board	3A
Date	Thursday, April 22, 2004	Sheet 34 of 40

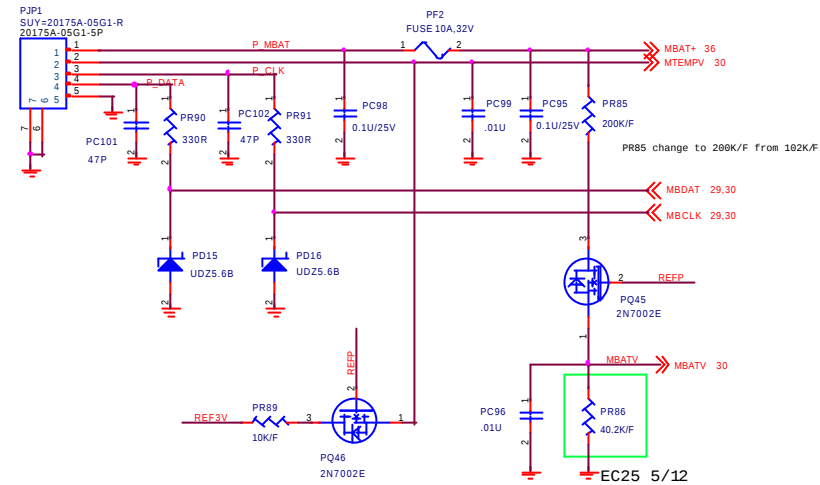
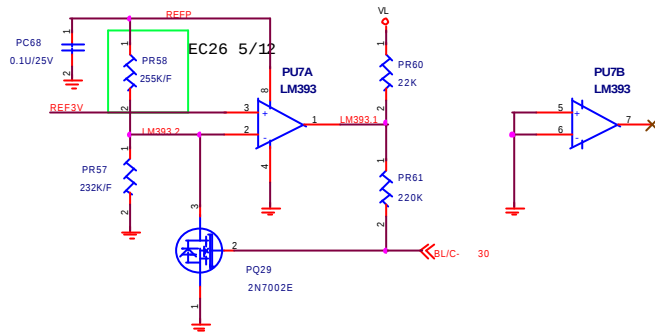


36

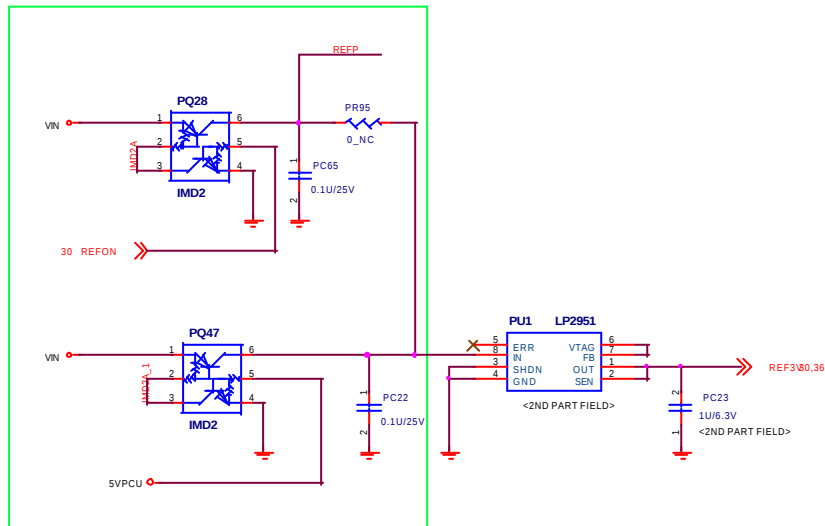


Battery Connector

Voltage low 7.2V detect
for Ni-MH battery



PR85 change to 40.2K/F from 200K/F



EC19 5/12

MODEL	REV	CHANGE LIST	Model	VM5MB	
VM5 MB	1A	First Release	Page	FM	TO
	2A	as below change is from Intel CRB schematic. P3 CPUR5,CPUR7,CPUR8,CPUR35 Change to 51/F P4 CPUR12 change to 220-0402 P4 CPUR1 change to 56/F-0402 P4 CPUR23 change to 300-0402 P4 CPUR38 change to 56/F-0402 P3 CPURN1 change to 200X4 P4 add R595 10K-0402 P.7 Rename net name 2.5SUS to 2.5VSUS P.10 correction VBGCLK to VAGCLK P.10 U21 change value to 302/ELV/302LV P.29 R591 change pull high to VCORE for Thermtrip timing Update Some net name. P.24 add 4 0R resist R596,R597,R598,R599 for Lan Net P.35 RP24 change Value from 1KX4 to 1KX4_0402 P.3 CPURN1 change Value from 200*4 to 51*4 P.20 L63,L65 Change Value from 0 to 0_0805 P.10 R41 change Value from 22 to 22_1206 P.10,P.26 R56,R67,R101 change Value from 0 to 0_0805 P.29 Del Q17 for FAN Issue. System Changed P.30 Remove Email,Internet button function NC parts SW1,SW2,R27,R28,Q24,Q25 P.22,P24 Remove wireless LED function NC parts D33(P.22) R428,Q18,SW4,C397,D16,R65 P.30 Add Mode ID add parts R424,R425,R426,JP2 P.30 Change 51 debug connector JDEBUG1 net name. P.31 Add H3,H4 for NB cooler ,Add H5 for MDC EMI request hole. P.3 Change CPU socket layout library to TM8 used. Power Change: P.35 PQ51,PQ53 change parts to SUD70N03-06P P.33 PQ23,PQ27 change parts to A04912 P.34 PQ38 change parts to A04912 P.33 Power add schematic add parts PC145,PC146,PC147,PC148,PR135,PR136,PR137,PR138,PR139,PR140,PR141,PR142 Remove mini-PCI function to unpopulated P.22 C108,C111,C112,C114,C116,C118,C444,C478,C493,C572,C86,C91,CON12,D31,L15,L16 and P.32 R172,R171,P.13 R534,C941,P.32 R157 P.33 Power placement changed footprint from 0603 to 0402 PC145,PC146,PC147,PC148,PR135,PR136,PR137,PR138,PR139,PR140,PR141,PR142 P.20 Remove 1394 function change U30 chip from PCI4510 to PCI1510GVF, and remove 10 compnents C210,C211,C630,C631,R169,R177,R179,R181,R183,Y8	1	1A	
			2	1A	
			3	2A	
			4	2A	
			5	1A	
			6	1A	
			7	2A	
			8	1A	
			9	1A	
			10	2A	
			11	1A	3A
			12	1A	
			13	1A	3A
			14	1A	
			15	1A	
			16	1A	
			17	1A	
			18	2A	3A
			19	1A	
			20	2A	3A
			21	1A	3A
			22	2A	
			23	2A	3A
			24	2A	
			25	2A	
			26	1A	
 QUANTA COMPUTER		PROJECT: VM5	PART NUMBER: 41VM5MB0004	REV: 3A	DOC NO. 204
		APPROVED BY: VIC Lin	CHECKED BY: Lit Wu	DRAWN BY: Wagner Hong	DATE: 4/6 2004
					SHEET 1 OF 3

MODEL	REV	CHANGE LIST	Model	VM5MB	
VM5 MB		P.10 FOR EMI SOLUTION U21.118 pin add L96 and C1002 DVDD net add C999 VDDV net add L95 and C1000 LVDD1 net R49 change to BK1608LL241,add C1003 C998 LVDD2 net add C1001 P.33 for 3vpcu turn off inrush current solution add diode PD23 P.18 P.30 For Software Boot-Block function use SouthBridge GPIO9 control and add 1 jumper for it, JP2 from 6PIN change to 8PINS,and R600 100K pull-high P.35 PQ49 change Library pin define P.18,P.22,P.25 For prevent Bit-clock failed, put some solution into schematic,Add R601,R602 and NC parts R603,C1004,R605,R604,C1005,C1006 P.36 Add a EMI solution Varistor RV1 on DC-IN jack P.23 Add EMI solution On net PWFBIN add a 10P cap C1011 On TXCLK and RXCLK net add a pi type filter as below components C1007,C1008,C1009,C1010,L97,L98 P.18 Fixed AC97 signal failed add R606,R607,R608,R609 P.30 RVS for NS97591V add L99 P.35 power add rvs item PR143,PR144	Page	FM	TO
			27	1A	
			28	1A	
			29	2A	
			30	2A	3A
			31	2A	3A
			32	2A	
			33	2A	
			34	2A	3A
			35	2A	3A
			36	2A	3A
			37	1A	
	3A	0317 P.18 Change R578 to 10K and Pull Down. P.20 Change page title. P.23 L97,L98 change footprint to 0603 P.35 Change PR111 to 2.49K/F. P.35 Change RP24 Value from 1KX4_0402 to 2.2KX4_0402 0318 Power changed P.35 PR100 from 1K change to 2.2K. P.35 PR105,PR119 change footprint and P/N to RC2512-DM1,CS+0018J104 for Rsens non-accurate. P.34 ADD A DIODE PD24 VCC1.8 NET. P.11 ADD INVERT POWER source start circuit ADD PARTS PC149,PQ54,PQ55,PR145,PR146,RP25. System. P.13 change C985 net to FB_IN close to U43 pin20. P.18 Remove net BitCLK and C591 of single net P.18 Add 6 resists R610,R611,R612,R613,R614,R615 use SB GPIO6,9,10 for VM5 board id circuit. For proto3 VM5 board mount R611,R613,R615 10K others NC. P.30 Remove B_Block function de-populated R600. 0319 P.31 Change H3,H4 library. 0323 P.13 Change C985 net from FB_IN to FB_OUT. 0324 Hole TH13,TH14,TH15,TH19,TH3,TH6,TH7,TH9 Change layout library and hole dim. P.36 EMI add PC150 and PC151 cap. 0325 P.21 Change CON19 layout library.			
		PROJECT: VM5	PART NUMBER: 41VM5MB0004	REV: 3A	DOC NO. 204
APPROVED BY: VIC Lin		CHECKED BY: Lit Wu	DRAWN BY: Wagner Hong	DATE: 4/6 2004	SHEET 2 OF 3

[illegible]