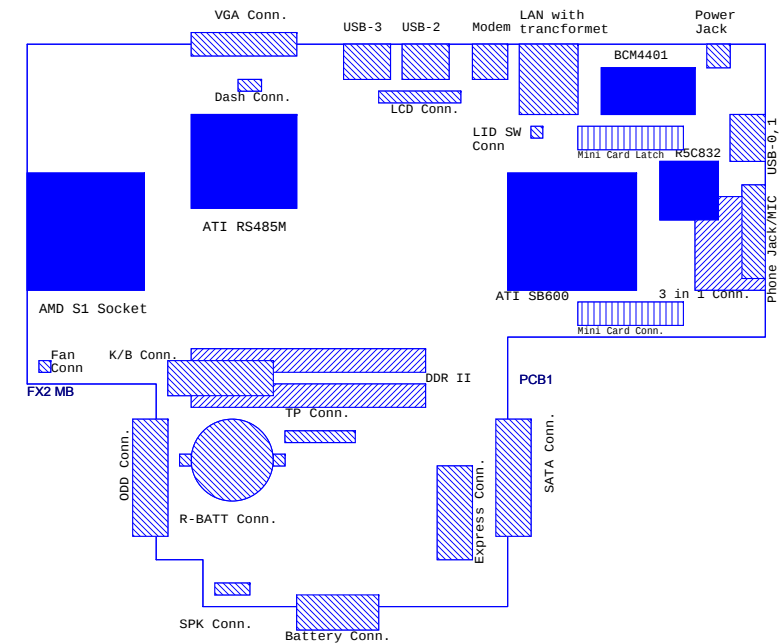
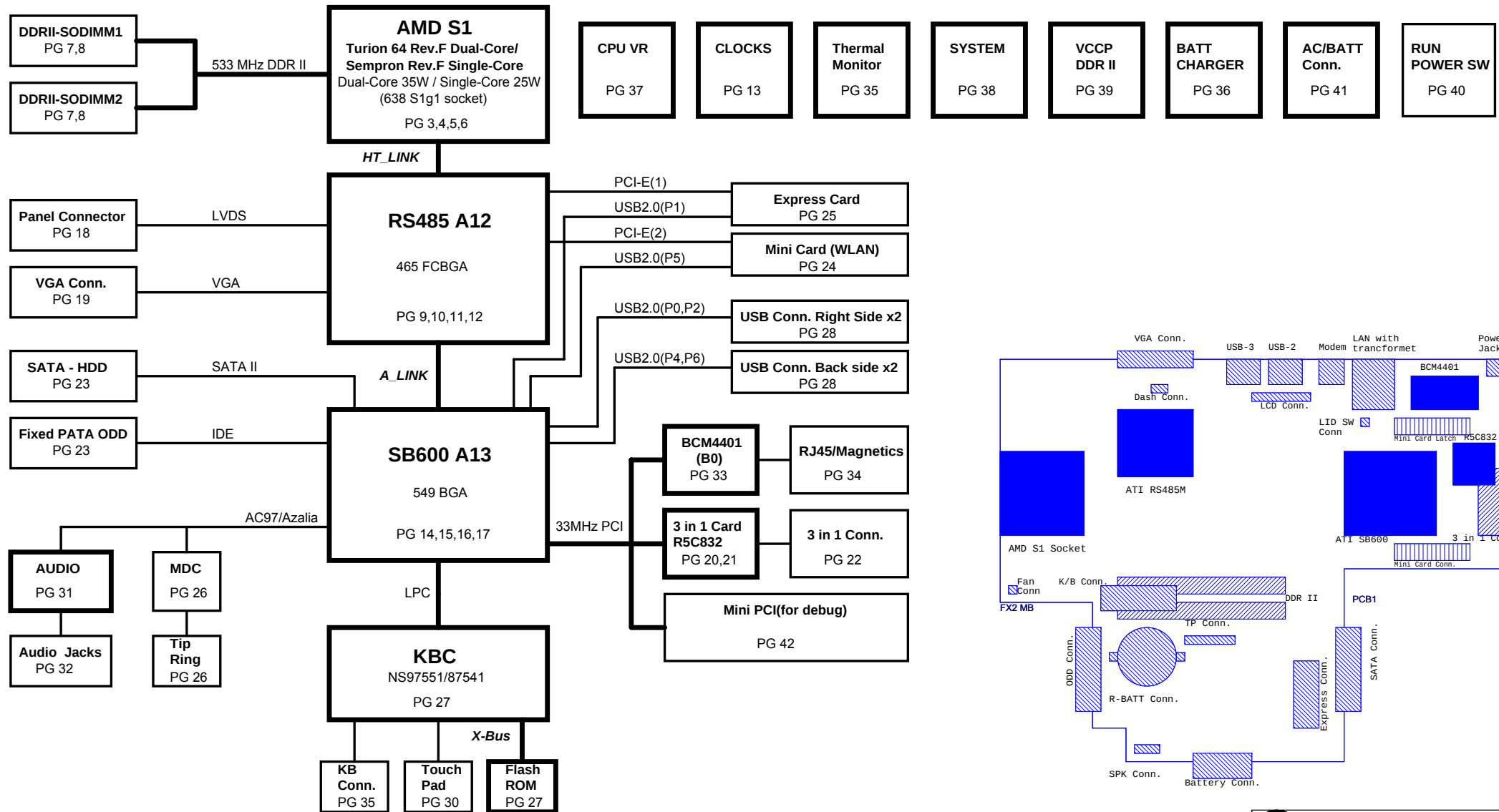


Kirin (FX2 with NS) VER : 1A



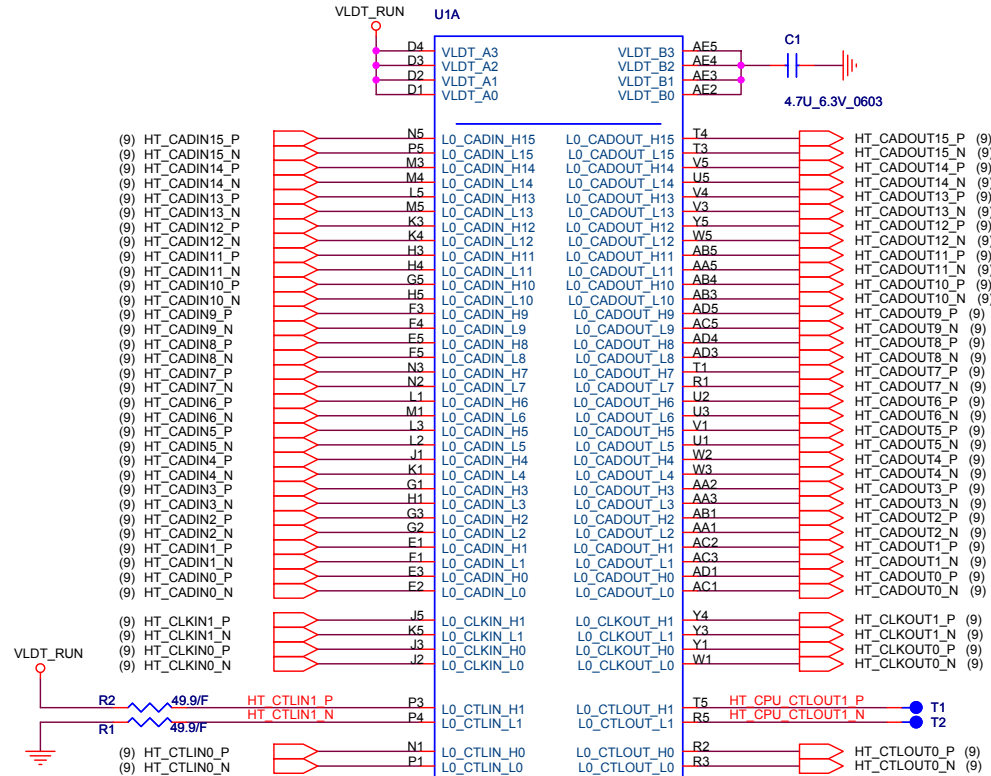
INDEX

Page	Description
1	BLOCK DIAGRAM
2	FRONT PAGE
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4	ATHLON64 DDRII MEMORY
5	ATHLON64 CTRL & DEBUG
6	ATHLON64 PWR & GND
7	DDRII SODIMMX2
8	DDRII TERMINATION
9	RS485-HT LINK0 I/F
10	RS485-PCIE LINK I/F
11	RS485-LVDS
12	RS485-POWER
13	CLOCK GENERATOR
14	SB600M-PCIE/PCI/LPC
15	SB600M ACPI/USB/AC97
16	SB600M HDD/POWER
17	SB600M STRAPS
18	LCD CONN
19	CRT
20	5C832/PCI
21	CARD READER
22	CARD READER CONN
23	SATA HDD & PATA ODD
24	MINI Card
25	MINI Card
26	MDC CONN
27	PC97551 & FLASH
28	USB
29	EMI & Screw hole
30	SWITCH & TP & LED
31	Azelia CODEC
32	AUDIO CONN
33	LAN(BCM4401)
34	LAN JACK
35	KB & THERMAL & FAN
36	CHARGER (MAX8731)
37	VHCORE (MAX8774)
38	SYSTEM (MAX8734)
39	VCCP & DDR2 (MAX8743)
40	RUN POWER SW
41	DCIN,Batt
42	MINI PCI(for debug)
43	Power On Sequence
44	Power On Diagram
45	SMBUS BLOCK

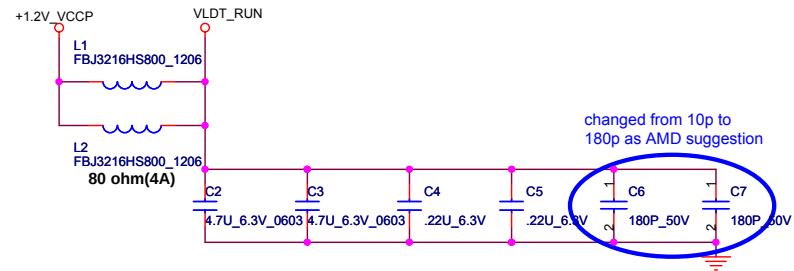


PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Athlon 64 S1
Processor Socket



LAYOUT: Place bypass cap on topside of board



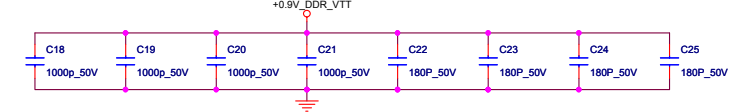
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS



QUANTA
COMPUTER

Title			ATHLON64 HT I/F
Size	Document Number	Rev	
	FX2	1A	
Date:	Friday, May 05, 2006	Sheet	3 of 47

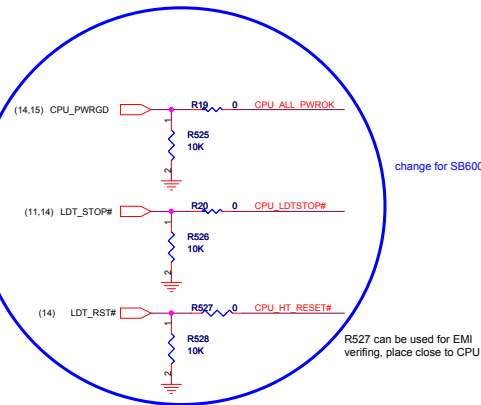
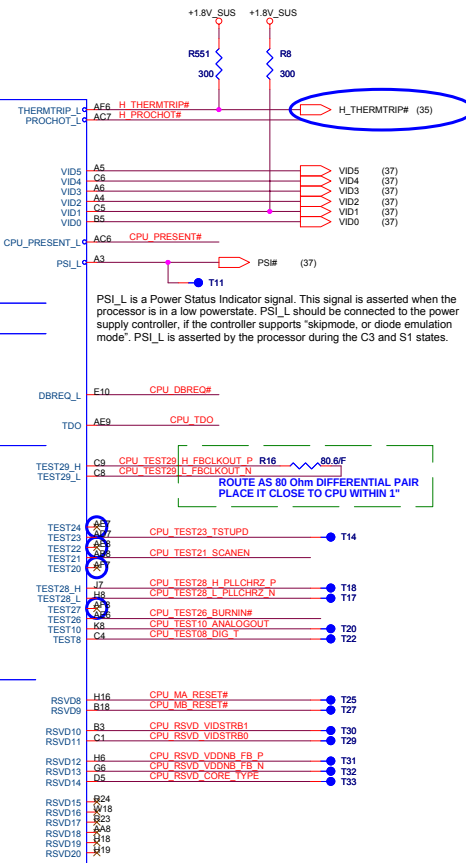
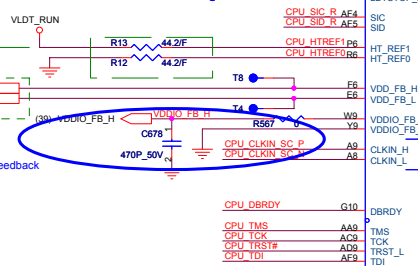
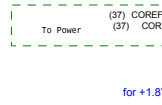
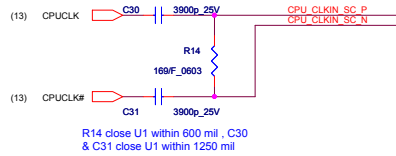
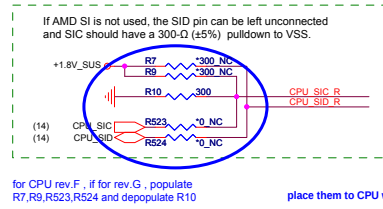
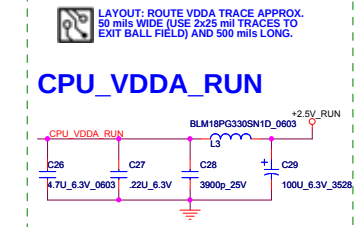
for +0.9V_DDR_VTT
feedback



To SODIMM socket B (Far)



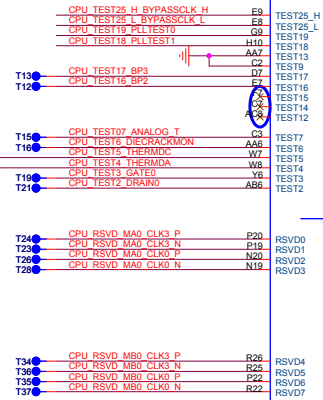
ATHLON Control and Debug



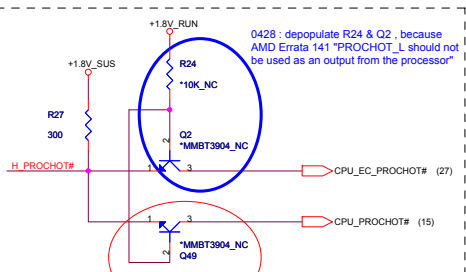
change for SB600 from SB460



add port to Page 35 U36 T1

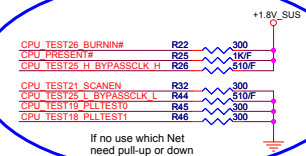


AMD NPT S1 SOCKET
Processor Socket

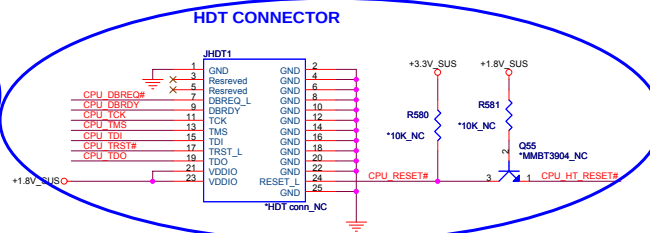


SB this pin is 3.3V, need it level-shift.

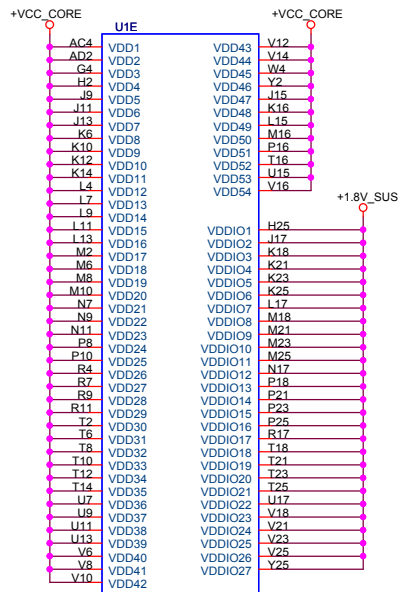
```
delete ED5 H_THERMTRIP# circuit
```



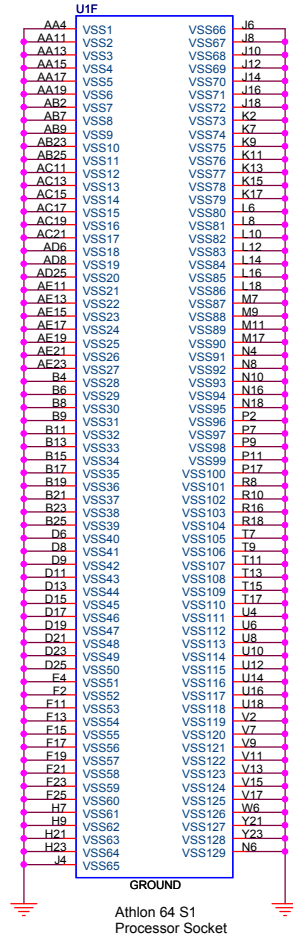
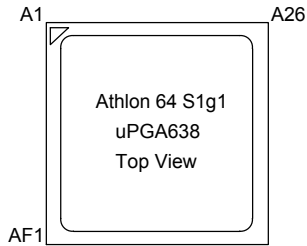
If no use which Net
need pull-up or down



delete ED5 thermal sensor

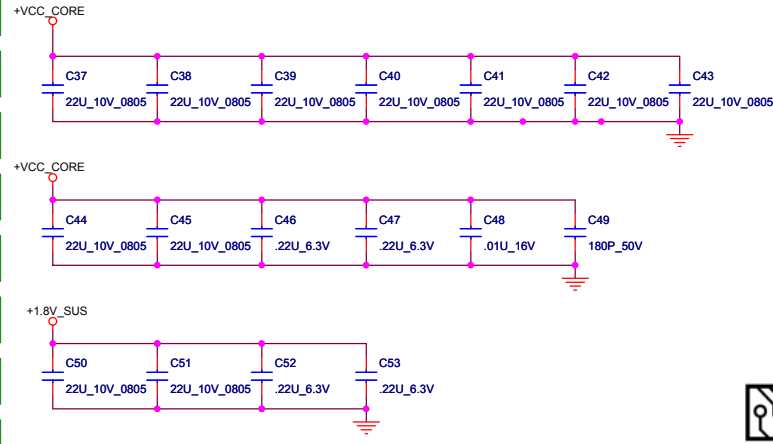


Athlon 64 S1
Processor Socket

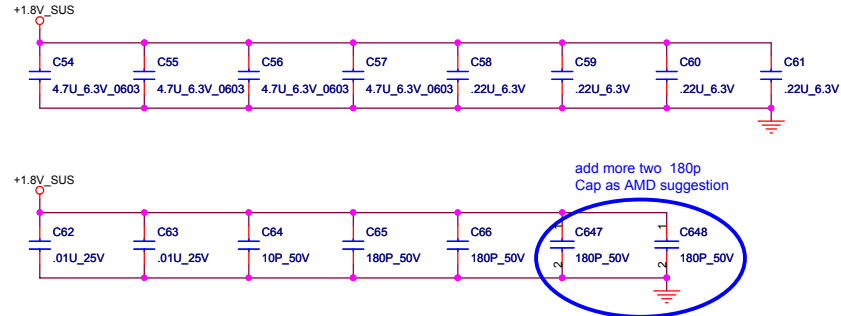


Athlon 64 S1
Processor Socket

BOTTOMSIDE DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE

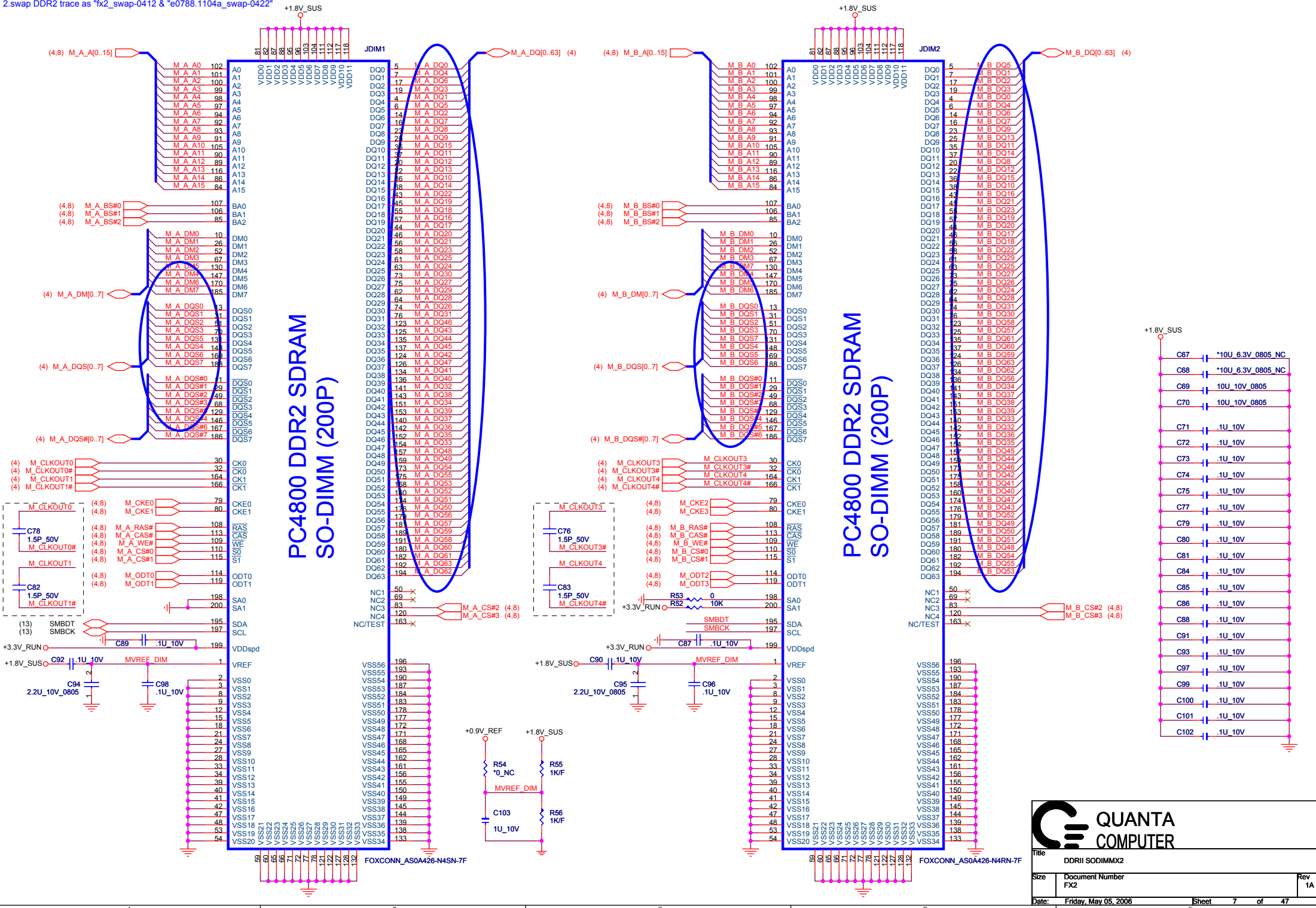


PROCESSOR POWER AND GROUND



Title ATHLON64 PWR & GND		
Size FX2	Document Number	Rev 1A
Date: Thursday, May 04, 2006	Sheet 6	of 47

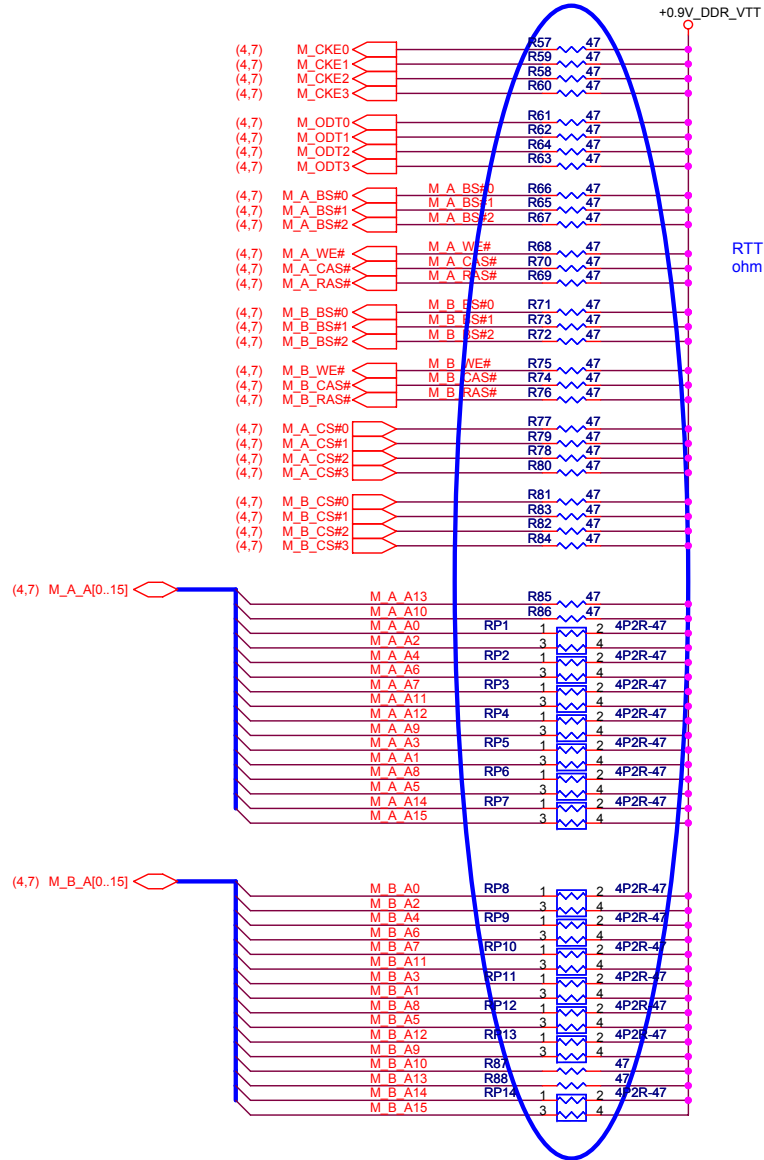
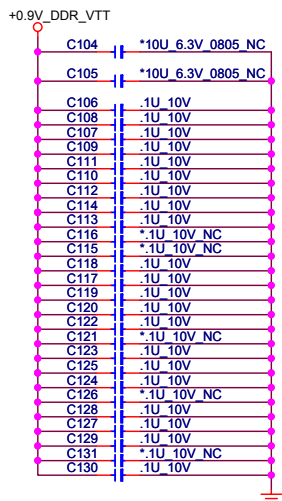
1.Change DDR2 socket(P/N, Description, footprint, part reference, value)
2.swap DDR2 trace as "fx2_swap-0412 & "e0788.1104a_swap-0422"



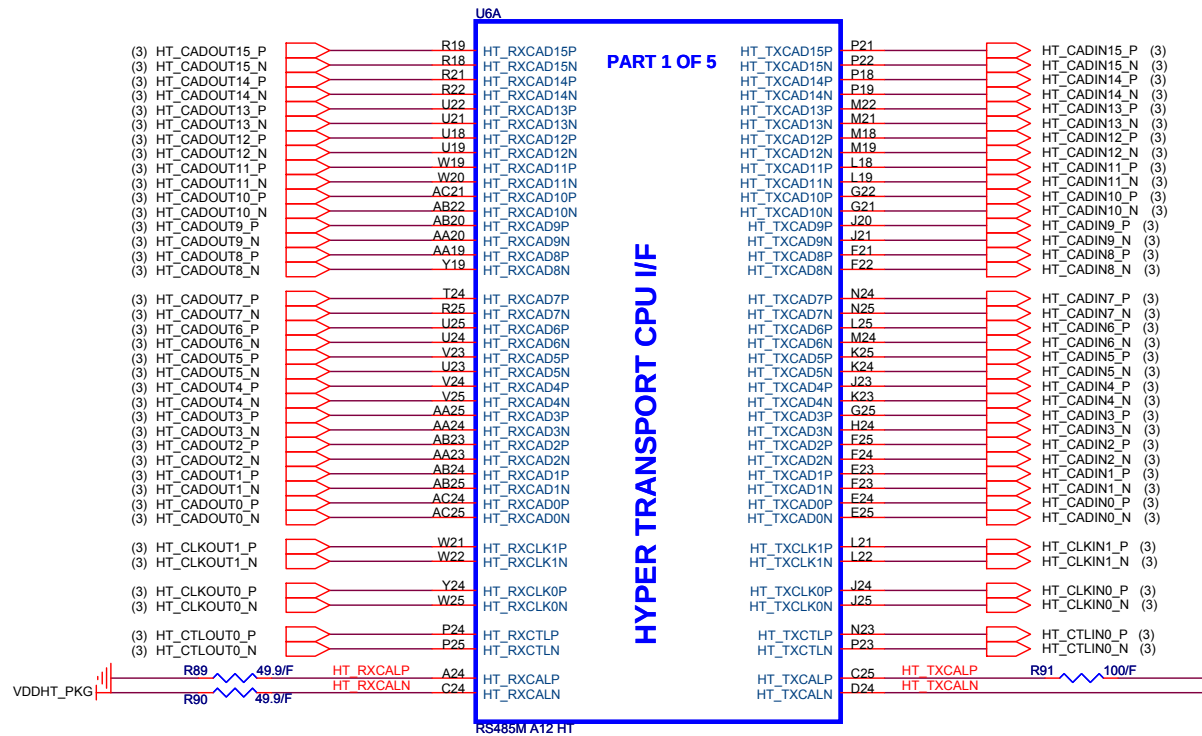


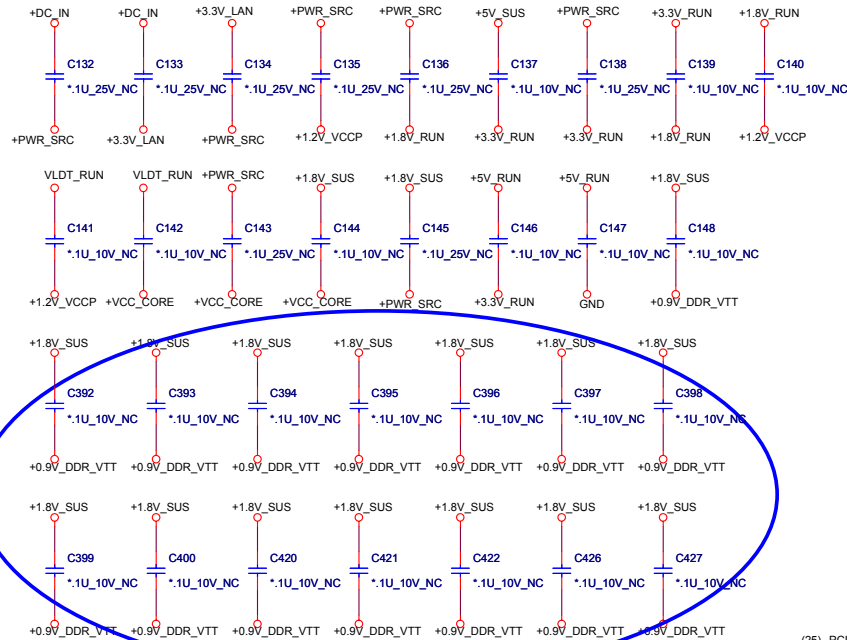
QUANTA
COMPUTER

Title DDR2I SODIMMx2		
Size FX2	Document Number FX2	Rev 1A
Date Friday, May 05, 2006		Sheet 7 of 47



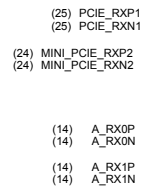
RTT termination changed from 56 ohm to 47 ohm as AMD suggestion



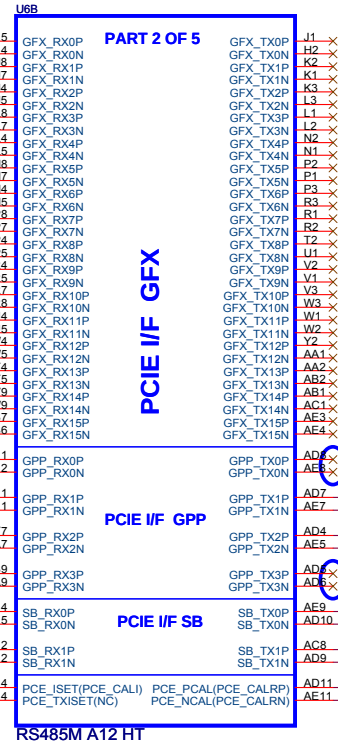


reserve more 14 Cap. between +0.9V_DDR_VTT & +1.8V_SUS

delete PCIE signal , original LAN & Mini Card of ED5



R93: 10KOhm FOR RS485
1.47KOhm FOR RS690
R92: 8.25KOhm FOR RS485
DNI FOR RS690



RS485M A12 HT

R95: 150 Ohm FOR RS485
562 Ohm FOR RS690
R94: Ward update to 100 Ohm FOR RS485
2KOhm FOR RS690

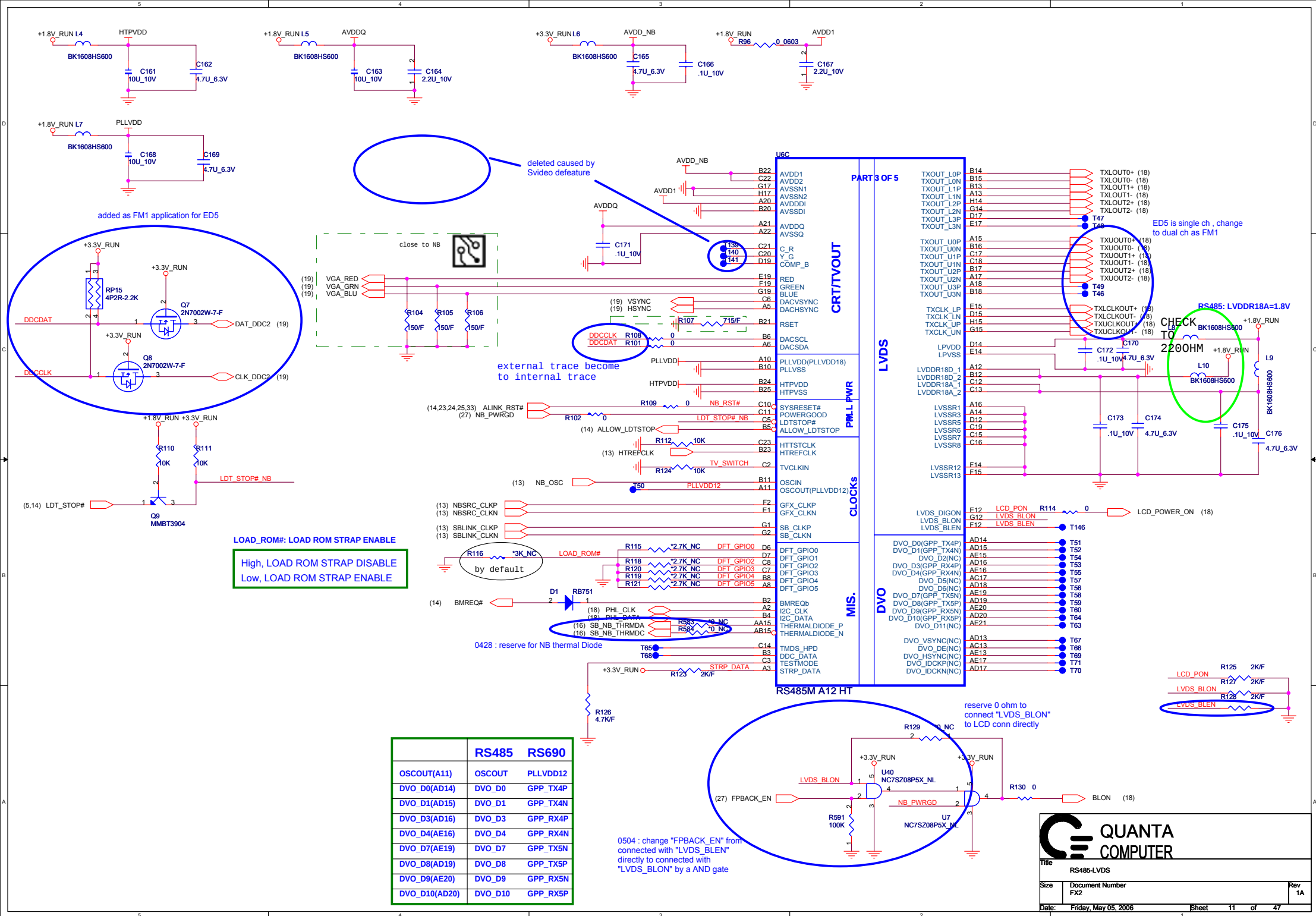


Place these caps close to connector

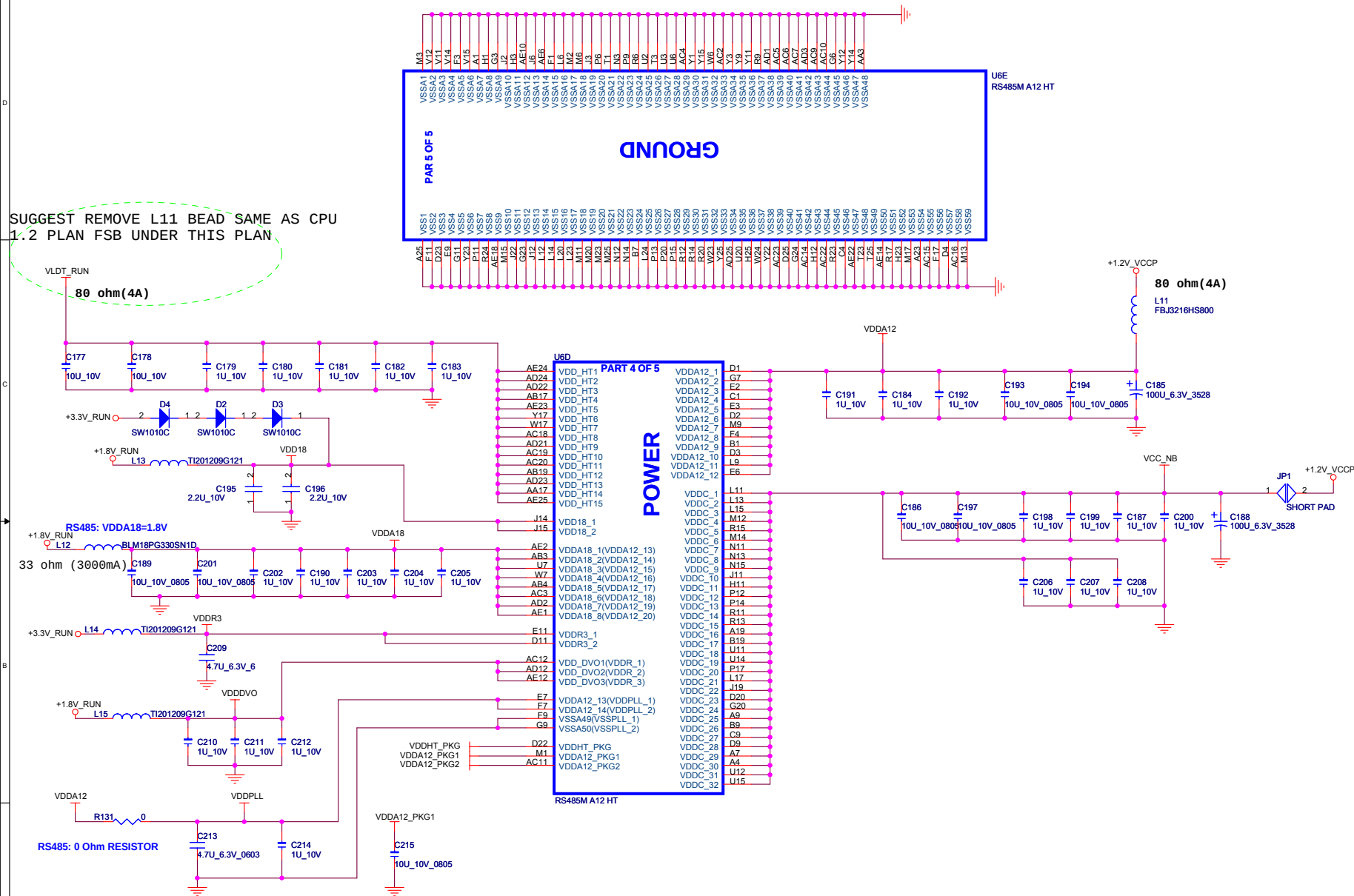


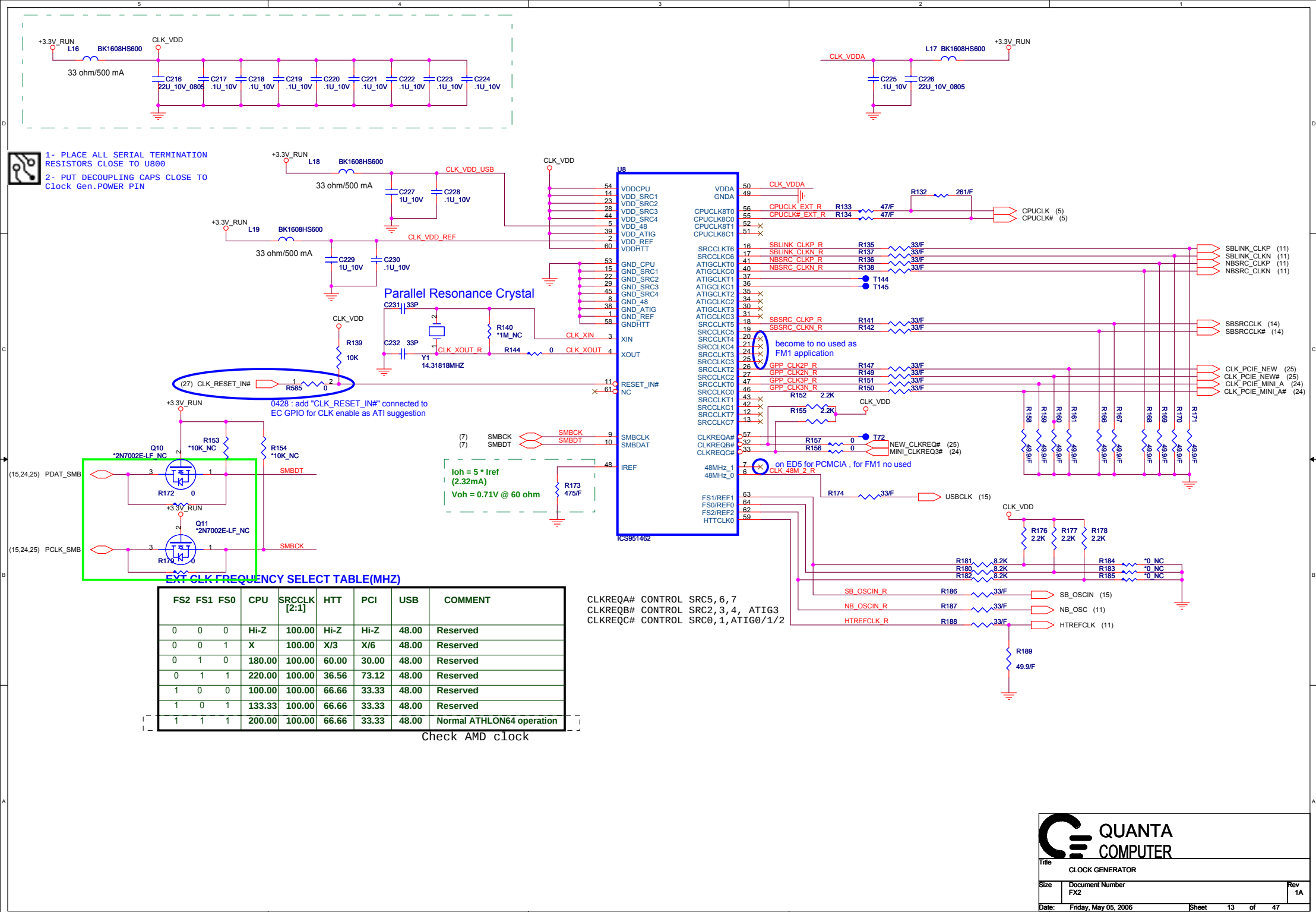
QUANTA
COMPUTER

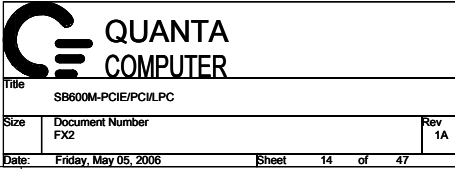
Title			
RS485-PCIE LINK I/F			
Size	Document Number	Rev	
FX2		1A	
Date:	Friday, May 05, 2006	Sheet	10 of 47

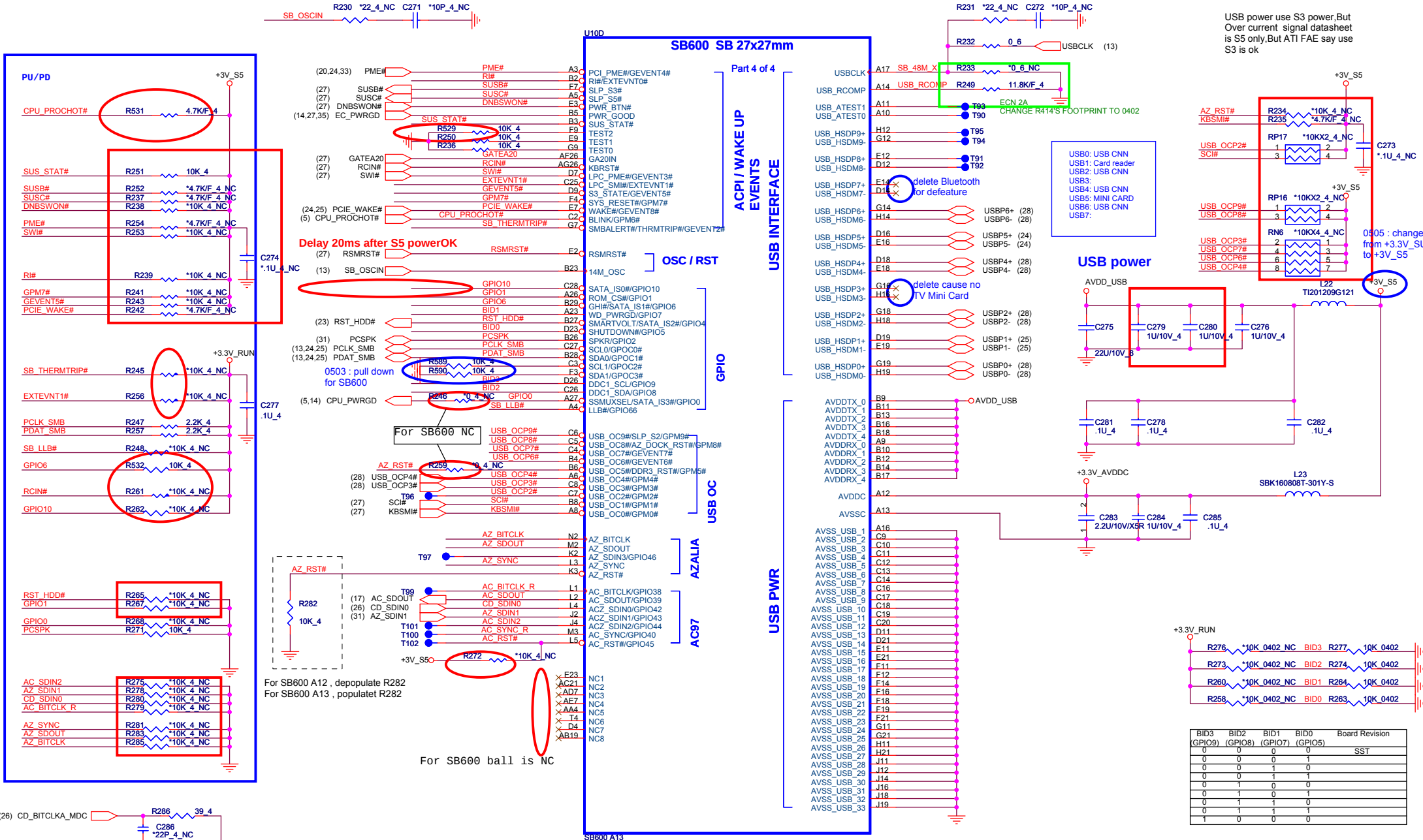


SUGGEST REMOVE L11 BEAD SAME AS CPU
1.2 PLAN FSB UNDER THIS PLAN









USB power use S3 power, But
Over current signal datasheet
is S5 only, But ATI FAE say use
S3 is ok

USB0: USB CNN
USB1: Card reader
USB2: USB CNN
USB3:
USB4: USB CNN
USB5: MINI CARD
USB6: USB CNN
USB7:

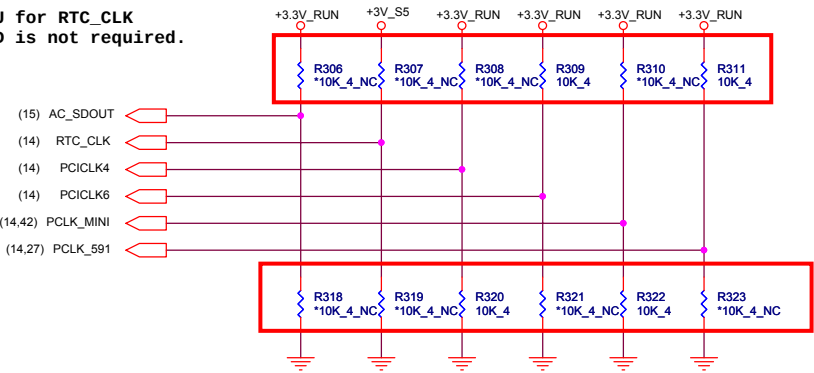
USB power

BID3	BID2	BID1	BID0	Board Revision
(GPIO9)	(GPIO8)	(GPIO7)	(GPIO5)	
0	0	0	0	SST
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	



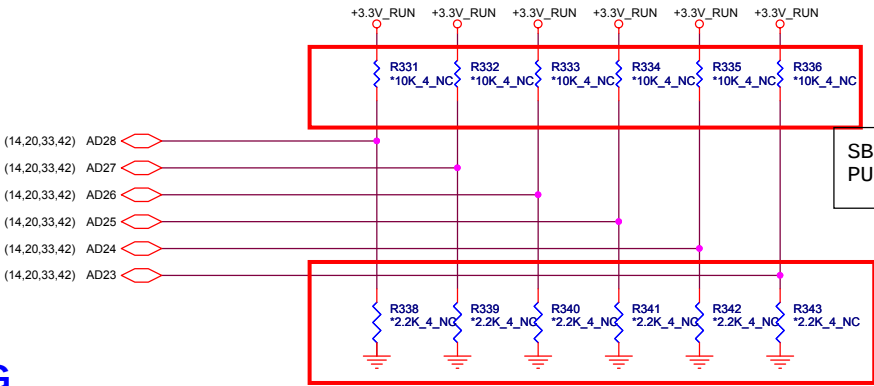
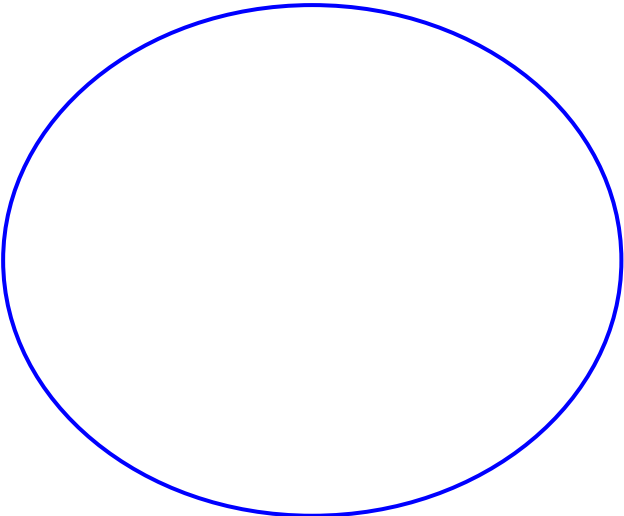
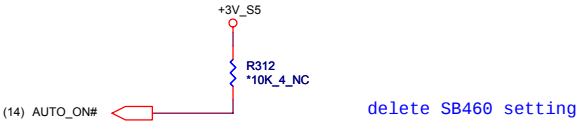
File	SB600M ACPI/USB/AC97	Rev	1A
Size	Document Number FX2		
Date:	Friday, May 05, 2006	Sheet	15 of 47

SB600 has 15K internal PD for AC_SDOUT
15K internal PU for RTC_CLK
,External PU/PD is not required.



REQUIRED STRAPS

		PCLK_MINI		PCLK_591	
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INT. PLL48	CPU IF=K8	H, H = PCI ROM H, L = SPI ROM
PULL LOW	IGNORE DEBUG STRAPS	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4	L, H = LPC ROM L, L = FWH ROM



SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET	Use Long Reset	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	boot fail time disabled
PULL LOW	USE SHORT RESET	Use Short Reset	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	boot fail time enabled

SB460 Only

SB600 Only

SB600 Only



QUANTA
COMPUTER

Title

SB600M STRAPS

Size

Document Number
FX2

Rev
1A

Date:

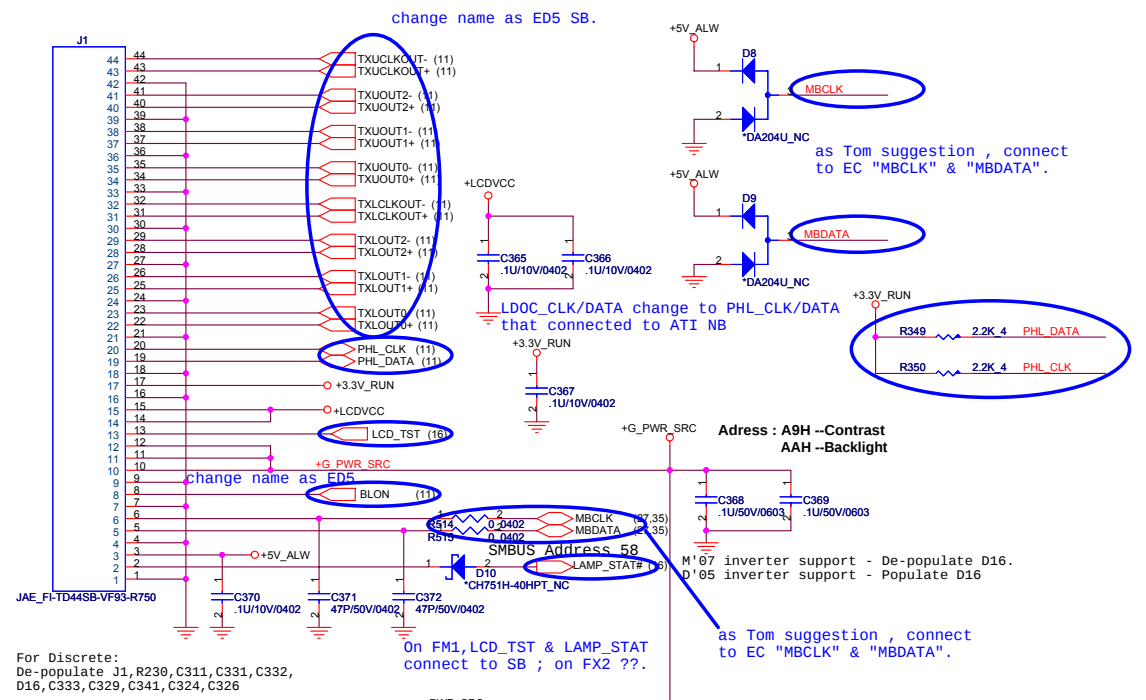
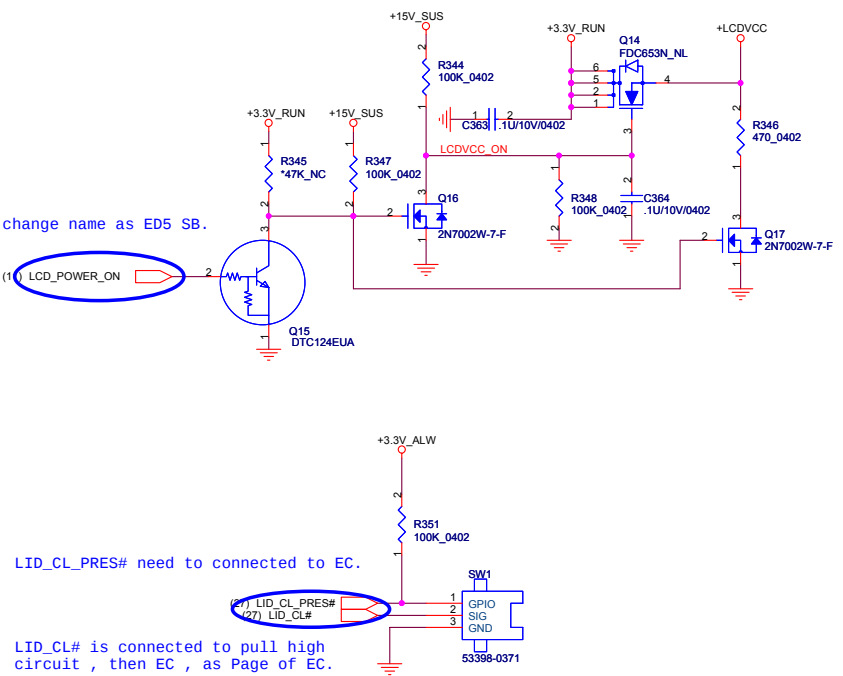
Friday, May 05, 2006

Sheet 17 of 47

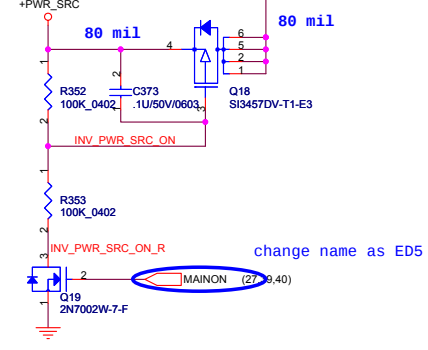
change name as ED5 SB.

LID_CL_PRES# need to connected to EC.

LID_CL# is connected to pull high circuit , then EC , as Page of EC.

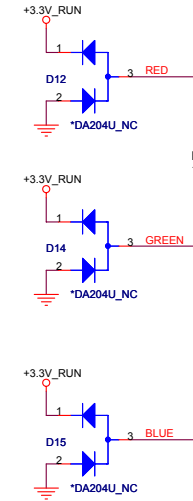
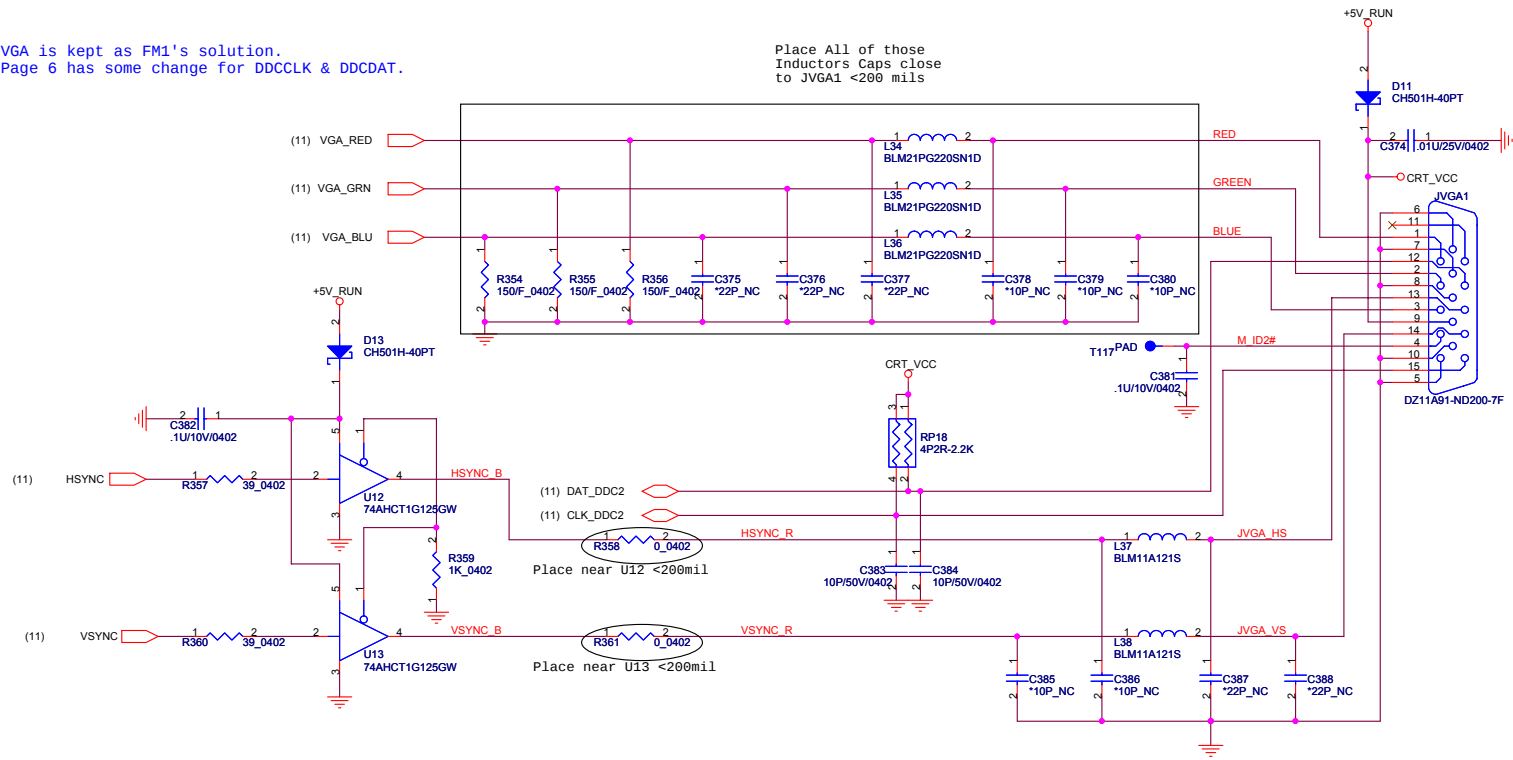


For Discrete:
De-populate J1, R230, C311, C331, C332,
D16, C333, C329, C341, C324, C326



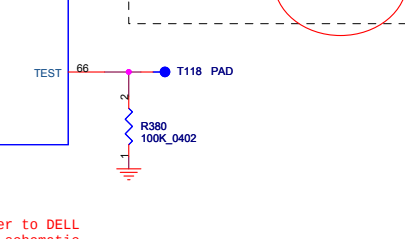
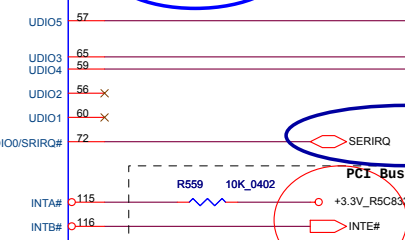
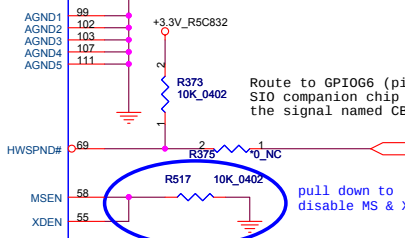
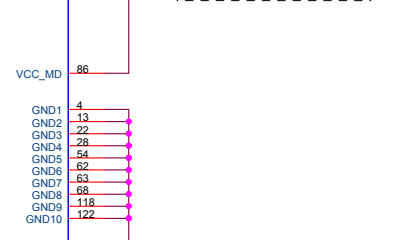
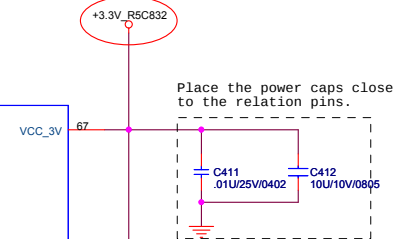
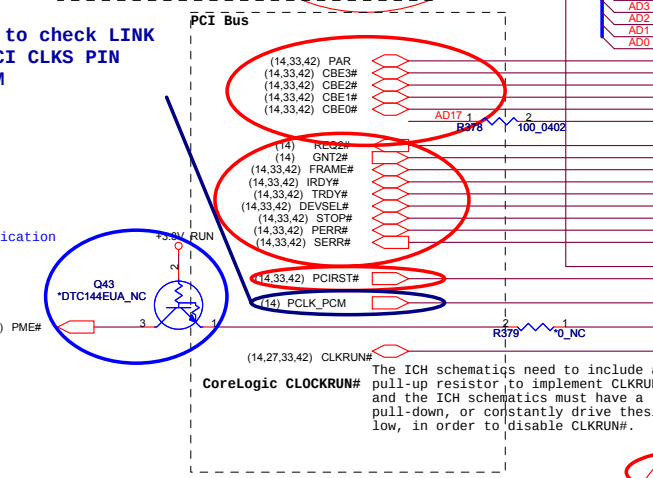
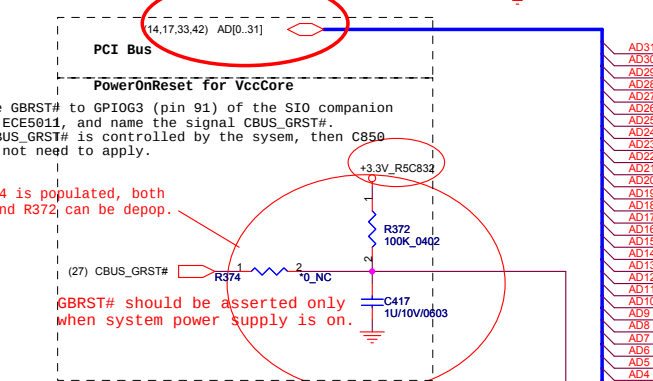
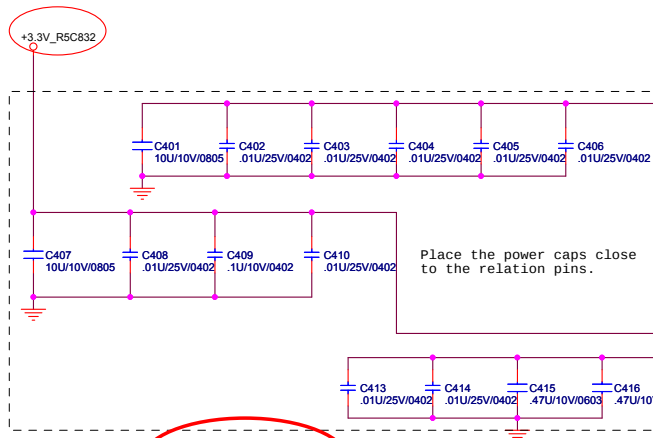
VGA is kept as FM1's solution.
Page 6 has some change for DDCCLK & DDCDAT.

Place All of those
Inductors Caps close
to JVGA1 <200 mils

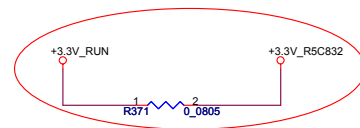


Place D4, D5, D6 close
to JVGA1 <200 mils

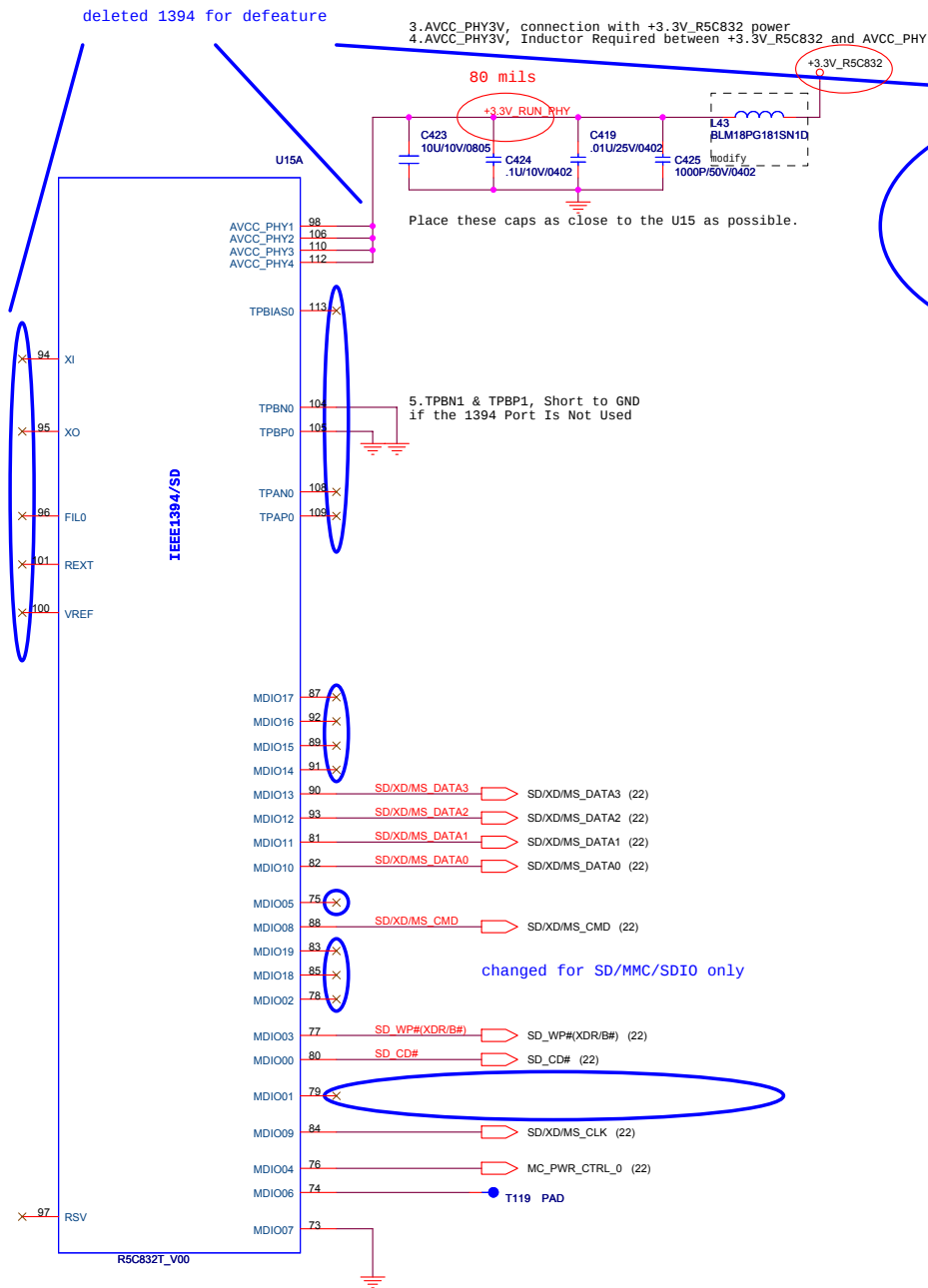
delete Svideo for defeature



— change name for ED5
— copy ED5 to FX2
— Waiting to check

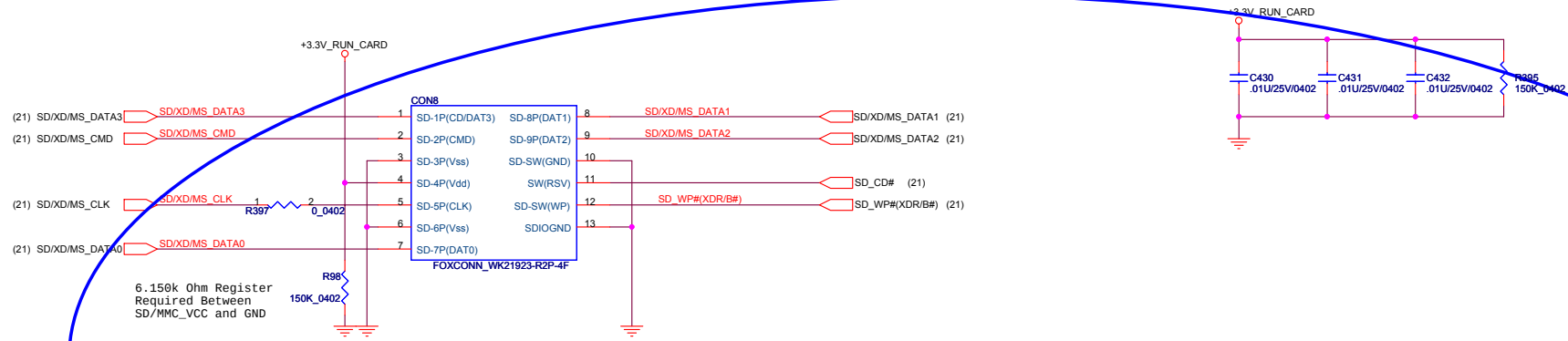


Waiting to check
LINK SB460
SERIRQ PIN
PCLK_PCM



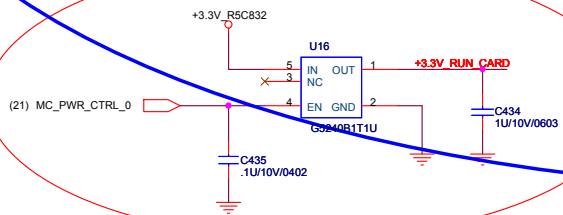
DO NOT INSERT SD/MMC SIMULTANEOUSLY.

changed for SD/MMC/SDIO only

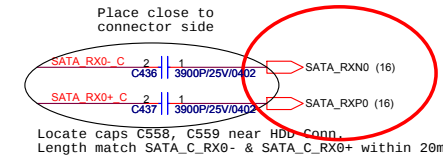
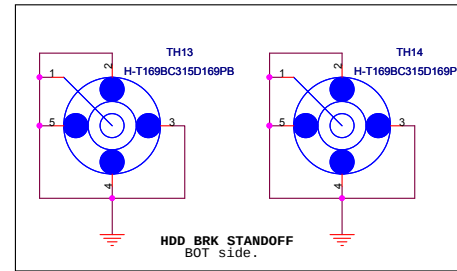
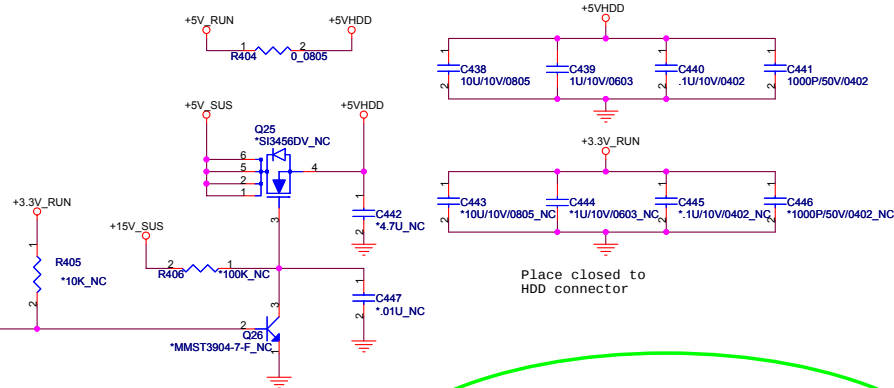


3 IN 1 CARD READER

For SD/MS power

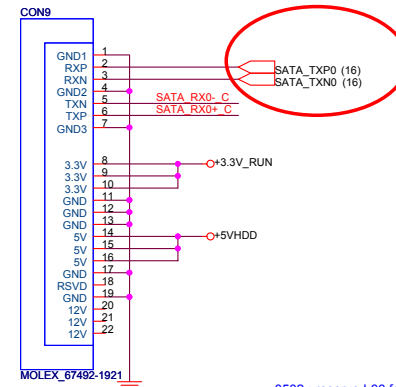


SATA HDD



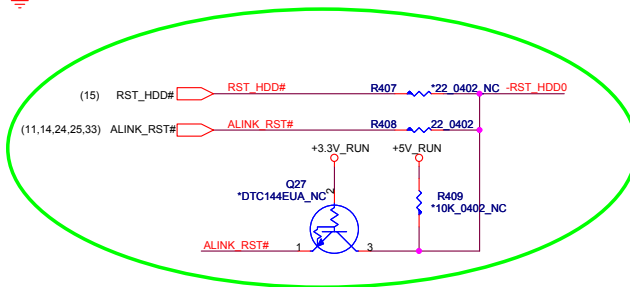
SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.

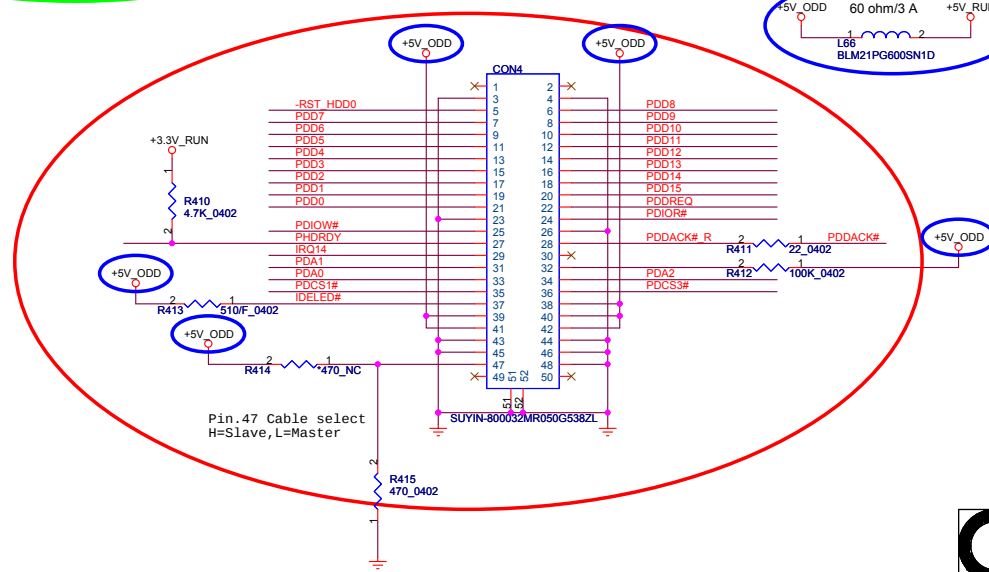
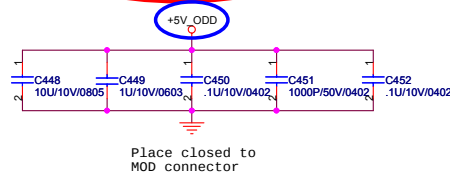
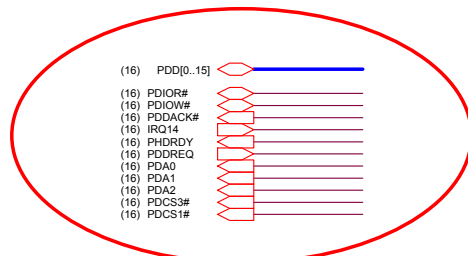
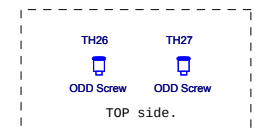


- change name for ED5
- copy ED5 to FX2
- Waiting to check

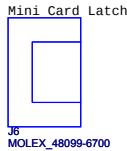
PATA ODD



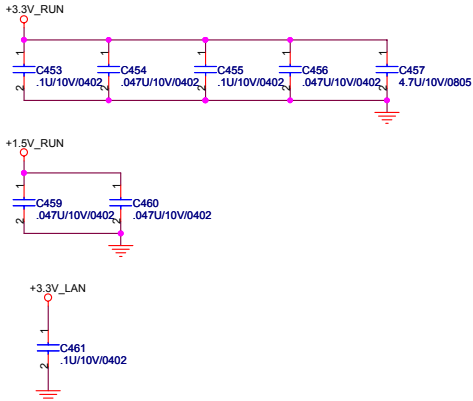
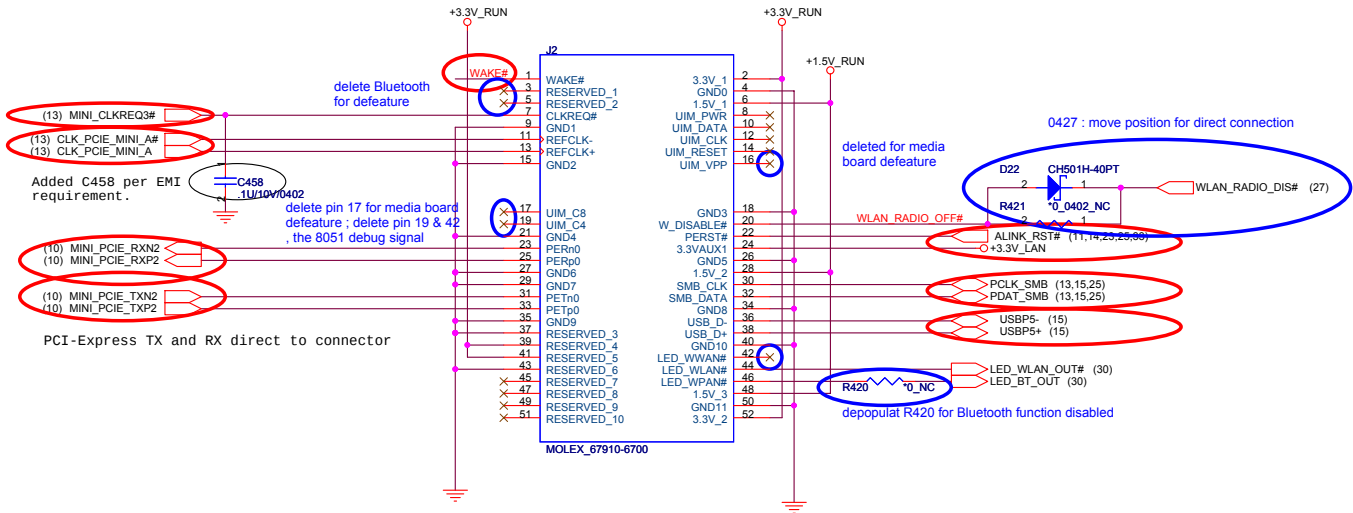
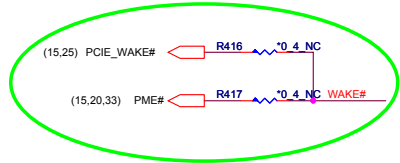
0502 : reserve L66 for current measurement , can be removed and short directly after RTS ; and change +5V_RUN to +5V_ODD for ODD side power



MINI CARD



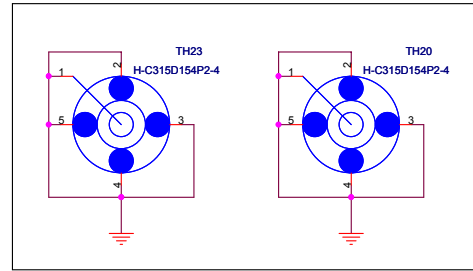
- change name for ED5
- copy ED5 to FX2
- Waiting to check



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Title			MINI Card
Size	Document Number	Rev	1A
FX2			
Date:	Friday, May 05, 2006	Sheet	24 of 47

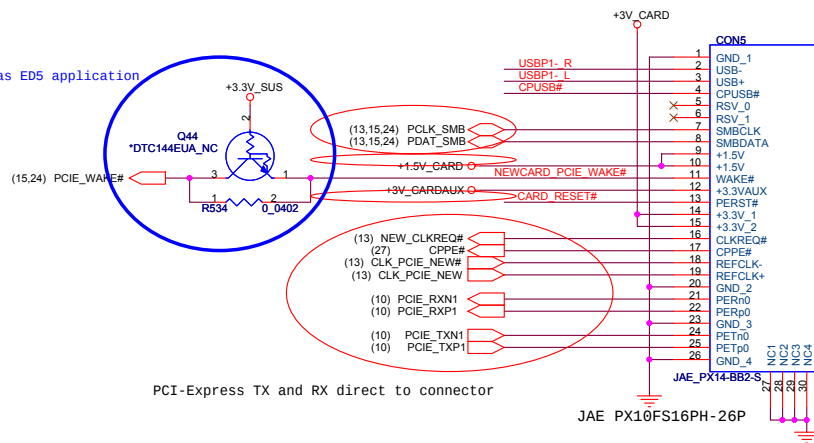
Express Card



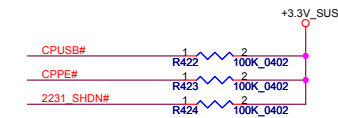
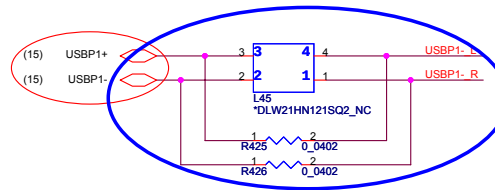
- change name for ED5
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NEW CARD GUIDE POST
TOP side.

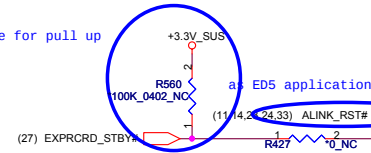
as ED5 application



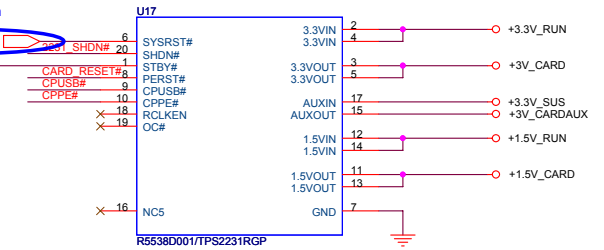
swap traces as "fx2_swap-0412"



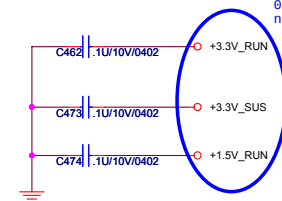
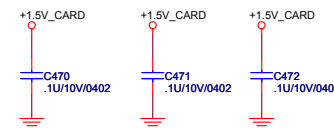
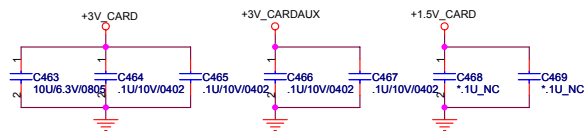
reserve for pull up



+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA



+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA



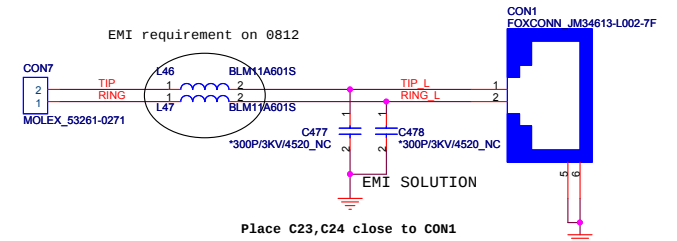
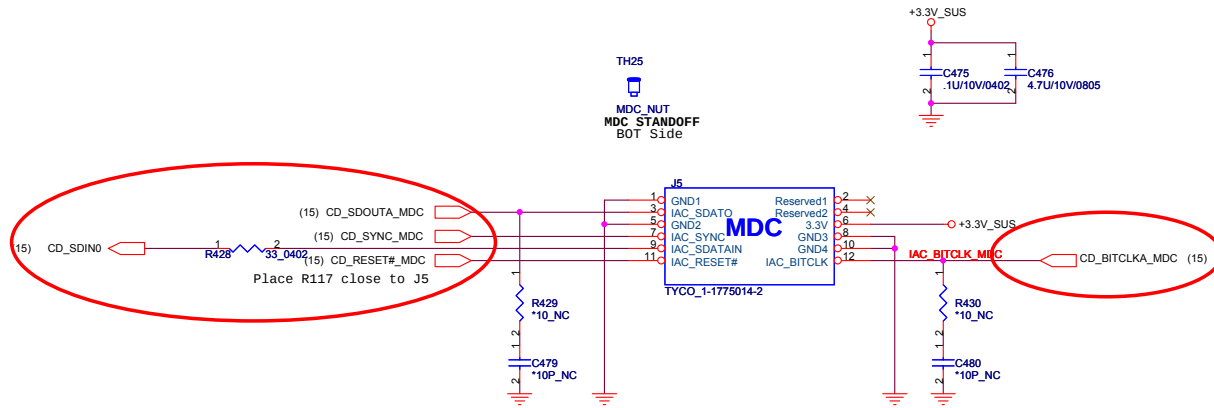
0427 : change from only net
name to symbol "power point"

MDC INTERFACE

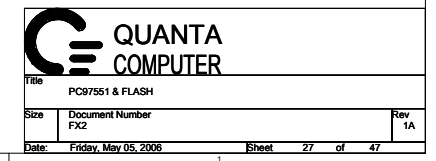
MDC Layout Notes

1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG (stranded or twisted pair wire)

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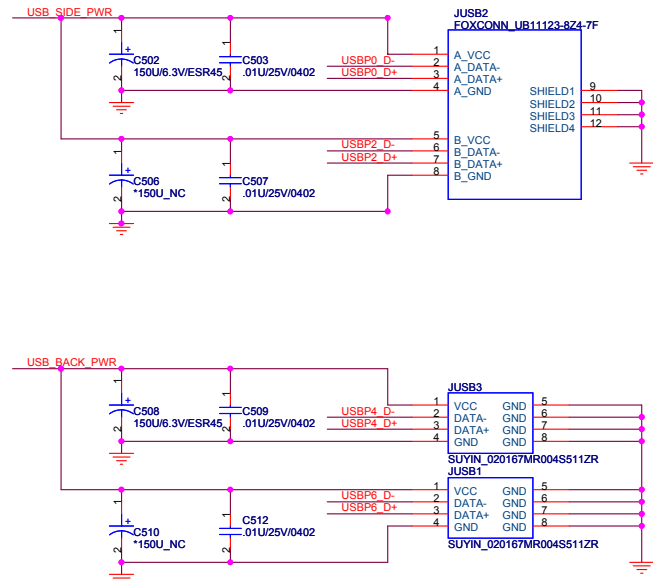
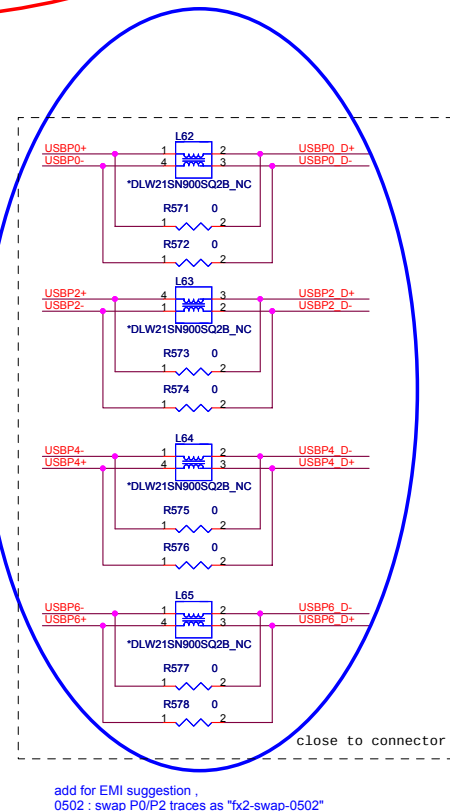
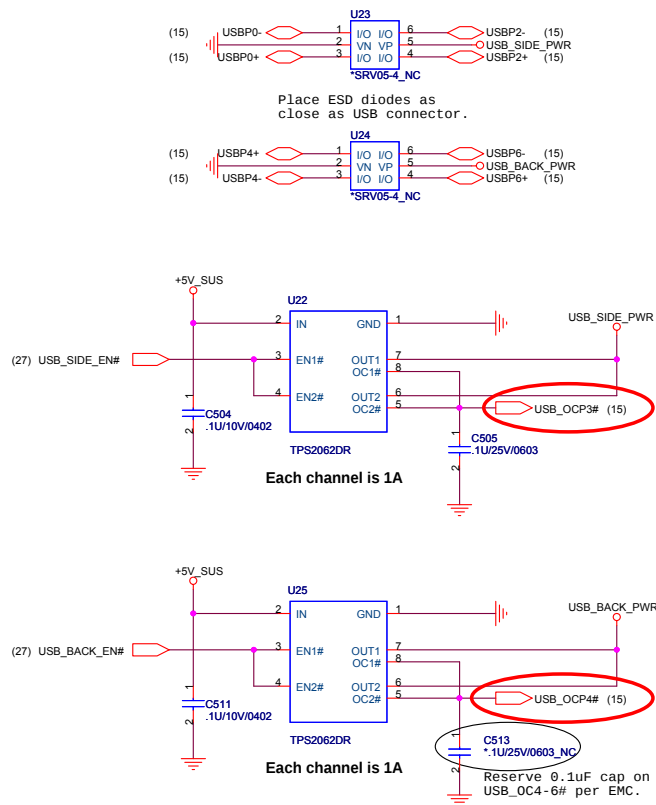


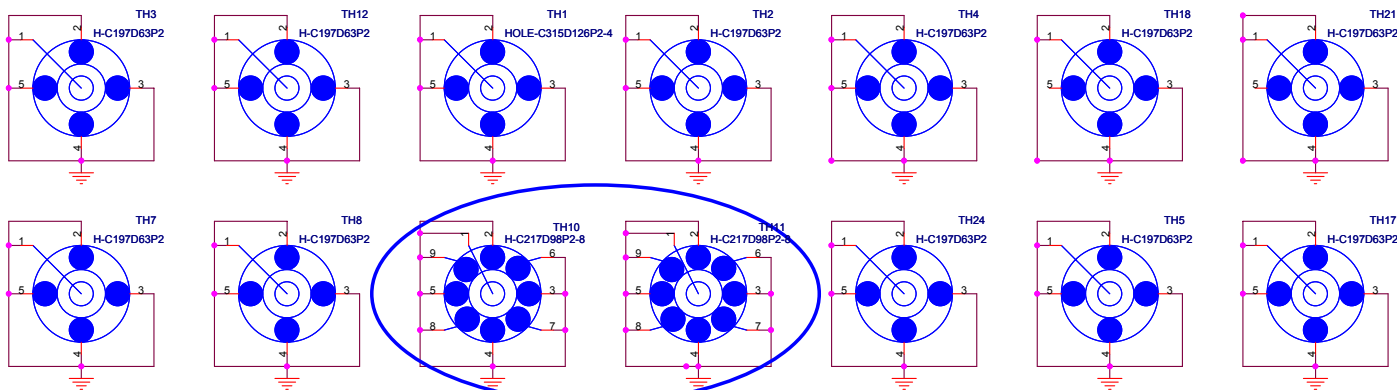
delete Bluetooth
for defeature



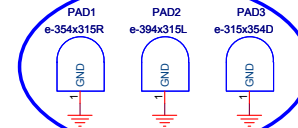
8Mbit (1M Byte), SPI

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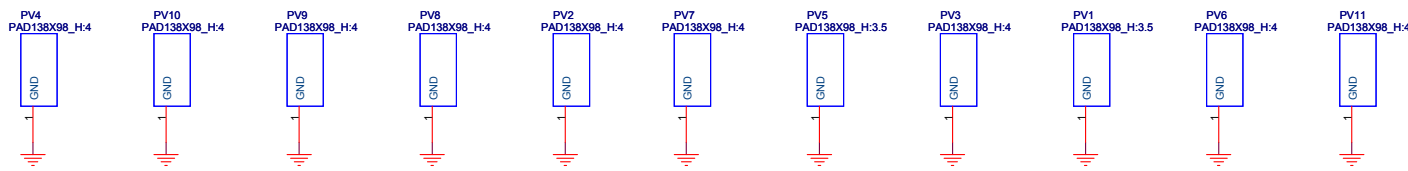




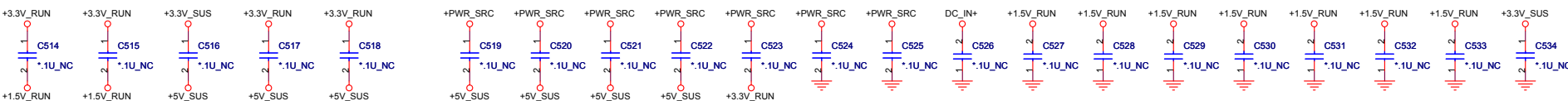
change footprint from
"H-C315D98P2-4" to "H-C217D98P2-8".



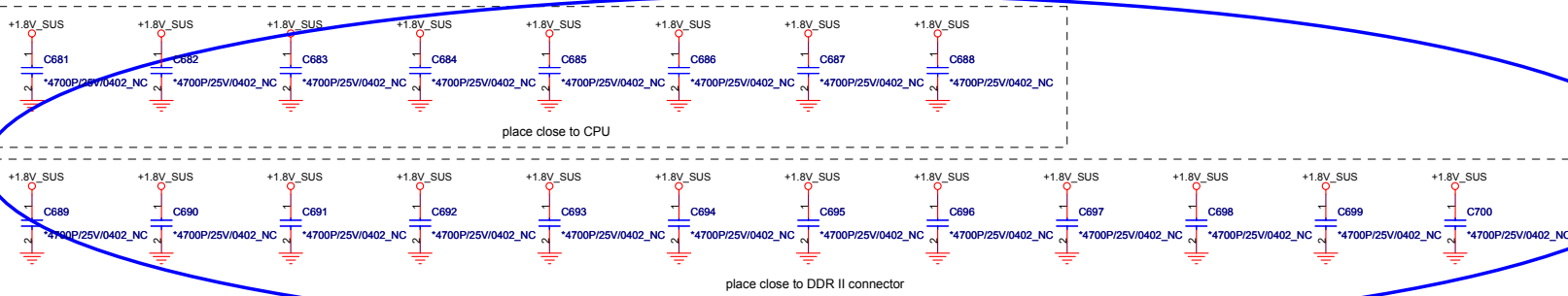
0427 : add 3 pads for EMI need

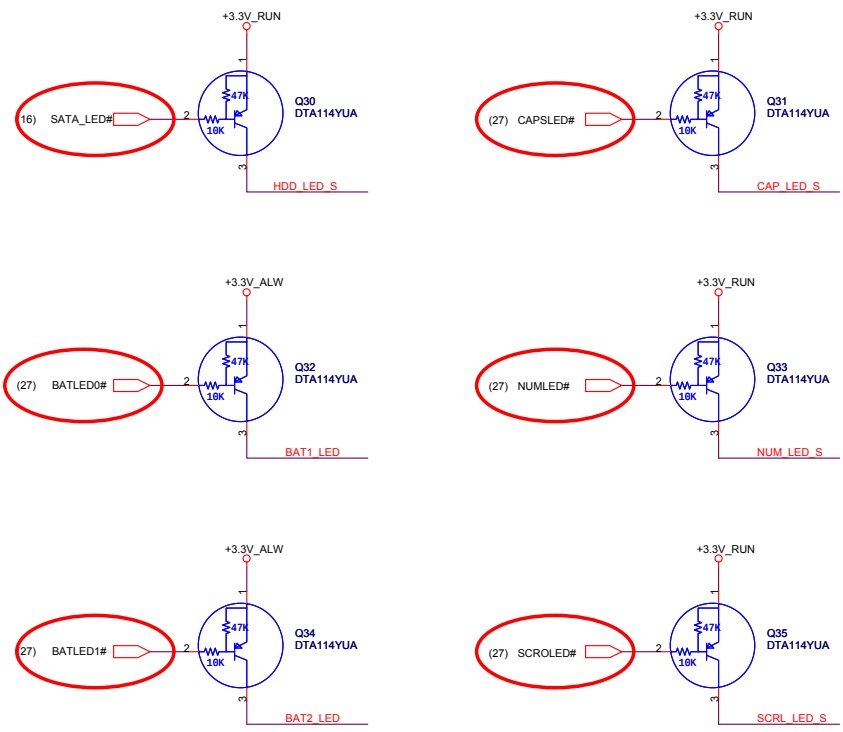


0505 : delete PV12 , caused interference with
power component , EMI confirm no concern

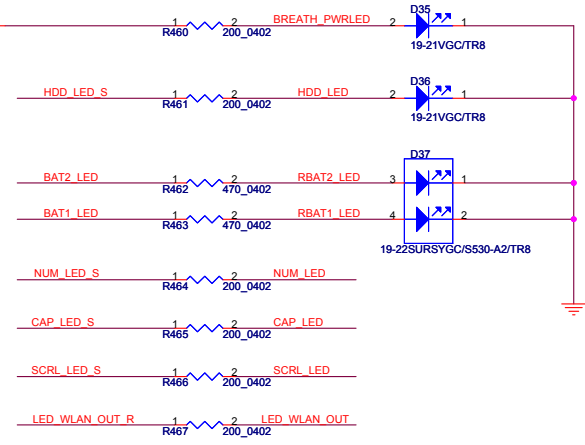
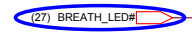


0502 : reserve 20 pcs of 4700pF stitching Cap. from +1.8V_SUS to GND for EMI concern

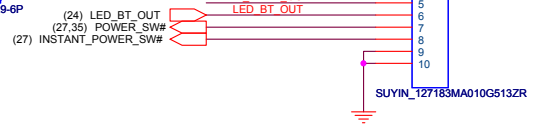
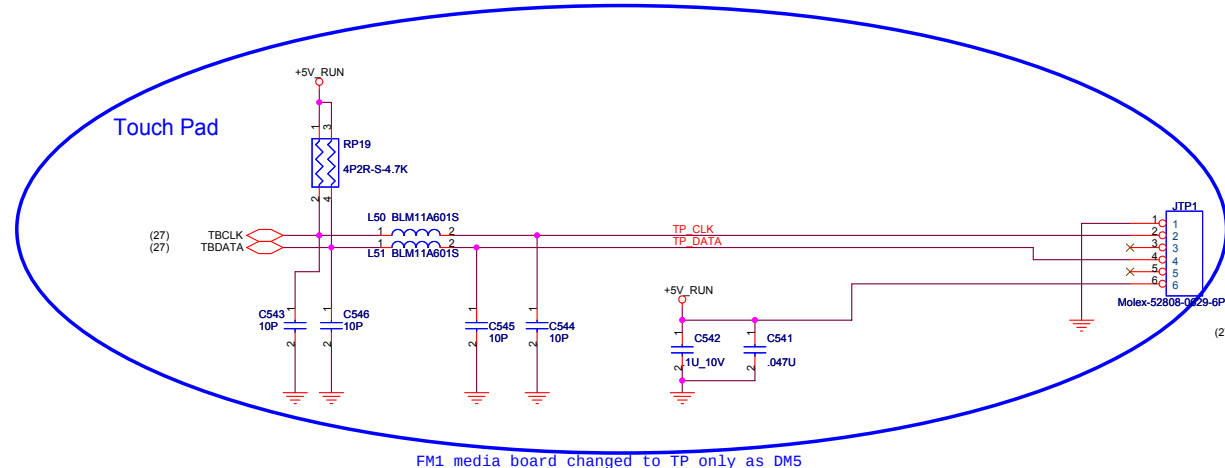
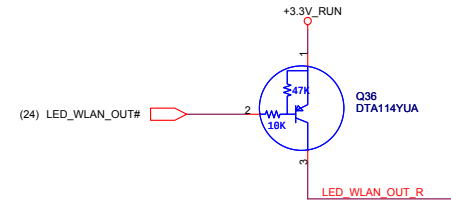


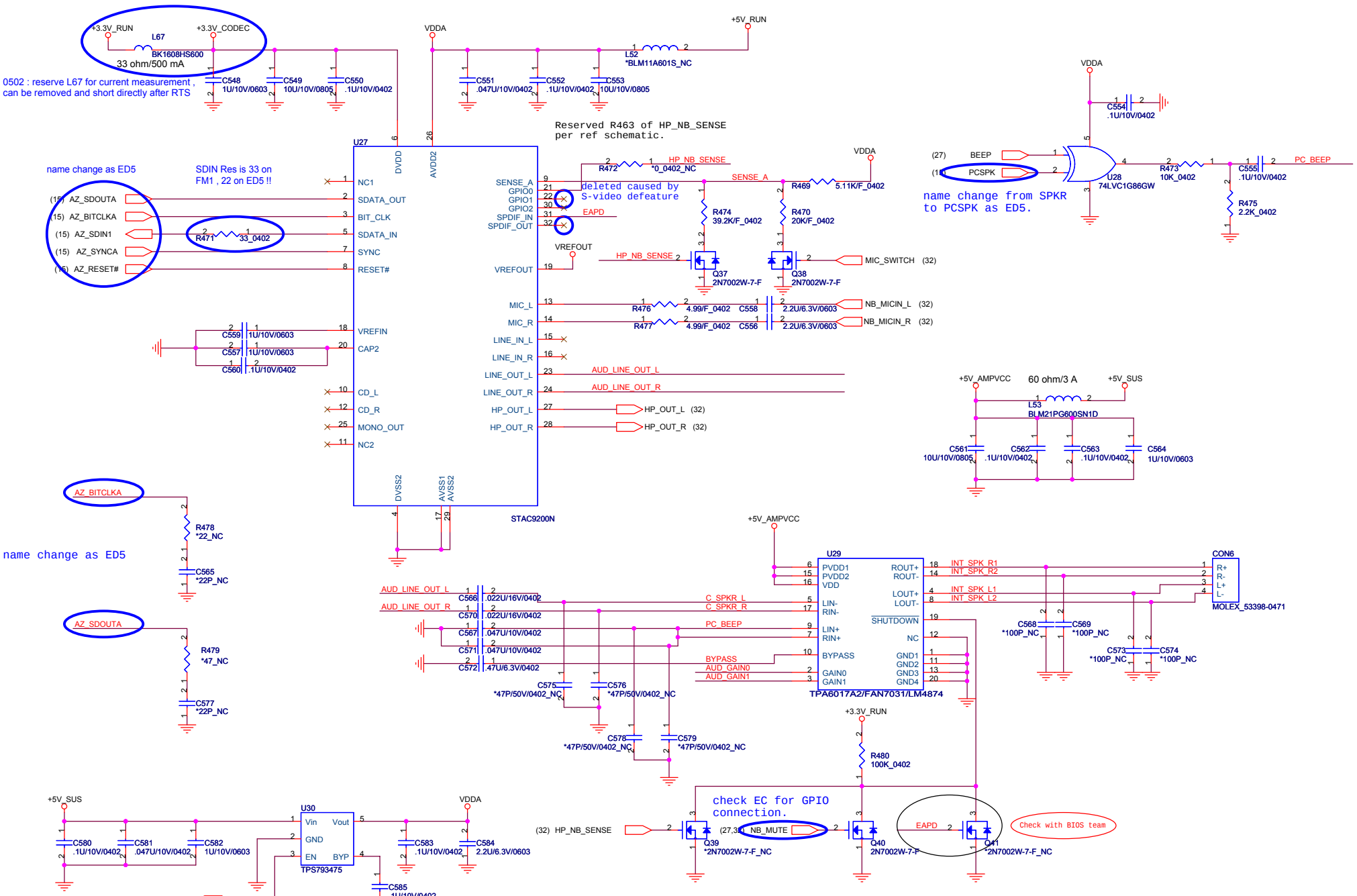


0427 : change from
BREATH_LED to BREATH_LED#



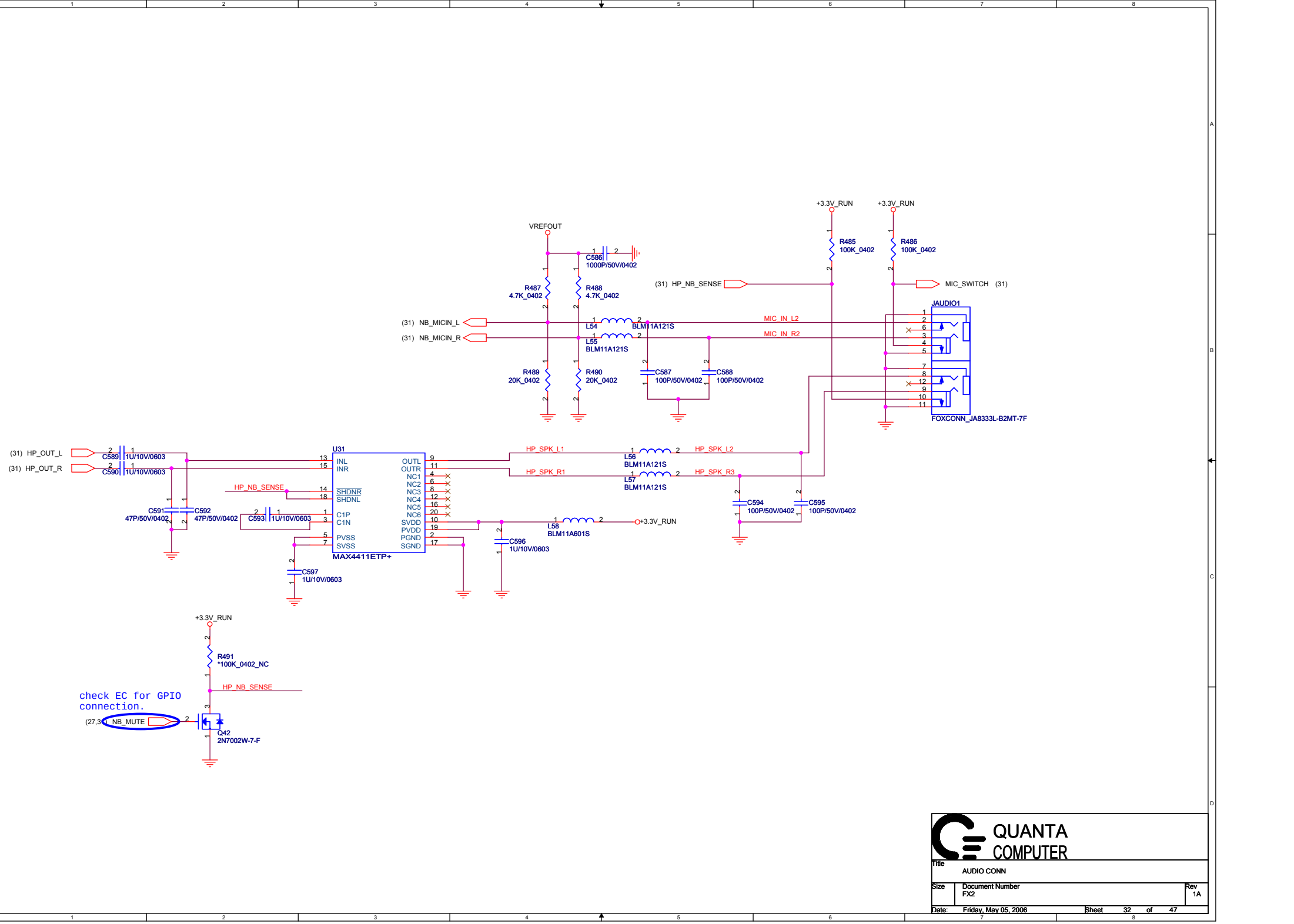
— change name for ED5
— copy ED5 to FX2
— Waiting to check

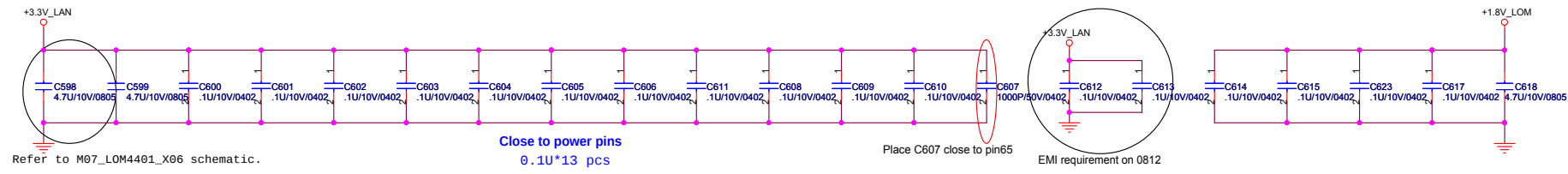




GAIN0	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB





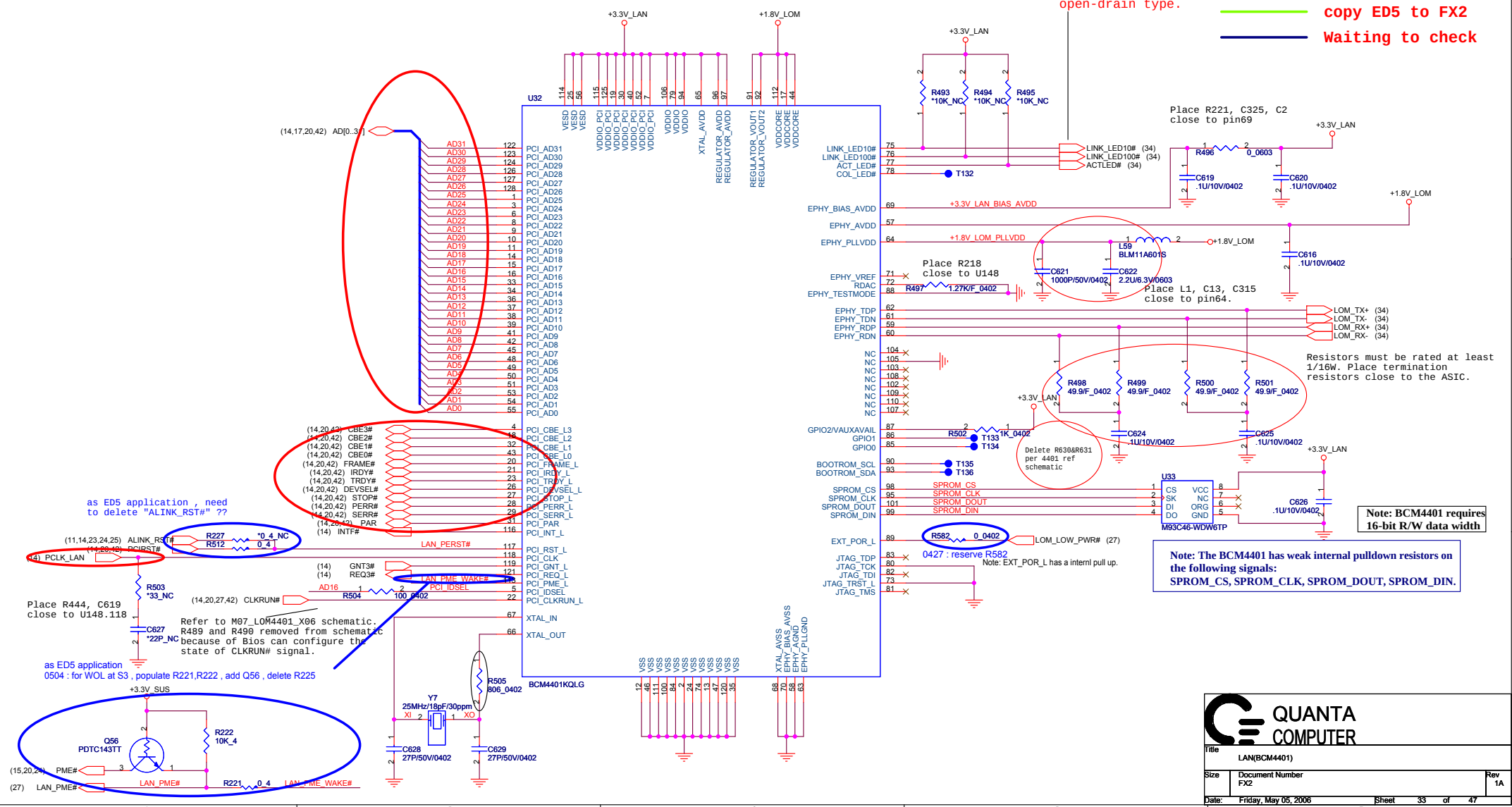


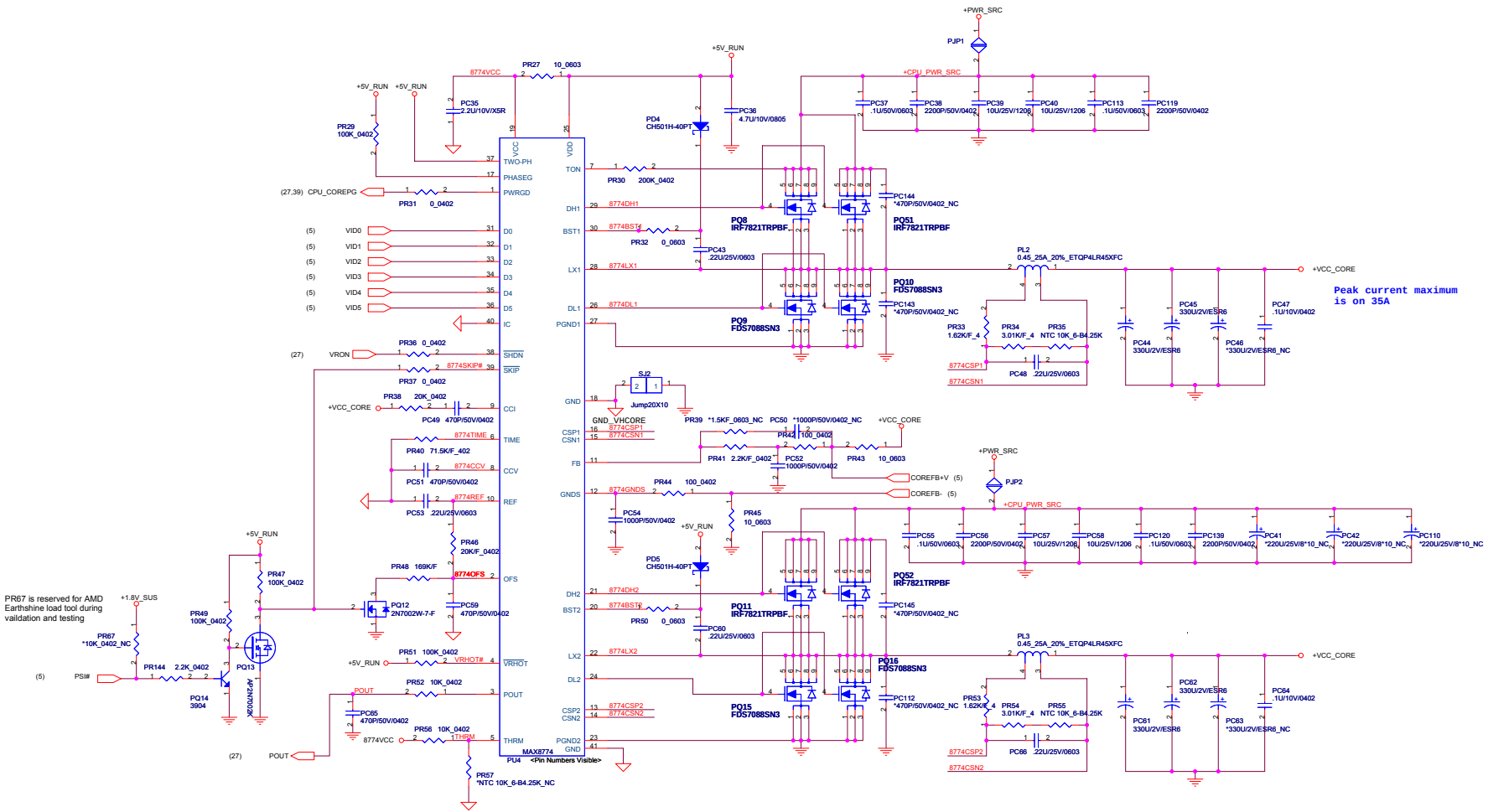
These three pin
LINK_LED10#,
LINK_LED100#,
ACT_LED are
open-drain type.

change name for ED5

copy ED5 to FX2

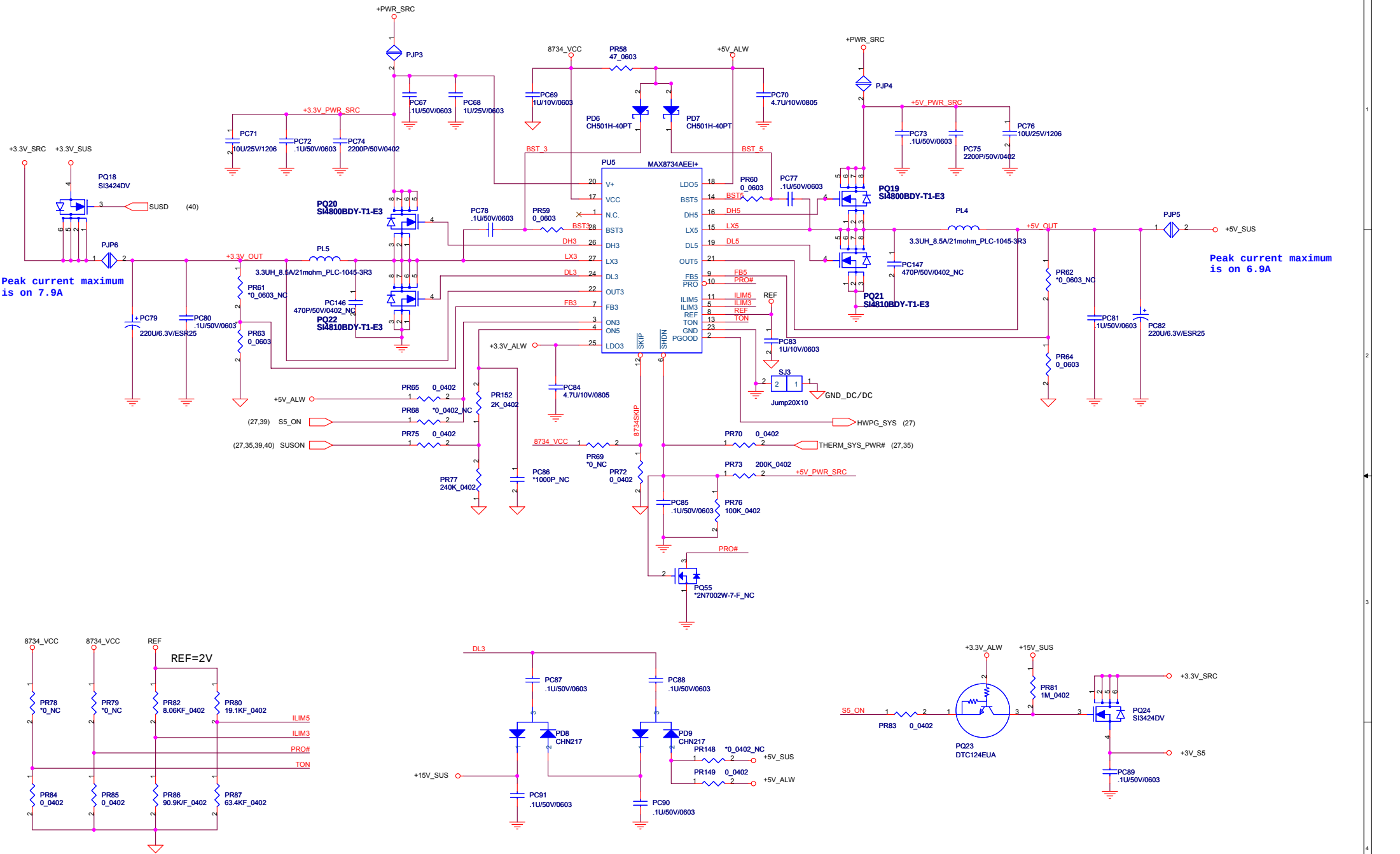
Waiting to check





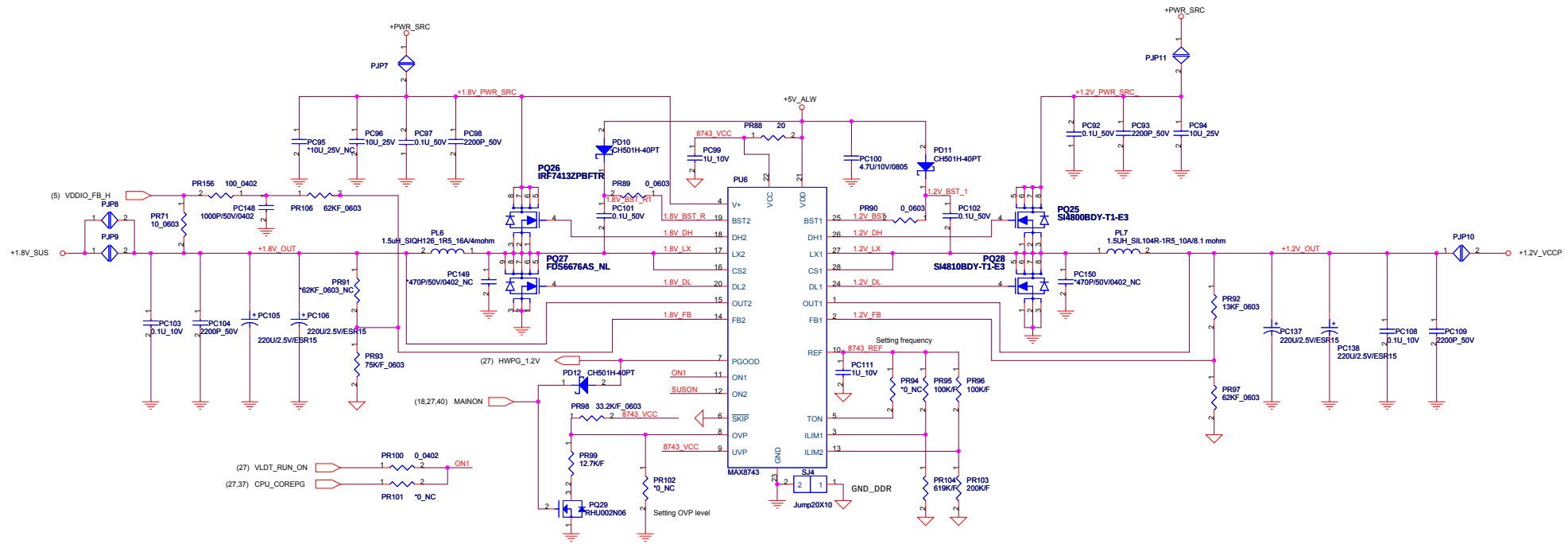
PR67 is reserved for AMD Earthshine load tool during validation and testing

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V	1	0	0	0	0	0	0.7500V
0	0	0	0	0	1	1.5250V	1	0	0	0	0	1	0.7375V
0	0	0	0	1	0	1.5000V	1	0	0	0	1	0	0.7250V
0	0	0	0	1	1	1.4750V	1	0	0	0	1	1	0.7125V
0	0	0	1	0	0	1.4500V	1	0	0	1	0	0	0.7000V
0	0	0	1	0	1	1.4250V	1	0	0	1	0	1	0.6875V
0	0	0	1	1	0	1.4000V	1	0	0	1	1	0	0.6750V
0	0	0	1	1	1	1.3750V	1	0	1	0	0	0	0.6625V
0	0	1	0	0	0	1.3500V	1	0	1	0	0	1	0.6500V
0	0	1	0	0	1	1.3250V	1	0	1	0	1	0	0.6375V
0	0	1	0	1	0	1.3000V	1	0	1	0	1	1	0.6250V
0	0	1	0	1	1	1.2750V	1	0	1	1	0	0	0.6125V
0	0	1	1	0	0	1.2500V	1	0	1	1	0	1	0.6000V
0	0	1	1	0	1	1.2250V	1	0	1	1	1	0	0.5875V
0	0	1	1	1	0	1.2000V	1	0	1	1	1	1	0.5750V
0	0	1	1	1	1	1.1750V	1	0	1	1	1	1	0.5625V
0	1	0	0	0	0	1.1500V	1	0	1	0	0	0	0.5500V
0	1	0	0	0	1	1.1250V	1	0	1	0	0	1	0.5375V
0	1	0	0	1	0	1.1000V	1	0	1	0	1	0	0.5250V
0	1	0	0	1	1	1.0750V	1	0	1	0	1	1	0.5125V
0	1	0	1	0	0	1.0500V	1	0	1	0	1	1	0.5000V
0	1	0	1	0	1	1.0250V	1	0	1	1	0	0	0.4875V
0	1	0	1	1	0	1.0000V	1	0	1	1	0	1	0.4750V
0	1	1	0	0	0	0.9750V	1	1	0	0	0	0	0.4625V
0	1	1	0	0	1	0.9500V	1	1	0	0	0	1	0.4500V
0	1	1	0	1	0	0.9250V	1	1	0	0	1	0	0.4375V
0	1	1	0	1	1	0.9000V	1	1	0	0	1	1	0.4250V
0	1	1	1	0	0	0.8750V	1	1	0	1	0	0	0.4125V
0	1	1	1	0	1	0.8500V	1	1	0	1	0	1	0.4000V
0	1	1	1	1	0	0.8250V	1	1	1	0	0	0	0.3875V
0	1	1	1	1	1	0.8000V	1	1	1	1	0	0	0.3750V
0	1	1	1	1	1	0.7750V	1	1	1	1	1	0	0.3625V

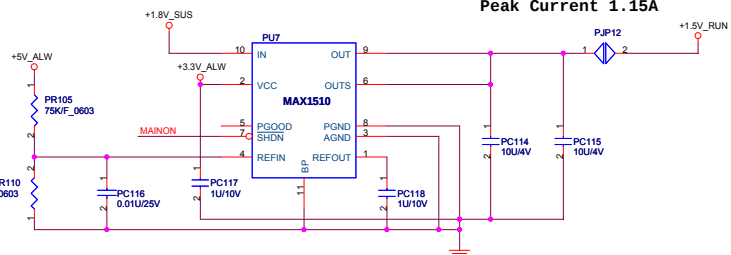


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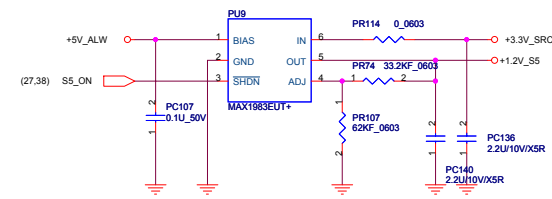
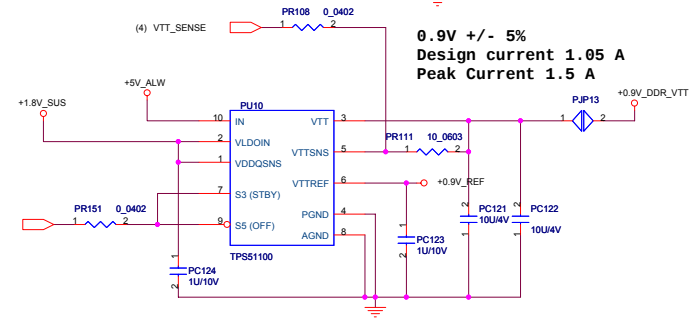
Title			SYSTEM (MAX8734)
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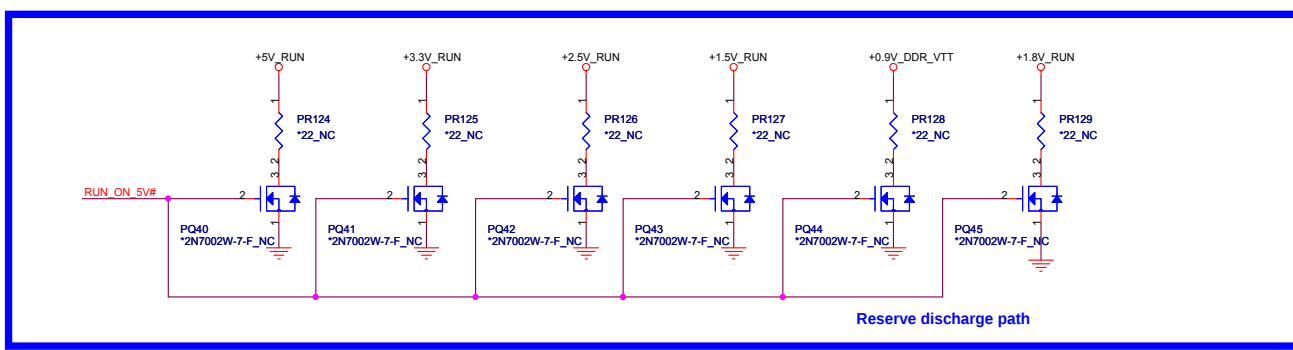
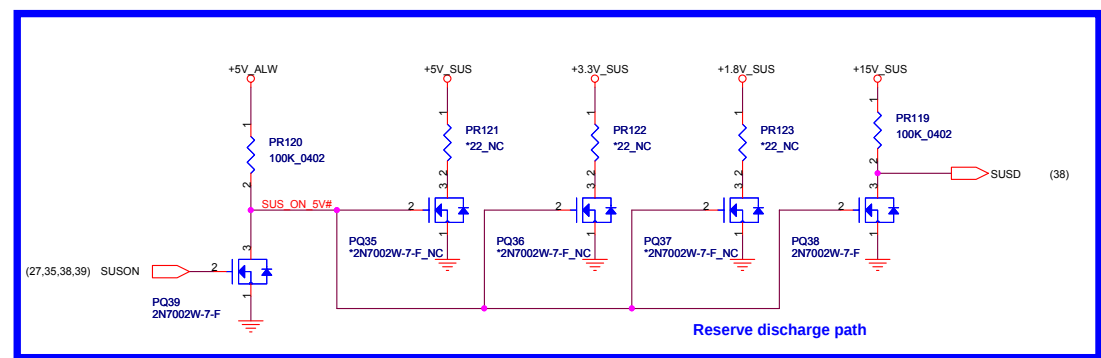
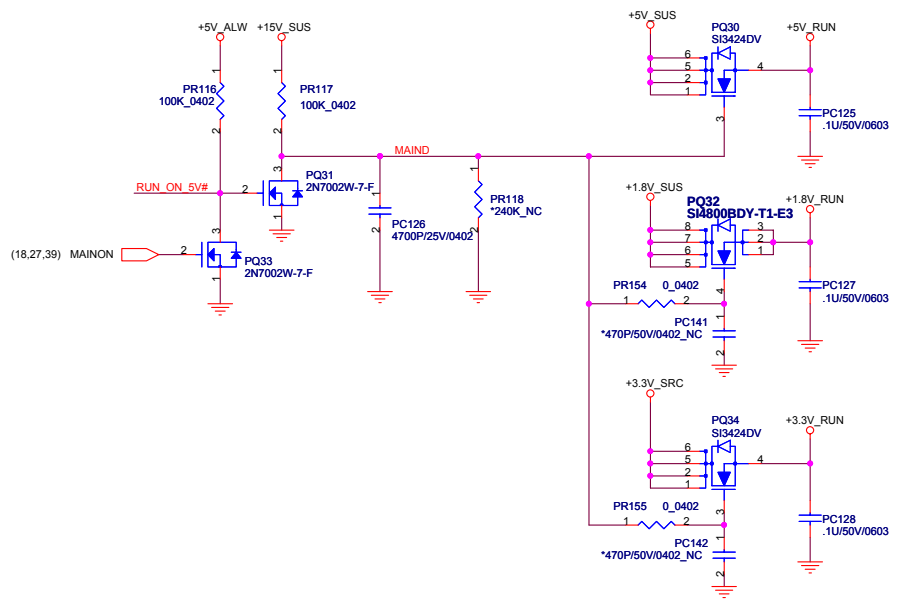


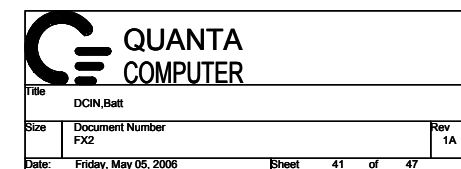
1.5 Volt +/- 5%
Design current 0.7A
Peak Current 1.15A



0.9V +/- 5%
Design current 1.05 A
Peak Current 1.5 A

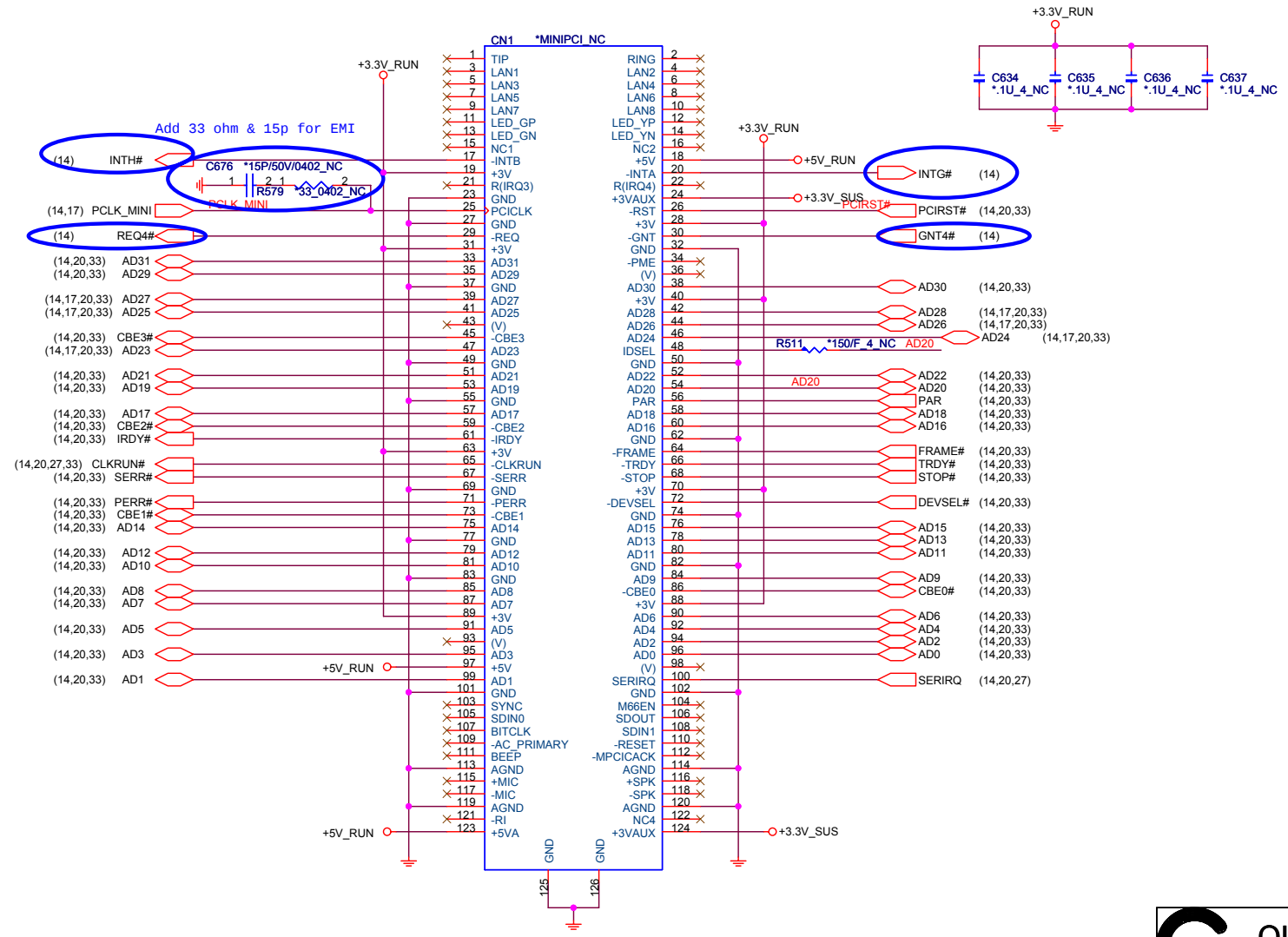






ID Select : AD20
Interrupt Pin : INTG# , INTH#
Request Indicate : REQ4#
Grant Indicate : GNT4#

DEBUG PURPOSE ONLY



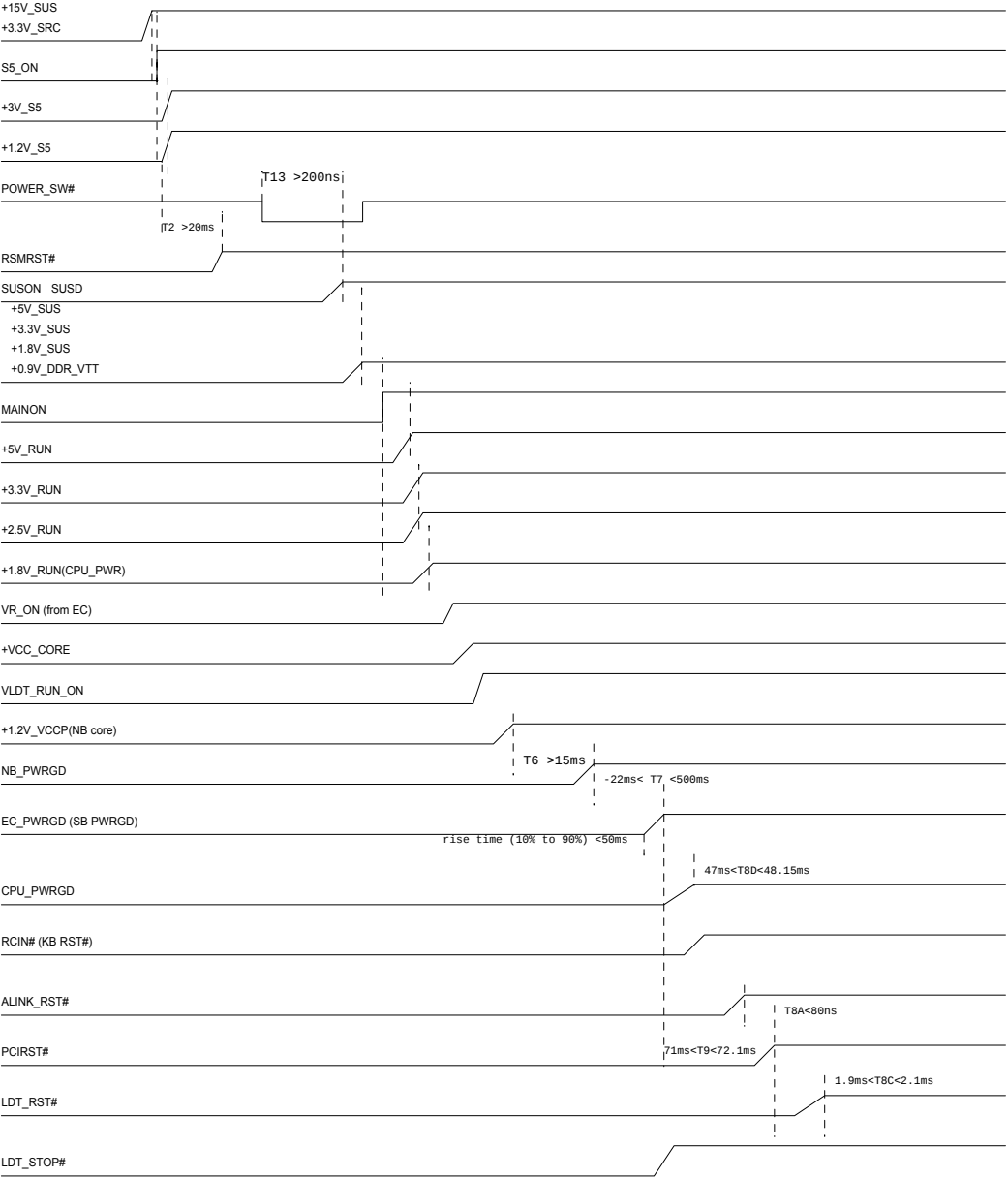
MPC



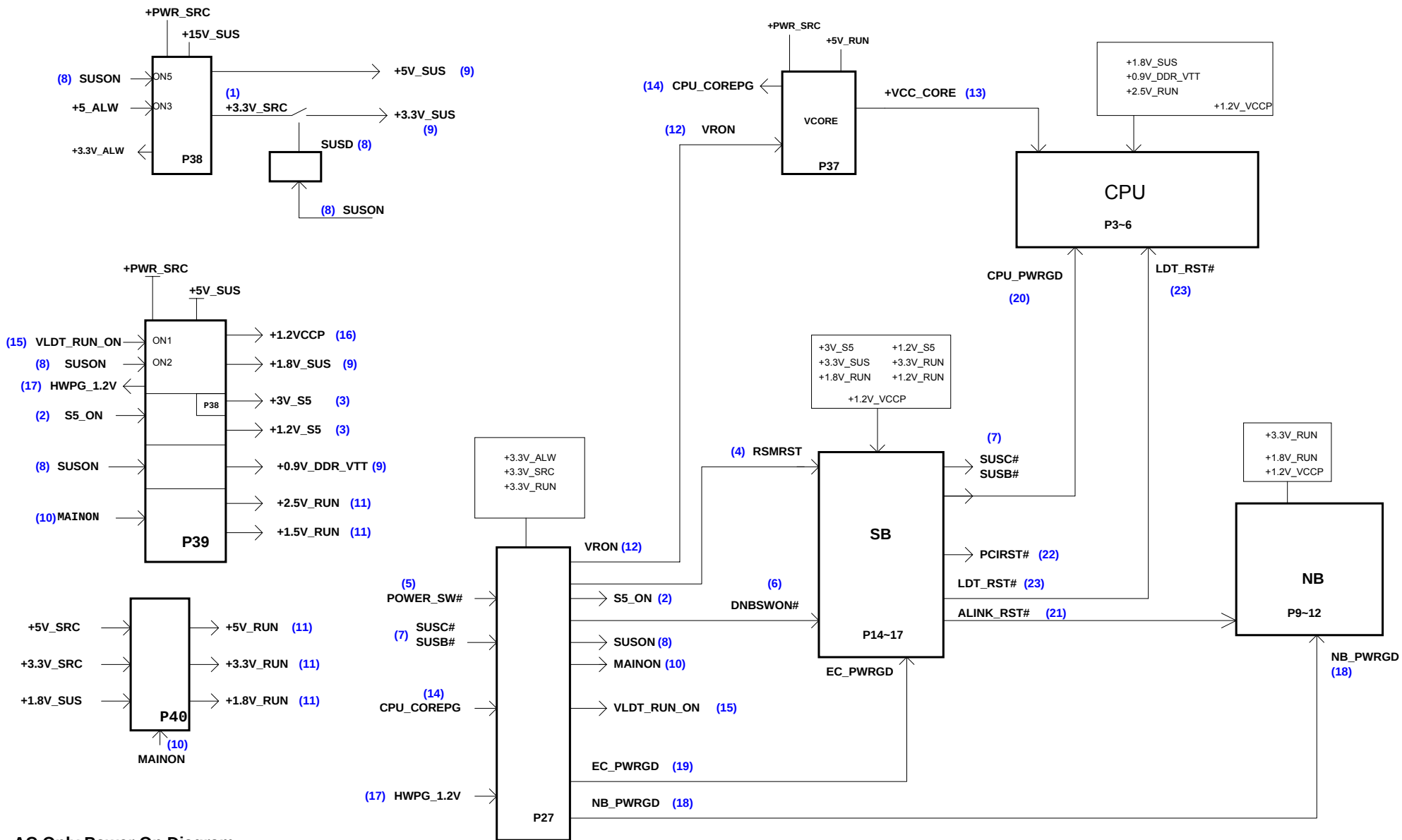
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Title MINI PCI(for debug)		
Size FX2	Document Number	Rev 1A
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Power On Sequence



T6: NB core voltage to NB_PWRGD
T7: NB_PWRGD to SB_PWRGD
T8D: SB_PWRGD to CPU_PWRGD
T8A: ALINK_RST# to PCIRST#
T9: SB_PWRGD to PCIRST#
T8C: PCIRST# to LDT_RST#



AC Only Power On Diagram

- | | | | |
|----------------------|-------------------------|------------------|-----------------|
| (1) +3.3V_SRC | (8) SUSON, SUSD | (13) +VCC_CORE | (20) CPU_PWRGD |
| (2) S5_ON | (9) +5V_SUS | (14) CPU_COREPG | (21) ALINK_RST# |
| (3) +3V_S5, +1.2V_S5 | (10) MAINON | (15) VLDT_RUN_ON | (22) PCI_RST# |
| (4) RSMRST | (11) +5V_RUN, +3.3V_RUN | (16) +1.2_VCCP | (23) LDT_RST# |
| (5) POWER_SW# | (12) VRON | (17) HWPG_1.2V | |
| (6) DNBSWON# | | (18) NB_PWRGD | |
| (7) SUSC#, SUBS# | | (19) EC_PWRGD | |

