UM8B DIS SYSTEM DIAGRAM

+3V/+5V PG.34
+1.05V/+1.8V PG.36
CPU Core PG.39
VGA Core/+1.1V PG.38
+1.5V/+0.75V PG.35
+1.05VTT PG.37
UMA VGACORE
Charger PG.33

14.318MHz
CLOCK GEN PG.2

SODIMM1 Max. 4GB PG.12
DDR3 Channel A
SODIMM2 Max. 4GB PG.13
DDR3 Channel B

INTEL Arrandale
37.5mm X 37.5mm
989pin PGA
TDP 35W
PG.3~6

PCI-E x16

ATI Madison
29mm X 29mm
PG.14~21

HDMI
HDMI PG.24
CRT
DB1
CRT
LVDS
LVDS PG.22

DDR3 700MHz
VRAM
64Mx16x4,64bit
PG.19,20

FDI
DMI

4M ROM PG.26

DB2

INTEL PCH
Ibex Peak-m
27mm X 25mm
1071pin FCBGA
TDP 5W
PG.7~11

SATA0
HDD PG.28
SATA1
ODD PG.28

FAN & THERMAL
GMT G990/
EMC1422-1-AIZL-TR PG.30

LANE0
WWAN
USB 2.0 PORT5
PCI-E x 1
LANE6
LAN
Atheros/AR8152
10/100
LANE1
WLAN
USB 2.0 PORT4
PCI-E x 1
LANE5
eSATA
SN75LVCP412
Combo port
PG.27
USB 2.0 PORT8

USB2.0 X1
USB2.0 X1
Webcam PG.22
USB 2.0
PORT0,1,7
PORT0,1,7
PORT11
PORT12
PORT9
Card Reader
RTS5138
PG.23
BT
BT365
PG.31

Stackup
TOP
GND
IN1
IN2
VCC
IN3
GND
BOT

LPC
KBC
ITE 8502
PG.25
KB PG.28
TP PG.28
1M ROM PG.26

Azalia
AUDIO CODEC
ALC269-GR
Speaker PG.25
HP/MIC
Analog MIC

Quanta Computer Inc.
PROJECT : UM8B DIS
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02

PDC (Power Cap quantities follow UM3)

25mA

+1.05V_PCH — L25 HCB1608KF-181T15_6 — +VDDIO_CLK

C327 0.1U/ 10V/X7R
C320 0.1U/ 10V/X7R
C323 10U/6.3V 8/X5R

Place each 0.1uF cap close to pin

8/20 Wait Victor check

300mA

+3.3V_RUN — L27 HCB1608KF-181T15_6 — +VDDSE_CLK

C352 10U/6.3V 8/X5R
C336 0.1U/ 10V/X7R
C353 0.1U/ 10V/X7R
C354 0.1U/ 10V/X7R
C322 0.1U/ 10V/X7R
C321 0.1U/ 10V/X7R

Place each 0.1uF cap close to pin

Check CLK P/N and footprint

U10 — 9LRS3197 — QFN32

+VDDSE_CLK: VDD_LCD (5), VDD_REF (29)
+VDDIO_CLK: VDD_CPU_IO (18), VDD_SRC_IO (15)
VDD_USB (1), VDD_SRC (17), VDD_CPU (24)
18,25,30 SMBDAT2 — SDATA (31)
18,25,30 SMBCLK2 — SCLK (32)
+3.3V_RUN — R196 10K — R213 33/J_4 — CPU_SEL
8 CLK_PCH_14M — CLK_PCH_14M — C338 *10P/50V_4_NC/COG
CPU_STOP# (16)
REF_0/CPU_SEL (30)
CK_PWRGD_R — CK_PWRGD/PD#_3.3 (25)
XTAL_OUT — XOUT (27)
XTAL_IN — XIN (28)
VSS_SATA (9), VSS_USB (2), VSS_LCD (8)

CPU-0 (23) — CLK_BUF_BCLKP_R
CPU-0# (22) — CLK_BUF_BCLKN_R
CPU-1 (20)
CPU-1# (19)
DOT96T_LPR (3) — CLK_BUF_DREFCLKP_R
DOT96C_LPR (4) — CLK_BUF_DREFCLKN_R
SRC-1 (13) — CLK_BUF_PCIE_3GPLLP_R
SRC-1# (14) — CLK_BUF_PCIE_3GPLLN_R
SATA (10) — CLK_BUF_DREFSSCLKP_R
SATA# (11) — CLK_BUF_DREFSSCLKN_R
27MHz_nonSS (6) — CLK_VGA_27M_NOSS
27MHz_SS (7) — CLK_VGA_27M_SS
GND (33), VSS_REF (26), VSS_CPU (21), VSS_SRC (12)

Place within 0.5" of C/G

RP5 0X2: CLK_BUF_BCLKP_R → CLK_BUF_BCLKP 8; CLK_BUF_BCLKN_R → CLK_BUF_BCLKN 8
RP8 0X2: CLK_BUF_DREFCLKP_R → CLK_BUF_DREFCLKP 8; CLK_BUF_DREFCLKN_R → CLK_BUF_DREFCLKN 8
RP6 0X2: CLK_BUF_PCIE_3GPLLP_R → CLK_BUF_PCIE_3GPLLP 8; CLK_BUF_PCIE_3GPLLN_R → CLK_BUF_PCIE_3GPLLN 8
RP7 0X2: CLK_BUF_DREFSSCLKP_R → CLK_BUF_DREFSSCLKP 8; CLK_BUF_DREFSSCLKN_R → CLK_BUF_DREFSSCLKN 8
R217 33/J_4 — R216 *33/J_4_NC: CLK_VGA_27M_NOSS → EVGA-XTALI 15; CLK_VGA_27M_SS → CLK_27M_SS 15

Discrete only

C351 *10P/50V_4_NC/COG

Place R8044 within 0.5" of C/G

+3.3V_RUN — R212 *10K_NC — CPU_SEL — R209 10K

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

BOM check

+3.3V_RUN — R199 1K/J_4 — CK_PWRGD_R
Q13 FDN357N
39 VR_PWRGD_CLKEN# — 2
R201 *100K/F_4_NC

Y1 14.318MHZ
XTAL_IN — C330 33P/50V_4/NPO
XTAL_OUT — C328 33P/50V_4/NPO

SLG: SLG8SP590VTR Seligo QPN: AL8SP590000
SLG: SLG8SP585VTR Seligo QPN: AL8SP585000
RSC: RTM875N-632-VB-GRT Realtek QPN: AL000875002

Quanta Computer Inc.
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	Clock Gen(9LRS3197)/HOLES	1A
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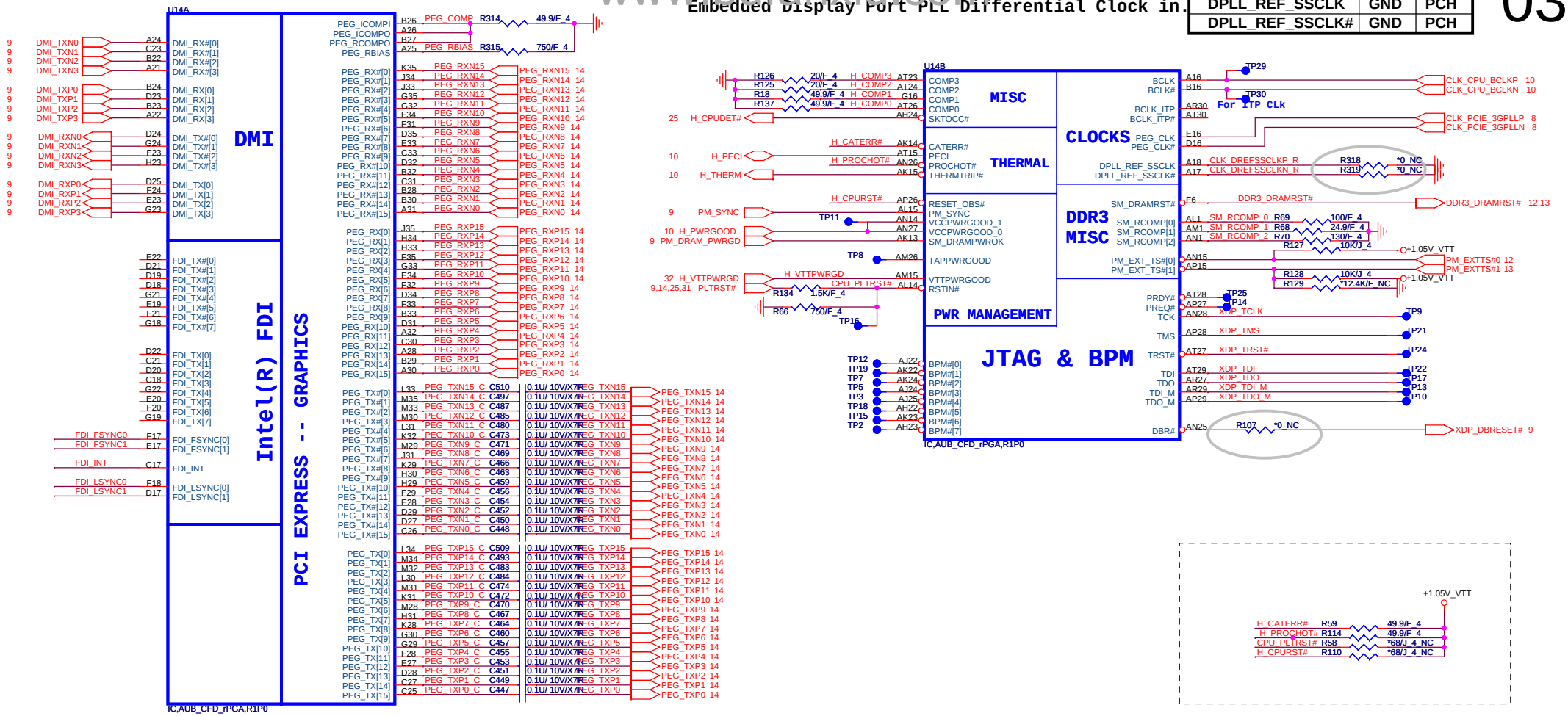
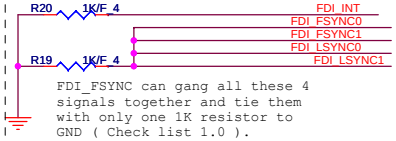
DPLL_REF_SSCLK/DPLL_REF_SSCLK#: Embedded Display Port PLL Differential Clock in.

	DIS	UMA
DPLL_REF_SSCLK	GND	PCH
DPLL_REF_SSCLK#	GND	PCH

03



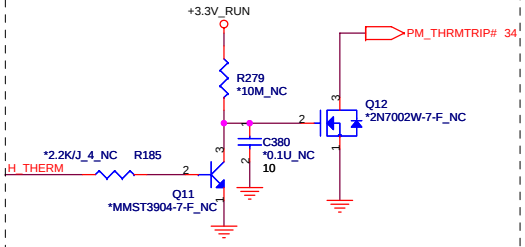
Discrete Only

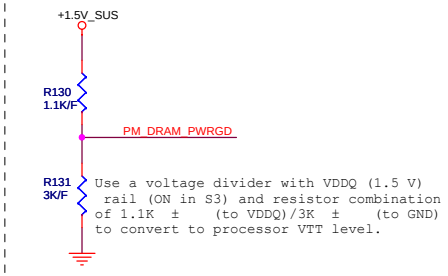


FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

DG(V1.0),P79: should be tied to GND (through 1K ±5% resistors), if these signals are left floating, there are nofunctional impacts but a small amount of power (~15 mW) maybe wasted.
DG(V1.1) P83: FDI_FSYNC[0], FDI_FSYNC[1],FDI_LSYN[0],FDI_LSYN[1] can be ganged together with one resistor.

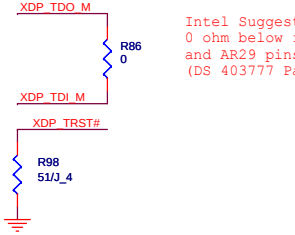
CPU THERMTRIP





Use a voltage divider with VDDQ (1.5 V) rail (ON in S3) and resistor combination of 1.1K ± (to VDDQ)/3K ± (to GND) to convert to processor VTT level.

JTAG MAPPING



Intel Suggest to reserve 0 ohm below for CPU AP29 and AR29 pins. (DS 403777 Page 81)

Quanta Computer Inc.
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Size	Document Number	Rev
	PROCESSER 1/4(HOST&PEX)	1A
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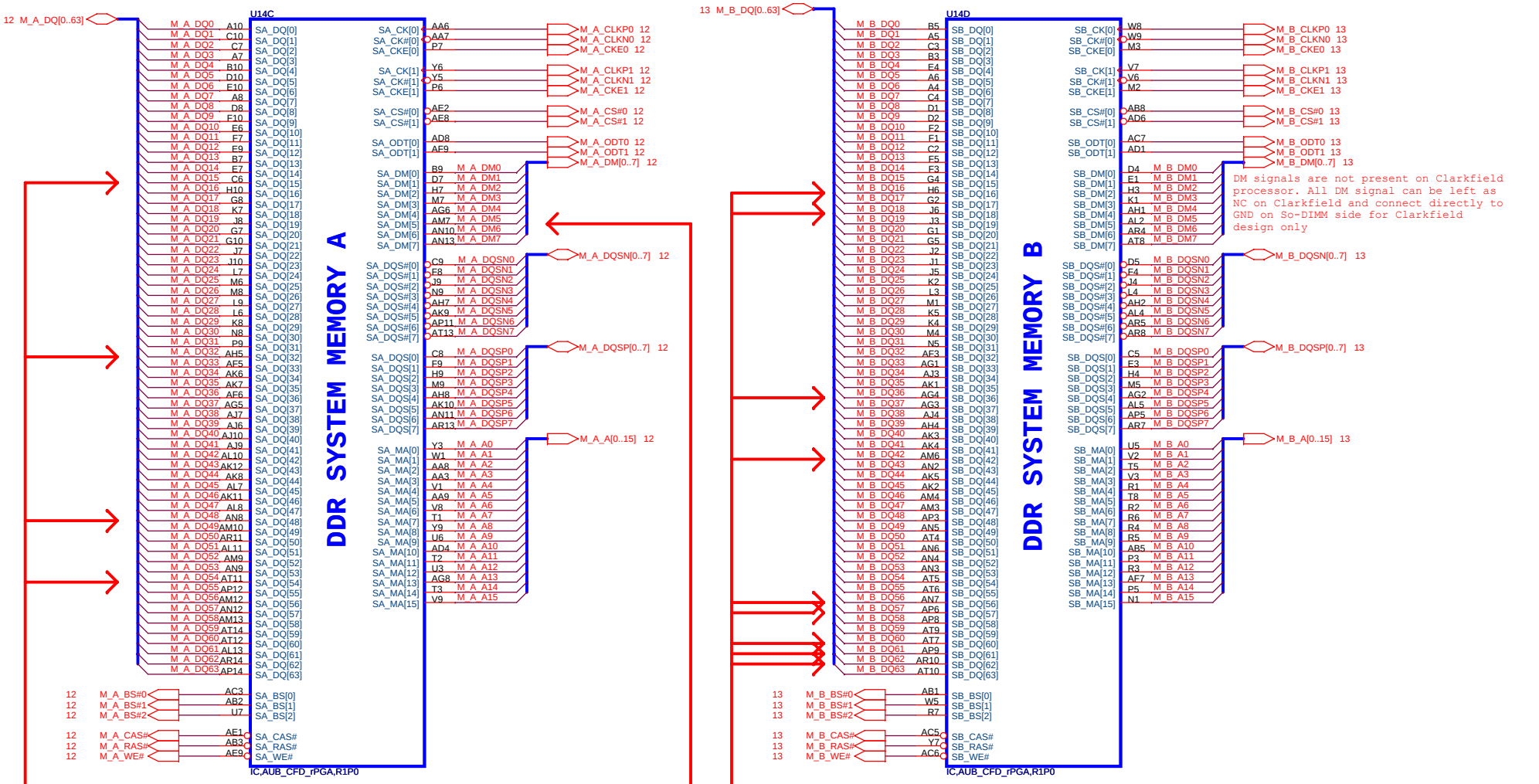
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number	Rev
	PROCESSER 2/4(DDR)	1A
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Name different with power

+VCC_CORE

C491 *22U/6.3V_8/X5R_NC
C490 *22U/6.3V_8/X5R_NC
C92 *22U/6.3V_8/X5R_NC
C70 *22U/6.3V_8/X5R_NC
C521 *22U/6.3V_8/X5R_NC
C125 22U/6.3V_8/X5R
C103 22U/6.3V_8/X5R
C121 22U/6.3V_8/X5R
C126 22U/6.3V_8/X5R
C77 22U/6.3V_8/X5R
C124 22U/6.3V_8/X5R
C129 22U/6.3V_8/X5R
C78 10U/6.3V_8/X5R
C488 10U/6.3V_8/X5R
C505 10U/6.3V_8/X5R
C445 10U/6.3V_8/X5R
C520 10U/6.3V_8/X5R
C60 10U/6.3V_8/X5R
C516 10U/6.3V_8/X5R
C122 10U/6.3V_8/X5R
C515 *10U/6.3V_8/X5R_NC
C489 *10U/6.3V_8/X5R_NC
C120 10U/6.3V_8/X5R
C117 10U/6.3V_8/X5R
C522 *10U/6.3V_8/X5R_NC
C518 *10U/6.3V_8/X5R_NC
C108 *10U/6.3V_8/X5R_NC
C123 *10U/6.3V_8/X5R_NC

C446 *470U_NC/
C18 *470U_NC

U14F

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

IC,AUB_CFD_rPGA,R1P0

CPU CORE SUPPLY

POWER

1.1V RAIL POWER

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32

AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

C519 10U/6.3V_8/X5R
C503 10U/6.3V_8/X5R
C478 10U/6.3V_8/X5R
C73 10U/6.3V_8/X5R
C46 *10U/6.3V_0805/X5R_NC
C481 *10U/6.3V_0805/X5R_NC
C47 *10U/6.3V_0805/X5R_NC
C119 *10U/6.3V_0805/X5R_NC
C114 *10U/6.3V_0805/X5R_NC
C524 22U/6.3V_8/X5R
C48 22U/6.3V_8/X5R
C514 *22U/6.3V_8/X5R_NC

+1.05V_VTT

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44

AF10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

C43 22U/6.3V_8/X5R
C84 22U/6.3V_8/X5R

+1.05V_VTT

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

CPU VIDS

PSI# AN33 H_PSI# 39

VID[0] AK35 VID0 39
VID[1] AK33 VID1 39
VID[2] AK34 VID2 39
VID[3] AL35 VID3 39
VID[4] AL33 VID4 39
VID[5] AM33 VID5 39
VID[6] AM35 VID6 39
PROC_DPRSLPVR AM34 DPRSLPVR 39

VTT_SELECT G15 TP1

VTT_SELECT:
High level 1.05V for Auburndale
Low level 1.1V for Clarksfield

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
100- ±1% pull-down to GND near processor

SENSE LINES

ISENSE AN35 I_MON 39

VTT_SENSE B15 VTT_SENSE 37
VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT T34

VCC_SENSE AJ34 VCCSENSE 39
VSS_SENSE AJ35 VSSSENSE 39

+VCC_CORE
R64 100/F
R61 100/F/

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND
or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

PROC_DPRSLPVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options
in the design for the Turbo functionality.
The stuffing and no-stuffing of the resistors
will depend on the POC configuration of AUB
and CFD
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

0525 Steg : As an option, VTT_SENSE pin on the processor can be left floating. But the platform needs to have the FB (feedback) pin of the VR tied to the VTT plane regulation.

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

U14G

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36

AT21 AT19 AT18 AT16 AR21 AR19 AR18 AR16 AP21 AP19 AP18 AP16 AN21 AN19 AN18 AN16 AM21 AM19 AM18 AM16 AL21 AL19 AL18 AL16 AK21 AK19 AK18 AK16 AJ21 AJ19 AJ18 AJ16 AH21 AH19 AH18 AH16

GRAPHICS

SENSE LINES

VAXG_SENSE AR22
VSSAXG_SENSE AT22

GRAPHICS VIDs

GFX_VID[0] AM22
GFX_VID[1] AP22
GFX_VID[2] AN22
GFX_VID[3] AP23
GFX_VID[4] AM23
GFX_VID[5] AP24
GFX_VID[6] AN24

GFX_VR_EN AR25
GFX_DPRSLPVR AT25
GFX_IMON AM24

Pop it when Arrandale Graphics disable.

R118 1K/J_4

POWER

DDR3 - 1.5V RAILS

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18

AJ1 AF1 AE7 AE4 AC1 AB7 AB4 Y1 W7 W4 U1 T7 T4 P1 N7 N4 L1 H1

+1.5V_SUS

C44 1U/6.3V/X5R
C90 1U/6.3V/X5R
C116 1U/6.3V/X5R
C53 1U/6.3V/X5R
C38 1U/6.3V/X5R
C55 22U/6.3V_8/X5R
C61 *22U/6.3V_8/X5R_NC
C20 330U/2V_7343

2A

FDI

+1.05V_VTT

C49 22U/6.3V_8/X5R
C475 *22U/6.3V_8/X5R_NC

VTT1_45 VTT1_46 VTT1_47

J24 J23 H25

PEG & DMI

+1.05V_VTT

C56 22U/6.3V_8/X5R
C62 22U/6.3V_8/X5R
C98 *22U/6.3V_8/X5R_NC
C37 *22U/6.3V_8/X5R_NC

K26 J27 J26 J25 H27 G28 G27 G26 F26 E26 E25

VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58

1.1V

VTT0_59 VTT0_60 VTT0_61 VTT0_62 VTT1_63 VTT1_64 VTT1_65 VTT1_66 VTT1_67 VTT1_68

P10 N10 L10 K10 J22 J20 J18 H21 H20 H19

+1.05V_VTT

C486 10U/6.3V_8/X5R
C495 *10U/6.3V_0805/X5R_NC
C476 22U/6.3V_8/X5R
C477 *22U/6.3V_8/X5R_NC

1.8V

VCCPLL1 VCCPLL2 VCCPLL3

L26 L27 M26

+1.8V_RUN

C45 22U/6.3V_8/X5R
C34 4.7U/6.3V/X5R
C42 2.2U/ 6.3V/X5R
C36 1U/6.3V/X5R
C479 1U/6.3V/X5R

IC,AUB_CFD_rPGA,R1P0

VID0 R96 1K/J_4 R313 *1K/J_4_NC
VID1 R84 1K/J_4 R312 *1K/J_4_NC
VID2 R104 1K/J_4 R311 *1K/J_4_NC
VID3 R111 1K/J_4 R310 *1K/J_4_NC
VID4 R115 1K/J_4 R309 *1K/J_4_NC
VID5 R148 1K/J_4 R308 *1K/J_4_NC
VID6 R124 1K/J_4 R307 *1K/J_4_NC
DPRSLPVR R139 1K/J_4 R306 *1K/J_4_NC
H_PSI# R140 1K/J_4 R305 *1K/J_4_NC

+1.05V_VTT

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	PROCESSER 3/4(POWER)	1A

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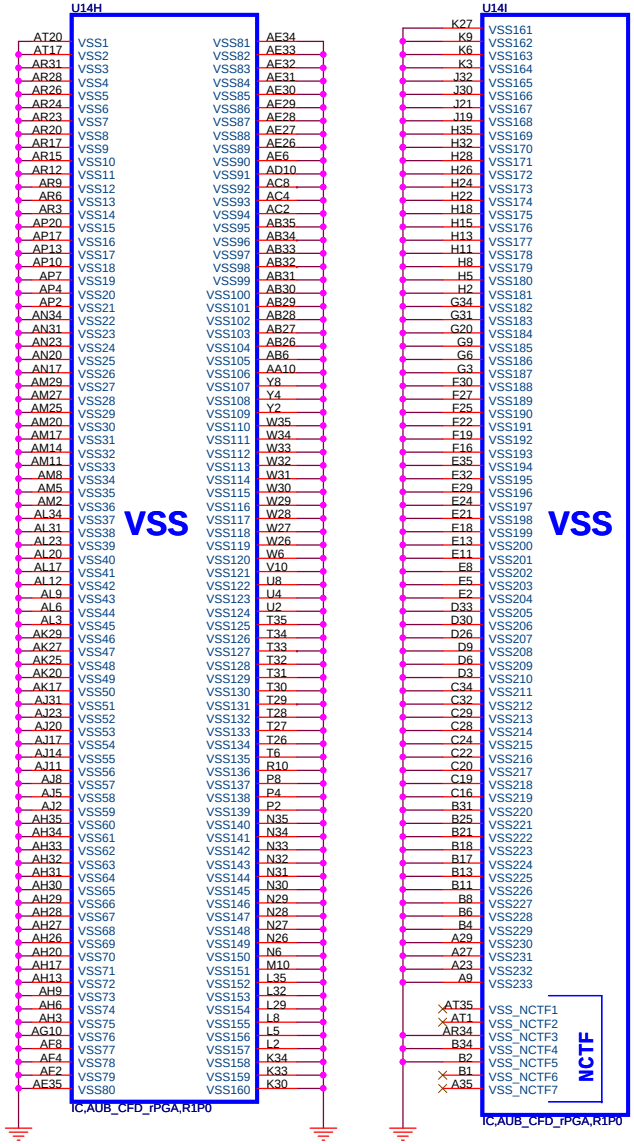
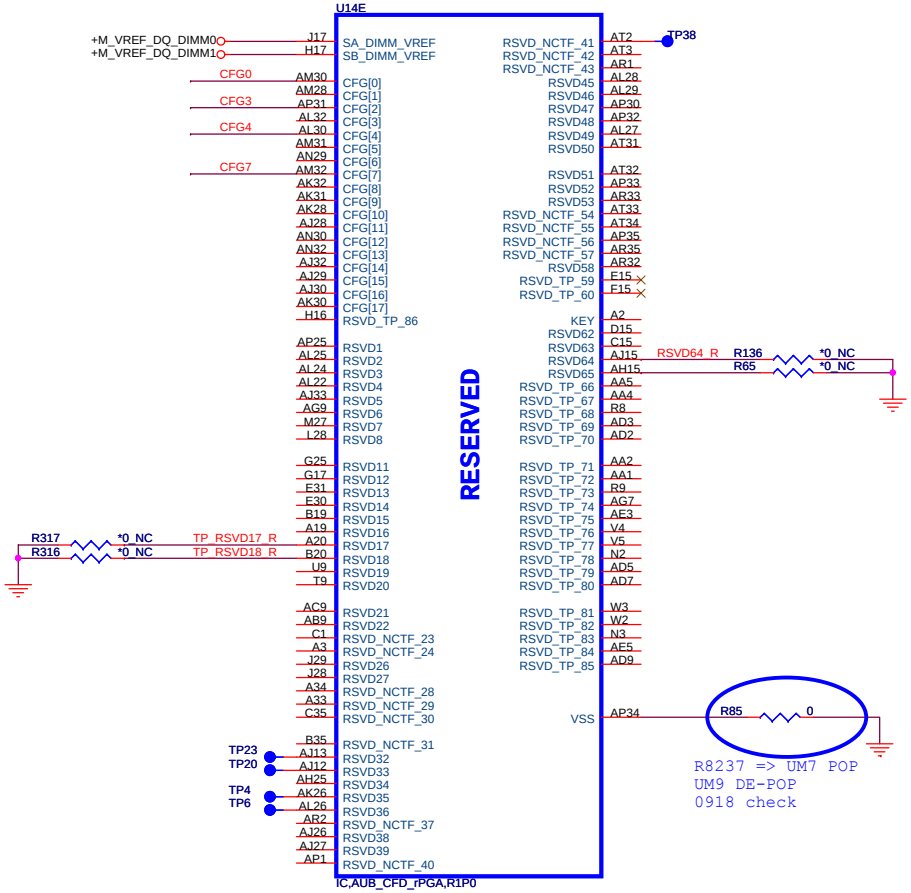
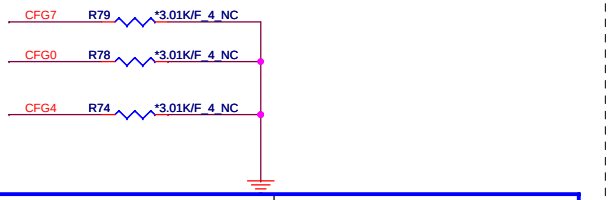
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)





	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	PROCESSER 4/4 (GND)	1A

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INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U21A

Ibex-M 1 OF 10

RTCX1 B13 — RTC_X1 — C422 18P/50V_4/COG — Y3 32.768KHZ — R268 10M/J_4 — C421 18P/50V_4/COG — RTC_X2 D13

RTC

T46 PAD — RTC_RST# — RTCRST# C14
T45 PAD — SRTC_RST# — SRTCRST# D17
SM_INTRUDER# — INTRUDER# A16
+RTC_CELL — R440 330K/J_6 — PCH_INVRMEN — INTVRMEN A14
T47 PAD

IHDA

ACZ_BITCLK — HDA_BCLK A30
ACZ_SYNC — HDA_SYNC D29
31 ACZ_SPKR — SPKR P1
ACZ_RST# — HDA_RST# C30
31 ACZ_SDIN0 — HDA_SDIN0 G30
HDA_SDIN1 F30
HDA_SDIN2 E32
HDA_SDIN3 E32
HDA_SDO B29
25 — R452 *0_NC — PCH_GPIO33 — HDA_DOCK_EN# / GPIO33 H32
25 PCH_MELOCK — HDA_DOCK_RST# / GPIO13 (+3V_S5) J30

JTAG

TP43 PCH_JTAG_TCK_BUF — JTAG_TCK M3
TP44 PCH_JTAG_TMS — JTAG_TMS K3
TP45 PCH_JTAG_TDI — JTAG_TDI K1
TP46 PCH_JTAG_TDO — JTAG_TDO J2
TP47 PCH_JTAG_RST# — TRST# J4
must add test point.

SPI

26 SPI_CLK — TP39 — SPI_CLK BA2
26 SPI_CS0# — TP40 — SPI_CS0# AV3
TP41 — SPI_CS1# AY3
26 SPI_SI — TP28 — SPI_MOSI AY1
26 SPI_SO — TP42 — SPI_MISO AV1
36 — C802 *100P/NPO_NC

ibexPeak-M_Rev1_0

LPC

FWH0 / LAD0 D33 — LAD0 25,31
FWH1 / LAD1 B33 — LAD1 25,31
FWH2 / LAD2 C32 — LAD2 25,31
FWH3 / LAD3 A32 — LAD3 25,31
FWH4 / LFRAME# C34 — LFRAME# 25,31
LDRQ0# A34
(+3V) LDRQ1# / GPIO23 E34
SERIRQ AB9 — SERIRQ 25

SATA

HDD

SATA0RXN AK7 — SATA_RXN0 28
SATA0RXP AK6 — SATA_RXP0 28
SATA0TXN AK11 — SATA_TXN0 28
SATA0TXP AK9 — SATA_TXP0 28

SATA1RXN AH6 — SATA_RXN1 28
SATA1RXP AH5 — SATA_RXP1 28
SATA1TXN AH9 — SATA_TXN1 28
SATA1TXP AH8 — SATA_TXP1 28

ODD

SATA2RXN AF11 — DG: Place TX cap close to connector
SATA2RXP AF9 — SATA port 2/3 are not support in HM55 .
SATA2TXN AF7 — They are only in PM 55
SATA2TXP AF6

SATA3RXN AH3
SATA3RXP AH1
SATA3TXN AF3
SATA3TXP AF1

ESATA

40

SATA4RXN AD9 — SATA_RXN4 27
SATA4RXP AD8 — SATA_RXP4 27
SATA4TXN AD6 — SATA_TXN4 27
SATA4TXP AD5 — SATA_TXP4 27

Distance between the PCH and cap on the "P" signal should be identical distace between the PCH and cap on the "N" signal for the same pair.

SATA5RXN AD3
SATA5RXP AD1
SATA5TXN AB3
SATA5TXP AB1

SATAICOMPO AF16
SATAICOMPI AF15 — SATA_COMP R218 37.4/F_4 — +1.05V_PCH
SATALED# T3 — SATA_LED# — SATA_LED# 29

(+3V) SATA0GP / GPIO21 Y9 — SATA_DET0#
(+3V_S5) SATA1GP / GPIO19 V1 — SATA_DET1#

Serial ATA LED: This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required.

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

+3.3V_RUN — R411 10K/J_4 — SATA_LED#
R237 10K/J_4 — SATA_DET0#
R405 10K/J_4 — SATA_DET1#

Flash Descriptor Security Override

GPIO33	Low = Enabled High = Disabled

R245 1 — 2 *1K_NC — PCH_GPIO33
(Internal 20K/F pull high to +3.3V_RUN)

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

iTPM ENABLE/DISABLE

+3.3V_RUN — R208 *1K_NC/ — SPI_SI

TPM Function	
Enable	Mount
Disable	NC (Default)

UMA CRT, LVDS&HDMI signals

IBEX PEAK-M (LVDS,DDI)

U21D

Ibex-M 4 OF 10

LVDS--A

T48 L_BKLTEN
T47 L_VDD_EN
Y48 L_BKLTCTL
AB48 L_DDC_CLK
Y45 L_DDC_DATA
AB46 L_CTRL_CLK
V48 L_CTRL_DATA
T29 PAD — AP39 LVD_IBG
T28 PAD — AP41 LVD_VBG
T26 PAD — AT43 LVD_VREFH
T27 PAD — AT42 LVD_VREFL
AV53 LVDSA_CLK#
AV51 LVDSA_CLK
BB47 LVDSA_DATA#0
BA52 LVDSA_DATA#1
AY48 LVDSA_DATA#2
AV47 LVDSA_DATA#3
BB48 LVDSA_DATA0
BA50 LVDSA_DATA1
AY49 LVDSA_DATA2
AV48 LVDSA_DATA3

LVDS--B

AP48 LVDSB_CLK#
AP47 LVDSB_CLK
AY53 LVDSB_DATA#0
AT49 LVDSB_DATA#1
AU52 LVDSB_DATA#2
AT53 LVDSB_DATA#3
AY51 LVDSB_DATA0
AT48 LVDSB_DATA1
AU50 LVDSB_DATA2
AT51 LVDSB_DATA3

CRT

AA52 CRT_BLUE
AB53 CRT_GREEN
AD53 CRT_RED
V51 CRT_DDC_CLK
V53 CRT_DDC_DATA
Y53 CRT_HSYNC
Y51 CRT_VSYNC
R221 1K/F_4 — DAC_IREF — AD48 DAC_IREF
AB51 CRT_IRTN

SDVO

SDVO_TVCLKINN BJ46
SDVO_TVCLKINP BG46
SDVO_STALLN BJ48
SDVO_STALLP BG48
SDVO_INTN BF45
SDVO_INTP BH45
SDVO_CTRLCLK T51
SDVO_CTRLDATA T53

DISPLAY PORT B

DDPB_AUXN BG44
DDPB_AUXP BJ44
DDPB_HPD AU38
DDPB_0N BD42
DDPB_0P BC42
DDPB_1N BJ42
DDPB_1P BG42
DDPB_2N BB40
DDPB_2P BA40
DDPB_3N AW38
DDPB_3P BA38

DISPLAY PORT C

DDPC_CTRLCLK Y49
DDPC_CTRLDATA AB49
DDPC_AUXN BE44
DDPC_AUXP BD44
DDPC_HPD AV40
DDPC_0N BE40
DDPC_0P BD40
DDPC_1N BE41
DDPC_1P BH41
DDPC_2N BD38
DDPC_2P BC38
DDPC_3N BB36
DDPC_3P BA36

DISPLAY PORT D

DDPD_CTRLCLK U50
DDPD_CTRLDATA U52
DDPD_AUXN BC46
DDPD_AUXP BD46
DDPD_HPD AT38
DDPD_0N BJ40
DDPD_0P BG40
DDPD_1N BJ38
DDPD_1P BG38
DDPD_2N BF37
DDPD_2P BH37
DDPD_3N BE36
DDPD_3P BD36

Digital Display Interface

ibexPeak-M_Rev1_0

UMA 0.5%
DIS 1%

+3.3V_SUS **Res. of TDI near PCH**

R416 *200_NC — R418 *200_NC — R420 *200_NC — R422 20K/F_4_NC
R417 *100_NC — R419 *100_NC — R421 *100_NC — R423 *10K_NC

PCH_JTAG_TMS
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_RST#

NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

R415 51/J_4 — PCH_JTAG_TCK_BUF

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

For AUDIO

25,31 ACZ_RST#_AUDIO — R229 33/J_4 — ACZ_RST#
31 ACZ_SDOUT_AUDIO — R235 33/J_4 — ACZ_SDOUT
C404 *10P/50V_4_NC/OOG
31 ACZ_SYNC_AUDIO — R234 33/J_4 — ACZ_SYNC
C399 *10P/50V_4_NC/OOG
31 ACZ_BITCLK_AUDIO — R231 33/J_4 — ACZ_BITCLK
77 — C389 10P/50V_4/COG

+3.3V_RUN — R412 *1K/F_4_NC — ACZ_SPKR

No Reboot strap.	
SPKR	Low = Default. High = No Reboot.

RTC

1mA

+RTC_CELL
R443 20K/F_4 — C582 1U/6.3V/X5R — RTC_RST#
R428 20K/F_4 — C583 1U/6.3V/X5R — SRTC_RST#
R427 1M/J_4 — SM_INTRUDER#

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	PCH 1/5 (SATA,HDA,LPC)	1A

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IBEX PEAK-M (GND)

U21I

AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L2
B7	VSS[169]	VSS[269]	L22
BG12	VSS[170]	VSS[270]	L32
BB12	VSS[171]	VSS[271]	L36
BB16	VSS[172]	VSS[272]	L40
BB20	VSS[173]	VSS[273]	L52
BB24	VSS[174]	VSS[274]	M12
BB30	VSS[175]	VSS[275]	M16
BB34	VSS[176]	VSS[276]	M20
BB38	VSS[177]	VSS[277]	N38
BB42	VSS[178]	VSS[278]	M34
BB49	VSS[179]	VSS[279]	M38
BB5	VSS[180]	VSS[280]	M42
BC10	VSS[181]	VSS[281]	M46
BC14	VSS[182]	VSS[282]	M49
BC18	VSS[183]	VSS[283]	M5
BC2	VSS[184]	VSS[284]	M8
BC22	VSS[185]	VSS[285]	N24
BC32	VSS[186]	VSS[286]	P11
BC36	VSS[187]	VSS[287]	AD15
BC40	VSS[188]	VSS[288]	P22
BC44	VSS[189]	VSS[289]	P30
BC52	VSS[190]	VSS[290]	P32
BH9	VSS[191]	VSS[291]	P34
BD48	VSS[192]	VSS[292]	P42
BD49	VSS[193]	VSS[293]	P45
BD5	VSS[194]	VSS[294]	P47
BE12	VSS[195]	VSS[295]	R2
BE16	VSS[196]	VSS[296]	R52
BE20	VSS[197]	VSS[297]	T12
BE24	VSS[198]	VSS[298]	T41
BE30	VSS[199]	VSS[299]	T46
BE34	VSS[200]	VSS[300]	T49
BE38	VSS[201]	VSS[301]	T5
BE42	VSS[202]	VSS[302]	T8
BE46	VSS[203]	VSS[303]	U30
BE48	VSS[204]	VSS[304]	U31
BE50	VSS[205]	VSS[305]	U32
BE6	VSS[206]	VSS[306]	U34
BE8	VSS[207]	VSS[307]	P38
BF3	VSS[208]	VSS[308]	V11
BF49	VSS[209]	VSS[309]	P16
BF51	VSS[210]	VSS[310]	V19
BG18	VSS[211]	VSS[311]	V20
BG24	VSS[212]	VSS[312]	V22
BG4	VSS[213]	VSS[313]	V30
BG50	VSS[214]	VSS[314]	V31
BH11	VSS[215]	VSS[315]	V32
BH15	VSS[216]	VSS[316]	V34
BH19	VSS[217]	VSS[317]	V35
BH23	VSS[218]	VSS[318]	V38
BH31	VSS[219]	VSS[319]	V43
BH35	VSS[220]	VSS[320]	V45
BH39	VSS[221]	VSS[321]	V46
BH43	VSS[222]	VSS[322]	V47
BH47	VSS[223]	VSS[323]	V49
BH7	VSS[224]	VSS[324]	V5
C12	VSS[225]	VSS[325]	V7
C50	VSS[226]	VSS[326]	V8
D51	VSS[227]	VSS[327]	W2
E12	VSS[228]	VSS[328]	W52
E16	VSS[229]	VSS[329]	Y11
E20	VSS[230]	VSS[330]	Y12
E24	VSS[231]	VSS[331]	Y15
E30	VSS[232]	VSS[332]	Y19
E34	VSS[233]	VSS[333]	Y23
E38	VSS[234]	VSS[334]	Y28
E42	VSS[235]	VSS[335]	Y30
E46	VSS[236]	VSS[336]	Y31
E48	VSS[237]	VSS[337]	Y32
E6	VSS[238]	VSS[338]	Y38
E8	VSS[239]	VSS[339]	Y43
F49	VSS[240]	VSS[340]	Y46
F5	VSS[241]	VSS[341]	P49
G10	VSS[242]	VSS[342]	Y5
G14	VSS[243]	VSS[343]	Y6
G18	VSS[244]	VSS[344]	Y8
G2	VSS[245]	VSS[345]	P24
G22	VSS[246]	VSS[346]	T43
G32	VSS[247]	VSS[347]	AD51
G36	VSS[248]	VSS[348]	AT8
G40	VSS[249]	VSS[349]	AD47
G44	VSS[250]	VSS[350]	Y47
G52	VSS[251]	VSS[351]	AT12
AF39	VSS[252]	VSS[352]	AM6
H16	VSS[253]	VSS[353]	AT13
H20	VSS[254]	VSS[354]	AM5
H30	VSS[255]	VSS[355]	AK45
H34	VSS[256]	VSS[356]	AK39
H38	VSS[257]	VSS[366]	AV14
H42	VSS[258]		

IbexPeak-M_Rev1_0

PCIE Clock Request

+3.3V_RUN

PCIE_CLK_REQ1# R406 10K/J_4
PCIE_CLK_REQ2# R413 10K/J_4

+3.3V_SUS

PCIE_CLK_REQ0# R239 10K/J_4
PCIE_CLK_REQ3# R434 10K/J_4
PCIE_CLK_REQ4# R249 10K/J_4
PCIE_CLK_REQB#_R R265 10K/J_4
PCIE_CLK_REQ5# R253 10K/J_4

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S (DS 401376 Table2-26)

PEG_CLKREQ# R435 10K/J_4

LOW acvite on GPIO47 for GFX CLK output

Q15 FDN357N

SMB_CLK_ME1 1 3 SMBCLK1 25

+3.3V_SUS

SMB_DATA_ME1 1 3 SMBDAT1 25

Q14 FDN357N

IBEX PEAK-M (PCI-E,SMBUS,CLK)

U21B

Ibex-M 2 OF 10

PCI-E*

[WLAN]
31 PCIE_RXN1
31 PCIE_RXP1
31 PCIE_TXN1
31 PCIE_TXP1
C348 0.1U/ 10V/X7R PCIE_TXN1_C
C349 0.1U/ 10V/X7R PCIE_TXP1_C

[LAN]
31 PCIE_RXN6_LAN
31 PCIE_RXP6_LAN
31 PCIE_TXN6_LAN
31 PCIE_TXP6_LAN
C334 0.1U/ 10V/X7R PCIE_TXN6_LAN_C
C333 0.1U/ 10V/X7R PCIE_TXP6_LAN_C

MiniWLAN
31 CLK_PCIE_WLANN
31 CLK_PCIE_WLANP
31 PCIE_CLK_REQ1#

LAN
31 CLK_PCIE_LANN
31 CLK_PCIE_LANP
31 PCIE_CLK_REQB#_R

SMBus
(+3V_S5) SMBALERT# / GPIO11
SMBCLK
SMBDATA
(+3V_S5) SML0ALERT# / GPIO60
SML0CLK
SML0DATA
(+3V_S5) SML1ALERT# / GPIO74
(+3V_S5) SML1CLK / GPIO58
(+3V_S5) SML1DATA / GPIO75

B9 SMBALERT# 10K/J_4 R438
H14 ICH_SMBCLK 2.2K/J_4 R282
C8 ICH_SMBDATA 2.2K/J_4 R281
J14 SMBL0ALERT# 10K/J_4 R262
C6 SMB_CLK_ME0 2.2K/J_4 R433
G8 SMB_DATA_ME0 2.2K/J_4 R256
M14 SML1ALERT# 10K/J_4 R263
E10 SMB_CLK_ME1 2.2K/J_4 R272
G12 SMB_DATA_ME1 2.2K/J_4 R271

+3.3V_SUS

SMB1 Check R value... (R8283, R8296)

Controller Link
CL_CLK1 T13
CL_DATA1 T11
CL_RST1# T9
ICH_SMBCLK ICH_SMBCLK 31
ICH_SMBDATA ICH_SMBDATA 31

PEG
(+3V_S5) PEG_A_CLKRQ# / GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P

H1 PEG_CLKREQ# PEG_CLKREQ# 15
AD43 CLK_PCIE_VGAN 14
AD45 CLK_PCIE_VGAP 14
AN4 CLK_PCIE_3GPLLN 3
AN2 CLK_PCIE_3GPLLP 3

From CLK BUFFER

CLKOUT_DP_N / CLKOUT_BCLK1_N AT1
CLKOUT_DP_P / CLKOUT_BCLK1_P AT3

CLKIN_DMI_N AW24 CLK_BUF_PCIE_3GPLLN 2
CLKIN_DMI_P BA24 CLK_BUF_PCIE_3GPLLP 2

CLKIN_BCLK_N AP3 CLK_BUF_BCLKN 2
CLKIN_BCLK_P AP1 CLK_BUF_BCLKP 2

CLKIN_DOT_96N F18 CLK_BUF_DREFCLKN 2
CLKIN_DOT_96P E18 CLK_BUF_DREFCLKP 2

CLKIN_SATA_N / CKSSCD_N AH13 CLK_BUF_DREFSSCLKN 2
CLKIN_SATA_P / CKSSCD_P AH12 CLK_BUF_DREFSSCLKP 2

REFCLK14IN P41 CLK_PCH_14M 2
C384 *5.6P/50V_4_NC/COG
CLKIN_PCILOOPBACK J42 CLK_PCI_FB
CLK_PCI_FB 9
T33
Intel recommendation
XTAL25_IN AH51
XTAL25_OUT AH53
R227 *0_NC
T56 short0402
XCLK_RCOMP AF38
R219 90.9/F_4
+1.05V_PCH

Clock Flex
(+3V) CLKOUTFLEX0 / GPIO64 T45 CLK_FLEX0 T30
(+3V) CLKOUTFLEX1 / GPIO65 P43 CLK_FLEX1 T32
(+3V) CLKOUTFLEX2 / GPIO66 T42 CLK_FLEX2 T34
(+3V) CLKOUTFLEX3 / GPIO67 N50 CLK_FLEX3
R243 22/J_4
CLK_48M_CARD 23

R8236 => UM7 POP 33ohm
UM9 POP 22ohm
0918 check
C419 10P/50V/COG

PCIE_CLK_REQ0# P9 PCIECLKRQ0# / GPIO73 (+3V_S5)
PCIE_CLK_REQ2# N4 PCIECLKRQ2# / GPIO20 (+3V)
PCIE_CLK_REQ3# A8 PCIECLKRQ3# / GPIO25 (+3V_S5)
PCIE_CLK_REQ4# M9 PCIECLKRQ4# / GPIO26 (+3V_S5)
PCIE_CLK_REQ5# H6 PCIECLKRQ5# / GPIO44 (+3V_S5)
PCIE_CLK_REQB#_R P13 PEG_B_CLKRQ# / GPIO56 (+3V_S5)

CLKOUT_PCIE0N
CLKOUT_PCIE0P
CLKOUT_PCIE1N
CLKOUT_PCIE1P
U4 PCIECLKRQ1# / GPIO18 (+3V)
CLKOUT_PCIE2N
CLKOUT_PCIE2P
CLKOUT_PCIE3N
CLKOUT_PCIE3P
CLKOUT_PCIE4N
CLKOUT_PCIE4P
CLKOUT_PCIE5N
CLKOUT_PCIE5P
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P

IbexPeak-M_Rev1_0

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Quanta Computer Inc.	PROJECT : UM8B DIS		
Size	Document Number		Rev
	PCH 2/5 (PCIE, SMBUS, CK)		1A
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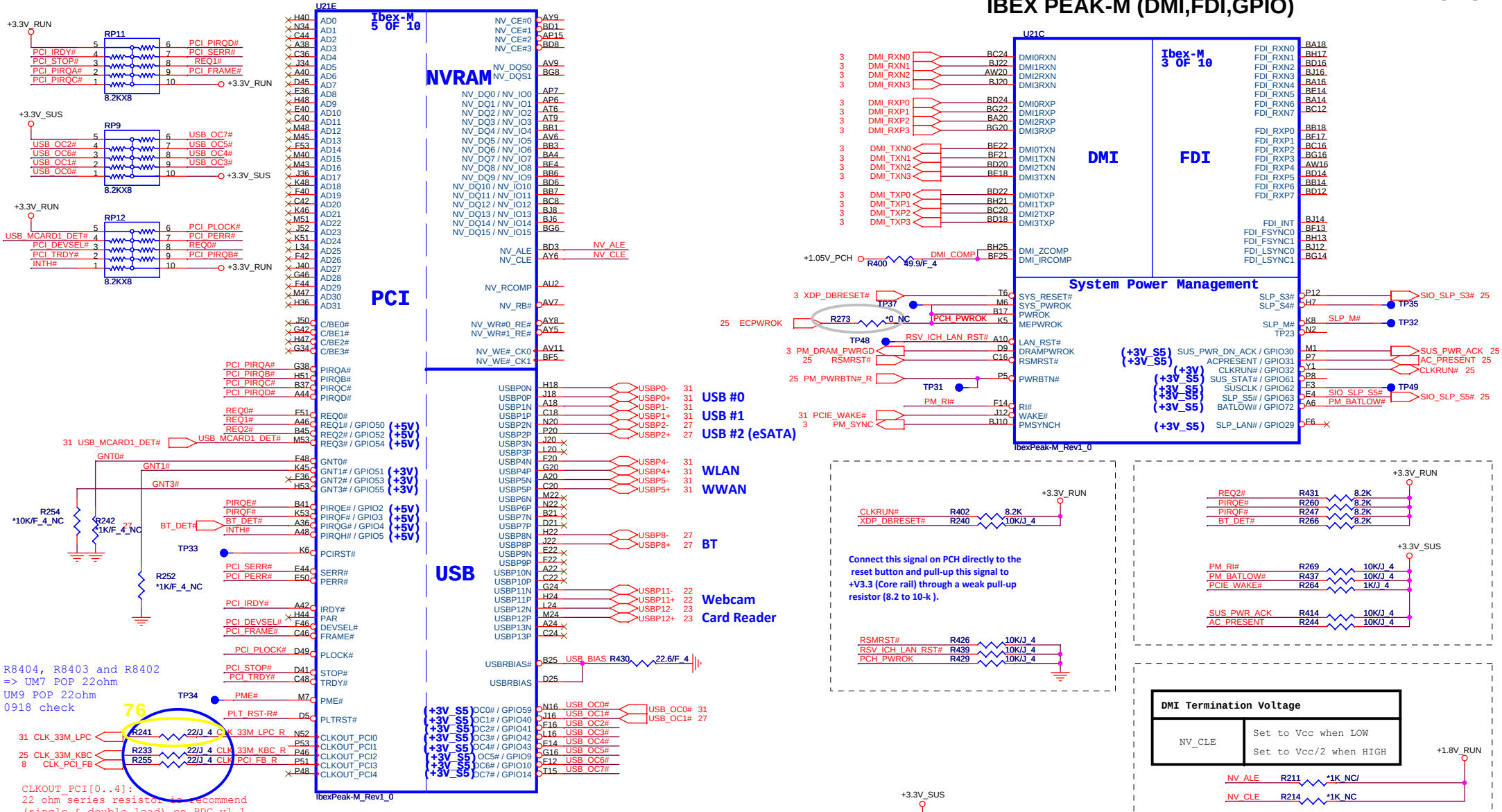
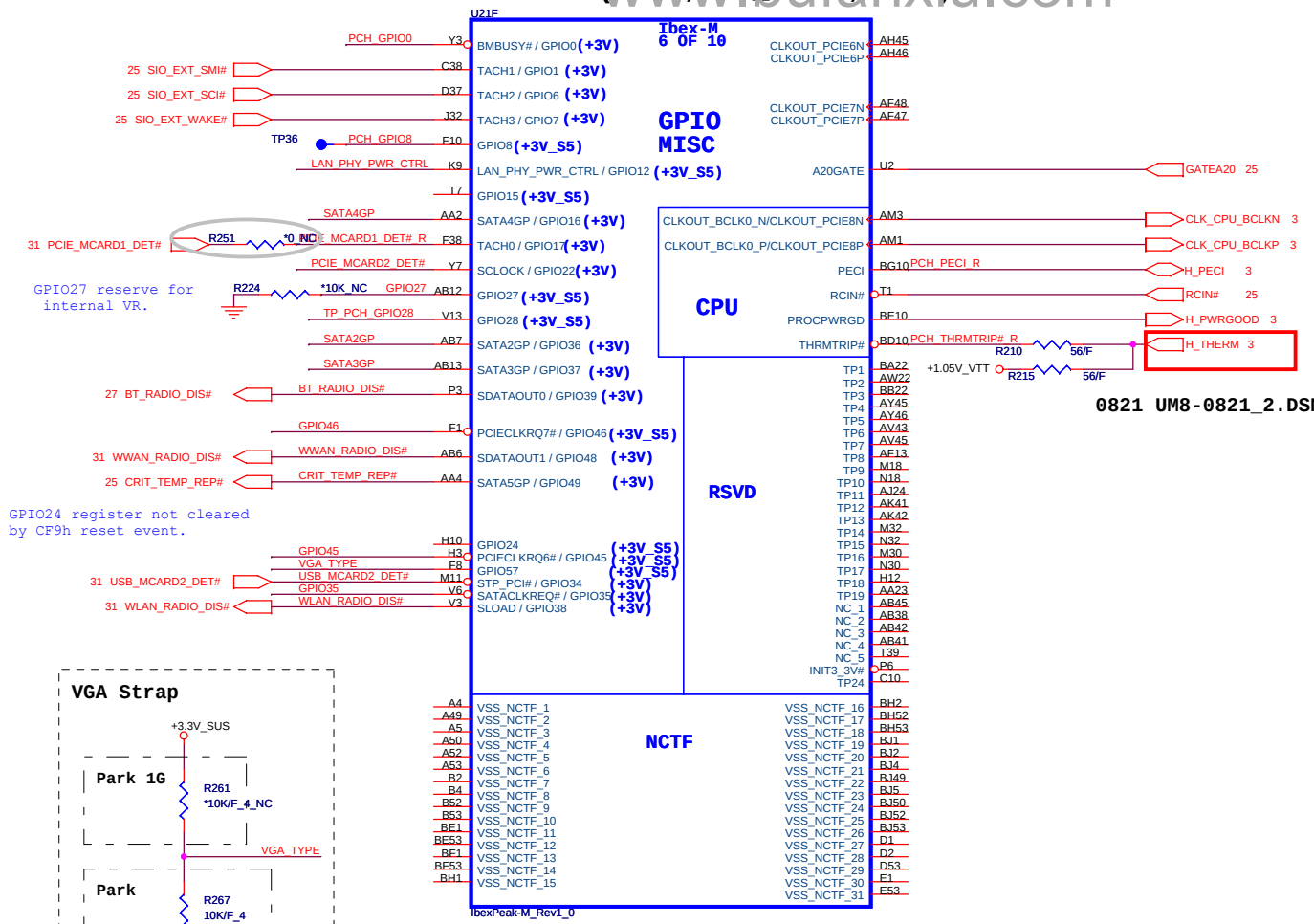
IBEX PEAK-M (PCI,USB,NVRAM)

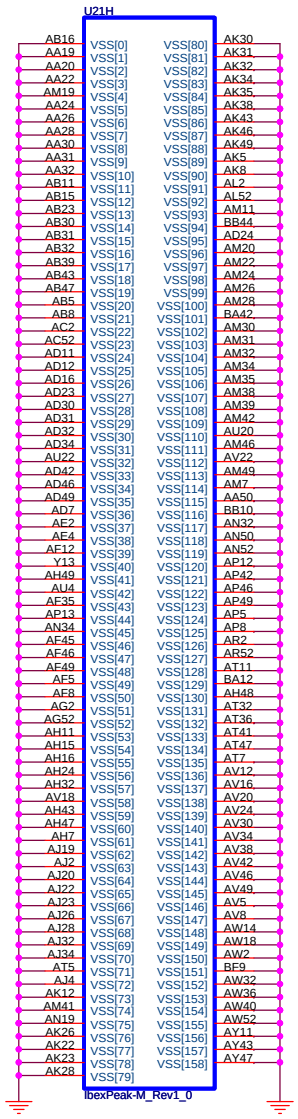
IBEX PEAK-M (DMI,FDI,GPIO)



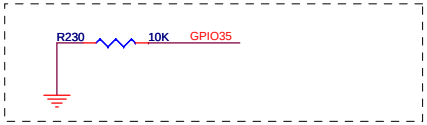
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

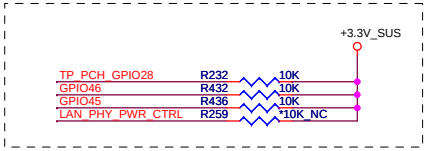


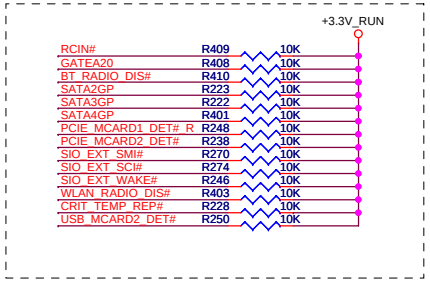
IBEX PEAK-M (GND)

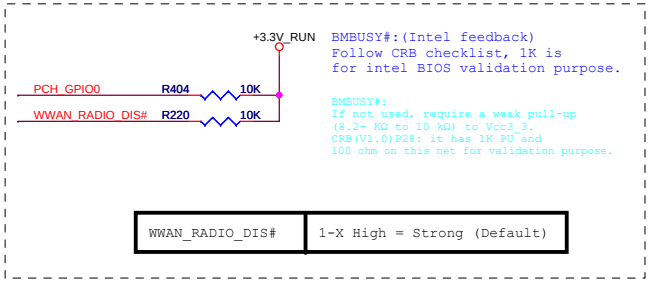


VGA Strap









WWAN_RADIO_DIS#	1-X High = Strong (Default)

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PROJECT : UM8B DIS

Size	Document Number	Rev
	PCH 4/5 (GPIO & Strap)	1A
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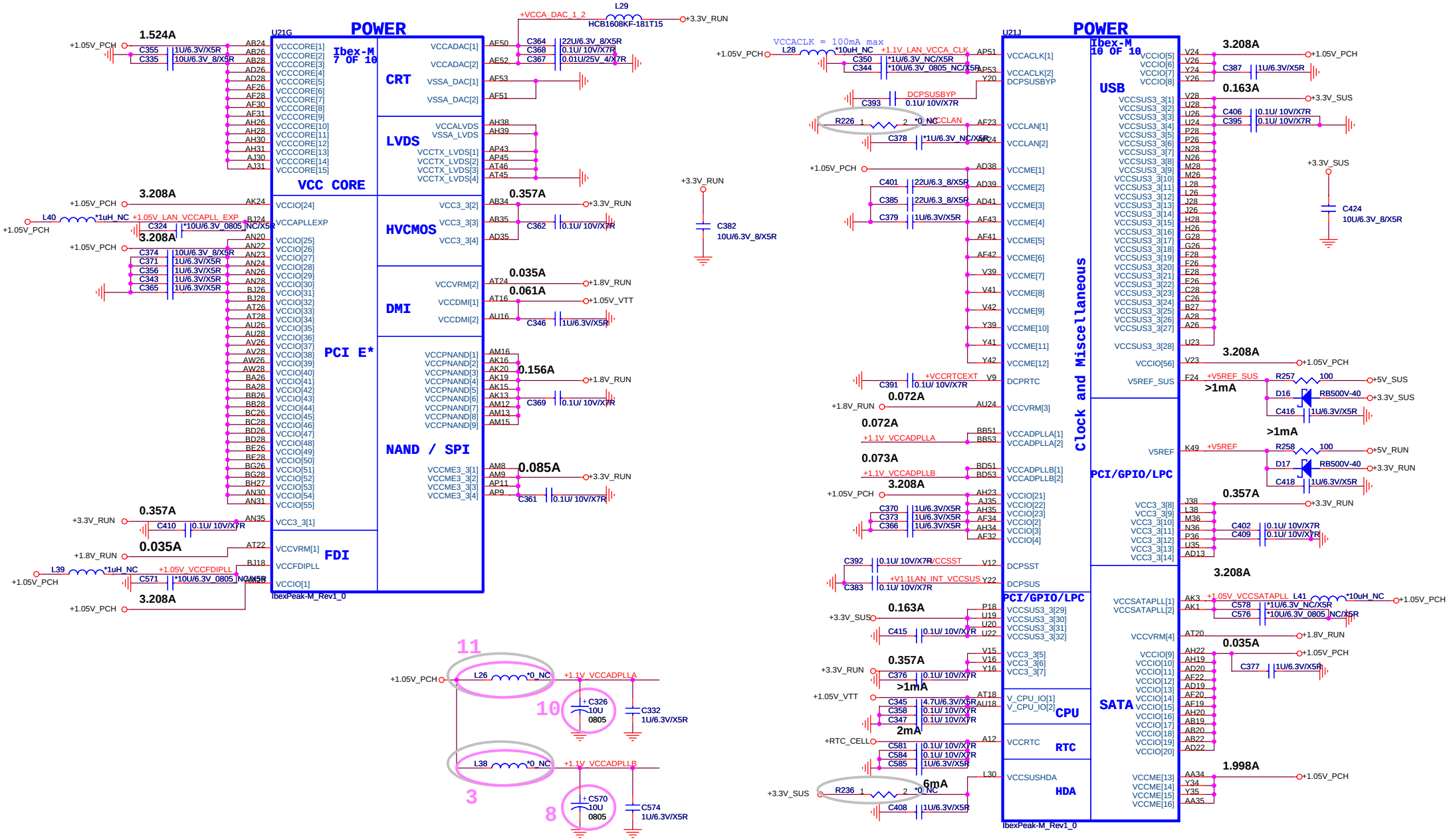
Cap quantities follow UM3



Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	PCH 5/5 (POWER)	1A

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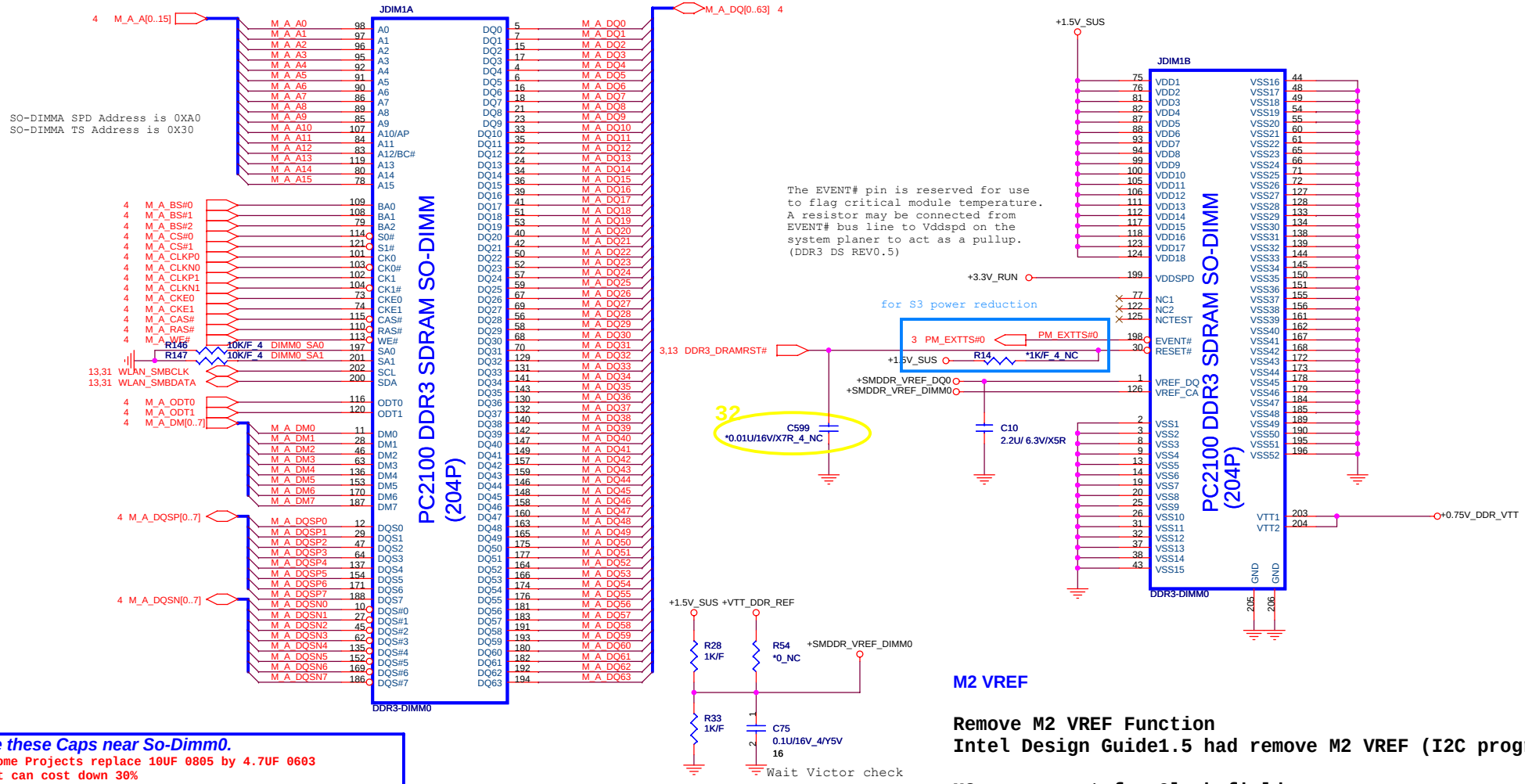


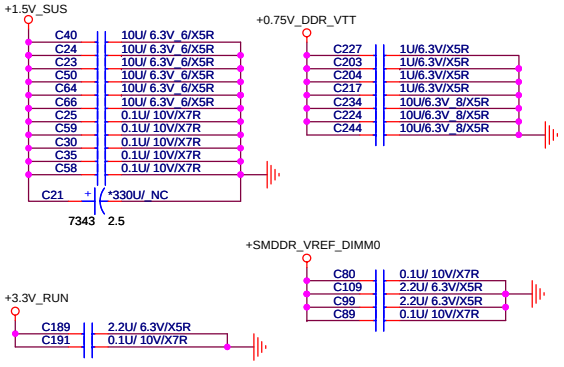
M2 VREF

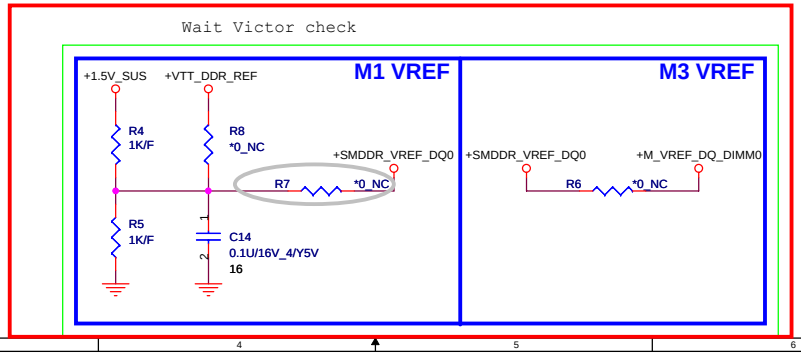
Remove M2 VREF Function
Intel Design Guide1.5 had remove M2 VREF (I2C programble VREF)

M3 => support for Clarksfield processor

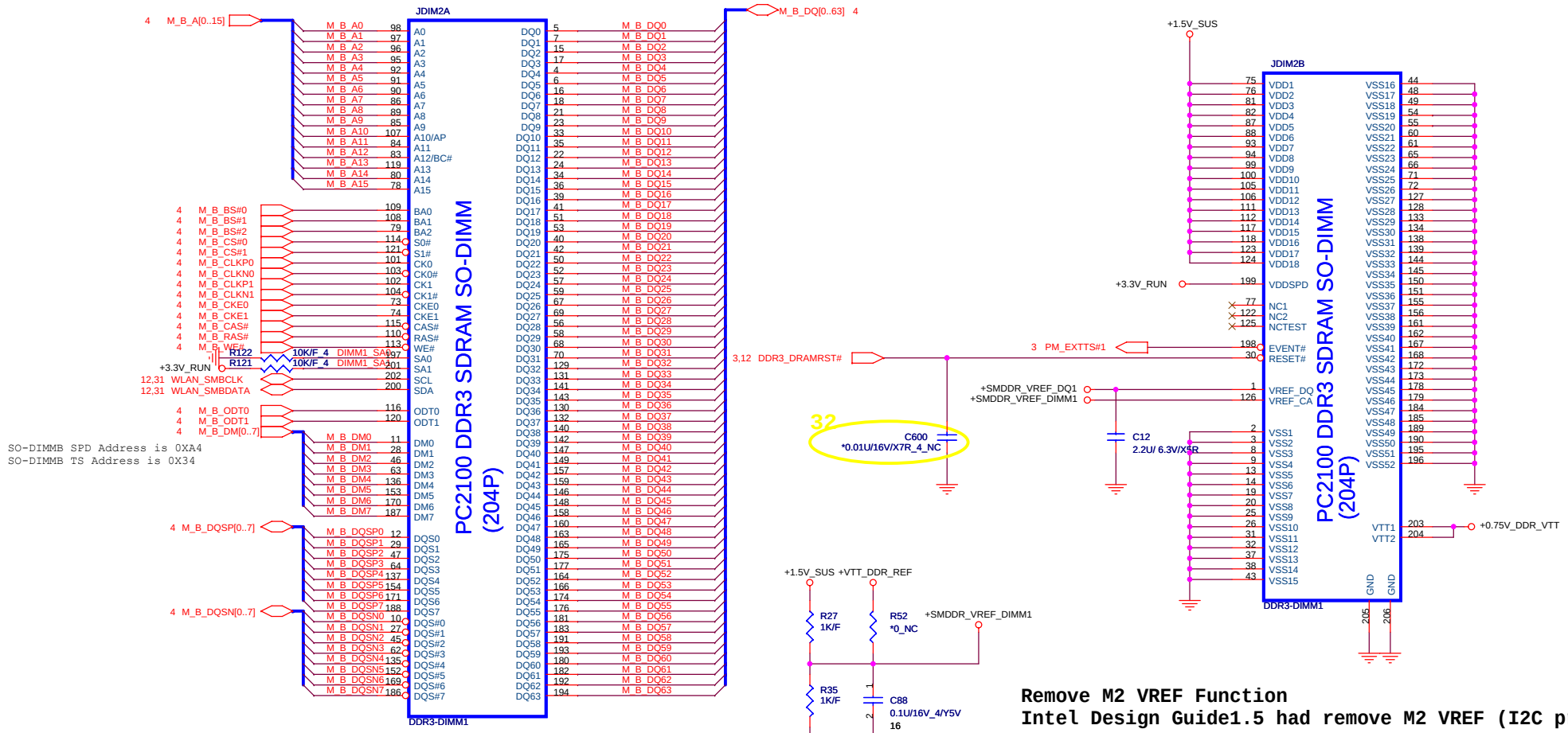
Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%

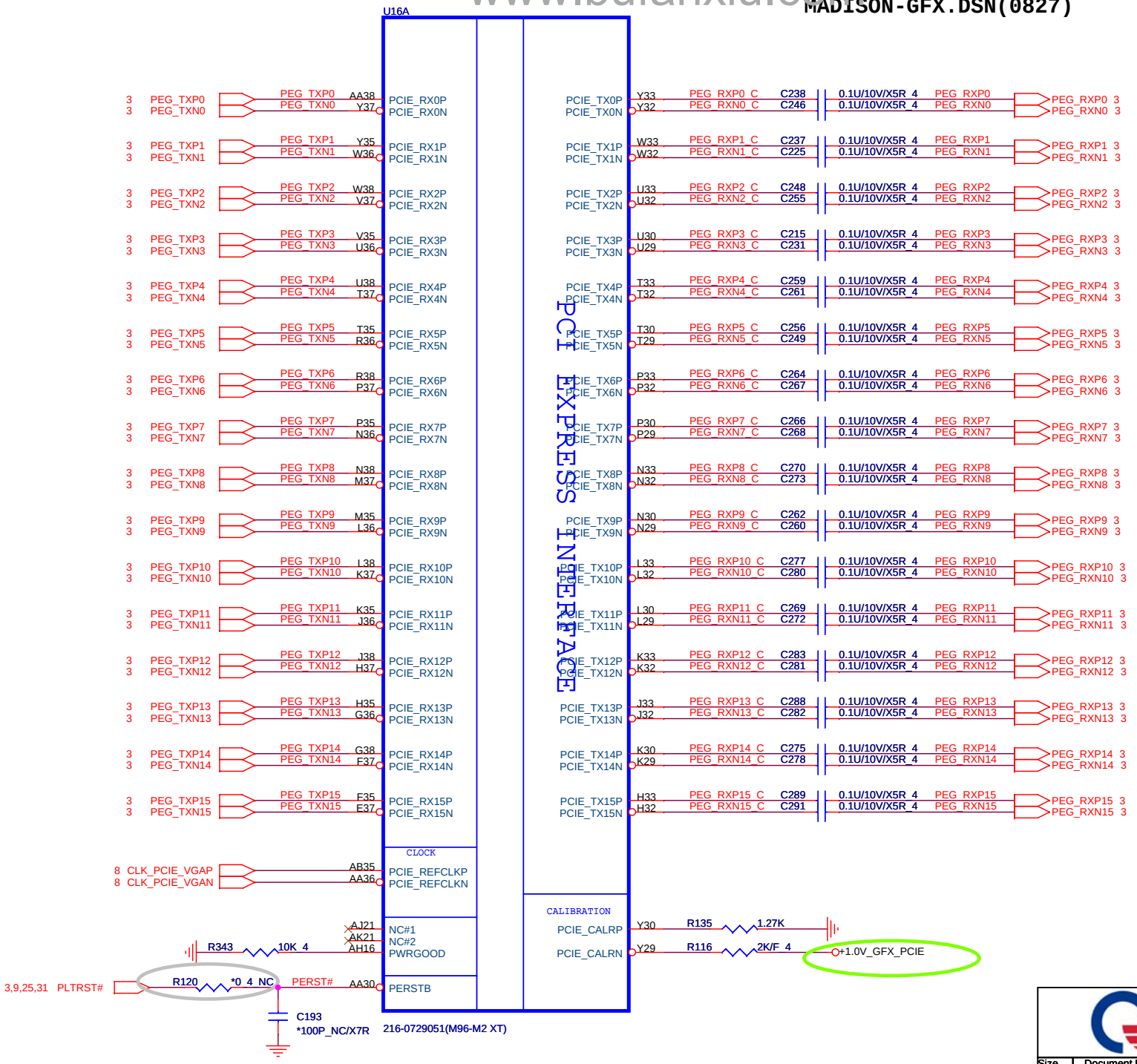




Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: DDR3 DIMM-0	Rev: 1A
Date: Friday, February 05, 2010	Sheet 12 of 46	



Quanta Computer Inc.	
PROJECT : UM8B DIS	
Size	Document Number: DDR3 DIMM-1 — Rev: 1A
Date: Friday, February 05, 2010	Sheet 13 of 46



Quanta Computer Inc.	
PROJECT : UM8B DIS	
Size	Document Number: Madison PCIE I/F — Rev: 1A
Date: Friday, February 05, 2010	Sheet 14 of 46

		R342 RAM_ TYPE_CFG3	R340 RAM_ TYPE_CFG2	R341 RAM_ TYPE_CFG1	R339 RAM_ TYPE_CFG0
Memory Straps					
800 MHz 1GB(64M*16) Hynix_Orion die	H5TQ1G63BFR-12C	0	0	0	0
800 MHz 1GB(64M*16) Samsung_E die	K4W1G1646E-HC12	0	0	0	1
800 MHz 1Gb(128M*16) Hynix_Orion die	H5TQ2G63BFR-12C	0	0	1	0
800 MHz 1Gb(128M*16) Samsung_E die	K4W2G1646b-HC12	0	0	1	1
		0	1	0	0
		0	1	0	1

Note : Required Frequency = 800 MHz

VRAM TYPE

APERTURE SIZE

MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

(GPIO_19_CTF)
Critical temperature fault (active high)
CTF will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the ASIC from damage by removing power.

!!! NC when PARK-M2

Park and Madison

GPU Power-on sequence

1 => +3V_D
2 => +1.5V_GPU = +1.5V_RUN
3 => +VGPU_CORE
4 => +VGPU_IO
5 => +1V = +1.0V_GFX_PCIE
6 => +1.8V_GPU = +1.8V_RUN_GFX
7 => dGPU_PWROK

CONFIGURATION STRAPS			
STRAPS	**PIN**	**DESCRIPTION**	**SET**
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	0
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	0
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	11
VIP_DEVICE_STRAP_EN	VGAVSYNC2	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0
BIOS_ROM_EN (Internal pull down)	GPIO_22_ROMCSB	1 = Enable external BIOS ROM device 0 = Disable external BIOS ROM device	0

Layout Note: Place 150 ohm termination resistors close to ATI CHIP.

For Park,Madison production version ASIC is need removed workaround.

Park
pre-production build could get the "ENG" marking.

Madison
- date codes up to 0941 are NOT Production Samples
- date codes from 0942 and up are Production Samples

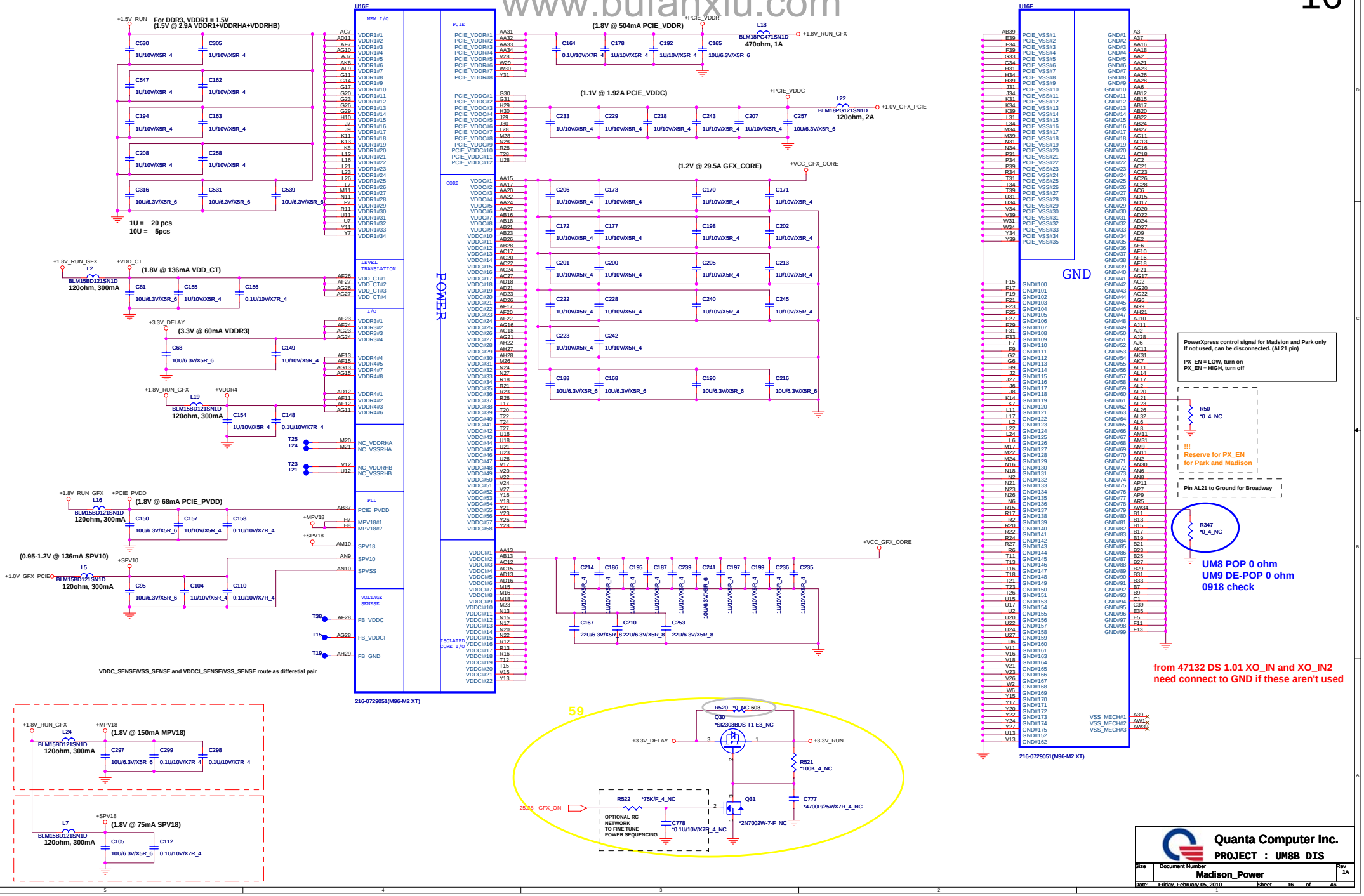
Solve Intermittent System Boot-up Hangs

DDC6CLK/DDC6DATA support internal HDCP(High-bandwidth Digital Content Protection) function.

216-0729051(M96-M2 XT)

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	Madison_IO&STRAP	1A
Date: Friday, February 05, 2010	Sheet 15 of 46	



Quanta Computer Inc.	
PROJECT : UM8B DIS	
Size	Document Number: Madison_Power
Rev	1A
Date: Friday, February 05, 2010	Sheet 16 of 46

!!!
For M96/92, DPx_VDD10 = 1.1
For M97 DPx_VDD10 = 1.0V

DPC & DPD aren't used.

U16H

DP C/D POWER

DP A/B POWER

+1.8V_RUN_GFX

AP20 DPC_VDD18#1
AP21 DPC_VDD18#2

C499 *0.1U/10V/X7R_4_NC

+1.0V_GFX_PCIE

AP13 DPC_VDD10#1
AT13 DPC_VDD10#2

C106 *0.1U/10V/X7R_4_NC

AN17 DPC_VSSR#1
AP16 DPC_VSSR#2
AP17 DPC_VSSR#3
AW14 DPC_VSSR#4
AW16 DPC_VSSR#5

DPA_VDD18#1 AN24
DPA_VDD18#2 AP24

+DPA_VDD18

+DPA_VDD10

(1V @ 200mA DPA_VDD10)

L3 BLM15BD121SN1D 120ohm, 300mA

+1.0V_GFX_PCIE

DPA for HDMI

DPA_VDD10#1 AP31
DPA_VDD10#2 AP32

C101 0.1U/10V/X7R_4
C111 1U/10V/X5R_4
C83 10U/6.3V/X5R_6

DPA_VSSR#1 AN27
DPA_VSSR#2 AP27
DPA_VSSR#3 AP28
DPA_VSSR#4 AW24
DPA_VSSR#5 AW26

+1.8V_RUN_GFX

AP22 DPD_VDD18#1
AP23 DPD_VDD18#2

C502 *0.1U/10V/X7R_4_NC

+1.0V_GFX_PCIE

AP14 DPD_VDD10#1
AP15 DPD_VDD10#2

C97 *0.1U/10V/X7R_4_NC

AN19 DPD_VSSR#1
AP18 DPD_VSSR#2
AP19 DPD_VSSR#3
AW20 DPD_VSSR#4
AW22 DPD_VSSR#5

DPB_VDD18#1 AP25
DPB_VDD18#2 AP26

+DPB_VDD18

+1.8V_RUN_GFX

C513 *0.1U/10V/X7R_4_NC

DPB_VDD10#1 AN33
DPB_VDD10#2 AP33

+1.0V_GFX_PCIE

C67 *0.1U/10V/X7R_4_NC

DPB_VSSR#1 AN29
DPB_VSSR#2 AP29
DPB_VSSR#3 AP30
DPB_VSSR#4 AW30
DPB_VSSR#5 AW32

(1.8V @ 20 mA DPA_PVDD)

(1.8V @ 400mA DPE_VDD18;
200mA for DPE/DPF respectively)

+DPE_VDD18

L10 BLM18PG600SN1D 60ohm, 500mA

+1.8V_RUN_GFX

C131 10U/6.3V/X5R_6
C128 1U/10V/X5R_4
C127 0.1U/10V/X7R_4

DPE & DPF for LVDS

150/F_4 R344 AW18

DPCD_CALR

DPAB_CALR

AW28 R345 150/F_4

DP E/F POWER

DP PLL POWER

DPE_VDD18#1 AH34
DPE_VDD18#2 AJ34

DPA_PVDD AU28
DPA_PVSS AV27

+DPA_PVDD

L33 BLM15BD121SN1D 120ohm, 300mA

+1.8V_RUN_GFX

C511 0.1U/10V/X7R_4
C501 1U/10V/X5R_4
C498 10U/6.3V/X5R_6

+DPE_VDD10

DPE_VDD10#1 AL33
DPE_VDD10#2 AM33

DPB_PVDD AV29
DPB_PVSS AR28

+1.8V_RUN_GFX

C492 *0.1U/10V/X7R_4_NC

DPC & DPD aren't used.

DPE_VSSR#1 AN34
DPE_VSSR#2 AP39
DPE_VSSR#3 AR39
DPE_VSSR#4 AU37
DPE_VSSR#5 AW35

DPC_PVDD AU18
DPC_PVSS AV17

+1.8V_RUN_GFX

C494 *0.1U/10V/X7R_4_NC

UM8 POP 0 ohm
UM9 DE-POP 0 ohm
0918 check

R348 0_4

+DPE_VDD18

DPF_VDD18#1 AE34
DPF_VDD18#2 AG34

DPD_PVDD AV19
DPD_PVSS AR18

C508 *0.1U/10V/X7R_4_NC

+DPE_PVDD

(1.8V @ 40mA DPE_PVDD; 20mA
for DPE/DPF respectively)

(1.1V @ 200mA DPE_VDD10;
100mA for DPE/DPF respectively)

+DPE_VDD10

+1.0V_GFX_PCIE

L4 BLM15BD121SN1D 120ohm, 300mA

C94 10U/6.3V/X5R_6
C86 1U/10V/X5R_4
C102 0.1U/10V/X7R_4

DPF_VDD10#1 AK33
DPF_VDD10#2 AK34

DPE_PVDD AM37
DPE_PVSS AN38

C529 0.1U/10V/X7R_4
C528 1U/10V/X5R_4
C523 10U/6.3V/X5R_6

L35 BLM15BD121SN1D 120ohm, 300mA

+1.8V_RUN_GFX

DPF_VSSR#1 AE39
DPF_VSSR#2 AH39
DPF_VSSR#3 AK39
DPF_VSSR#4 AL34
DPF_VSSR#5 AM34

NC_DPF_PVDD AL38
NC_DPF_PVSS AM35

150/F_4 R354 AM39

DPEF_CALR

216-0729051(M96-M2 XT)

+DPA_VDD18

(1.8V @ 110mA DPA_VDD18)

L34 BLM15BD121SN1D 120ohm, 300mA

+1.8V_RUN_GFX

C87 0.1U/10V/X7R_4
C512 1U/10V/X5R_4
C500 10U/6.3V/X5R_6

from 47132 DS 1.01 XO_IN and XO_IN2
need connect to GND if these aren't used

U16G

LVDS CONTROL

R346 10K_4
R30 10K_4

VARY_BL AK27 BIA_PWM 22
DIGON AJ27 ENVDD 22

LVTMDP

TXCLK_UP_DPF3P AK35
TXCLK_UN_DPF3N AL36

TXOUT_U0P_DPF2P AJ38
TXOUT_U0N_DPF2N AK37

TXOUT_U1P_DPF1P AH35
TXOUT_U1N_DPF1N AJ36

TXOUT_U2P_DPF0P AG38
TXOUT_U2N_DPF0N AH37

TXOUT_U3P AF35 PAD T37
TXOUT_U3N AG36 PAD T20

TXCLK_LP_DPE3P AP34 LCD_ACLK+ LCD_ACLK+ 22
TXCLK_LN_DPE3N AR34 LCD_ACLK- LCD_ACLK- 22

TXOUT_L0P_DPE2P AW37 LCD_A0+ LCD_A0+ 22
TXOUT_L0N_DPE2N AU35 LCD_A0- LCD_A0- 22

TXOUT_L1P_DPE1P AR37 LCD_A1+ LCD_A1+ 22
TXOUT_L1N_DPE1N AU39 LCD_A1- LCD_A1- 22

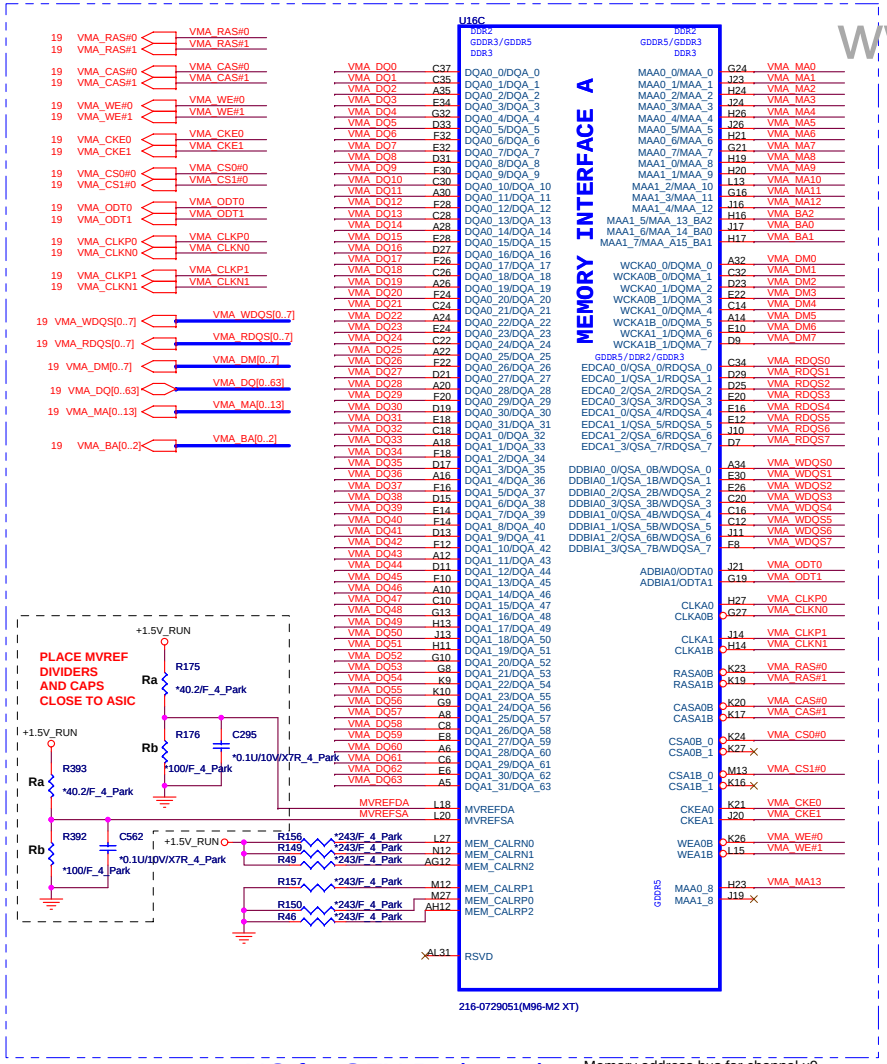
TXOUT_L2P_DPE0P AP35 LCD_A2+ LCD_A2+ 22
TXOUT_L2N_DPE0N AR35 LCD_A2- LCD_A2- 22

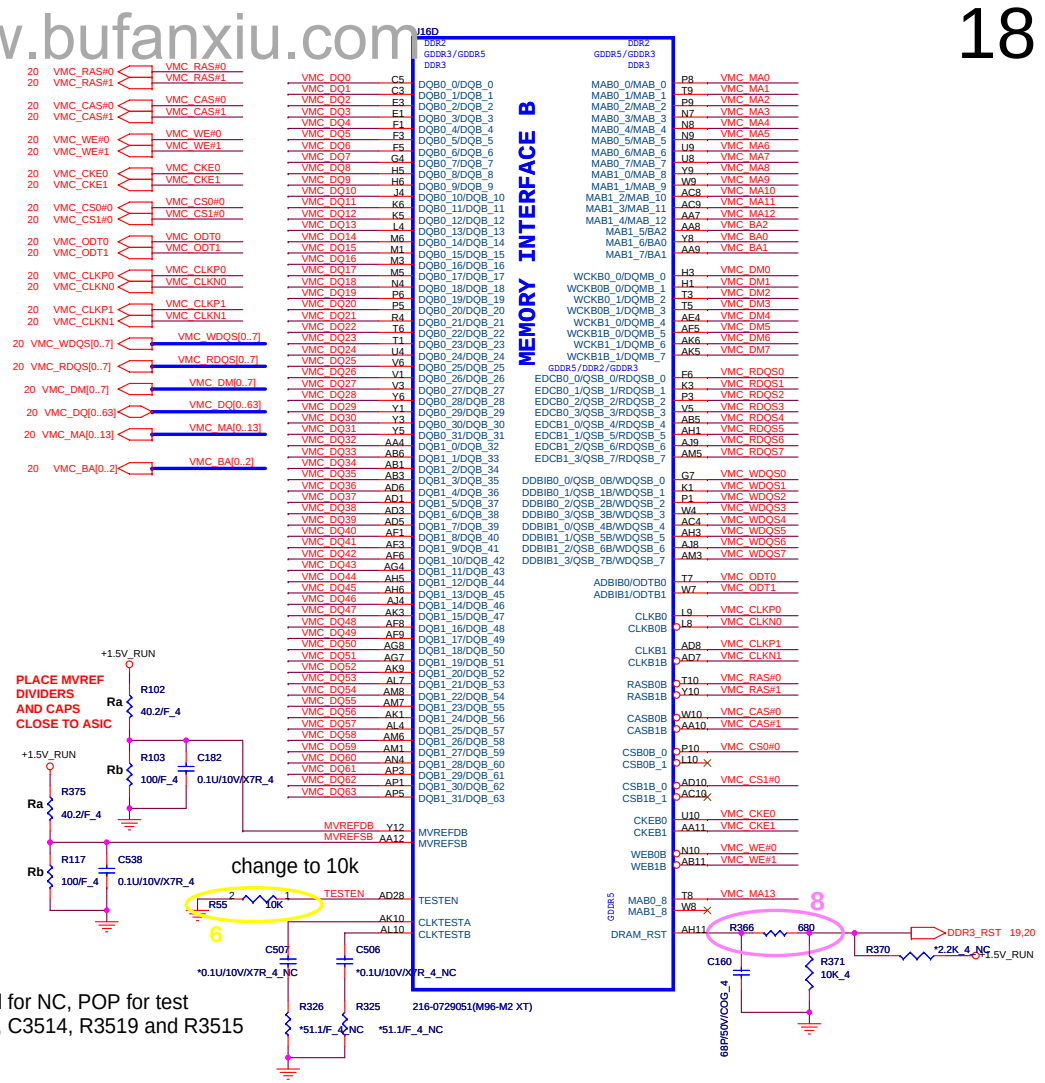
TXOUT_L3P AN36 PAD T36
TXOUT_L3N AP37 PAD T35

216-0729051(M96-M2 XT)

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	Madison_DP_POWER	1A
Date: Friday, February 05, 2010	Sheet 17 of 46	





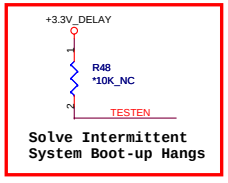
Normal for NC, POP for test
C3513, C3514, R3519 and R3515

NC for GFX Park portion

For Park,Madison production version ASIC is need removed workaround.

Park
pre-production build could get the "ENG" marking.

Madison
- date codes up to 0941 are NOT Production Samples
- date codes from 0942 and up are Production Samples

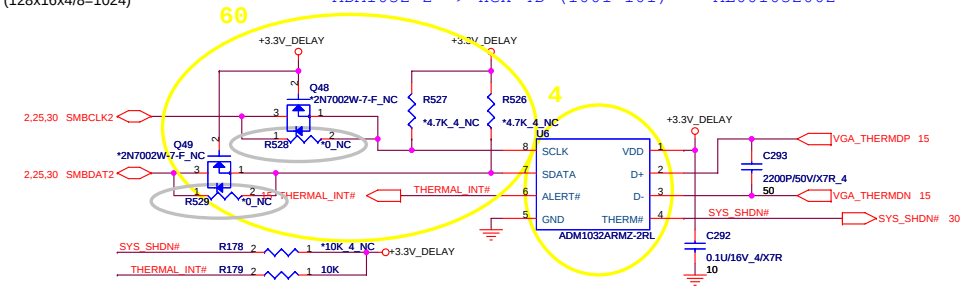


DDR3/GDDR3 Memory Stuff Option

	GDDR3	DDR3
MVDDQ	1.5V/1.8V	1.5V
Ra	40.2R	40.2R
Rb	100R	100R

Memory address bus for channel x0. Provides multiplexed row and column addresses. For 128-Mbit x16 DDR3 support, MAx13 is supported on MAx0_8. (128x16x4/8=1024)

ADM1032-1 => Hex 4C (1001 100) AL001032001
ADM1032-2 => Hex 4D (1001 101) AL001032002



Designator	For M97-M2	For Madison
R272	10K	10K
R271	0R/Short	680R
R273	NC	NC
C408	2.2nF	68pF

Quanta Computer Inc.	
PROJECT : UM8B DIS	
Size	Document Number: Madison_MEMORY/THERM
Rev	1A
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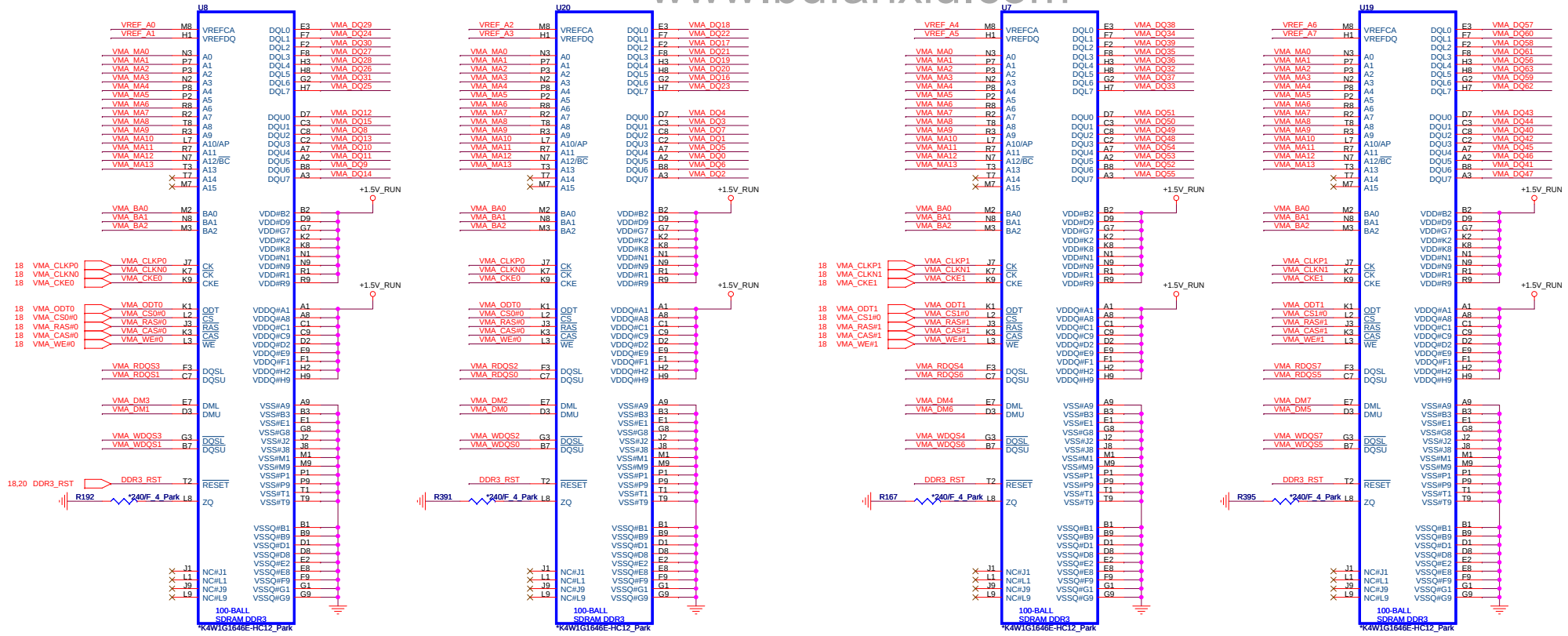
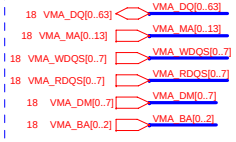
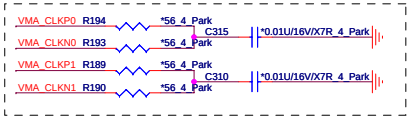
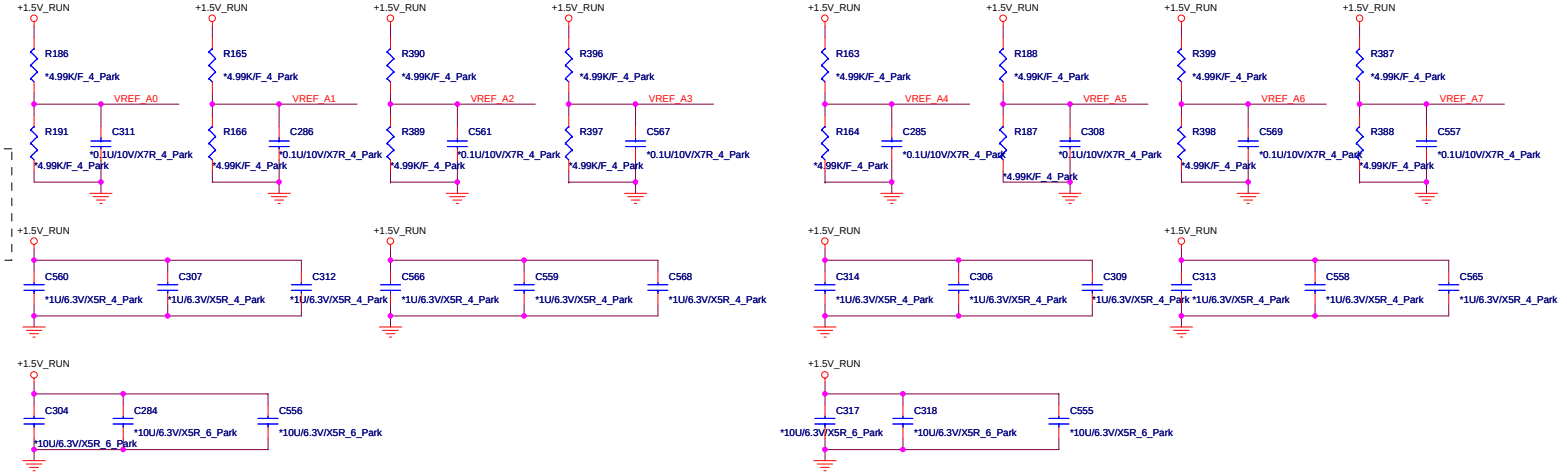
CHECK PN DDR3 64MX16_SH A 512MB





Placement has to be close to VRAM



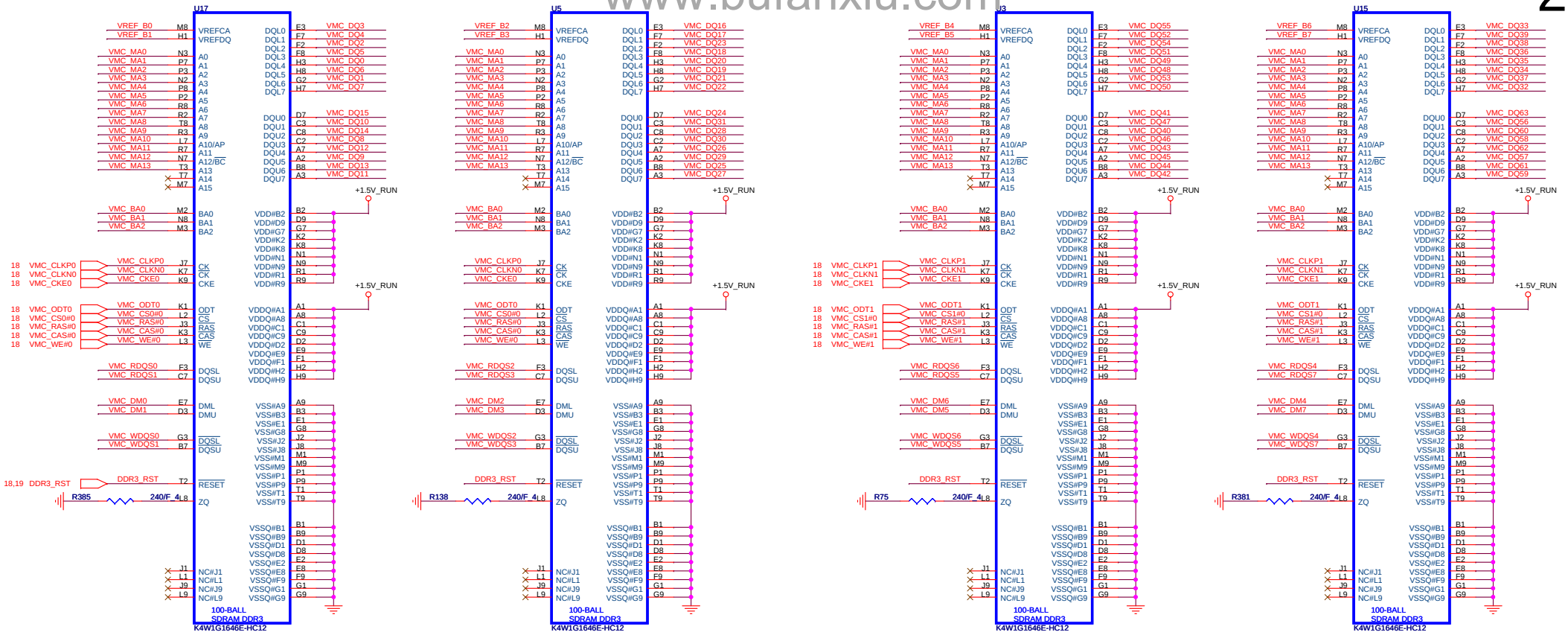


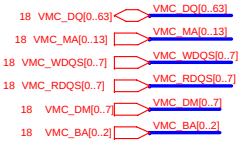
NC for GFX Park portion

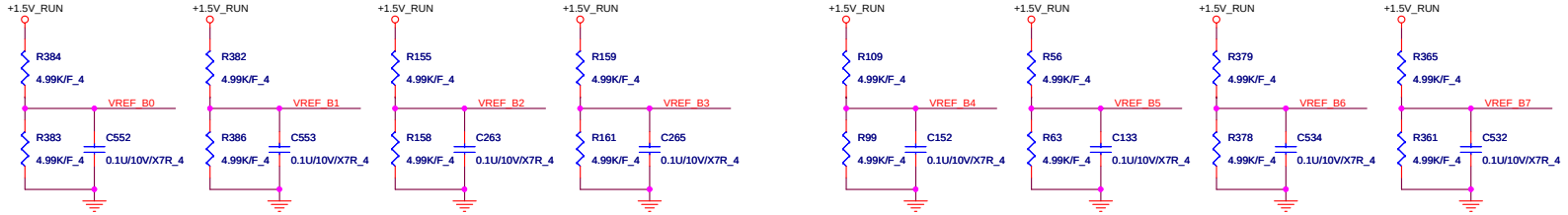
Samsung: AKD5LGGT505
Hynix: AKD5LZGTW03

Quanta Computer Inc.
PROJECT : UM8B DIS

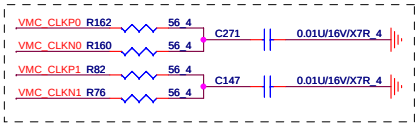
Size	Document Number	Rev
	Madison_DDR3_A_512M	1A
Date: Friday, February 05, 2010	Sheet 19 of 46	

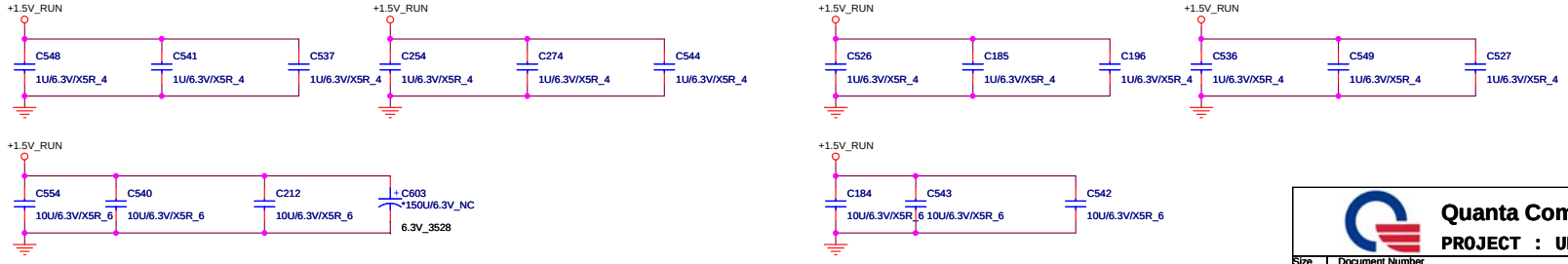






Placement has to be close to VRAM

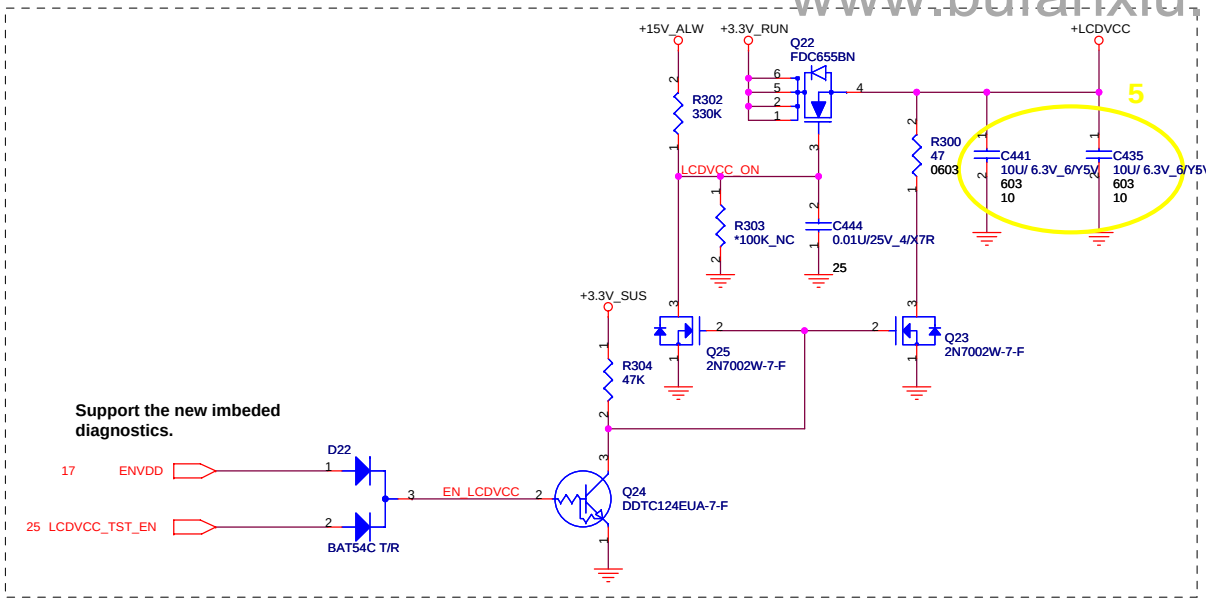


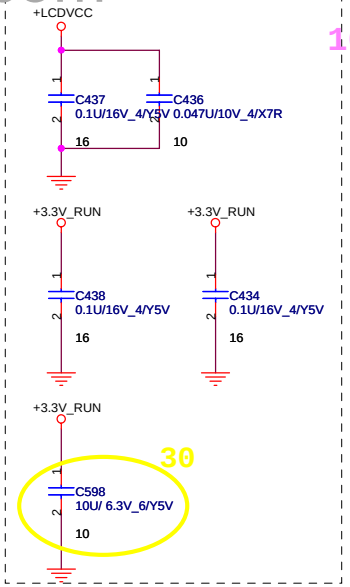


Quanta Computer Inc.

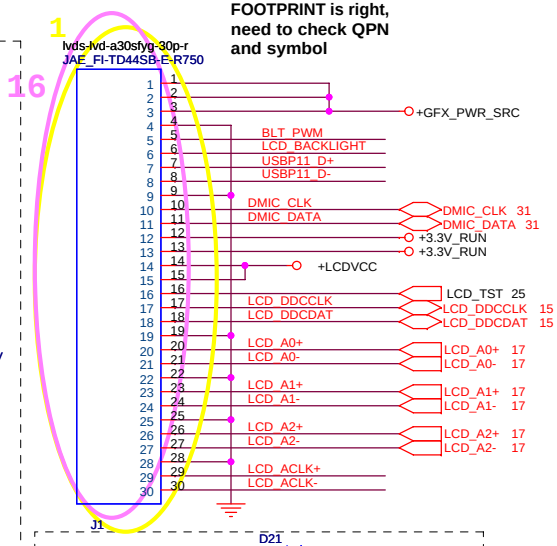
PROJECT : UM8B DIS

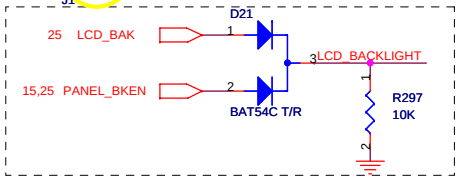
Size	Document Number	Rev
	Madison_DDR3_B_512M	1A
Date: Friday, February 05, 2010	Sheet 20 of 46	

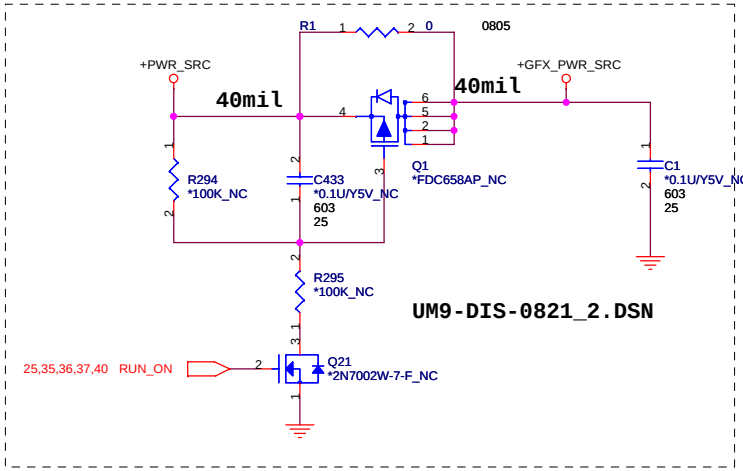


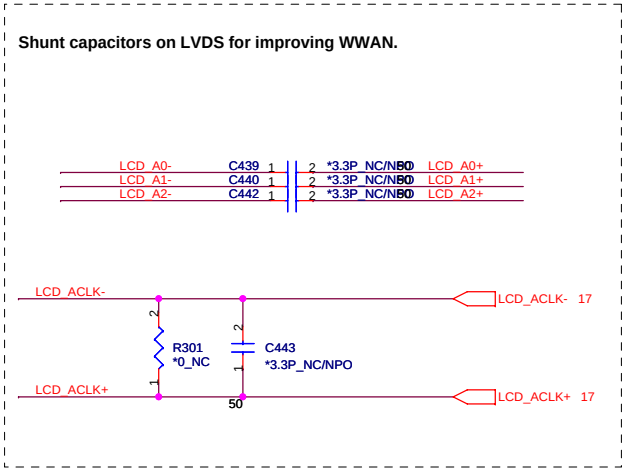


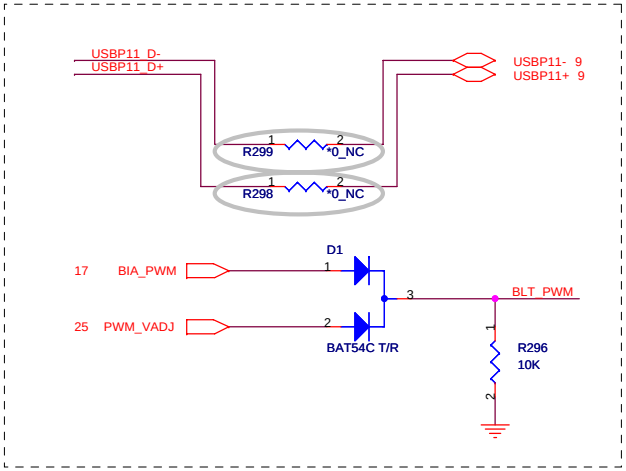
FOOTPRINT is right, need to check QPN and symbol











Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	LCD CONN	1A
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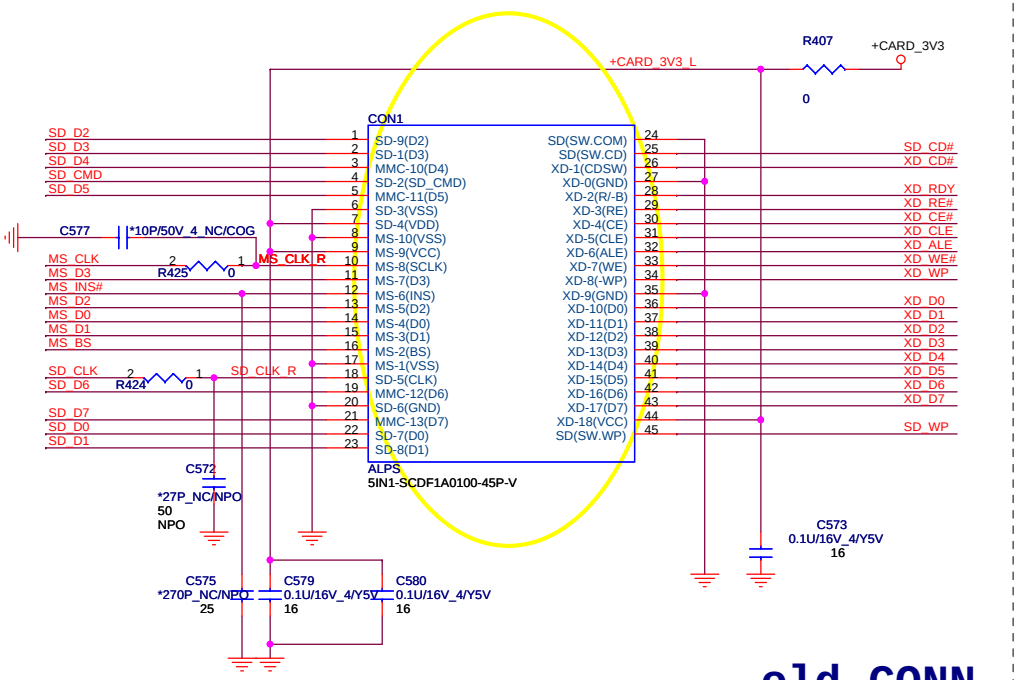
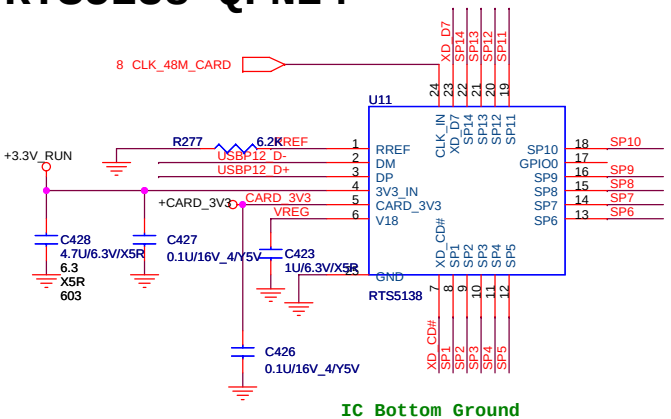


old CONN

RTS5138-QFN24

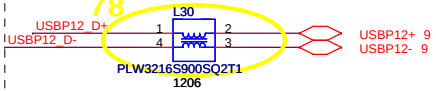


IC Bottom Ground

SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS

Share Pin

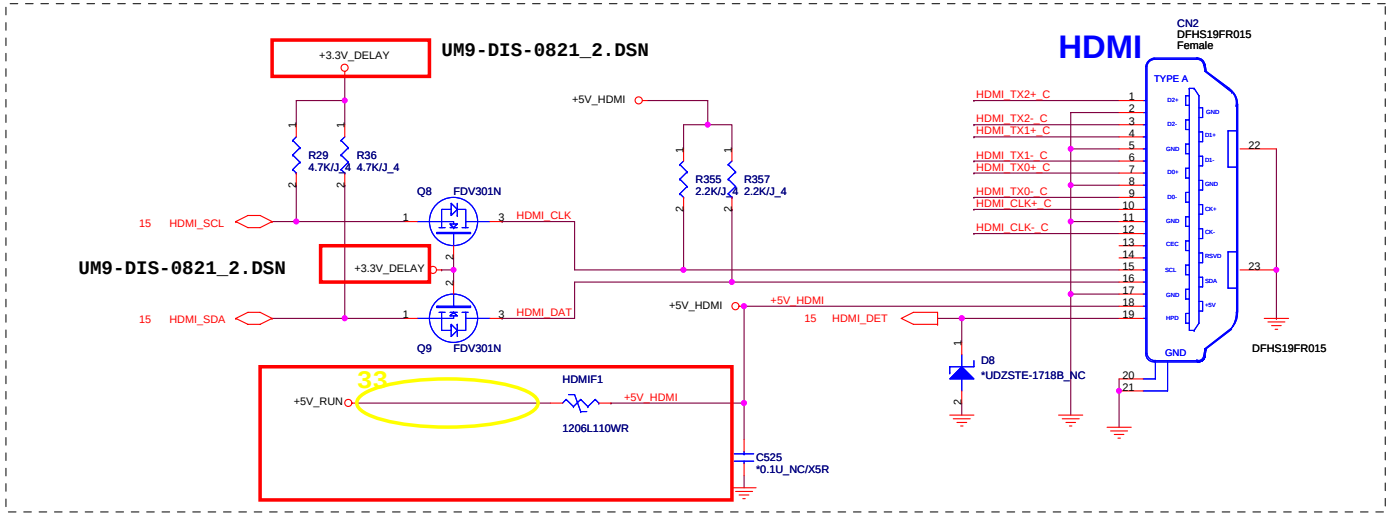
78

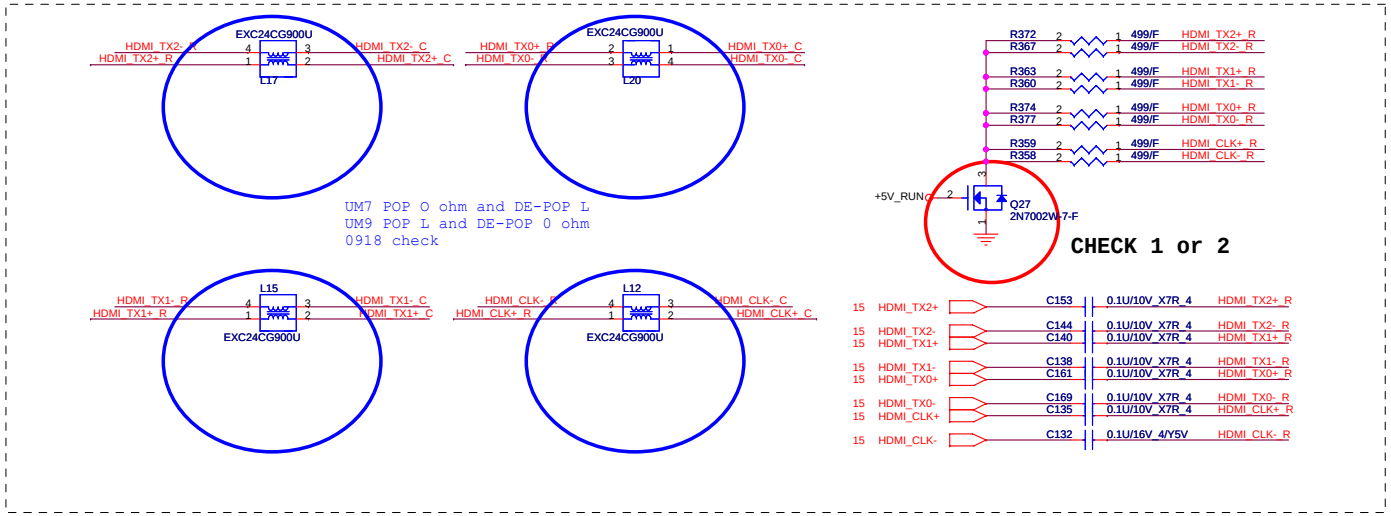


Quanta Computer Inc.

PROJECT : UM8B DIS

Size	Document Number	Rev
	Card Reader(RST5138)	1A
Date: Friday, February 05, 2010	Sheet 23 of 46	





Quanta Computer Inc.			
PROJECT : UM8B DIS			
Size	Document Number		Rev
	HDMI		1A
Date: Friday, February 05, 2010	Sheet 24 of 46		

UM3

U4

ITE8502E
LQFP-128L

KEYBOARD
ADC/DAC
PWM
LPC
IR/UART
SMBUS
LPC/FWH FLASH
EGPC
PS/2
GPIO

ITE8502E
lqfp128-16x16-4

Place these caps close to ITE8502.

SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.

Charge and BAT
PCH
LAN, Clock Thermal IC

32KHz Clock.

Check

UM7 POP 2.2k
UM9 POP 10k
0918 check

UM7 DE-POP
UM9 POP
0918 check

Board ID Straps

Park 1G
Discrete
Park
UMA

VGA_TYPE
VGA_IDENTIFY

	LCD_SIZE_ID (99)	LCD_SIZE_ID2 (107)
13"	0	0
14"	1	0
17"	0	1

BID1	USB_RIGHT_EN#	UM8(UMA)	UM8C (Dis)
0	0	SSI (X00)	SSI (X00)
0	1	PT (X01)	PT (X01)
1	0	ST (X02)	ST (X02)
1	1	OT (A00)	OT (A00)
0	0	(A01)	(A01)

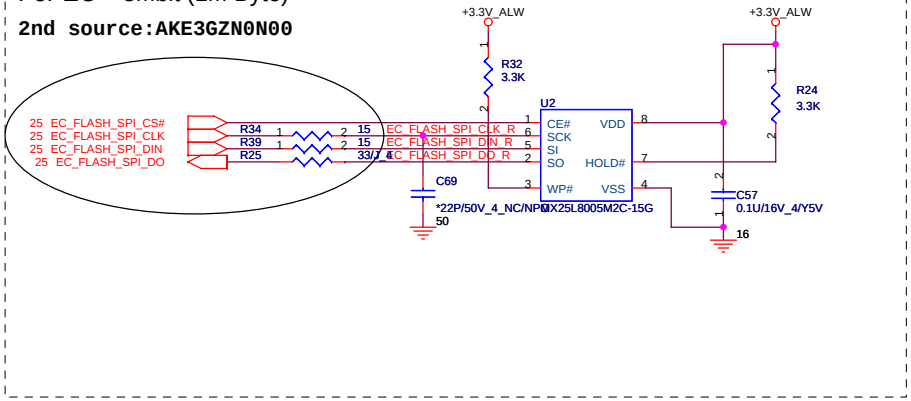
Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	SIO ITE8502	1A

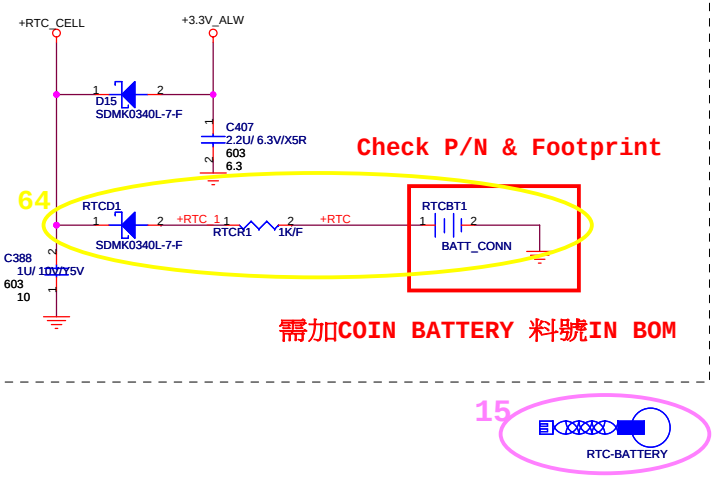
Date: Friday, February 05, 2010 Sheet 25 of 46

For EC 8Mbit (1M Byte)

2nd source:AKE3GZN0N00



RTC BATTERY

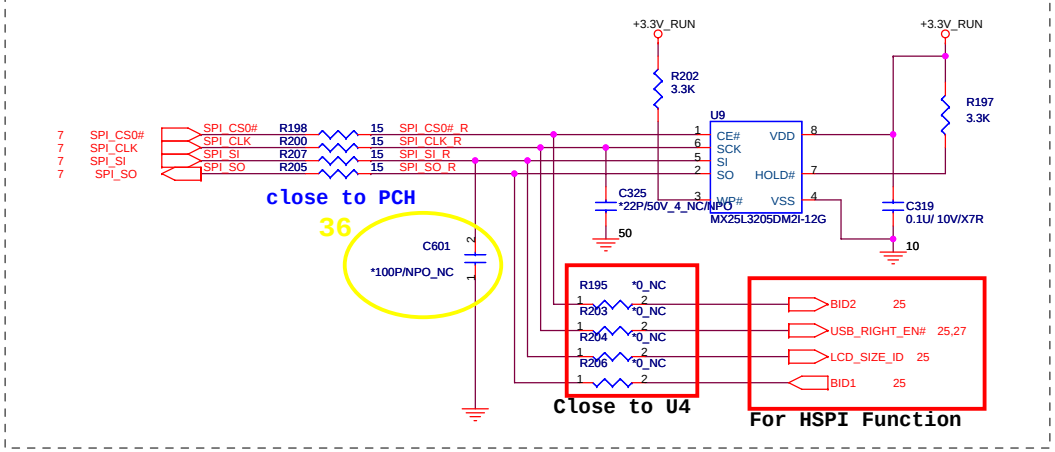


15

For PCH

32Mbit (4M Byte)

2nd source:AKE39ZP0N00



Quanta Computer Inc.

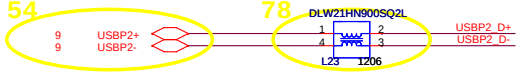
PROJECT : UM8B DIS

Size	Document Number	Rev
	FLASH/RTC	1A

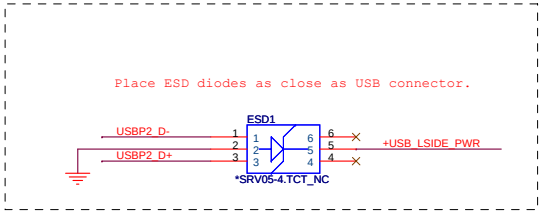
Date: Friday, February 05, 2010 Sheet 26 of 46

eSATA and USB To DB

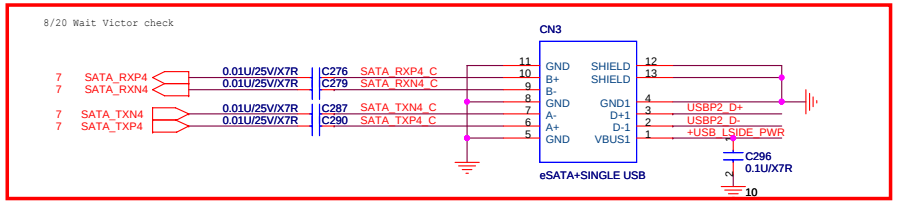
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

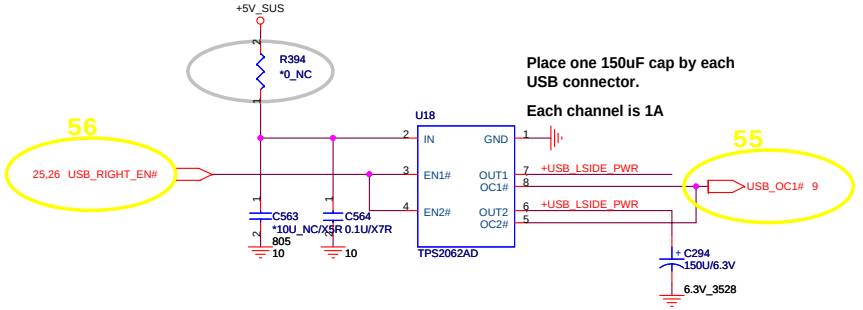


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



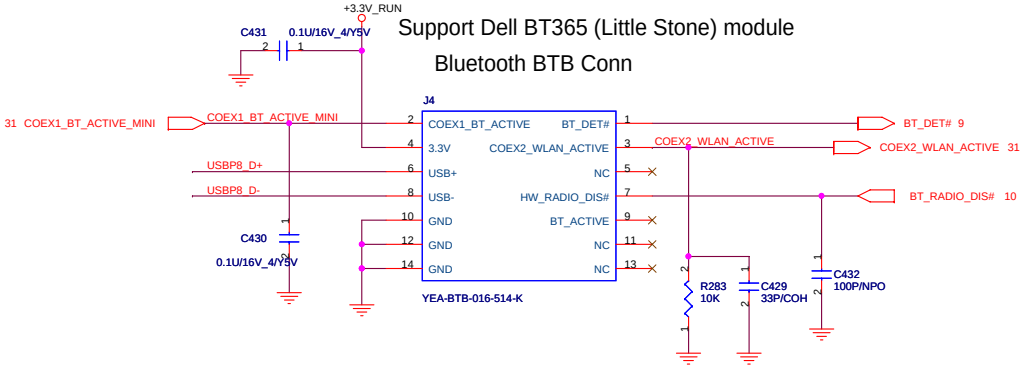
USB and eSATA Conn.

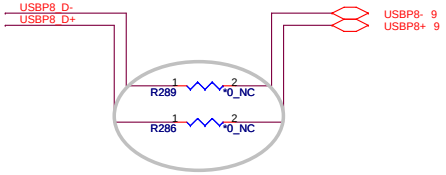




Place one 150uF cap by each USB connector.

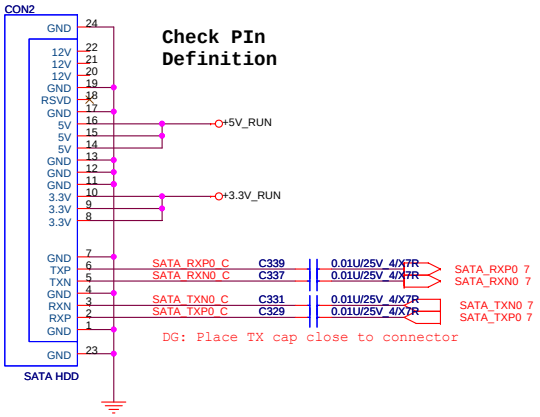
Each channel is 1A

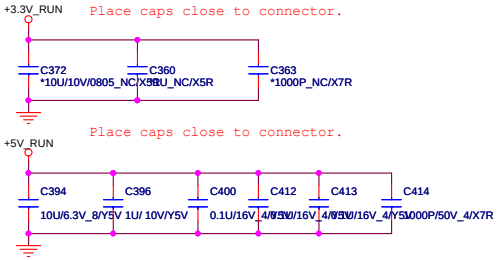




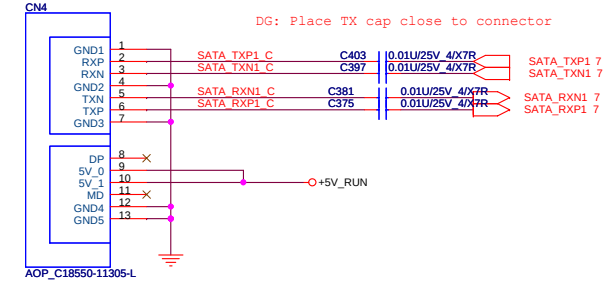
Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: eSATA & Right USB & BT	Rev: 1A
Date: Friday, February 05, 2010	Sheet 27 of 46	

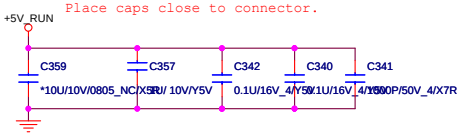
SATA Connector.



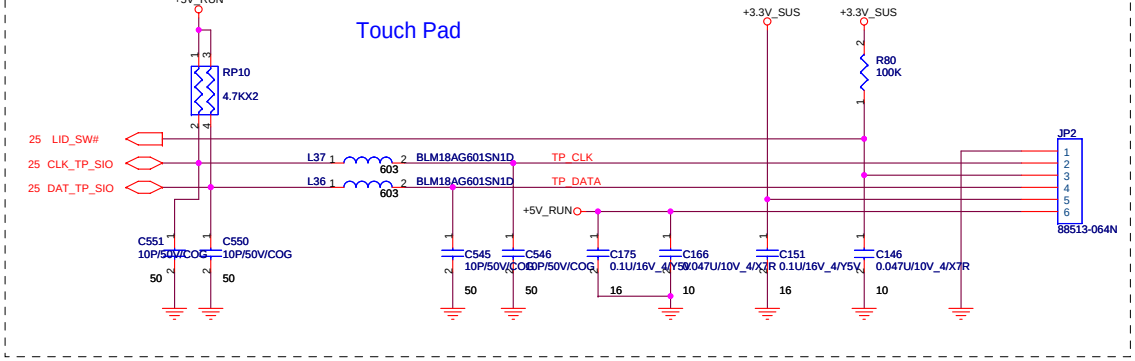


ODD Connector



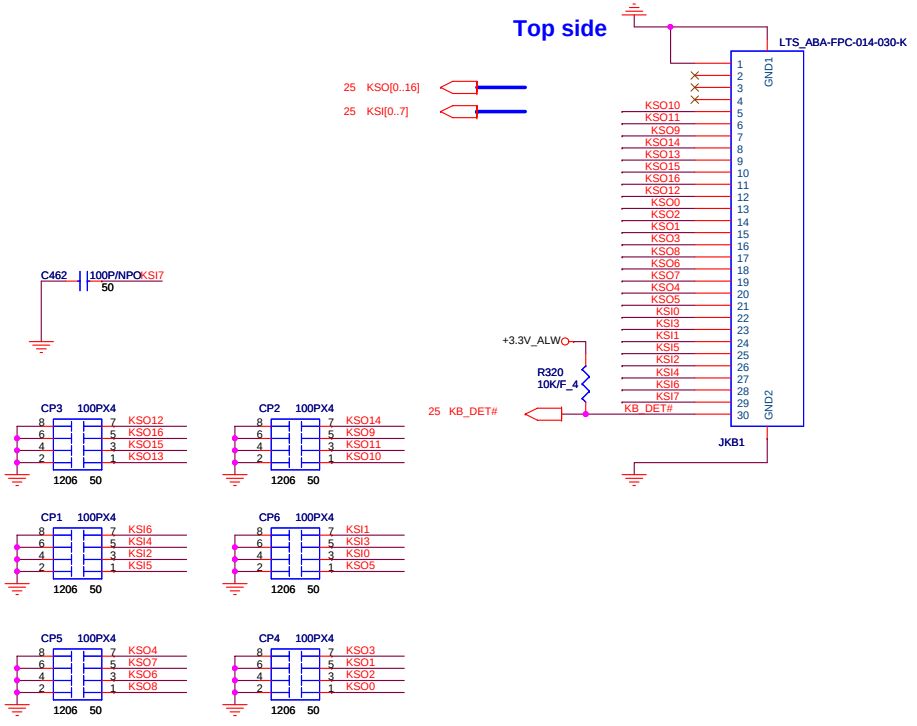


Touch Pad



KEYBOARD CONNECTOR

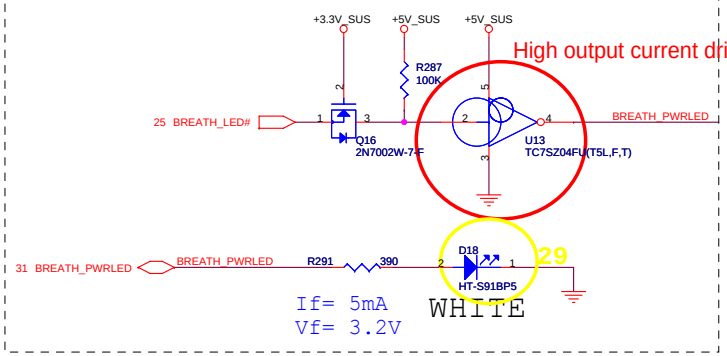
Top side



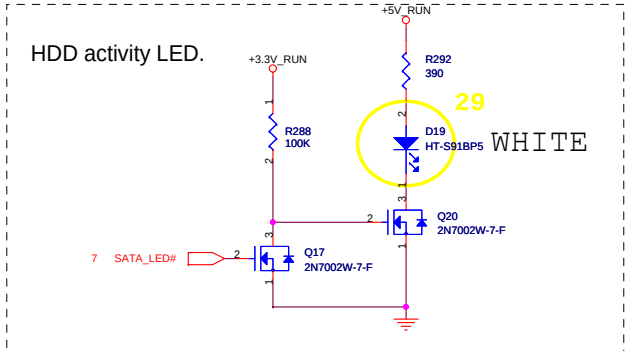
100P CAPS CLOSE TO JKB1

Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: SATA (HDD&ODD) & TP & KB	Rev 1A
Date: Friday, February 05, 2010	Sheet 28 of 46	

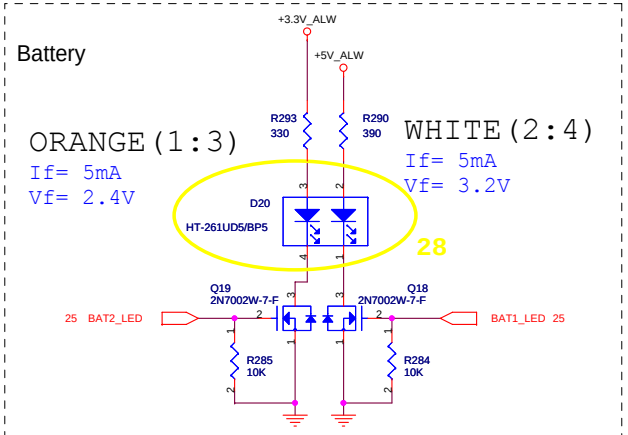
Power



HDD activity LED.



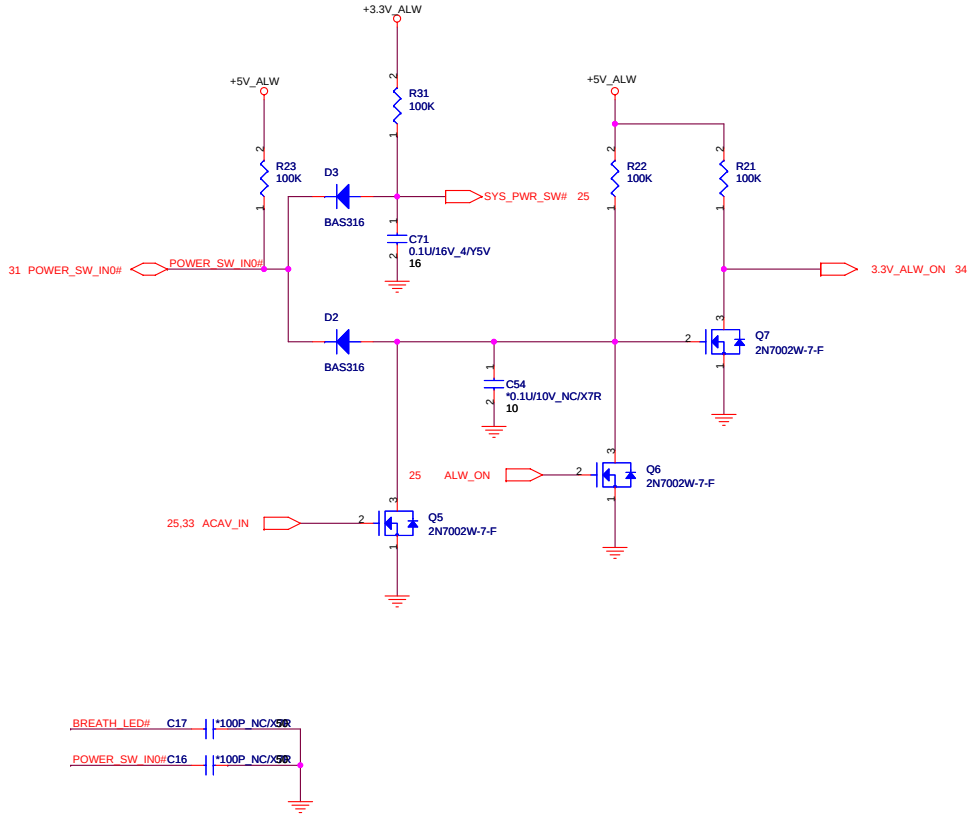
Battery



UM3_DIS_20090824_1000_SSI_STEPHEN.DSN

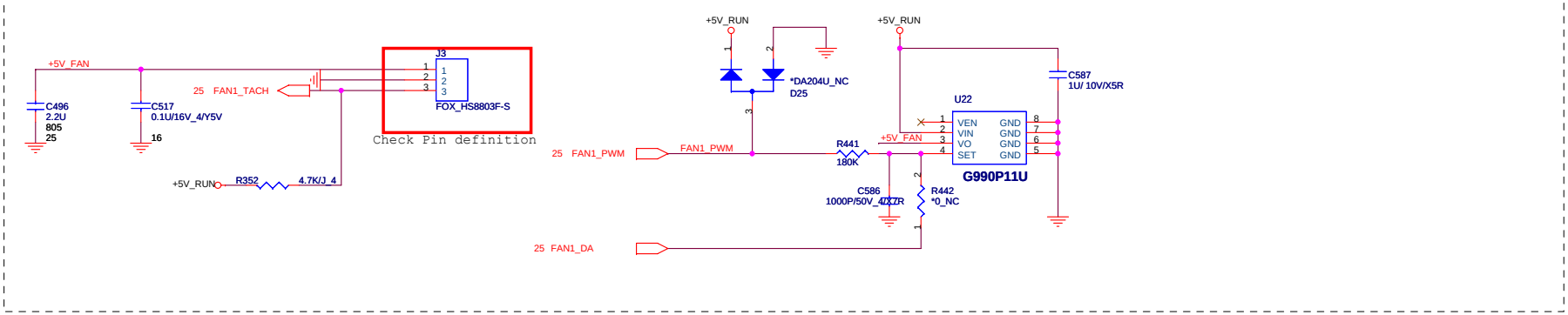
check outpout current for 3 LED

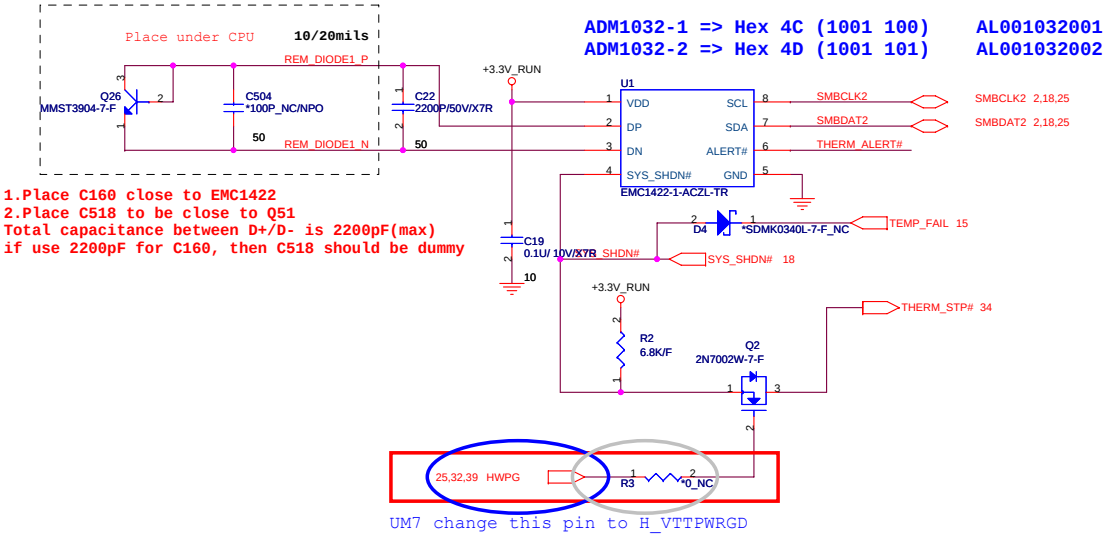
3VALW ON POWER LOGIC

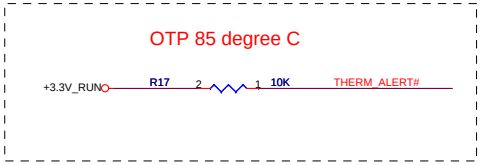


Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: SWITCH, LED	Rev: 1A
Date: Friday, February 05, 2010	Sheet 29 of 46	

FAN CONTROL



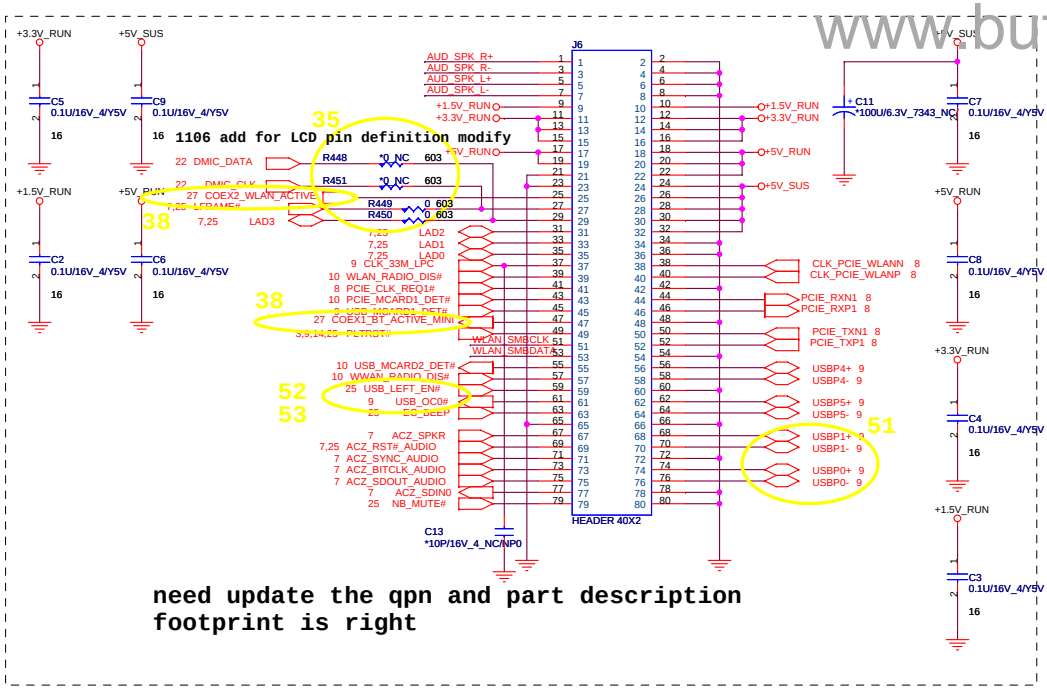




SYS_SHD# / ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C

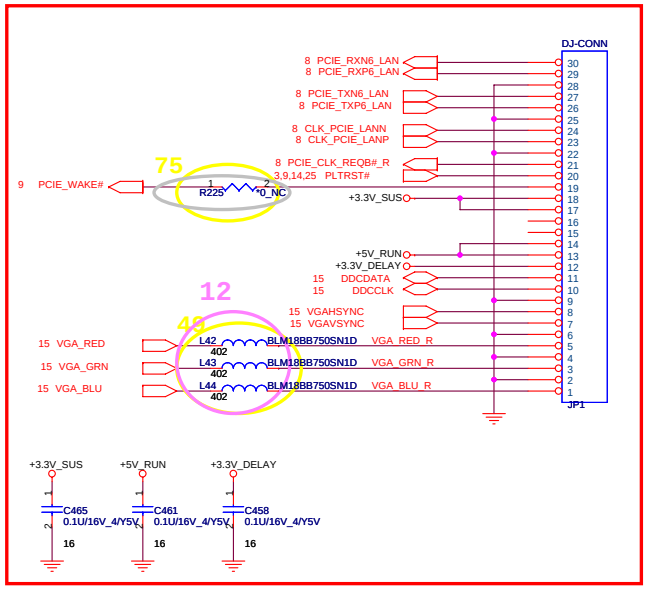
Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	FAN & THERMAL	1A
Date: Friday, February 05, 2010	Sheet 30 of 46	

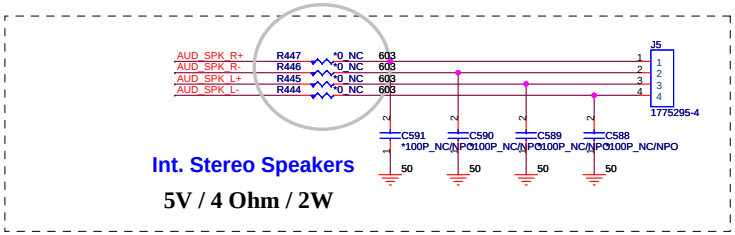


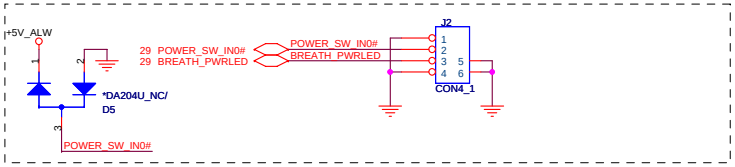
need update the qpn and part description
footprint is right

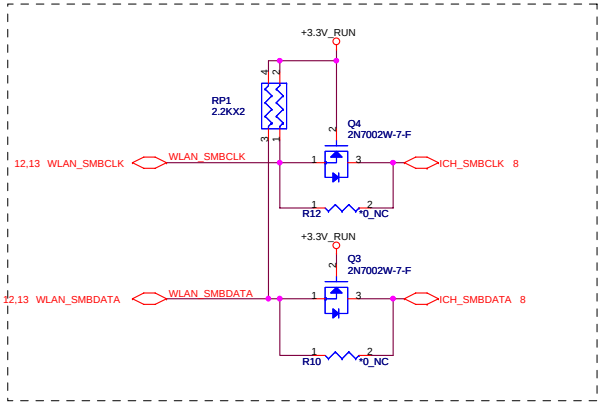
Check P/N and footprint



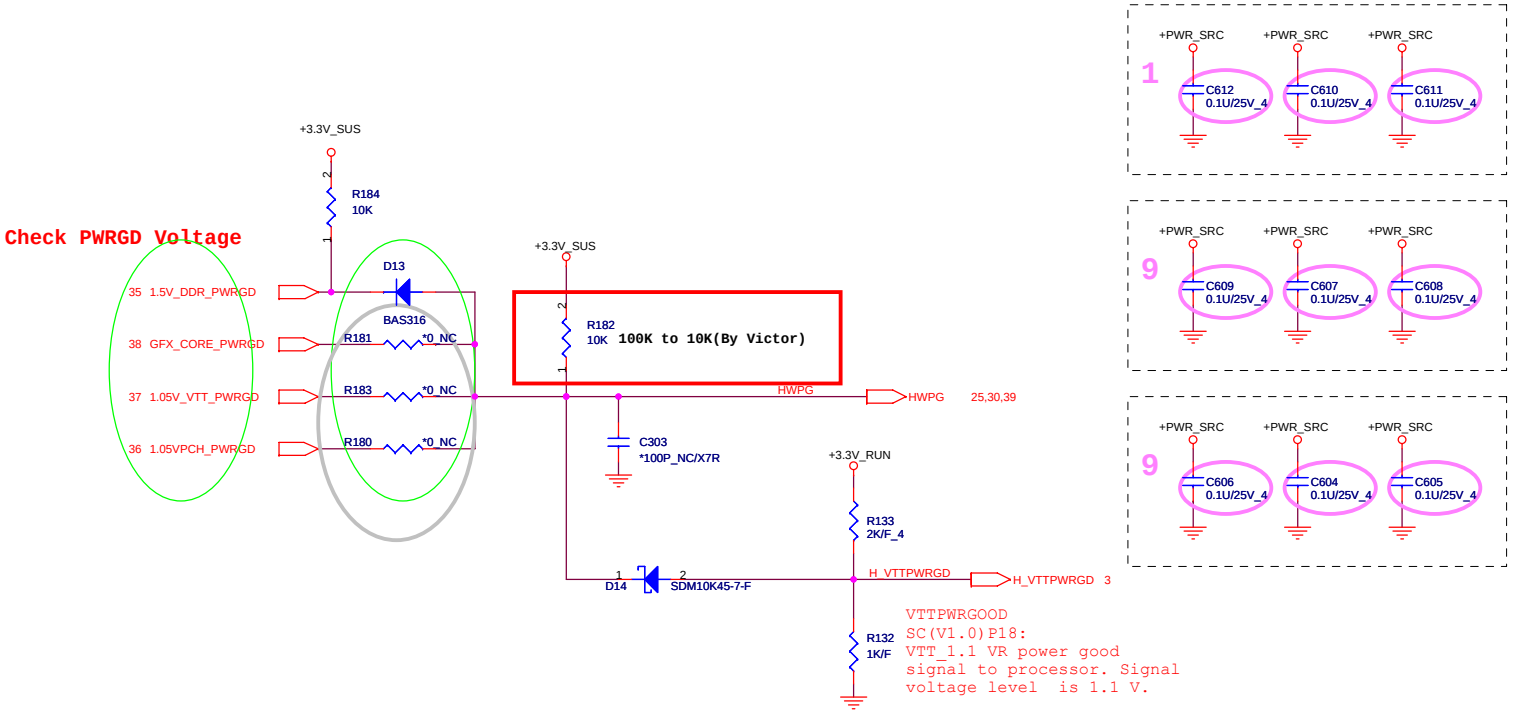
To CRT board





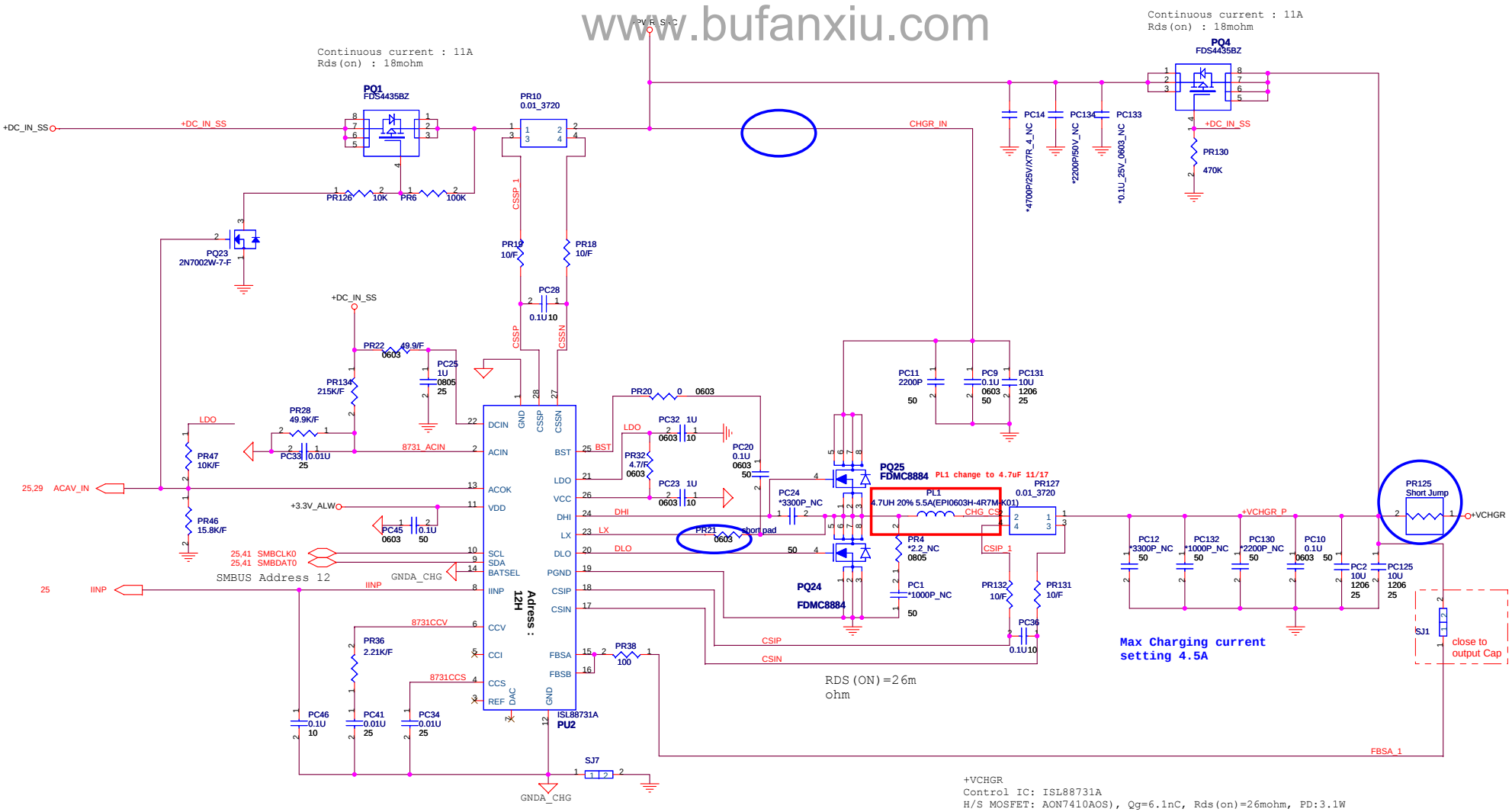


Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number	Rev
	BTB CONN & Audio conn	1A
Date: Friday, February 05, 2010	Sheet 31 of 46	



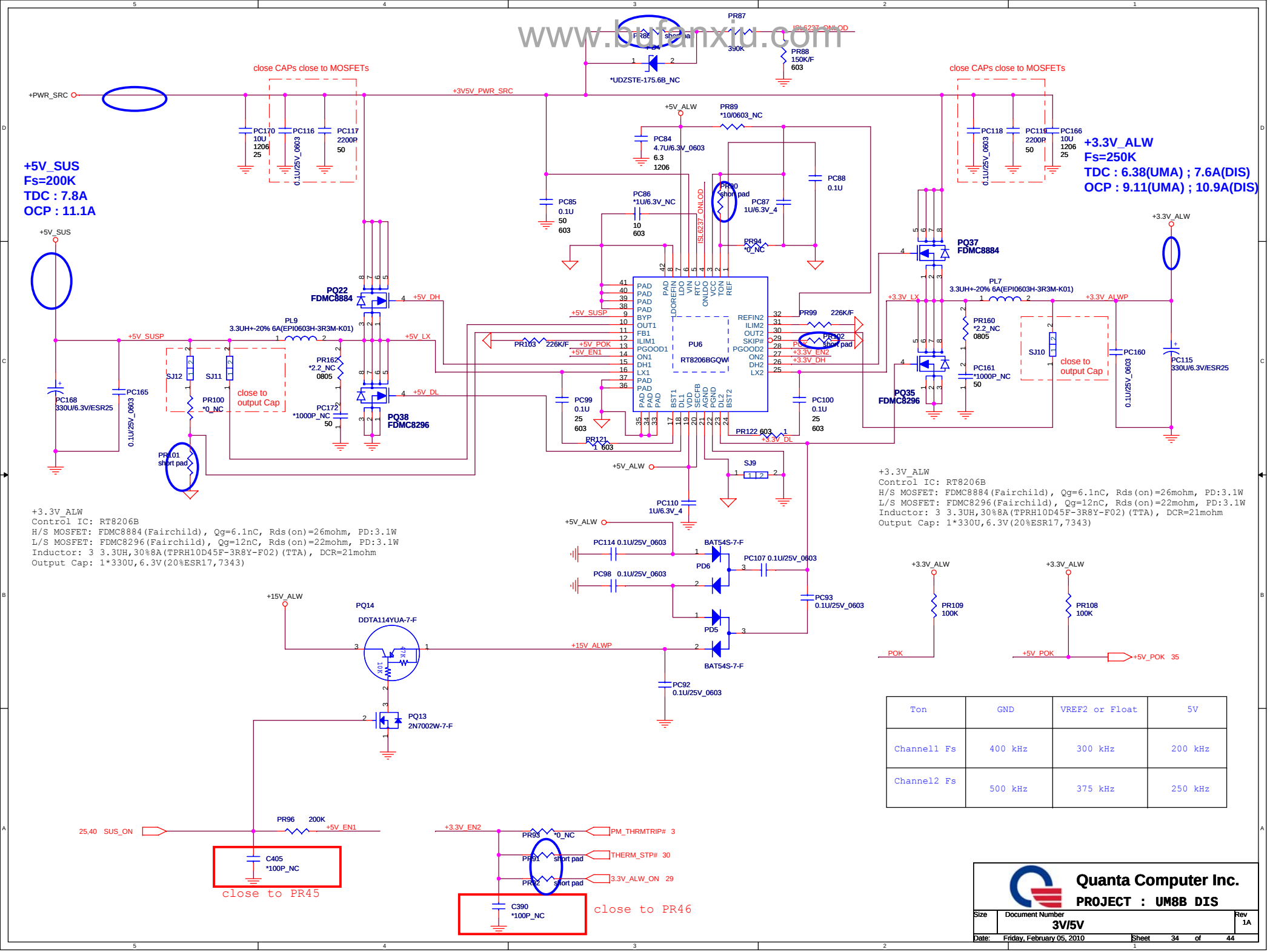
Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	System Reset Circuit	1A
Date: Friday, February 05, 2010	Sheet 32 of 46	



+VCHGR
Control IC: ISL88731A
H/S MOSFET: AON7410AOS), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: AON7410(AOS), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
Inductor: 6.8UH +-30% 5.5A SDSL10D40F-5R8Y(TTA), DCR=21mohm
Output Cap: 2*10U 25V(+-10%,X6S,1206)

Quanta Computer Inc.			
PROJECT : UM8B DIS			
Size	Document Number		Rev
	Charger		1A
Date: Friday, February 05, 2010		Sheet 33 of 44	



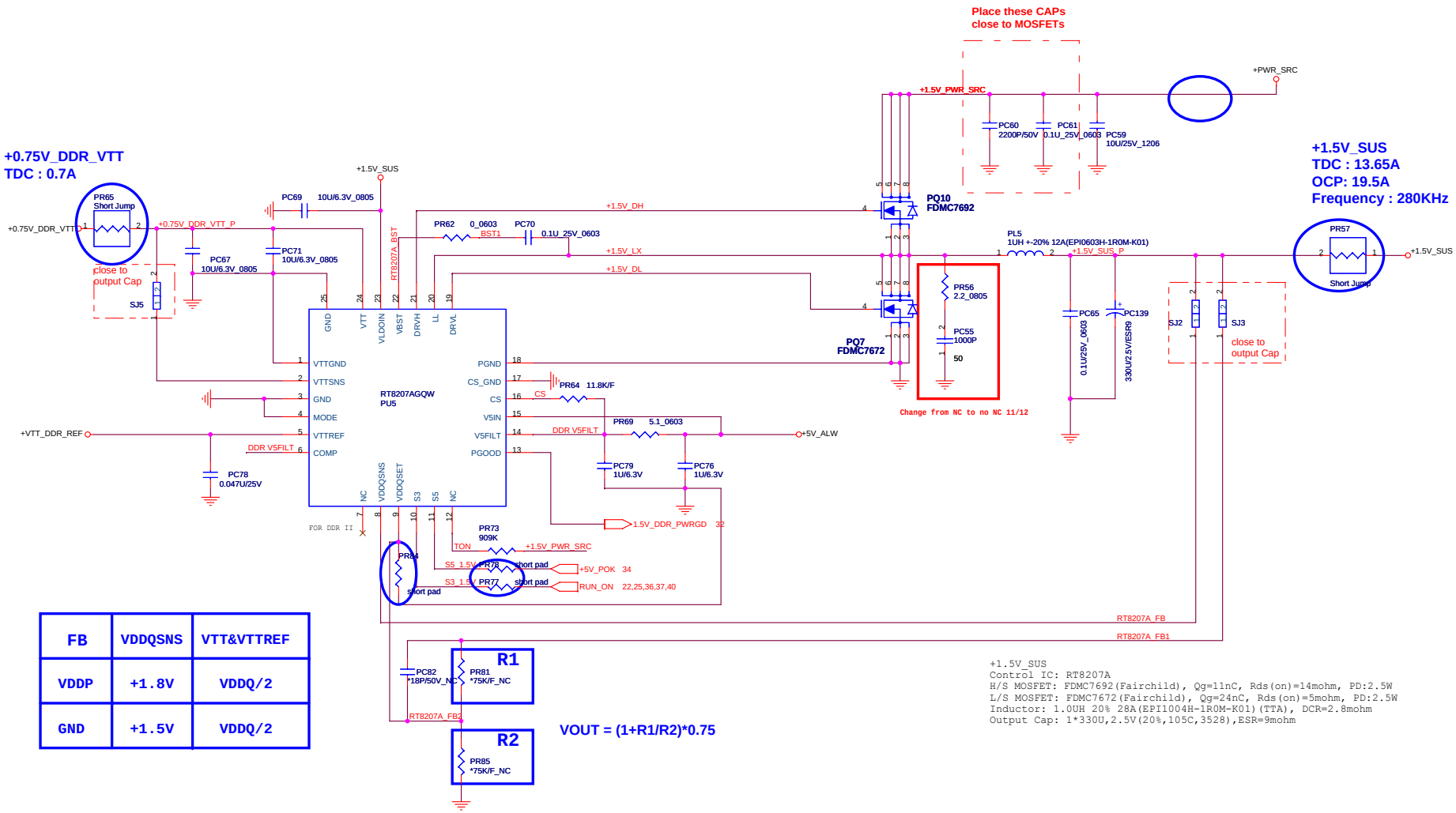
+3.3V_ALW
Control IC: RT8206B
H/S MOSFET: FDMC8884(Fairchild), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: FDMC8296(Fairchild), Qg=12nC, Rds(on)=22mohm, PD:3.1W
Inductor: 3 3.3UH,30%8A(TPRH10D45F-3R8Y-F02)(TTA), DCR=21mohm
Output Cap: 1*330U,6.3V(20%ESR17,7343)

+3.3V_ALW
Control IC: RT8206B
H/S MOSFET: FDMC8884(Fairchild), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: FDMC8296(Fairchild), Qg=12nC, Rds(on)=22mohm, PD:3.1W
Inductor: 3 3.3UH,30%8A(TPRH10D45F-3R8Y-F02)(TTA), DCR=21mohm
Output Cap: 1*330U,6.3V(20%ESR17,7343)

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	3V/5V	1A
Date: Friday, February 05, 2010	Sheet 34 of 44	



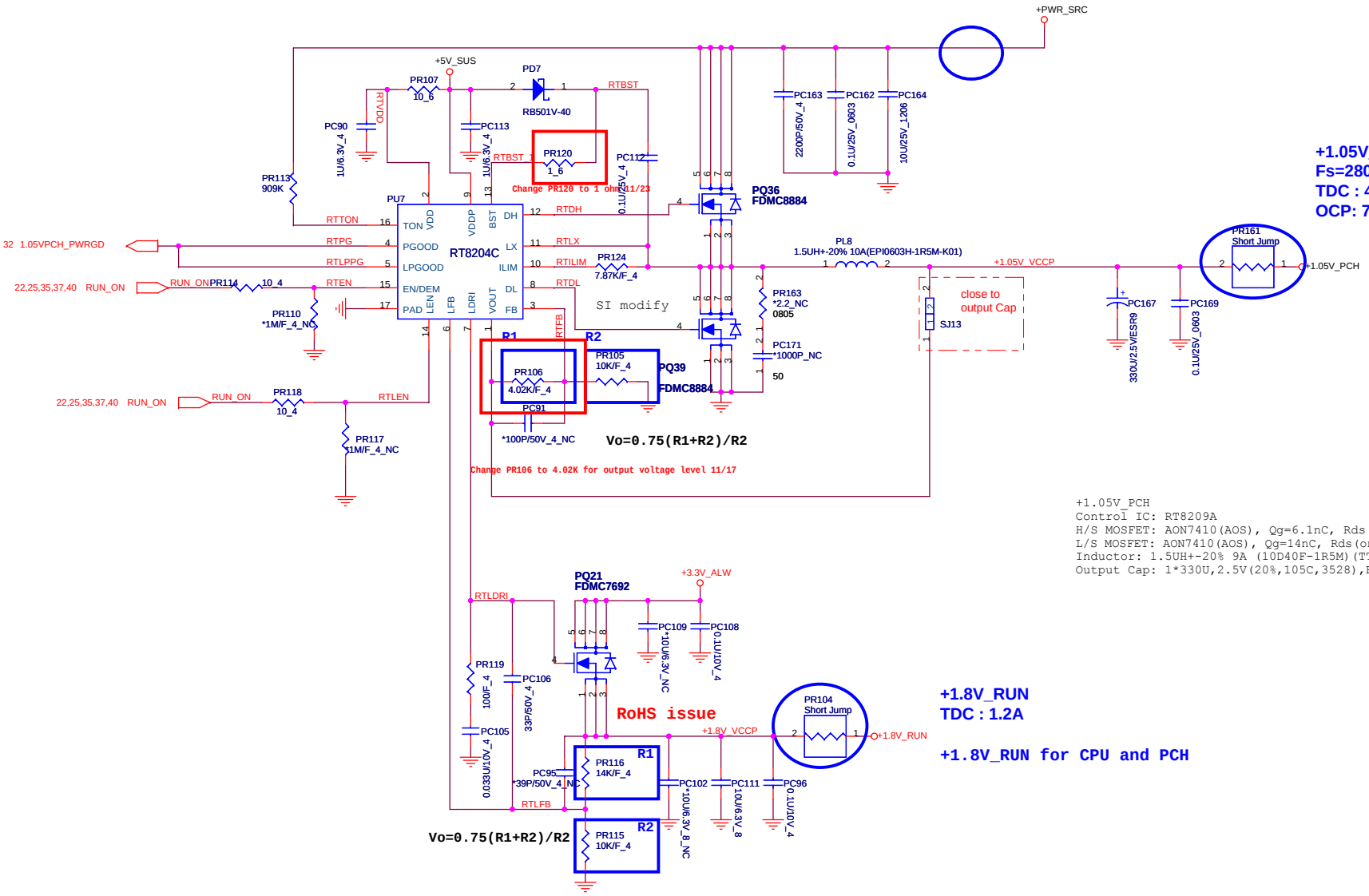
FB	VDDQSNS	VTT&VTTREF
VDDP	+1.8V	VDDQ/2
GND	+1.5V	VDDQ/2

+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDMC7692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMC7672(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 1.0UH 20% 28A(EPI1004H-1R0M-K01)(TTA), DCR=2.8mohm
Output Cap: 1*330U,2.5V(20%,105C,3528),ESR=9mohm

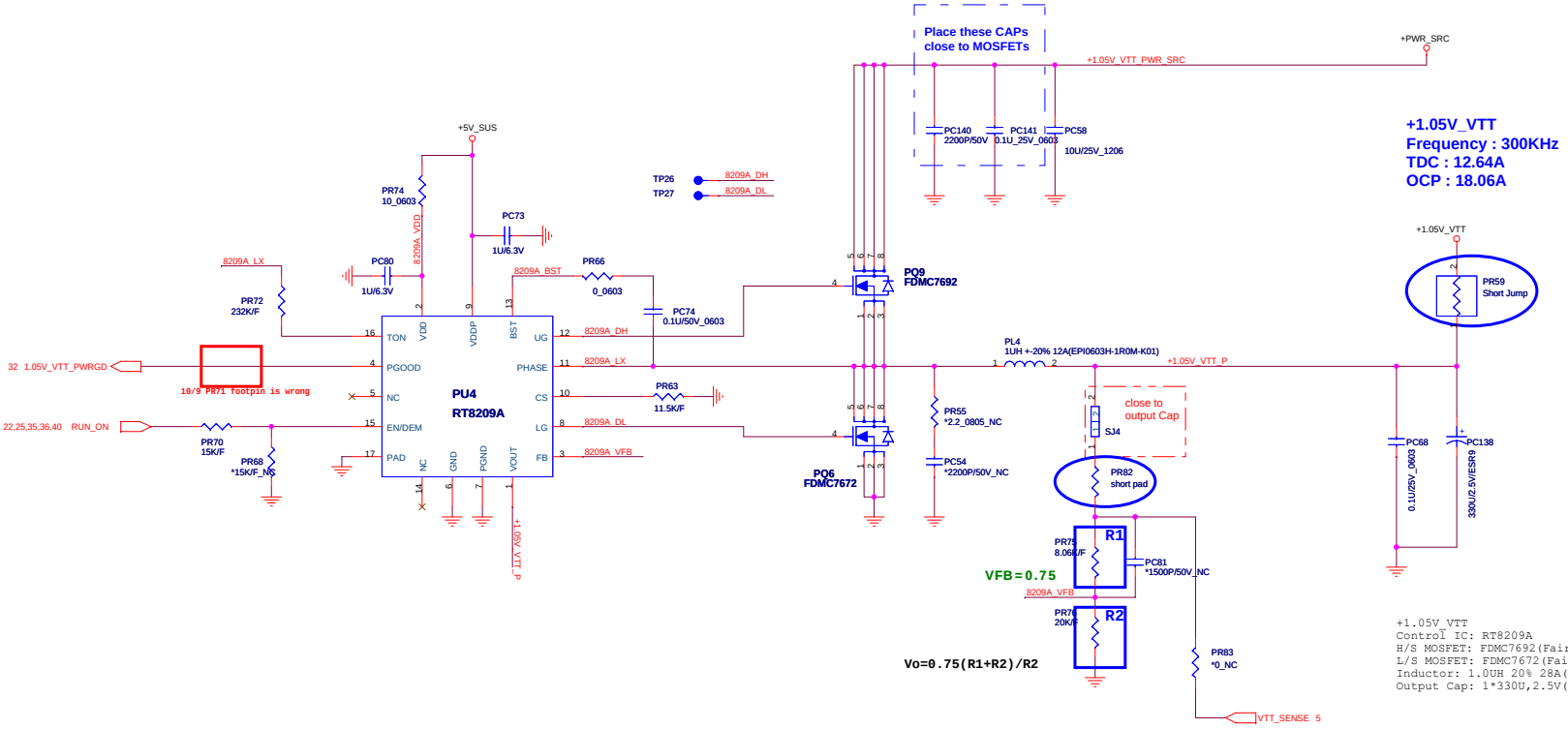
Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	1.5V_DDR/0.75V	1A

Date: Friday, February 05, 2010 Sheet 35 of 44



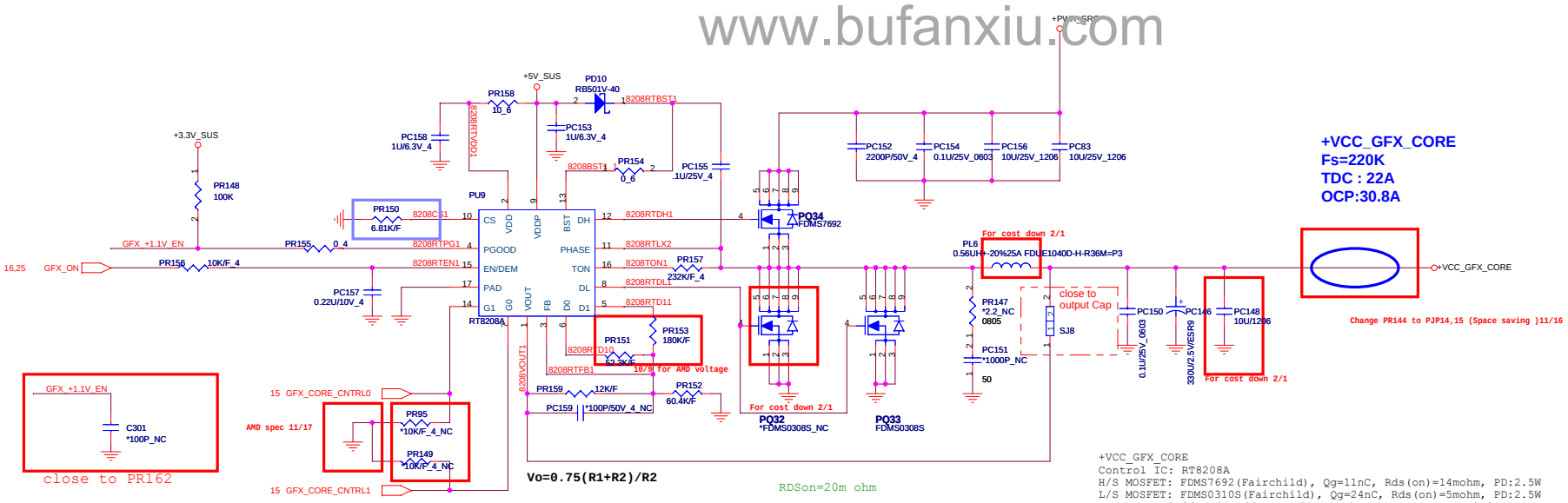
Quanta Computer Inc.		
PROJECT : UM8B DIS		
Size	Document Number: 1.05V_PCH	Rev: 1A
Date: Friday, February 05, 2010	Sheet 36 of 44	



+1.05V_VTT
Control IC: RT8209A
H/S MOSFET: FDMC7692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMC7672(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 1.0UH 20% 28A(EPI1004H-1R0M-K01)(TTA), DCR=2.8mohm
Output Cap: 1*330U,2.5V(20%,105C,3528),ESR=9mohm

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	1.05V_VTT	1A
Date: Friday, February 05, 2010	Sheet 37 of 44	



+VCC_GFX_CORE
Control IC: RT8208A
H/S MOSFET: FDMS7692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS0310S(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.36UH 20% 28A(EPI1004H-1R0M-K01)(TTA), DCR=2.8mohm
Output Cap: 2*330U,2.5V(20%,105C,3528),ESR=9mohm

+VCC_GFX_CORE_M92

For M96-LP:

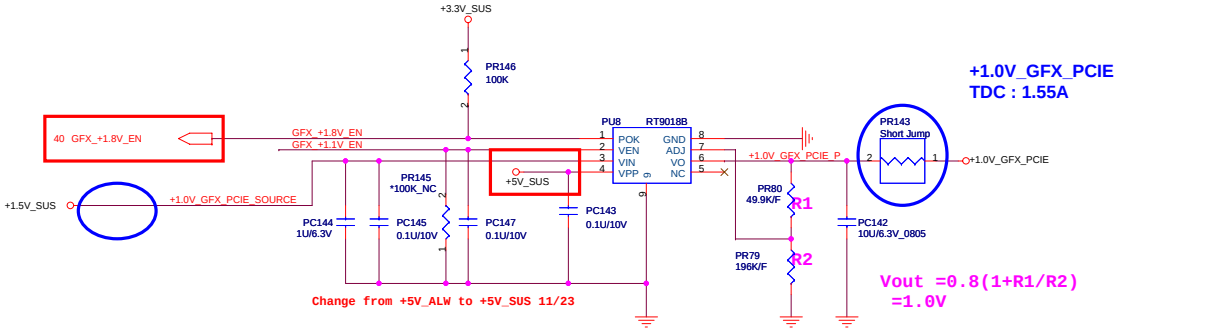
GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
LOW	HIGH	1.0V
HIGH	HIGH	1.05V(N/A)

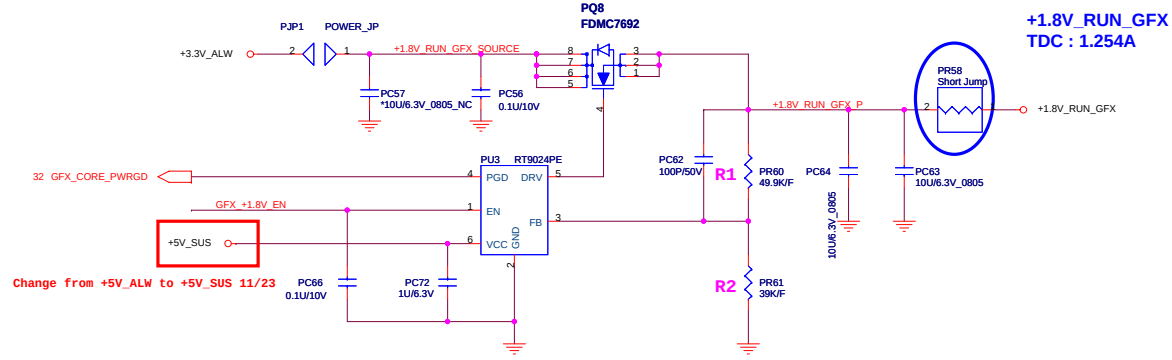
For Park-XT:

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
LOW	HIGH	1.07V(N/A)
HIGH	HIGH	1.12V

Chagne List:

For Park-XT:	For M96-LP:
PR151:52.3K	PR151:90.9K
PN:CS35232FB10	PN:CS39092FB11
PR79:196K	PR79:133K
PN:CS41962FB01	PN:CS41332FB06





Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	VGA power	1A

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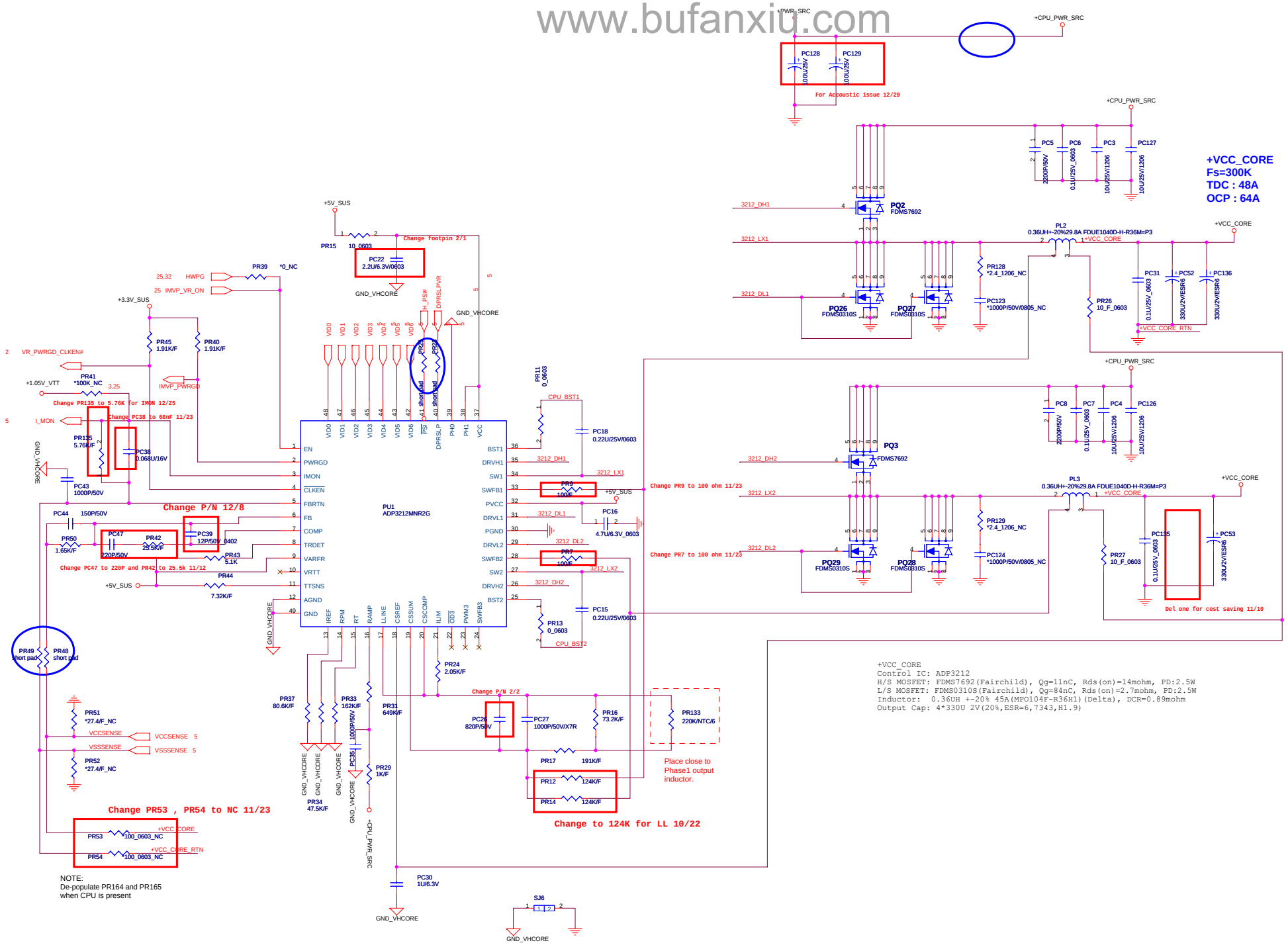

Quanta Computer Inc.			
PROJECT : UM8B DIS			
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	CPU_CORE		1A
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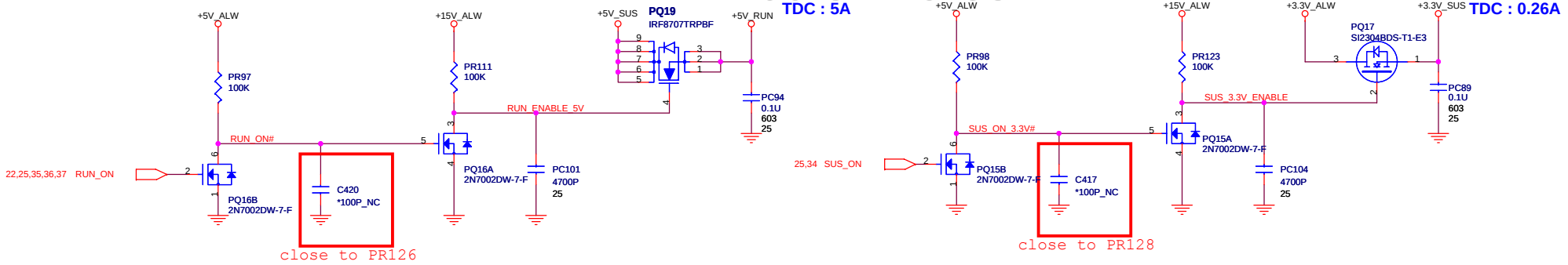
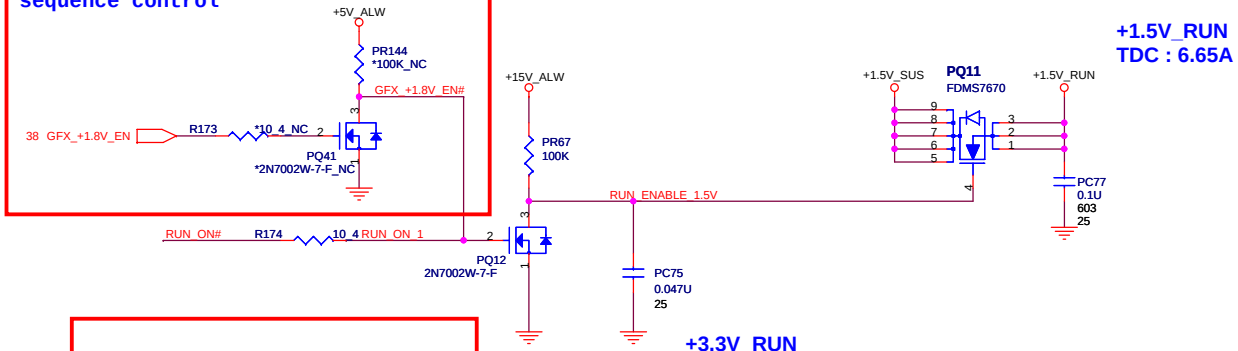
+5V_RUN
TDC : 5A

+3.3V_SUS
TDC : 0.26A

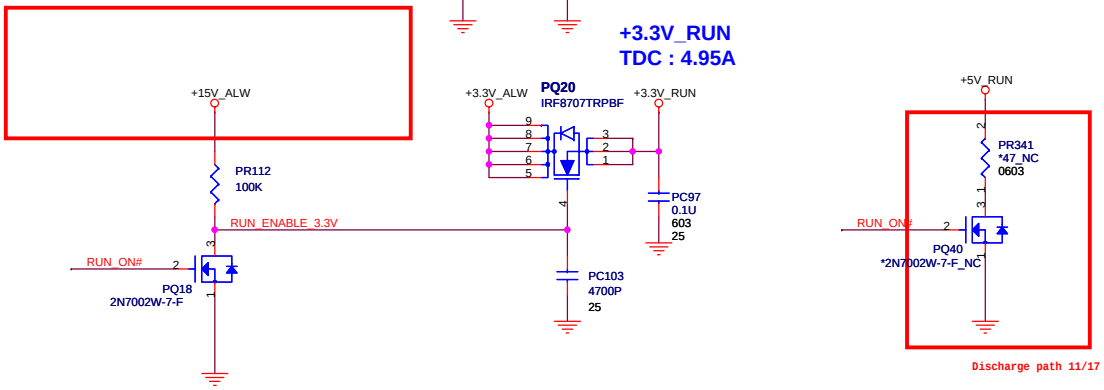


EE add this portion for power sequence control

+1.5V_RUN
TDC : 6.65A



+3.3V_RUN
TDC : 4.95A



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Size	Document Number	Rev
	Run Power Switch	1A
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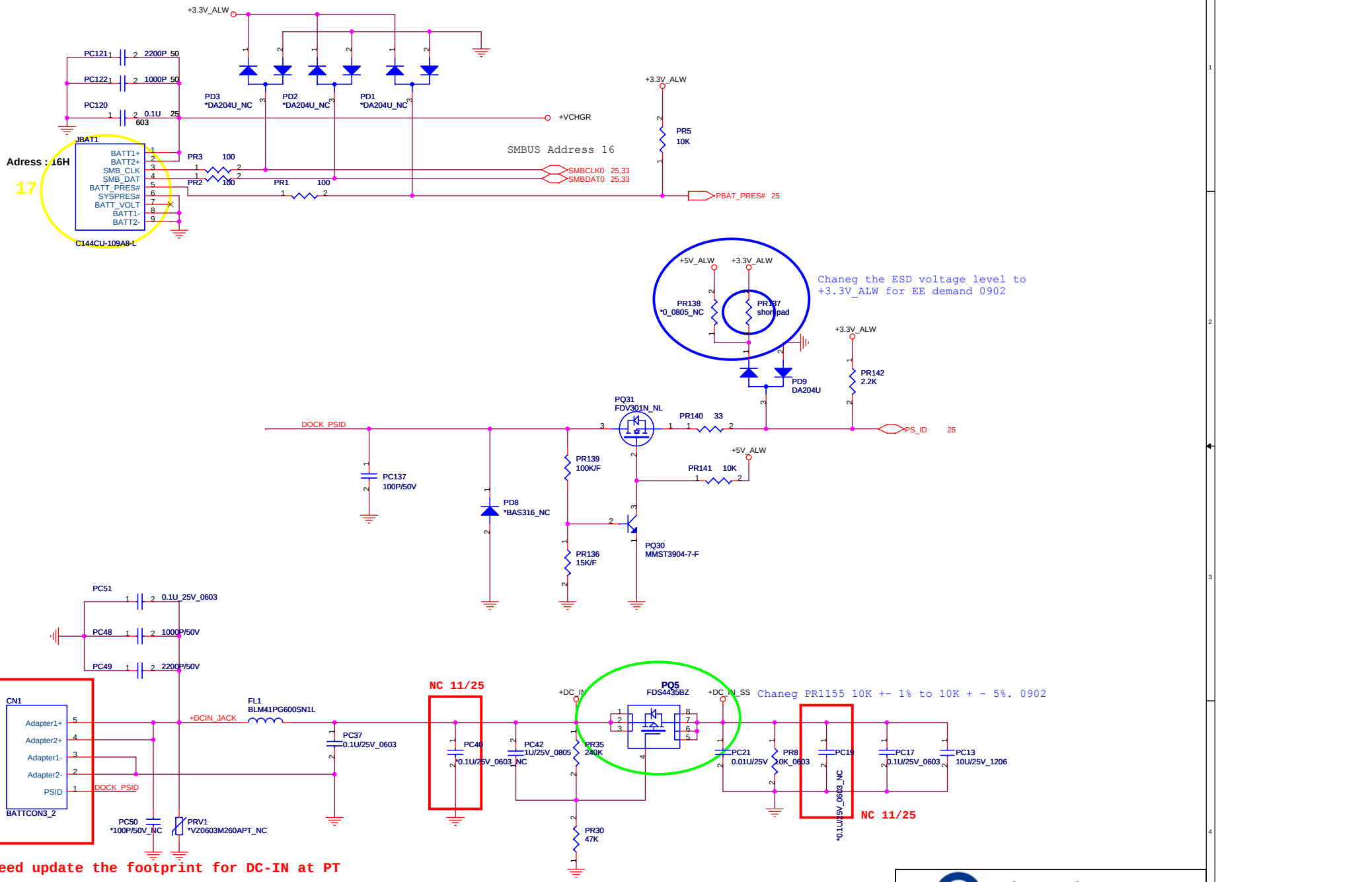

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Size	Document Number	Rev
	Batt & DC-IN	1A

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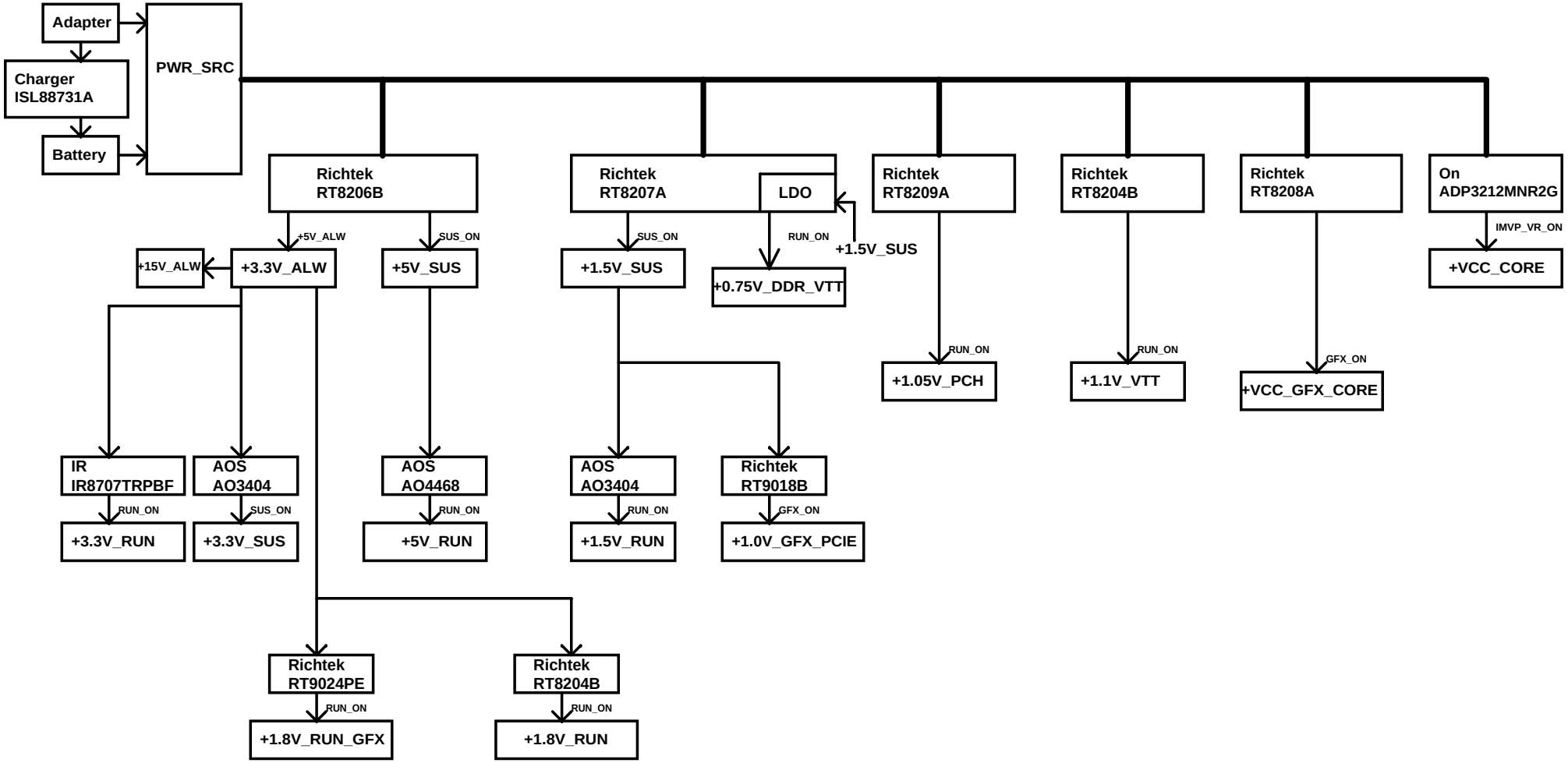
VER : 1A



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PROJECT : UM8B DIS

Size	Document Number	Rev
	Schematic Block Diagram1	1A
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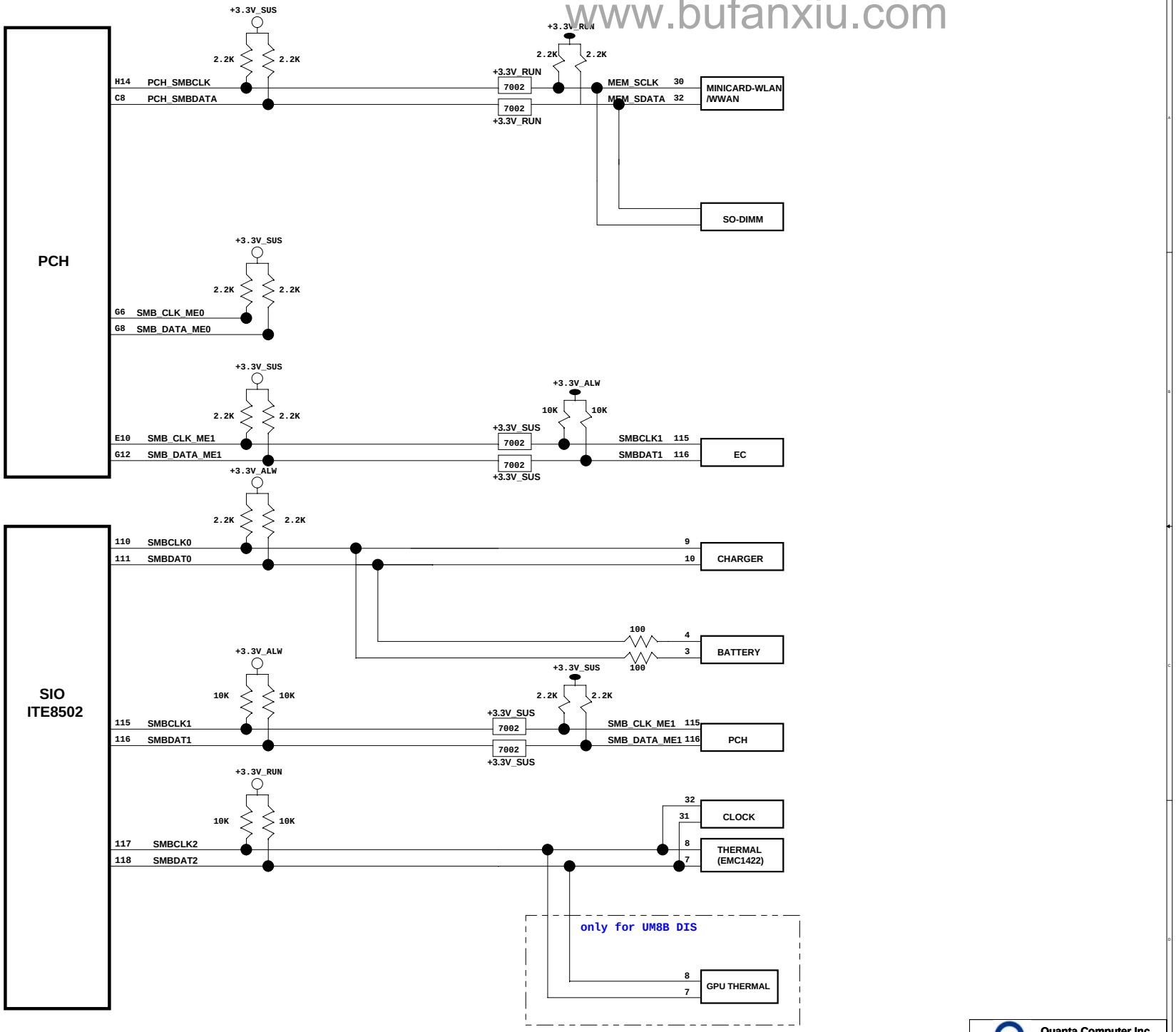

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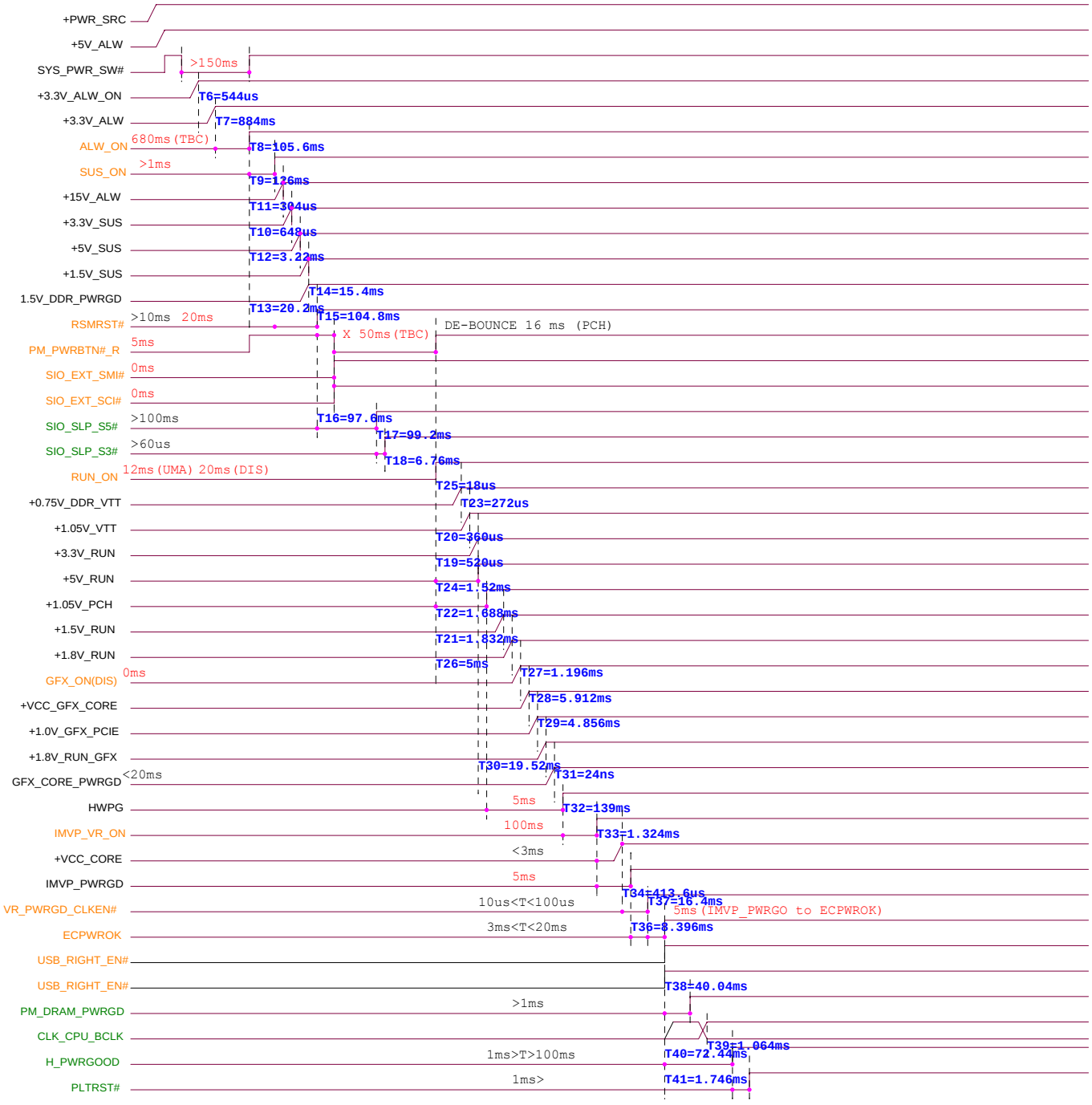
UM8B_ X00 Power On Timing(BATTERY MODE BY SOFTWARE SETUP, W/O ADAPTOR)



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Size	Document Number: POWER SEQUENCE	Rev 1A
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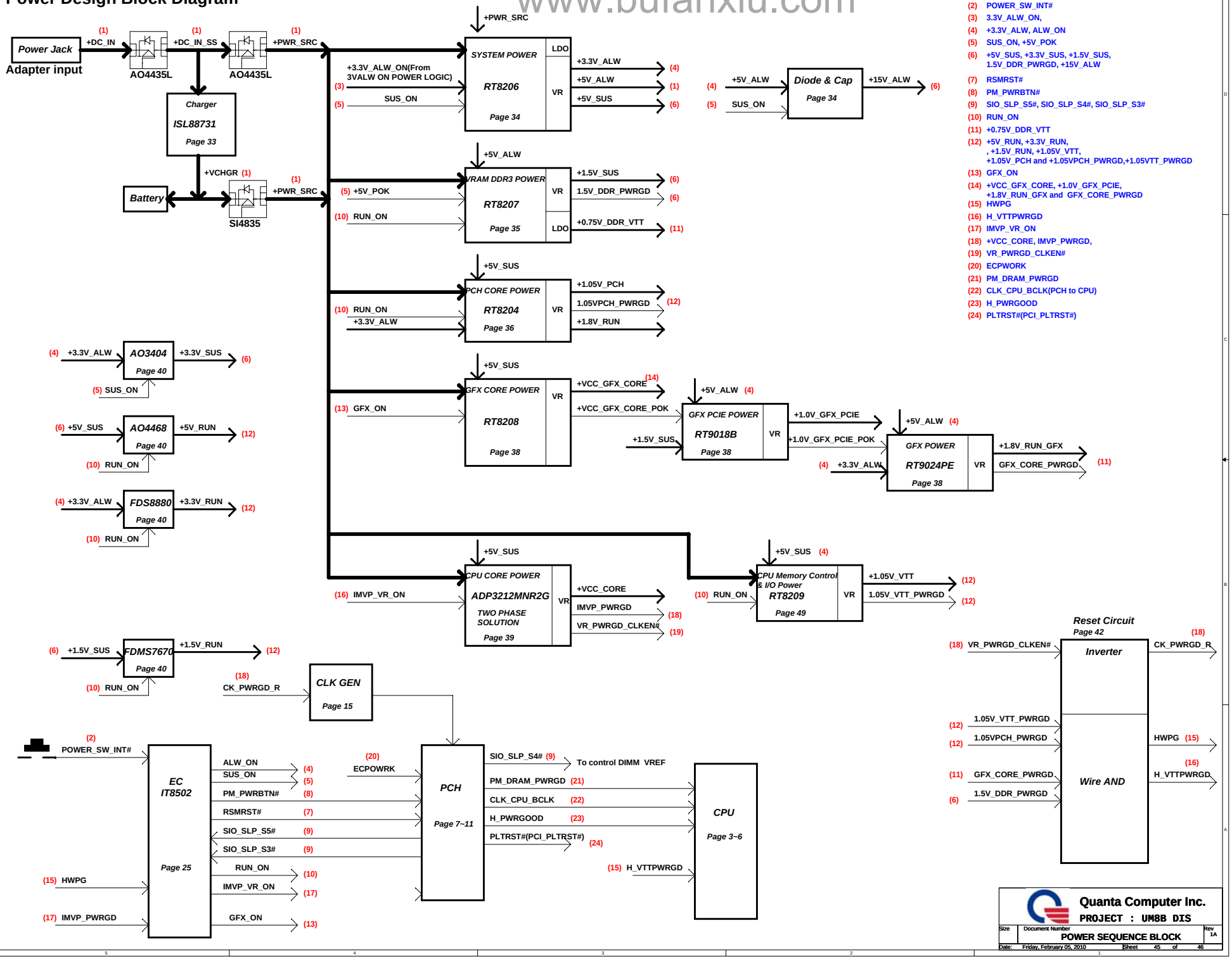
Power Design Block Diagram



(1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC,+5V_ALW
(2) POWER_SW_INT#
(3) 3.3V_ALW_ON,
(4) +3.3V_ALW, ALW_ON
(5) SUS_ON, +5V_POK
(6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD, +15V_ALW
(7) RSMRST#
(8) PM_PWRBTN#
(9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
(10) RUN_ON
(11) +0.75V_DDR_VTT
(12) +5V_RUN, +3.3V_RUN, , +1.5V_RUN, +1.05V_VTT, +1.05V_PCH and +1.05VPCH_PWRGD,+1.05VTT_PWRGD
(13) GFX_ON
(14) +VCC_GFX_CORE, +1.0V_GFX_PCIE, +1.8V_RUN_GFX and GFX_CORE_PWRGD
(15) HWPG
(16) H_VTTPWRGD
(17) IMVP_VR_ON
(18) +VCC_CORE, IMVP_PWRGD,
(19) VR_PWRGD_CLKEN#
(20) ECPWORK
(21) PM_DRAM_PWRGD
(22) CLK_CPU_BCLK(PCH to CPU)
(23) H_PWRGOOD
(24) PLTRST#(PCI_PLTRST#)

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	POWER SEQUENCE BLOCK		1A
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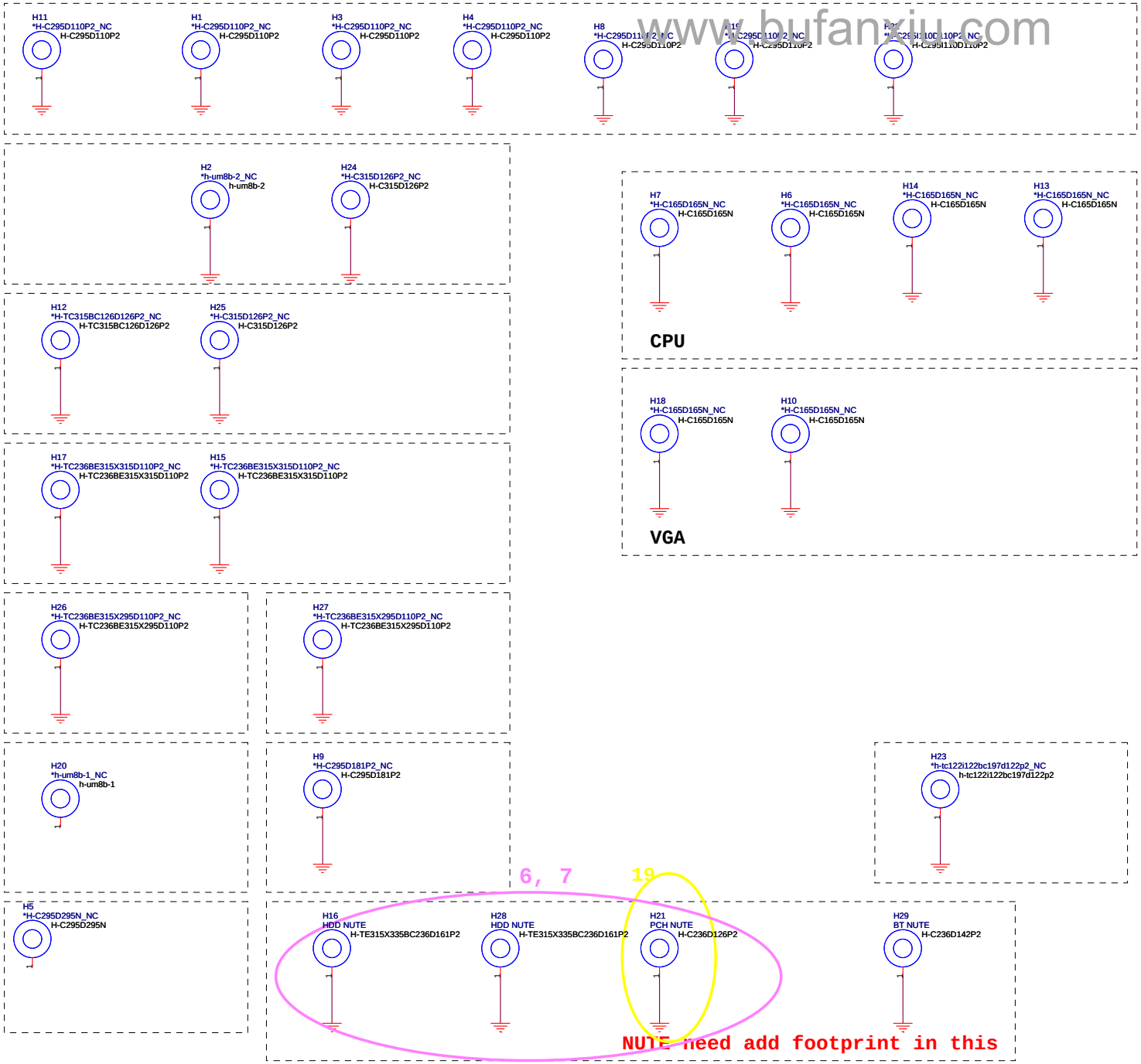

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PROJECT : UM8B DIS		
Size	Document Number	Rev
	PAD&SCREW	1A
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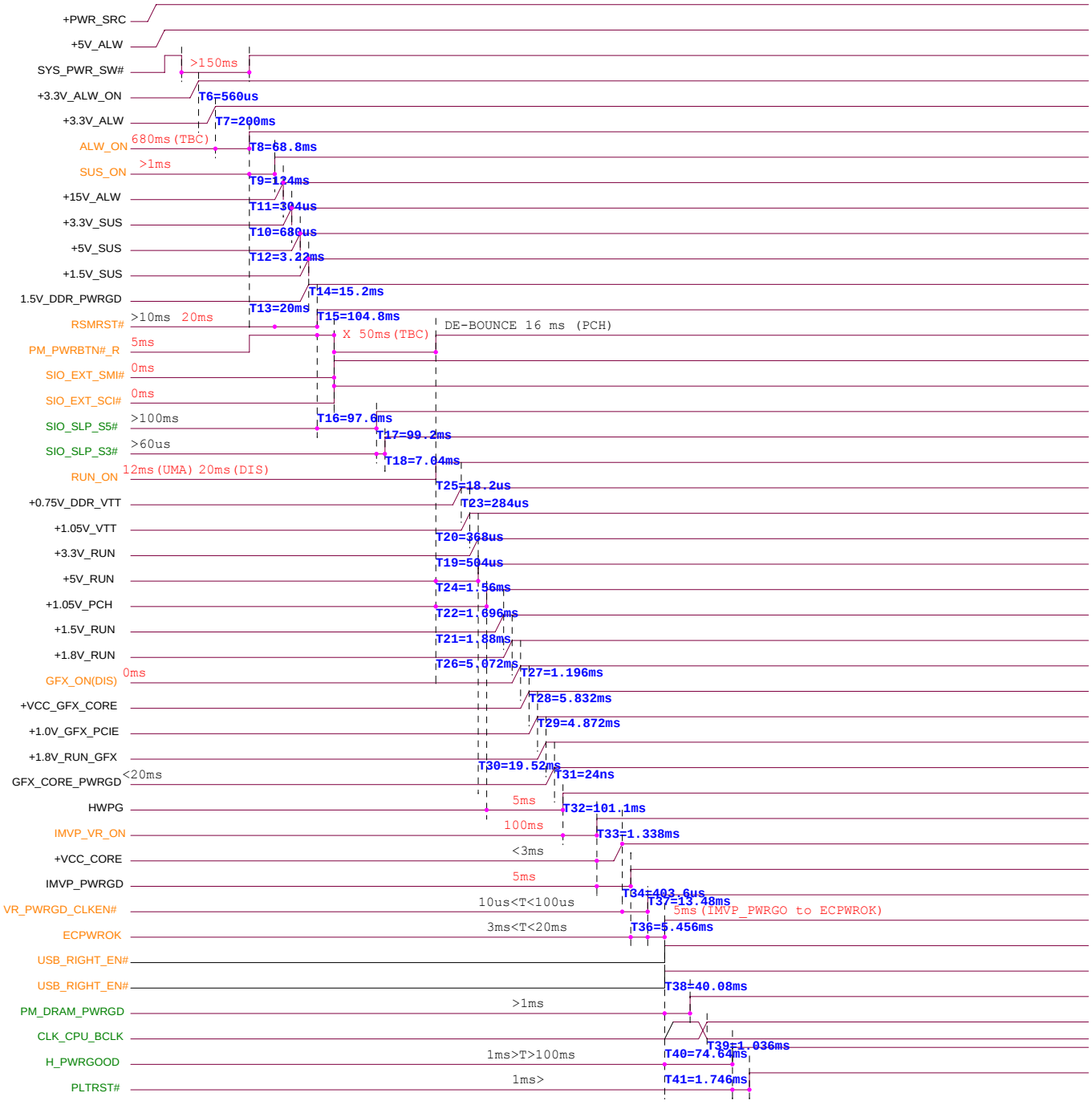
UM8B_ X00 Power On Timing(BATTERY MODE BY SOFTWARE SETUP, W/O ADAPTOR)



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PROJECT : UM8 UMA

Size	Document Number	Rev
	POWER SEQUENCE	1A

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