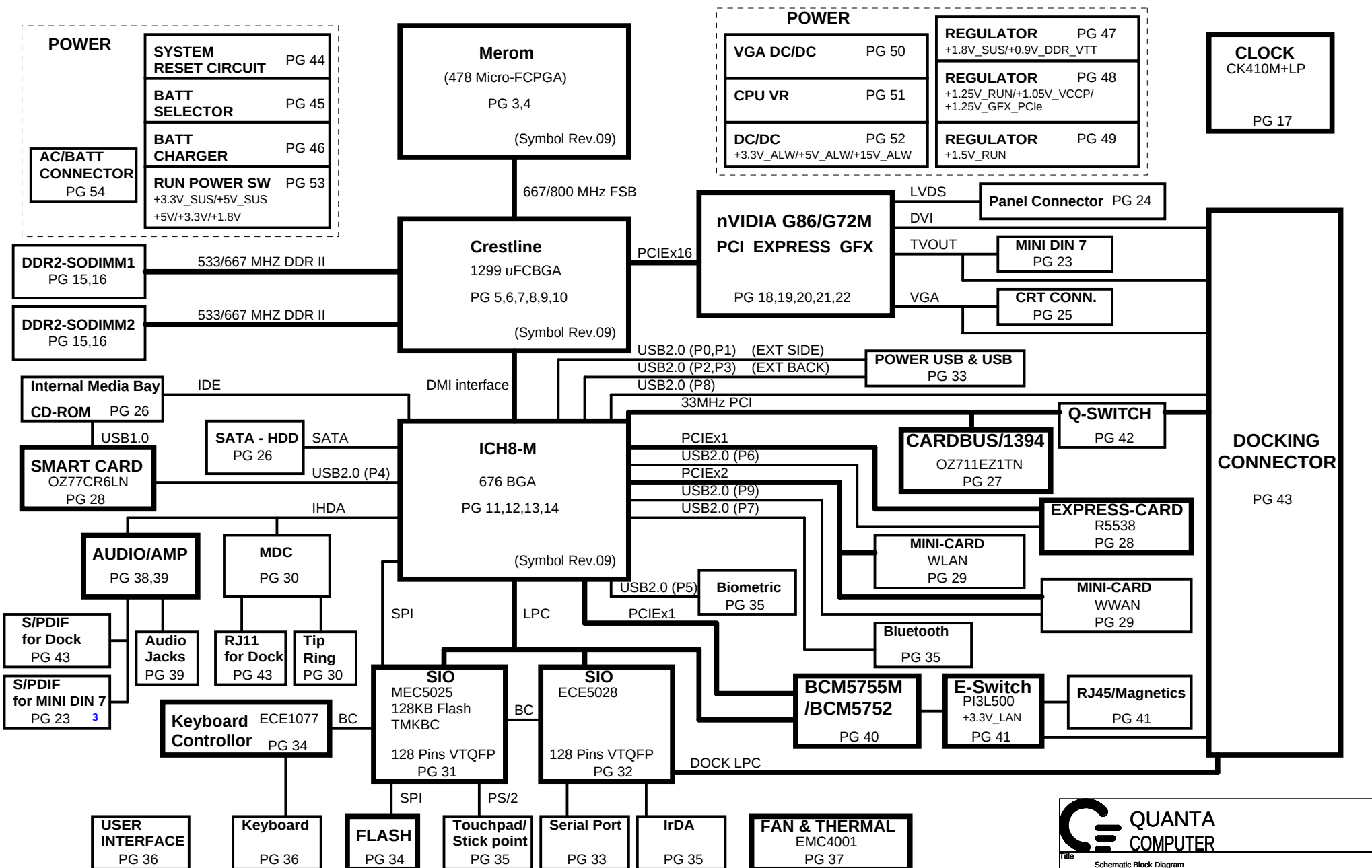


JM7B-DISCRETE

PWA FP382, PWB UW445,
SCHEM PM333. (128MB)
VER : 2B

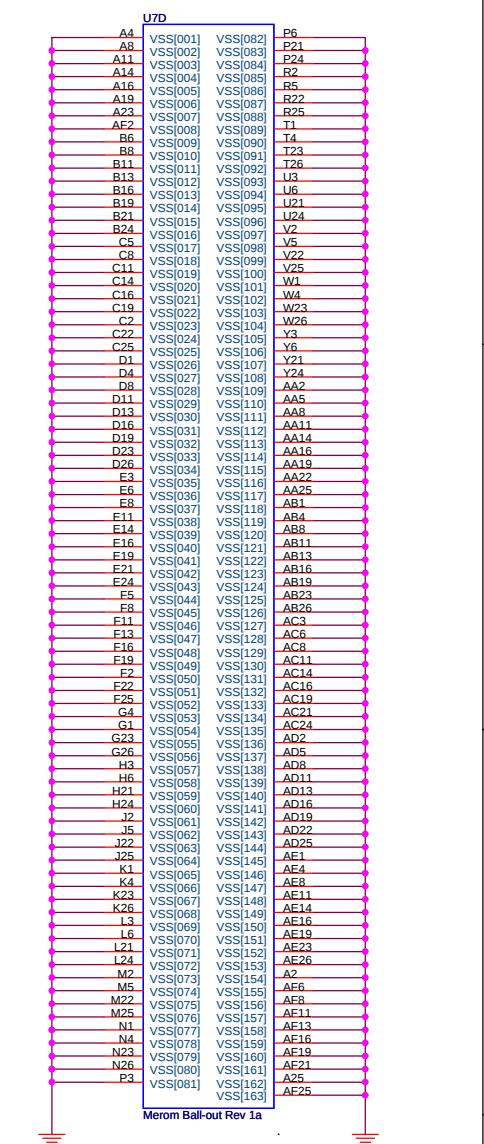
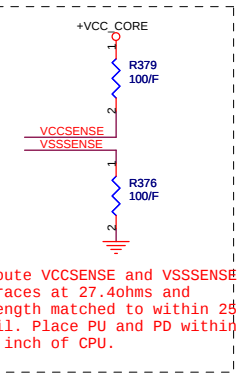
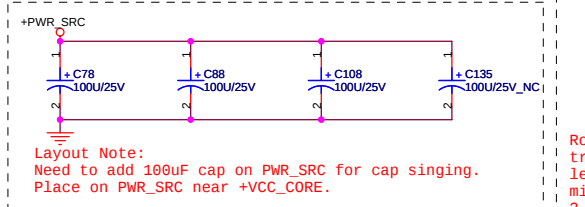
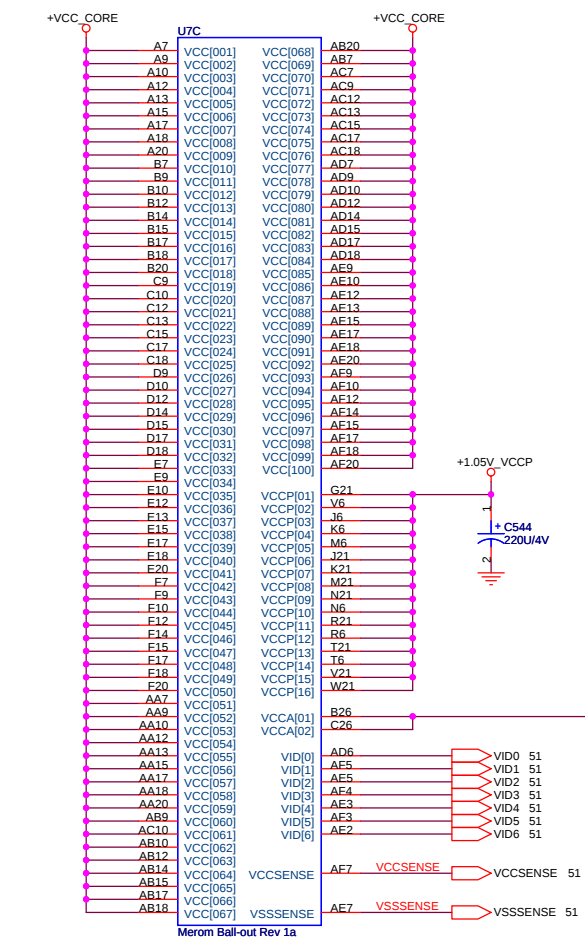
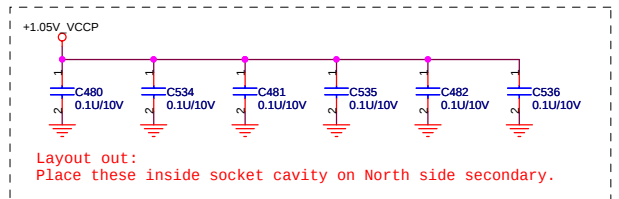
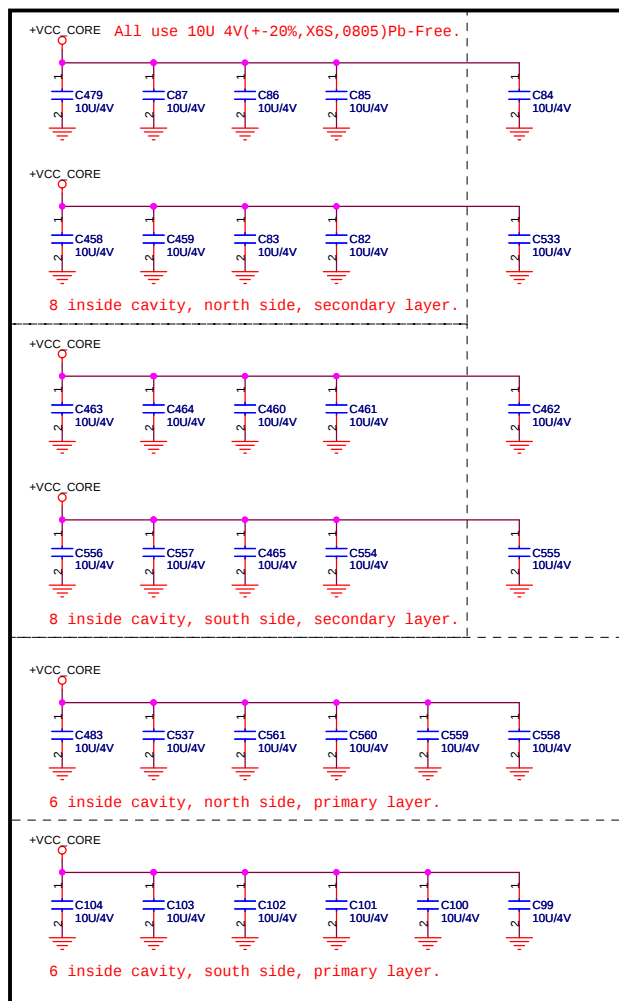


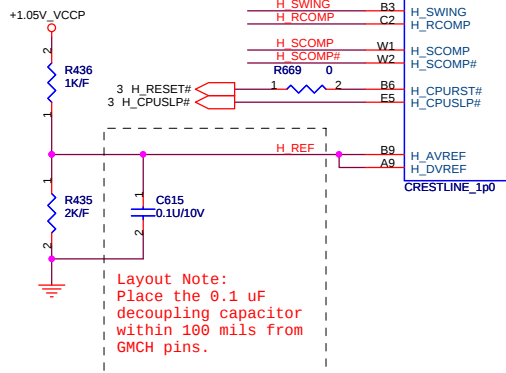
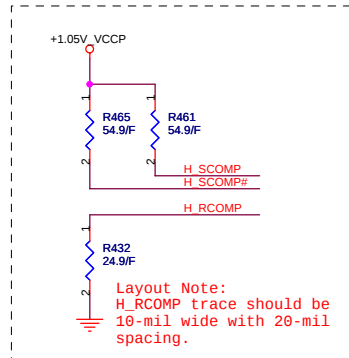
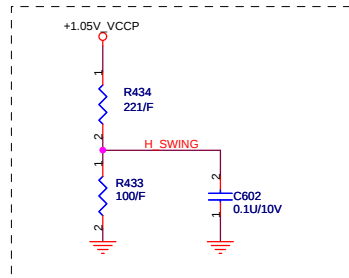
INDEX

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50	CPU_MAX8786(3phase)
51	D/D Power
52	RUN Power Switch
53	DCIN,Batt
54	PAD& SCREW
55	EMI CAP
56	SMBUS BLOCK

Power States

Power Rail	Control Signal	S0/M0	S3/M1	S3/M1	S4/M1	S3/M-off	S4/M-off	S5/M-off
+3.3V_ALW								
+5V_ALW								
+3.3V_LAN								
+1.25V_SRC_M								
+1.05V_M								
+1.8V_SUS								
+0.9V_DDR_VTT								
+5V_SUS								
+3.3V_SUS								
+5V_RUN								
+3.3V_RUN								
+1.8V_RUN								
+1.25V_RUN								
+1.5V_RUN								
+1.05V_VCCP								
VCC_VCRE								
+LCDVCC								
+5V_MOD								
+VCC_GFX_CORE								
+1.25V_GFX_PCle								
+2.5V_RUN								





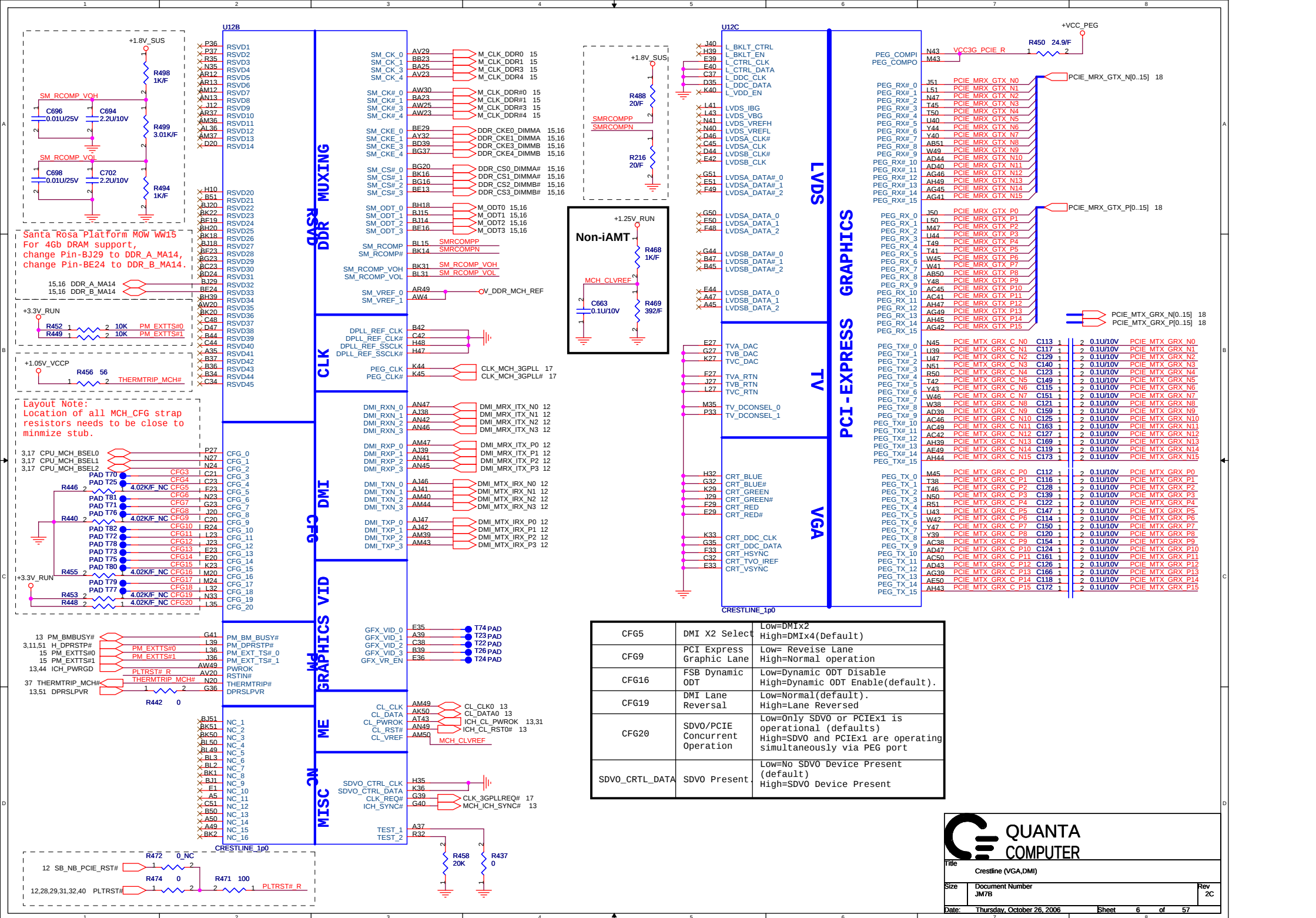
H_D#0	E2	H_D#_0
H_D#1	G2	H_D#_1
H_D#2	G7	H_D#_2
H_D#3	M6	H_D#_3
H_D#4	H7	H_D#_4
H_D#5	H3	H_D#_5
H_D#6	G4	H_D#_6
H_D#7	F3	H_D#_7
H_D#8	N8	H_D#_8
H_D#9	H2	H_D#_9
H_D#10	M10	H_D#_10
H_D#11	N12	H_D#_11
H_D#12	N9	H_D#_12
H_D#13	H5	H_D#_13
H_D#14	P13	H_D#_14
H_D#15	K9	H_D#_15
H_D#16	M2	H_D#_16
H_D#17	W10	H_D#_17
H_D#18	V4	H_D#_18
H_D#19	V4	H_D#_19
H_D#20	M3	H_D#_20
H_D#21	J1	H_D#_21
H_D#22	N5	H_D#_22
H_D#23	N3	H_D#_23
H_D#24	W6	H_D#_24
H_D#25	W9	H_D#_25
H_D#26	N2	H_D#_26
H_D#27	Y7	H_D#_27
H_D#28	Y9	H_D#_28
H_D#29	P4	H_D#_29
H_D#30	W3	H_D#_30
H_D#31	N1	H_D#_31
H_D#32	AD12	H_D#_32
H_D#33	AE3	H_D#_33
H_D#34	AD8	H_D#_34
H_D#35	AC3	H_D#_35
H_D#36	AC7	H_D#_36
H_D#37	AC14	H_D#_37
H_D#38	AD11	H_D#_38
H_D#39	AC11	H_D#_39
H_D#40	AE2	H_D#_40
H_D#41	AD7	H_D#_41
H_D#42	AB1	H_D#_42
H_D#43	Y3	H_D#_43
H_D#44	AC6	H_D#_44
H_D#45	AE2	H_D#_45
H_D#46	AC5	H_D#_46
H_D#47	AG3	H_D#_47
H_D#48	A39	H_D#_48
H_D#49	AH8	H_D#_49
H_D#50	AJ14	H_D#_50
H_D#51	AE9	H_D#_51
H_D#52	AE11	H_D#_52
H_D#53	AH12	H_D#_53
H_D#54	AJ5	H_D#_54
H_D#55	AH5	H_D#_55
H_D#56	AJ6	H_D#_56
H_D#57	AE7	H_D#_57
H_D#58	AJ7	H_D#_58
H_D#59	AJ2	H_D#_59
H_D#60	AE5	H_D#_60
H_D#61	AJ3	H_D#_61
H_D#62	AH2	H_D#_62
H_D#63	AH13	H_D#_63

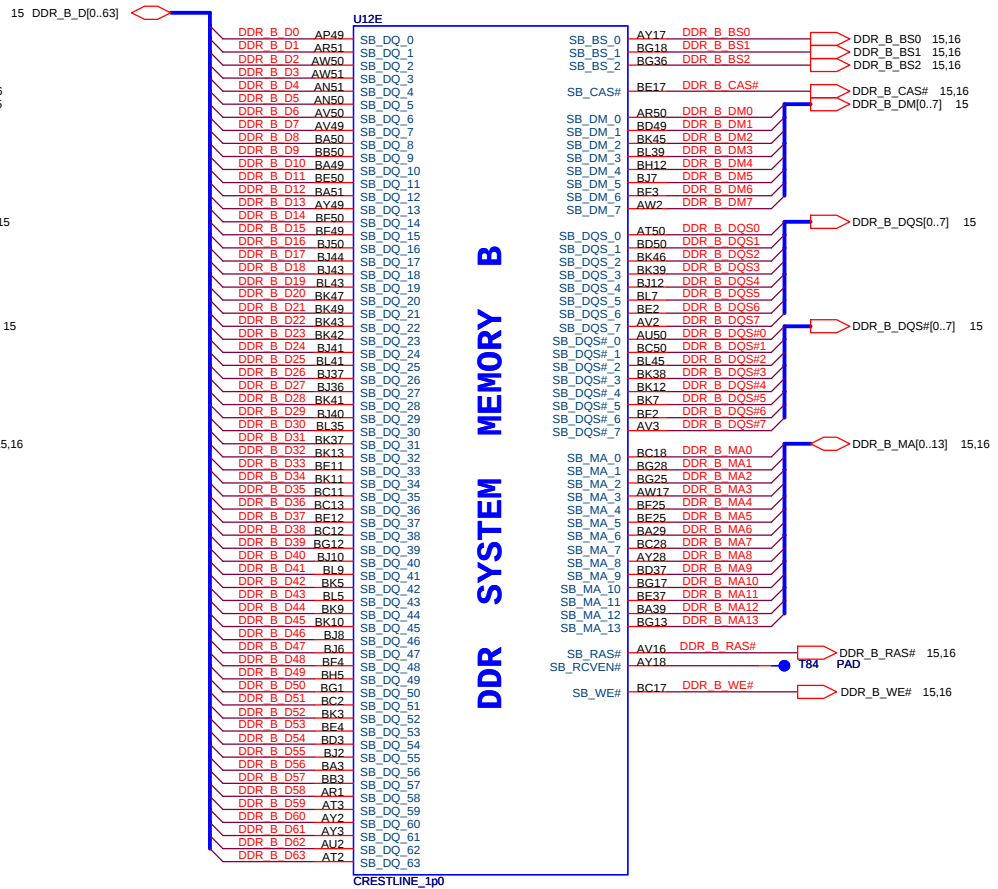
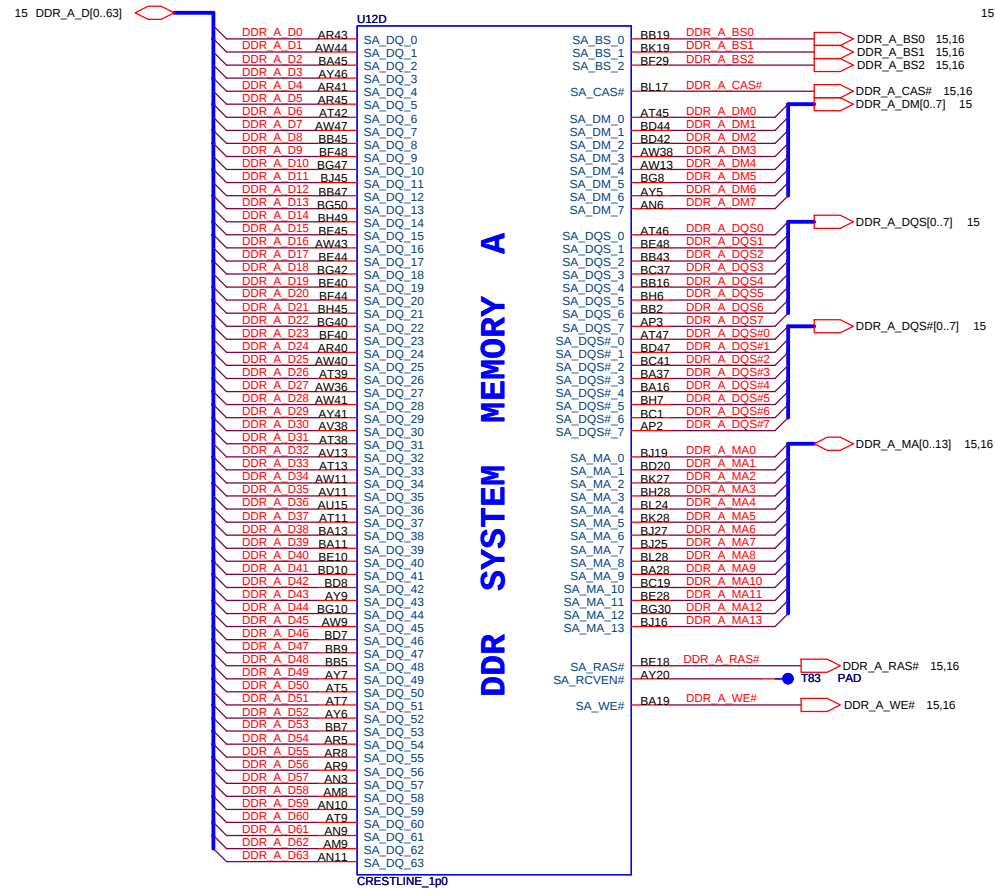
HOST

H_A#_3	J13	H_A#3
H_A#_4	B11	H_A#4
H_A#_5	C11	H_A#5
H_A#_6	M11	H_A#6
H_A#_7	C15	H_A#7
H_A#_8	F16	H_A#8
H_A#_9	L13	H_A#9
H_A#_10	G17	H_A#10
H_A#_11	C14	H_A#11
H_A#_12	K16	H_A#12
H_A#_13	B13	H_A#13
H_A#_14	L16	H_A#14
H_A#_15	J17	H_A#15
H_A#_16	B14	H_A#16
H_A#_17	K19	H_A#17
H_A#_18	P15	H_A#18
H_A#_19	R17	H_A#19
H_A#_20	B16	H_A#20
H_A#_21	J20	H_A#21
H_A#_22	L19	H_A#22
H_A#_23	D17	H_A#23
H_A#_24	M17	H_A#24
H_A#_25	N16	H_A#25
H_A#_26	J19	H_A#26
H_A#_27	B18	H_A#27
H_A#_28	E19	H_A#28
H_A#_29	B17	H_A#29
H_A#_30	B15	H_A#30
H_A#_31	E17	H_A#31
H_A#_32	C18	H_A#32
H_A#_33	A19	H_A#33
H_A#_34	B19	H_A#34
H_A#_35	N19	H_A#35
H_ADS#_0	G12	H_ADS#_0
H_ADS#_1	A17	H_ADS#_1
H_ADSTB#_0	G20	H_ADSTB#_0
H_ADSTB#_1	C8	H_ADSTB#_1
H_BNR#_0	E8	H_BNR#_0
H_BPRI#_0	F12	H_BPRI#_0
H_BREQ#_0	D6	H_BREQ#_0
H_DEFER#_0	C10	H_DEFER#_0
H_DBSY#_0	AM5	H_DBSY#_0
HPLL_CLK#_0	AM7	HPLL_CLK#_0
H_DPWR#_0	H8	H_DPWR#_0
H_DRDY#_0	K7	H_DRDY#_0
H_HIT#_0	E4	H_HIT#_0
H_HITM#_0	C6	H_HITM#_0
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H_TRDY#_0	B7	H_TRDY#_0
H_DINV#_0	K5	H_DINV#_0
H_DINV#_1	L2	H_DINV#_1
H_DINV#_2	AD13	H_DINV#_2
H_DINV#_3	AE13	H_DINV#_3
H_DSTBN#_0	J7	H_DSTBN#_0
H_DSTBN#_1	K3	H_DSTBN#_1
H_DSTBN#_2	AD2	H_DSTBN#_2
H_DSTBN#_3	AH11	H_DSTBN#_3
H_DSTBP#_0	L7	H_DSTBP#_0
H_DSTBP#_1	K2	H_DSTBP#_1
H_DSTBP#_2	AC2	H_DSTBP#_2
H_DSTBP#_3	AJ10	H_DSTBP#_3
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H_REQ#_2	A11	H_REQ#_2
H_REQ#_3	H13	H_REQ#_3
H_REQ#_4	B12	H_REQ#_4
H_RS#_0	E12	H_RS#_0
H_RS#_1	D7	H_RS#_1
H_RS#_2	D8	H_RS#_2

QUANTA
COMPUTER

Title Crestline (HOST)		
Size JM7B	Document Number	Rev 2C
Date: Thursday, October 26, 2006	Sheet 5	of 57







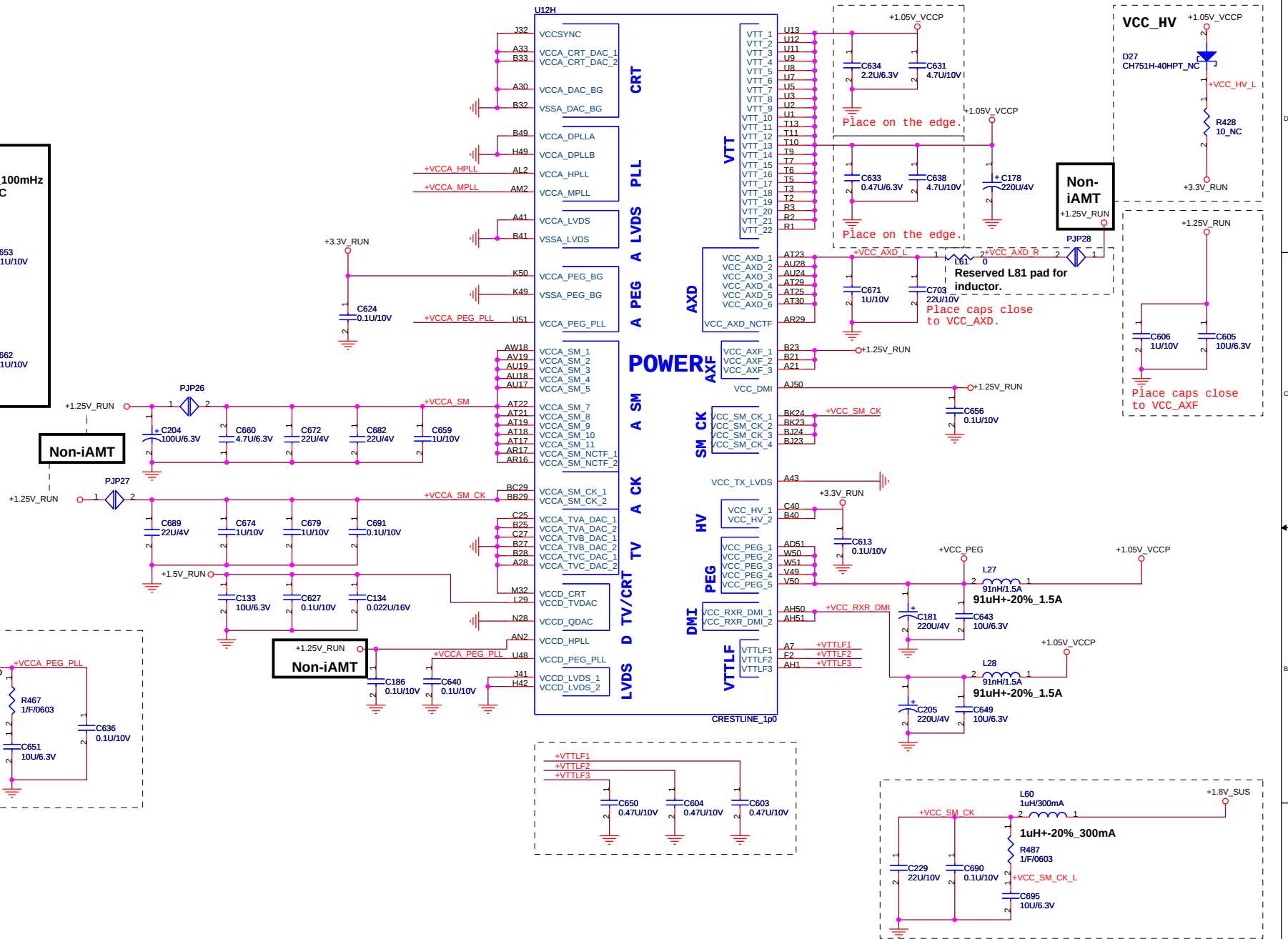
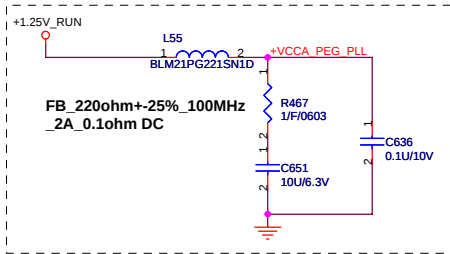
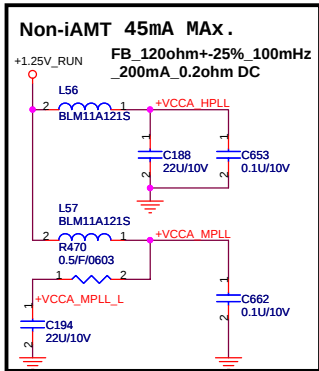
Title	Crestline (VCC,NCTF)
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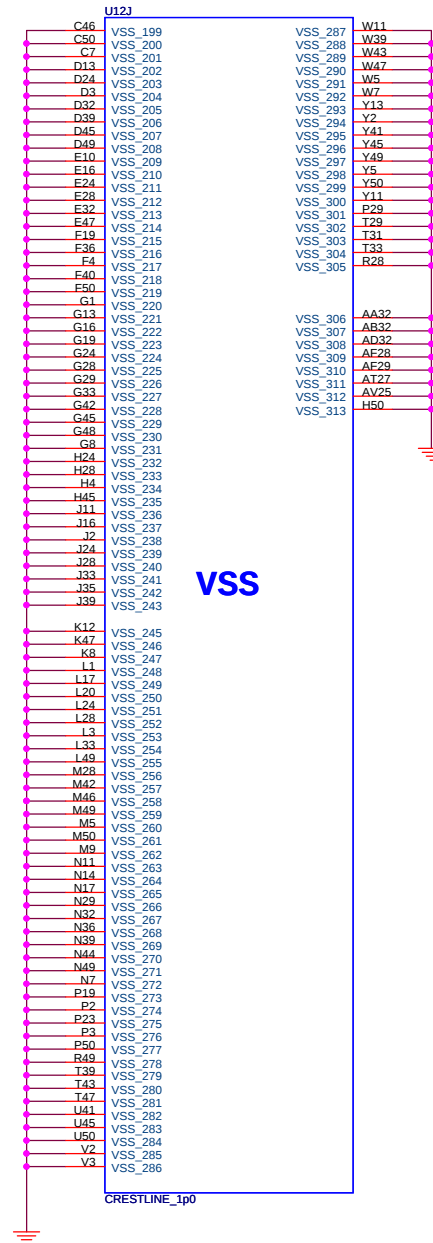
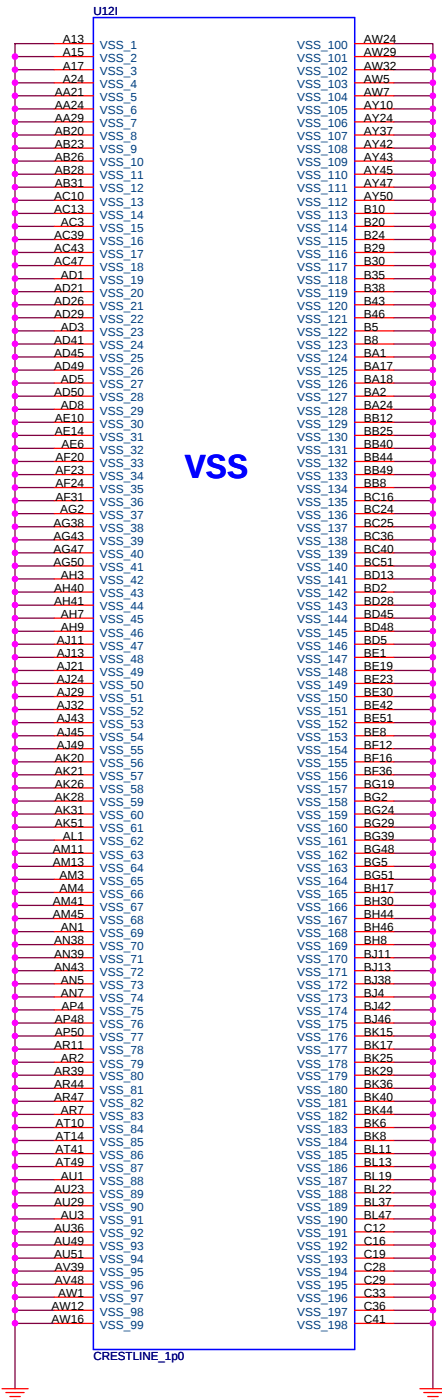
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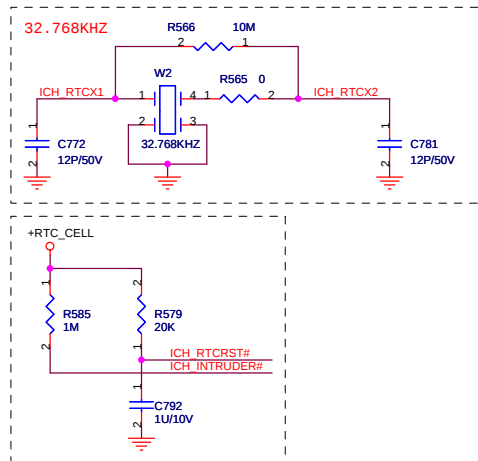
Document Number
JM7BRev
2C

Date: Friday, October 20, 2006

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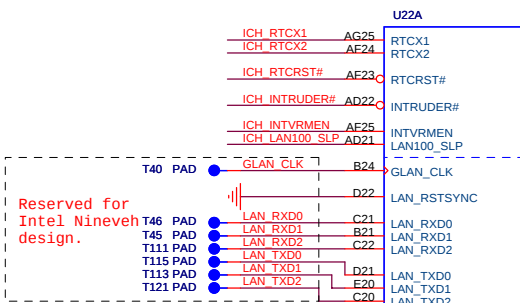




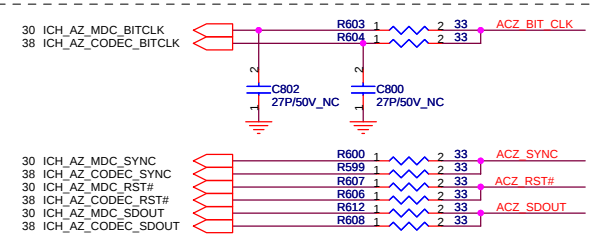
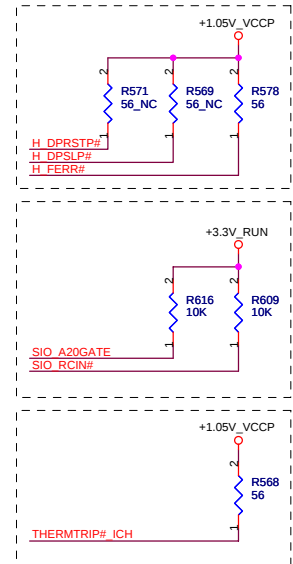
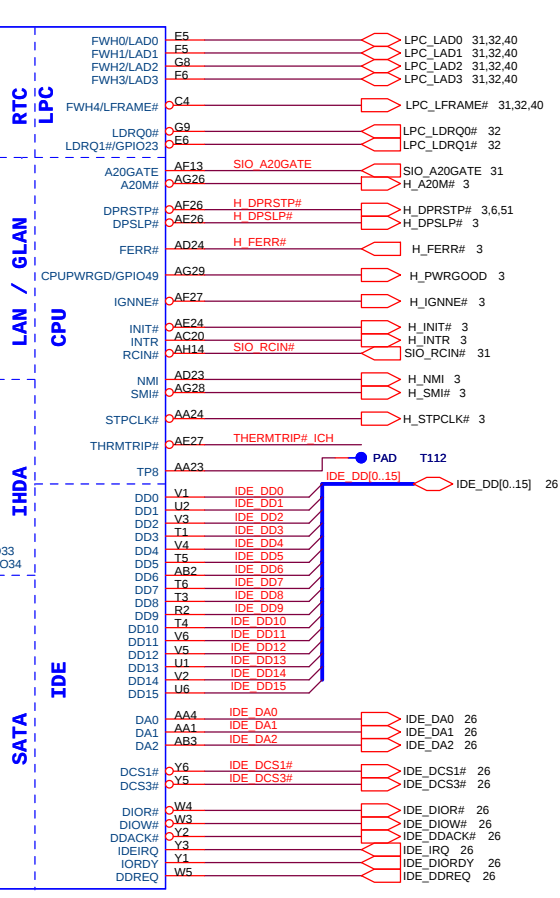
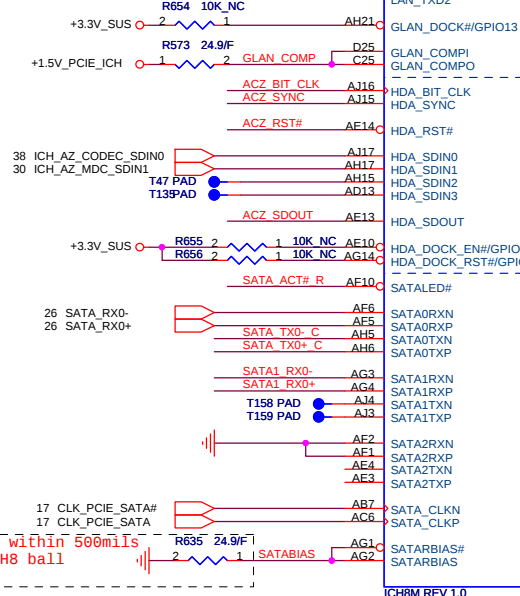


ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)		
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)	

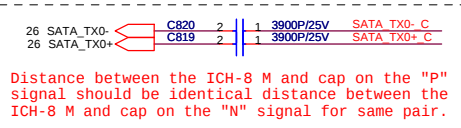
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)		
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)	



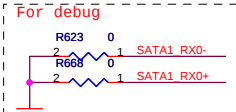
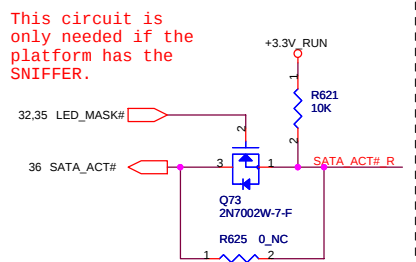
Reserved for
Intel Nineveh
design.



Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respectively. Basically, keep the same distance from T for all series termination resistors.

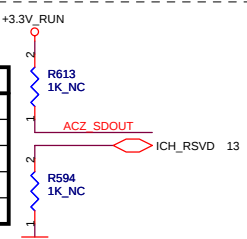


Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-8 M and cap on the "N" signal for same pair.



Place within 500mils
of ICH8 ball

XOR Chain Entrance Strap		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1



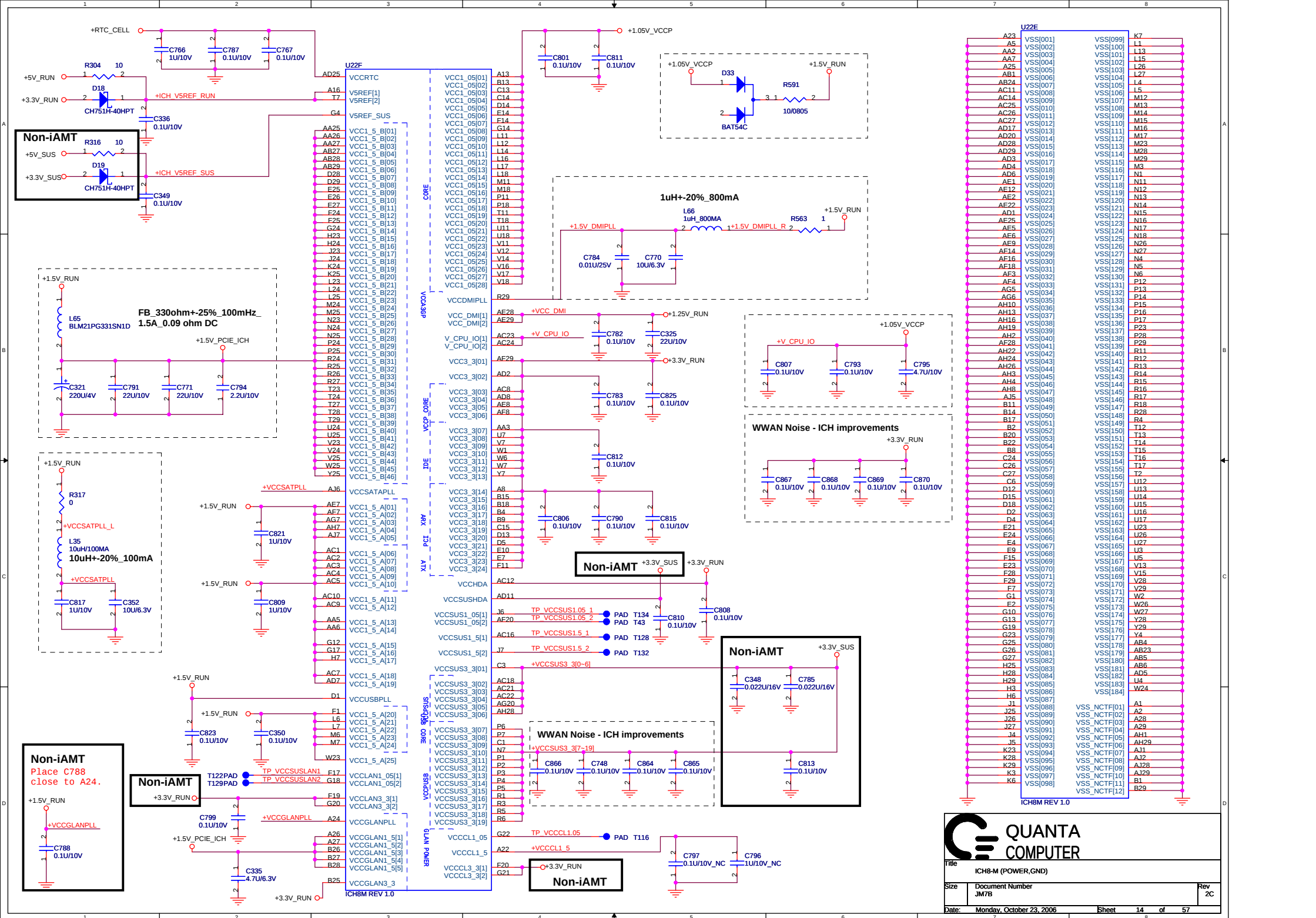
QUANTA
COMPUTER

Title: ICH8-M (CPU,IDE,SATA,LPC,AC97,LAN)

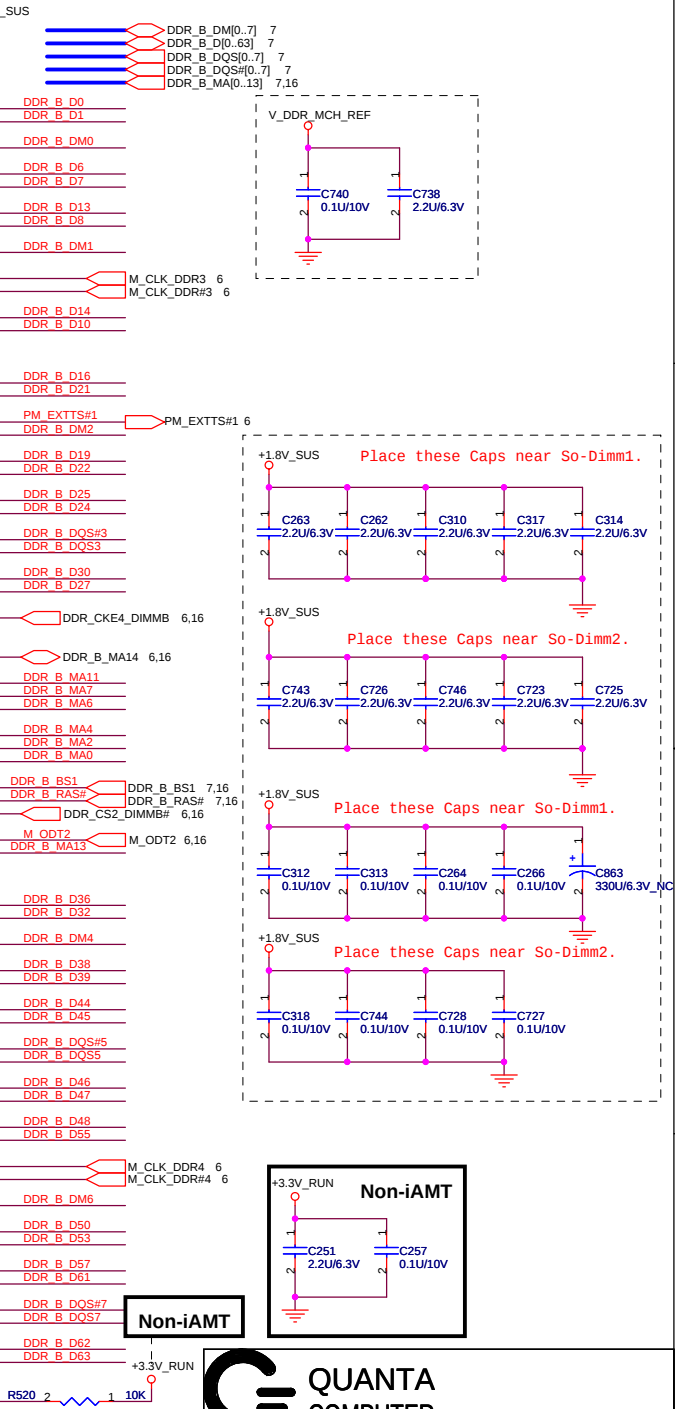
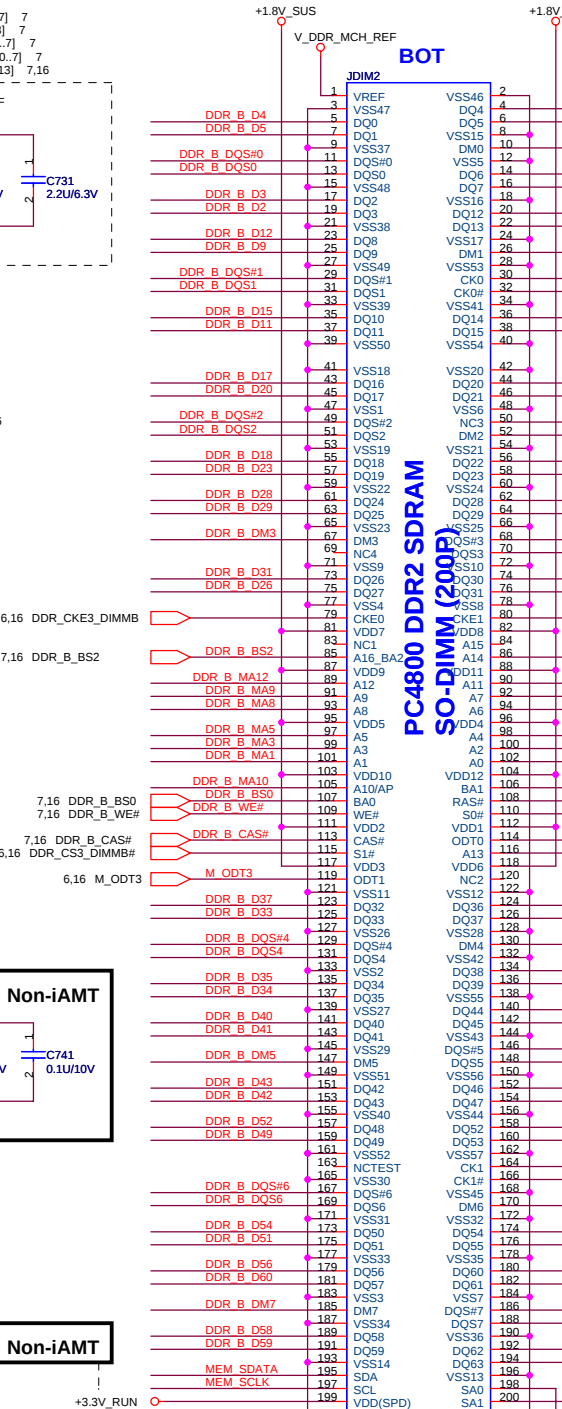
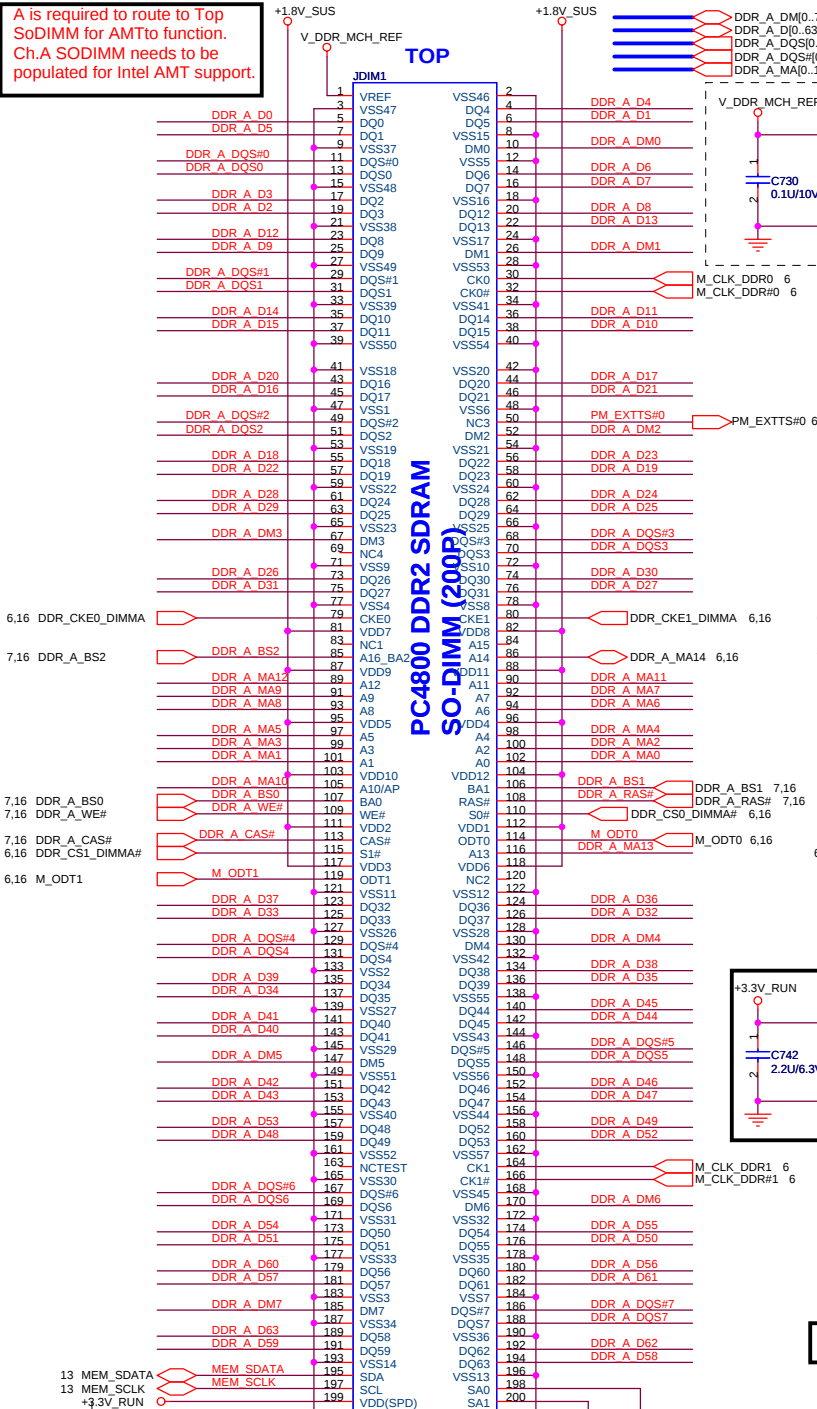
Size: Document Number JM7B Rev 2C

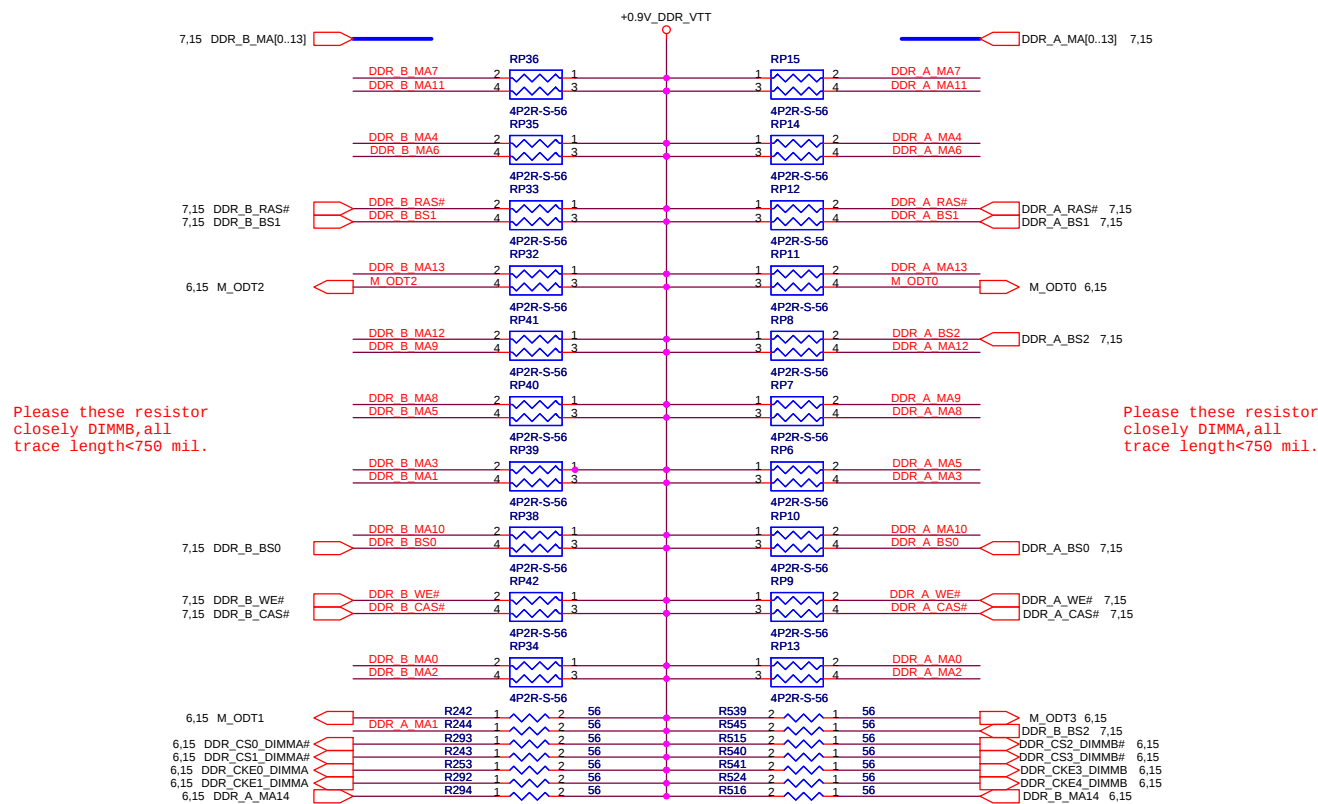
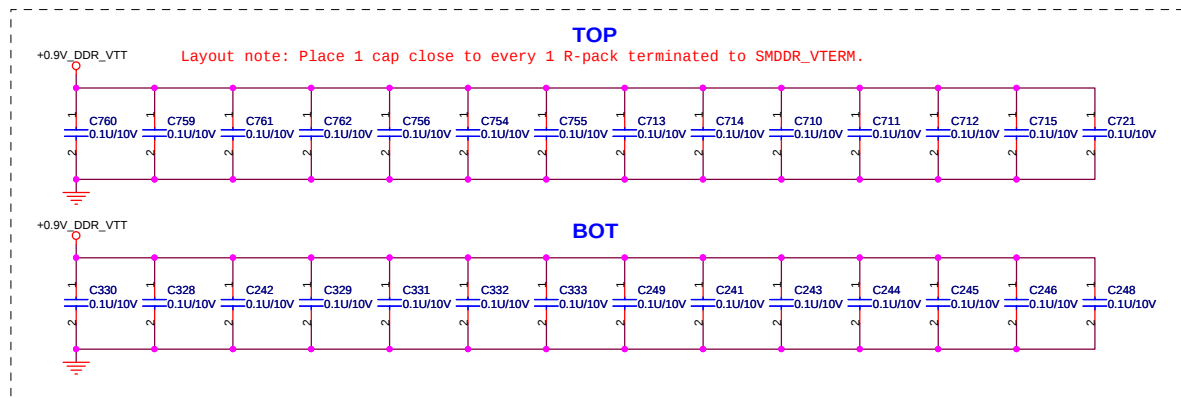
Date: Thursday, October 26, 2006 Sheet 11 of 57

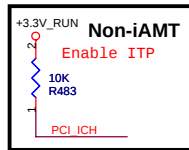
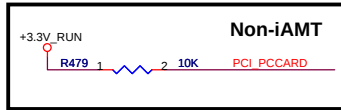
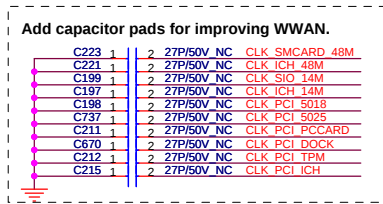
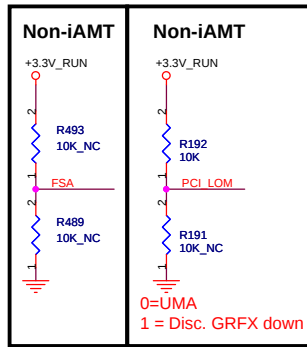




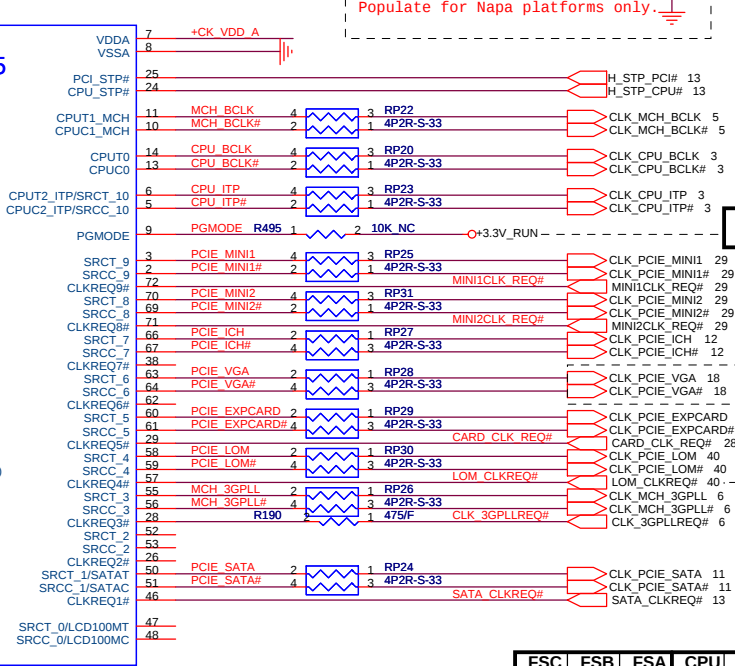
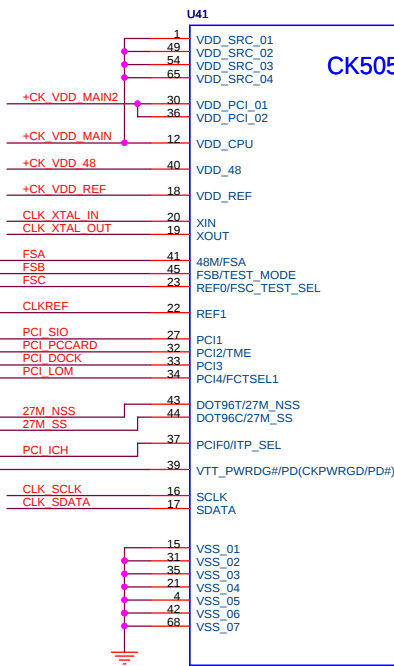
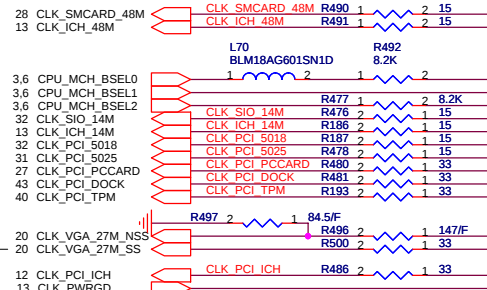
A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.







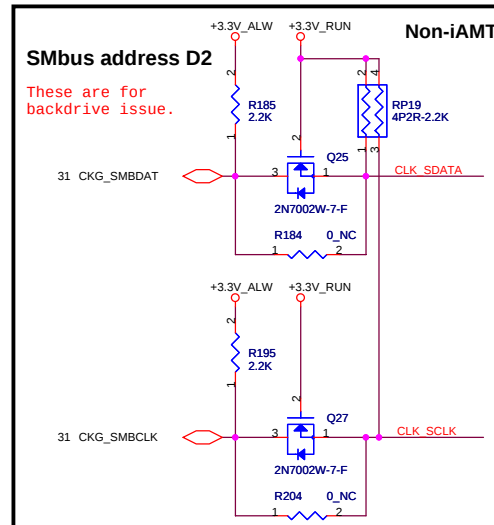
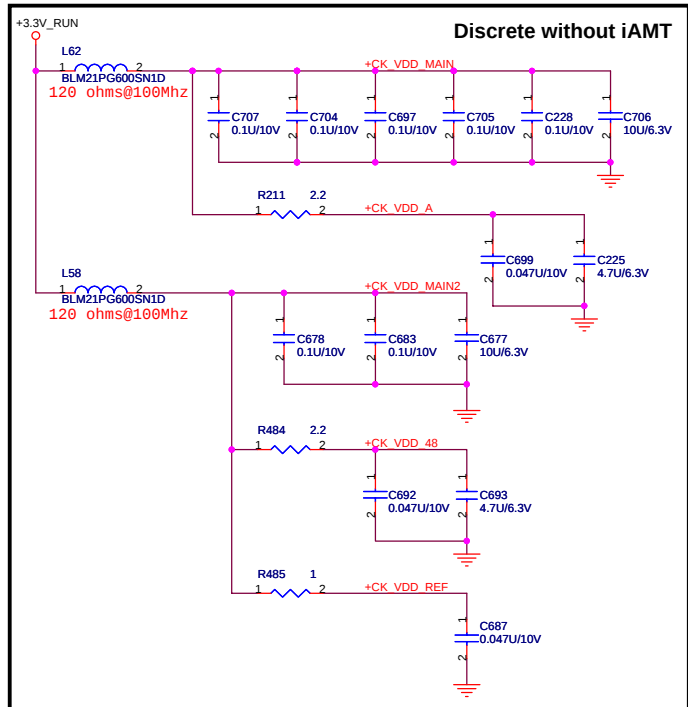
Change R496 to 147 ohm TBD and pop R497 84.5 ohm TBD pull down on R496 pin2. CLK_VGA_27M_NSS is max 1.2V.



Non-iAMT

Discrete

Broadcom



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI_LOM = FCTSEL1

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRCT0	SRCC0



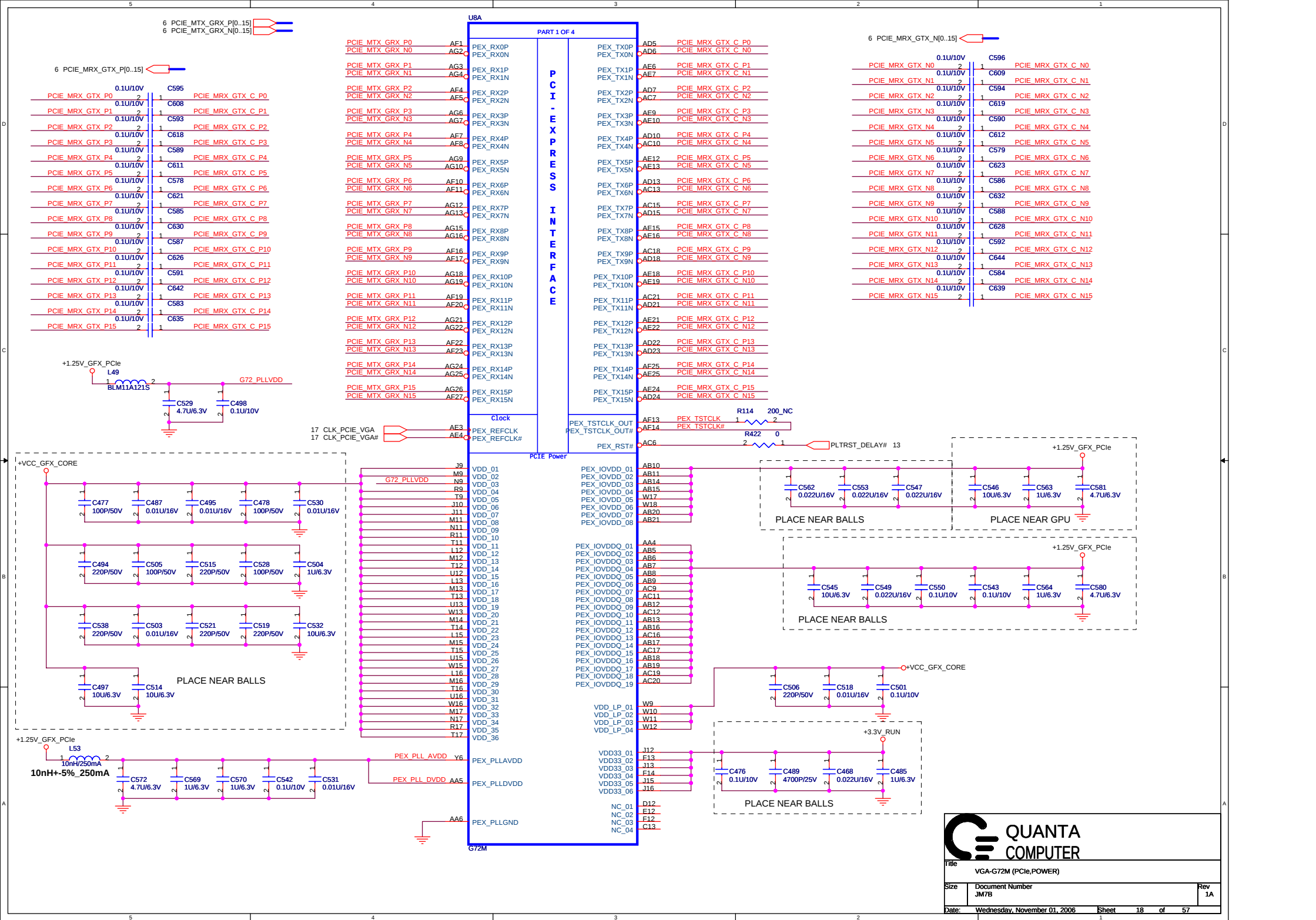
Title: CLOCK GENERATOR

Size: Document Number JM7B

Date: Wednesday, November 01, 2006

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Rev: 2C



256MB: Pop R89;
depop R90.
128MB: Pop R90;
depop R89.
No-pop R99 for
G72, pop resistor
for G86.

81

+2.5V_RUN L44
BLM11A121S
+1.25V_RUN
L45
BLM11A121S_NC
C456 2.2U/6.3V
C454 4700P/25V
C455 470P/50V
+2.5V_RUN for G72
+1.25V_RUN for G8x

hexainf@hotmail.com
GRATIS - FOR FREE

35
T59 PAD D11
20 I2CH_SCL C7
20 I2CH_SDA B7
AC8 RFU_GND

G72M

VIDEO & MULTIMEDIA

General Purpose I/O

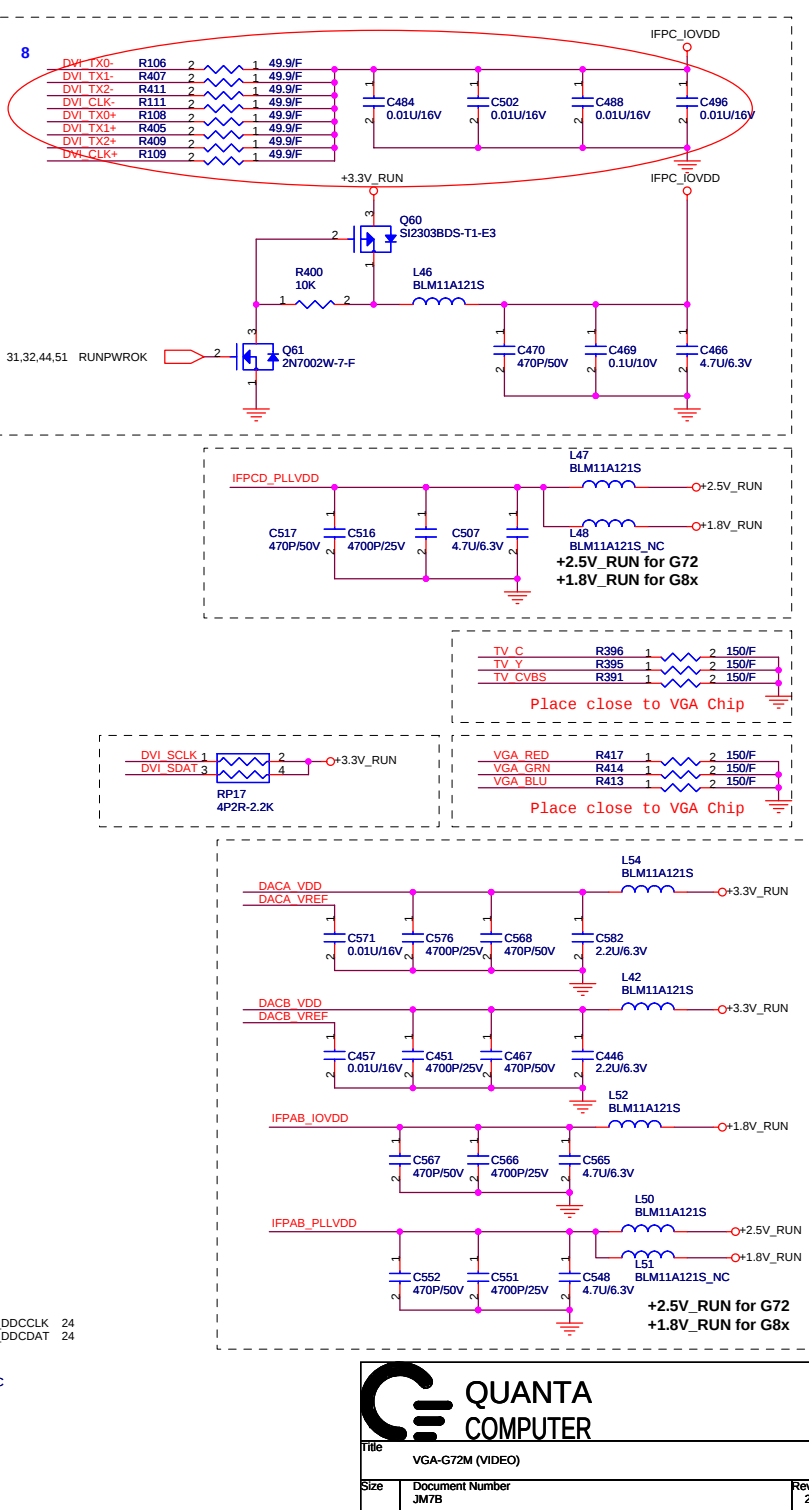
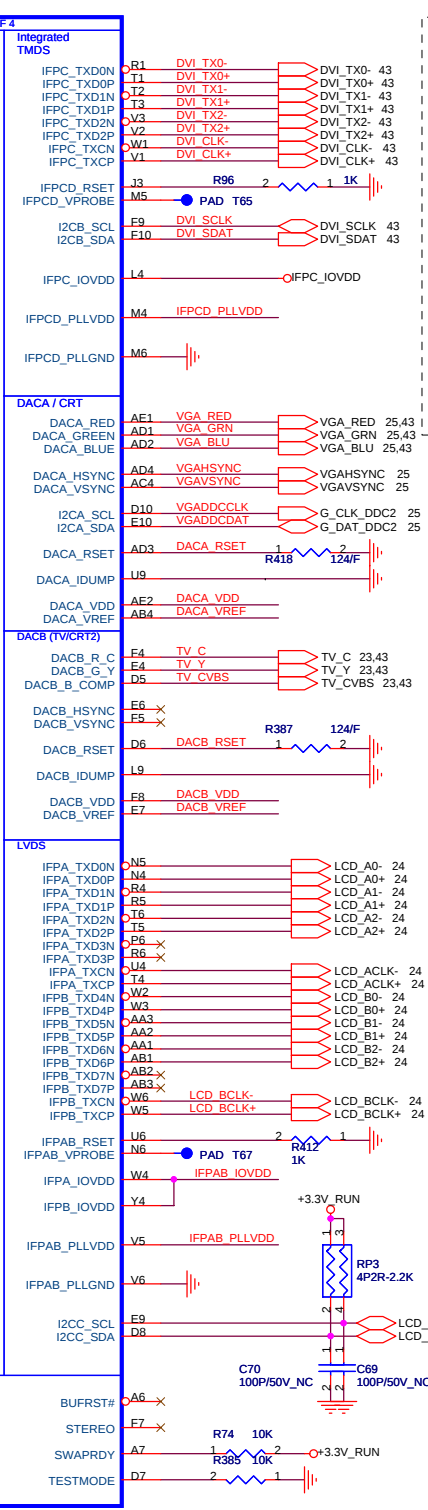
Thermal Diode

PLL & XTAL

Test

ROM

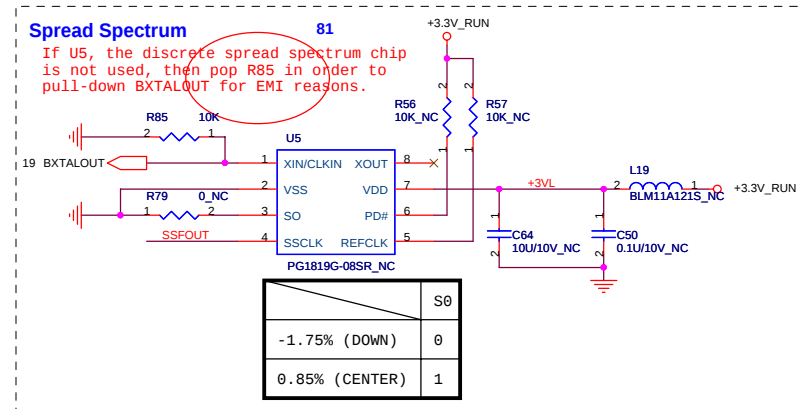
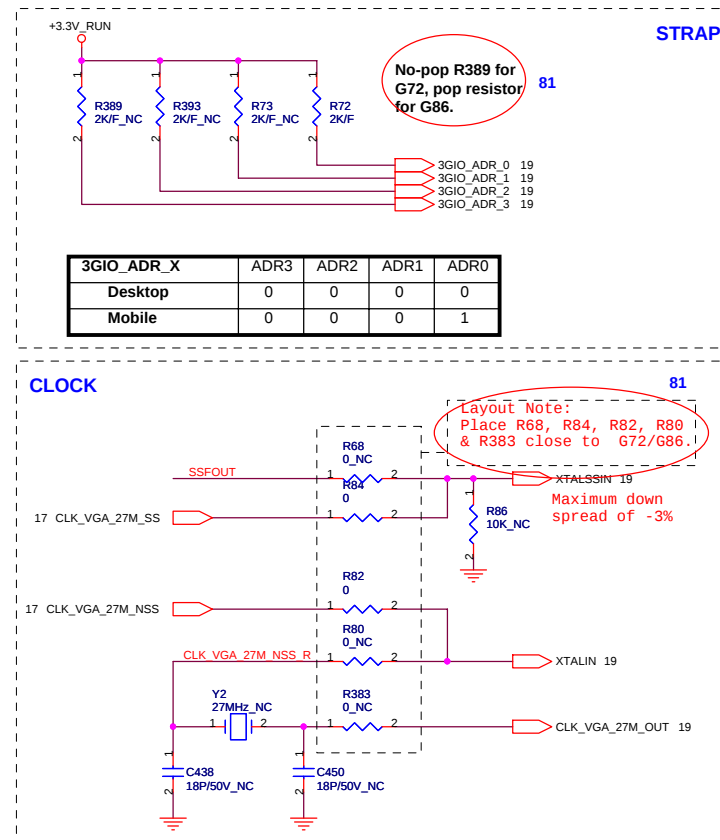
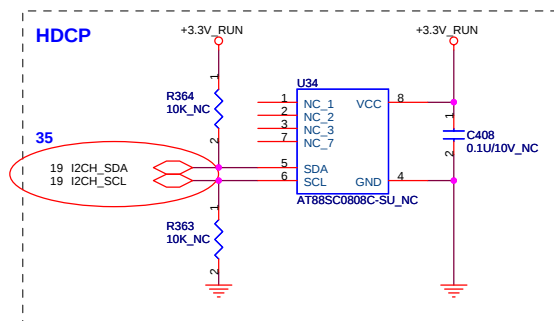
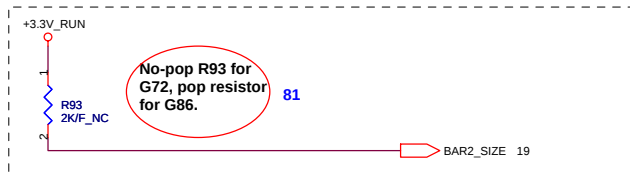
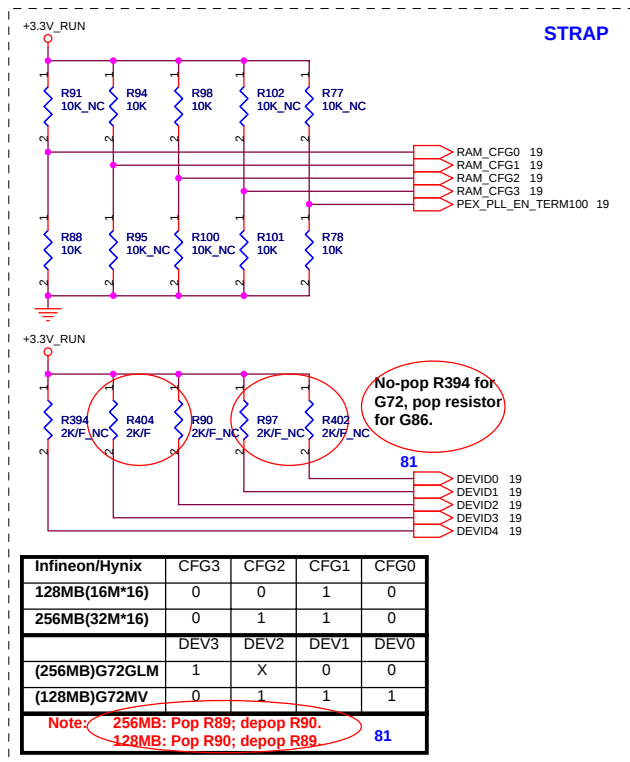
MISC





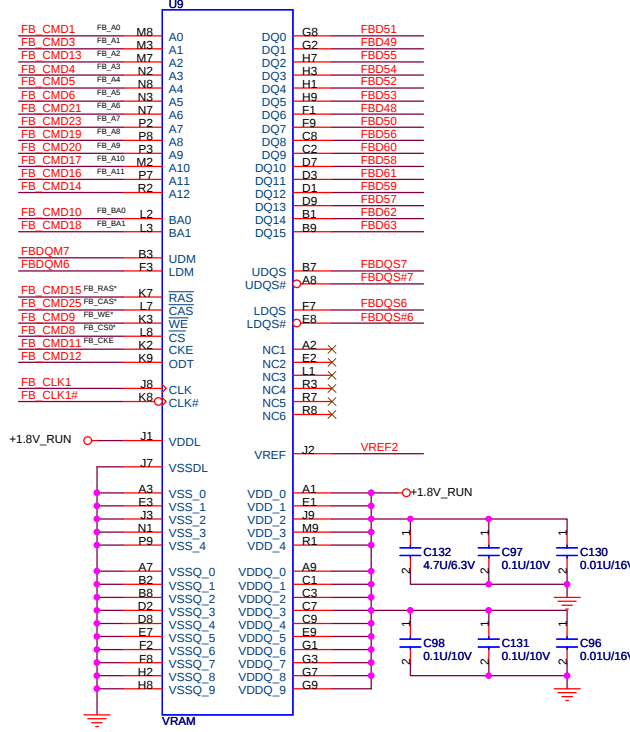
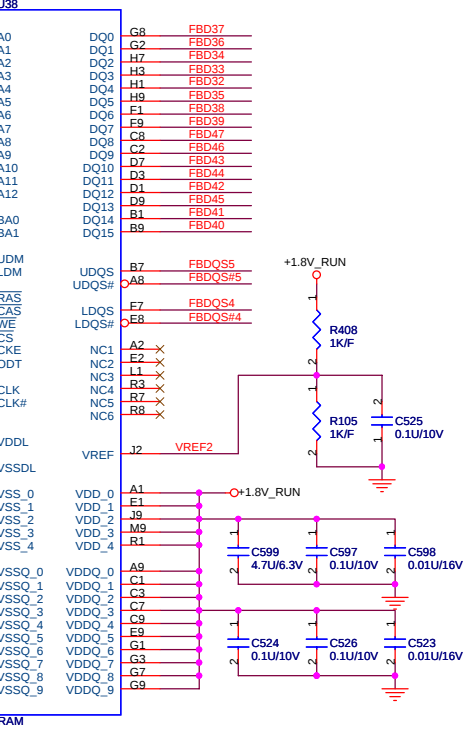
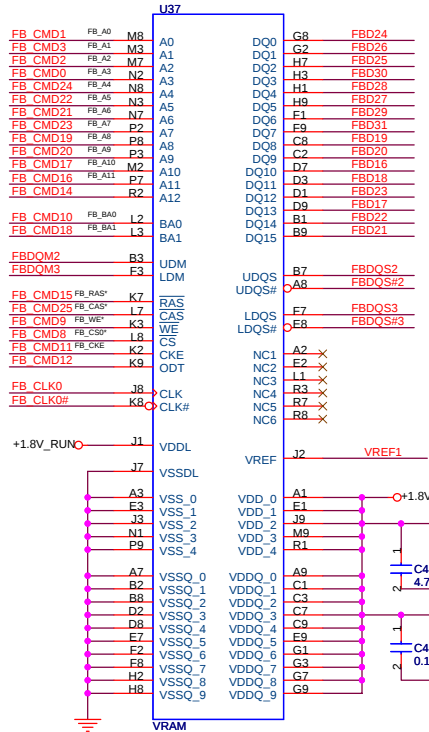
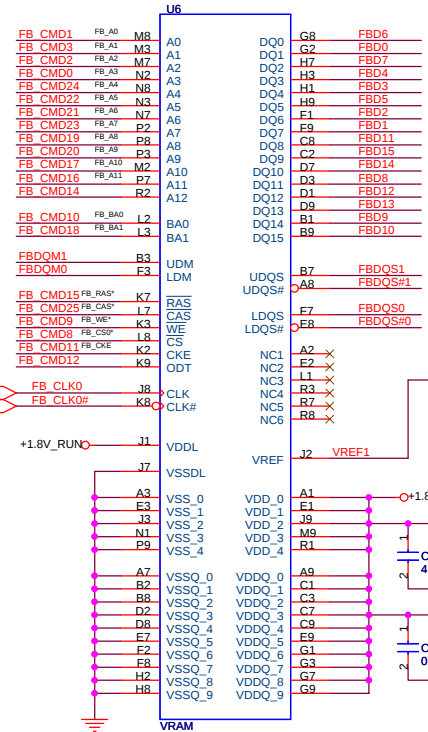
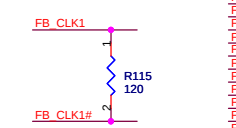
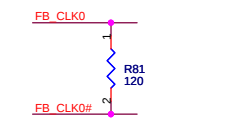
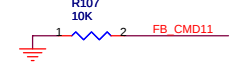
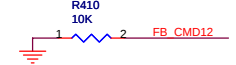
QUANTA
COMPUTER

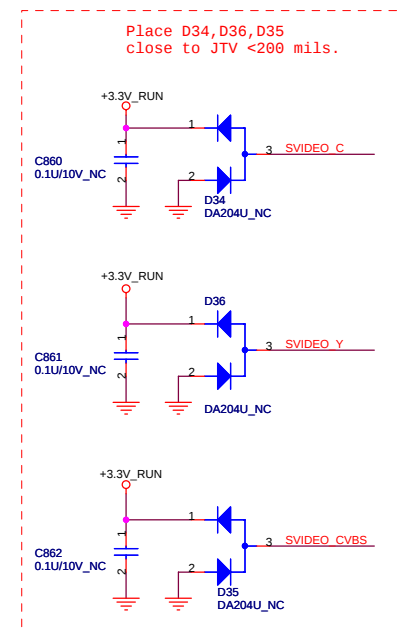
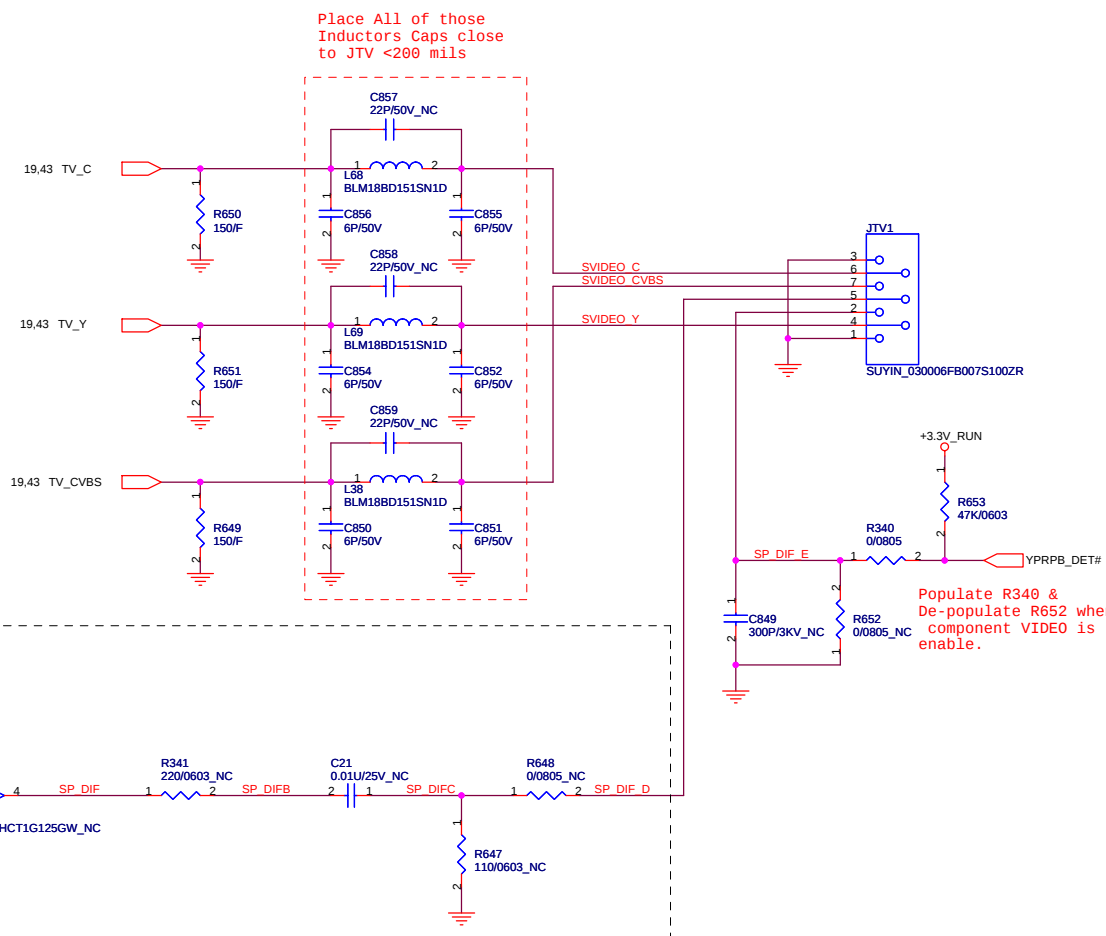
Title VGA-G72M (VIDEO)		
Size JM7B	Document Number	Rev 2A
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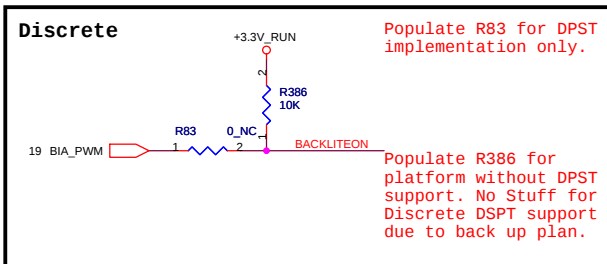
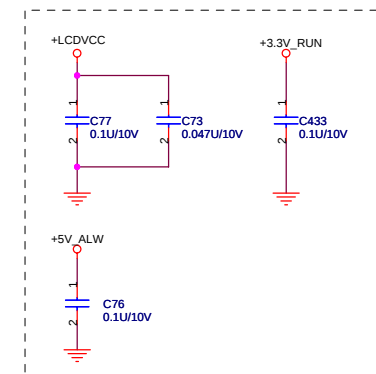
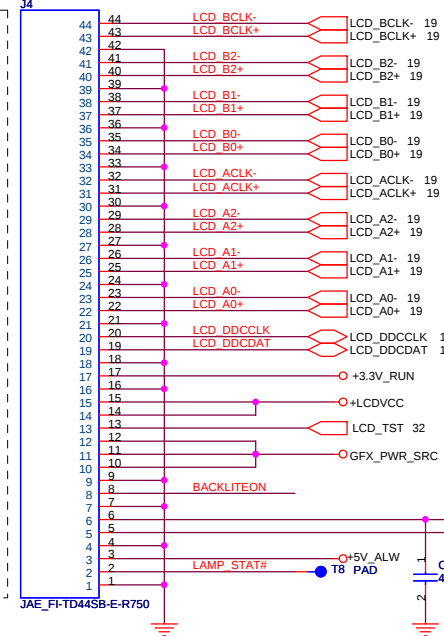
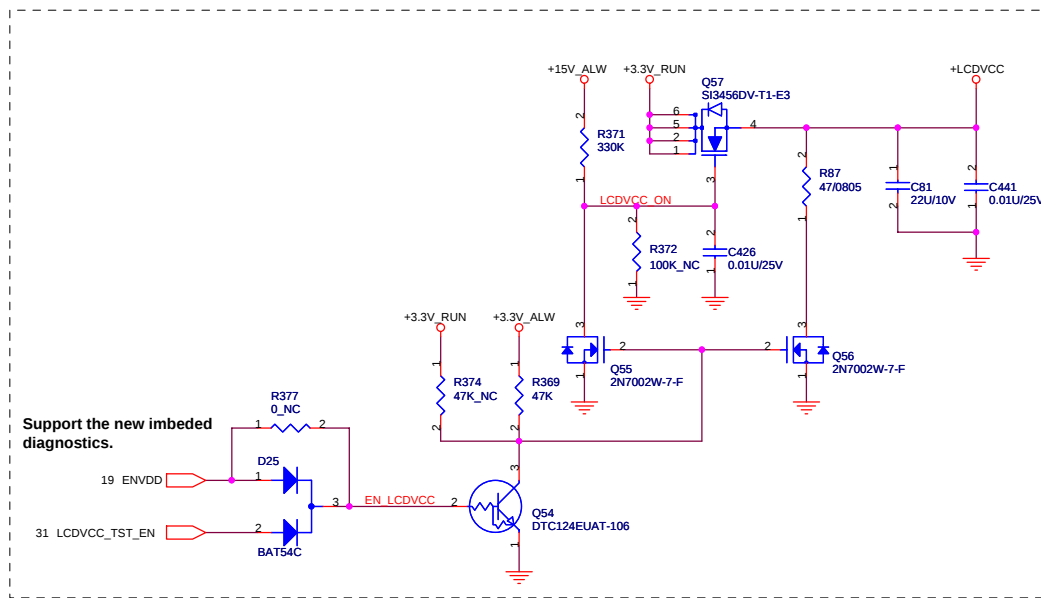




FB_CMD[0..26] 21
FBD[0..63] 21
FBDQM[0..7] 21
FBDQS[0..7] 21

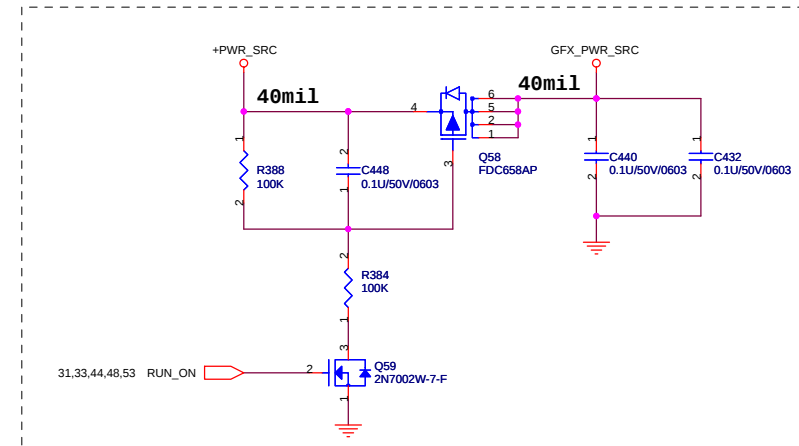


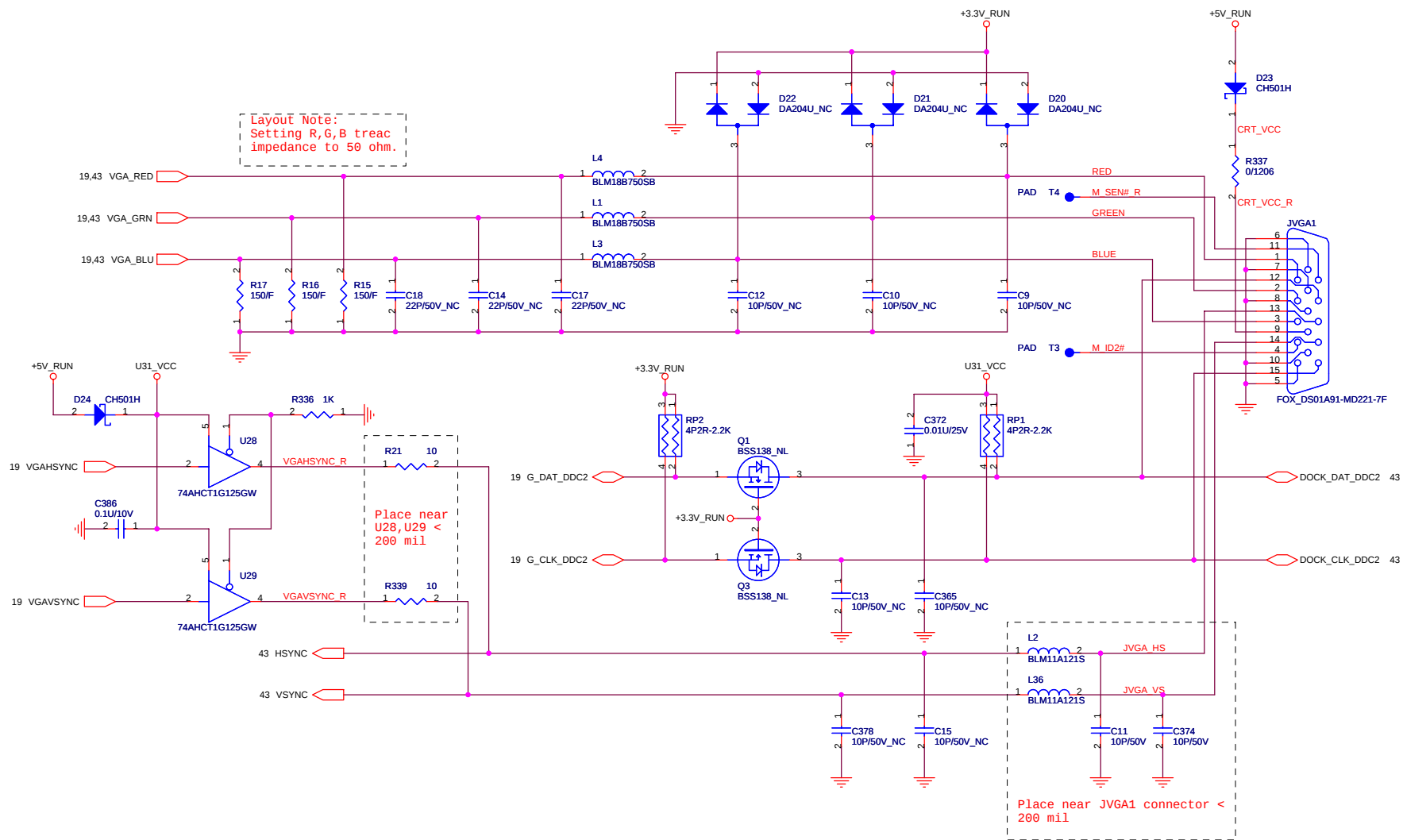




Shunt capacitors on LVDS for improving WWAN.

LCD_B0-	C430	1	2	3.3P/50V_NC	LCD_B0+
LCD_B1-	C434	1	2	3.3P/50V_NC	LCD_B1+
LCD_B2-	C425	1	2	3.3P/50V_NC	LCD_B2+
LCD_BCLK-	C63	1	2	3.3P/50V_NC	LCD_BCLK+
LCD_A0-	C80	1	2	3.3P/50V_NC	LCD_A0+
LCD_A1-	C71	1	2	3.3P/50V_NC	LCD_A1+
LCD_A2-	C72	1	2	3.3P/50V_NC	LCD_A2+
LCD_ACLK-	C57	1	2	3.3P/50V_NC	LCD_ACLK+







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Title CRT&TV CONN		
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+5V_HDD

C357 0.1uF/10V_NC

C358 1000pF/50V_NC

Place caps close to connector.

GND1
RXN
RXPO
GND2
TXN
TXP
GND3

SATA_TX0+ 11
SATA_TX0- 11

SATA_RXN0_C
SATA_RXPO_C

3.3V_0
3.3V_1
3.3V_2
GND4
GND5
GND6
5V_0
5V_1
5V_2
GND7
RSVD
GND8
12V_0
12V_1
12V_2

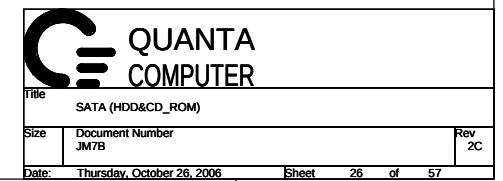
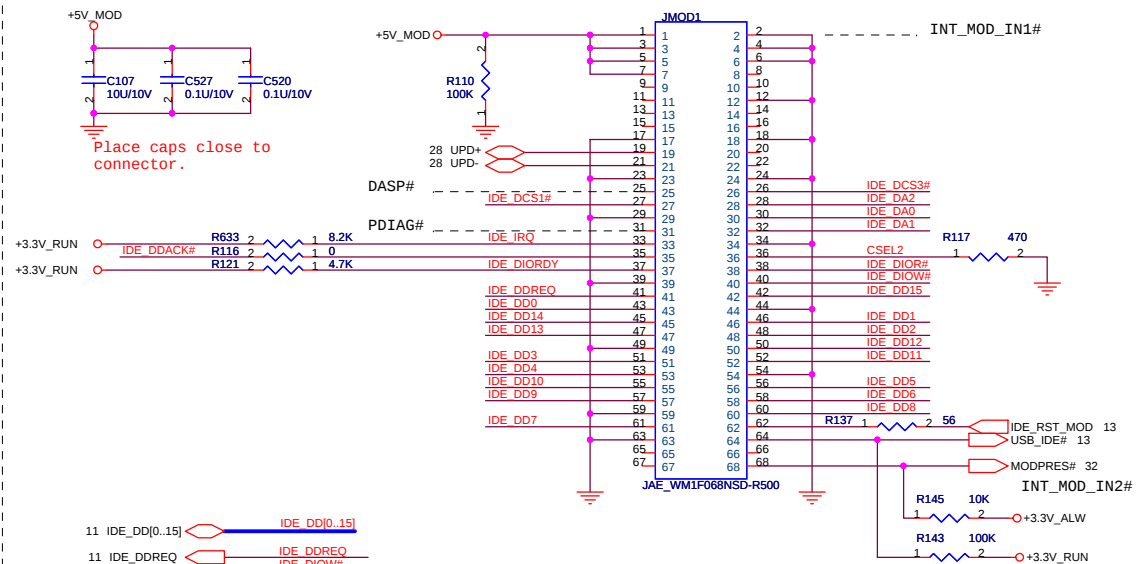
+3.3V_RUN
+5V_HDD

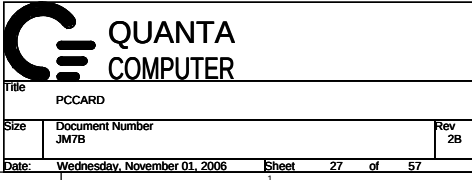
MLX_67492-1821

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22

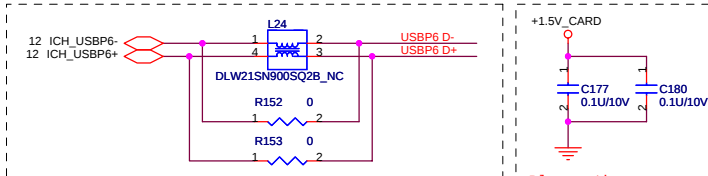
SATA_RXN0_C C345 2 1 3900P/25V SATA_RX0- 11

SATA_RXPO_C C346 2 1 3900P/25V SATA_RX0+ 11

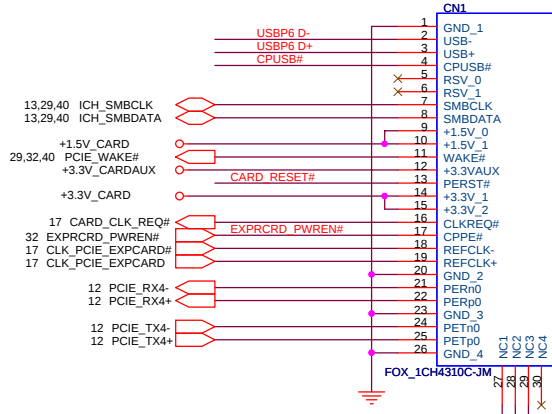
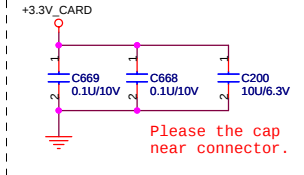




Express Card



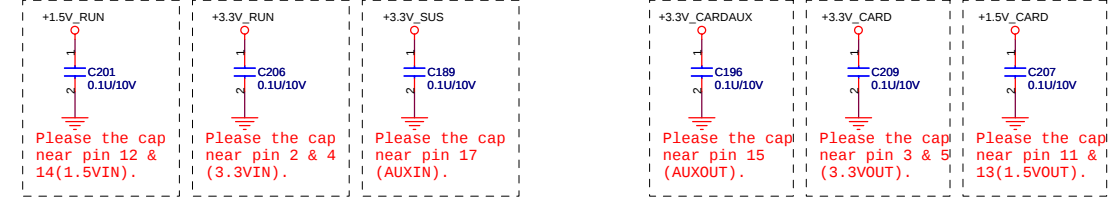
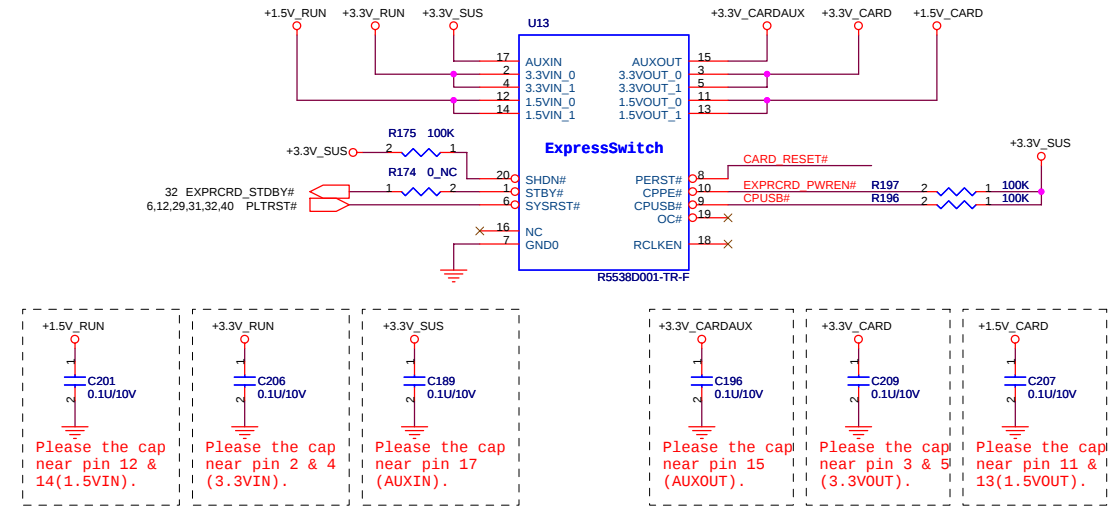
Please the cap near connector.



JAE PX10FS16PH-26P

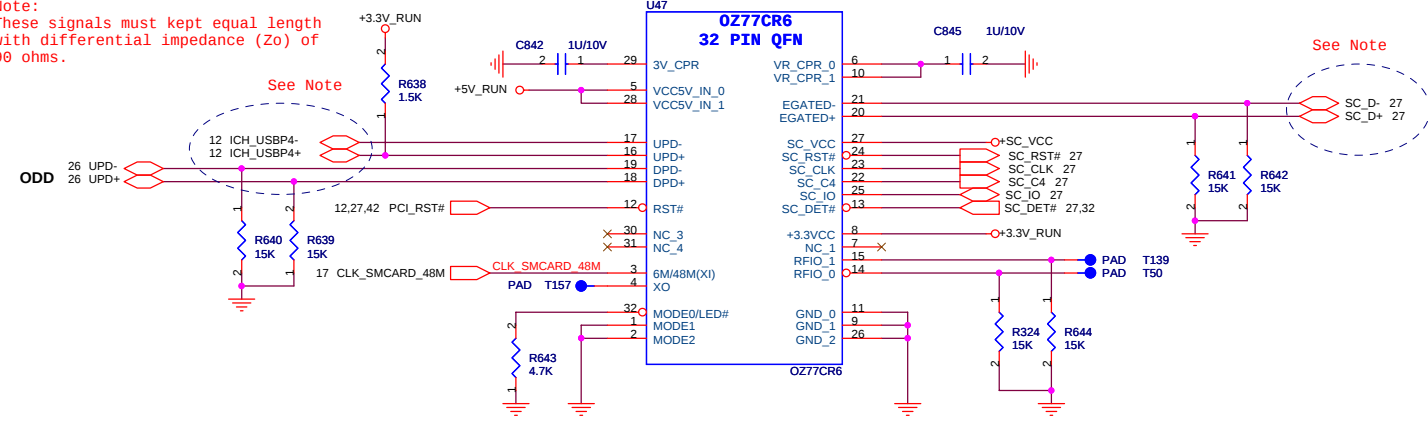
PCI-Express TX and RX direct to connector.

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

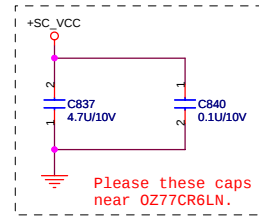
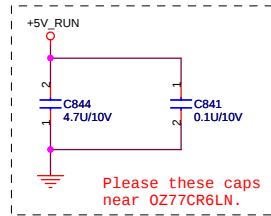
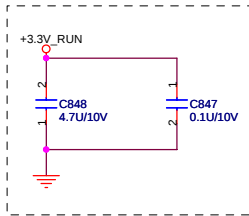
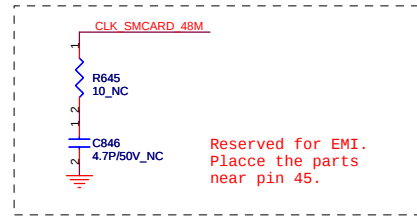


Smart Card

Note:
These signals must kept equal length with differential impedance (Z_0) of 90 ohms.



See Note

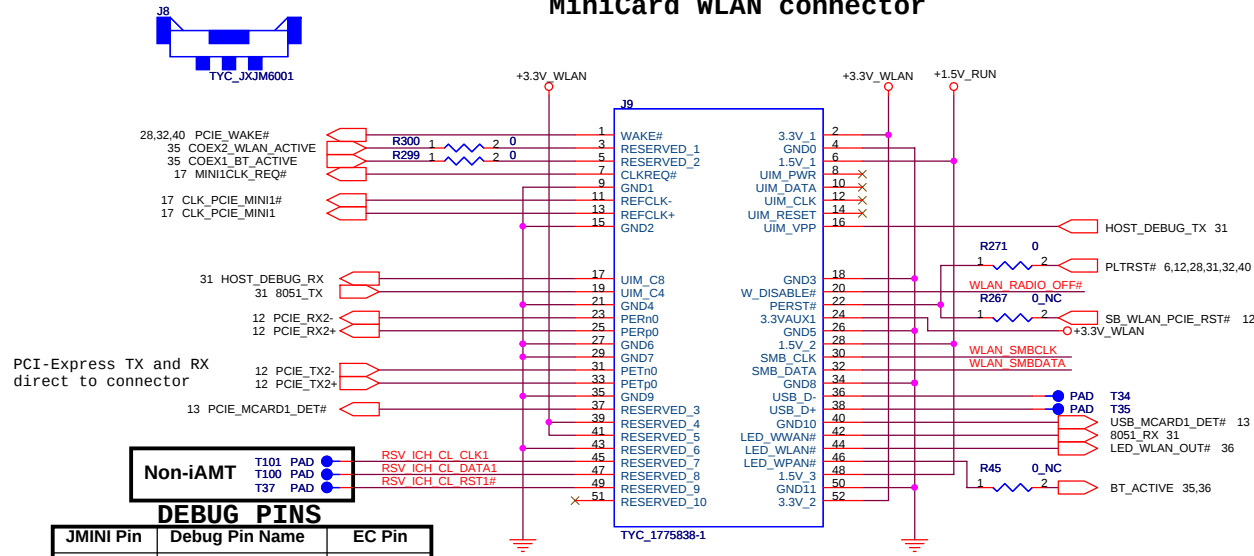




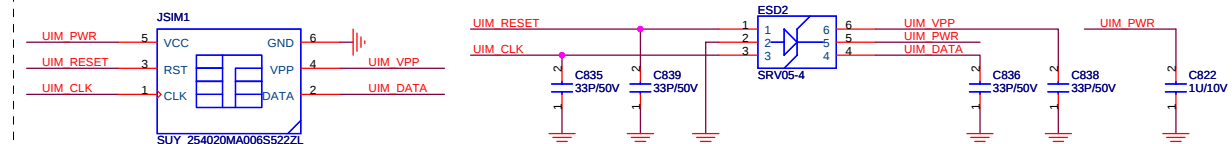
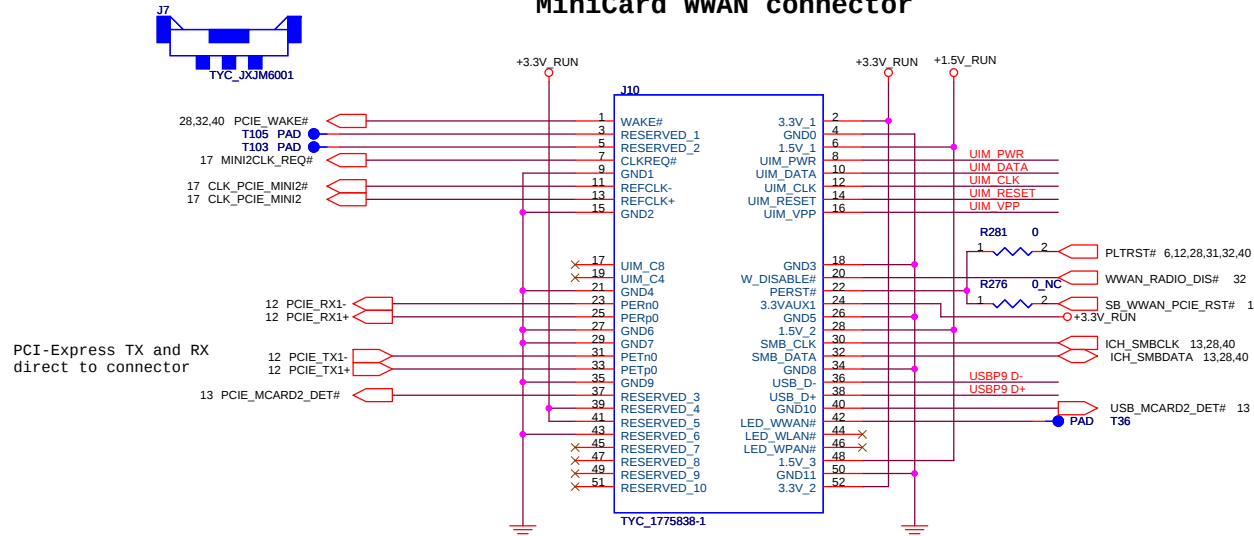
**QUANTA
COMPUTER**

Title ExpressCard/SmartCard		
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MiniCard WLAN connector



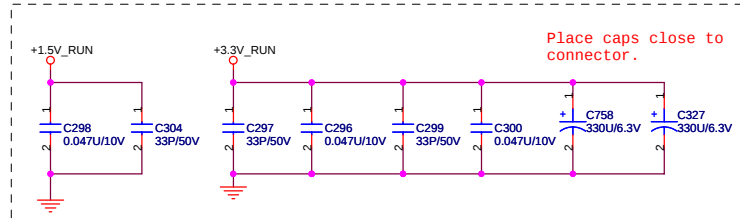
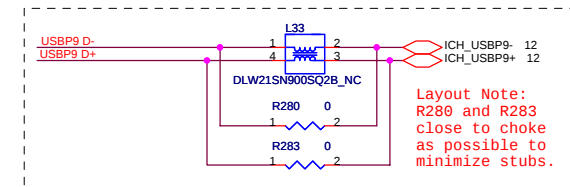
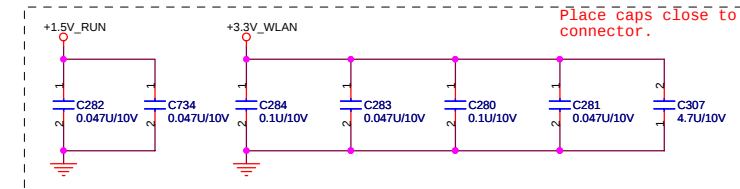
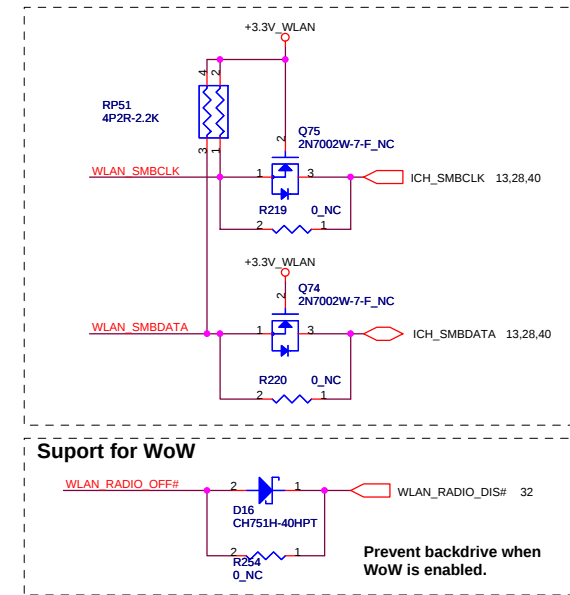
MiniCard WWAN connector



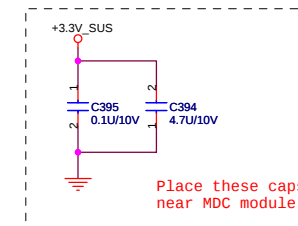
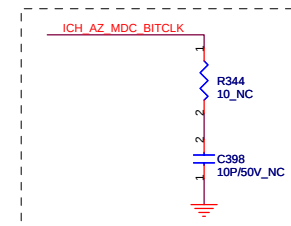
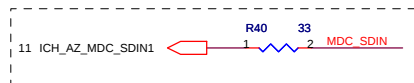
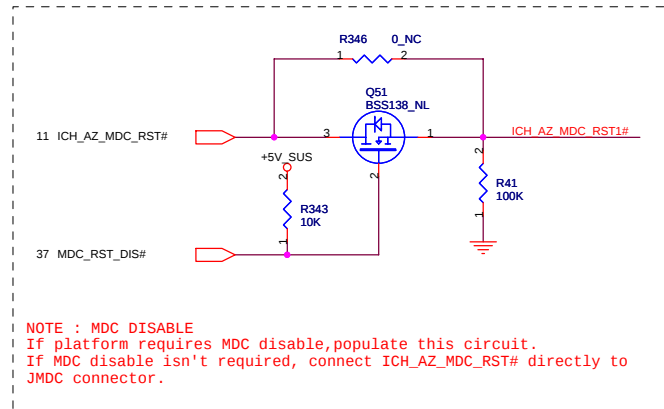
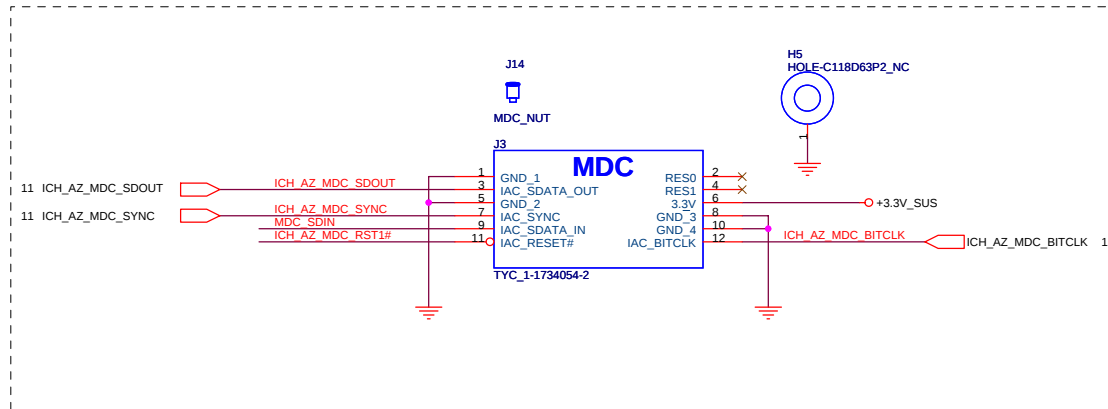
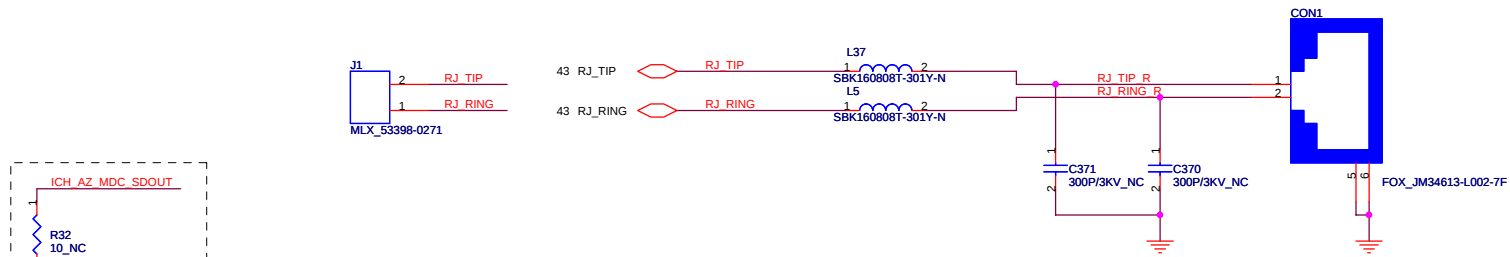
Place as close as possible to JMINI connector

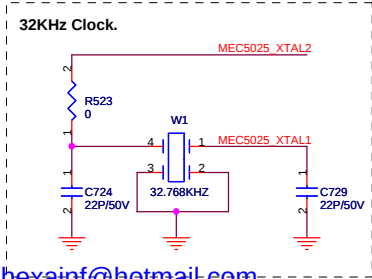
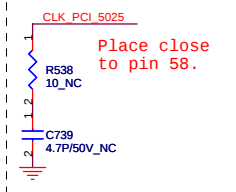
hexainf@hotmail.com

GRATIS - FOR FREE

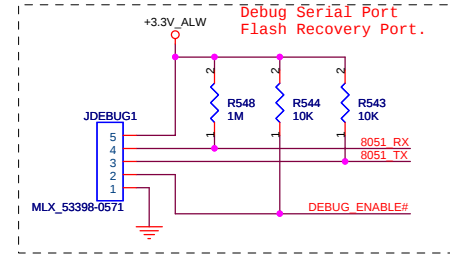
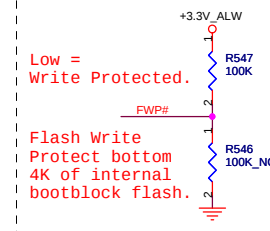
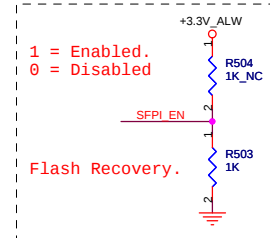
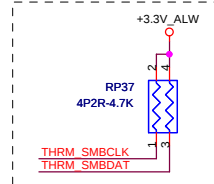
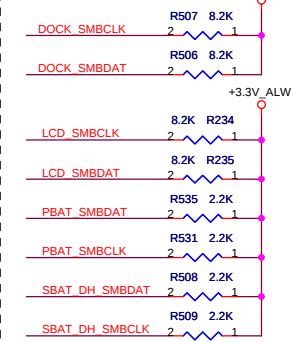
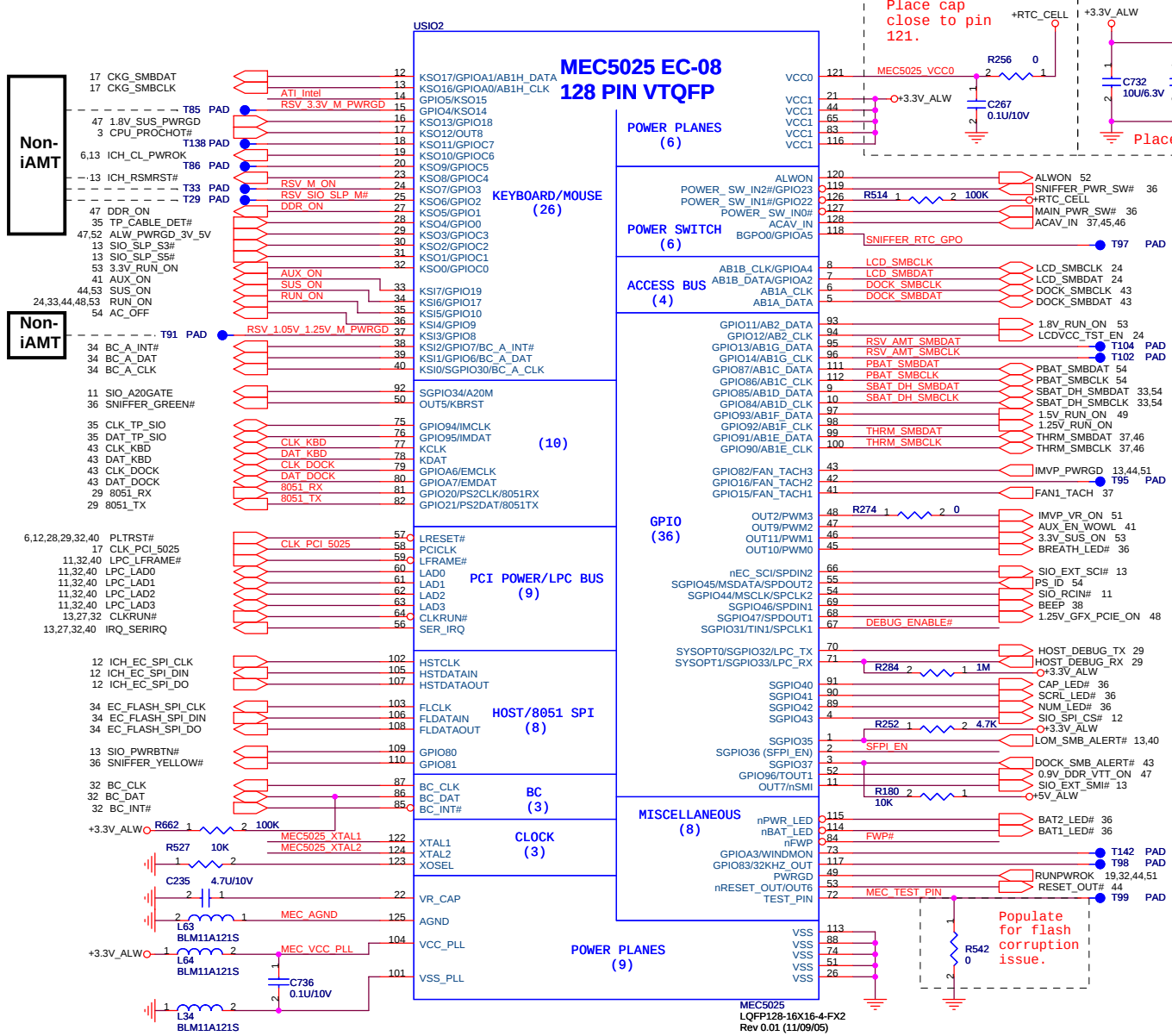


QUANTA COMPUTER		
Title: MINI-PCI		
Size: JM7B	Document Number: JM7B	Rev: 2C
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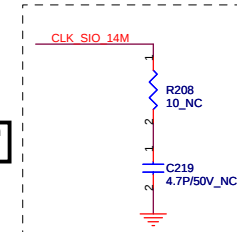
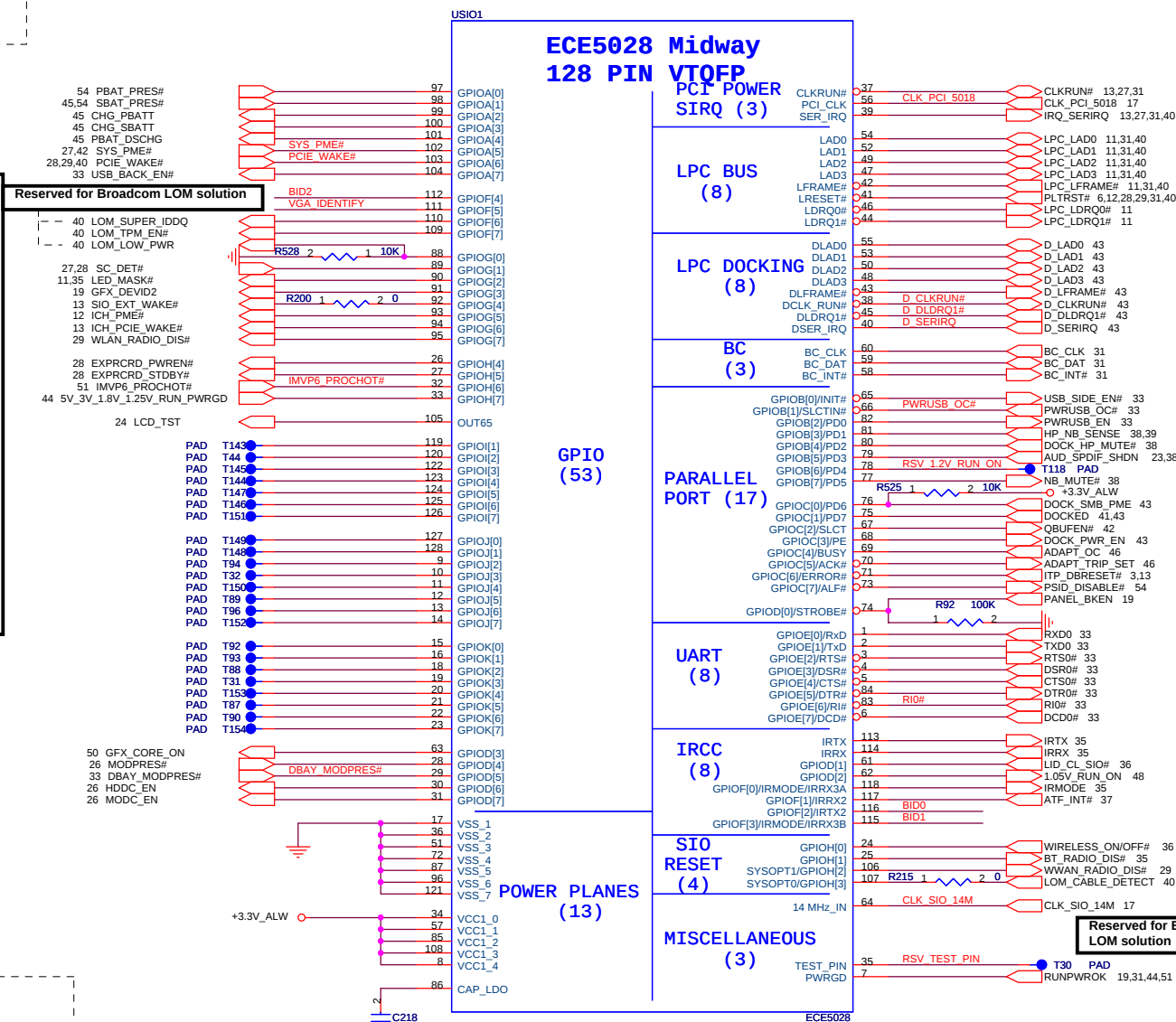
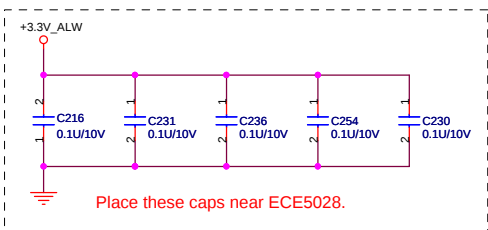


hexainf@hotmail.com
GRATIS + FOR FREE

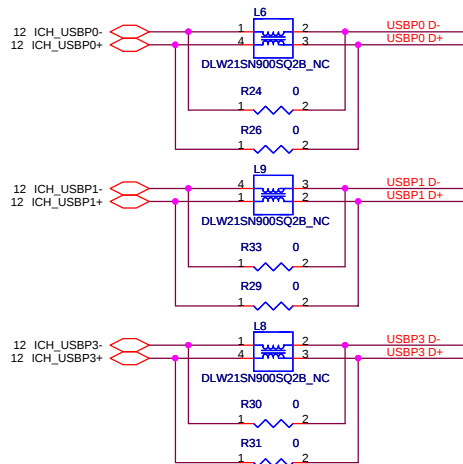


Title	Ultra I/O Controller MEC5025
-------	------------------------------

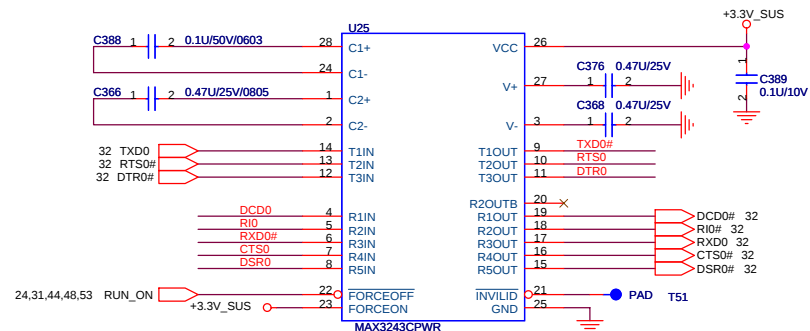
Size	Document Number JM7B	Rev 2C
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External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

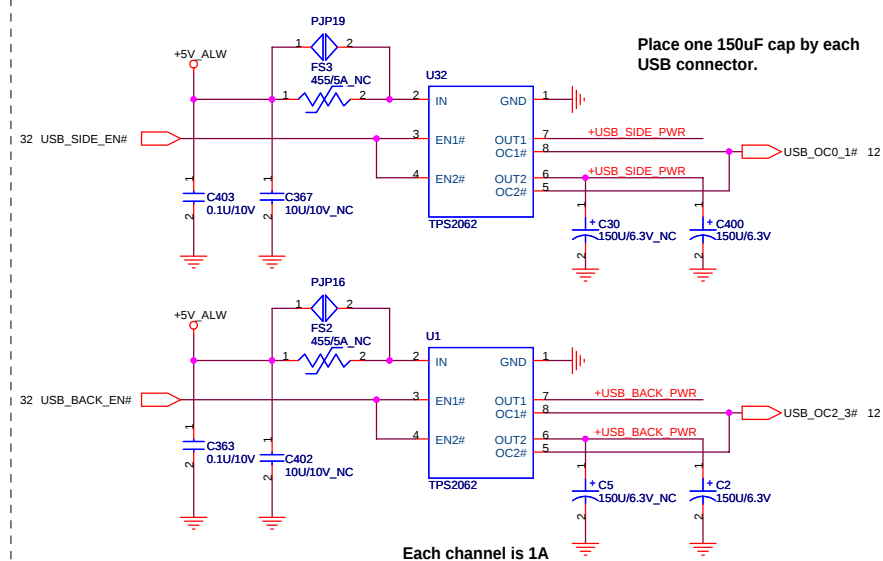
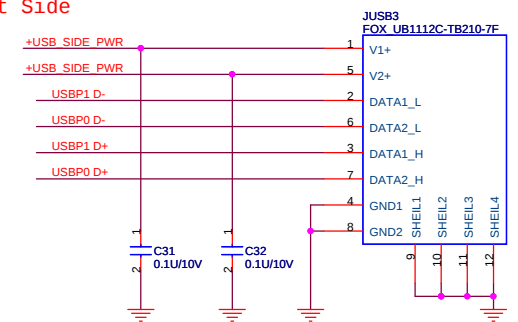


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



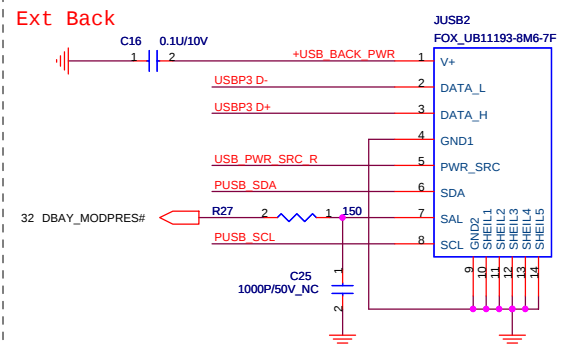
Place these beads close to JCOM1 as soon as possible
If MAX3243 pin 22 tied to RUN_ON, then it can not support Ring Out

Ext Side



Each channel is 1A

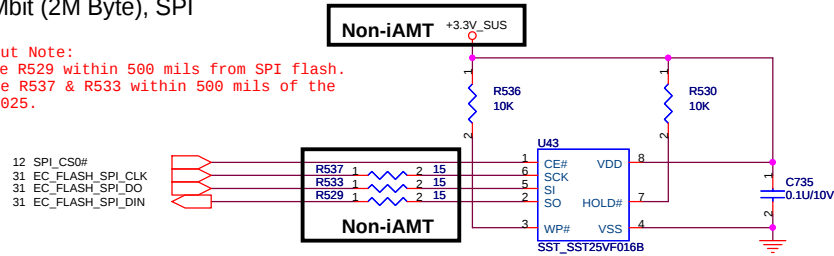
Ext Back



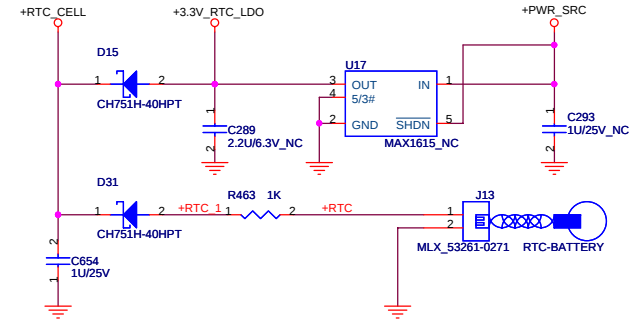
Title			
SERIAL PORT & USB			
Size	Document Number	Rev	
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16Mbit (2M Byte), SPI

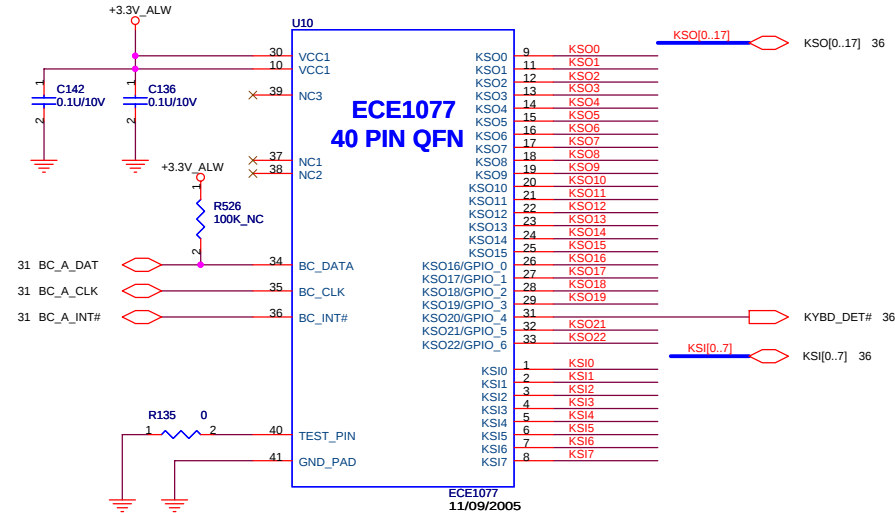
Layout Note:
Place R529 within 500 mils from SPI flash.
Place R537 & R533 within 500 mils of the
MEC5025.



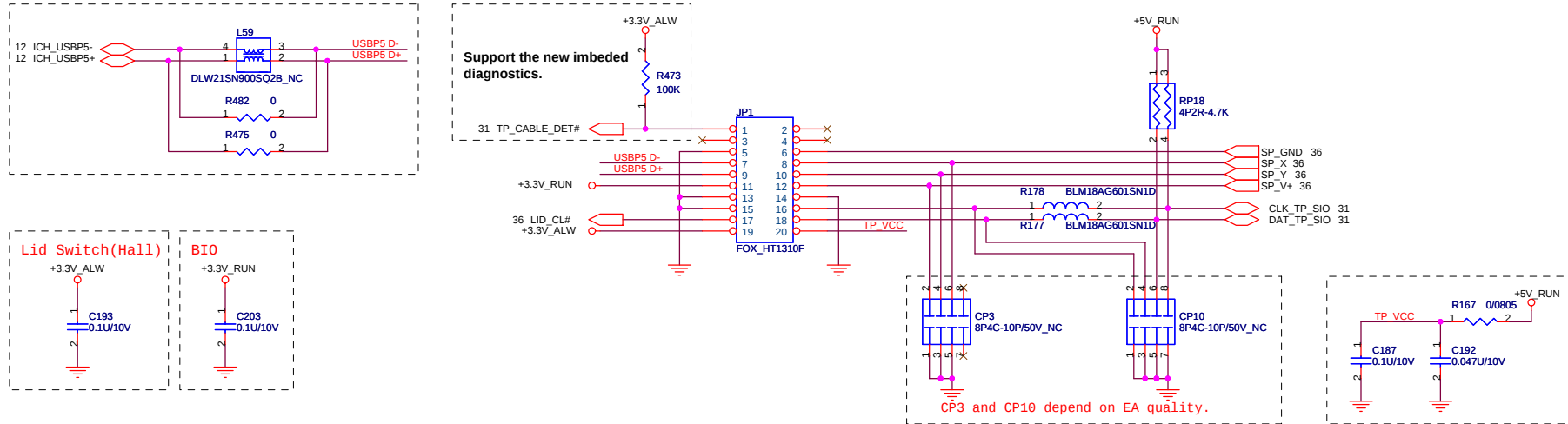
RTC BATTERY



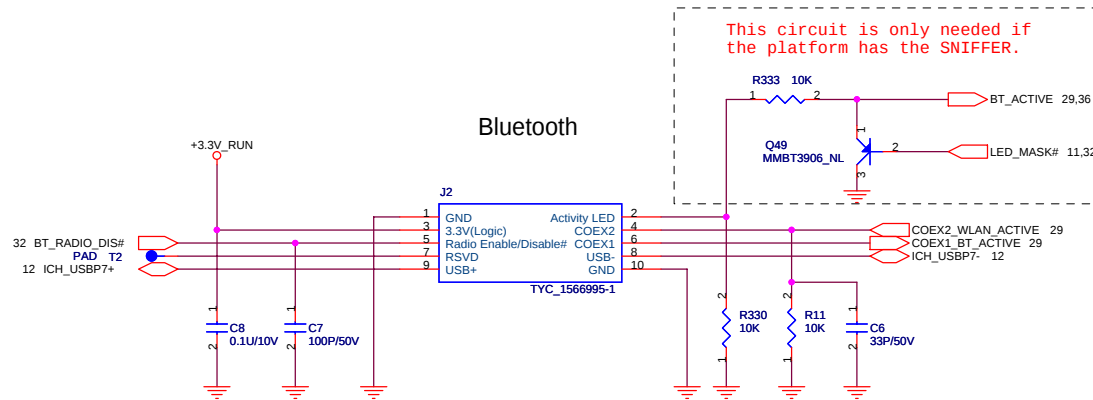
Keyboard Scan Extension



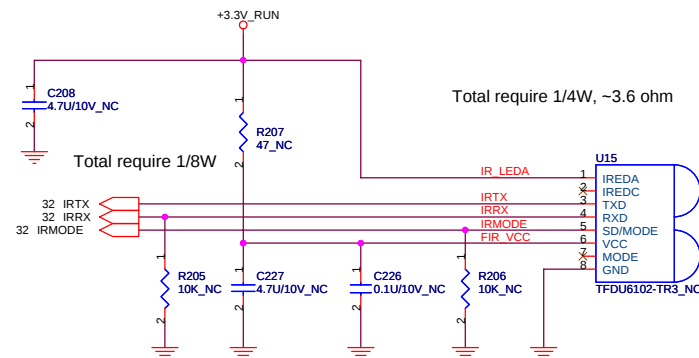
Touch Pad



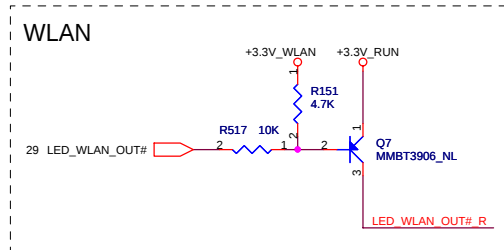
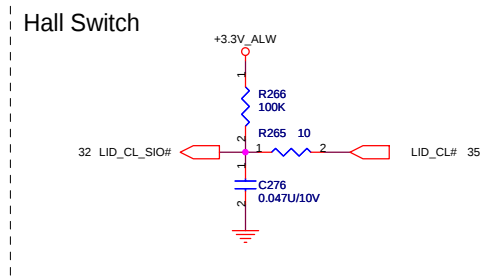
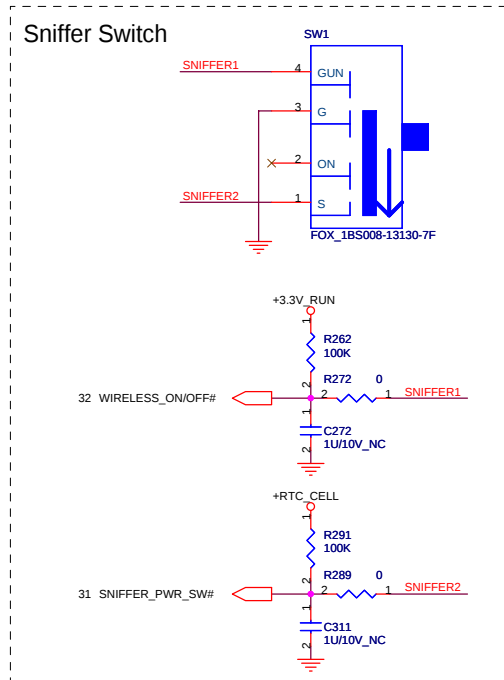
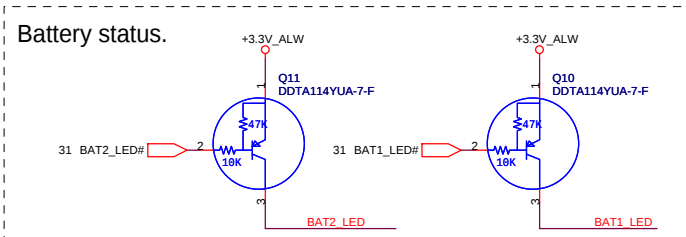
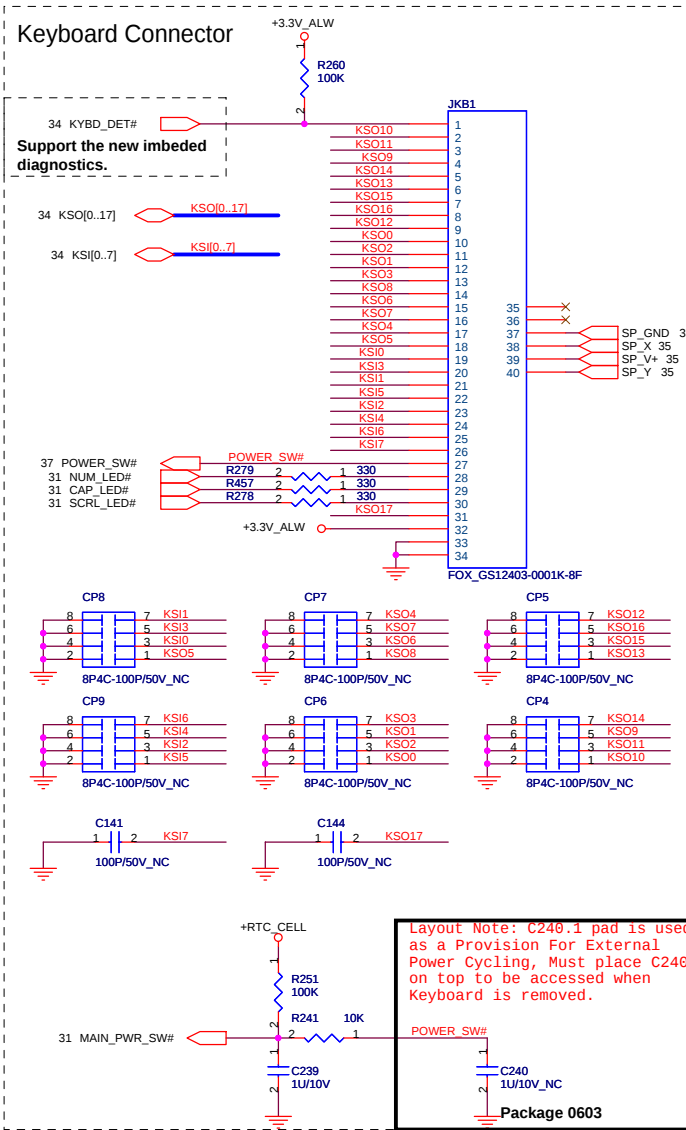
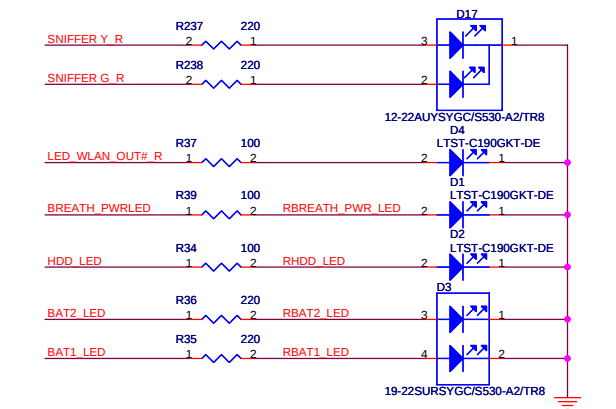
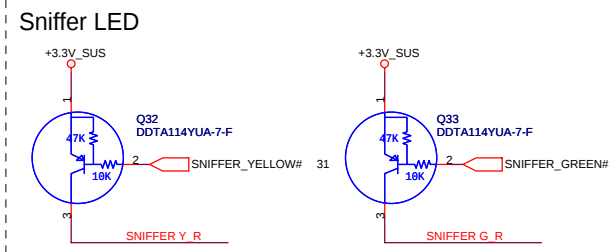
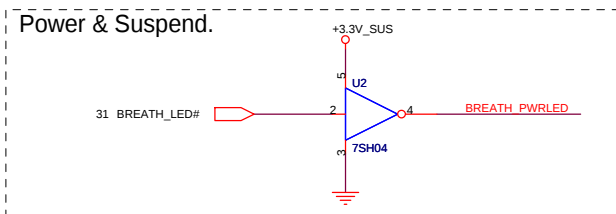
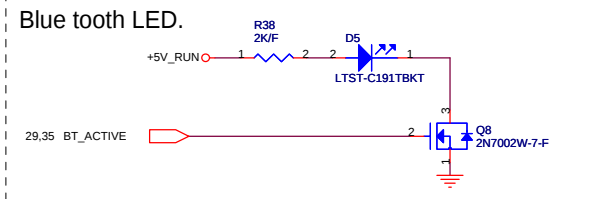
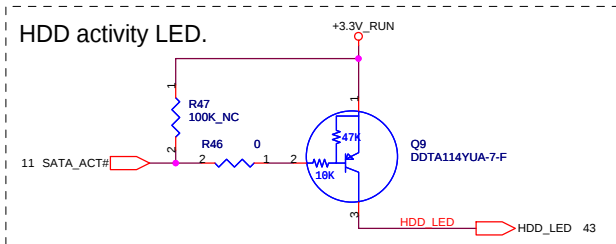
Bluetooth

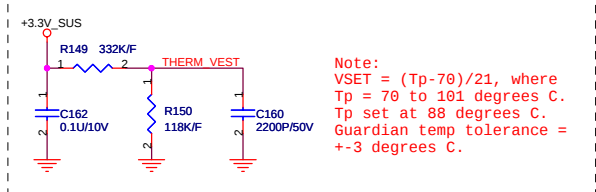
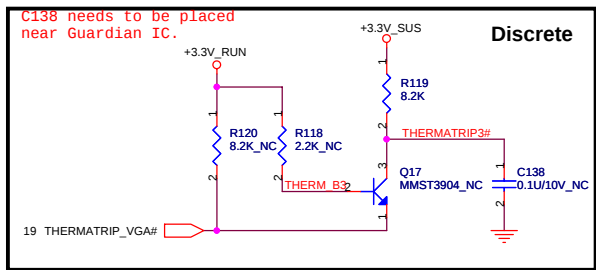
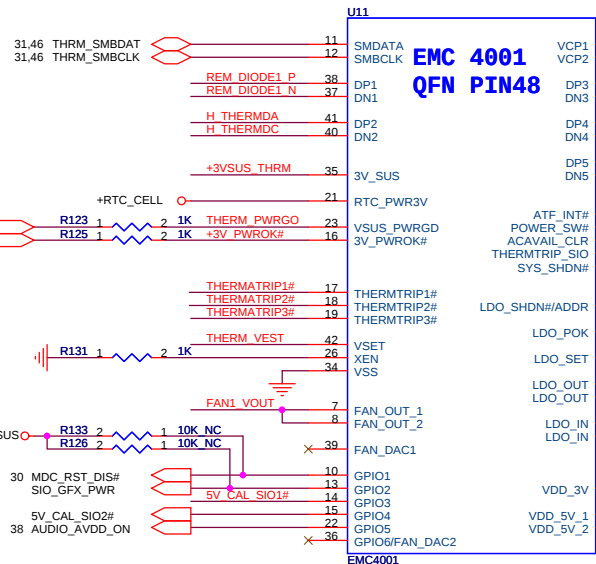
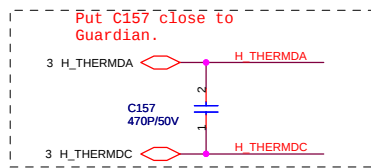
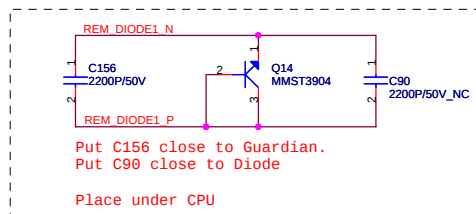
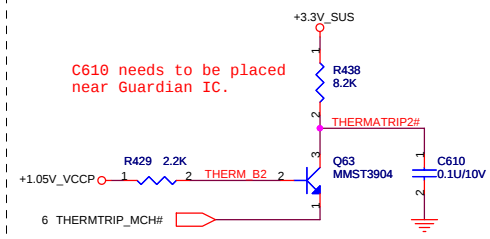
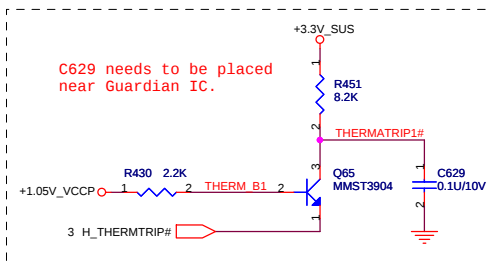
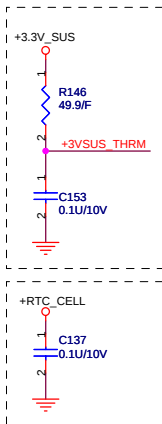
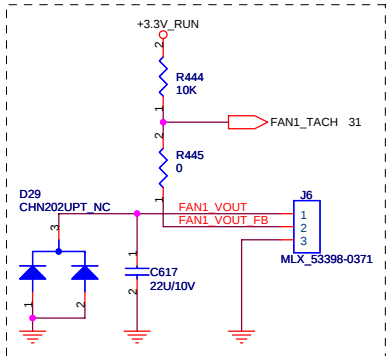


FIR

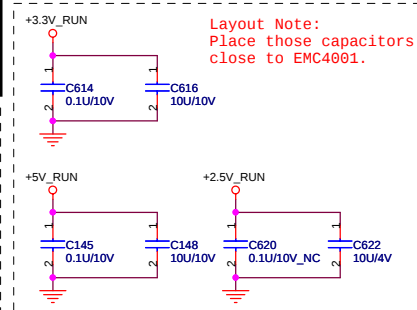
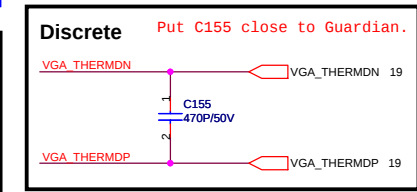
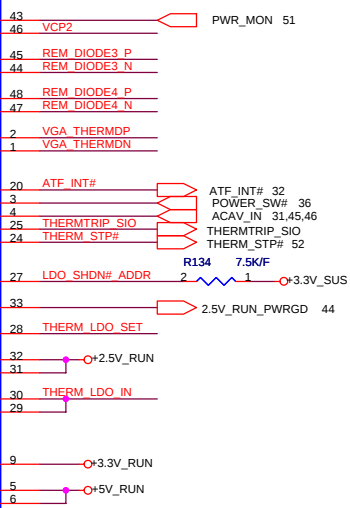
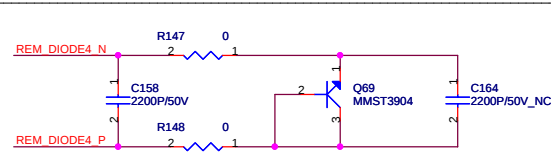
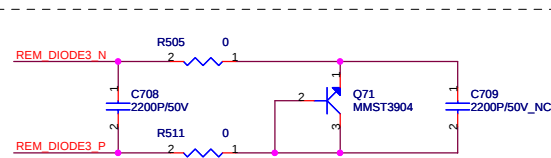


Title TOUCH PAD, BULE TOOTH & FIR		
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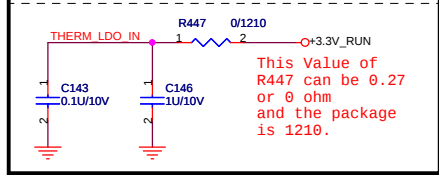
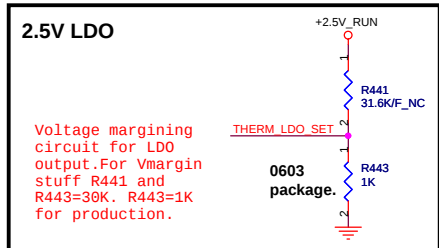
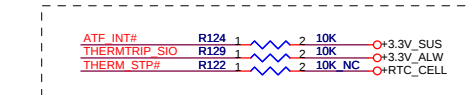
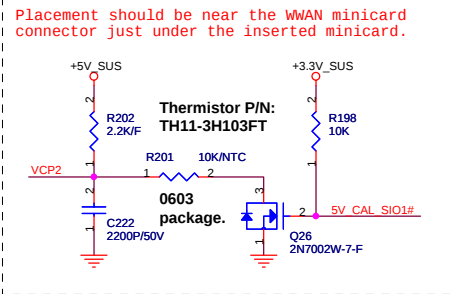


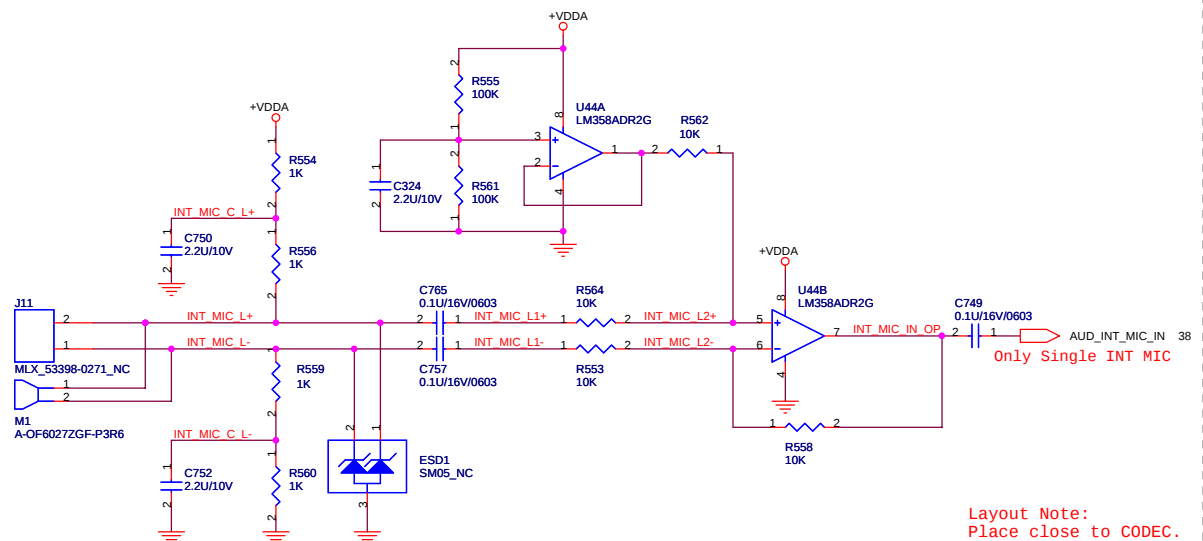
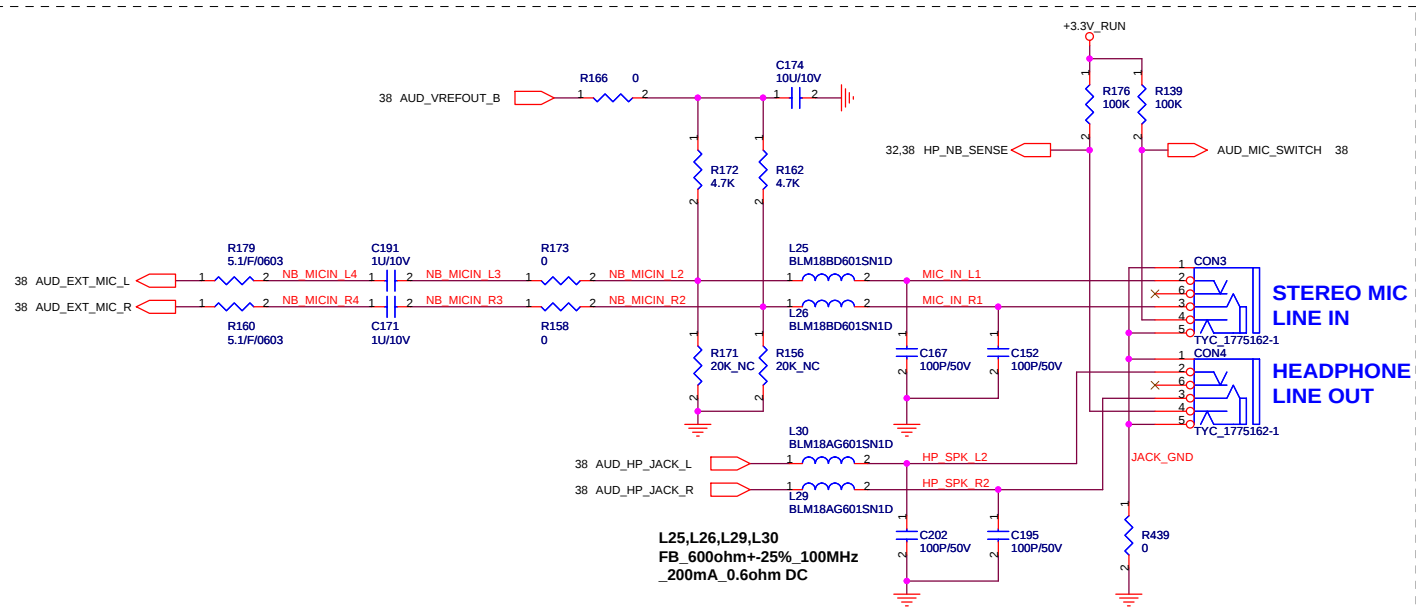
Note:
 $VSET = (T_p - 70) / 21$, where
 $T_p = 70$ to 101 degrees C.
 T_p set at 88 degrees C.
 Guardian temp tolerance = ± 3 degrees C.



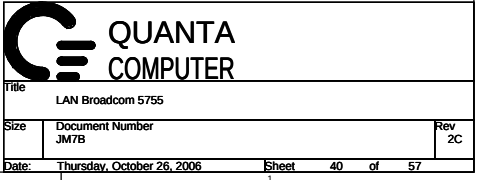
Put C708, R505 & R511 as close as possible to Guardian.
 Put C709 close to Diode.
 Place near the bottom SODIMM

Put C158, R147 & R148 as close as possible to Guardian.
 Put C164 close to Diode.
 Placement should be on bottom side of MB, located within triangle of CPU/MCH/DRAM



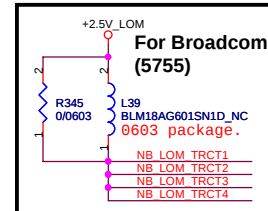
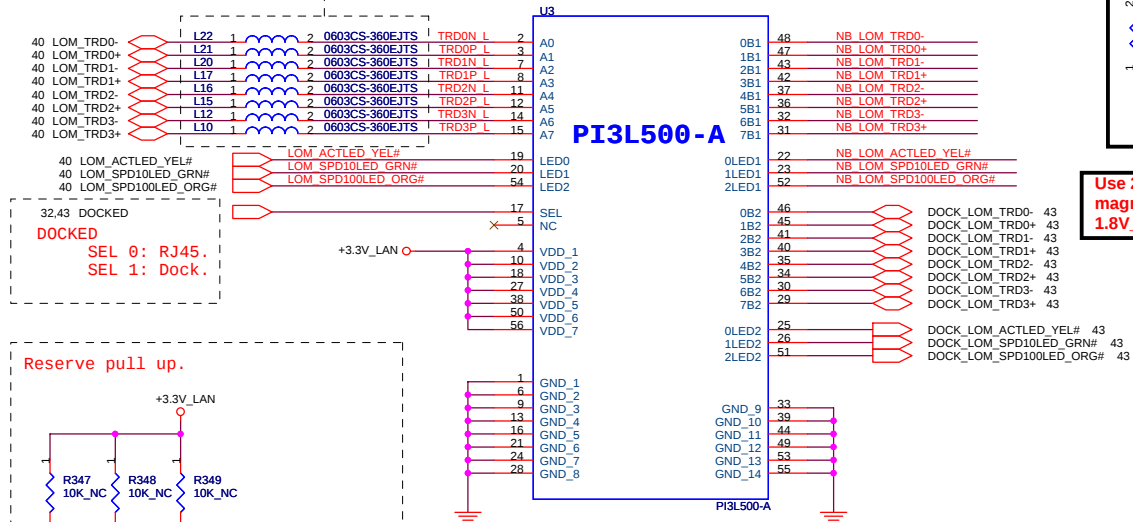


Title		
AUDIO CONN		
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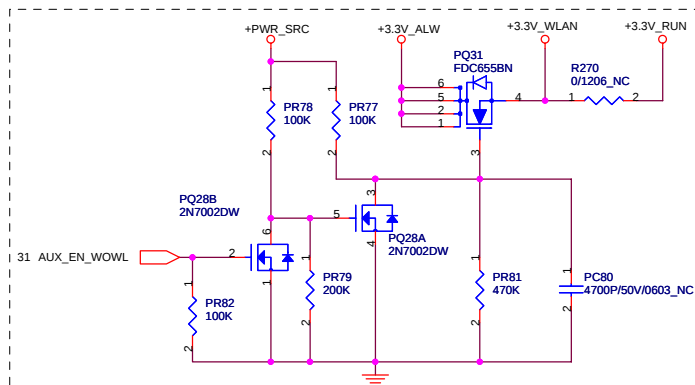
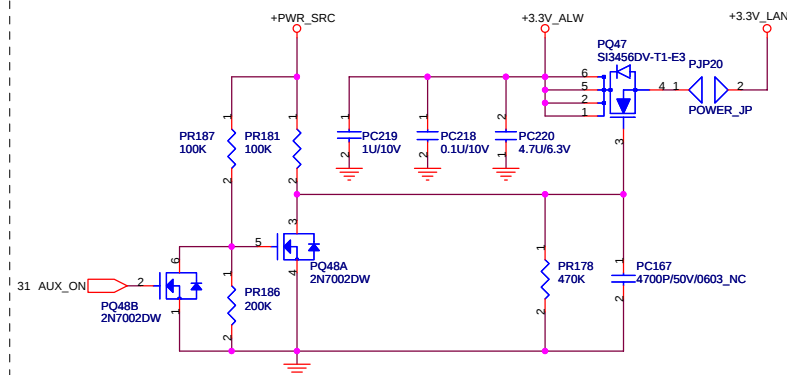
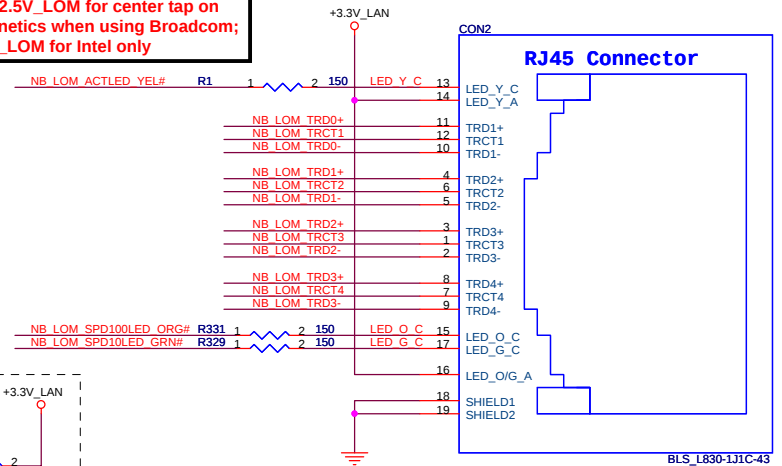
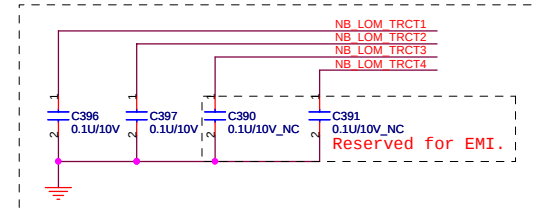


TRANSFORM+RJ45

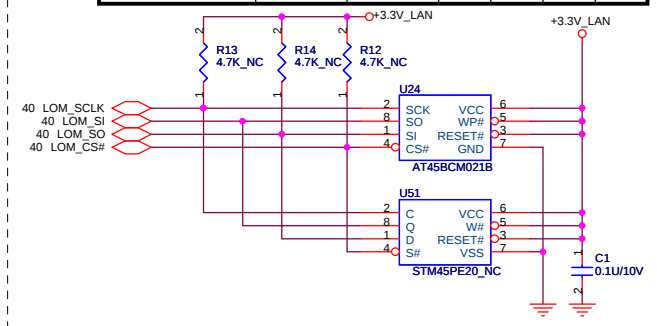
36nH is a suggested value.
Actual value will be systgem dependent.
Must use 0603 package for lower DC resistance.



Use 2.5V_LOM for center tap on magnetics when using Broadcom; 1.8V_LOM for Intel only



	NV_STRAP1	NV_STRAP0	S0	SI	CS#	SCLK
Auto-Sense Mode	0	0	0	0	0	0
ST M45PE20	0	1	1	0	0	1
Atmel AT45BCM021B	0	0	1	0	1	1



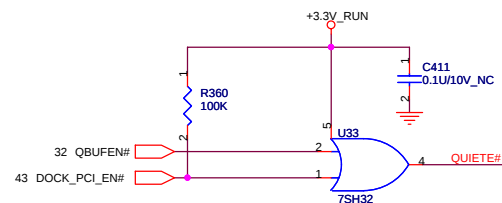
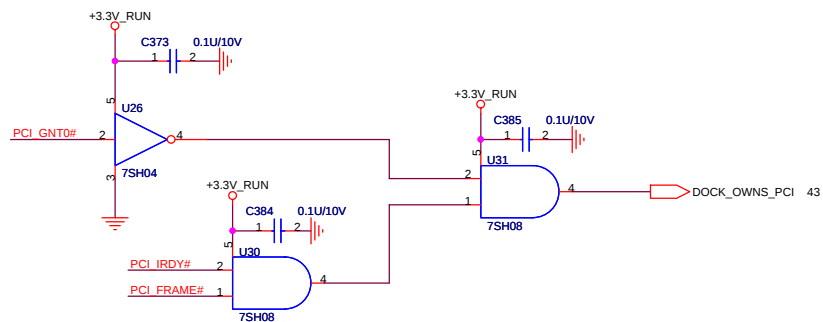
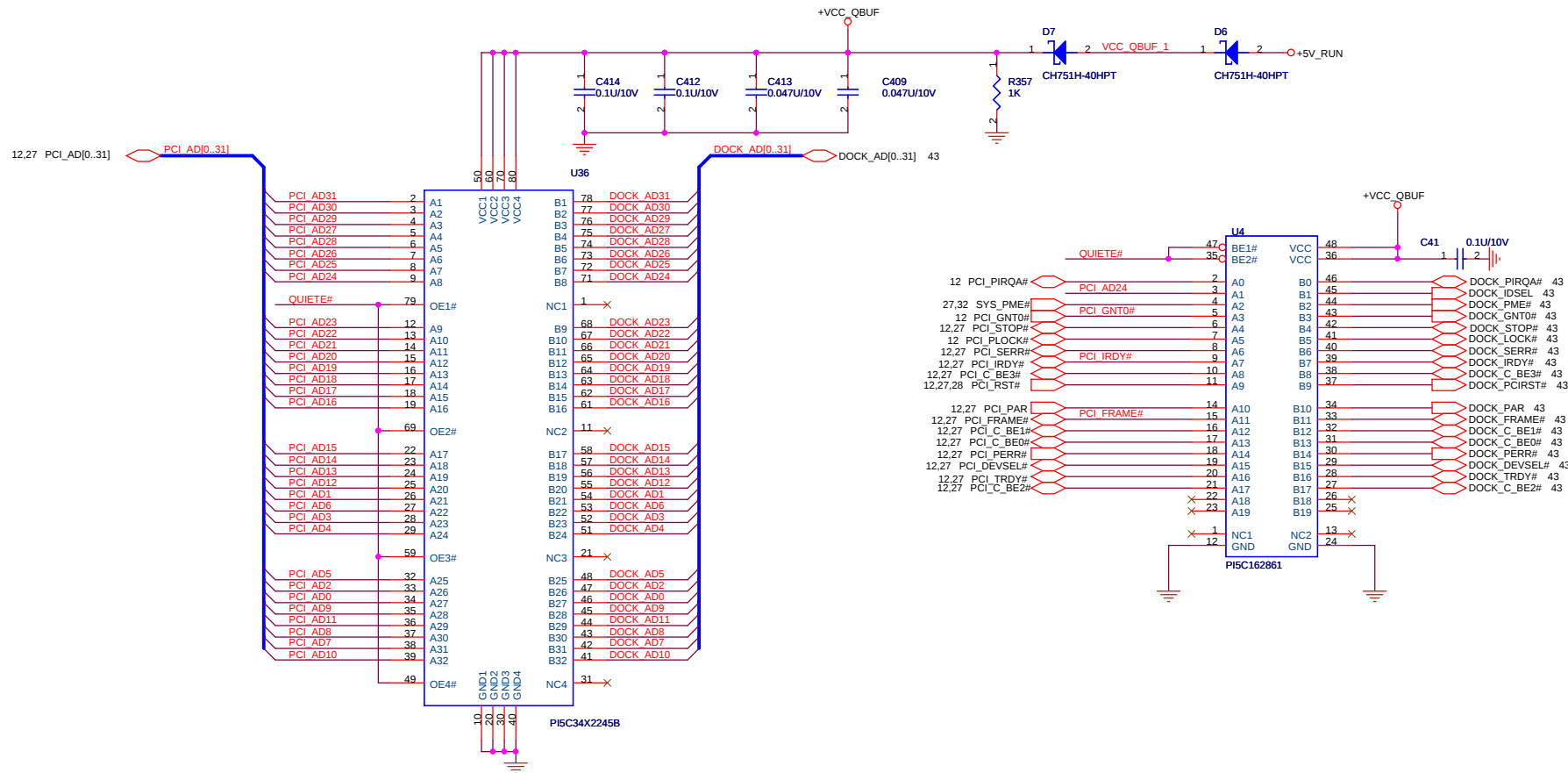
Title	LAN SWITCH
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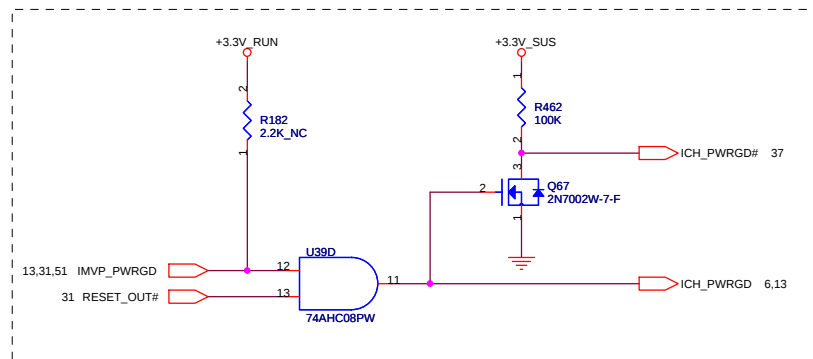
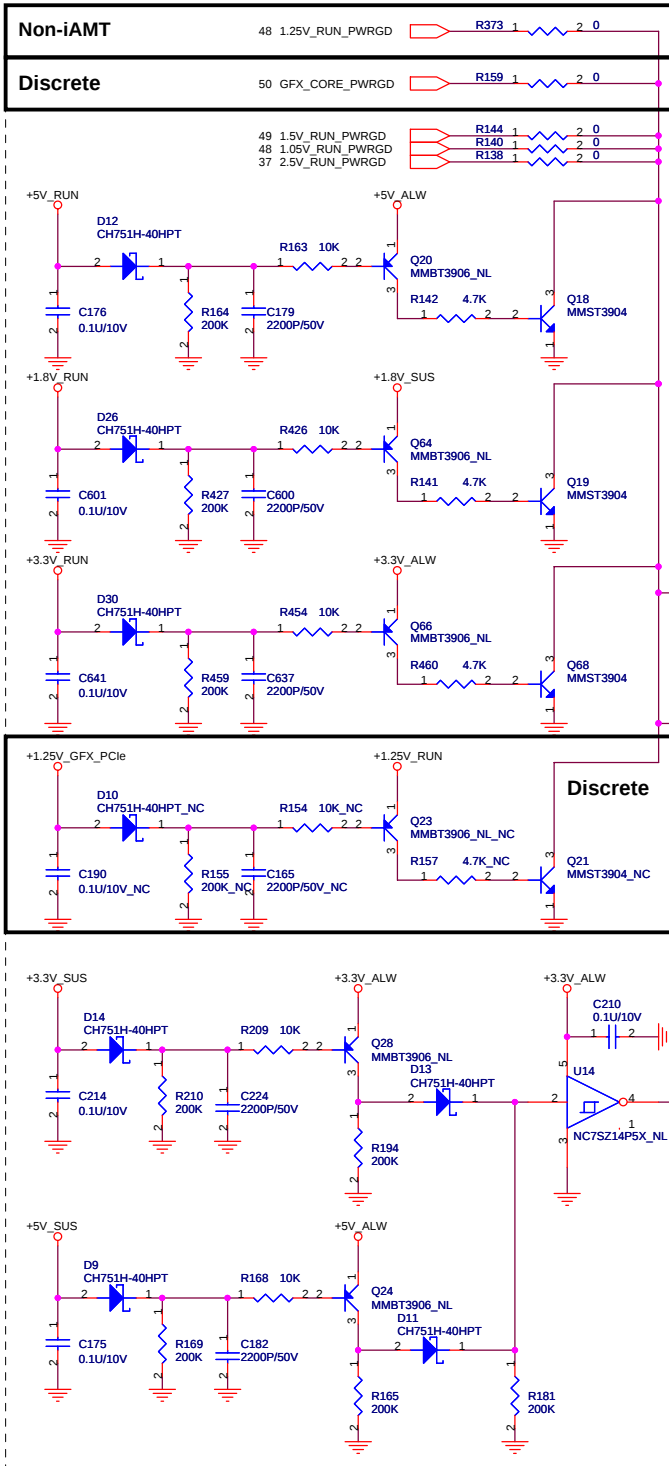
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Date: Thursday, October 26, 2006

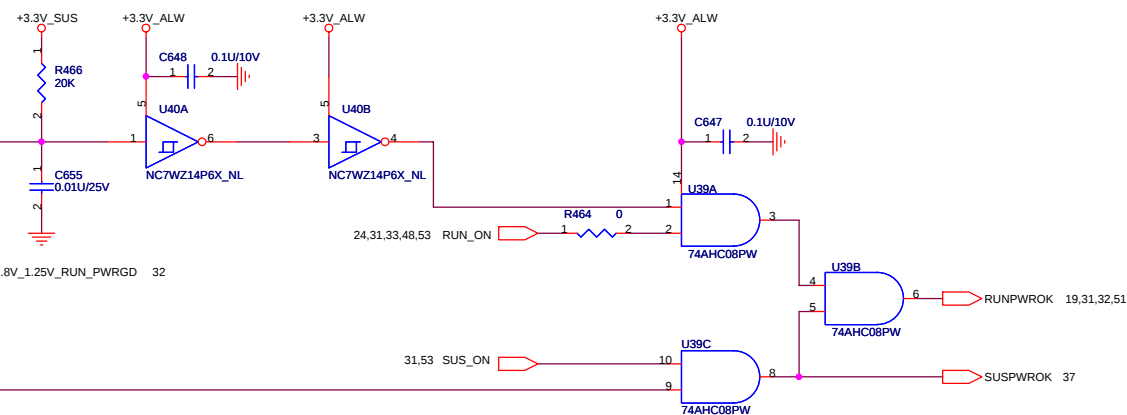
	Rev 2C
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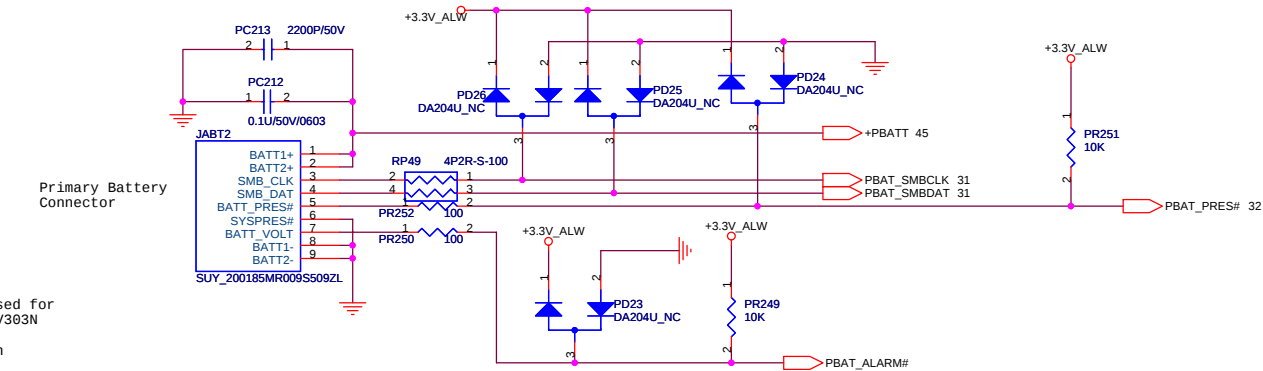
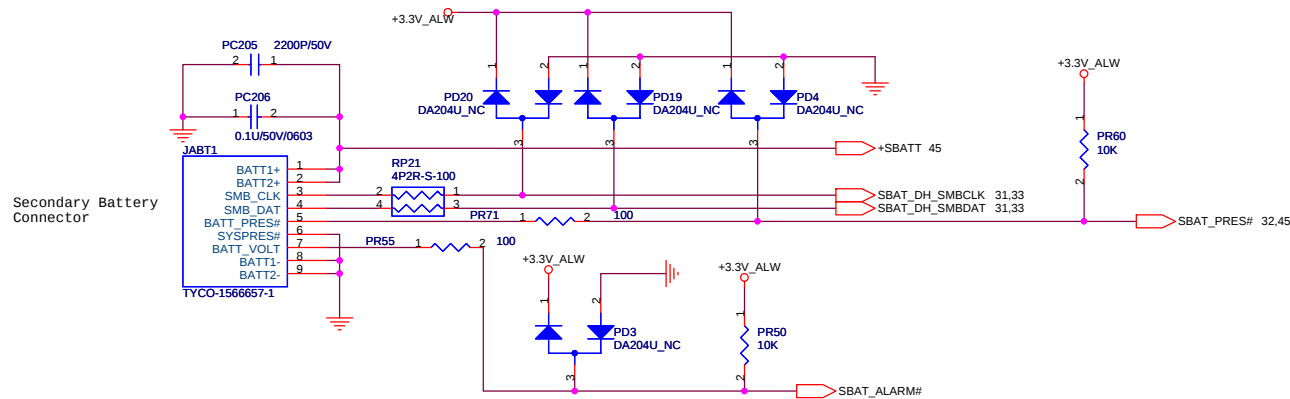
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Keep Away from high speed buses





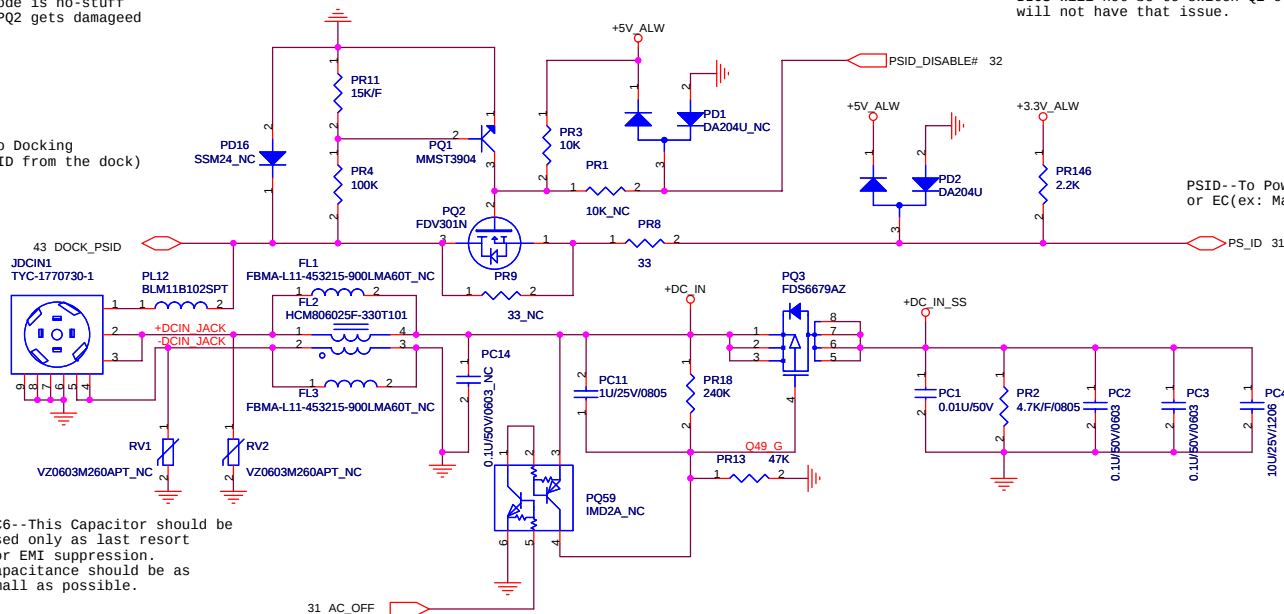
PQ2--Three transistor can be used for PQ2(pin compatible):FDV301N/FDV303N has low Vgs_on w/built-in ESD protection.MMBT100 BJT works in reverse conduction mode.

D12--This diode is no-stuff populate if PQ2 gets damaged by ESD.

PR1--This resistor must be depopulated if FDV301N/FDV303 are used to avoid a 1.36mA constant current drain from +3VALW. Thus, BIOS will not be to switch Q1 off. MMBT100 will not have that issue.

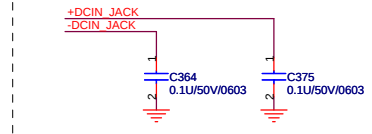
DOCK_PSID--To Docking connector(PSID from the dock)

PSID--To Power Management Controller or EC(ex: Macallan3)



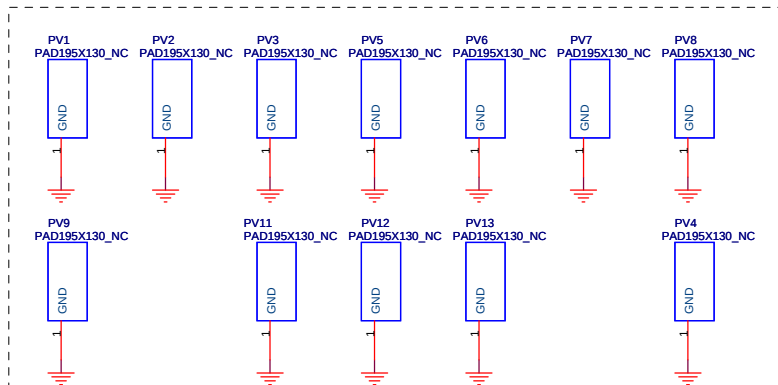
PC6--This Capacitor should be used only as last resort for EMI suppression. Capacitance should be as small as possible.

Reserved for EMI.



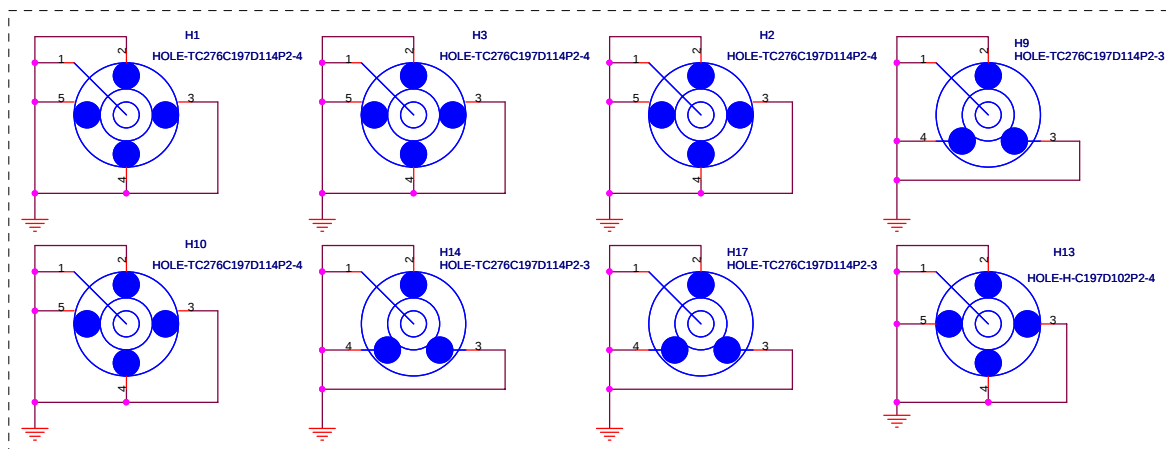
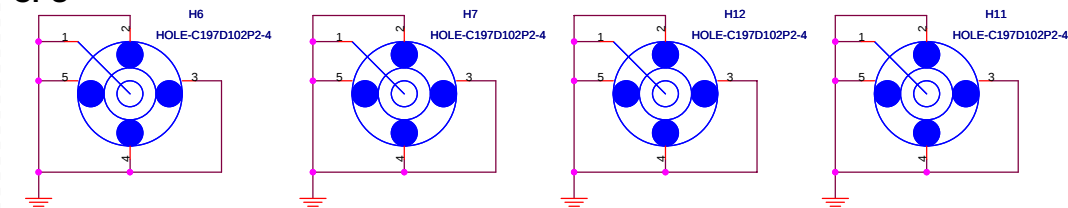
QUANTA COMPUTER

Title			DCIN,BATT CONN.
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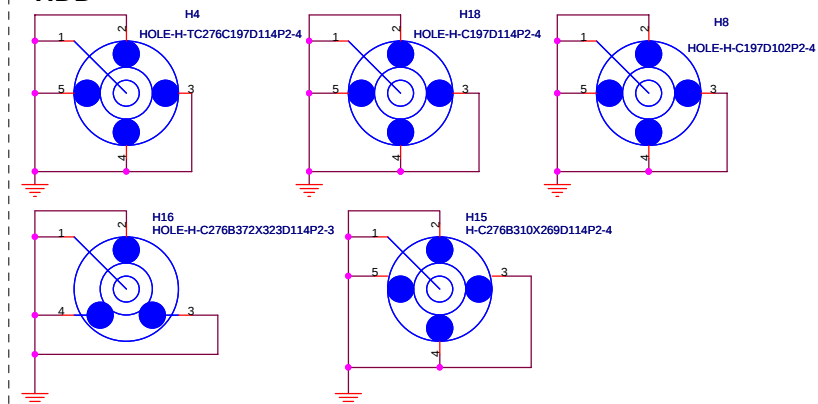


Reserved for EMI.

CPU



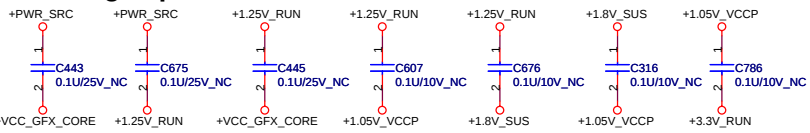
HDD



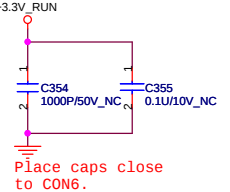
Title			SCREW PAD
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Reserved for EMI.

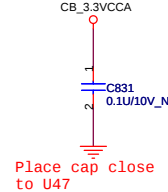
Stitching caps



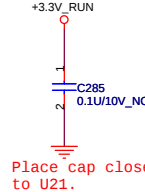
Page 26
SATA (HDD&CD_ROM)



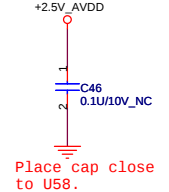
Page 27
PCCARD /CONN



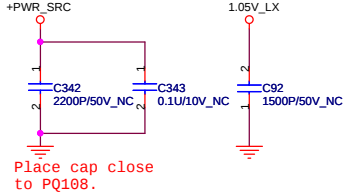
Page 38
Azelia CODEC



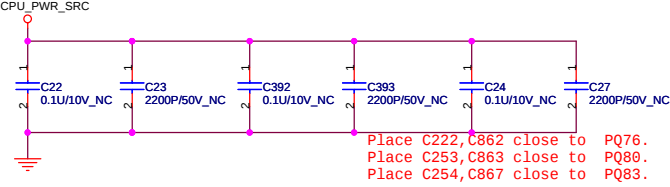
Page 40
LAN(BCM5755M)



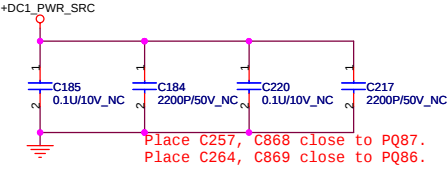
Page 48
1.25V & 1.05V(MAX8778)



Page 51
CPU_MAX8786(3phase)



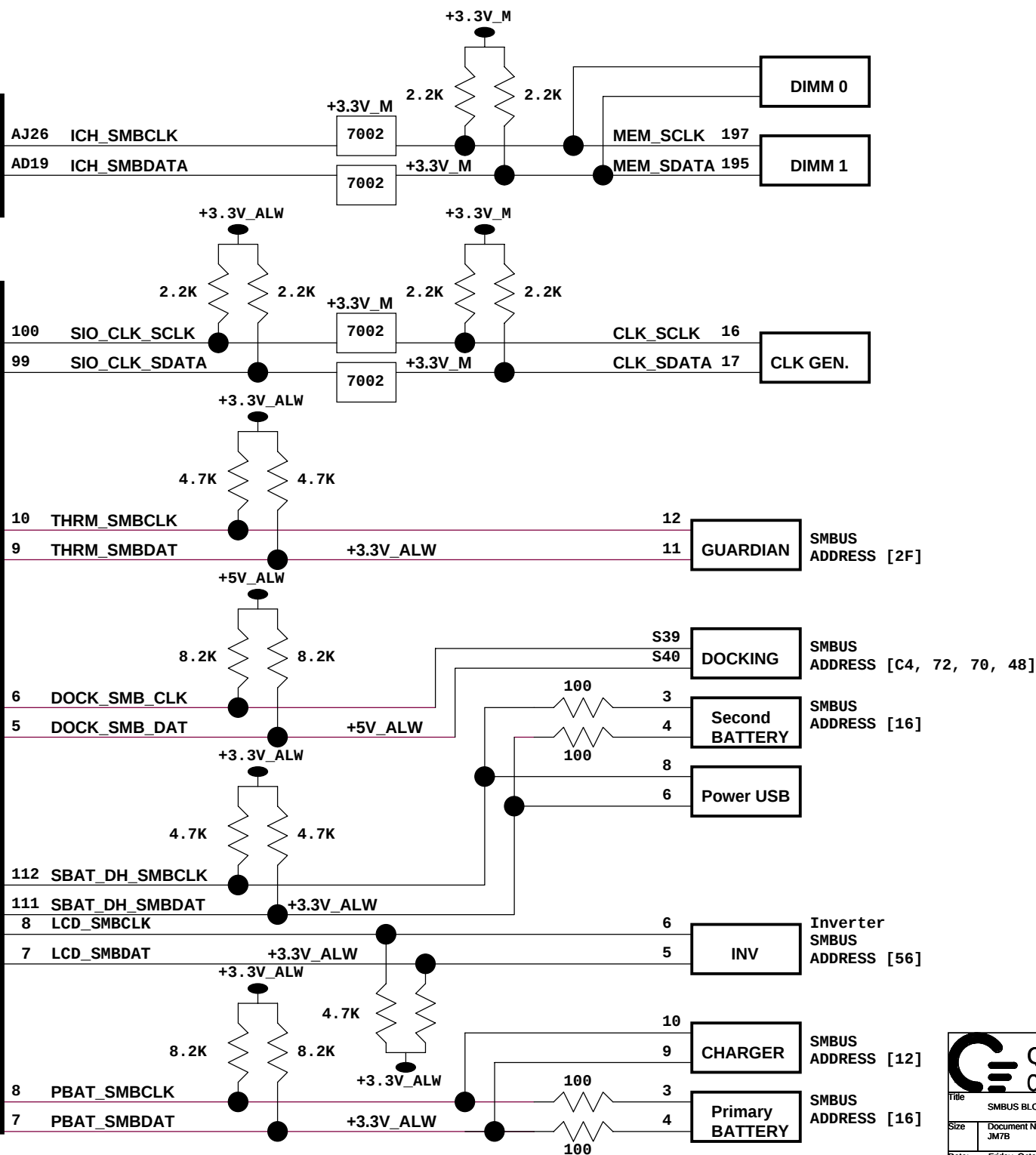
Page 52
D/D Power



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ICH8-M

SIO
MEC5025



QUANTA COMPUTER

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