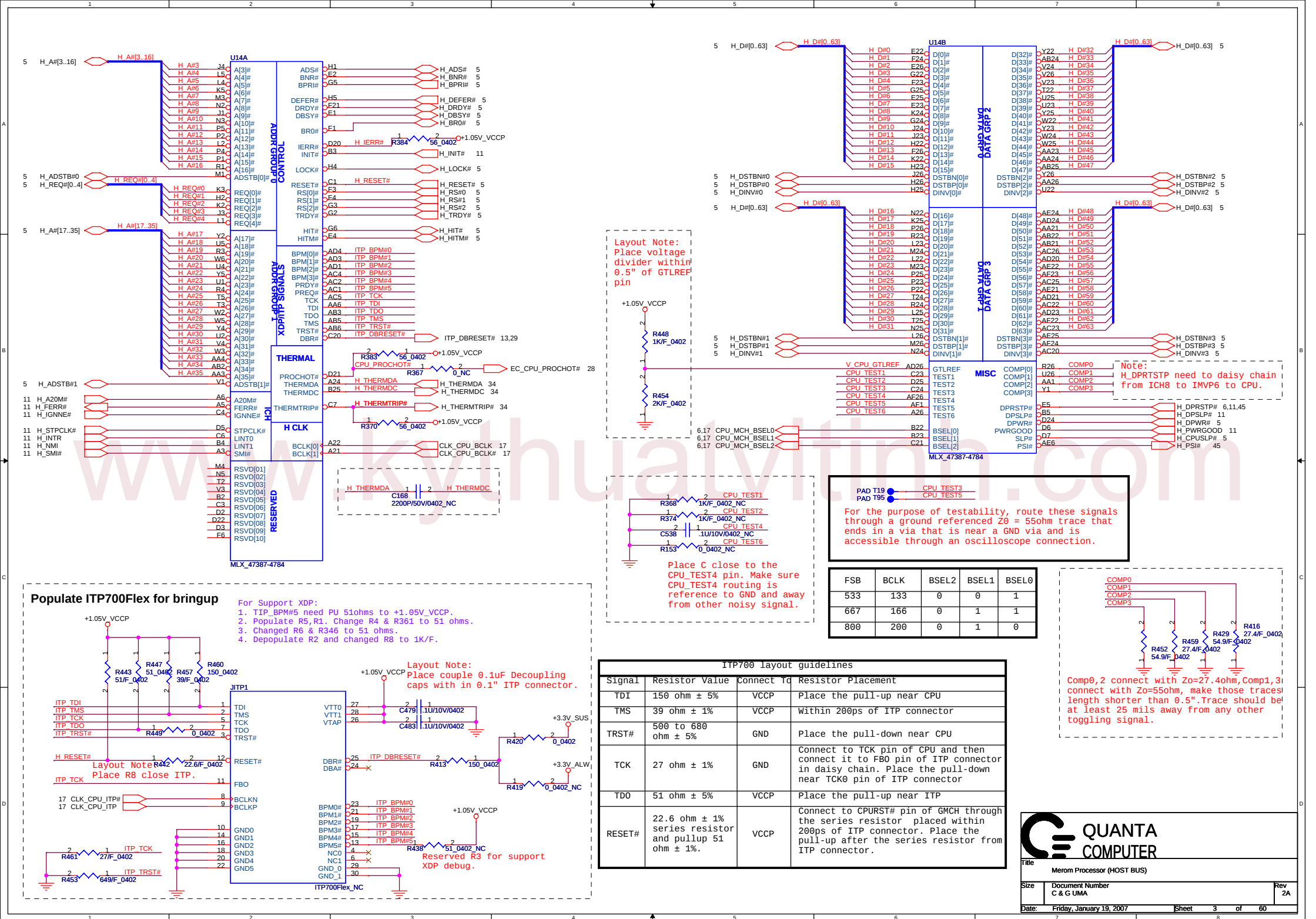
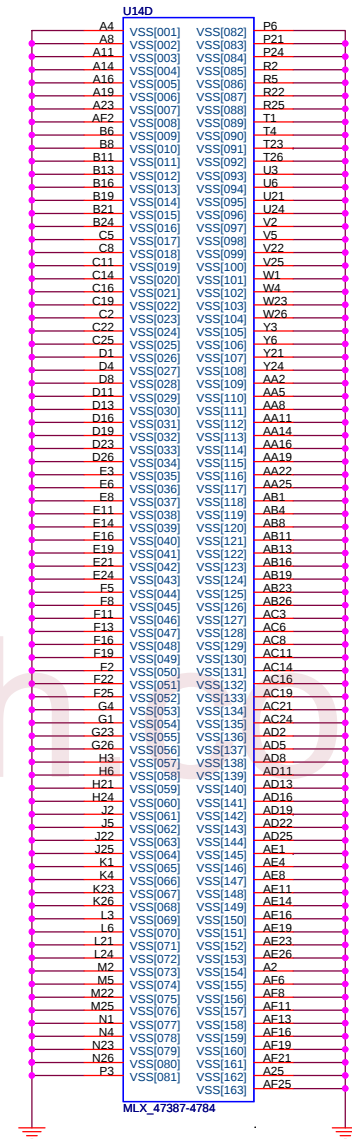
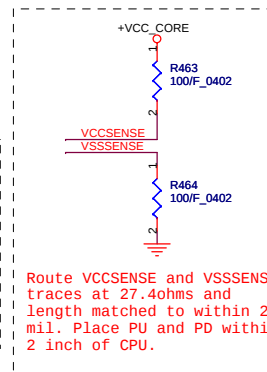
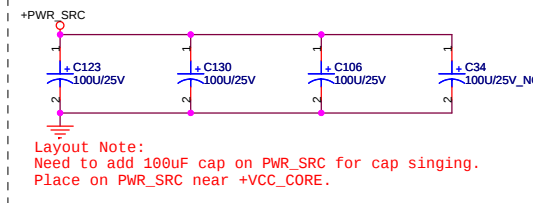
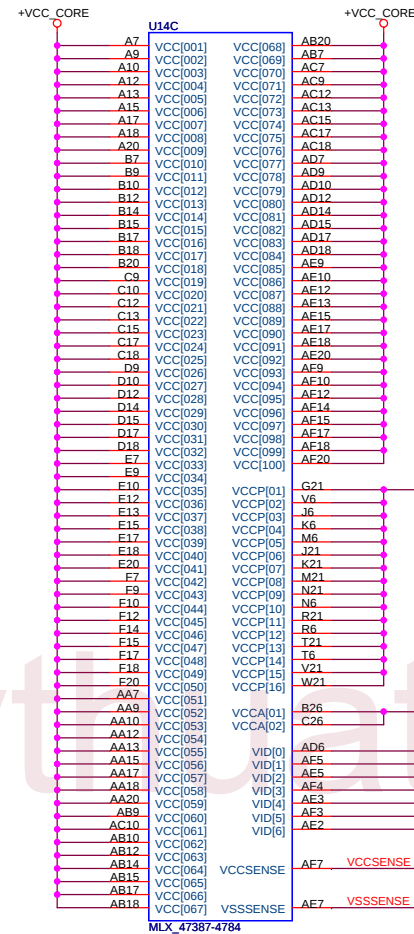
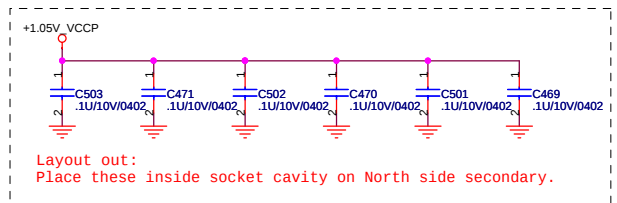
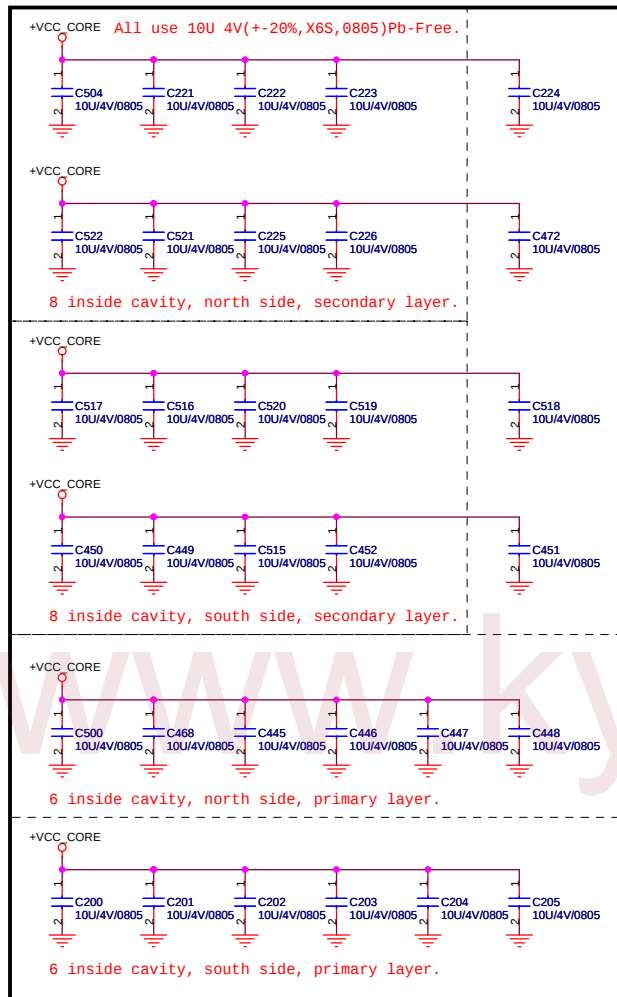


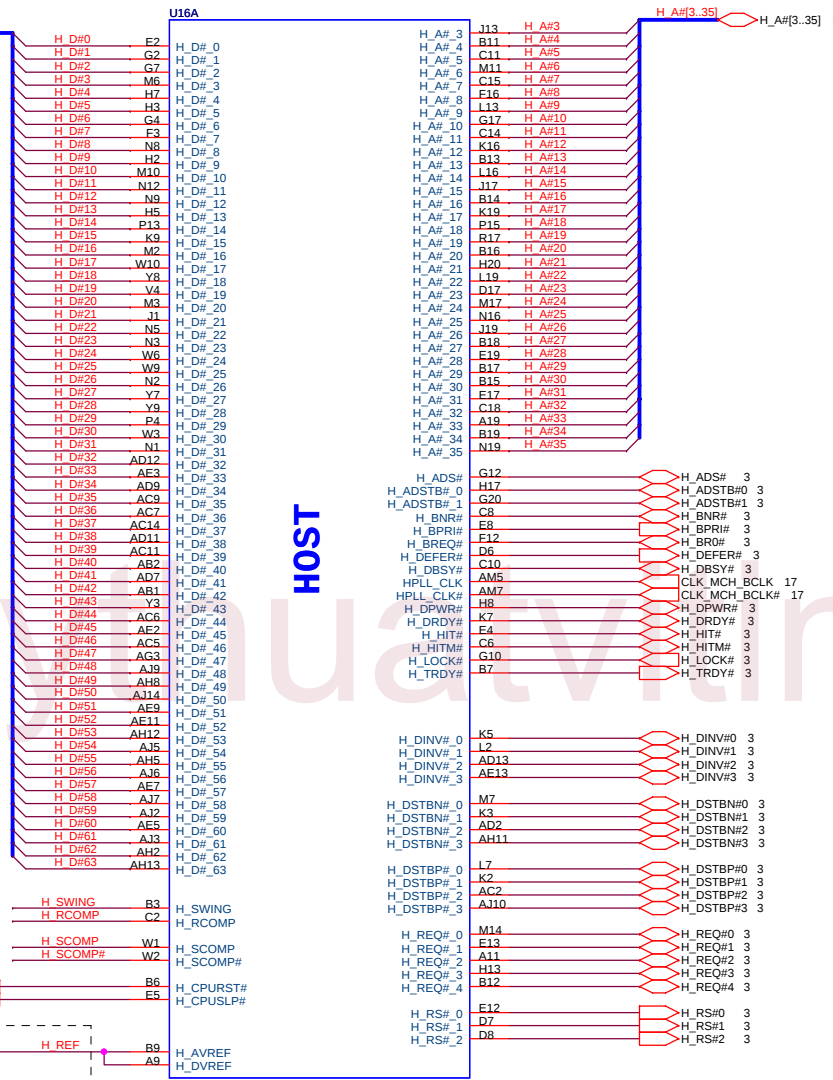
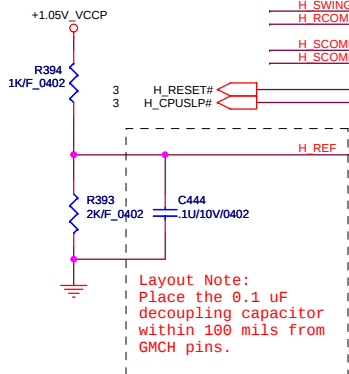
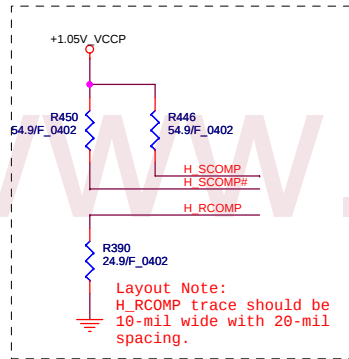
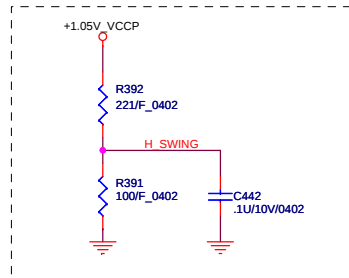
INDEX		
Pg#	Description	DNI LIST
1	Schematic Block Diagram	
2	Front Page	
3-4	Merom	
5-10	Crestline	
11-14	ICH8M	
15-16	DDRII SO-DIMM(200P)	
17	Clock Generator	
18-19	VGA/LVDS/CRT/S-Video	
20	8 in 1 controller	
21	1394 function	
22	8 in 1 connector	
23	SATA & IDE Conn	
24-25	Mini Card (WLAN/WPAN/WWAN)	
26	Express Card + MDC BTB Connector	
27	USB Conn.	
28	SIO (MEC5025)	
29	SIO (MEC5011)	
30	Flash / RTC	
31	TP/KB/Media/CIR Conn.	
32-33	Audio CODEC(STAC9200)/Phone Jack	
34	FAN & Thermal	
35-36	LOM (BCM4401)	
37	Dash/LED/BT Conn.	
38	System reset CKT.	
39	RUN Power Switch	
40	Battery Charger	
41	DCIN/Batt Conn.	
42	1.25V,1.8V,0.9V	
43	1.5VSUS,1.05V(VTT)	
44	D/D Power	
45	CPU_ISL6260(3phase)	
46	EMI CAP & Screw Hole.	

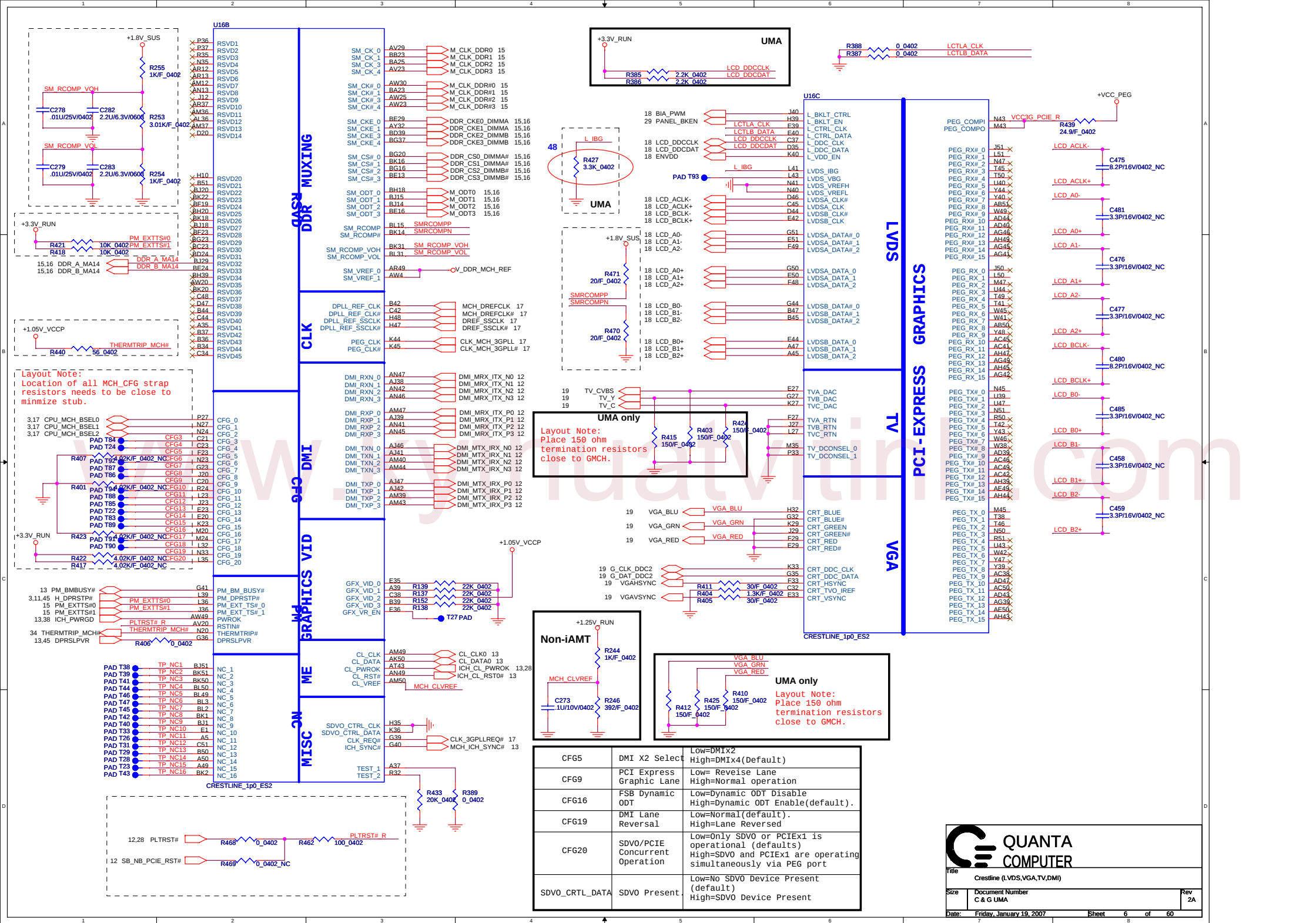
Power & Ground			
Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (19V)	
PBATT+		MAIN BATTERY + (10~17V)	
PBATT+		SECOND BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~19V)	
RTC_PWR3_3V		RTC & +3.3V_RTC_LDO(3.3V)	
+VCC_CORE		CPU CORE POWER (1.5V)	RUNPWROK
+15V_ALW		LARGE POWER (15V)	SUS_ON
+3.3V_RUN		SLP_S3# CTRLD POWER	RUN_ON
+3.3V_SUS		SLP_S5# CTRLD POWER	SUS_ENABLE
+3.3V_ALW		8051 POWER (3.3V)	ALWON/THERM_STP#
+5V_RUN		SLP_S3# CTRLD POWER	RUN_ON
+5V_SUS		SLP_S5# CTRLD POWER	SUS_ON
+5V_HDD		HDD POWER (5V)	+5V_RUN
+5V_MOD		MODULE POWER (5V)	HDD_EN
+5V_ALW		LCD/CHARGE POWER (5V)	
+VDDA		AUDIO ANALOG POWER (5V)	AUDIO_AVDD_ON
+1.5V_RUN		CALISTOGA/ICH7 POWER	RUN_ON
+1.05V_VCCP		CPU/CALISTOGA/ICH7 POWER	RUN_ON
+1_8V_SUS		SODIMM POWER	SUSPWROK_5V
+1.8V_RUN		SDVO POWER	RUN_ON
+0.9V_DDR_VTT		SODIMM POWER	RUN_ON
+3.3V_LAN		LAN POWER	AUX_EN
 GND	ALL PAGES	DIGITAL GROUND	
 AGND_ISL6260		CPU GND	
 AGND_TPS51120		DC/DC POWER GND	
 AGND1		VTT POWER GND	
 AGND2		VTT POWER GND	
 8731AGND		CHARGER GND	

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Title Index, DNI, Power & Ground		
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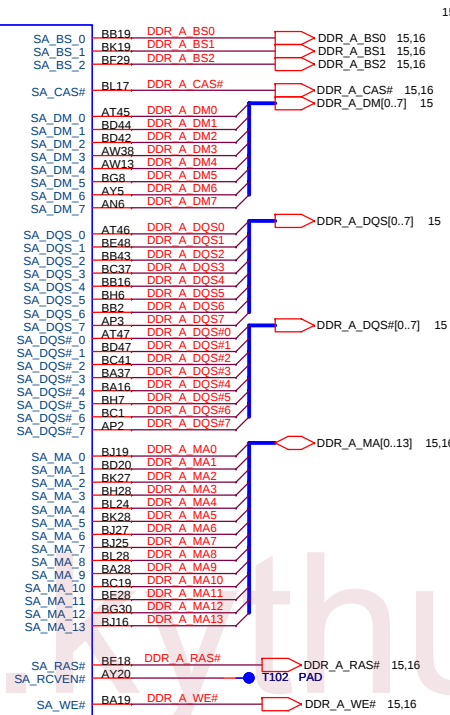
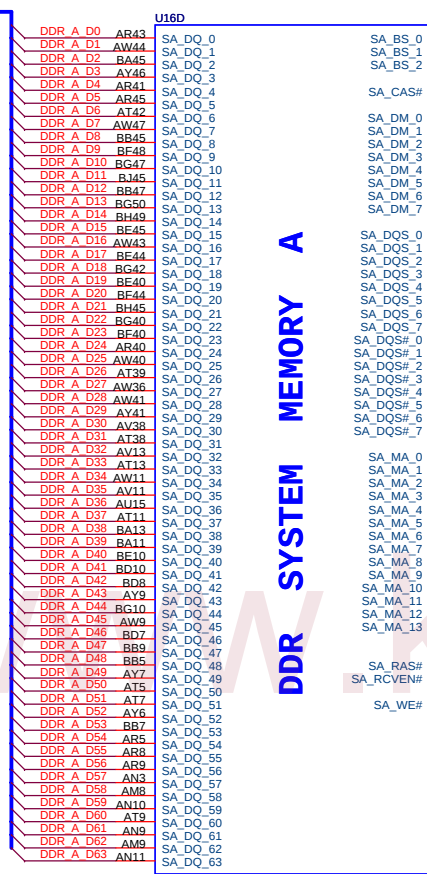




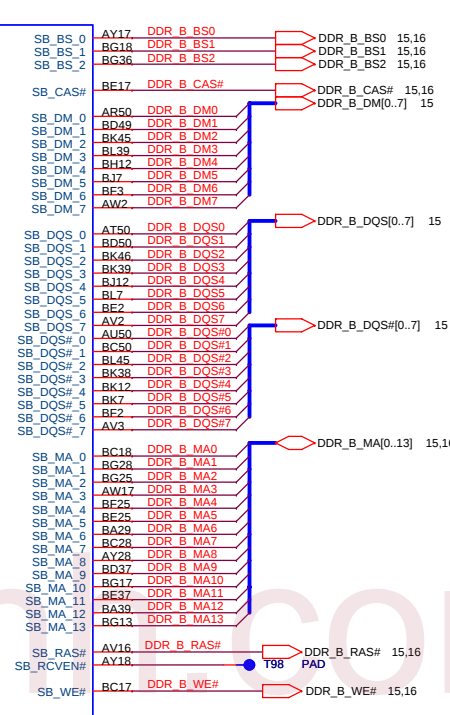
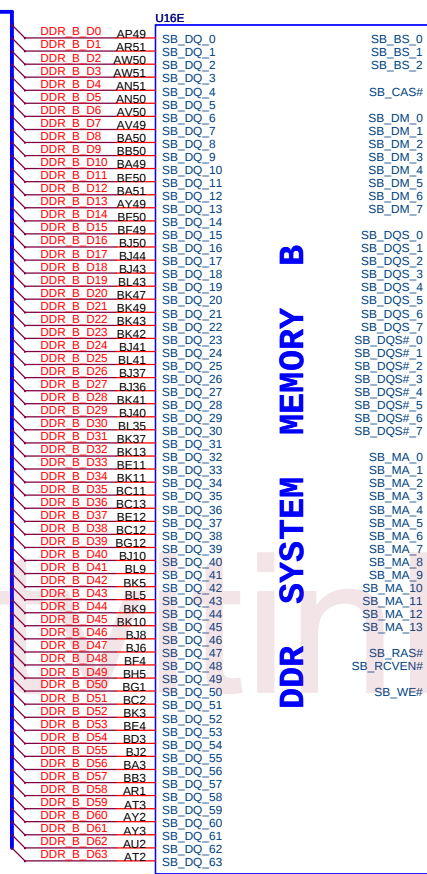


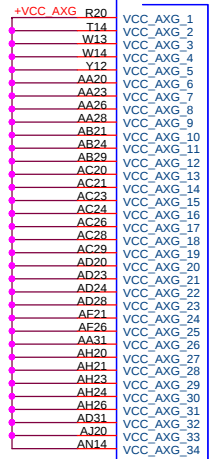
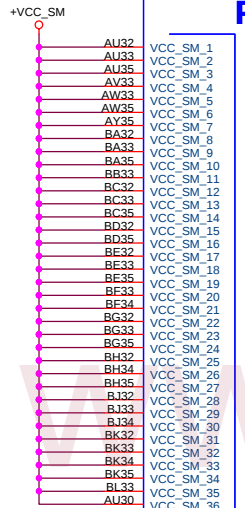
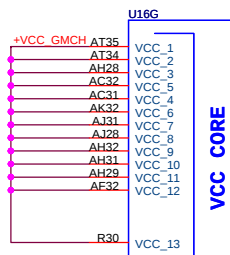


15 DDR_A_D[0..63]



15 DDR_B_D[0..63]





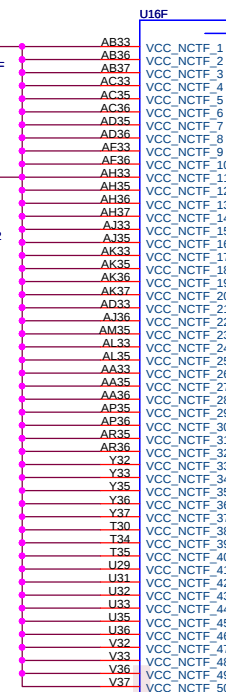
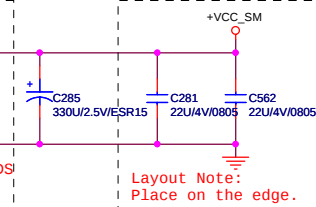
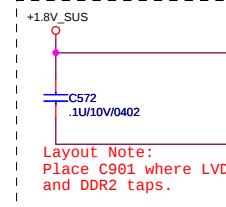
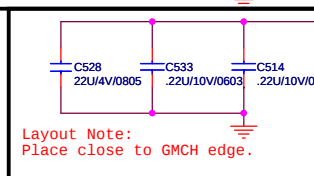
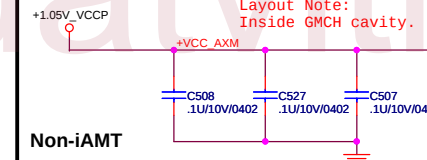
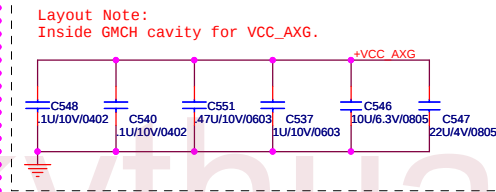
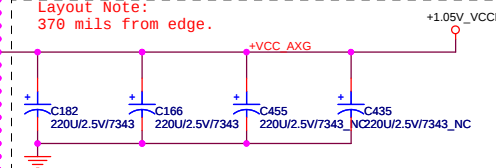
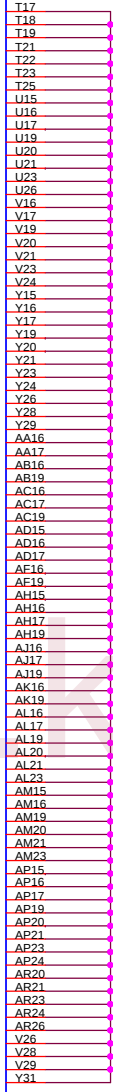
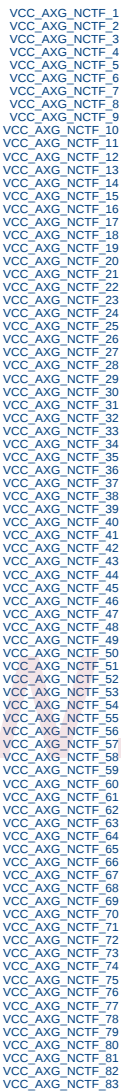
POWER

VCC SM

VCC GFX NCTF

VCC GFX

VCC SM LF



POWER

VCC AXM

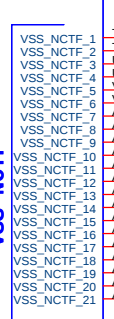
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VCC SM LF



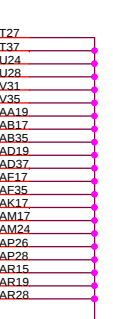
VSS SCB

VSS AXM

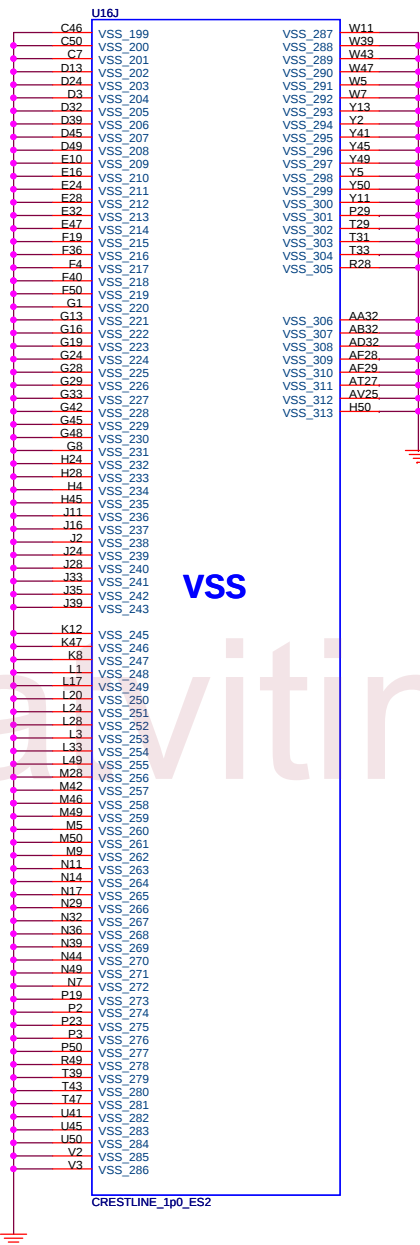
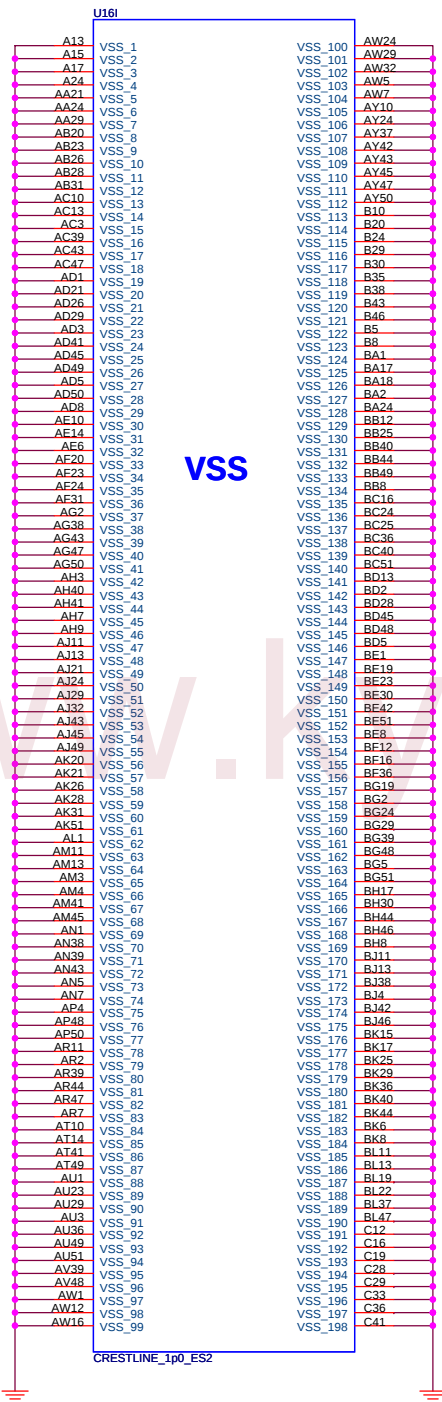


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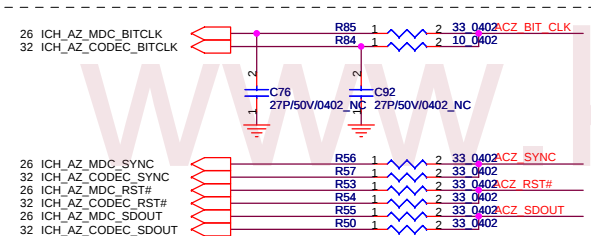
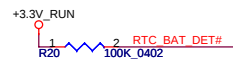
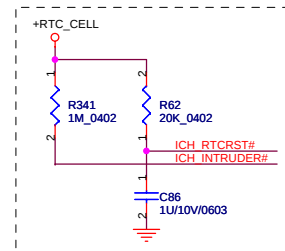
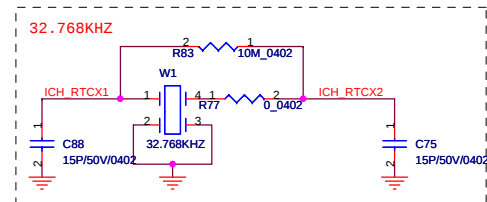
VSS AXM



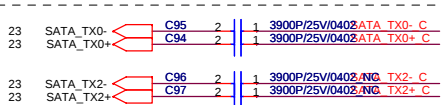
Title Crestline (VCC,NCTF)		
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Title		
Crestline (VSS)		
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Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R292, R286, R283 & R289 should equal distance to the T split trace point as R291, R285, R284 & R290 respectively. Basically, keep the same distance from T for all series termination resistors.



Populate C96, C97 (P/N:CH23904KB13) for Gilligan

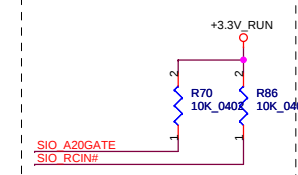
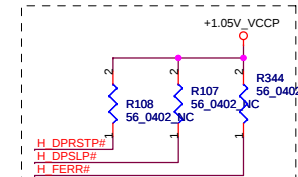
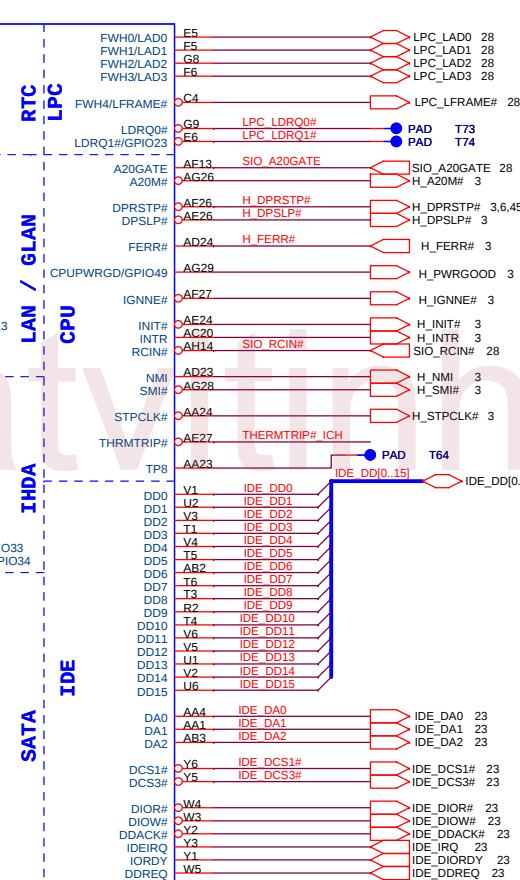
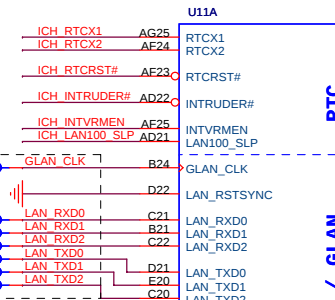
Distance between the ICH-8 M and cap on the "p" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.

Place within 500mils of ICH8 ball

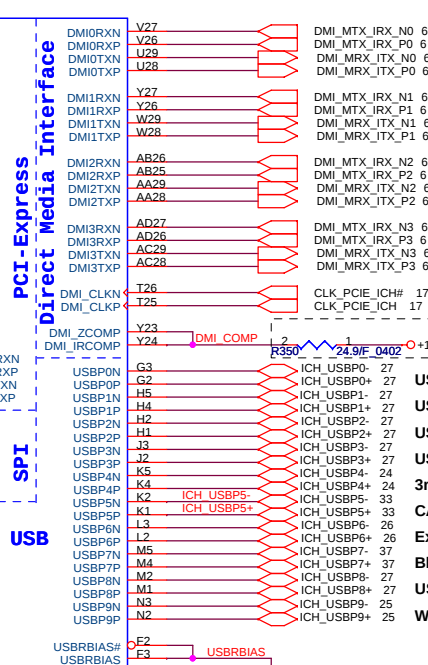
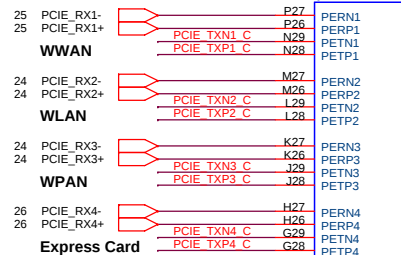
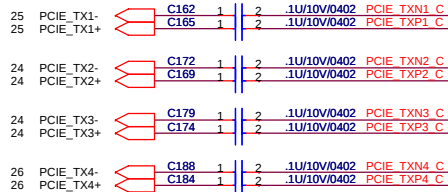
XOR Chain Entrance Strap		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)		
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)	

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)		
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)	

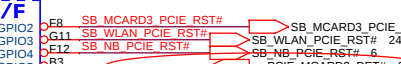
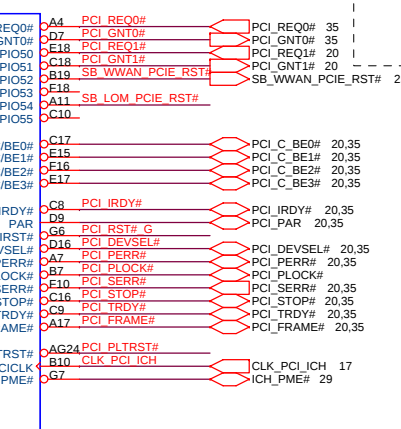
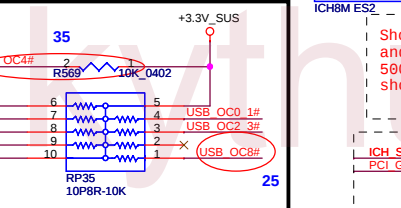
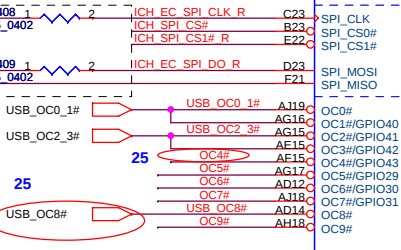
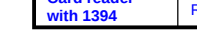
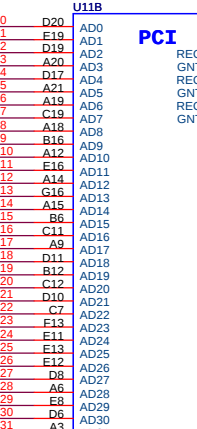
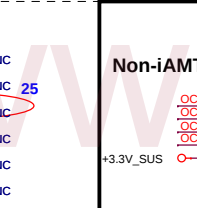
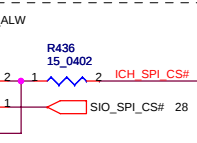
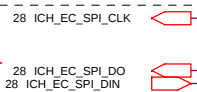


Place TX DC blocking caps close ICH8.



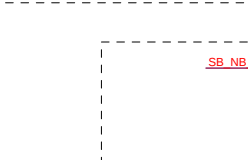
Place within 500mils of ICH8

Layout Note:
Place R288, R688 and R282
within 500 mils from ICH.



Short F2 and F3 at the package
and keep length to less than
500mils. Trace Impedance
should be 60ohms +/- 15%.

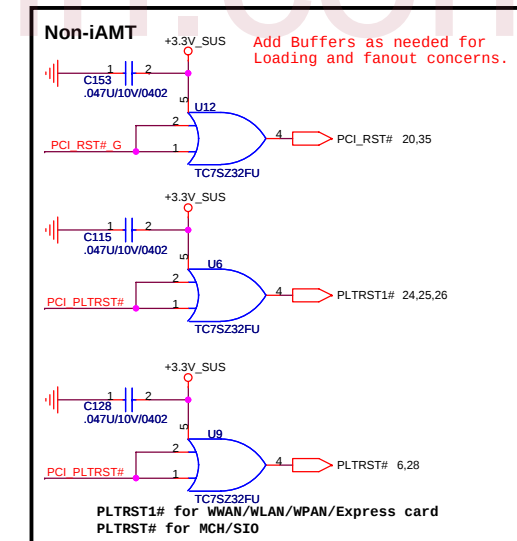
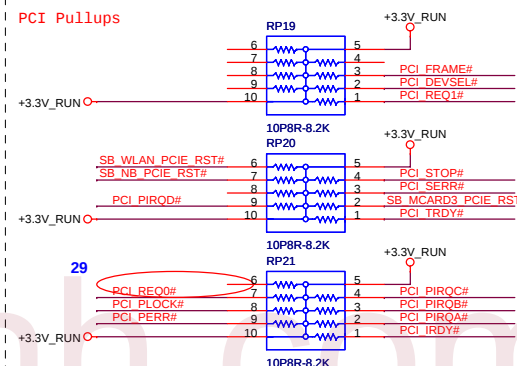
	Boot BIOS Strap
LPC	11
PCI	10
SPI	01



	A16 away override strap.
PCI_GNT3#	Low = A16 swap override enabled. High = Default.



Reserved for EMI.
Place resistor and cap
close to ICH.



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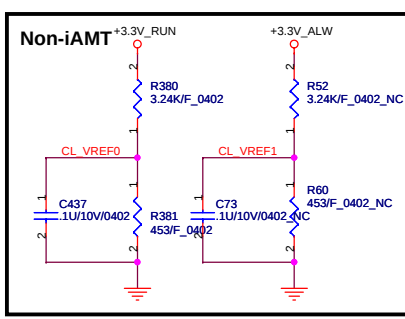
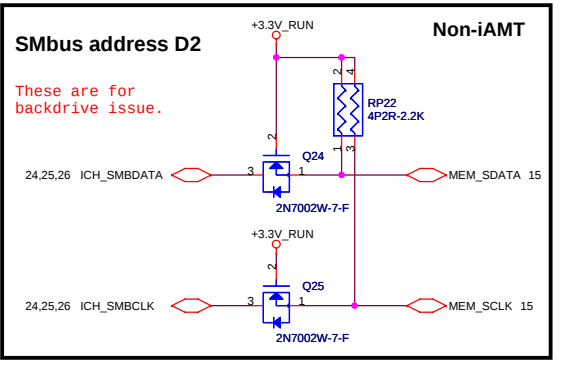
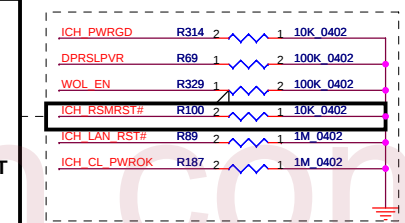
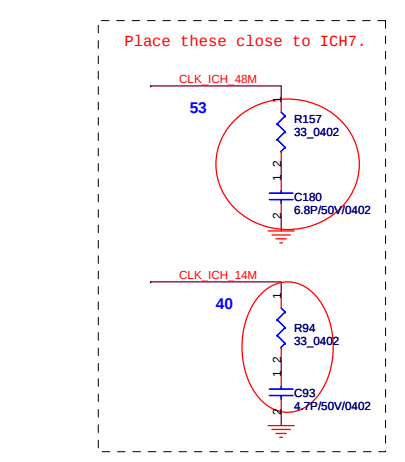
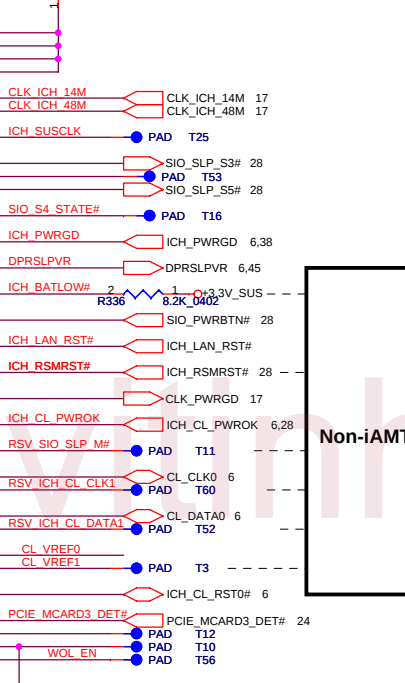
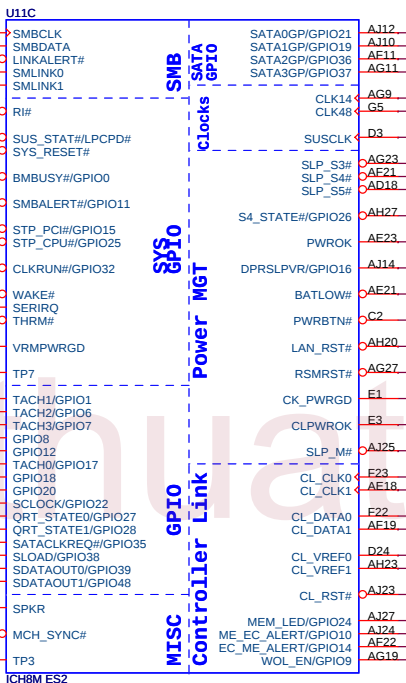
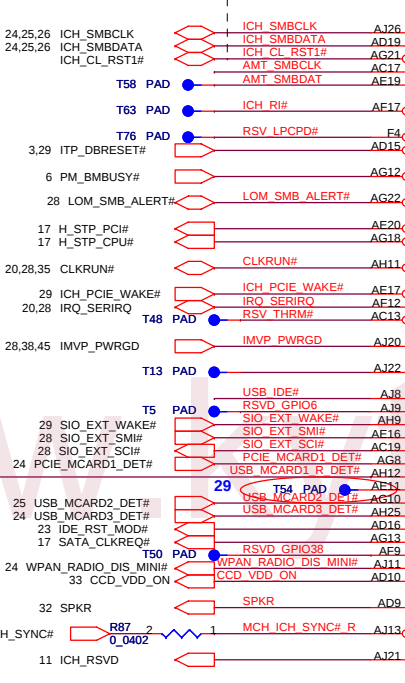
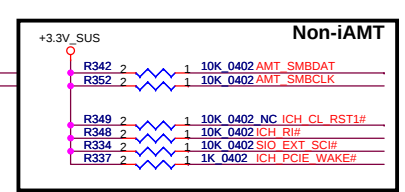
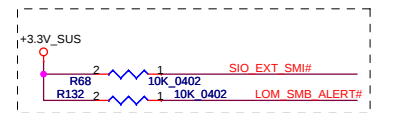
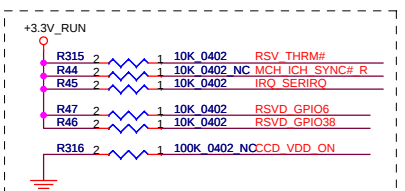
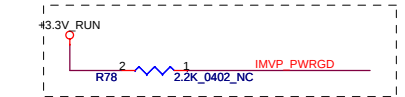
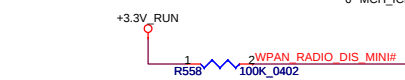
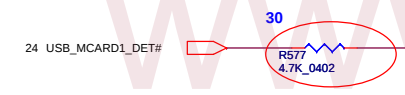
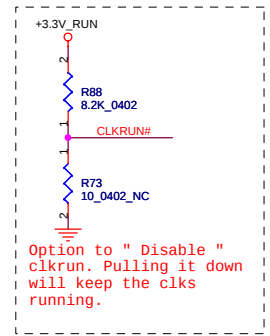
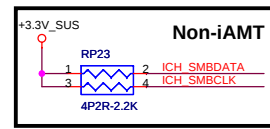
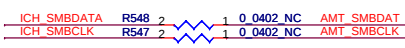
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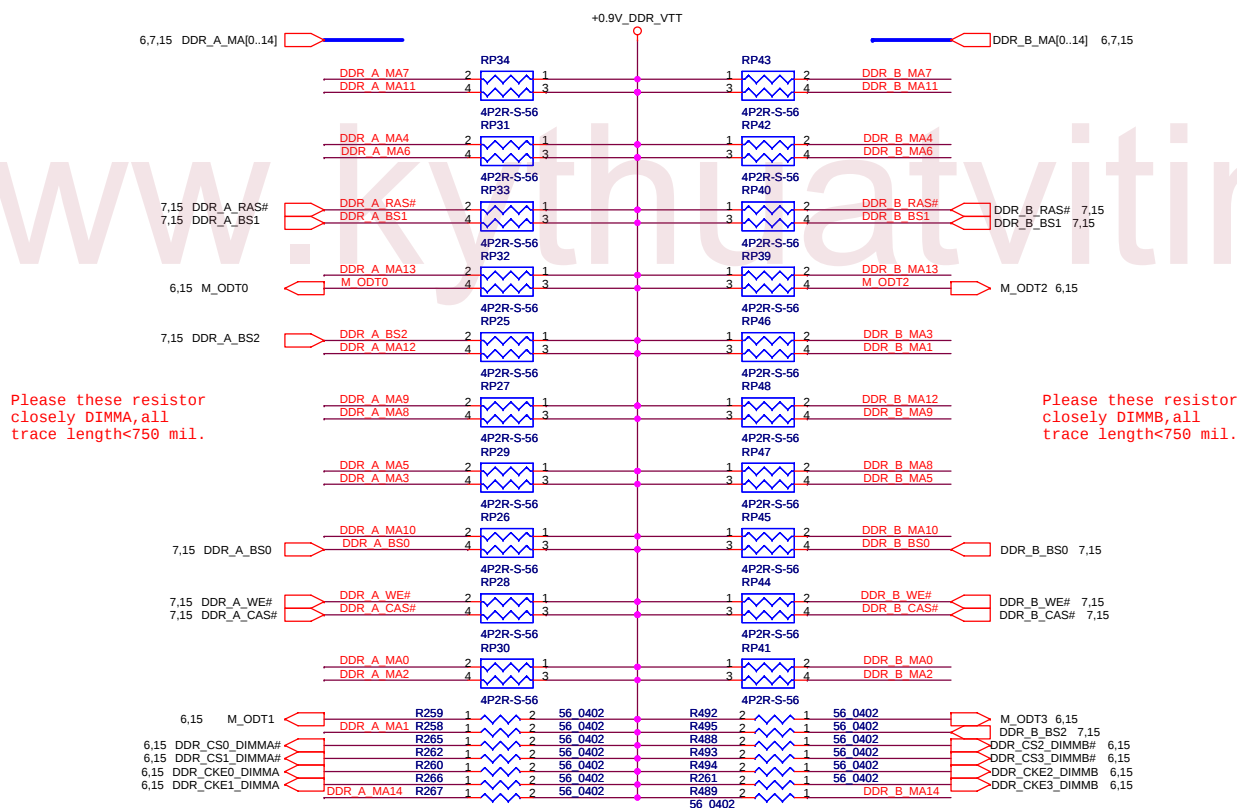
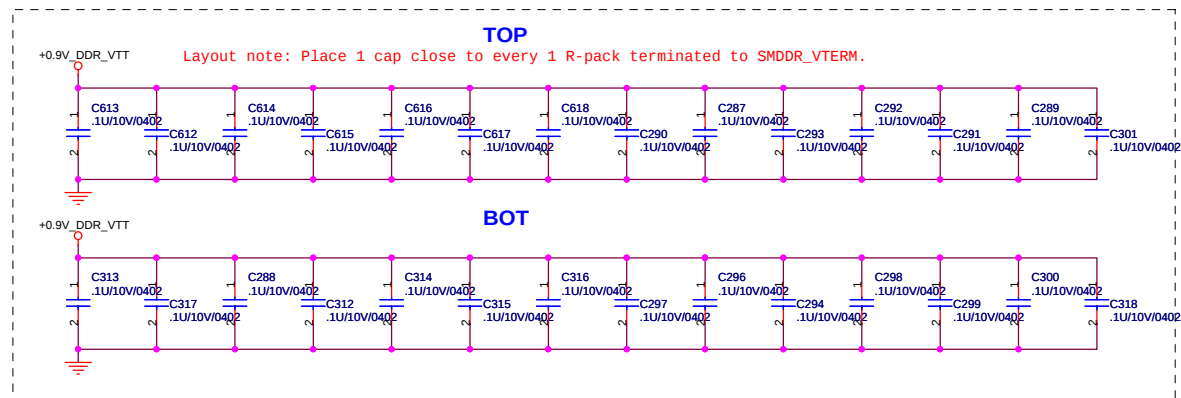
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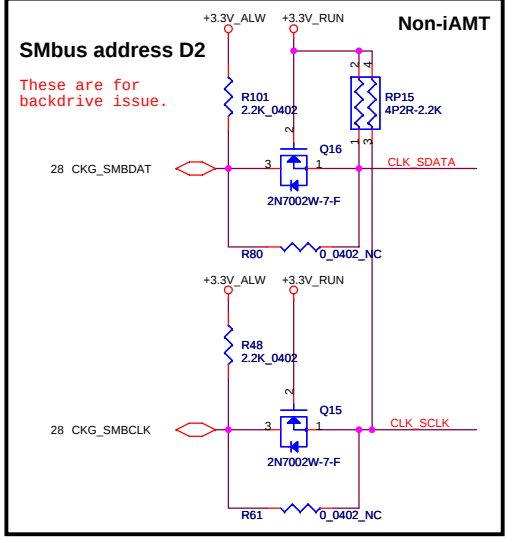
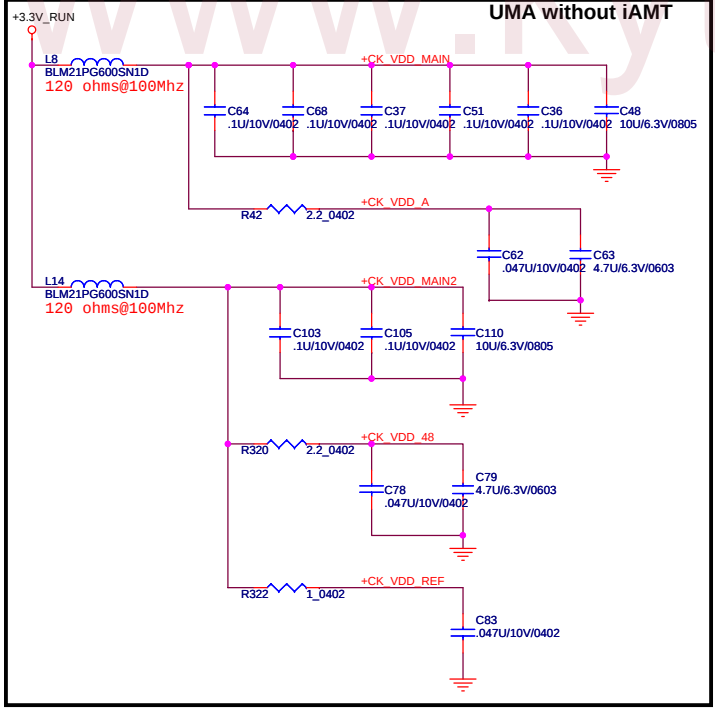
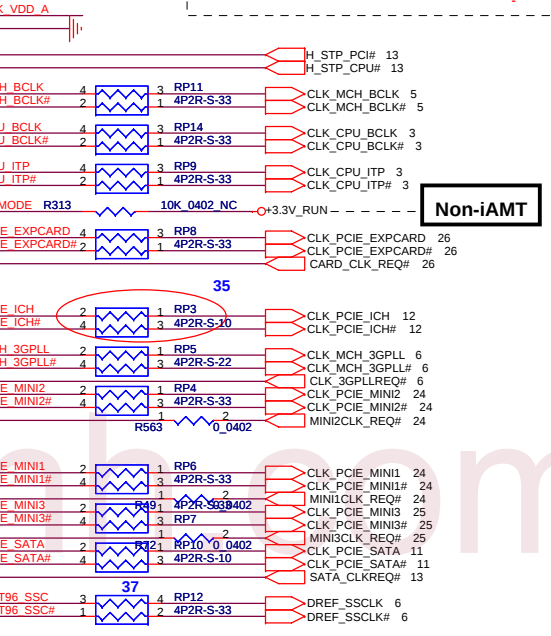
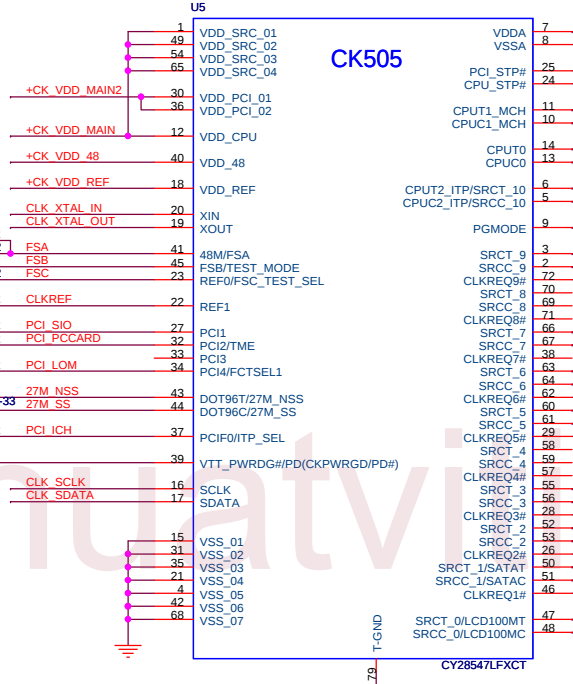
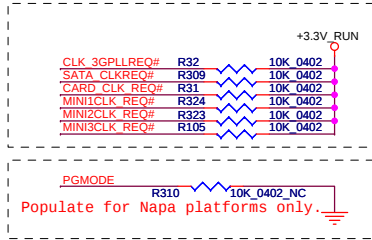
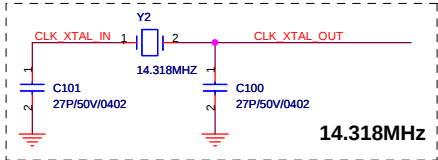
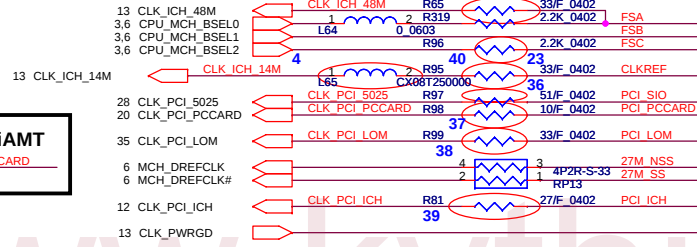
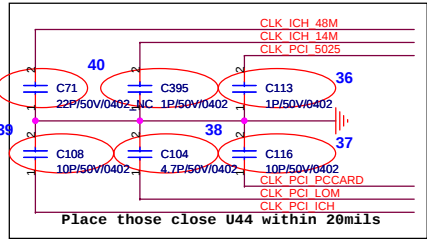
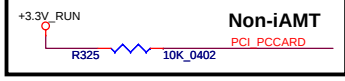
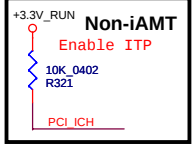
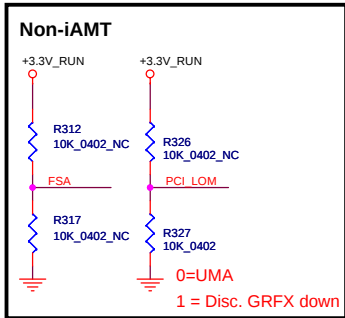
Date: Friday, January 19, 2007

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Rev: 2A







FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI_LOM = FCTSEL1

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRCT0	SRCC0

QUANTA COMPUTER

Title: CLOCK GENERATOR

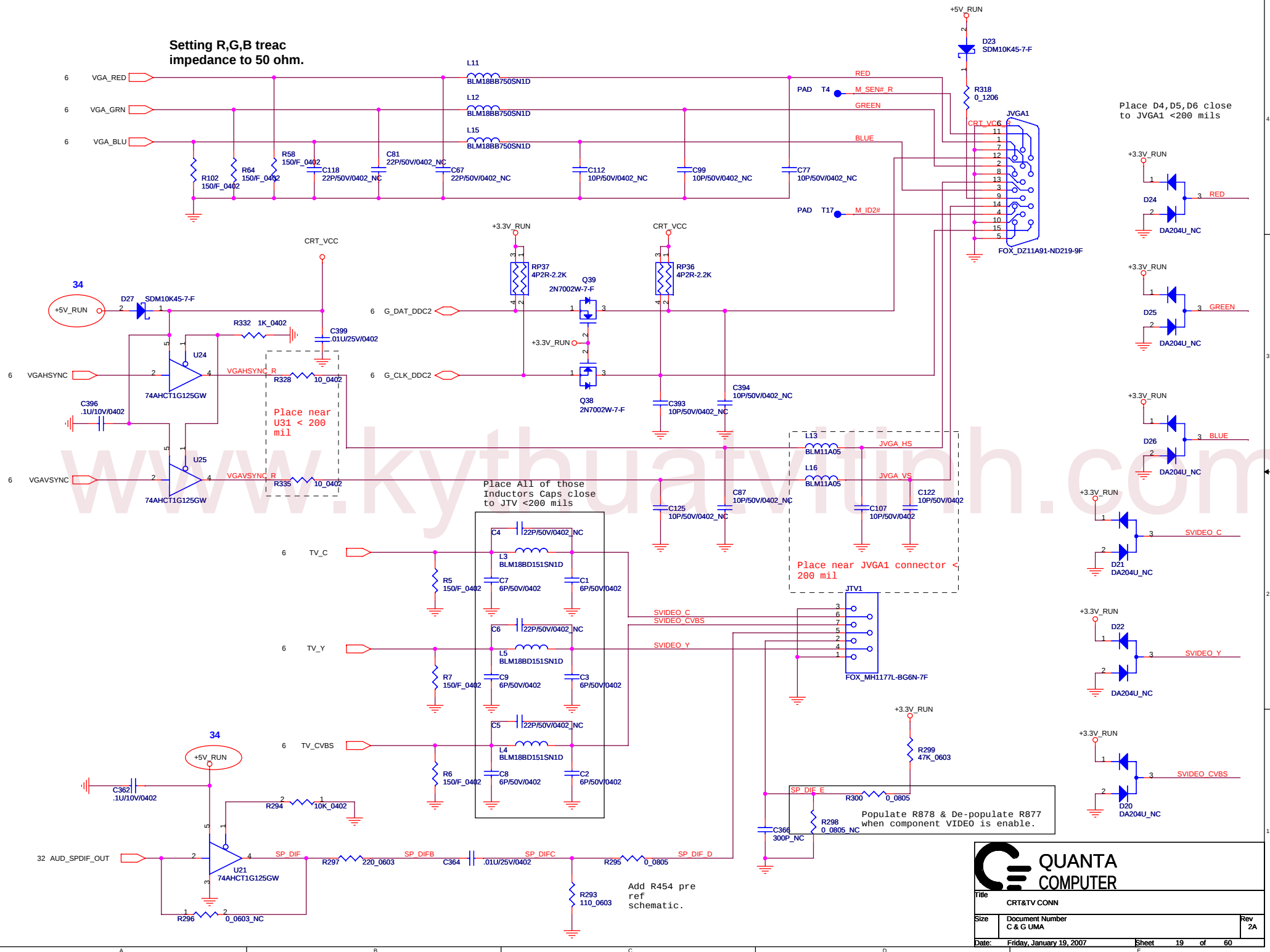
Size: Document Number C & G UMA

Date: Friday, January 19, 2007

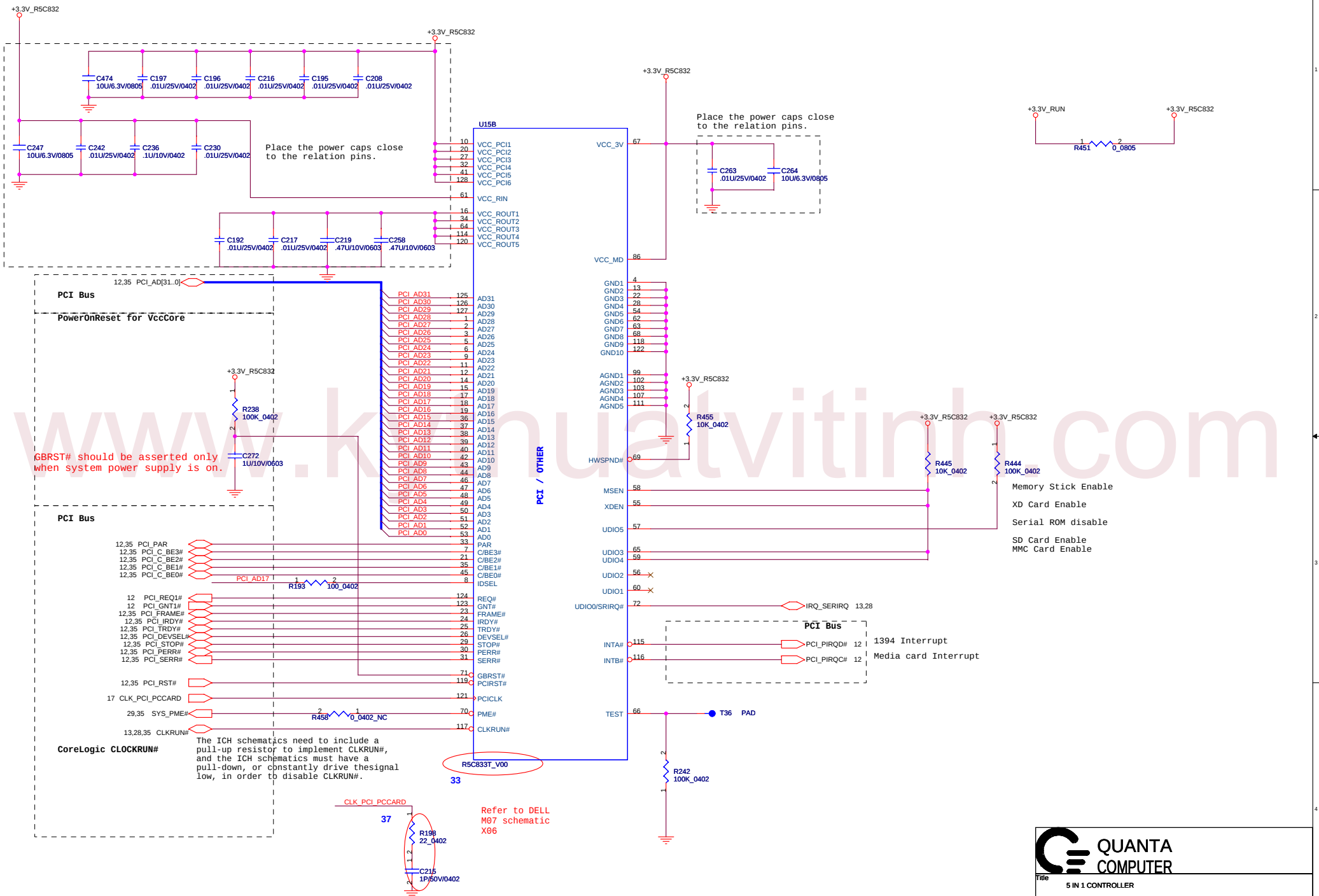
Sheet: 17 of 60

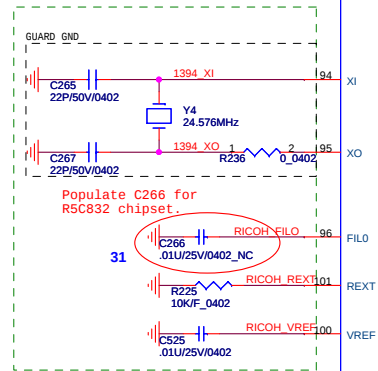
Rev: 2A

Setting R,G,B treac
impedance to 50 ohm.

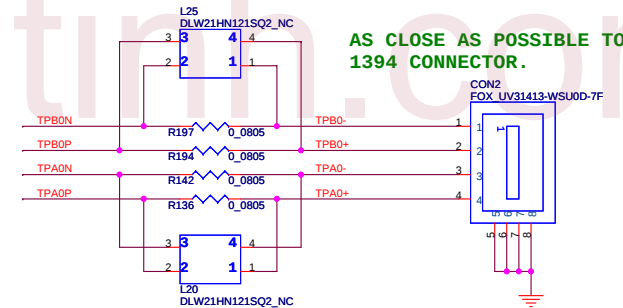
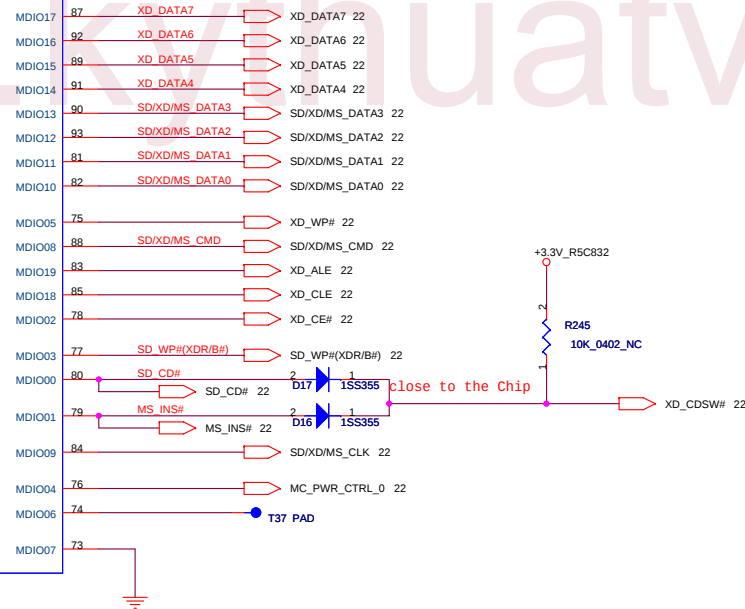


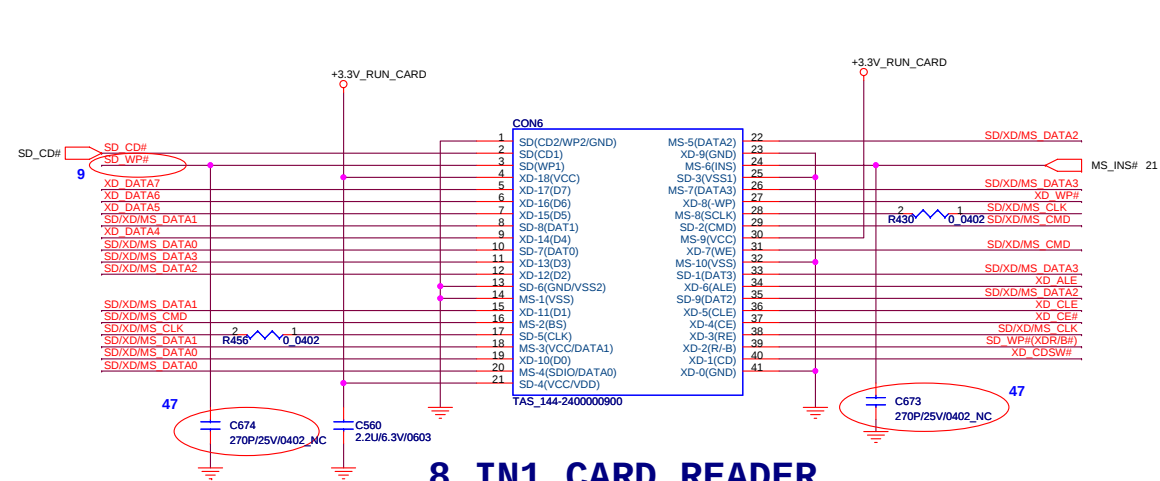
Title			CRT&TV CONN
Size			Document Number
			C & G UMA
			Rev 2A
Date:	Friday, January 19, 2007	Sheet	19 of 60



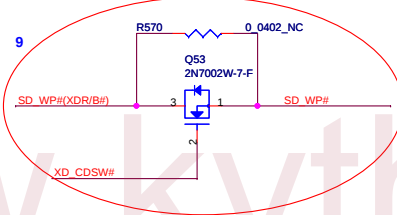


IEEE1394/SD

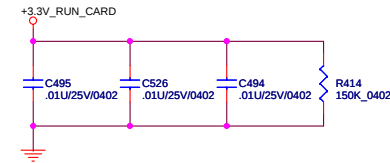
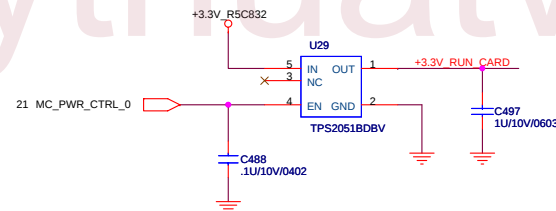




8 IN1 CARD READER



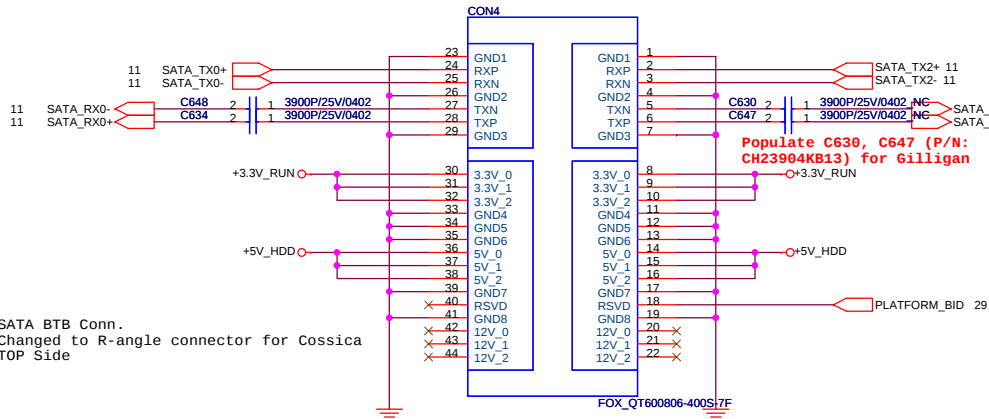
- 21 XD_CDSW#
- 21 SD_WP#(XDR/B#)
- 21 XD_DATA7
- 21 XD_DATA6
- 21 XD_DATA5
- 21 XD_DATA4
- 21 SD/XD/MS_DATA3
- 21 SD/XD/MS_DATA2
- 21 SD/XD/MS_DATA1
- 21 SD/XD/MS_DATA0
- 21 SD/XD/MS_CMD
- 21 XD_WP#
- 21 XD_ALE
- 21 XD_CLE
- 21 XD_CE#
- 21 SD/XD/MS_CLK



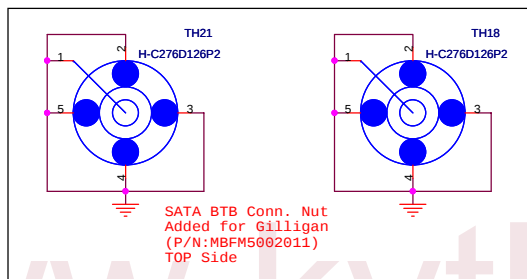
QUANTA
COMPUTER

Title			CARD READER CONN
Size	Document Number	Rev	
	C & G UMA	2A	
Date:	Thursday, January 25, 2007	Sheet	22 of 60

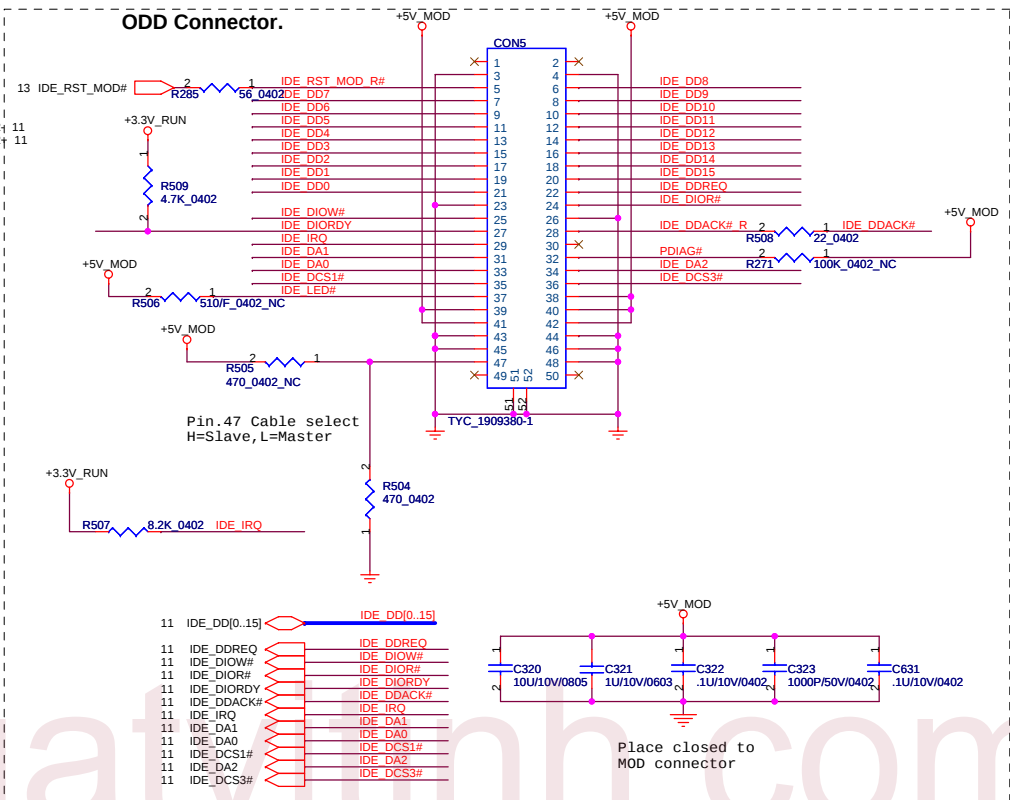
SATA 1 & 2 Connector. Change CON4 P/N to DFHS44FS611 for Gilligan.



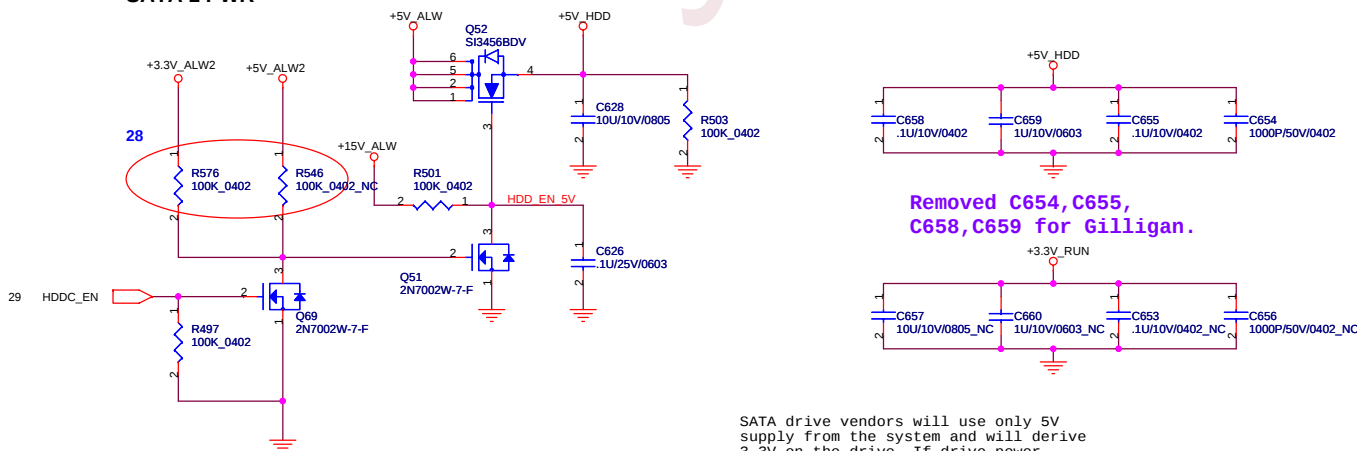
SATA BTB Conn.
Changed to R-angle connector for Cossica
TOP Side



ODD Connector.



SATA 1 PWR

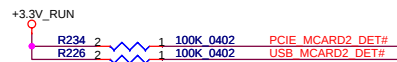


SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

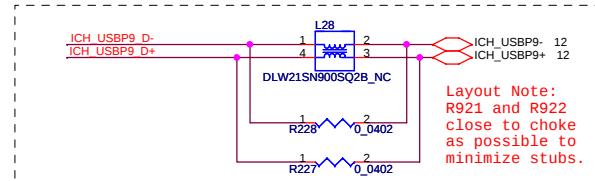
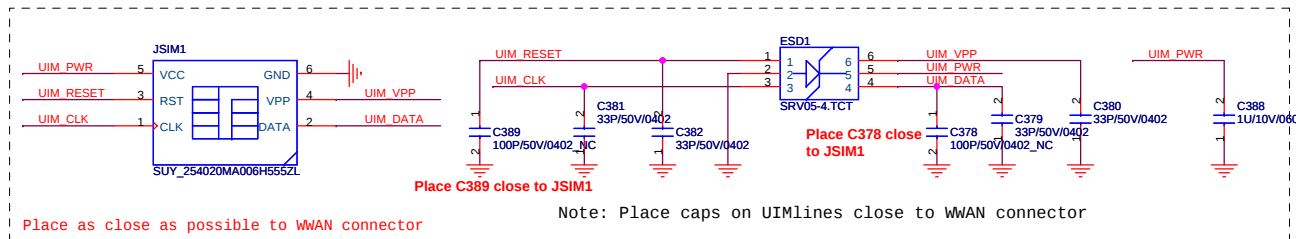
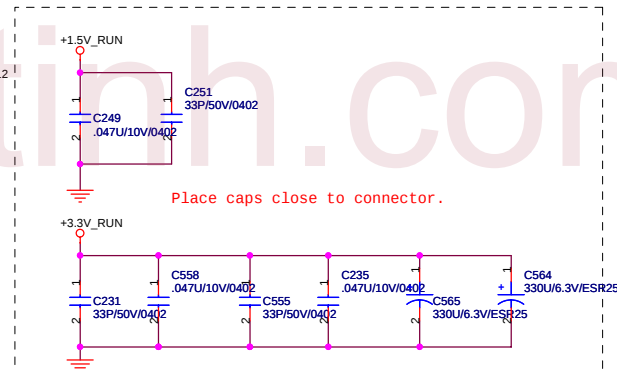
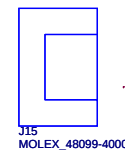
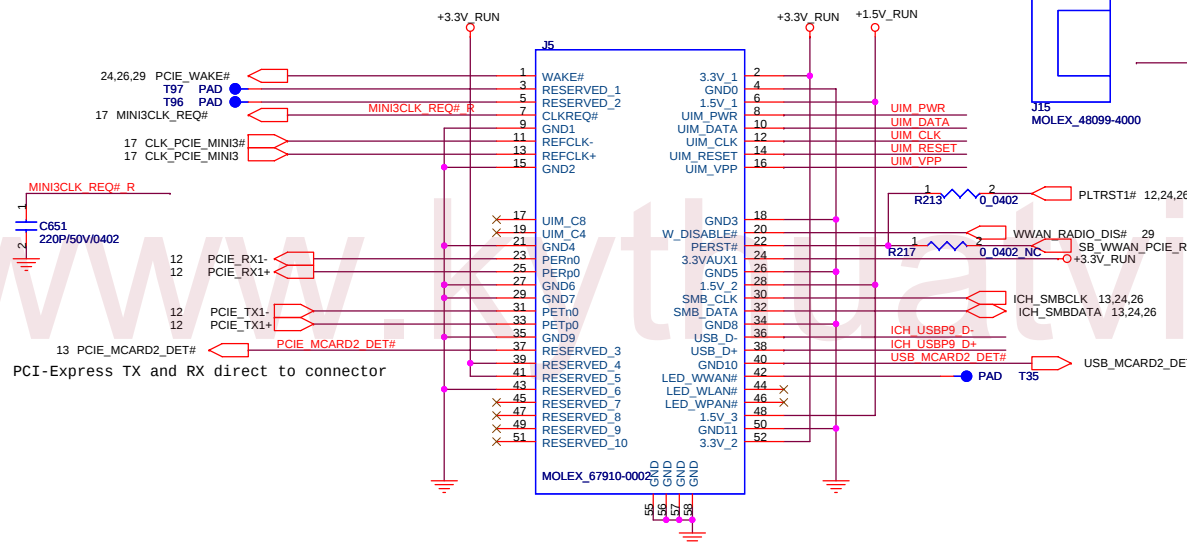
Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.



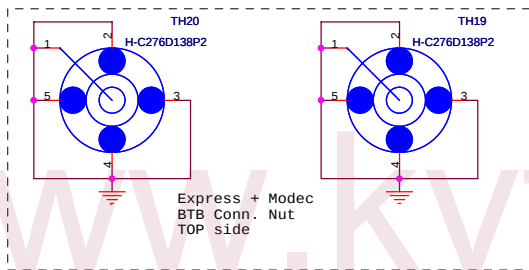
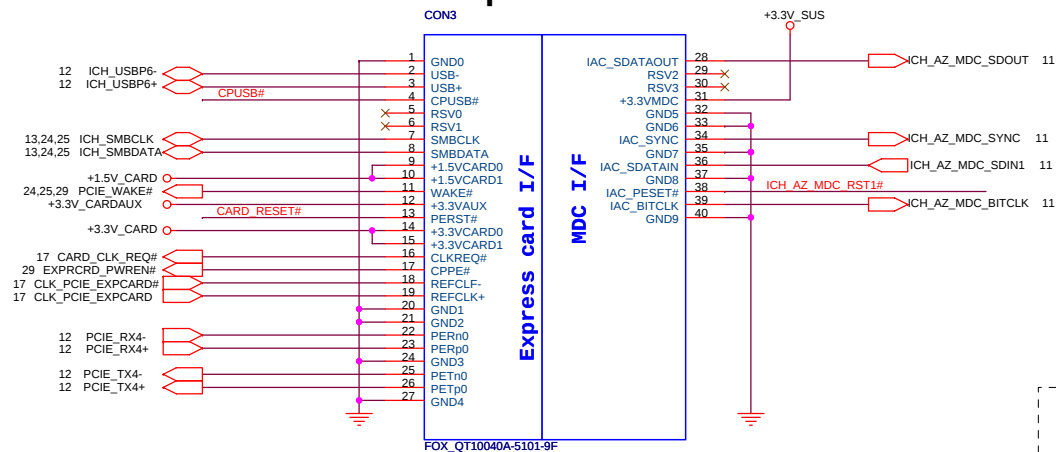
Title SATA (HDD&CD_ROM)		
Size	Document Number C & G UMA	Rev 2A
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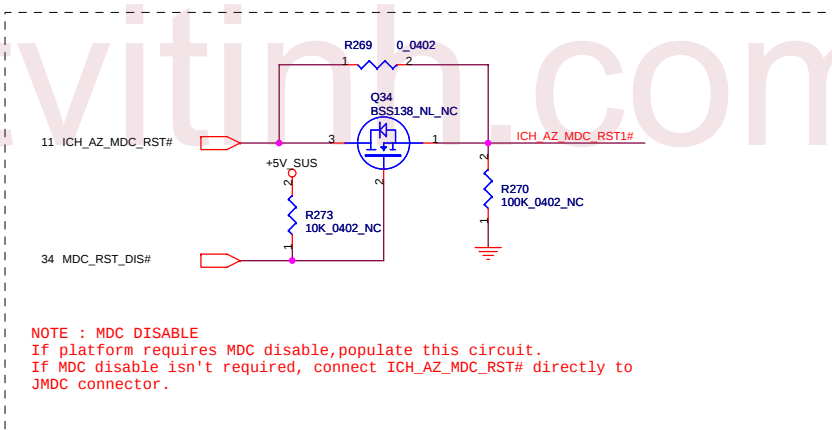
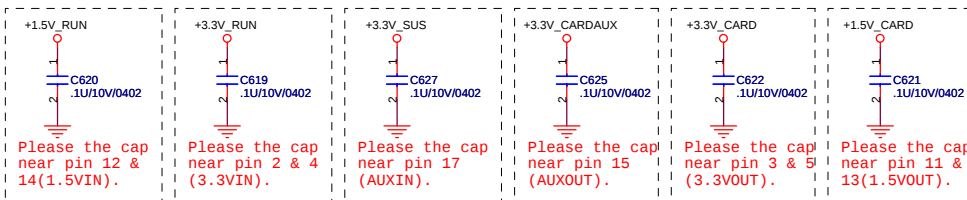
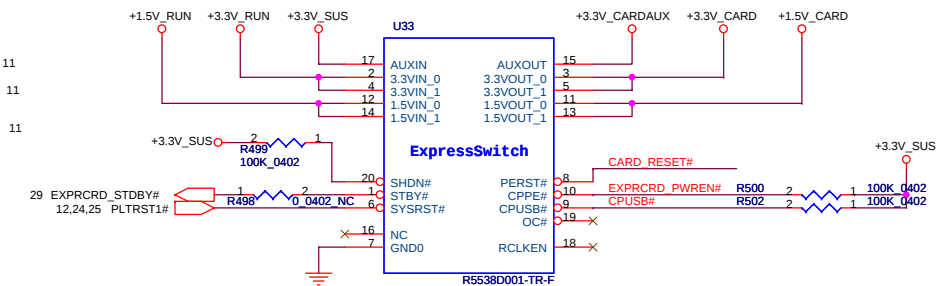
MiniCard WWAN connector

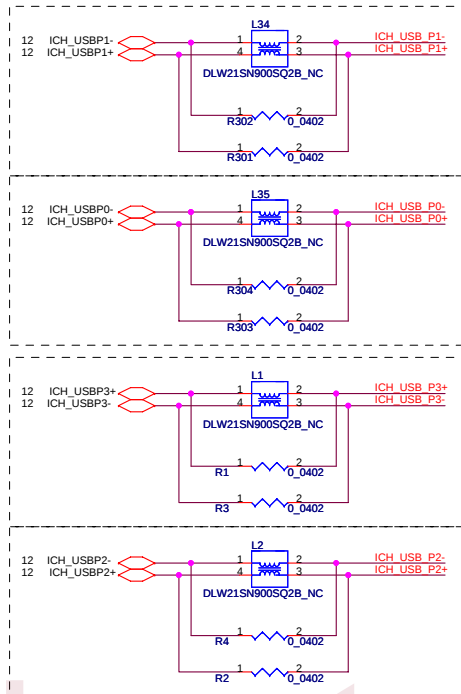
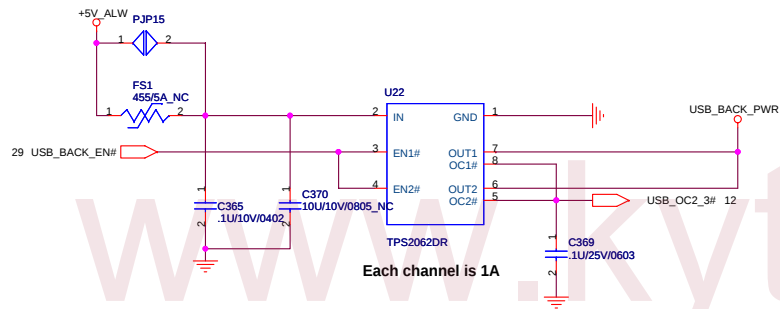
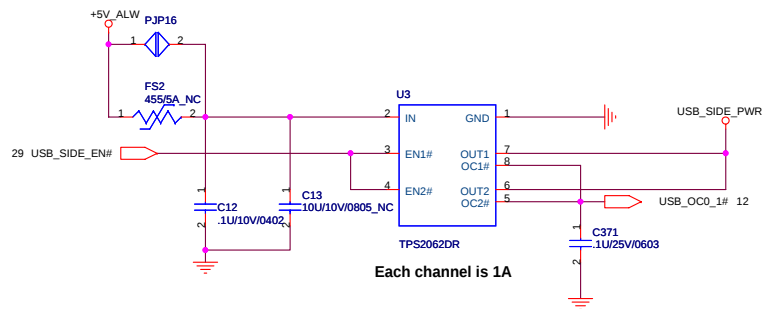


EXPRESS+MDC Update PN

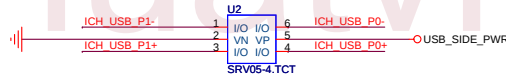


+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

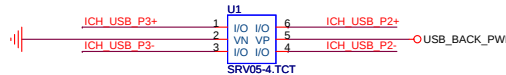




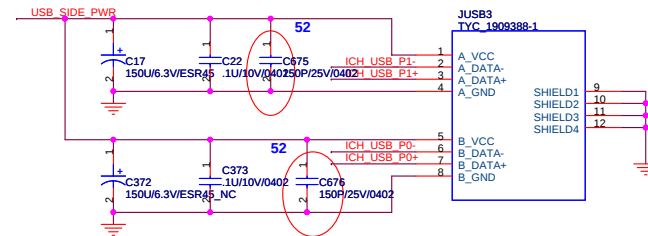
Place ESD diodes as close as USB connector.



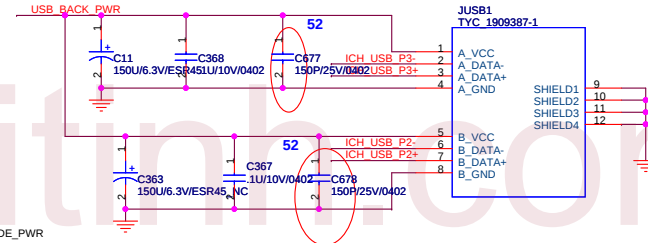
Place ESD diodes as close as USB connector.



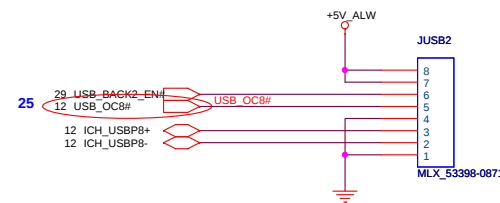
Right



Back



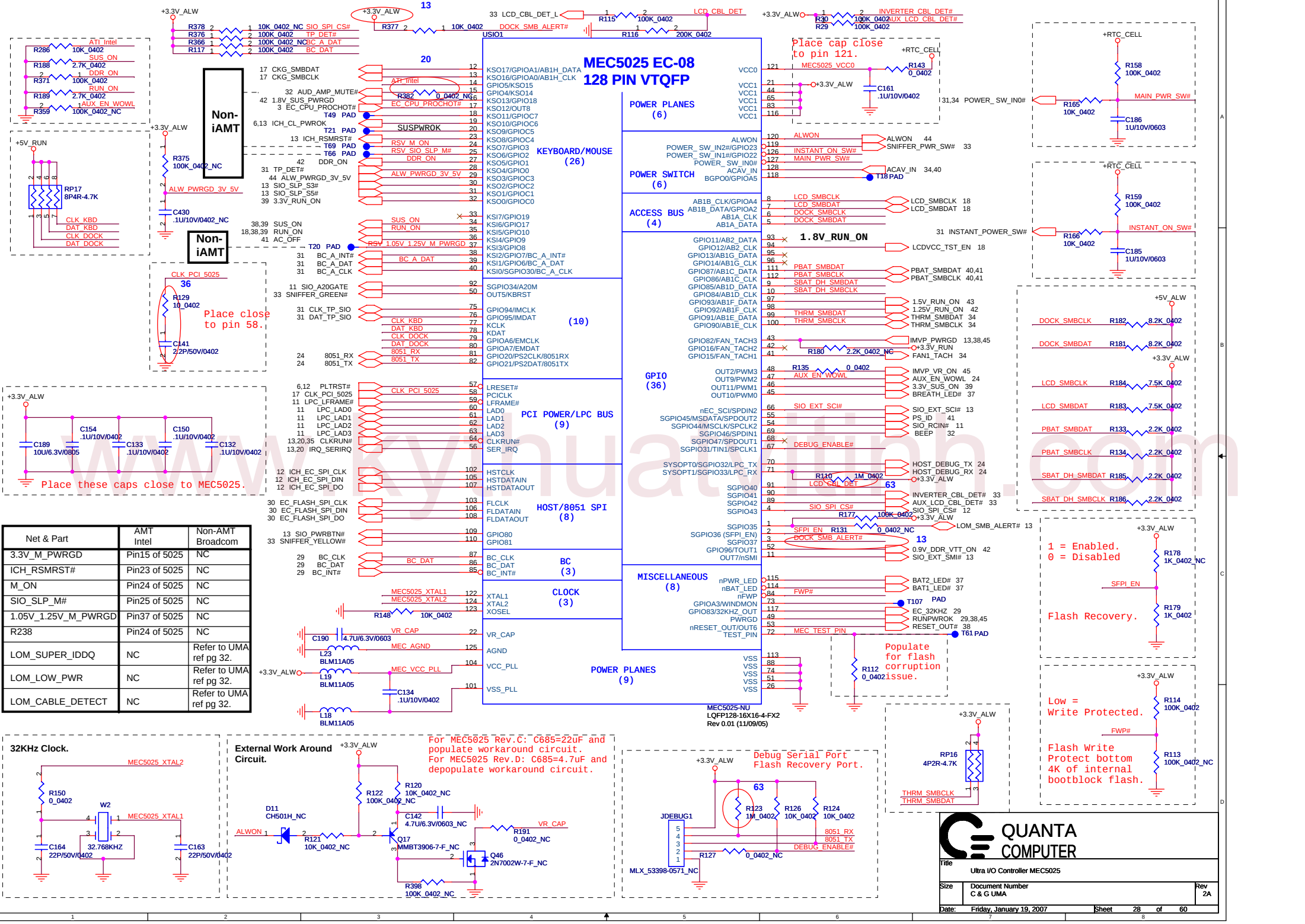
For Gilligan



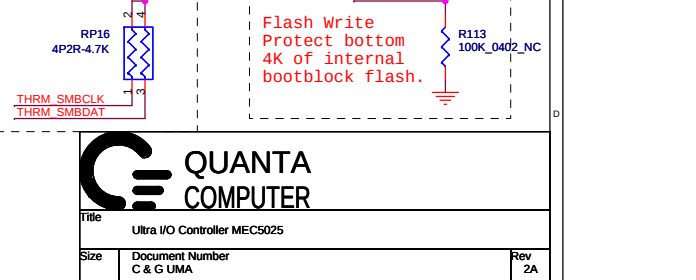
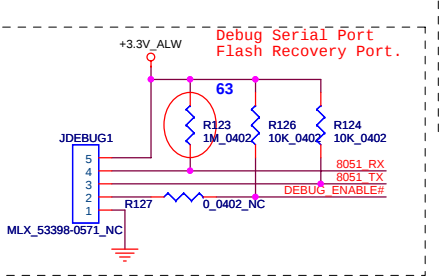
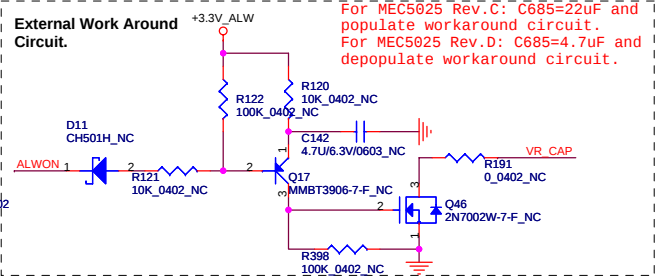
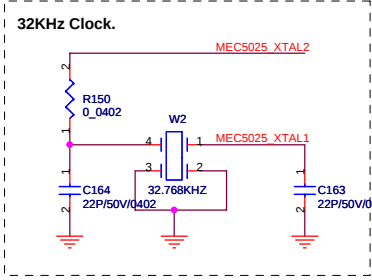
Ext. USB WTB Conn.
Populate for Gilligan
(P/N: DFHD08MS731)
TOP Side



Title	External USB	Rev	2A
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Net & Part	AMT Intel	Non-AMT Broadcom
3.3V_M_PWRGD	Pin15 of 5025	NC
ICH_RSMRST#	Pin23 of 5025	NC
M_ON	Pin24 of 5025	NC
SIO_SLP_M#	Pin25 of 5025	NC
1.05V_1.25V_M_PWRGD	Pin37 of 5025	NC
R238	Pin24 of 5025	NC
LOM_SUPER_IDDQ	NC	Refer to UMA ref pg 32.
LOM_LOW_PWR	NC	Refer to UMA ref pg 32.
LOM_CABLE_DETECT	NC	Refer to UMA ref pg 32.





QUANTA

COMPUTER

Title

Ultra i/O Controller MEC5025

Size

Document Number
C & G UMA

Date:

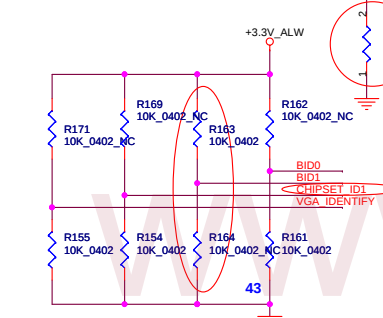
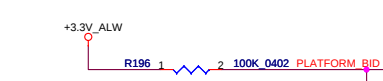
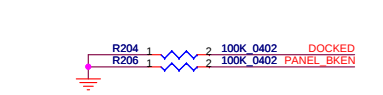
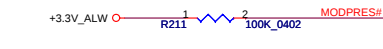
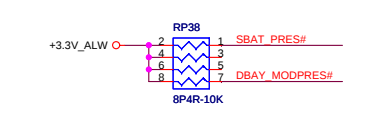
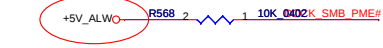
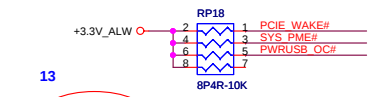
Friday, January 19, 2007

Sheet

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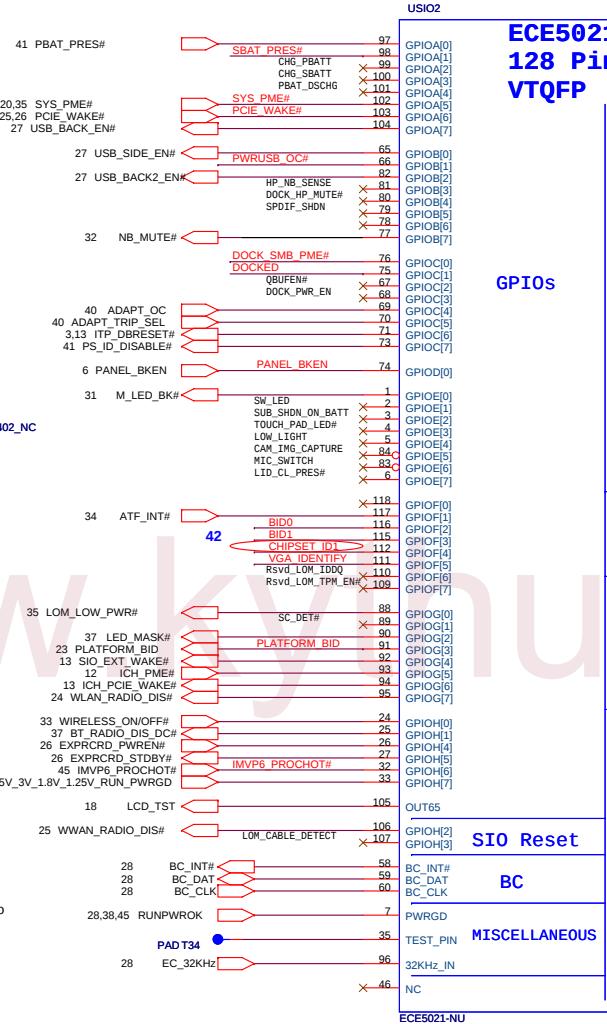
Rev

2A



BID3	BID2	BID1	BID0	Board Revision
0	0	0	0	SST (X00)
0	0	0	1	ST (X01)
0	0	1	0	ST (X02)
0	0	1	1	QT (A00)
0	0	0	0	RAMP(A01)

PROCHOT# change to CPU_PROCHOT# per ref schematic.



ECE5021
128 Pin
VTQFP

GPIOs

SIO Reset

BC

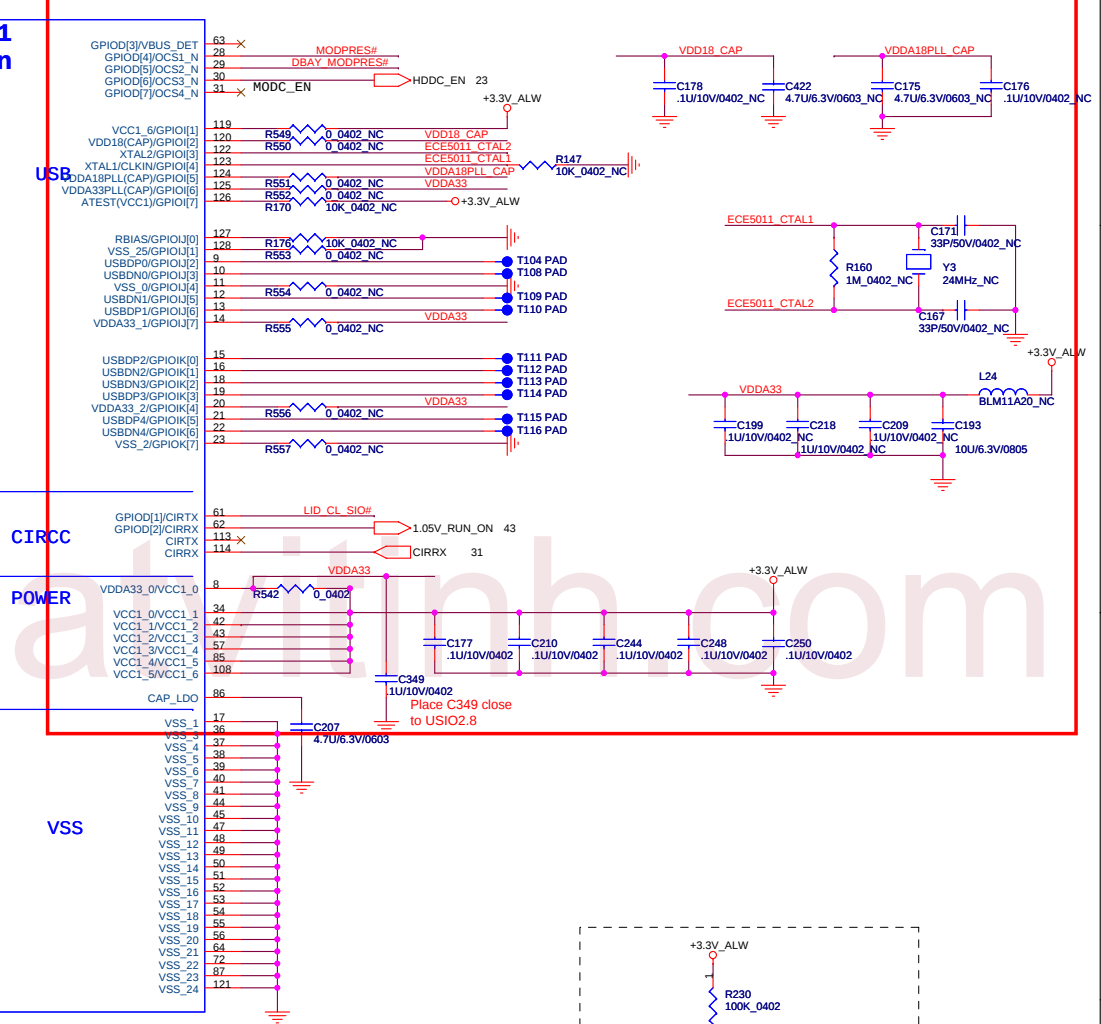
MISCELLANEOUS

ECE5021-NU

55

Update to 5021:

Depopulate R549, R550, R551, R552, R170, R176, R553, R554, R555, R556, R557, C178, C442, C175, C176, C199, C218, C209, L24. Populate R542, C349.



CIRCC

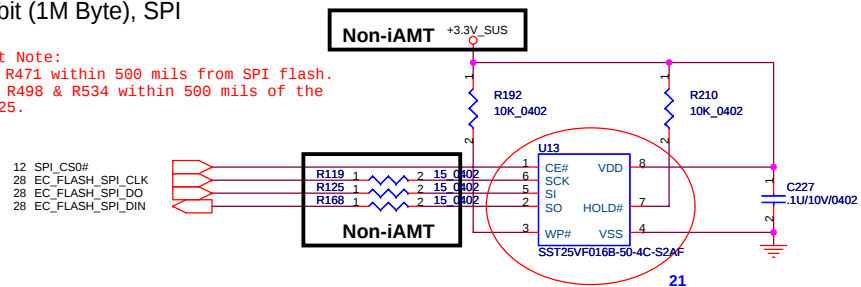
POWER

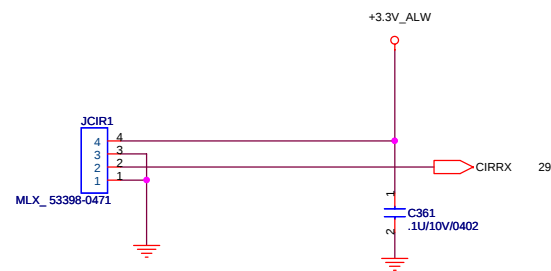
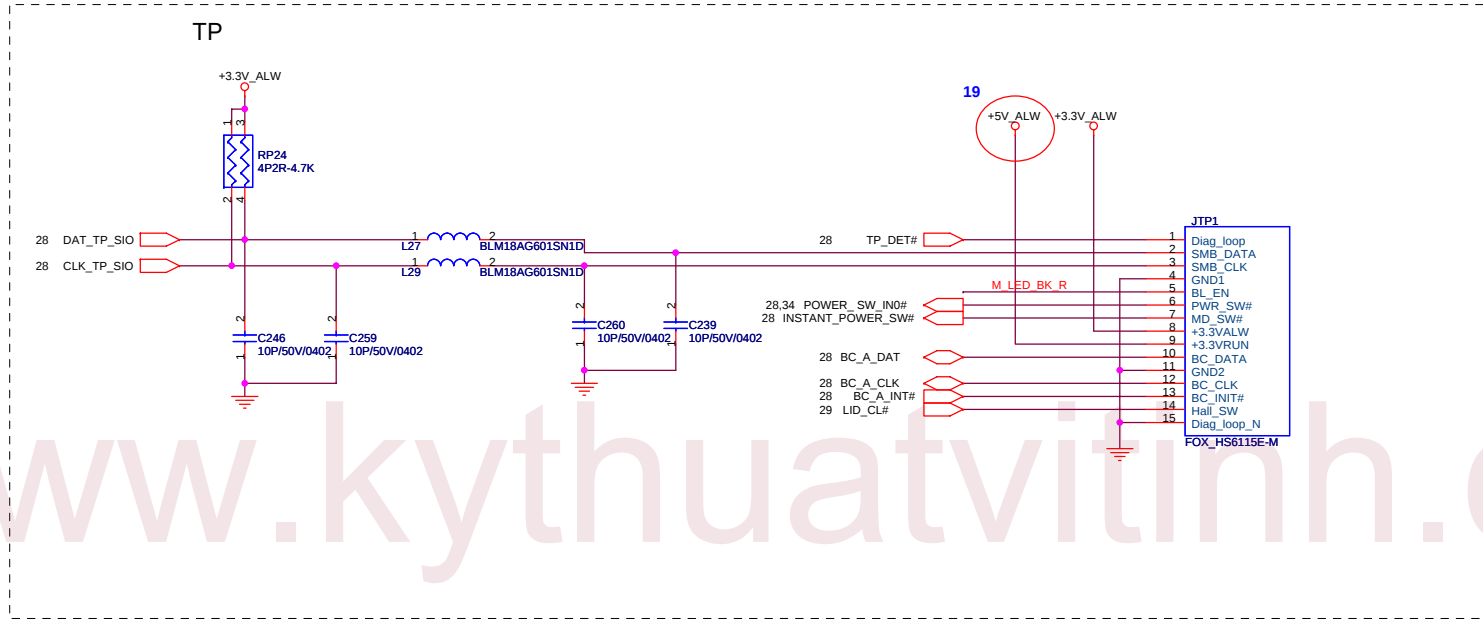
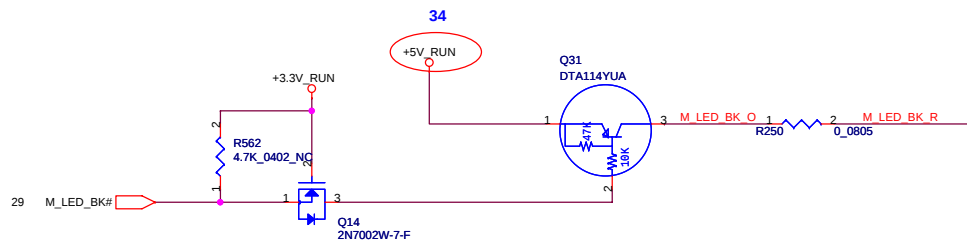
VSS



Title SIO (GPIO/BC/USB/CIRR)		
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Layout Note:
Place R471 within 500 mils from SPI flash.
Place R498 & R534 within 500 mils of the
MEC5025.

[illegible]



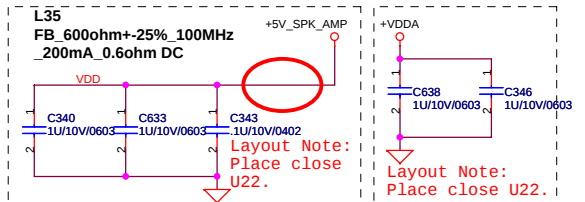
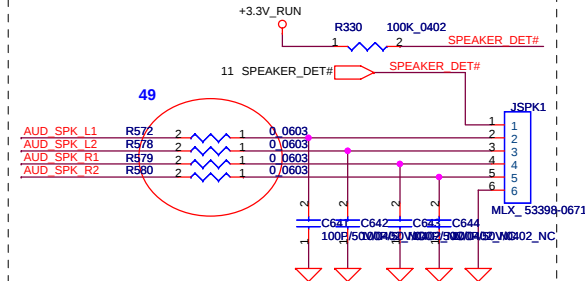
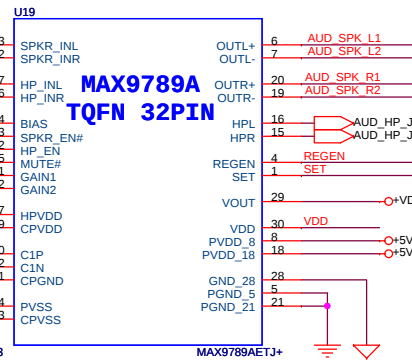
Package 1206 for THD+N performance for Vista Logo requirements.

AUD LINE OUT L C331 1 2 0.033U/25V/X7R/1206
AUD LINE OUT R C332 1 2 0.033U/25V/X7R/1206
AUD HP OUT L C351 2 1 1uF/25V/X7R/1206
AUD HP OUT R C354 2 1 1uF/25V/X7R/1206

For TPA6040A, pop R530, depop R531.

AUDIO AVDD_ON 1 2 0.0402_NC
AUD AMP MUTE# 1 2

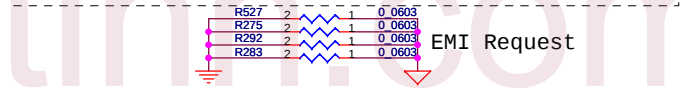
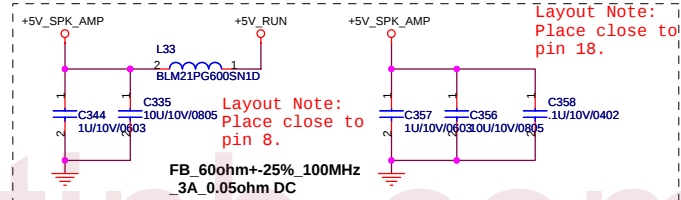
INTERNAL SPEAKER AMP



C1425/C331 value need to match with C326/C290. This value be chosen in PT phase

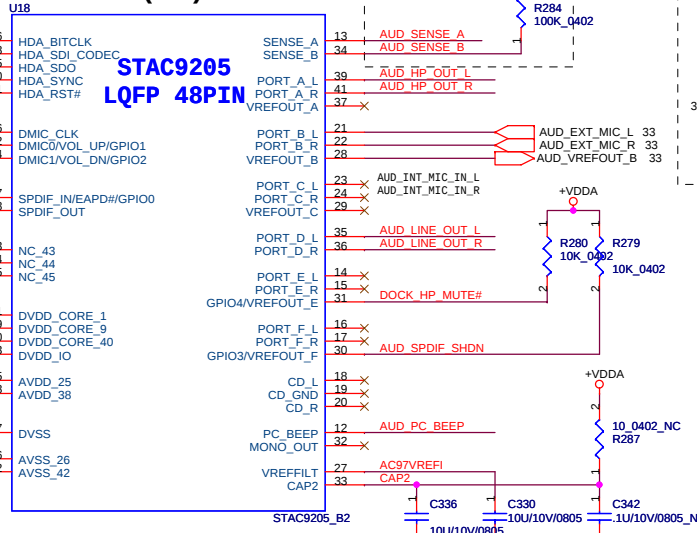
For TPA6040A, pop C640, depop R529.

For TPA6040A, pop C331, depop R406.



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

AZALIA (HD) CODEC



ICH AZ CODEC BITCLK 11 ICH AZ CODEC SDINO 11 ICH AZ CODEC SDOUT 11 ICH AZ CODEC SYNC 11 ICH AZ CODEC_RST# 11

33 AUD_DMIC_CLK 33 AUD_DMIC_IN0 33

19 AUD_SPDIF_OUT 19

NC_43 NC_44 NC_45

DVDD_CORE_1 DVDD_CORE_9 DVDD_CORE_40 DVDD_IO

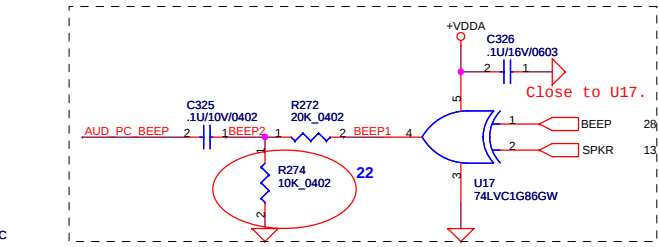
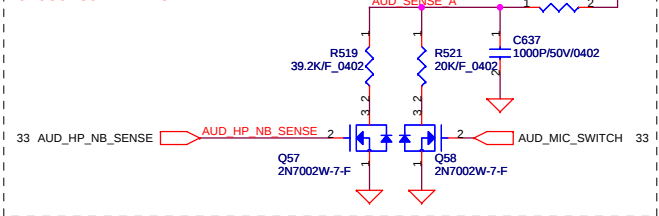
AVDD_25 AVDD_38

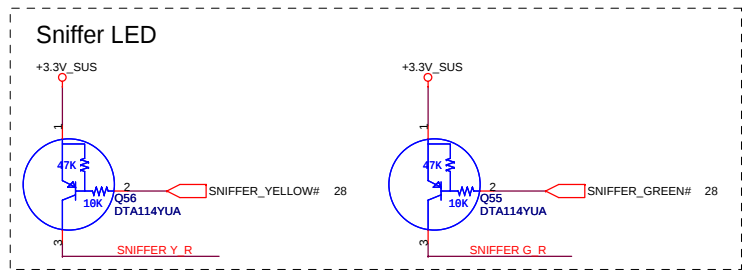
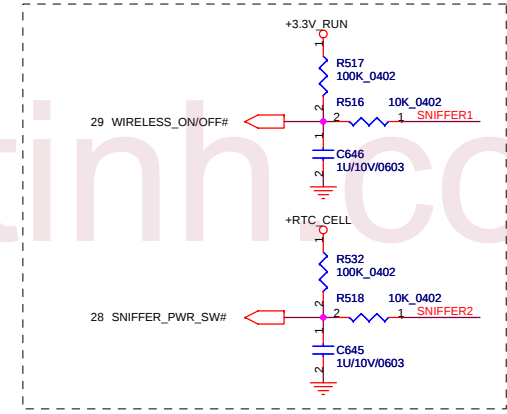
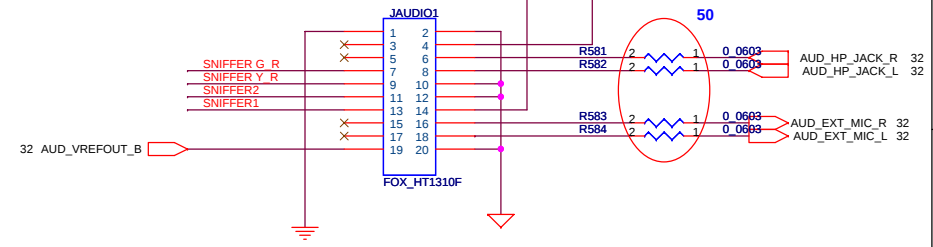
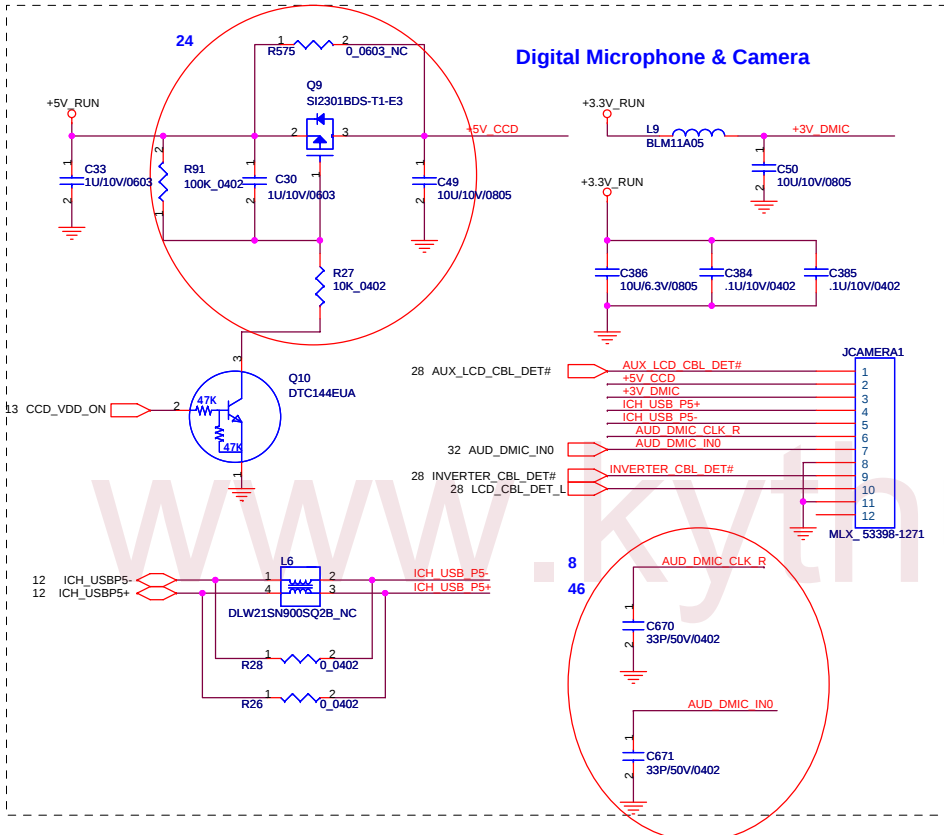
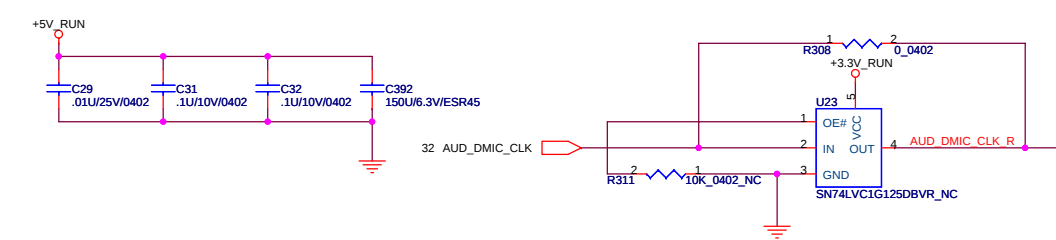
DVSS

AVSS_26 AVSS_42

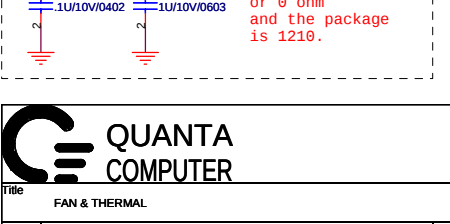
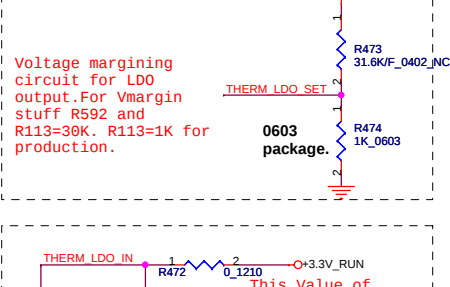
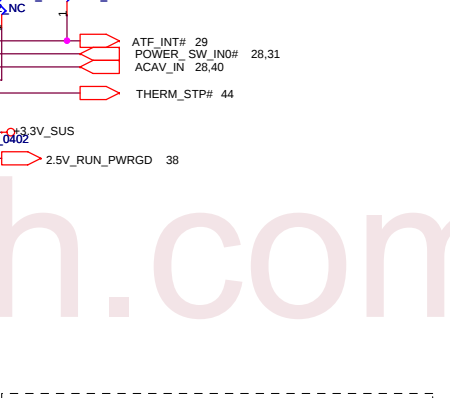
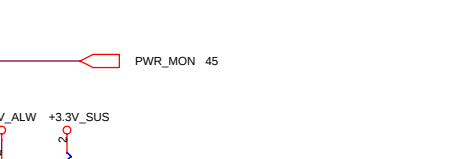
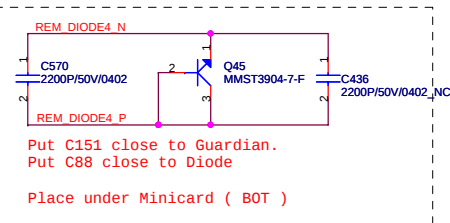
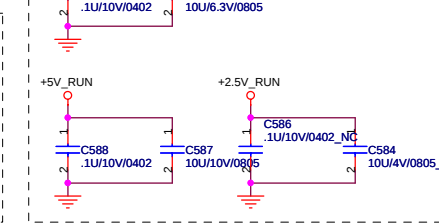
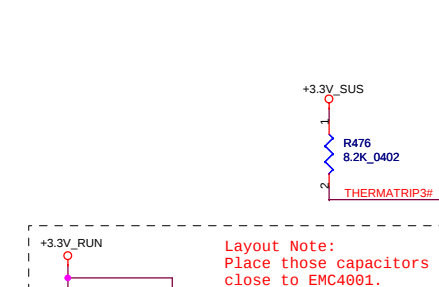
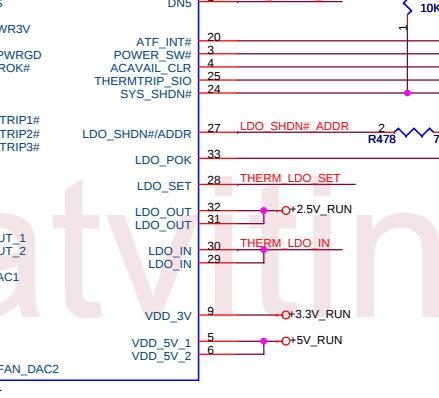
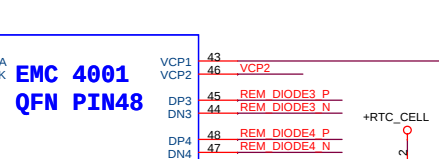
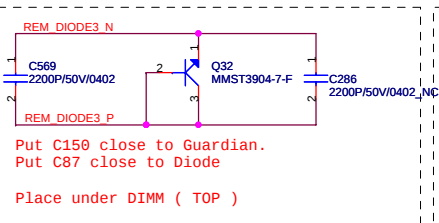
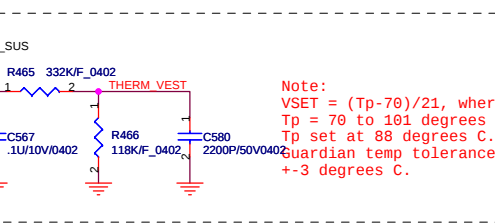
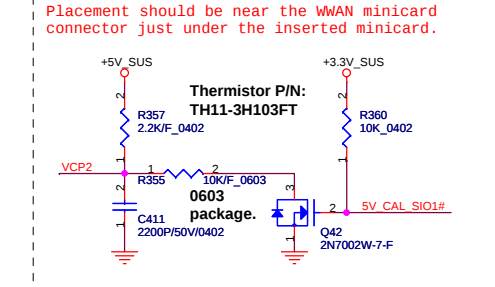
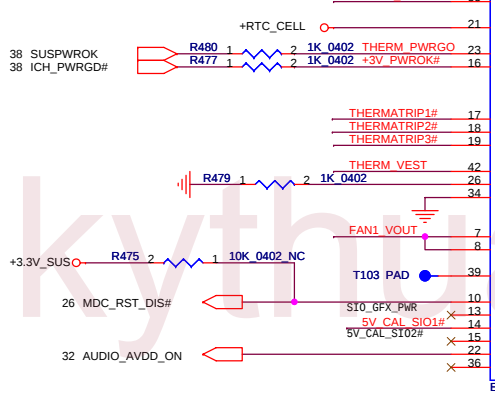
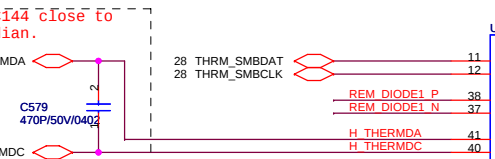
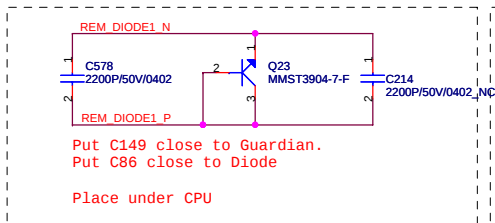
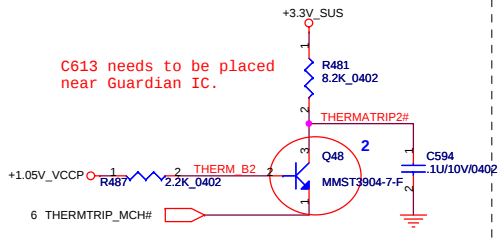
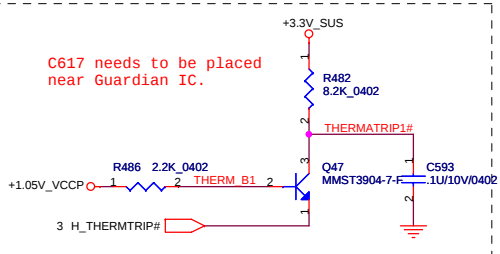
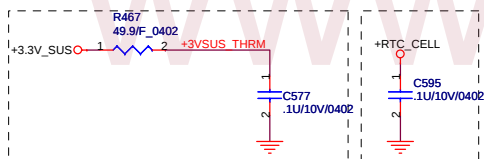
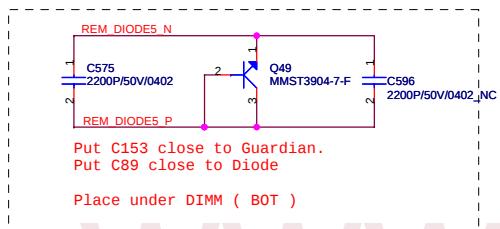
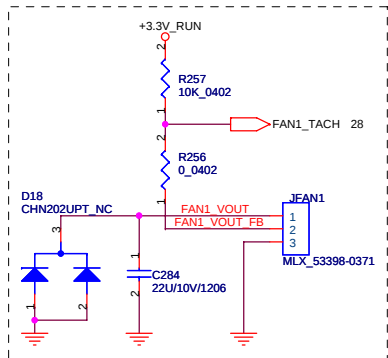
Depop R441 & pop C394 & C312 for AD1984.

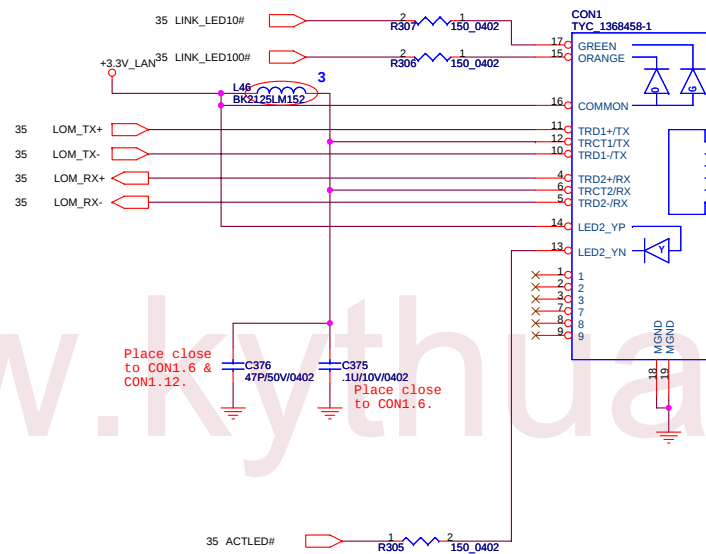
Layout Note: Close to Pin 13.



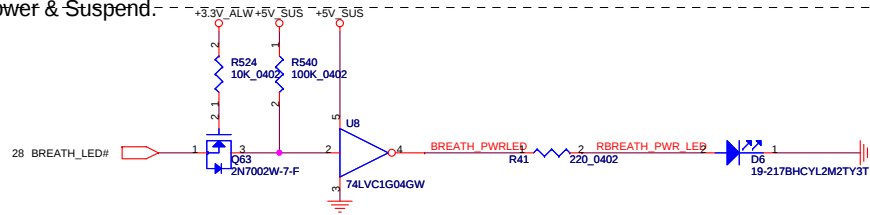


- | | | |
|----|------------------------------------|---------------------------------|
| 1 | Diag Loop | Diag MB connector (Local Loop) |
| 2 | Mic Signal | |
| 3 | Mic Pwr Mic Power 3.3v (run) | |
| 4 | Mic clock | Mic Clock |
| 5 | GND | |
| 6 | USB Signal | |
| 7 | USB Pwr Camera Power 3.3v (Camera) | |
| 8 | USB Clock | |
| 9 | Diag CAM | Diag Camera/Inverter |
| 10 | Diag LVDS | Diag 5v return (LVDS connector) |
| 11 | Diag Loop | Diag MB connector (Local Loop) |



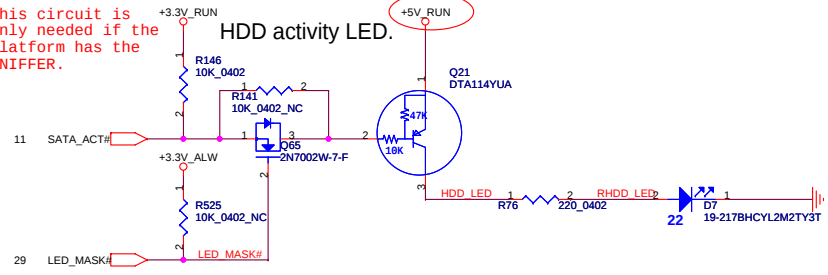


Power & Suspend.

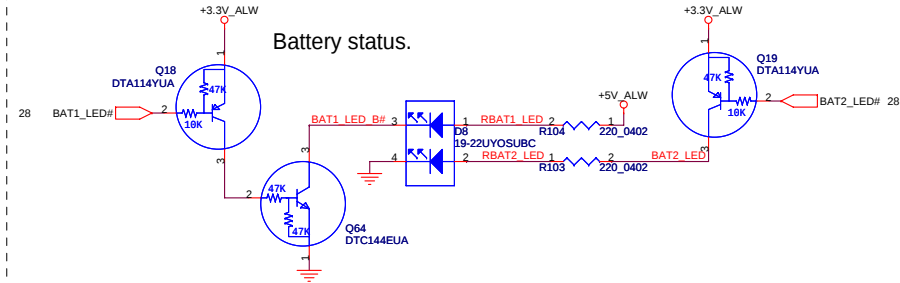


This circuit is only needed if the platform has the SNIFFER.

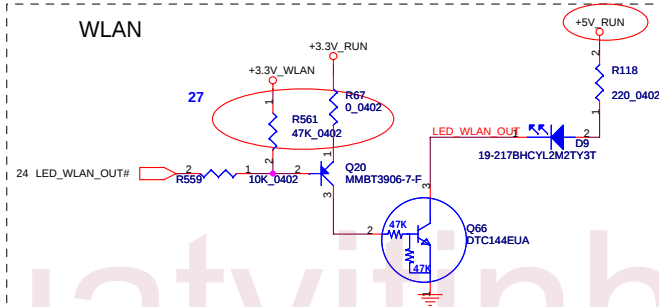
HDD activity LED.



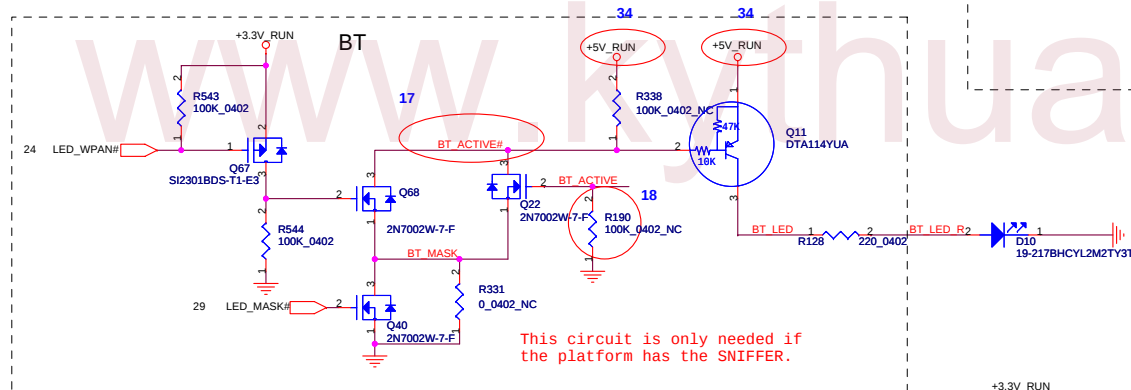
Battery status.



WLAN

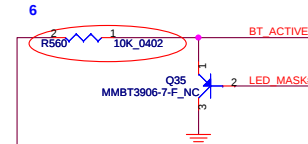


BT

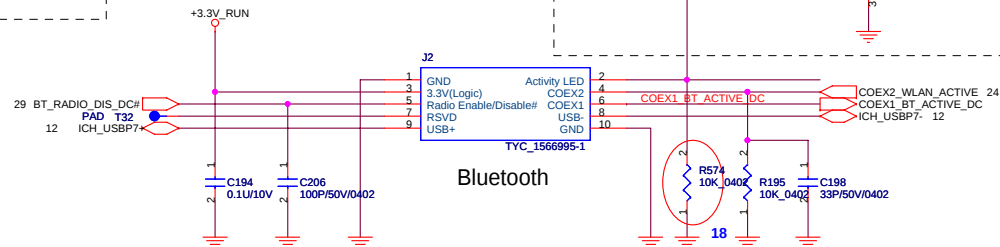


This circuit is only needed if the platform has the SNIFFER.

This circuit is only needed if the platform has the SNIFFER.



Bluetooth



SWITCH & LED

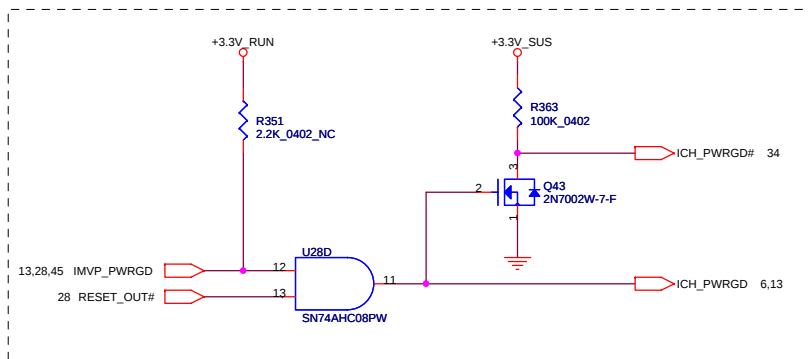
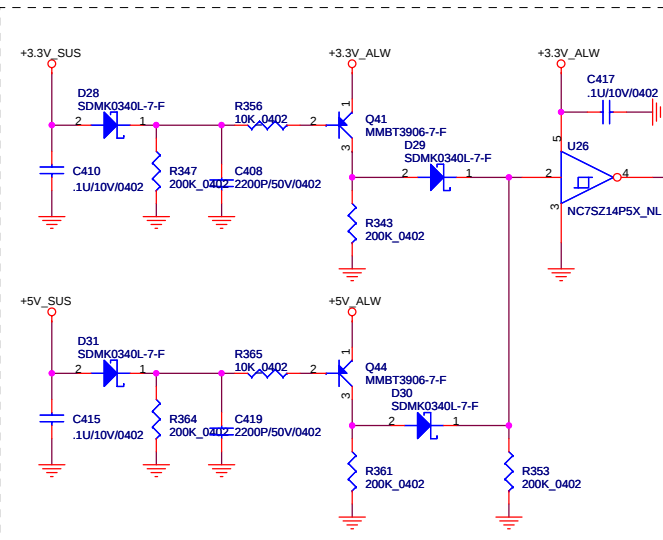
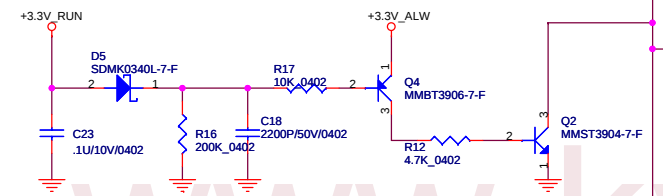
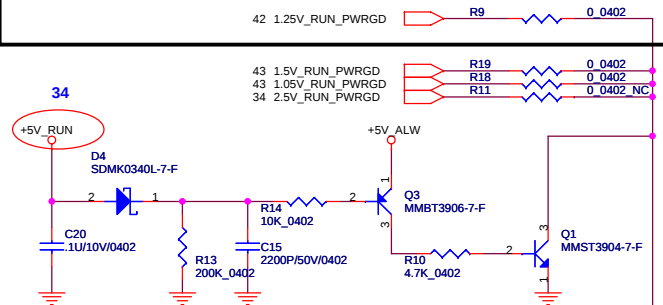
Size Document Number
C & G UMA

Date: Tuesday, January 23, 2007

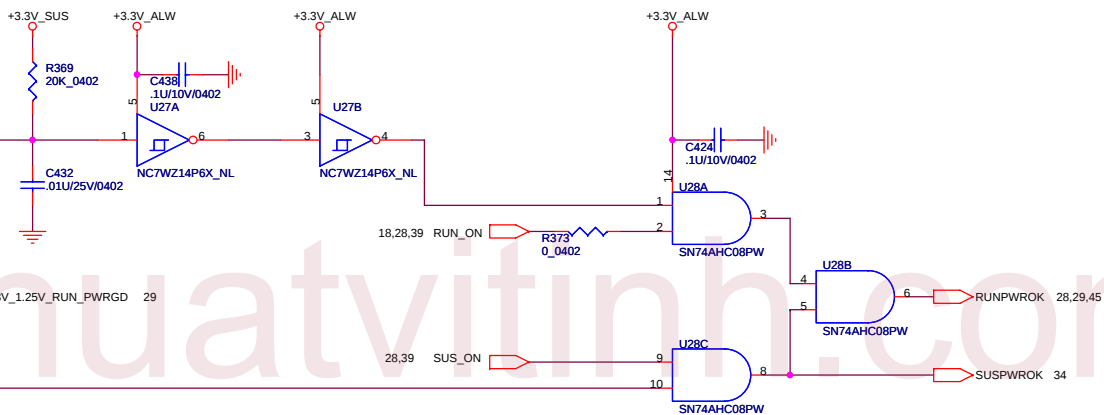
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Non-iAMT



Keep Away from high speed buses



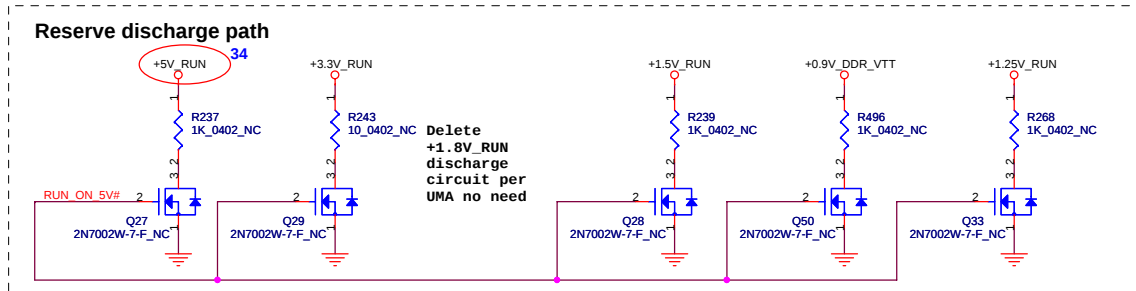
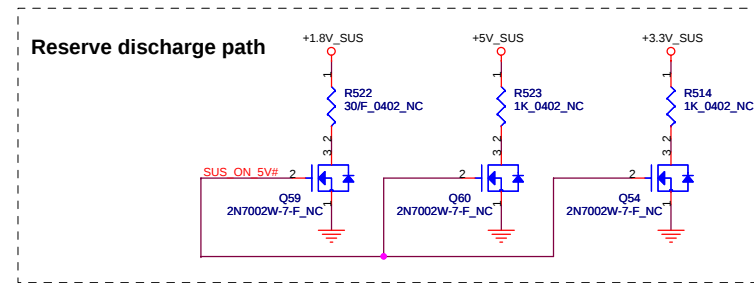
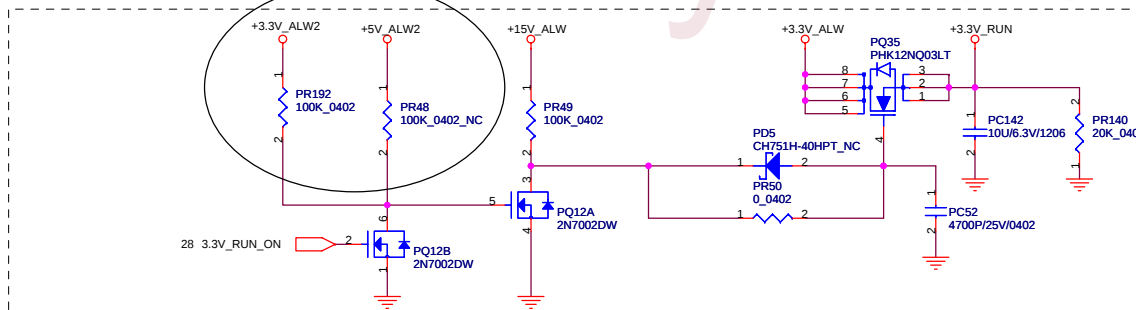
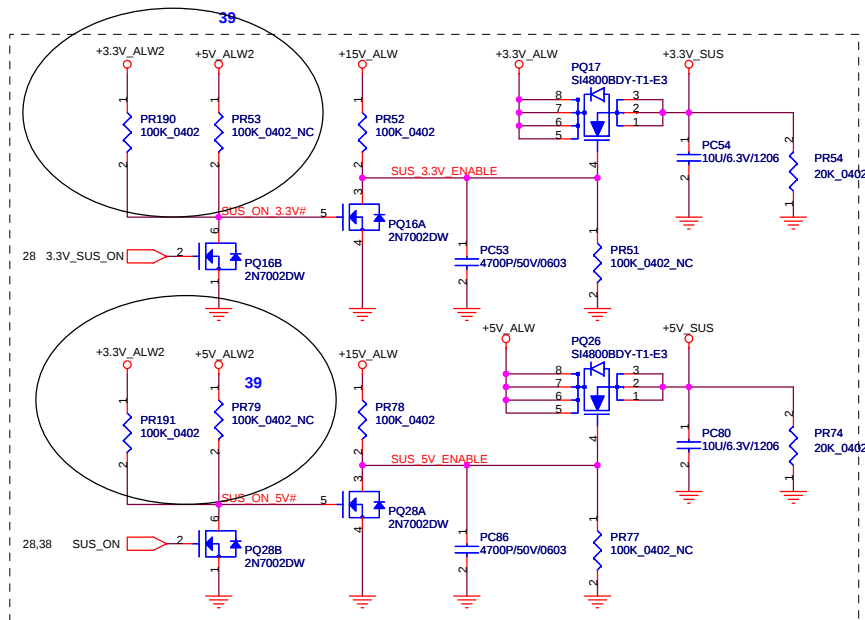
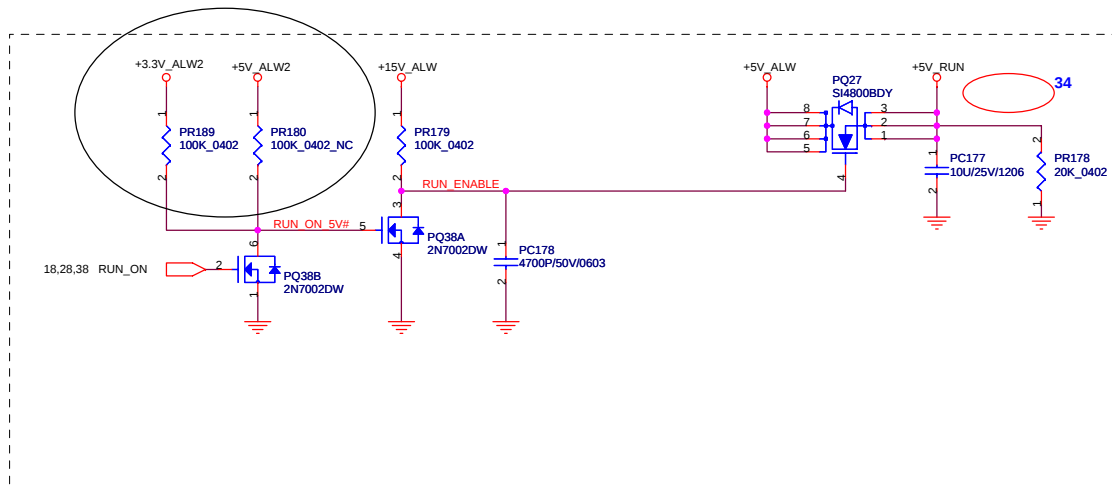
Title	System Reset Circuit
-------	----------------------

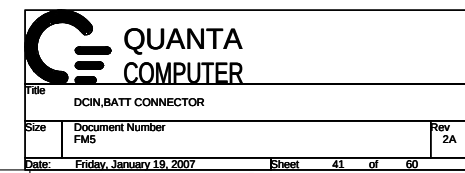
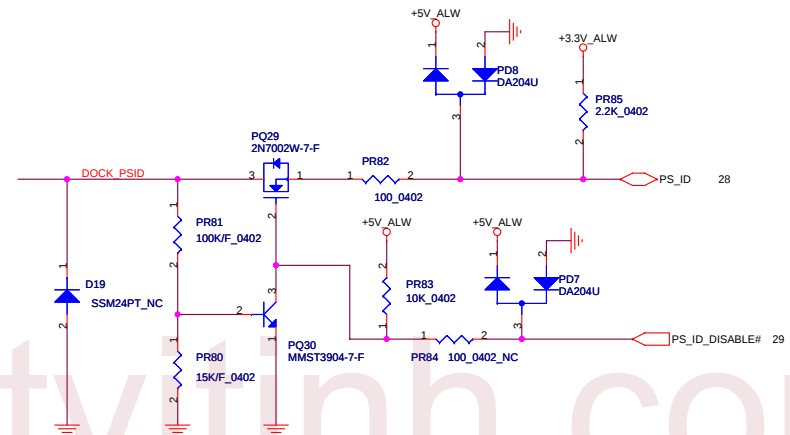
Size	Document Number C & G UMA
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Date: Friday, January 19, 2007

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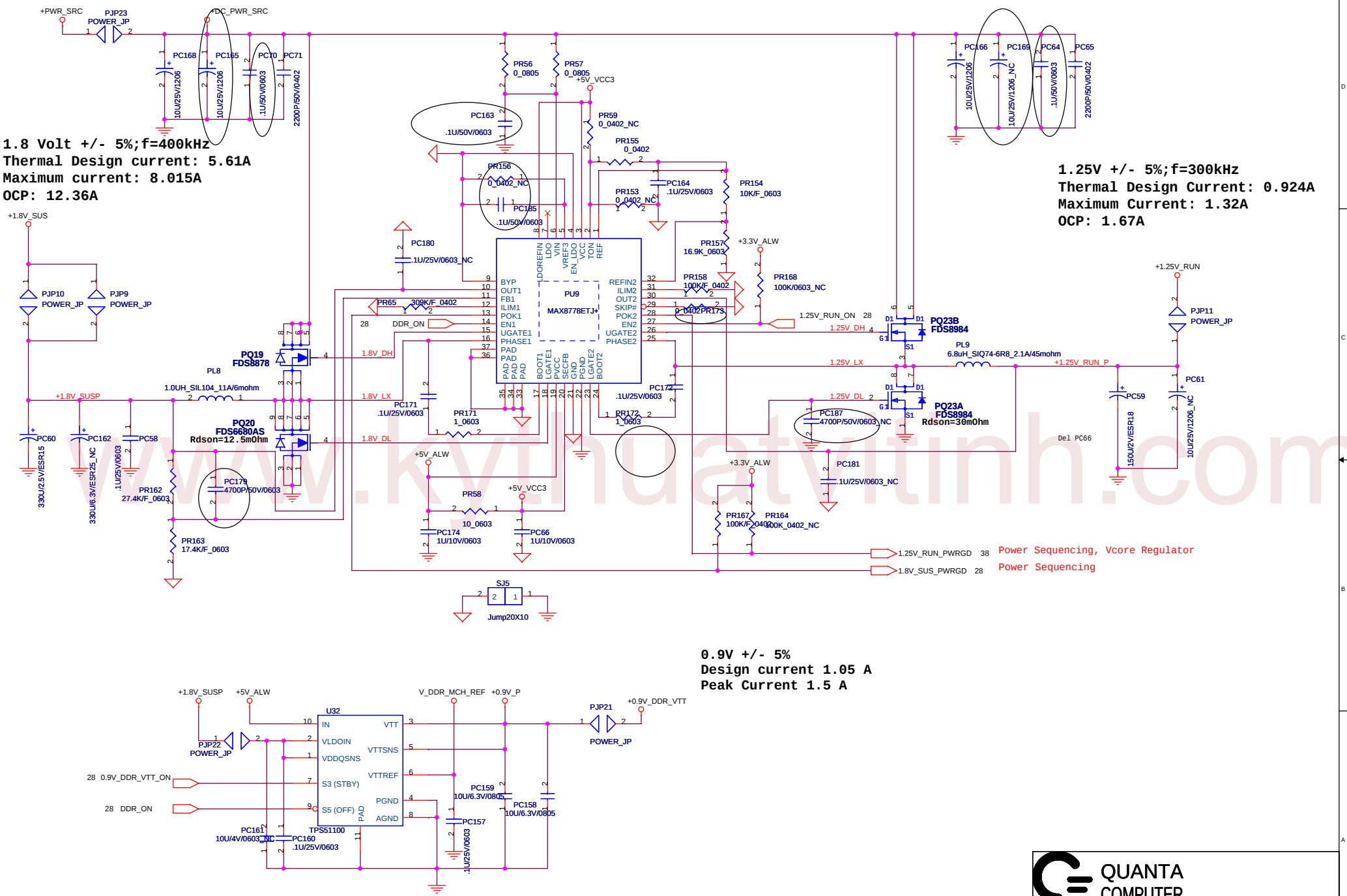




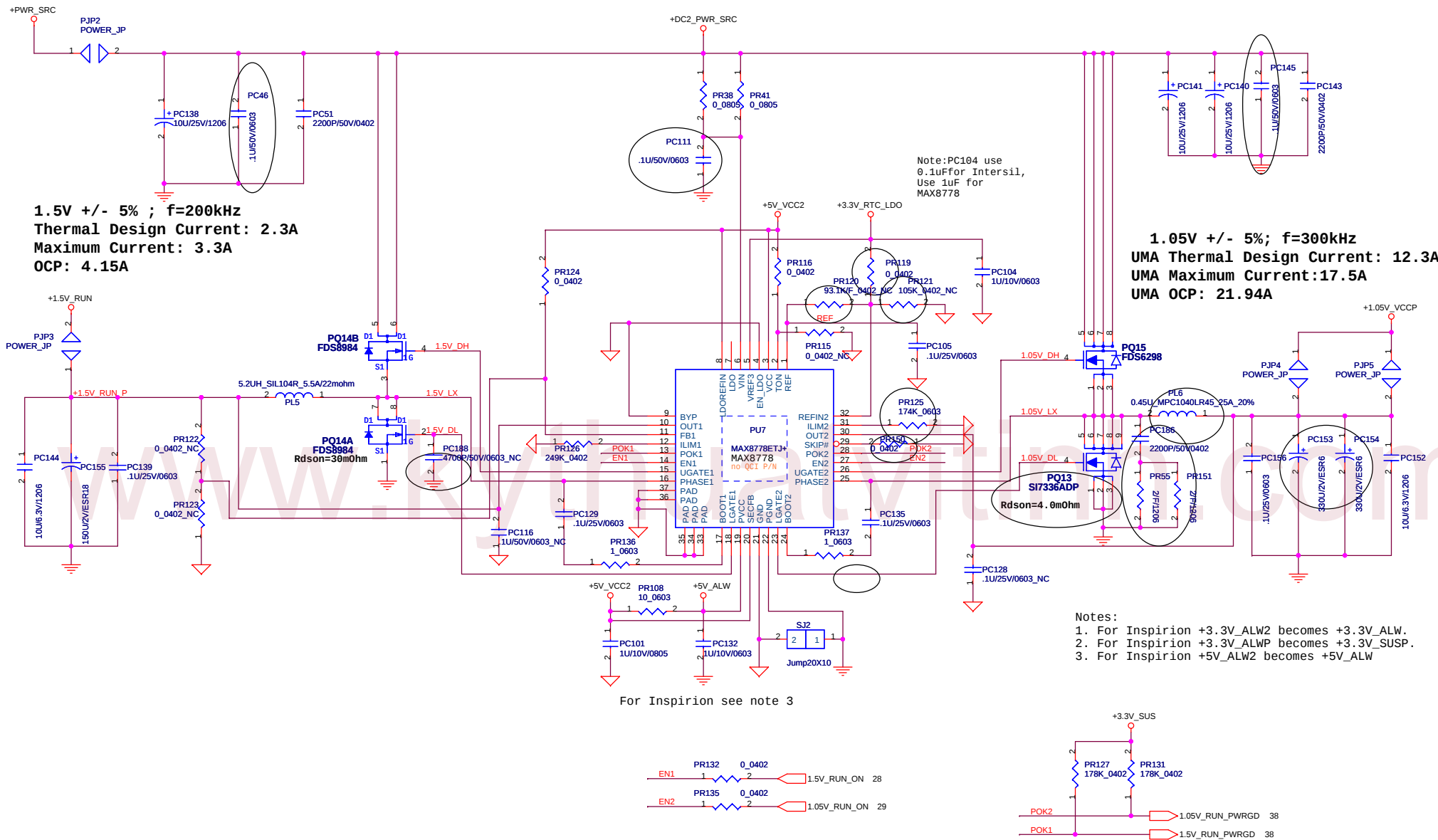
1.8 Volt +/- 5%;f=400kHz
 Thermal Design current: 5.61A
 Maximum current: 8.015A
 OCP: 12.36A

1.25V +/- 5%;f=300kHz
 Thermal Design Current: 0.924A
 Maximum Current: 1.32A
 OCP: 1.67A

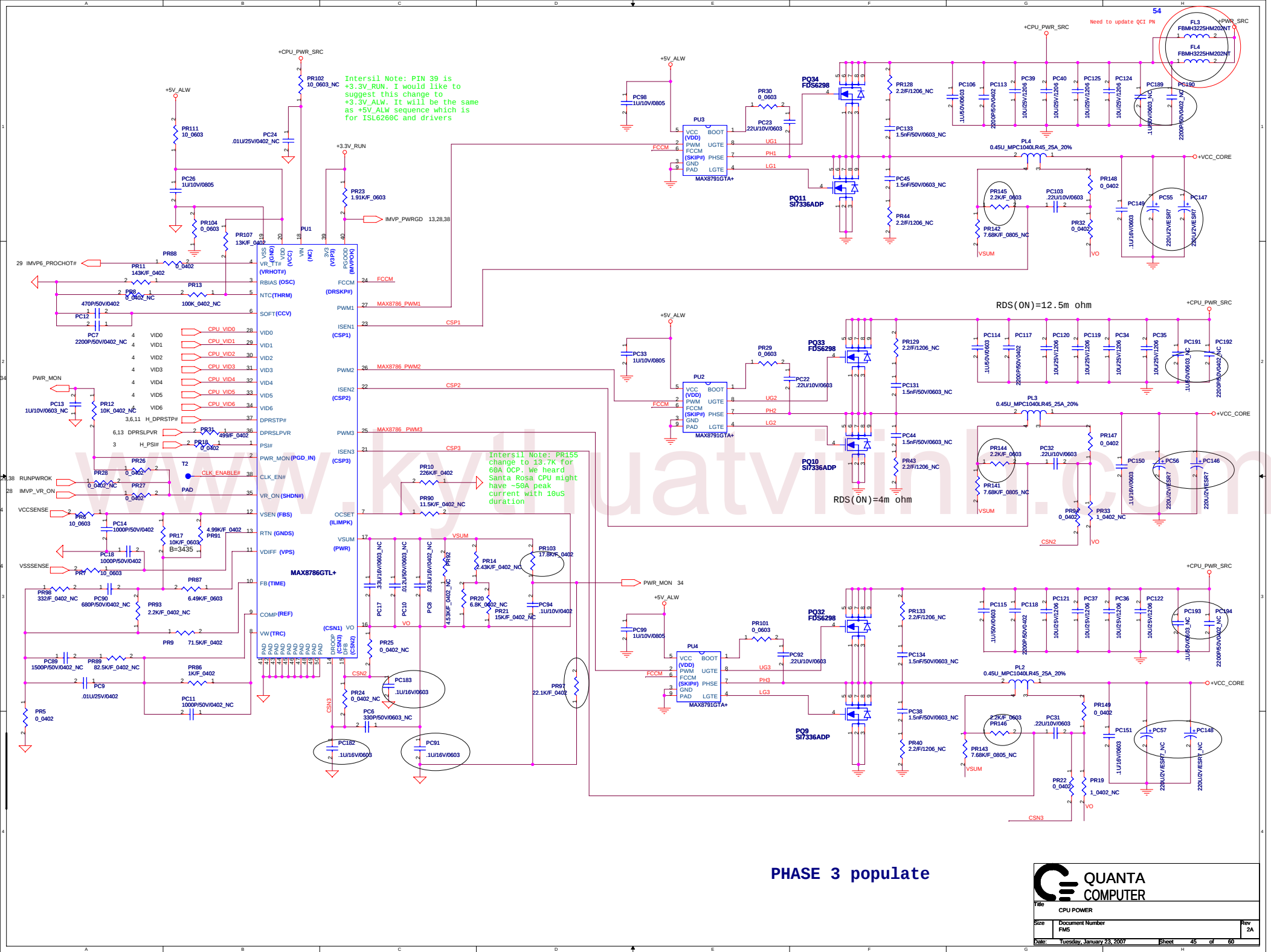
0.9V +/- 5%
 Design current 1.05 A
 Peak Current 1.5 A

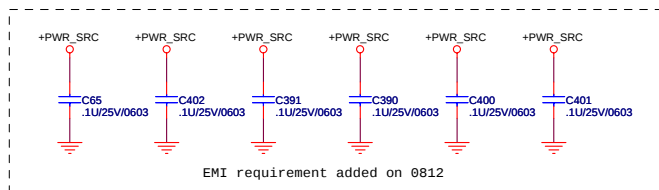
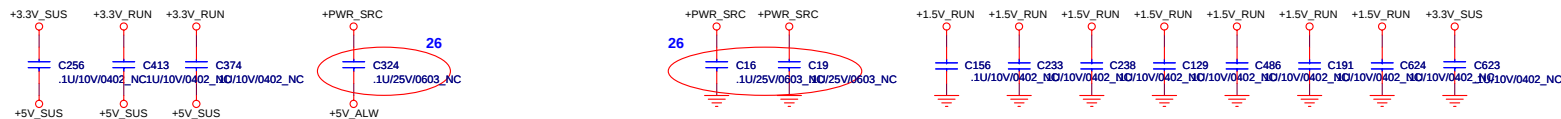
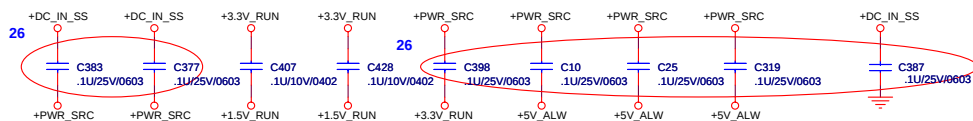
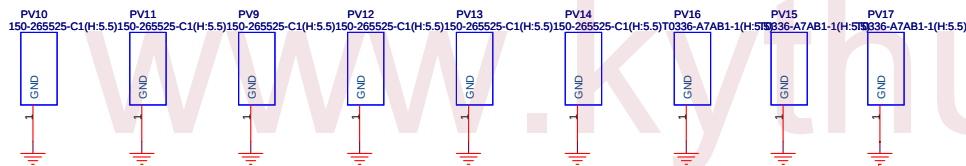
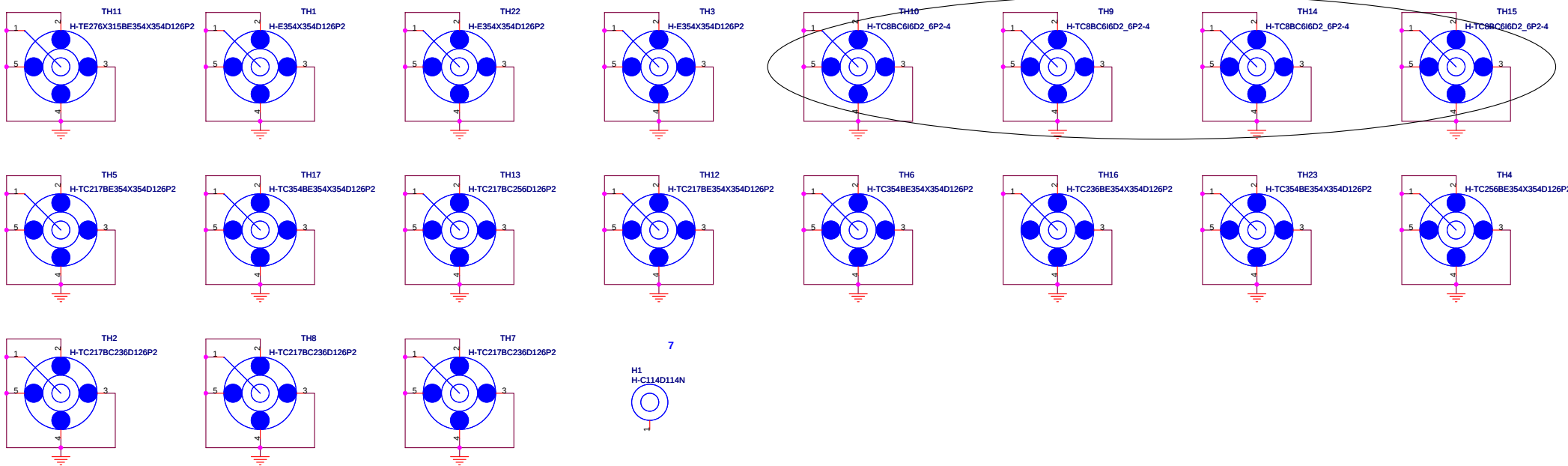


+1.5V_RUN /+1.05V_VCCP /+3.3V_ALW /+3.3_RTC_LDO



Title		
1.5V,1.05V		
Size	Document Number	Rev
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW	+1.8V_SUS +1.8V_LOM +3.3V_LAN +3.3V_SUS +5V_SUS	+0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN	+3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA	+DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	OFF	ON
S5 S4/AC	ON	OFF	OFF	OFF	ON
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	ON

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
BCM4401B	AD16	REQ#0 / GNT#0	PIRQB
R5C833	AD17	REQ#1 / GNT#1	PIRQC: Card reader PIEQD: 1394

ICH8-M

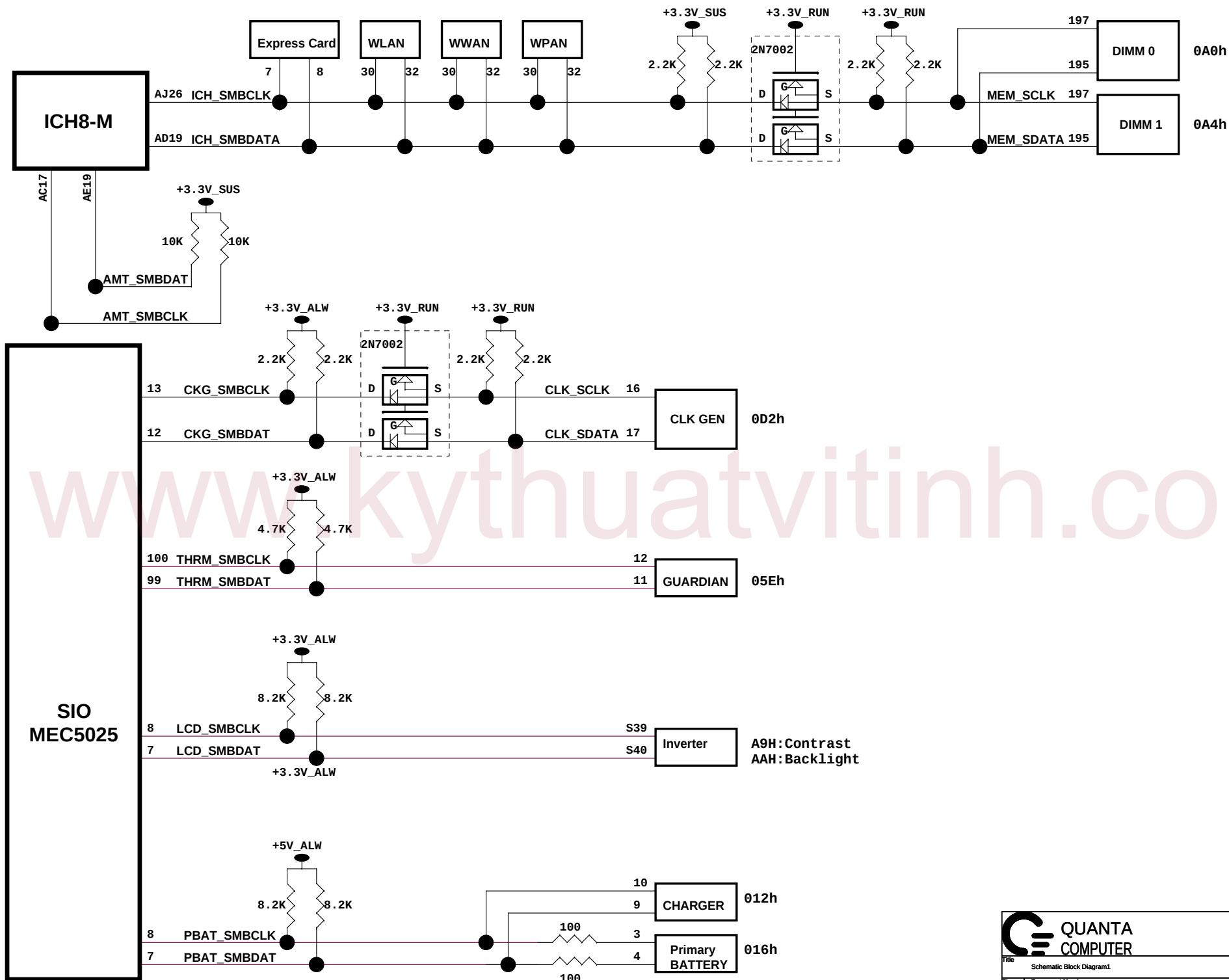
ECE 5011

USB PORT#	DESTINATION
0	Right Top
1	Right Bottom
2	Side TOP
3	Side Bottom
4	Ext. USB TOP
5	Digital Camera
6	Express Card
7	WPAN/Bluetooth
8	Ext. USB Bottom
9	WWAN
1	None
2	None
3	None
4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 WPAN
Lane 4	Express Card
Lane 5	None
Lane 6	None



QUANTA
COMPUTER



Model	Item	Page	Date	Rev.	Description
C & G UMA	1	P.3	0619	1A	Update no populated ITP schmatic per ref. Intel checklist V:1.201a. And added ITP to XDP implement txt.
	2	P.23,25,46	0620	1A	Update Screw hole per ME update.
	3	P.17	0620	1A	Update SRC CLK per followed Discrete schematic changed.
	4	P.12	0620	1A	Swap RP21.2, RP21.3, RP52.3, RP52.4, RP52.6 net for layout requirement.
	5	P.15,16	0620	1A	Swap RP14.2, RP14.4, JDIM2.136, JDIM2.137, JDIM2.141, JDIM2.143 per layout requirement.
	6	P.13,28	0620	1A	Change USIO2.28 net name from SIO_S4_STATE# to TP_DET# and delete U25.AH27.
	7	P.18	0620	1A	Update +LCDVCC circuit per ref. CD_Diag_0619.ppt file.
	8	P.33	0620	1A	Added AUX_LCD_CBL_DET#, INVERTER_CBL_DET#, LCD_CBL_DET Pull-up resistor.
	9	P.13,28	0620	1A	Delete WOL_EN of U25.AG19 and R571. Changed USIO2.94 net-name from WOL_EN to EC_ENVDD per ref BITS WI74741.
	10	P.32	0620	1A	Update JSPK1 and added SPK DET. PU Resistor.
	11	P.28	0620	1A	Delete R479 per ref BITS WI75517
	12	P.24,28	0620	1A	Added WoWL power SW circuit per ref BITS WI74552.
	13	P.6	0620	1A	Delete all of NC pins connected to test pad per ref. BITS issue WI75504.
	14	P.6	0620	1A	Populate R1, R5, R9 per implement ITP function.
	15	P.31	0621	1A	DAT_TP_SIO & CLK_TP_SIO pull up to +3.3V_ALW, Added PU to +3.3V_ALW for TP_DET#.
	16	P.33	0621	1A	Correction LCD_CBL_DET pull up circuit.
	17	P.11,30	0621	1A	Change RTC_BAT_DET# PU resistor from 10K to 100K and moved to P.30
	18	P.11,32	0621	1A	Change SPEAKER_DET# PU resistor from 10K to 100K and moved to P.32
	19	P.24,25	0621	1A	Change Mini card DET. PU resistor from 10K to 100K.
	20	P.29	0621	1A	Delete PBAT_ALERT# per M08 GPIO table removed.
	21	P.39-45	0621	1A	Update power schematic per ref power team updated schematic.
	22	P.22	0622	1A	Per TaiSol suggest, the CD2/WP2 is a dynamic pin; CD1 is a fixed pin, CD2 will touch CD1 when SD card insert into connector
	23	P.22	0622	1A	After discussion with the Taisol's FAE, pin-1 must connect to GND
	24	P.20	0622	1A	Ricoh check result: UDIO3 & UDIO4 apply NC required. Removed pull high resistor from UDIO3 and UDIO4.
	25	P.20	0622	1A	Ricoh check result: INTA# and INTB# interrupt line change required. Please apply PCI_PIRQC# interrupt line for INTA#, PCI_PIRQD# interrupt line for INTB#
	26	P.21	0622	1A	Ricoh check result: Shield GND for XTAL for XO/XI Please apply shield GND for XTAL for XO/XI to reduce external noise for XTAL.
	27	P.12,20	0627	1A	Changed REQ2/GNT2 to REQ1/GNT1 and swap PIRQD/PIRQC for C&G card reader+1394.
	28	P.12,35	0627	1A	Changed REQ3/GNT3 to REQ0/GNT0 and change PIRQB for C&G LOM.
	29	P.35	0629	1A	L90 changed to BLM11A601.
	30	P.24,25	0629	1A	Update PCI-E chennals. Update WPAN LED signal circuit.
	31	P.23	0629	1A	Delete SATA power2 for ref. Discrete schematic.
	32	P.9	0629	1A	De-populate C1 per Intel review update.
	33	P.13	0629	1A	Delete ICH_CL_RST1# per Intel review.Delete AMT_SMBCLK & AMTSMBDAT per not support AMT function.
	34	P.39	0703	1A	Added ALW power transfer circuit per power changed.
	35	P.25	0703	1A	Change ESD2 from CDA6C05GTH to SRV05-4 per refer Dawson schematic update.
	36	P.40-45	0704	1A	Power update schematic.
	37	P.29	0705	1A	The net name of IMVP6_PROCHOT# is for pin32 not for pin33. So, I change the the net name of IMVP6_PROCHOT# from pin 33 to pin 32.
	38	P.27	0707	1A	Ref Discrete schematic, changed the pin define of JCAMERA2 between pin 5 & pin6
					 QUANTA COMPUTER
					Title: EMI & Screw hole Size: Document Number C & G UMA Rev 2A Date: Friday, January 19, 2007 Sheet 49 of 60

Model	Item	Page	Date	Rev.	Description
C & G UMA	39	P.26	0707	1A	Ref Discrete schematic, Move R24 and C25 to DB.
	40	P.26	0707	1A	Ref Discrete schematic, Move R317 and C405 to DB.
	41	P.26	0707	1A	Ref Discrete schematic, Move C293 and C396 to DB.
	42	P.27	0707	1A	Ref Discrete schematic, Add a fuse on U64
	43	P.27	0707	1A	Ref Discrete schematic, Add a fuse on U67
	44	P.32	0707	1A	Ref Discrete schematic, added a net name SPEAKER_DET# on U21.4. Delete off-page connection from JSPK1.
	45	P.11	0707	1A	Ref Discrete schematic, deleted off-page connection from U25.AE10
	46	P.32	0707	1A	Ref Discrete schematic, added an offpage connection name SPDIF_SHDN on U21.30.
	47	P.37	0707	1A	Ref Discrete schematic, changed LED schematic of BT based on Discrete schemaitc. Remove U72, R23, D6 and Q7. Add Q?, R? and D? on page 37.
	48	P.29	0707	1A	Ref Discrete schematic, USIO.98 pull up to +3.3V_ALW through a 10k ohm.
	49	P.29	0707	1A	Ref Discrete schematic, USIO.66 pull up to +3.3V_ALW through a 10k ohm.
	50	P.29	0707	1A	Ref Discrete schematic, USIO.76 pull up to +3.3V_ALW through a 10k ohm.
	51	P.29	0707	1A	Ref Discrete schematic, USIO.29 pull up to +3.3V_ALW through a 10k ohm.
	52	P.29	0707	1A	Ref Discrete schematic, USIO.28 pull up to +3.3V_ALW through a 100k ohm.
	53	P.21	0710	1A	Per vendor check result, UDIO3 and UDIO4 pull-up resistor through a 10K ohm. (UDIO3 pull-up: SD enabled, UDIO4 pull-up: MMC enabled)
	54	P.24	0711	1A	Ref Discrete schematic, connect 0 ohm from J10 pin 22 to Sourth Bridge SB_WLAN_PCIE_RST#.
	55	P.12	0711	1A	Ref Discrete schematic, U25B.F18: change the net name from PCI_GNT2# to SB_WLAN_PCIE_RST#; Add 20K pull down resistor at U25B pin F18
	56	P.24	0711	1A	Ref Discrete schematic, connect 0 ohm from J9 pin 22 to Sourth Bridge SB_MCARD3_PCIE_RST#.
	57	P.12	0711	1A	Ref Discrete schematic, U25B.F8: connect 0 ohm population option to J9.22. GPIO table suggests that we add 20k pull down. Dis NO.
	58	P.25	0711	1A	Ref Discrete schematic, connect 0 ohm from J16 pin 22 to Sourth Bridge SB_WWAN_PCIE_RST#.
	59	P.12	0711	1A	Ref Discrete schematic, U25B.B19: change the net name from PCI_REQ2# to SB_WWAN_PCIE_RST#; Add 20K pull down resistor at U25B pin B19
	60	P.25	0711	1A	Ref Discrete schematic, UIM_DATA: add a 100pF(NC) capacitor at the point nearest the SIM connector.
	61	P.25	0711	1A	Ref Discrete schematic, change the net name of J16 pin 40 from USB_MCARD3_DET# to USB_MCARD2_DET#
	62	P.24	0711	1A	Ref Discrete schematic, change the net name of J9 pin 40 from USB_MCARD2_DET# to USB_MCARD3_DET#
	63	P.33	0711	1A	Ref Discrete schematic, Reserve SN74LVC1G125DBVR buffer and Add 0 ohm between buffer input and output pin for AUD_DMIC_CLK
	64	P.31	0711	1A	Ref Discrete schematic, Remove R451 between JTP1 pin 1 and +3.3V_ALW
	65	P.19	0711	1A	Ref Discrete schematic, Remove RP45,Q54 and Q55 from G_DAT_DDC2 and G_CLK_DDC2
	66	P.32	0711	1A	Per GG item 7 and Discrete schematic, C&G can remove this reserve circuit without no docking support. U59 pin1 pull down 10K. EC pin79 NC. Del R867
	67	P.19	0711	1A	Per GG item 7 and Discrete schematic, C&G can remove this reserve circuit without no docking support. U59 pin1 pull down 10K. EC pin79 NC. Del R867
	68	P.29	0711	1A	Per GG item 7 and Discrete schematic, C&G can remove this reserve circuit without no docking support. U59 pin1 pull down 10K. EC pin79 NC. Del R867
	69	P.32	0711	1A	Ref Discrete schematic, Reserve R603 and C315 at U21 pin 33
	70	P.32	0711	1A	Ref Discrete schematic, Reserve R441,C394 and C312 at U21 pin 1.
	71	P.32	0711	1A	Ref Discrete schematic, Remove 3.3V_LAN_PWRGD circuit.
	72	P.27	0712	1A	Ref Discrete schematic, Add common choke
	73	P.26	0712	1A	Common choke and capacitor move to DB, delete L25,R145,R142,C180,C183,C656,C654,C198.
	73	P.28 P.3	0712	1A	Ref Discrete schematic, USIO2.17 change the net name from DDR_ON to EC_CPU_PROCHOT# Ref Discrete schematic, U9.D21 connect to EC_CPU_PROCHOT# through a 0 ohm.
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Model	Item	Page	Date	Rev.	Description
C & G UMA	74	P.28	0712	1A	Ref Discrete schematic, Add net name ALW_PWRGD_3V_5V on USIO.18 Per GPIO table,Del. RC circuit. 100K and 0.1 uF.
	75	P.28 P.13	0712	1A	Ref Discrete schematic, USIO2.27 change the net name from SIO_SLP_S4# to DDR_ON and then add a 100k pull down. U25.AF21: change to TEST PAD
	76	P.28	0712	1A	Ref Discrete schematic and GG item 41, AUX_EN_WOWL add 100K pull down
	77	P.28	0712	1A	Ref Discrete schematic, change net name IMVP_PWRGD from USIO2 pin3 to USIO2 pin43.
	78	P.28	0712	1A	Ref Discrete schematic, add a off-page connection at USIO2 pin66
	79	P.28 P.13	0712	1A	Ref Discrete schematic, SB side add test pad. EC side ME_EC_ALERT change net name to LOM_SMB_ALERT# reserver pull high.
	80	P.28	0712	1A	Ref Discrete schematic,USIO2 pin 3 change signal name to DOCK_SMB_PME# and Add Pull up to +3.3V_ALW by 10K resister.
	81	P.28	0712	1A	Ref Discrete schematic,USIO2 pin 4 reserve 10K NC resister Pull high to +3.3V_ALW.
	82	P.28 P.18	0712	1A	Per GPIO pin table 0.1, UMA Use "LCDVCC_TST_EN" signal name for LCD TST.Change net name from EC_ENVDD to LCDVCC_TST_EN.
	83	P.28	0712	1A	Per Dell's Diag implementation and ref Discrete schematic,USIO2 pin 28 add 10K resister Pull high to +3.3V_ALW.
	84	P.32 P.29	0712	1A	Per GG list, AUD_HP_NB_SENSE/NB_MUTE# come into a AND gate output to U22 pin22 HP EN. Delete AUD_HP_NB_SENSE from USIO1 pin 81.
	85	P.29	0712	1A	Ref Discrete schematic, Delete R658 between USIO1 and NB_MUTE#
	86	P.29	0712	1A	Ref Discrete schematic, Add Pull down 100K.
	87	P.29	0712	1A	Ref Discrete schematic, USIO1 pin 95 add a off-page connection named WLAN_RADIO_DIS#
	88	P.29	0712	1A	Ref Discrete schematic, Add a TEST PAD on USIO1.35
	89	P.29 P.31	0712	1A	Ref Discrete schematic,USIO1 pin 61 Add 100K ohm and 0.047uF cap. RC circuit to+3.3V_ALW and serial 10 ohm resister. Change net name of JTP1 from LID_CL_SIO# to LID_CL#
	90	P.29	0712	1A	Ref Discrete schematic, delete net name DOCK_SIO_ALERT# from RP59
	91	P.29	0712	1A	Ref Discrete schematic, USIO1 pin 75 pull down through a 100k.
	92	P.29 P.23	0712	1A	Ref Discrete schematic, USIO1 pin 31 add an off-page connection named MODC_EN# Ref Discrete schematic, Reserve MODC_EN# circuit.
	93	P.12	0712	1A	Ref Discrete schematic, U25C pin AE19 pull high to +3.3V_SUS
	94	P.12	0712	1A	Ref Discrete schematic, U25C pin AC17 pull high to +3.3V_SUS
	95	P.12	0712	1A	Ref Discrete schematic, U25C pin AG21 pull high to +3.3V_SUS Ref Discrete schematic, add a off-page connection at AG21
	96	P.12	0712	1A	Ref Discrete schematic, add a off-page connection at F4
	97	P.12	0712	1A	Ref Discrete schematic, U25.AJ18 reserve 8.2K pull up to +3.3V_RUN
	98	P.12	0712	1A	Per GG list, DOCKED# should pull high to +3.3V_SUS.
	99	P.25	0712	1A	Ref Discrete schematic, delete off-page connection ICH_LAN_RST# and add TEST PAD
	100	P.12	0712	1A	Ref Discrete schematic, U25 pin AG19 pull down through a 100k
	101	P.17	0712	1A	Added C788-C793 per GG updated.
102	P.34	0712	1A	Added VCP2 circuit per GG updated.	
103	P.6	0713	1A	TV_DCONSEL_0 & TV_DCONSEL_1 connected to GND.	
104	P.11	0713	1A	Update LAN function circuit per ref Discrete update.	
105	P.12	0713	1A	SB_LOM_PCIE_RST# Pull High to +3.3V_RUN per ref GPIO recommend. SB_NB_PCIE_RST# pull down per refer Discrete added.	
106	P.13	0713	1A	Change SIO_EXT_SMI# pull up power from +3.3V_ALW to +3.3V_SUS.	
107	P.17	0713	1A	Update CLK Gen. circuit per GG & Discrete update.	
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C & G UMA	108	P.17	0713	1A	Update CLK Gen. circuit per GG & Discrete update.
	109	P.18	0713	1A	Update LVDS power control method per ref JM7.
	110	P.19	0713	1A	Update SPDIF CIRCUIT per ref Discrete & GG.
	111	P.24,25	0713	1A	Update WLAN,WPAN,WWAN circuit per GG requirement.
	112	P.26	0713	1A	Update MDC_RST_DIS# circuit per GG requirement.
	113	P.27	0713	1A	Correction USB connector side signals name.
	114	P.28,29	0713	1A	Update SIO circuit per ref GG requirement and GPIO list.
	115	P.32,33	0713	1A	Update Audio,AMP,SPK circuit per refer GG.
	116	P.39	0713	1A	Populated PC10,PC13,PC63,PC66 per GG requirement.
	117	P.39-45	0713	1A	Power updated schematic.(File name changed to FM5 MB UMA-0714_JM-5)
	118	P.46	0714	1A	Per ME's drawing, add clips.
	119	P.31	0714	1A	Depopulate RP61 per GG requirement
	120	P.27	0714	1A	Added C313 & C323 per GG requirement.
	121	P.6	0714	1A	Populate R411 per GG requirement.
	122	P.17	0714	1A	Populate R487 per GG requirement
	123	P.11,30	0714	1A	Changed RTC_BAT_DET# PU from P.30 to P.11 per GG requirement.
	124	P.12	0714	1A	Changed SB_LOM_PCIE_RST# to PD. Delete PCI_PIRQA# off page symbol.
	125	P.13	0714	1A	Added R529, De-pop R655, R657, C936 per GG requirement.
	126	P.16	0714	1A	Added C690,C702 per GG requirement.
	127	P.24	0714	1A	Populate Q67 per support Sniffer function.
	128	P.31	0714	1A	Removed C3 & R436 to DB per GG requirement.
	129	P.24	0717	1A	De-populate WoWL power SW circuit.
	130	P.17	0717	1A	Removed R429 & R859 per Vendor review update.
	131	P.9,28,38,39	0718	1A	Removed +1.8V_RUN power for UMA no need.
	132	P.31	0718	1A	Populate RP61 per provide TP AMB BUS driving.
	133	P.6,12,24 25,26,28	0718	1A	Split PLTRST to 2 single gate. PLTRST1# for WWAN?WLAN/WPAN/Express Card. PLTRST2# for MCH/SIO.
	134	P.37	0719	1A	Added BT circuit.
	135	P.25	0719	1A	De-populate C1249 per ref JM7 schematic update.
	136	P.39-45	0720	1A	Power update schematic.
	137	P.9	0720	1A	Added R429,R436,R456,R461 pull up/down for Crestline sighting report V:9.0 P.16 update.
138	P.6,12,28	0720	1A	Change net name from PLTRST2# to PLTRST# for same as Discrete.	
139	P.14	0720	1A	Change R253 package from 0402 to 0603.	
140	P.29	0724	1A	Delete R927, Change R929 value from 12K/F to 10K per SMSC revier updated.	
141	P.28	0724	1A	Changed R325&R265 vlaue from 1M to 47K per SmSC review updated.	
142	P.31	0724	1A	Added Media board LED control signal cirfuit, changed enable signals to low active per GG updated.	
143	P.29,33	0724	1A	Added CCD control power circuit, DMIC filter circuit, USB common choke circuit, per GG requirement.	
144	P.23	0724	1A	Added R927 and R595. Depopulate R917,R918 per GG updated.	
145	P.6	0724	1A	LCTLA_CLK/LCTLA_DATA changed to connect GND per GG updated.	
146	P.27,29	0724	1A	Change Signal net from Gilligan USB EN# to USB_BACK2_EN# per GG updated.	
147	P.24	0724	1A	Change Signal net PCIE_MCARD3_DET#/USB_MCARD3_DET# PU to +3.3V_SUS per GG updated.	
148	P.39-45	0725	1A	Update power schematic for layout requirement and checked updated.	
149	P.29	0727	1A	Added R647 for BC_DAT pull-up per Dell requirement.	
149	P.28,29	0727	1A	Update GPIO table per DELL update A12 include ITP_DBRESET# / BEEP / PS_ID	



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C & G UMA	1	24	9/18/2006	2A	Add SMBus isolation circuitry for WLAN.Add isolation circuitry for SMBus on WLAN.
	2	37	9/18/2006	2A	Update footprint name of D8.
	3	39- 45	9/21/2006	2A	Per Power schematic 0920, update power schematic.
	4	27	10/02/2006	2A	Update footprint name of JUSB2, and change to 8 pin.
	5	12	10/02/2006	2A	Delete ICH_USBP8+ and ICH_USBP8-
	6	19	10/02/2006	2A	Update footprint name of JVGA1.
	7	31	10/02/2006	2A	Update footprint name and QCI PN of JTP1.
	8	25	10/02/2006	2A	Update footprint name and QCI PN of JSIM1.
	9	11&23	10/16/2006	2A	Changed SATA port1 to port2 for Gilligan used.
	10	18	10/16/2006	2A	De-populate C45&C46 for LCD SMBUS rise/fall time issue.
	11	12&24	10/16/2006	2A	Update USB ports assigment
	12	18	10/16/2006	2A	Update LVDS per EMC requirement.
	13	35	10/23/2006	2A	Added L47, Change R66 to bead, Change L7 vlaue, Change C42, C69, C143, C145, C56, C114, C124, C144, C102, C126, C57, C146, C109, C70, C55, C148 pre Dell RF EMI requirement.
	14	36	10/23/2006	2A	Added L46 and changed C376 value for Dell RF EMI requirement.
	15	13	10/24/2006	2A	Change R67 value from 100K to 10K per GG list checked. Because GPIO update, Delete R67 by change item 49.
	16	34	10/24/2006	2A	Change R360 power up rail from +5V_SUS to +3.3V_SUS pwe GG updated.
	17	28 & 33	10/24/2006	2A	Per change Sniffer control same as M07 of GG list, Change Q55, Q56 from 3904 to DTA114YUA, delete R131, R132, R524, R525.
	18	28	10/24/2006	2A	Change R188&R189 value from 1M to 2.7K per GG requirement.
	19	23	10/24/2006	2A	Change HDD EN control power rail from +5V_ALW to +5V_ALW2 per GG requirement.
	20	13	10/24/2006	2A	Depopulate R329 and change R92 value from 10K to 8.2K per GG requirement.
	21	17	10/24/2006	2A	Change Single End serial damping value for fine tune value per GG requirement.
	22	11&37	10/25/2006	2A	Changed the LED control method. Move SATA LED mask to P.37. 1109 JM: Corrected LED of WLAN circuit.
	23	13	10/25/2006	2A	Depopulate R342, R352 per GG requirement.
	24	46	10/25/2006	2A	Pop C377, C407, C428, C383, C398, C10, C25, C319, C387 with 0.1uF caps for GG requirement
	25	24 & 25	10/25/2006	2A	Remove C252, C157, C253 per Mini-card no used +3V_LAN.
	26	24	10/25/2006	2A	Add R541 and non-populate for GG requirement, Changed PD on P.28
	27	24	10/25/2006	2A	Added 2 TP for GG requirement.
	28	25	10/25/2006	2A	Added R542 and non-populate per GG requirement.
	29	24 & 37	10/25/2006	2A	Moved the LED_MASK# circuit to 37 and followed GG to update BT LED control method, for this change, added R543,R544, Q67,Q68. Change Q11 from DTA114YUA to 2N7002W-7-F. Change R383 from 10K to 100K. Change R128 from 220 to 2K.
	30	24	10/25/2006	2A	Change the net of pin 5 of J4 from "COEX1_BT_ACTIVE" to "COEX1_BT_ACTIVE_Mini" per GG requirement.
	31	37	10/25/2006	2A	Change the net of pin 6 of J2 from "COEX1_BT_ACTIVE" to "COEX1_BT_ACTIVE_DC" pre GG requirement
	32	37	10/25/2006	2A	Added U34 Circuit per GG requirement.
	33	33	10/25/2006	2A	Update Audio DB BTB circuit per update connector pin define.
	35	11	10/27/2006	2A	Change CODEC bitclok with 10 ohm damping resistor per GG requirement.
	36	24	10/27/2006	2A	Added "BT_ACTIVE#" with 0_NC on J3.46 per GG requirement.
	37	17	10/27/2006	2A	Change RP10 from 33 to 10, RP3, RP5 from 33 to 22 per EA updated.
	38	17	10/27/2006	2A	Pop C71, C395, C113, C108, C104, C116 with 22p caps per GG requirement.
	39	39	10/27/2006	2A	Change +3.3V_SUS & +5V_SUS EN power up to +5V_ALW2 per GG requirement.
	40	32	10/27/2006	2A	Change C331, 332 to 0.033uF/16V/X7R/1206 & C351, C354 to 1uF/16V/X7R/1206 per Gg requirement.
	41	29	10/27/2006	2A	Depopulate EC non control resistor. Dell don't agree to do it.
	42	28	10/27/2006	2A	Depopulate EC non control resistor. Dell don't agree to do it.
	43	13&28	10/27/2006	2A	Per GPIO A14, changed U11.AG22 to LOM_SMB_ALERT#.
	44	28&29	10/27/2006	2A	Per GPIO A14, Swap DOCK_SMB_ALERT# and DOCK_SMB_PME.



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C & G UMA	1	29	21/12/2006	3A	Add R564,move the 'PLATFORM_BID' signal from SATA DB to MB							
	2	34	21/12/2006	3A	Pop Q48, per JM's mail.							
	3	35,36	21/12/2006	3A	Base on internal notice,Change L7,L46 P/N from CX8LM152000 to CX5LM152000;L47,R66 P/N from CX5LM152000 to CX8LM152000.							
	4	17	21/12/2006	3A	Base on internal notice, L65: Change QCI PN from CS00003J951 to CX08T250000							
	5	18	21/12/2006	3A	Base on internal notice, Delete location C26 at CH31004KB17							
	6	37	21/12/2006	3A	Per "Reference Schematic & Checklist Updates" mail, Change R560 from 0 to 10K							
	7	46	01/02/2006	3A	Add a TH.							
	8	32,33	01/02/2006	3A	Per EMI request, to reserve the filtering components for MIC signals.							
	9	22	01/02/2006	3A	Add a switch, to prevnet XD card no detect issue. 0110: Reserve R570							
	10	39-45	01/02/2006	3A	Power update schematic.							
	11	14	01/03/2006	3A	C482 change the footprint to CC0402-C.							
	12	32	01/04/2006	3A	Per GG list item 2:add 100kohm resistor (R567) between pin 40 and +3.3V_RUN and a 1000pF cap (C672 below) from Pin 40 to ground							
	13	28,29	01/04/2006	3A	Per GG list item 3:DOCK_SMB_PME# should be pulled up to +5V_ALW DOCK_SMB_ALERT# should be pulled up to +3.3V_ALW							
	14	24	01/04/2006	3A	Per GG list item 6: add series resistors(0ohm) on host debug signal.							
	15	24	01/05/2006	3A	Per GG list item 7: Change the pin BT_ACTIVE# to LED_WPAN#							
	16	24	01/05/2006	3A	Per GG list item 10: Add a series 0ohm resistor on the trace of pin 46 of J3							
	17	37	01/05/2006	3A	Per GG list item 11: Delete the offpage connection of BT_ACTIVE#							
	18	37	01/05/2006	3A	Per GG list item 12:Add a 10K pull down on J2 pin2. and R190 100K NC.							
	19	31	01/05/2006	3A	Per GG list item 13: Change TP MB connector JTP1 pin9 from +3.3V_RUN to +5V_ALW							
	20	28	01/05/2006	3A	Per GG list item 17: NC R382							
	21	29	01/05/2006	3A	Per GG list item 20: BIOS ROM 1M change to 2M							
	22	32	01/05/2006	3A	Per GG list item 24: Pop R274							
	23	17	01/05/2006	3A	Per GG list item 18: R96 change to 2.2K							
	24	33	01/05/2006	3A	Per GG list item 19: CCD soft-start circuit correct and Add reserve 0 ohm for remove Camera VCCD_ON. JM: For layout placement spacing concern, I need removed R569,R570,R571,R572.							
	25	12,27	01/05/2006	3A	Per GG list item 25: USB_OC4_8# channel separate							
	26	46	01/08/2006	3A	Per Derating report, C383,C377,C398,C10,C25,C319,C387,C16,C19,C324 change part number to CH41004M912							
	27	37	01/08/2006	3A	Per GG list item 15, R67 47K change to 0 ohm and R561 10K change to 47K.							
	28	23	01/08/2006	3A	Per GG list item 1:+5V_ALW2 changes to +3.3V_ALW2 Pop R576, Depop R546							
	29	12,13	01/08/2006	3A	Per GG list item 15: PCIE_MCARD2_DET# from GPIO20 to ICH8 GPIO5/PIRQH# pin B3.(GPIO20 add test pad)							
	30	13	01/08/2006	3A	Per GG list item 15: Add R577 (4.7K) series resistor at ICH8 pin AH12 (USB_MCARD1_DET#).							
	31	21	01/08/2006	3A	Depop C266, for R5C833							
	32	30	01/08/2006	3A	Delete RTC battery PN for moving to ME BOM							
	33	20,21	01/08/2006	3A	Change U15 PN from 5C832 to R5C833							
	34	14,19,31 37,38,39	01/09/2006	3A	RF had request split +5V_RUN for 14MHz noise fine tune resistor PR66 on PT stage. Now removed PR66 and change net name from +5V_RUN2 to +5V_RUN.							
	35	17	01/10/2006	3A	Per fine-tune table, change PR3 from 22 ohm to 10 ohm.							
	36	17,28	01/10/2006	3A	Per fine-tune table, change R97 from 100ohm to 51 ohm,and pop R129,C113 change to 10P,Pop C141 and change to 2.2P							
	37	17,20	01/10/2006	3A	Per fine-tune table, change R98 from 100ohm to 10 ohm,and pop R198 and change from 10 to 22, C116 change to 10P, Pop C215 and change to 1P							
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