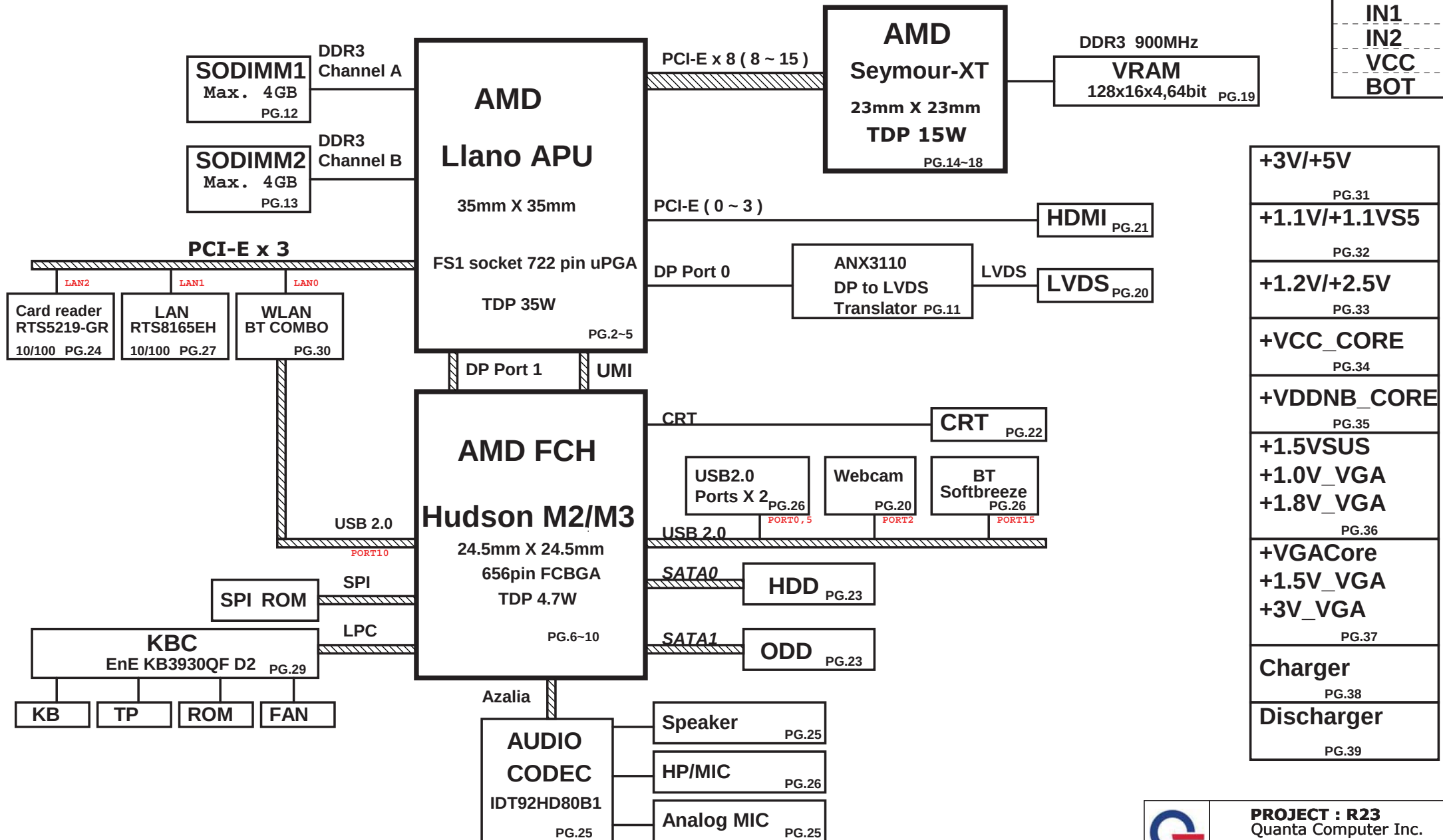
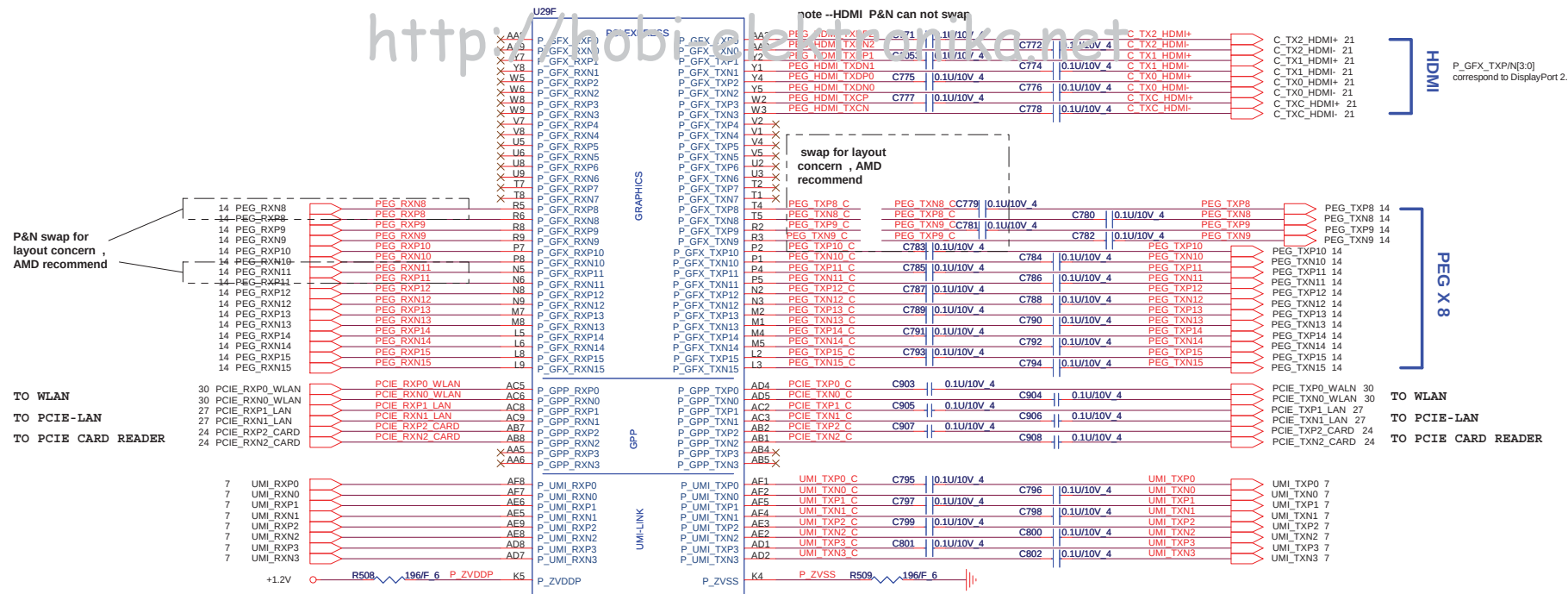


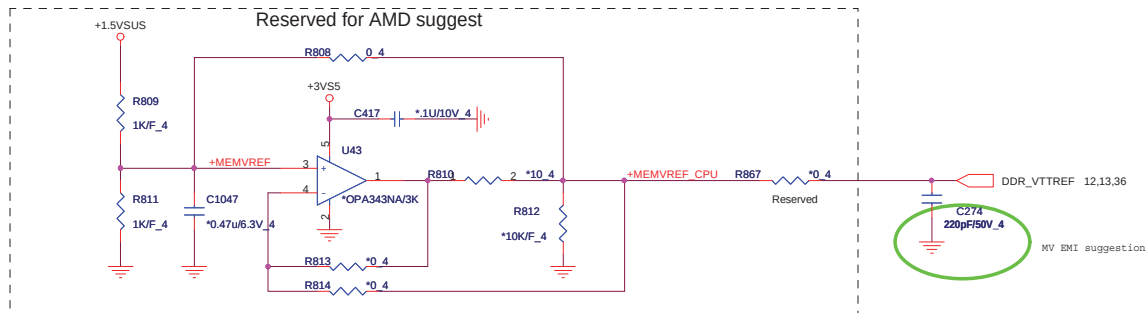
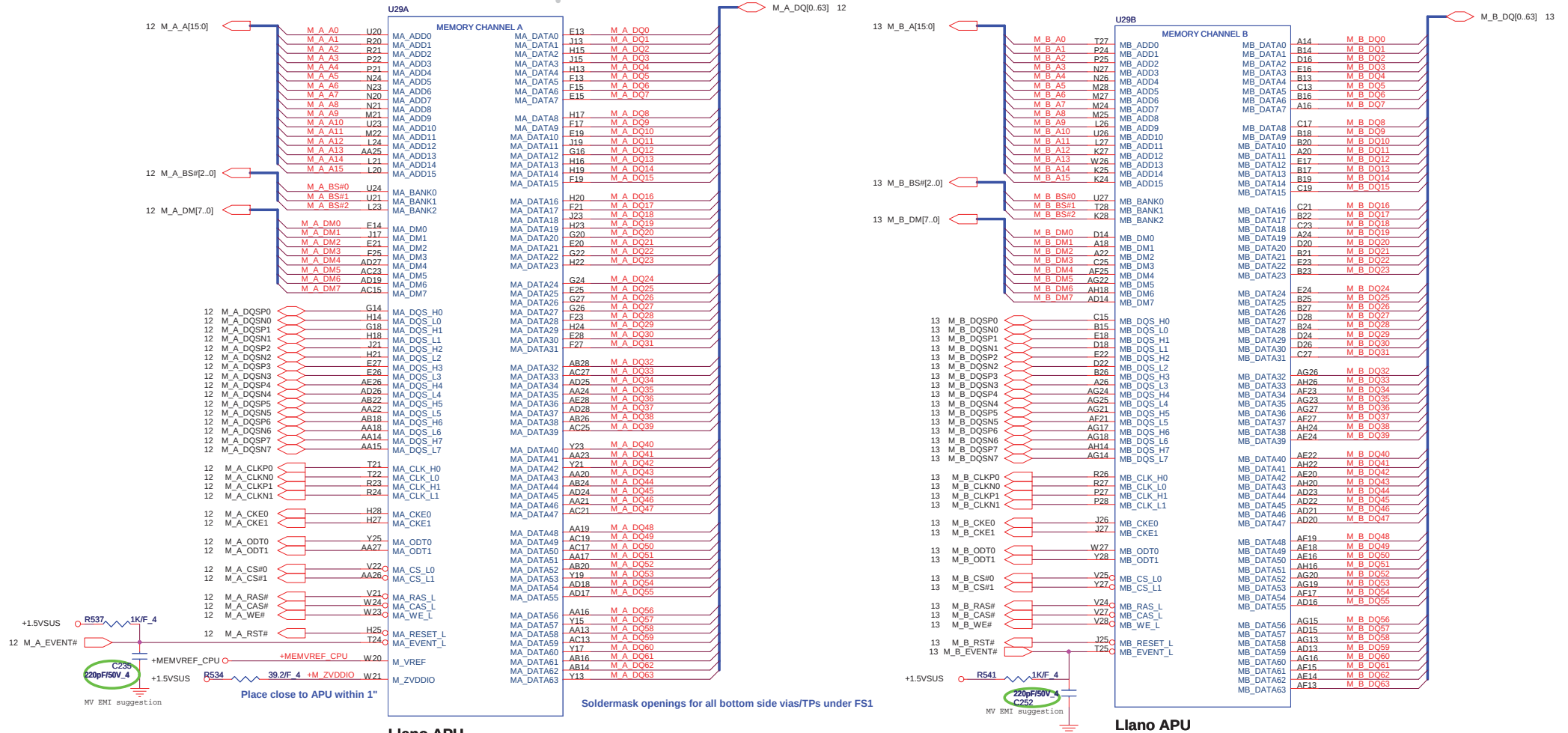
R23 AMD Sabin UMA/Muxless SYSTEM DIAGRAM

Stackup

TOP
GND
IN1
IN2
VCC
BOT

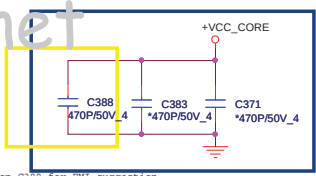




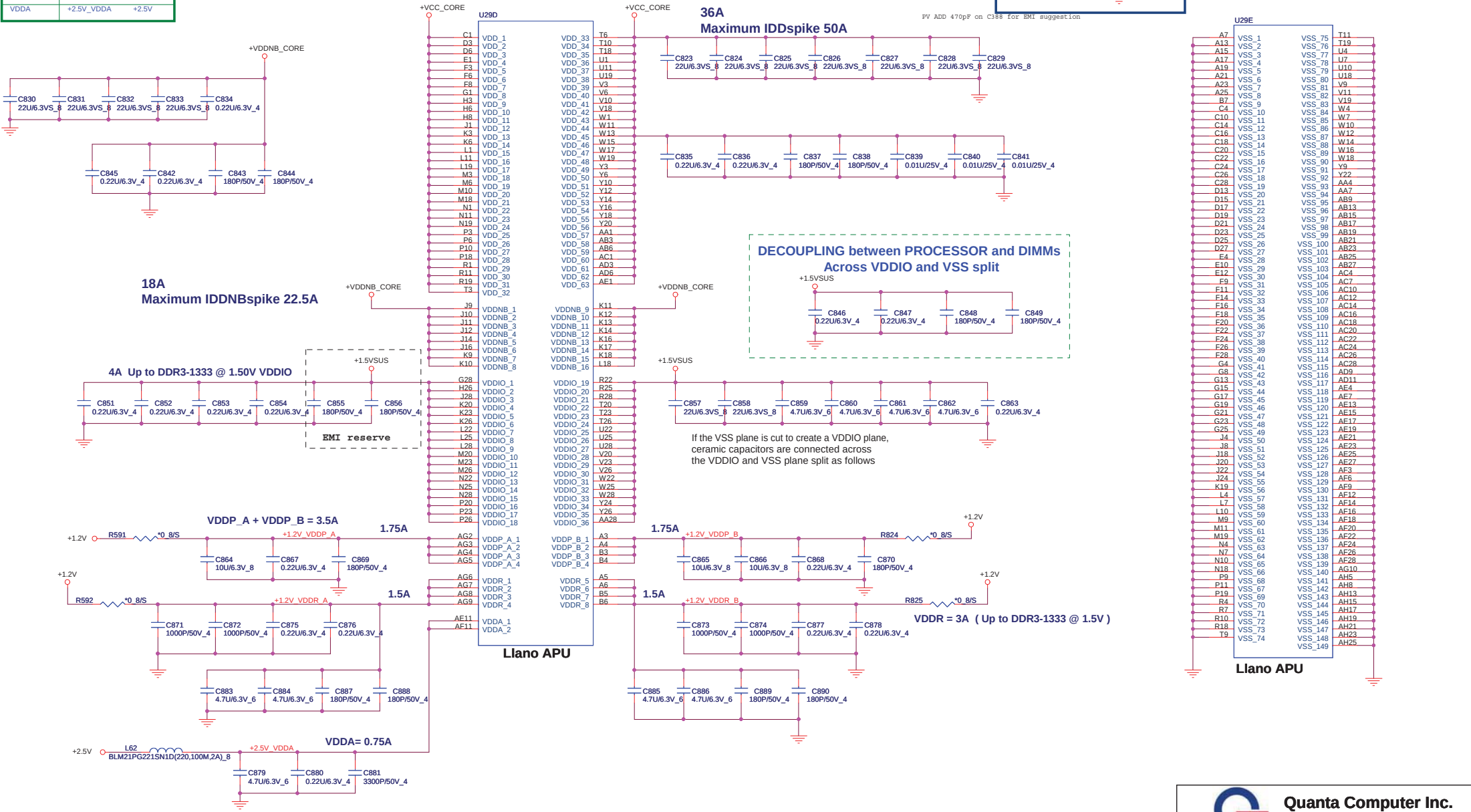




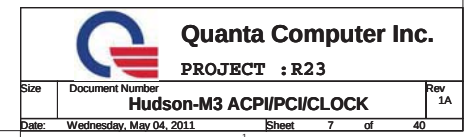
APU POWER TABLE		
PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

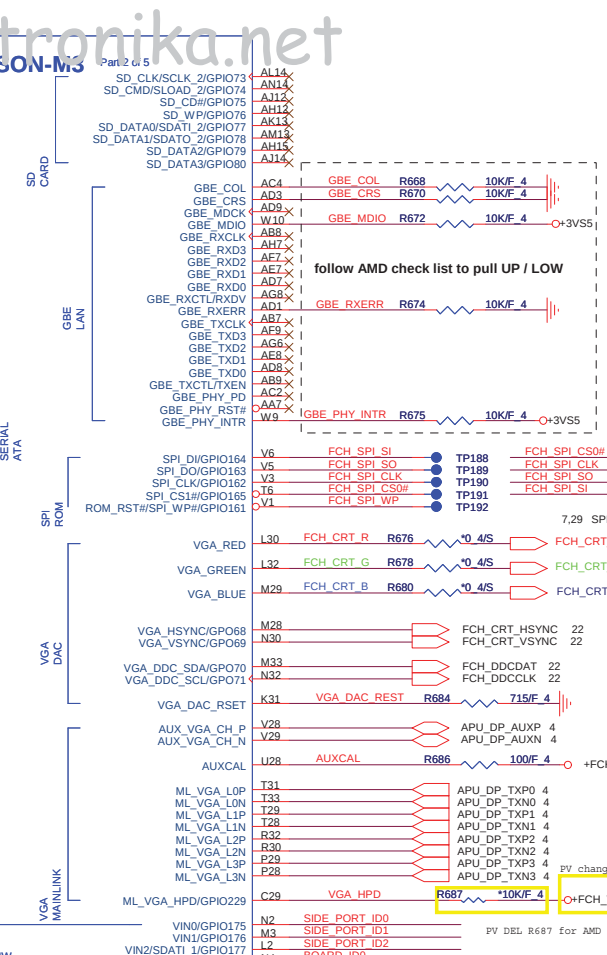
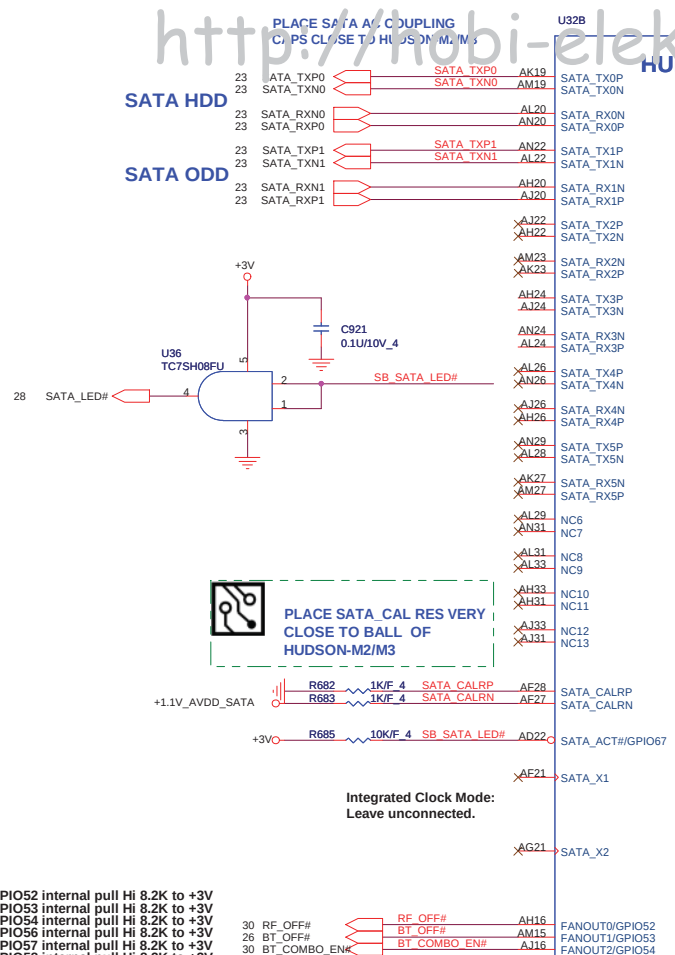
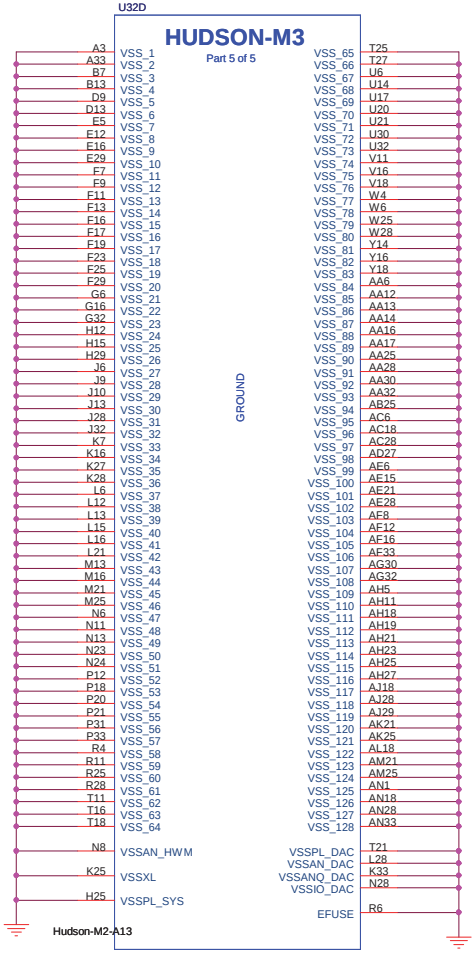


SI EMI

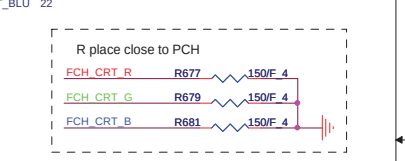
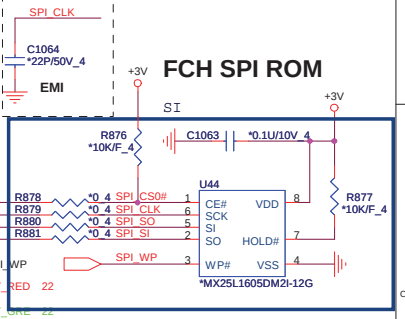


Llano APU

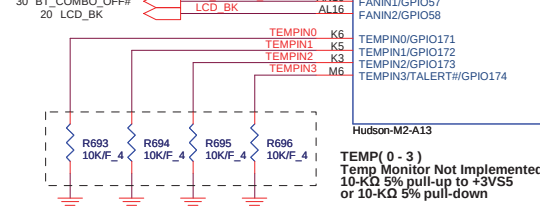




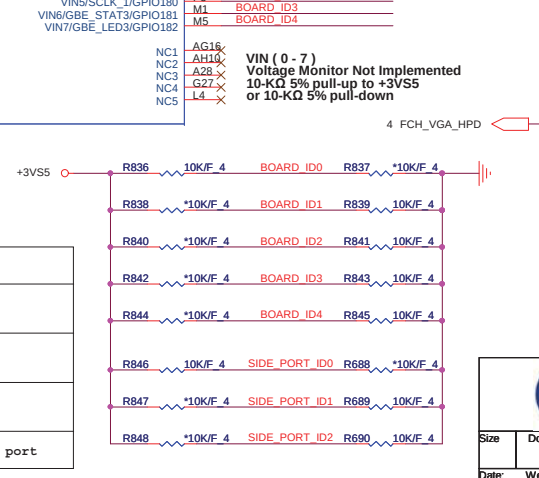
Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FF0N01
Socket		DFHS08FS023

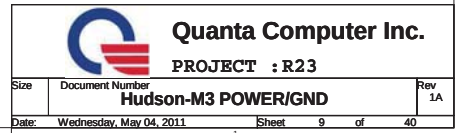


ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12



SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port

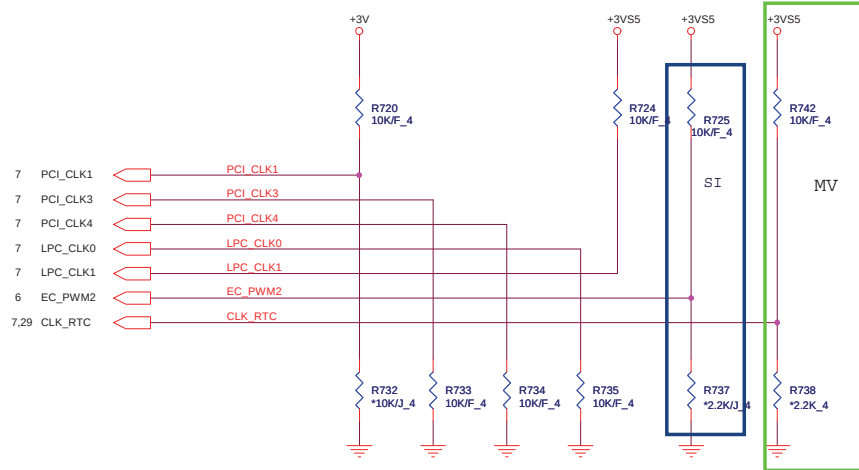




STRAPS PINS



OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE ENABLED

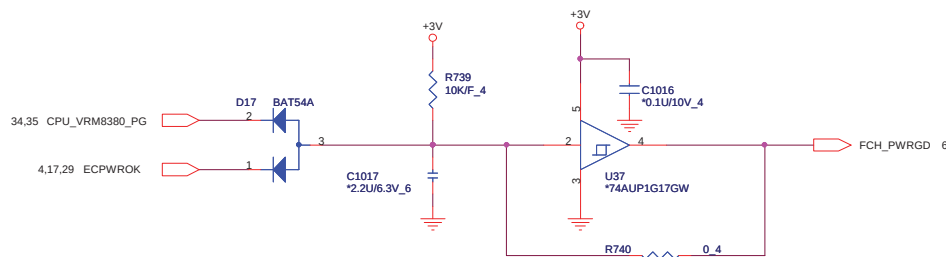
DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH_PWRGD



Quanta Computer Inc.

PROJECT : R23

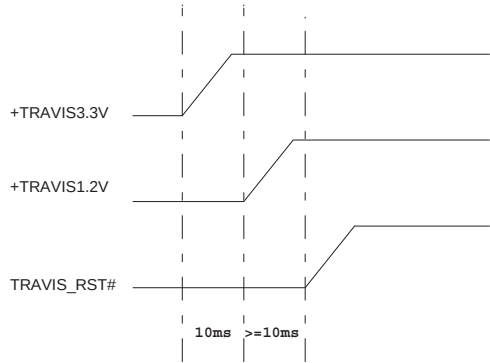
Size	Document Number	Rev
	Hudson-M3 STRAP/PWRGD	1A

Date: Wednesday, May 04, 2011 Sheet 10 of 40

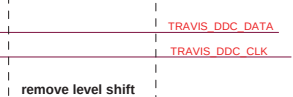
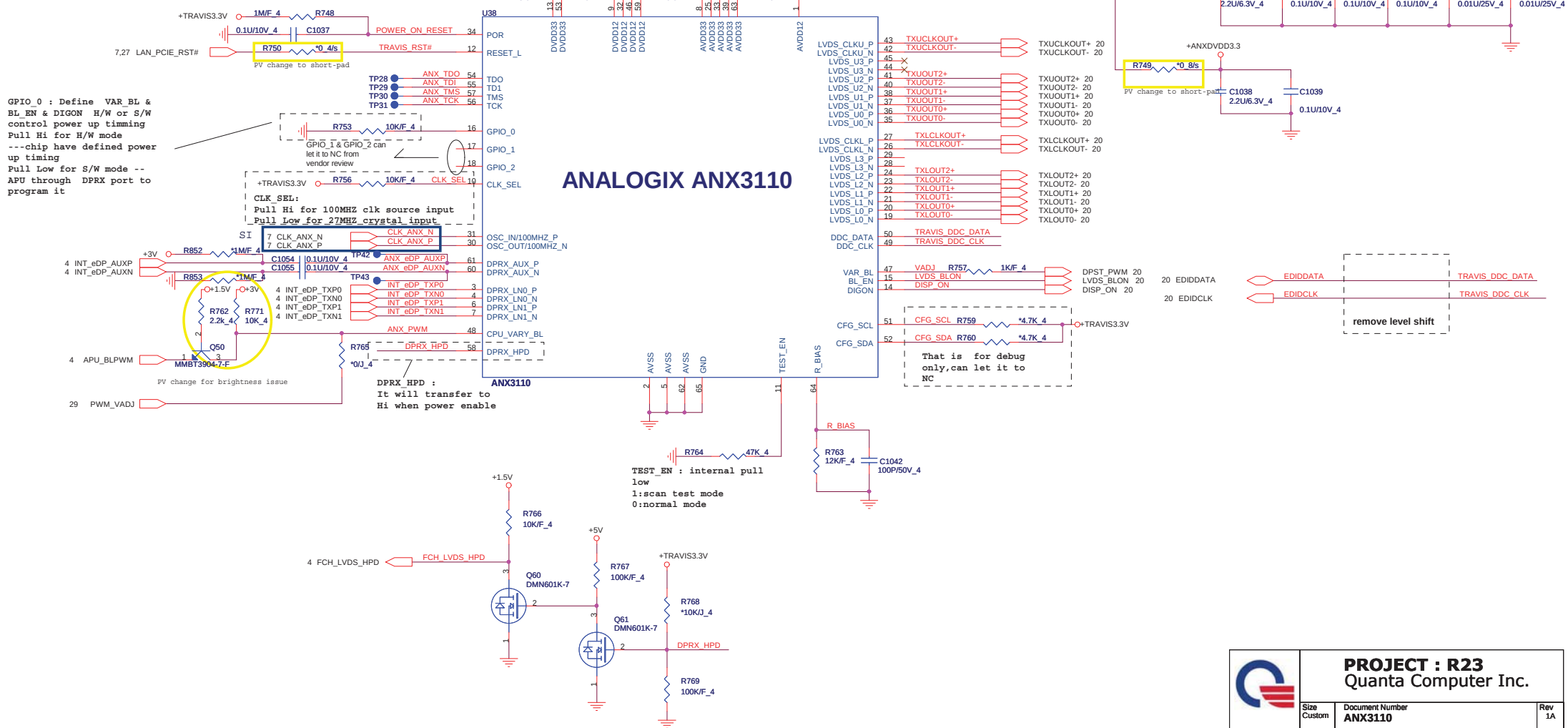
ANX3110 Power Up Sequence

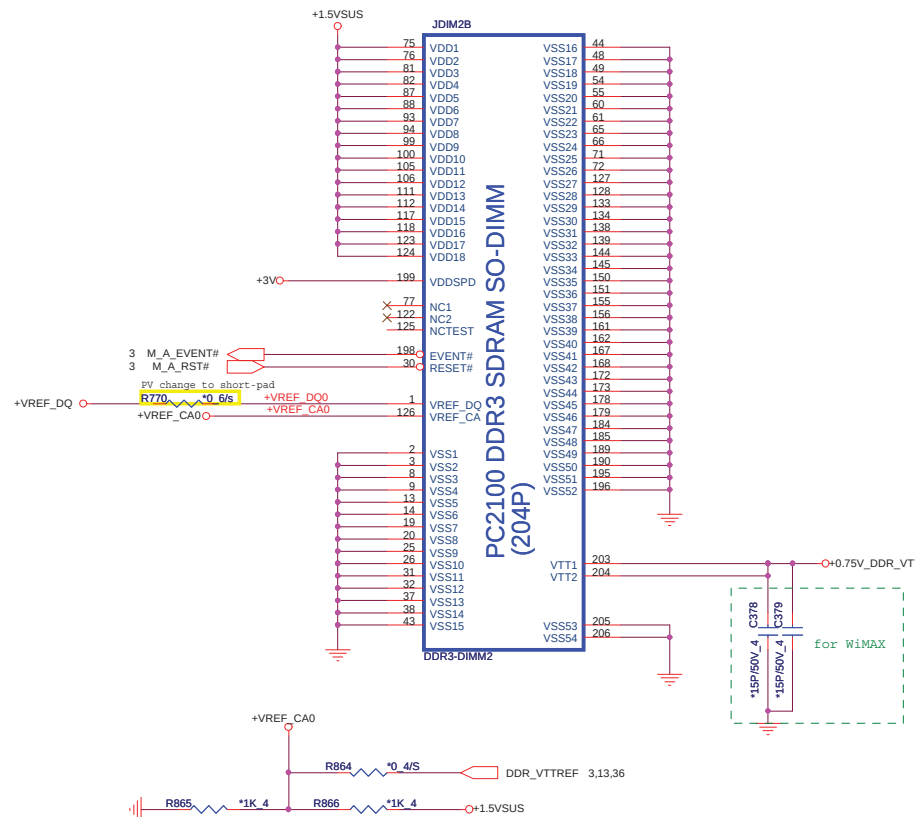
http://hobi-elektronika.net

11

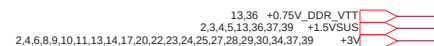
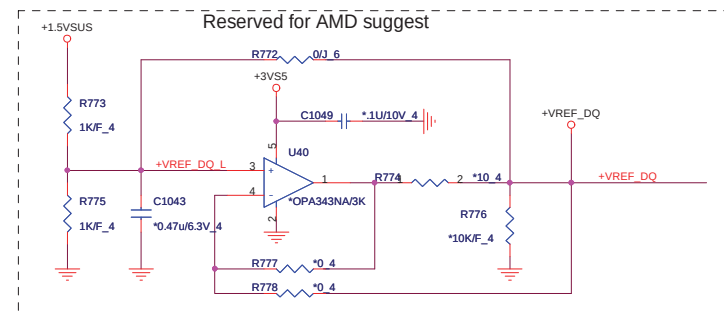
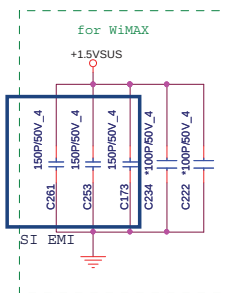


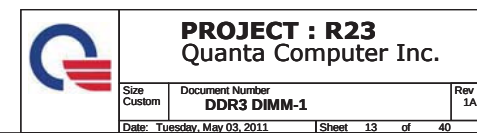
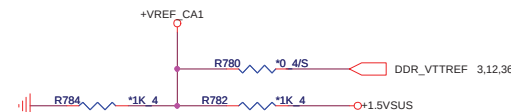
GPIO_0 : Define VAR_BL & BL_EN & DIGON H/W or S/W control power up timing
Pull Hi for H/W mode
---chip have defined power up timing
Pull Low for S/W mode -- APU through DPRX port to program it

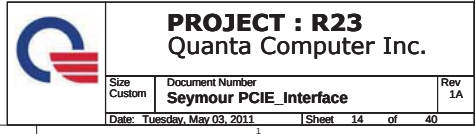


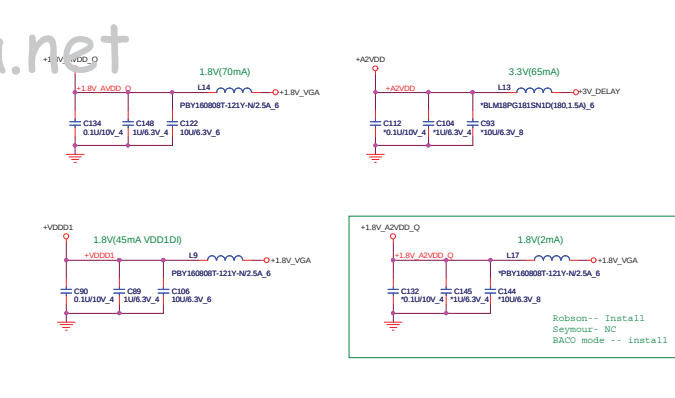
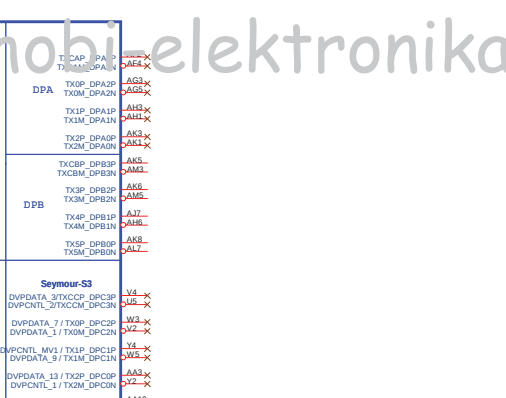
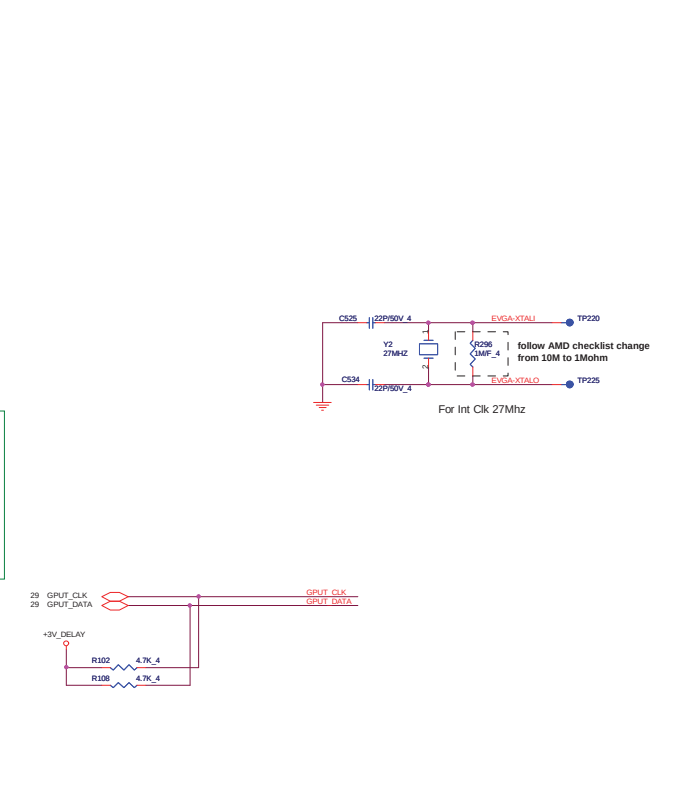
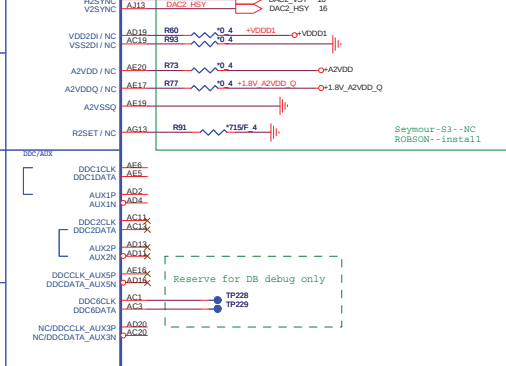
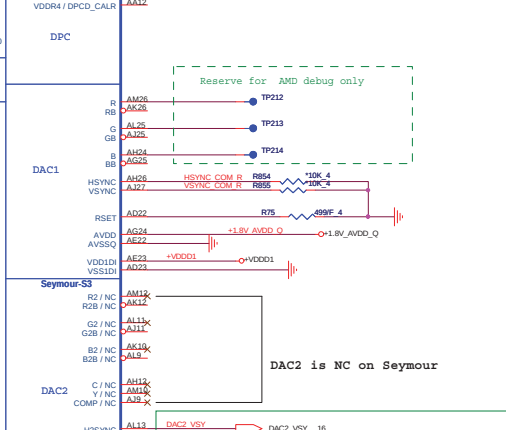


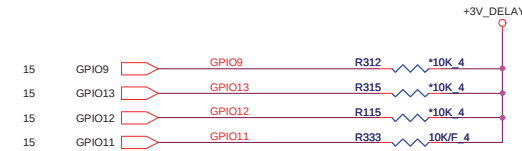
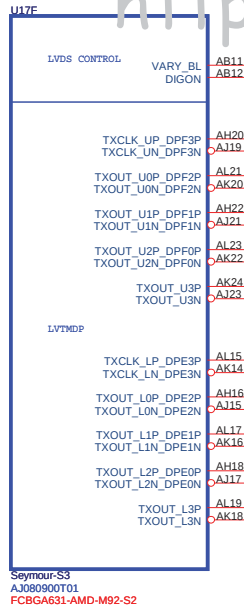
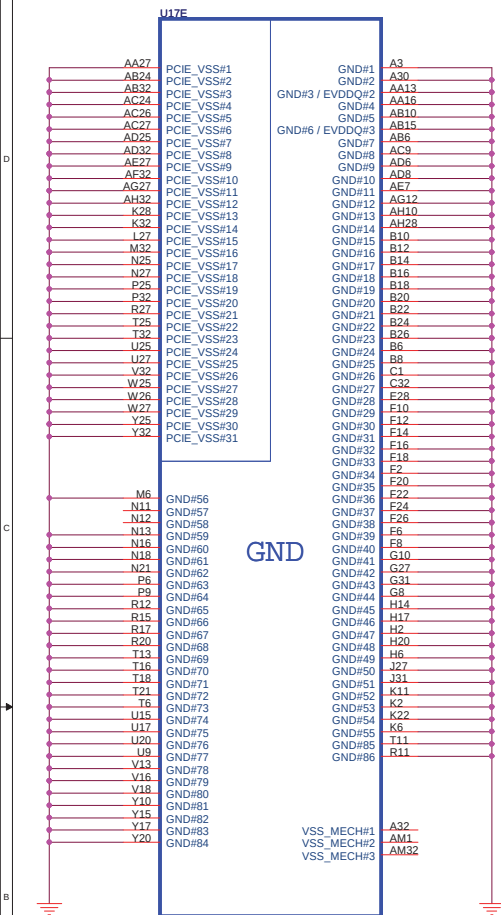
H9 . 2mm



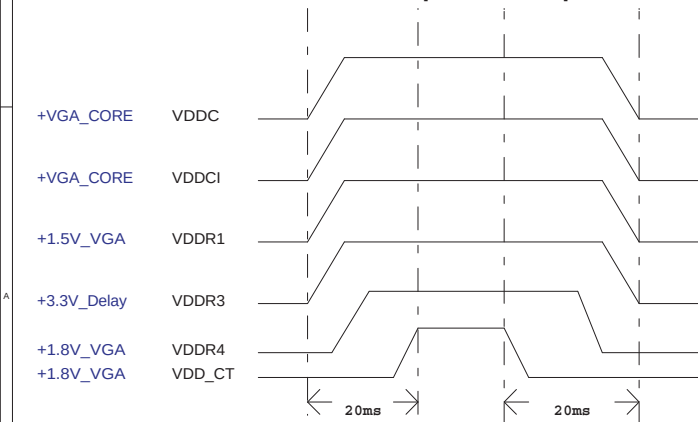




[illegible][illegible]



Power Up/Down Sequence



Memory Aperture size

GPIO9		GPIO13	GPIO12	GPIO11
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRs_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

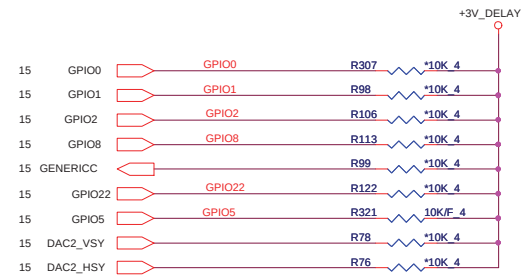
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN



15,17 +3V_DELAY

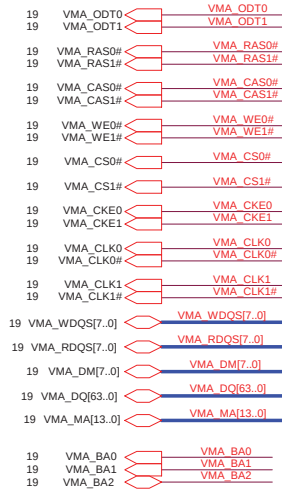


PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour GND / LVDS/ Straps	1A
Date: Tuesday, May 03, 2011	Sheet 16 of 40	

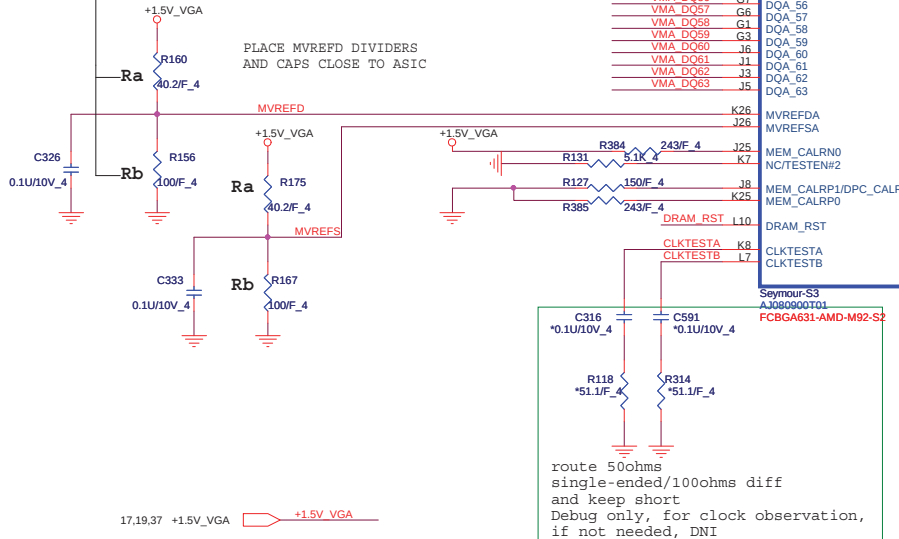


	PROJECT : R23 Quanta Computer Inc.		
	Size Custom	Document Number Seymour_Power_and_NC	Rev 1A
	Date: Tuesday, May 03, 2011	Sheet 17 of 40	

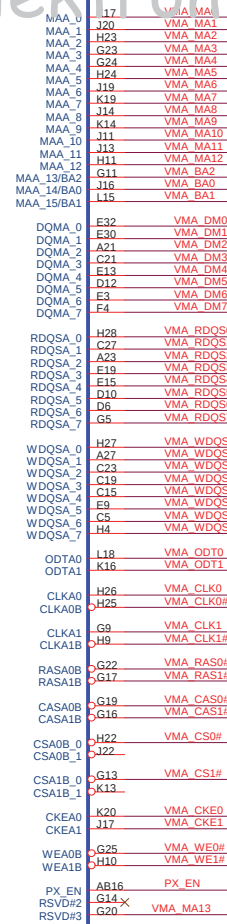


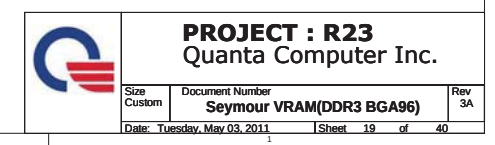
support 1Gbit
VRAM (64M X 16)

DIVIDER RESISTORS	GDDR5	DDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R

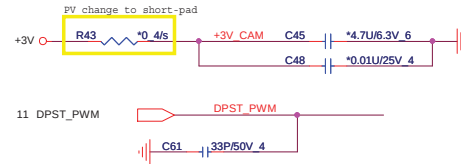
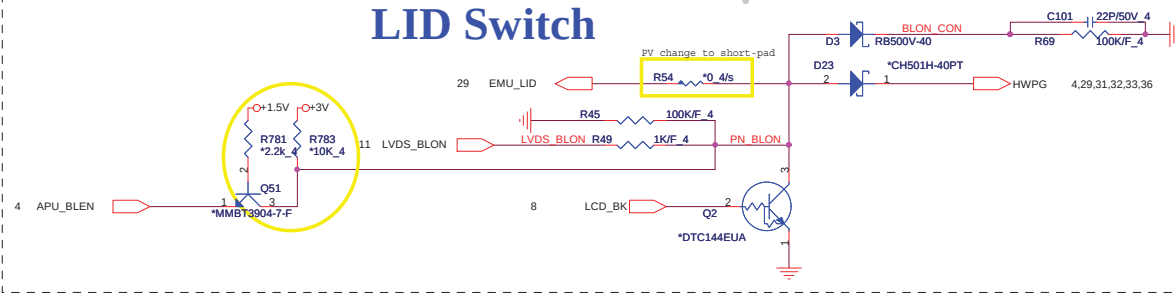


MEMORY INTERFACE

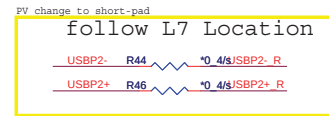
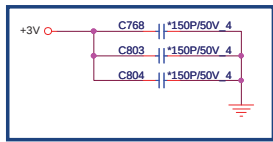




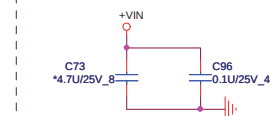
LID Switch



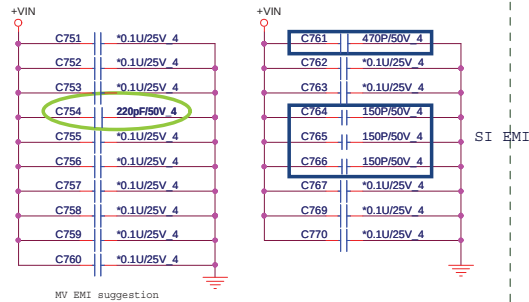
SI EMI



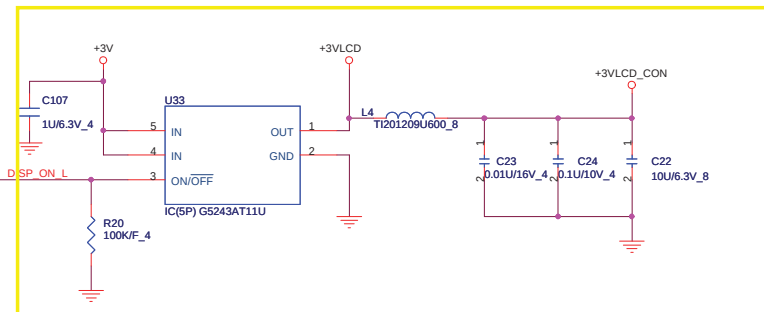
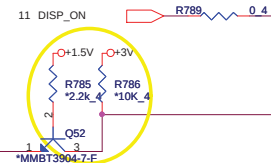
EMI & RF



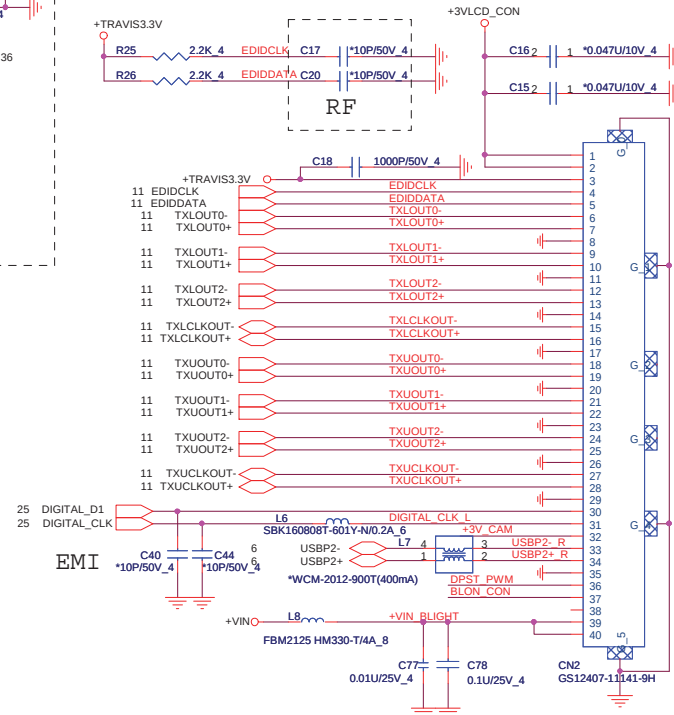
Coupling CAP.



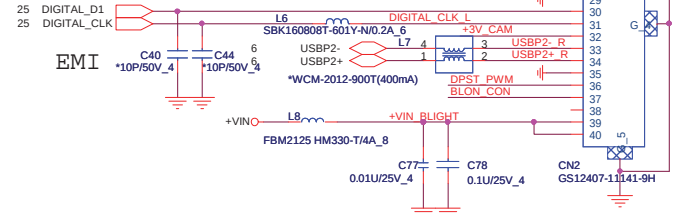
MV EMI suggestion



PV change for reduce circuit!



EMI

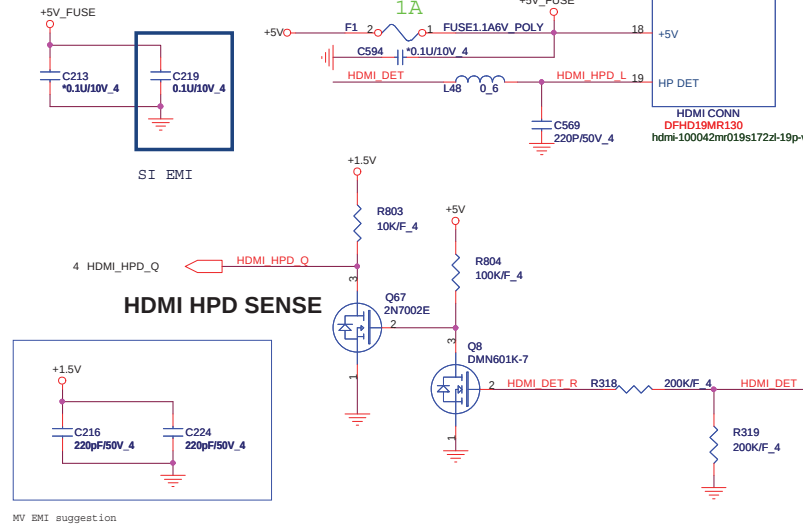
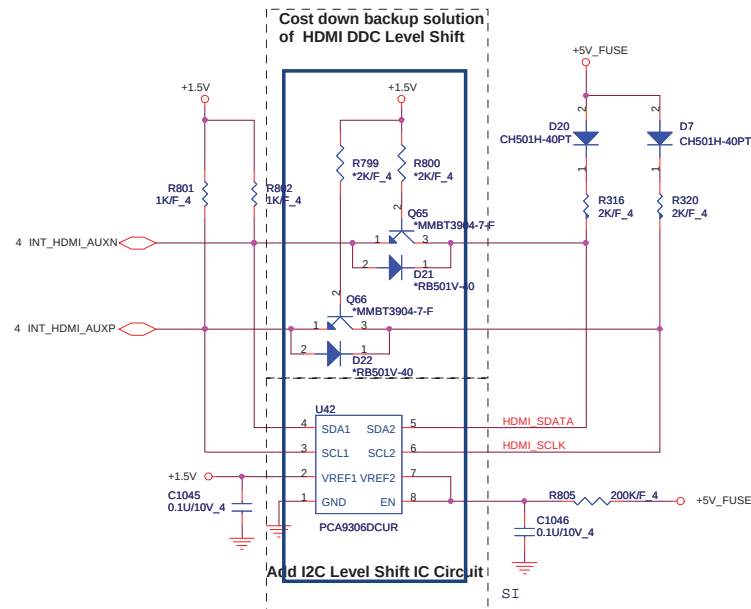
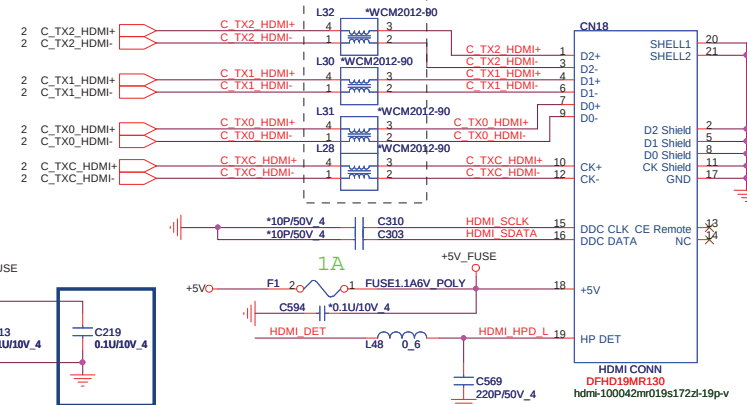
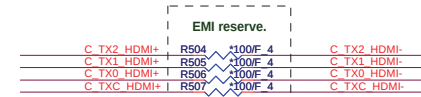
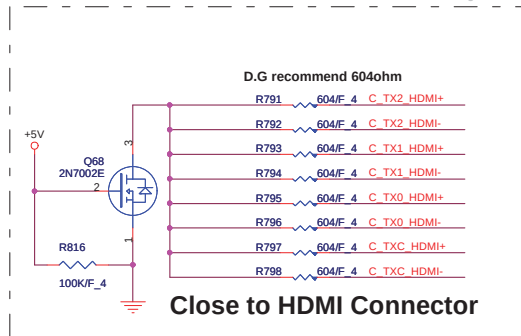


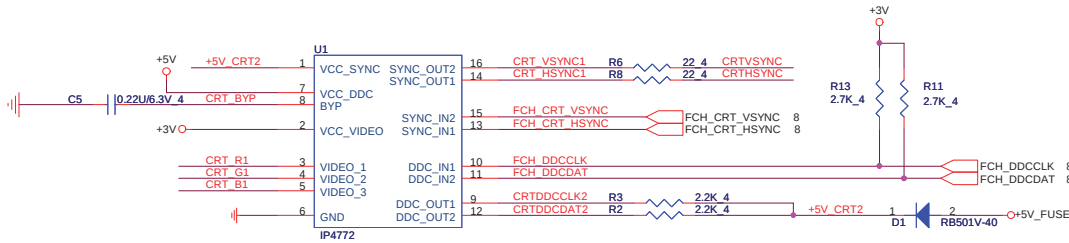
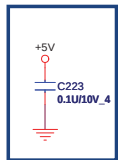
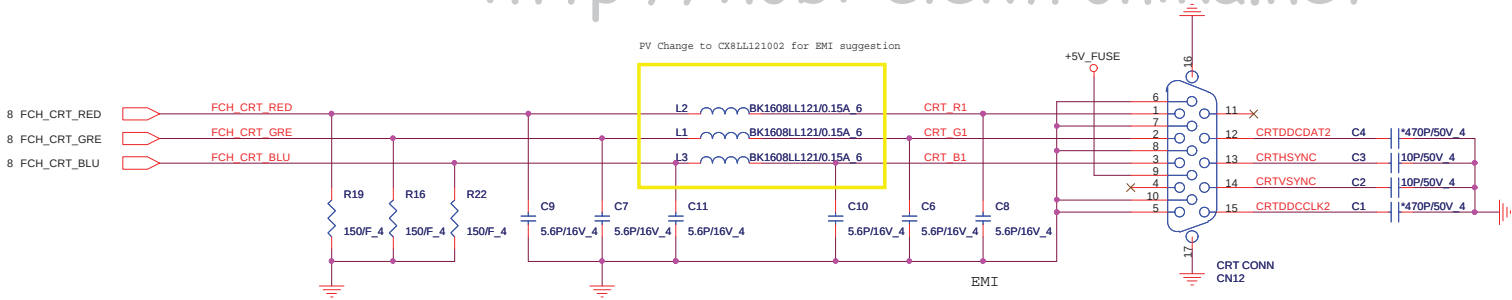
4,7,26,28,29,31,38 +3VPCU
2,4,6,8,9,10,11,12,13,14,17,22,23,24,25,27,28,29,30,34,37,39 +3V
9,37,38,39 +12VALW
31,32,33,34,35,36,37,38,39 +VIN



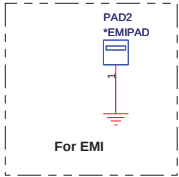
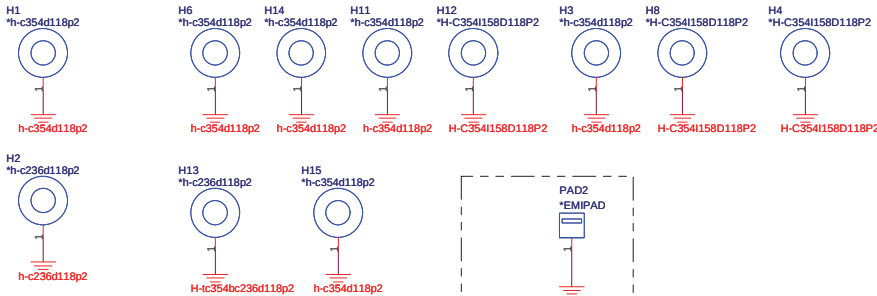
PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
Date: Tuesday, May 03, 2011	Sheet 20 of 40	

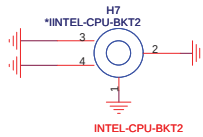




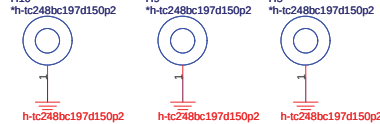
HOLE



CPU



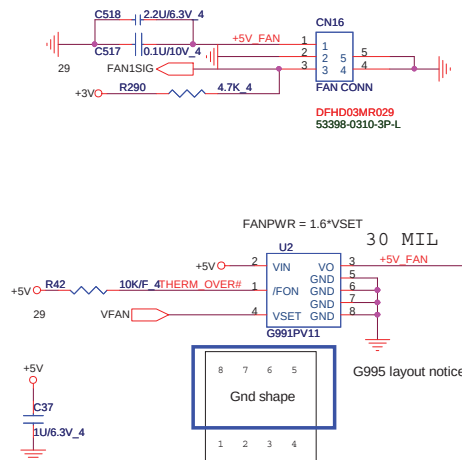
VGA



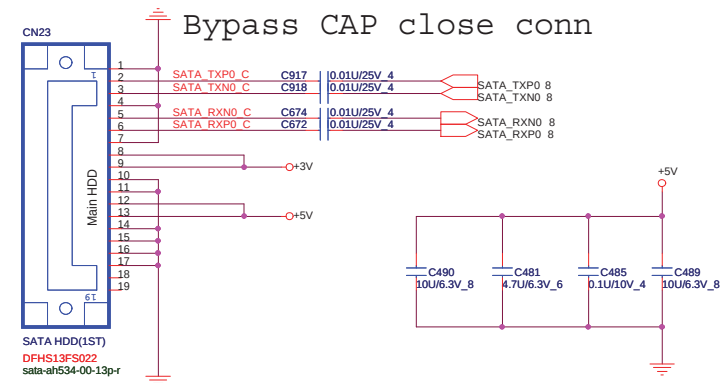
PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT,Hole	1A
Date: Tuesday, May 03, 2011 Sheet 22 of 40		

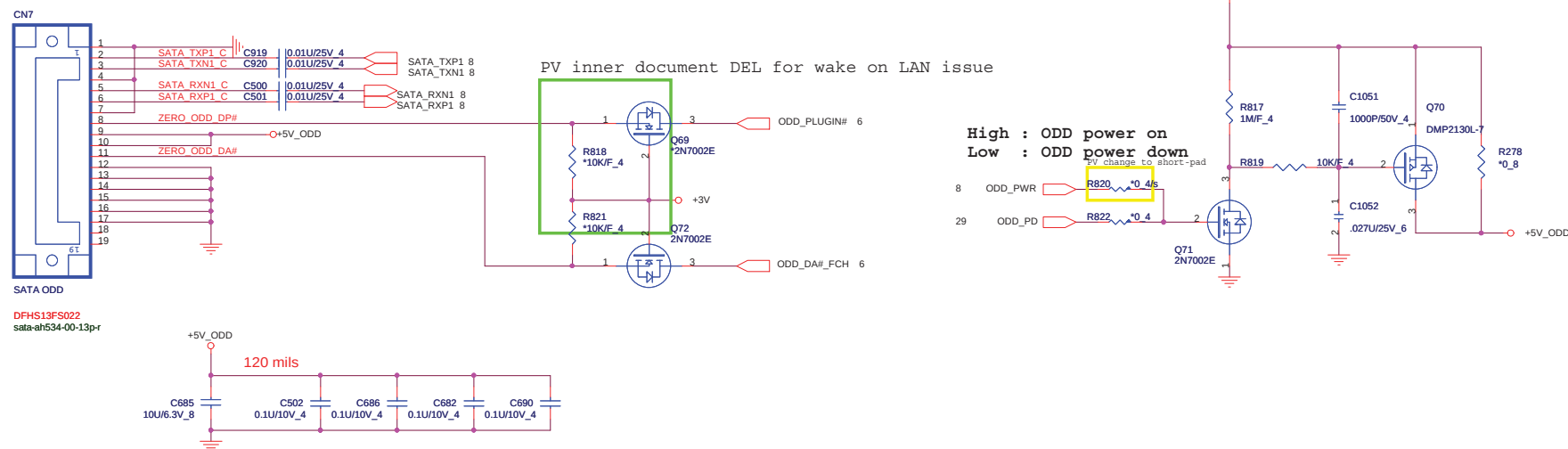
CPU FAN

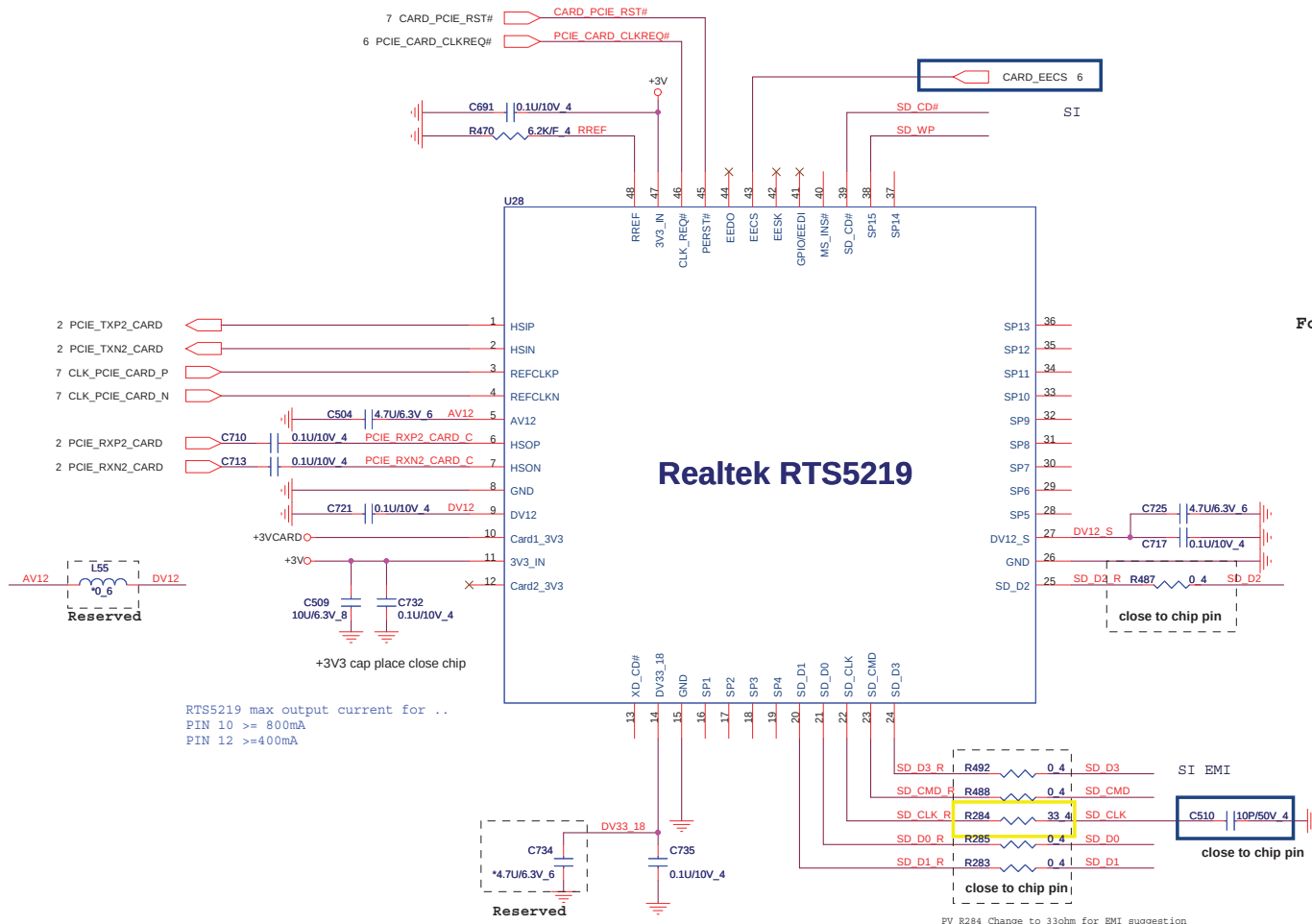


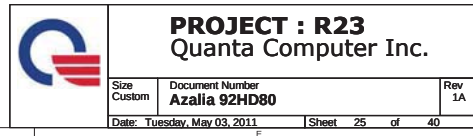
SATA HDD CONNECTOR

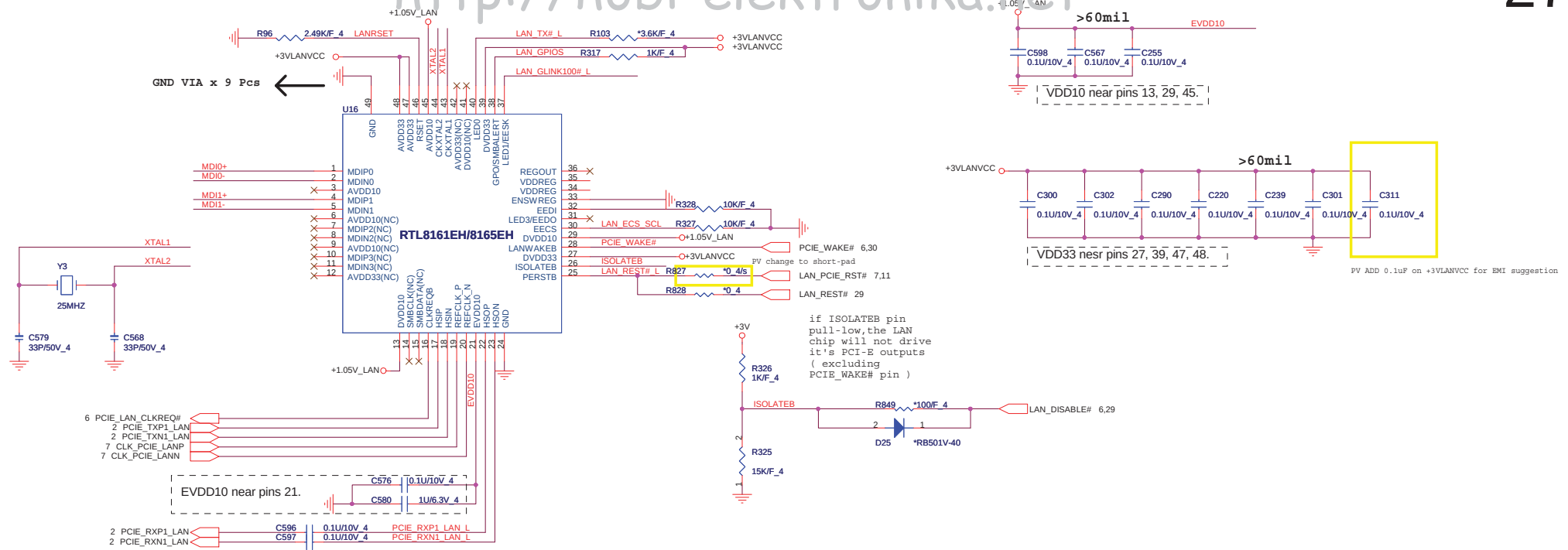


SATA ODD CONNECTOR SATA ODD

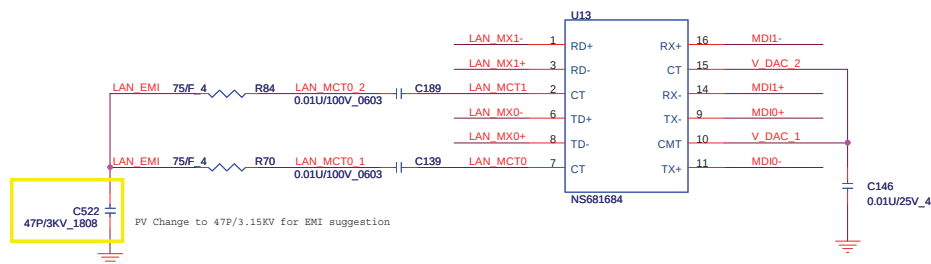




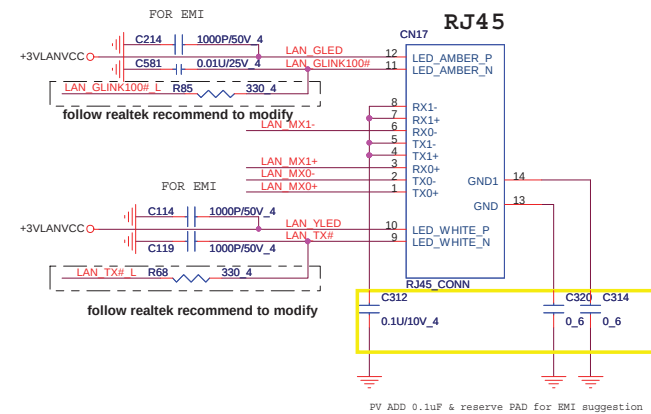




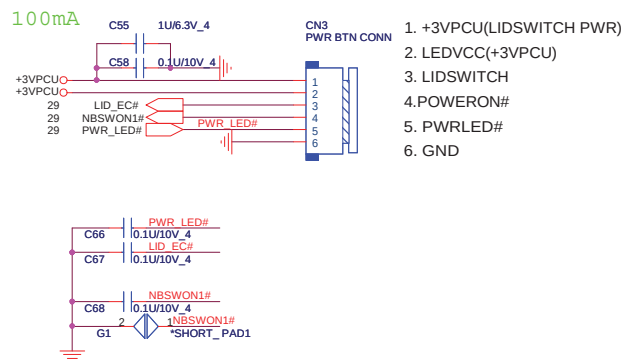
Transformer for 10/100



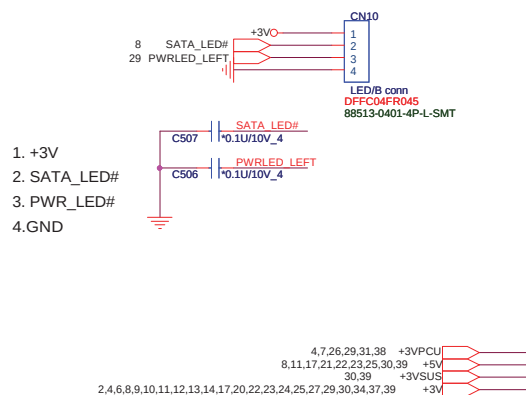
Lan Con.



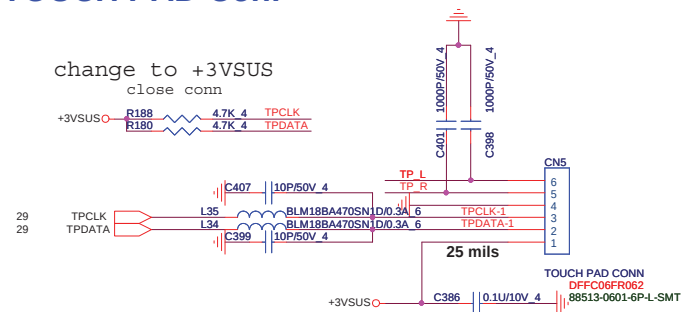
POWER BOTTON CONNECT



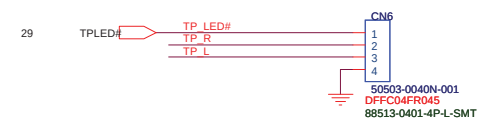
LED Con.



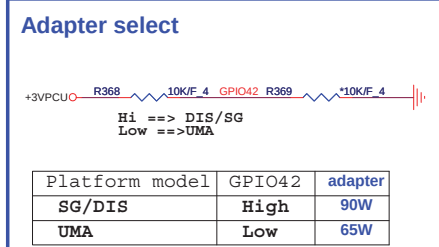
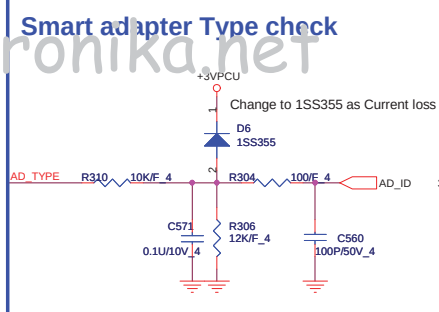
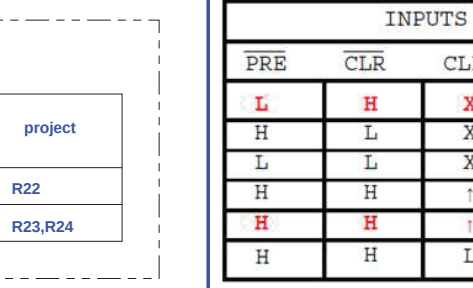
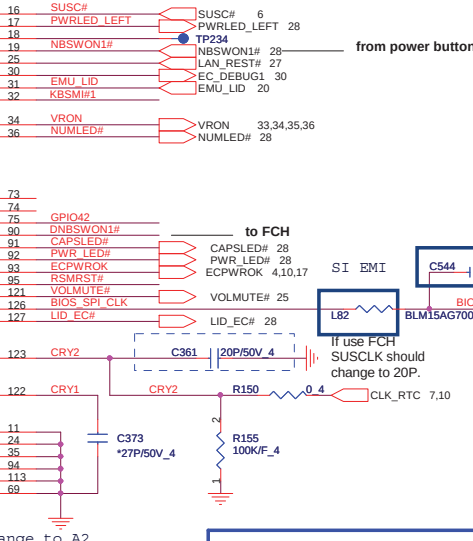
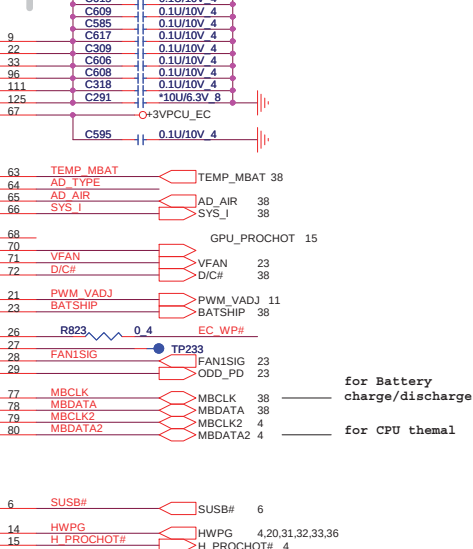
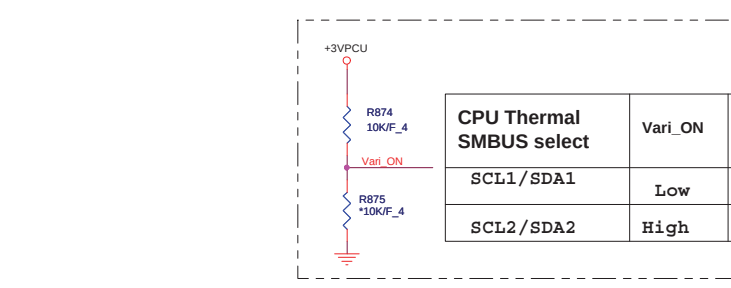
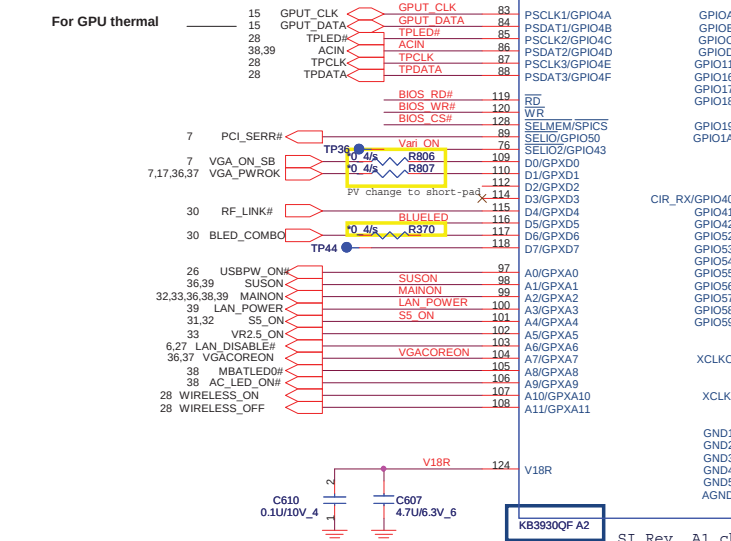
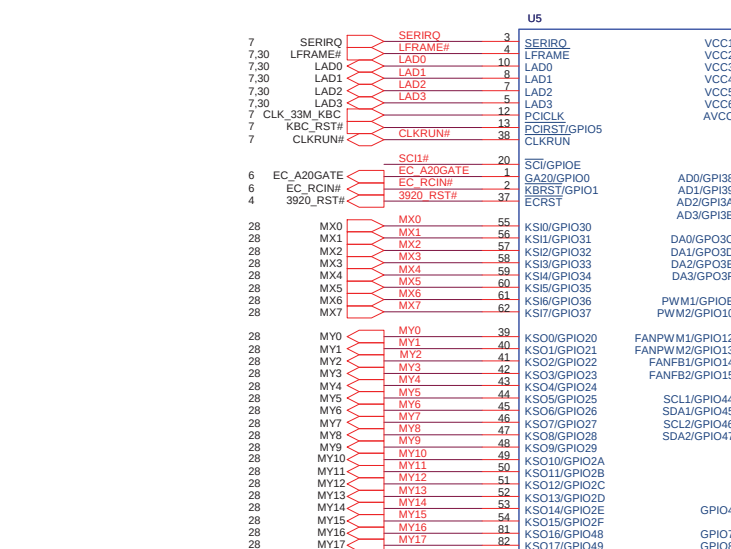
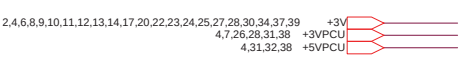
TOUCH PAD Con.



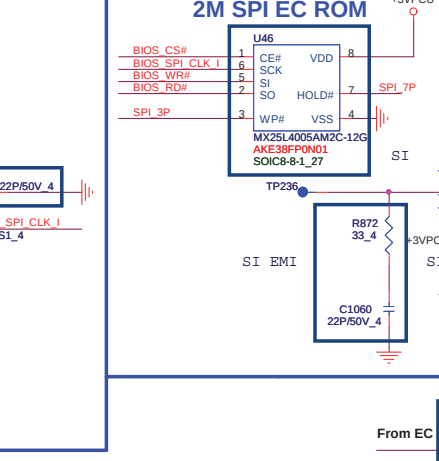
To TOUCH PAD SW board



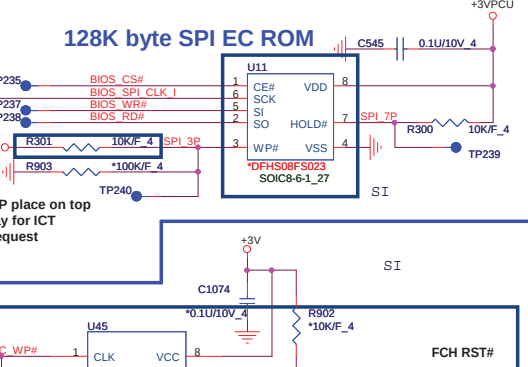
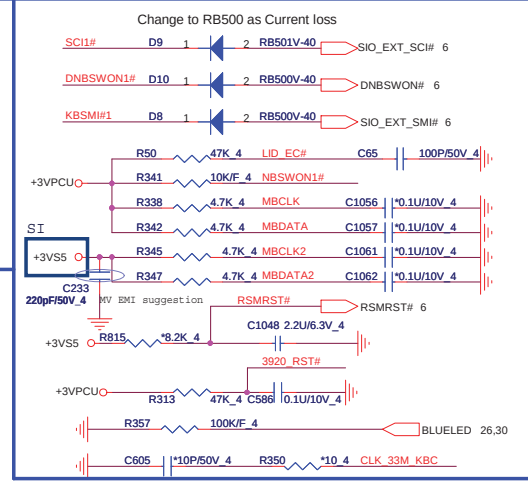
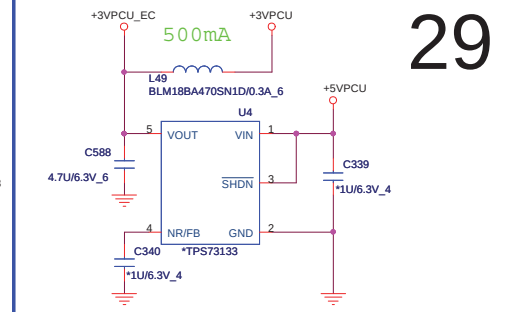
	PROJECT : R23 Quanta Computer Inc.		
	Size Custom	Document Number LED/KB/SW/TP	Rev 1A
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Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W

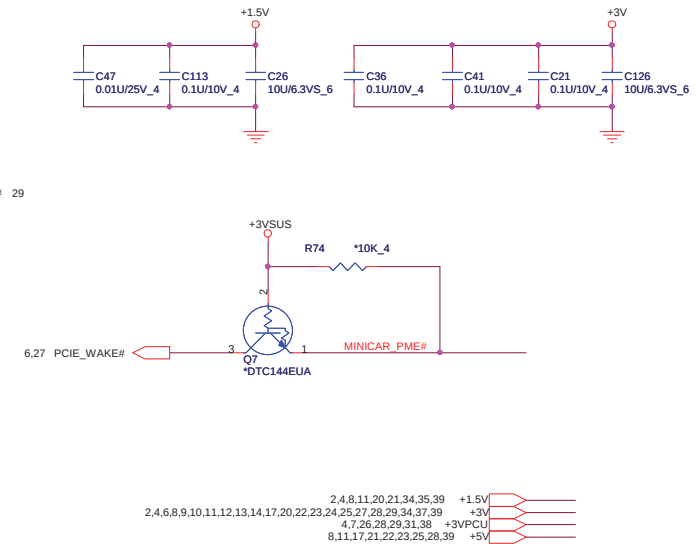


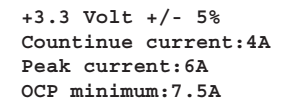
INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (3)	H (3)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q̄	Q̄

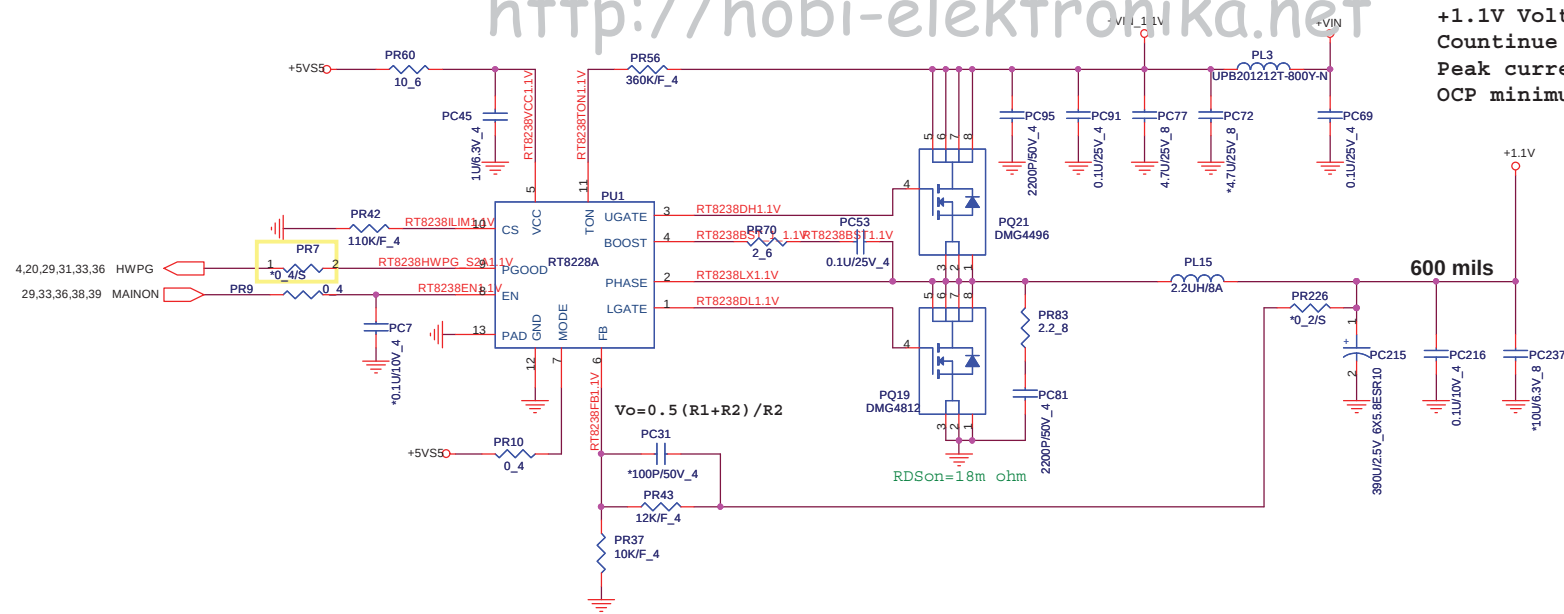


PROJECT : R23
Quanta Computer Inc.

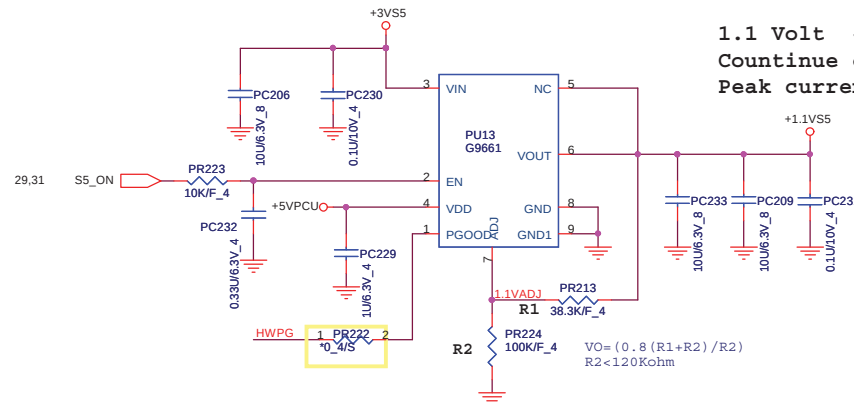
Size Custom	Document Number EC (K33926)/ROM	Rev 1A
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WLAN





+1.1V Volt +/- 5%
 Countinue current:3A
 Peak current: 4A
 OCP minimum:6A

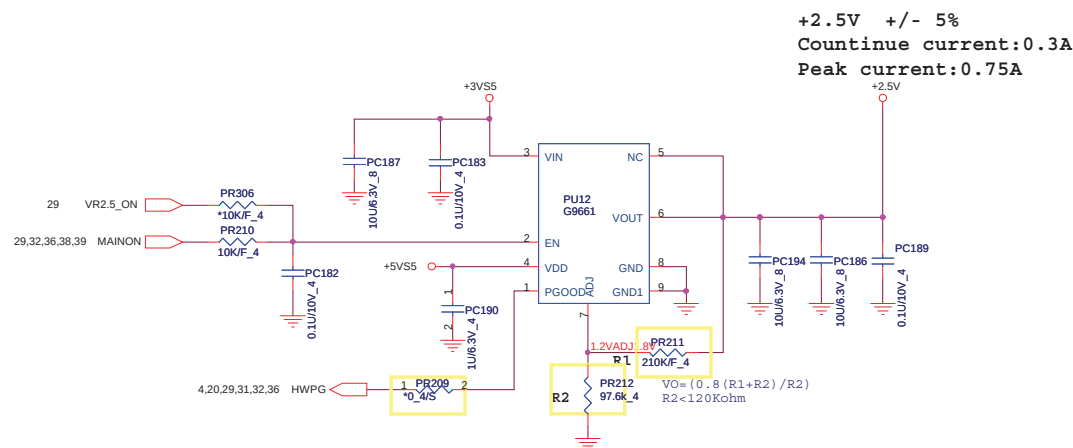
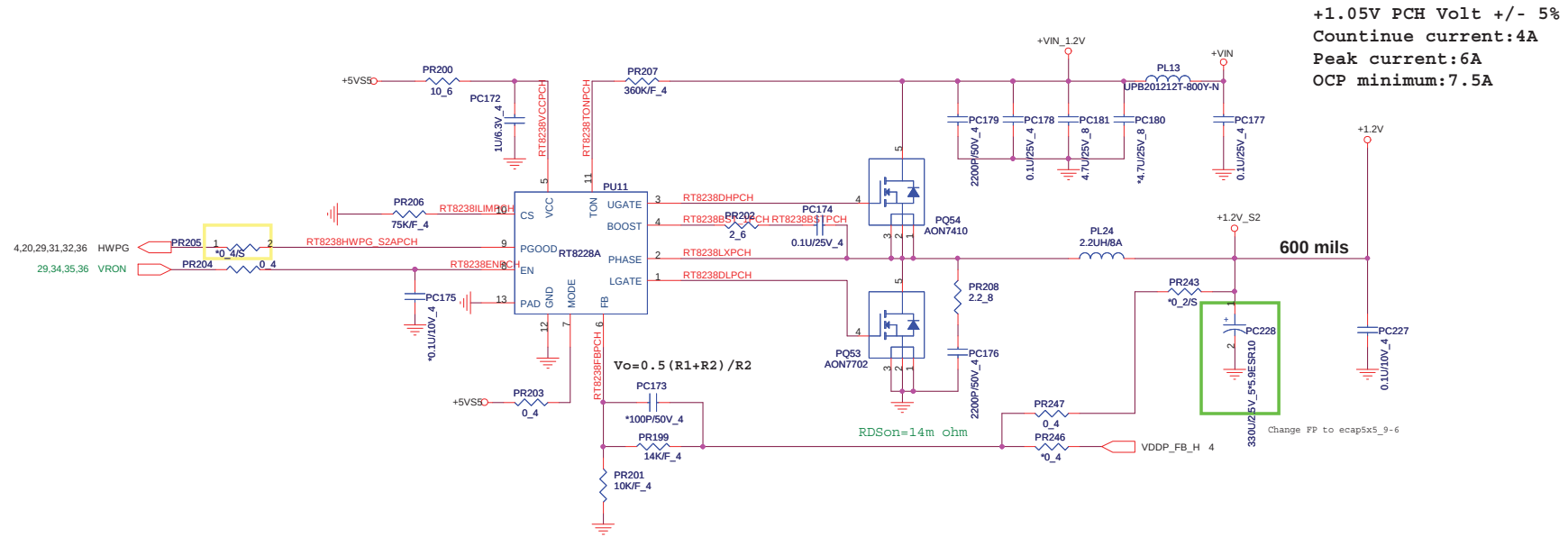


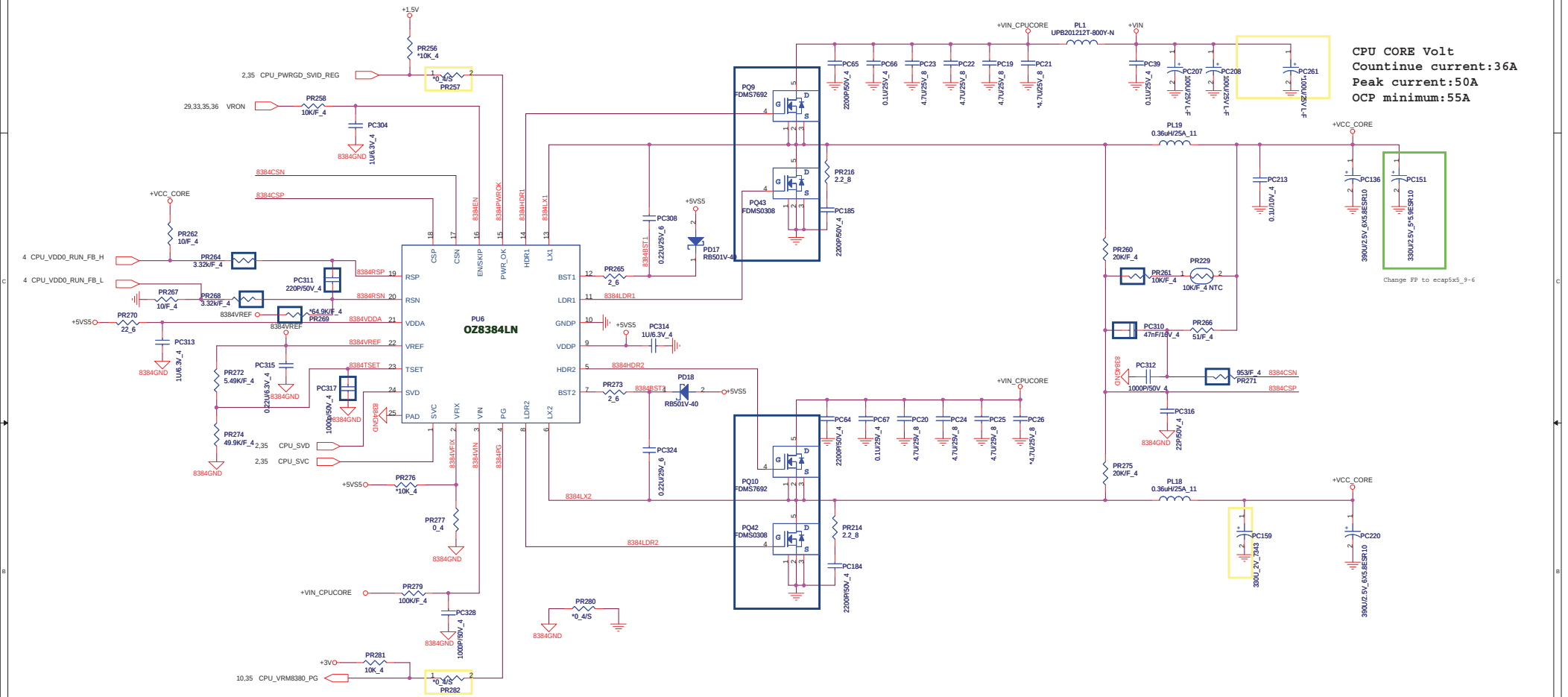
1.1 Volt +/- 5%
 Countinue current:0.2A
 Peak current:0.5A

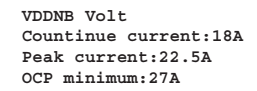


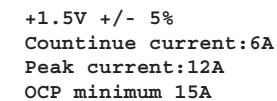
PROJECT : R23
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA Core/+1.8VGFY/1.0VGFY	1A
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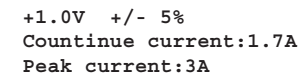
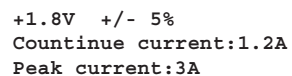




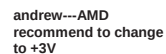




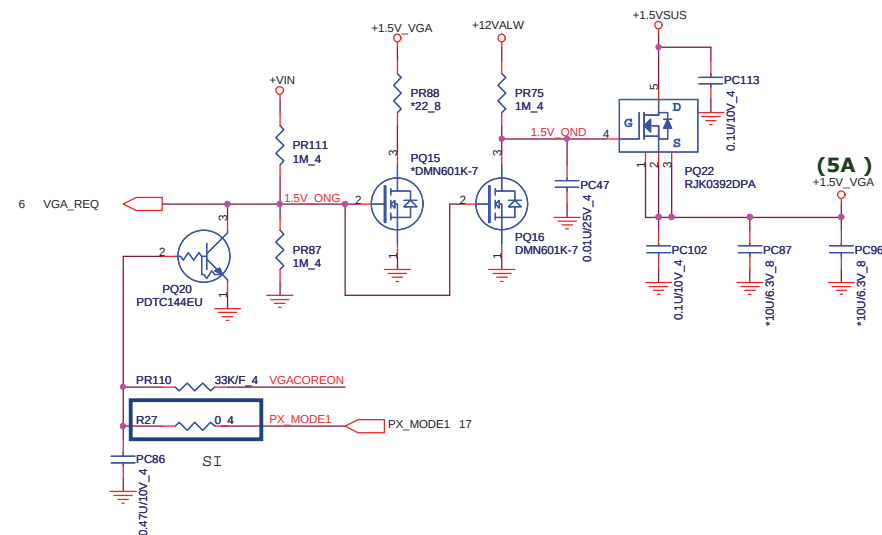
SG & Discrete Only



Size Custom	Document Number DDR3 (RT8207)	Rev 1A
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Seymour-XT	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA



PROJECT : R23
Quanta Computer Inc.

Size Custom	Document Number +VGACORE (RT8208/1.8V)	Rev 1a
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