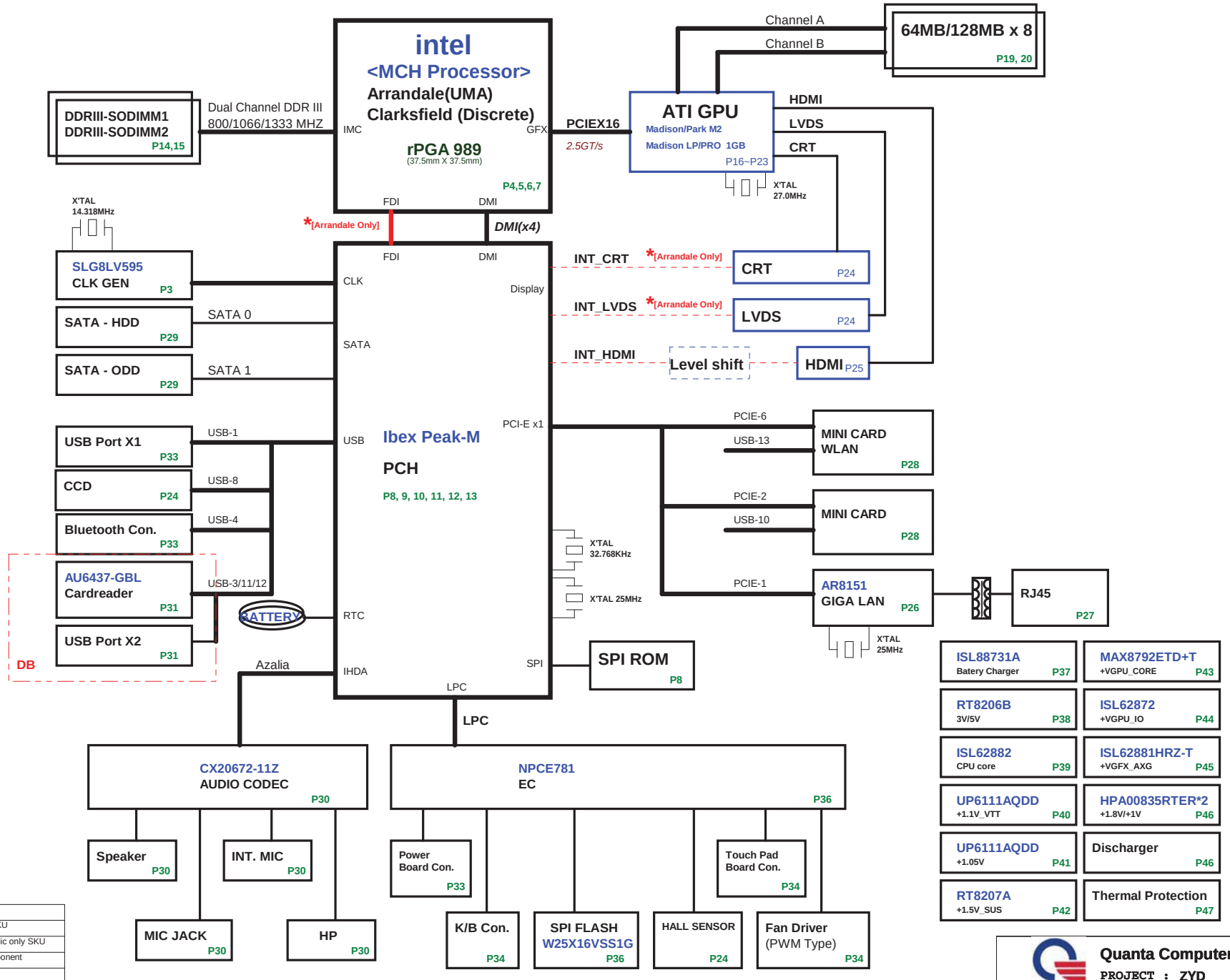
ZYD SYSTEM BLOCK DIAGRAM



BOM Option Table

Reference	Description
IV@	for UMA only SKU
EV@	for Discrete Graphic only SKU
SP@	special case component
*	do not stuff

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	Block Diagram	3B

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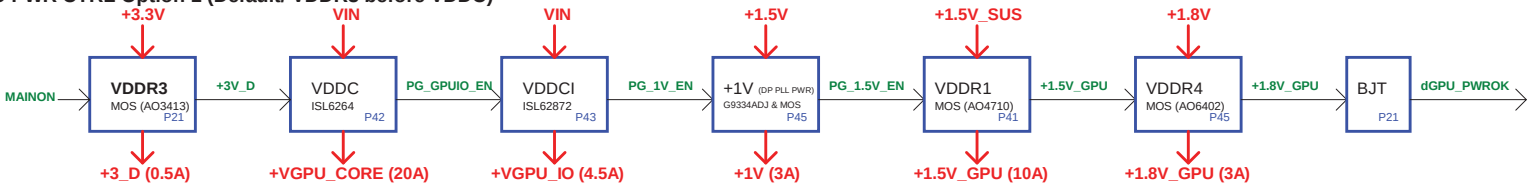
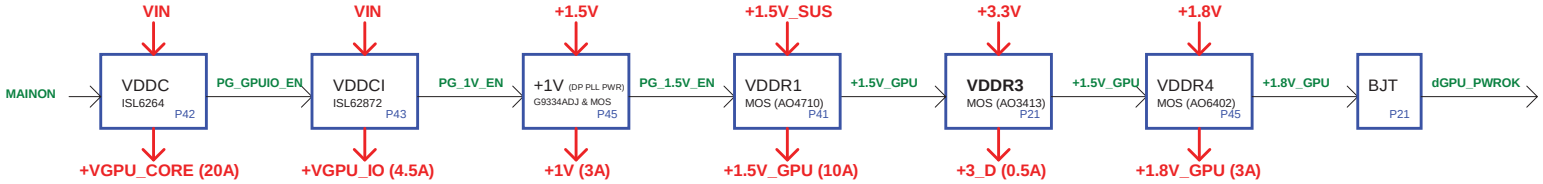
GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



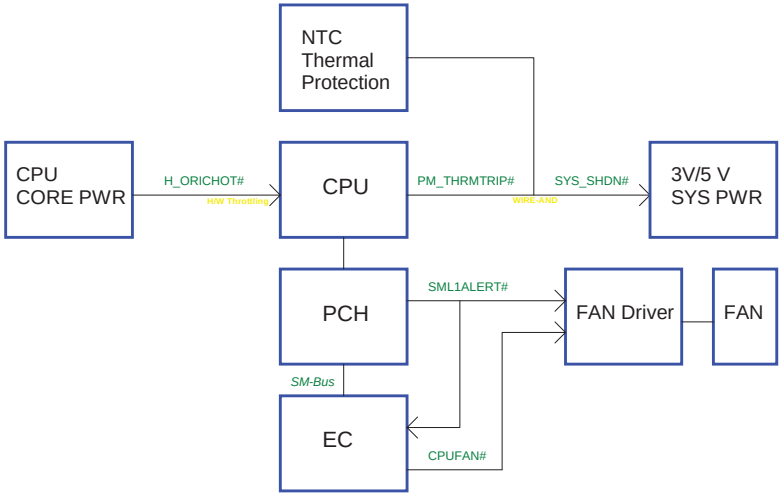
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/PCH	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT	MAINON	S0
+3V	+3.3V	CLK GEN/PCH/GPU/LVDS/Mini card/Codec/card reader	MAINON	S0
+1.5V_SUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+3V_D	+3.3V	I/O POWER for 3.3V pins	dGPU_VRON	Discrete enable
+VGPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+VGPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable

Thermal Follow Chart



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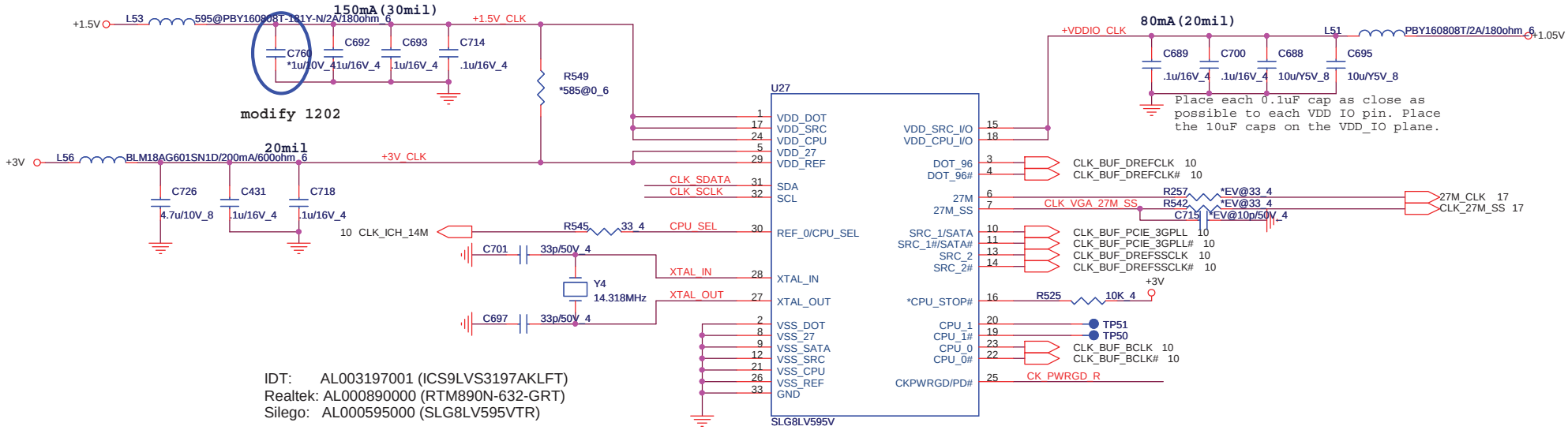
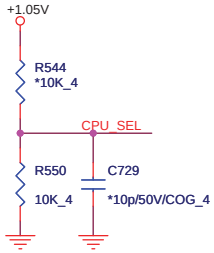


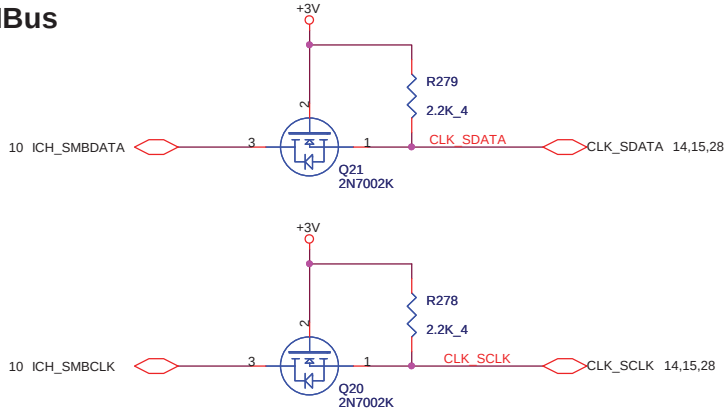
IDT: AL003197001 (ICS9LVS3197AKLFT)
Realtek: AL000890000 (RTM890N-632-GRT)
Silego: AL000595000 (SLG8LV595VR)

CPU_CLK select

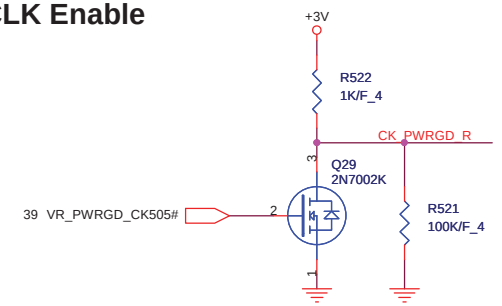


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable



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	Clock Generator	3B
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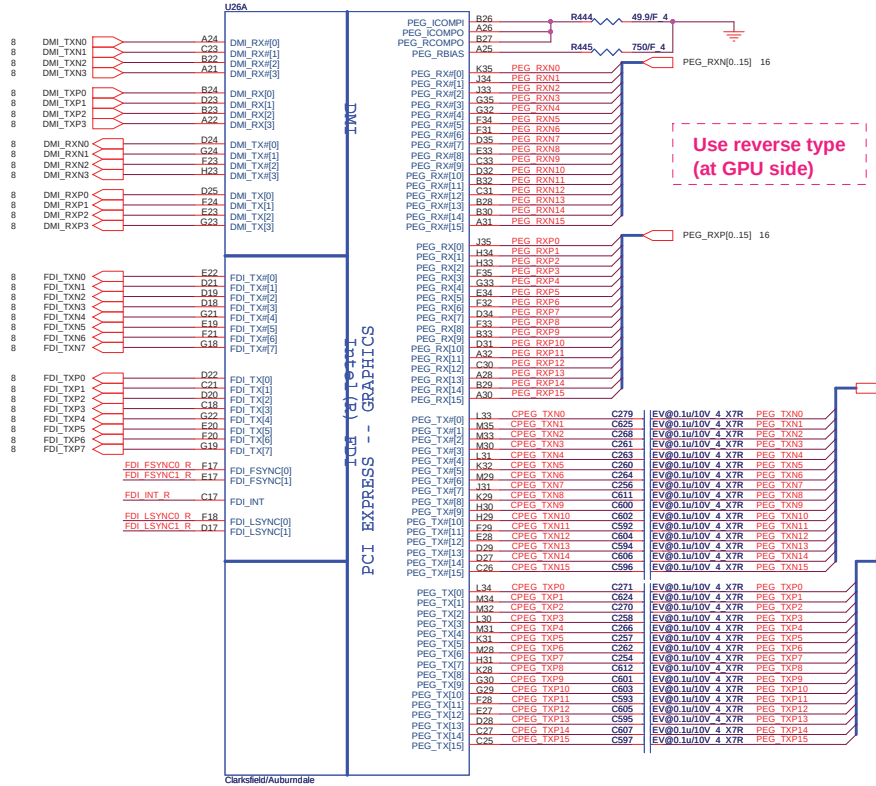
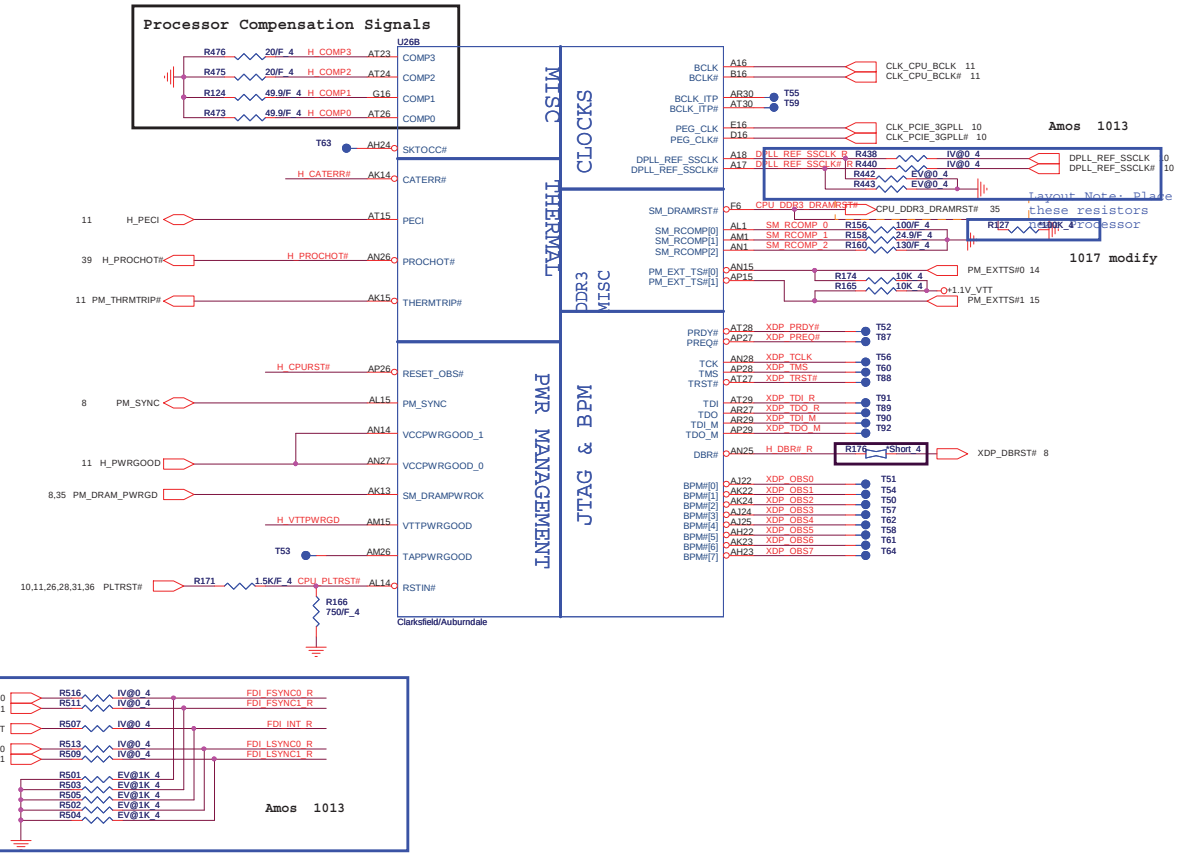
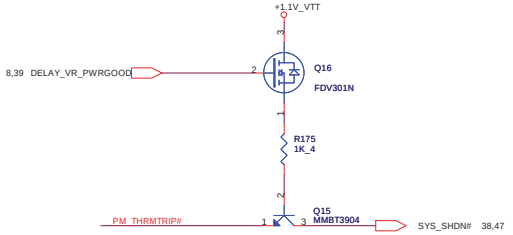
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



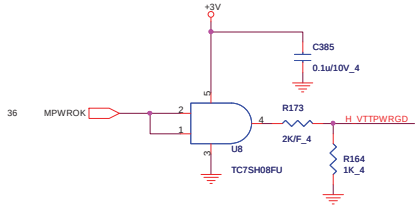
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



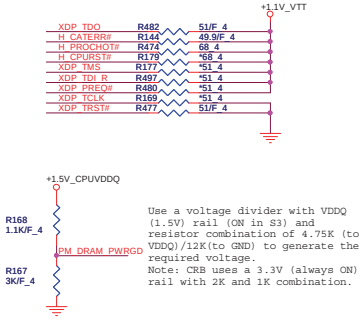
Thermaltrip protect



VTT PWR_Good



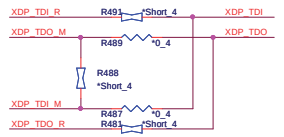
Processor pull-up



Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.

PM_DRAM_PWRGD:
Never drive hight before DDR3 voltage ramp to stable

JTAG MAPPING



Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

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	AUBURNDA 1/4	3B
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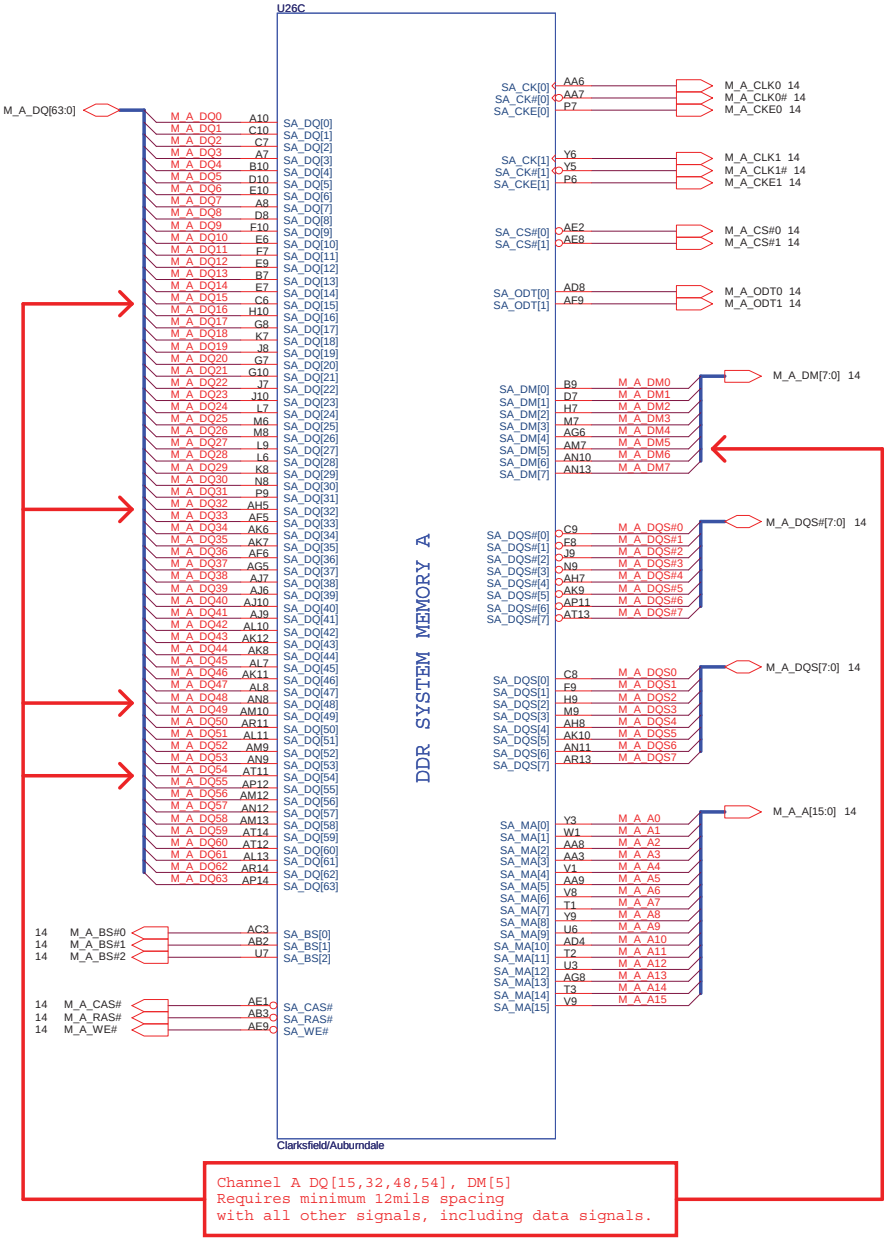
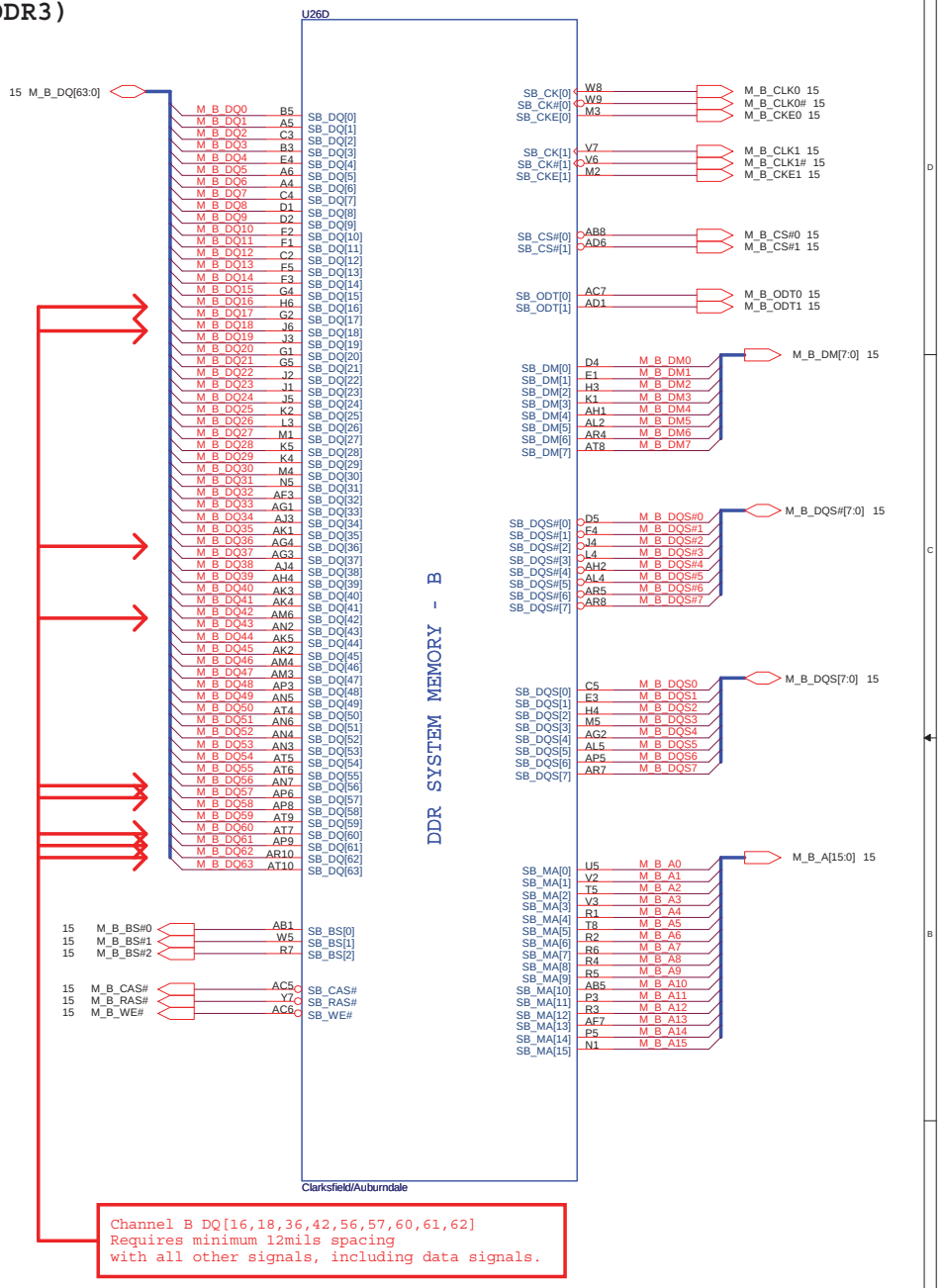
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)





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	AUBURNDA 2/4	3B
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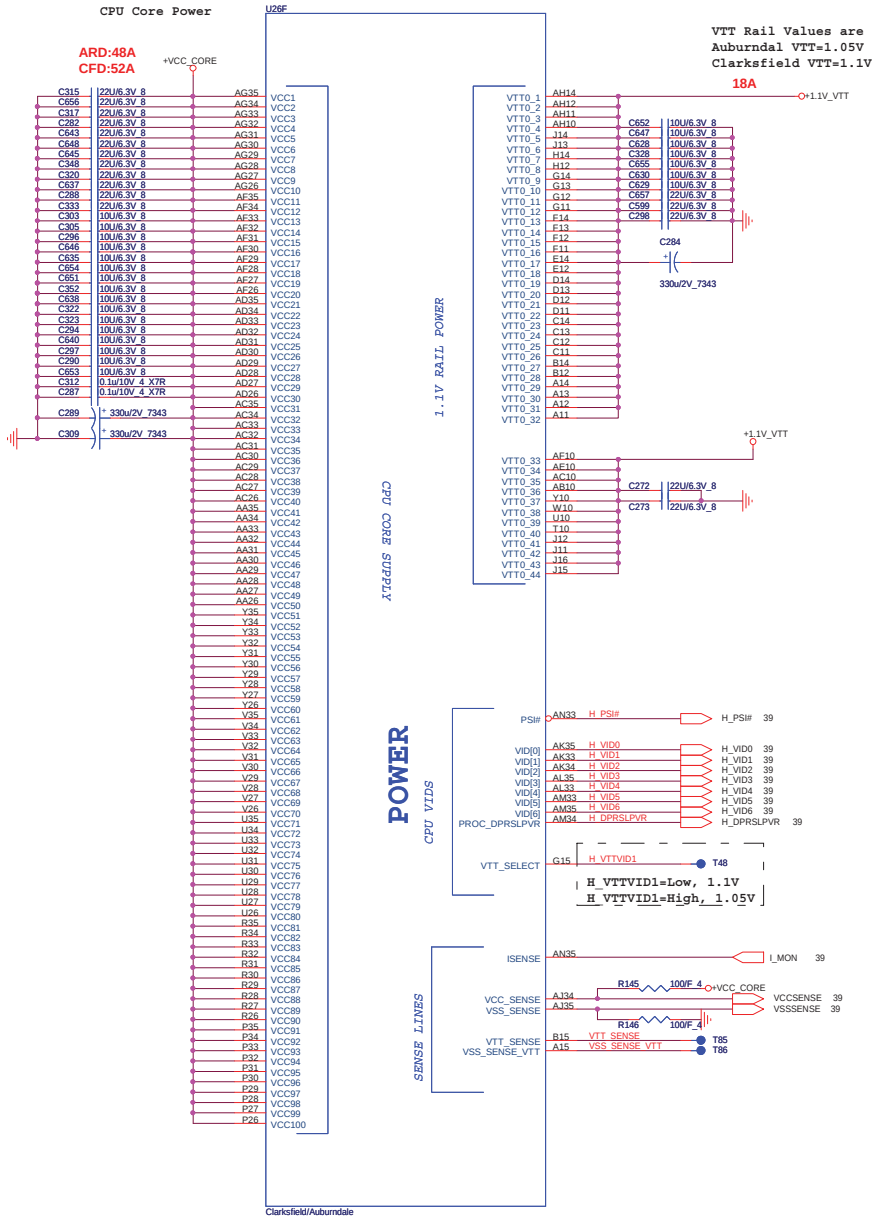
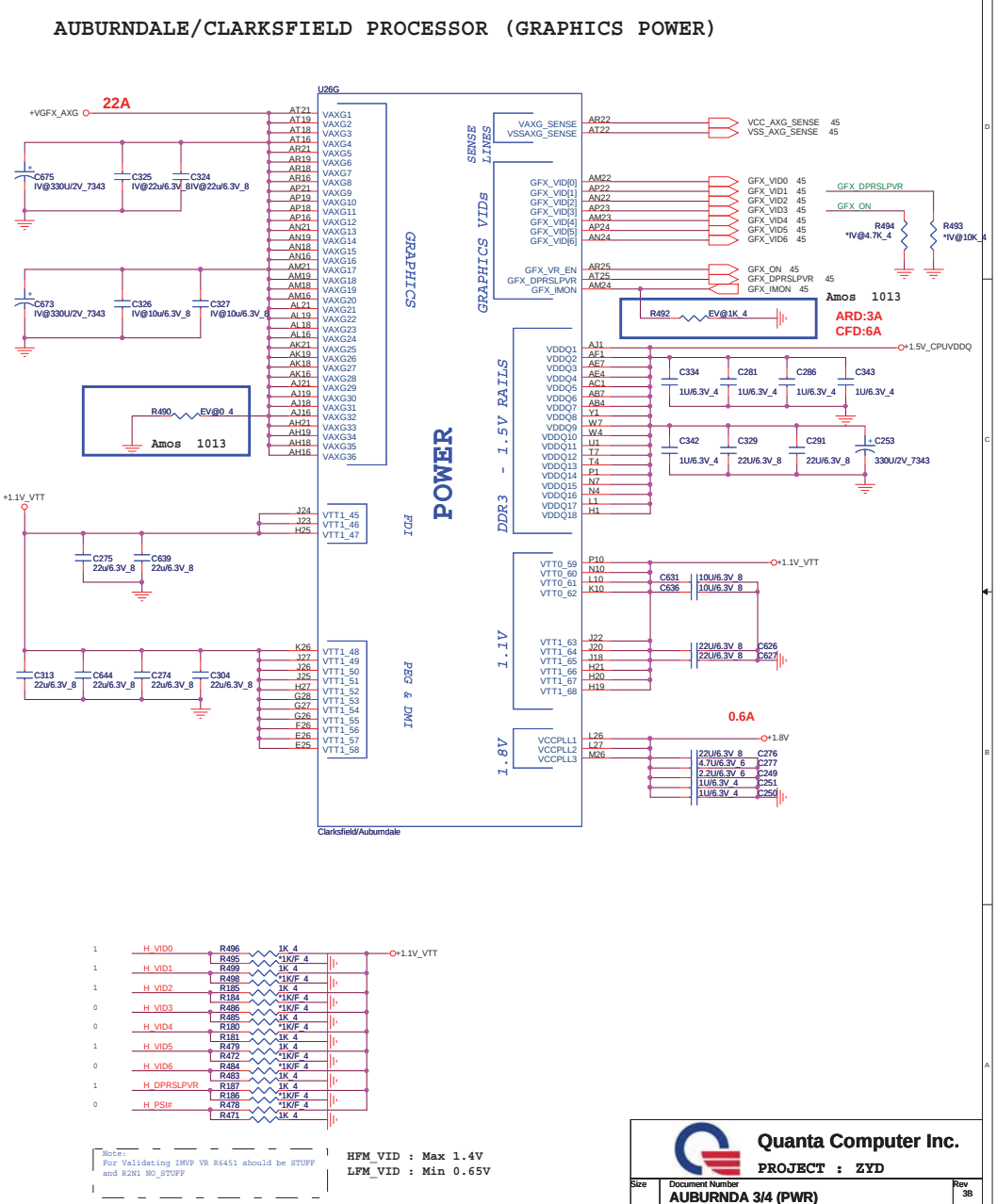


AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)



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	AUBURNDA 3/4 (PWR)	3B

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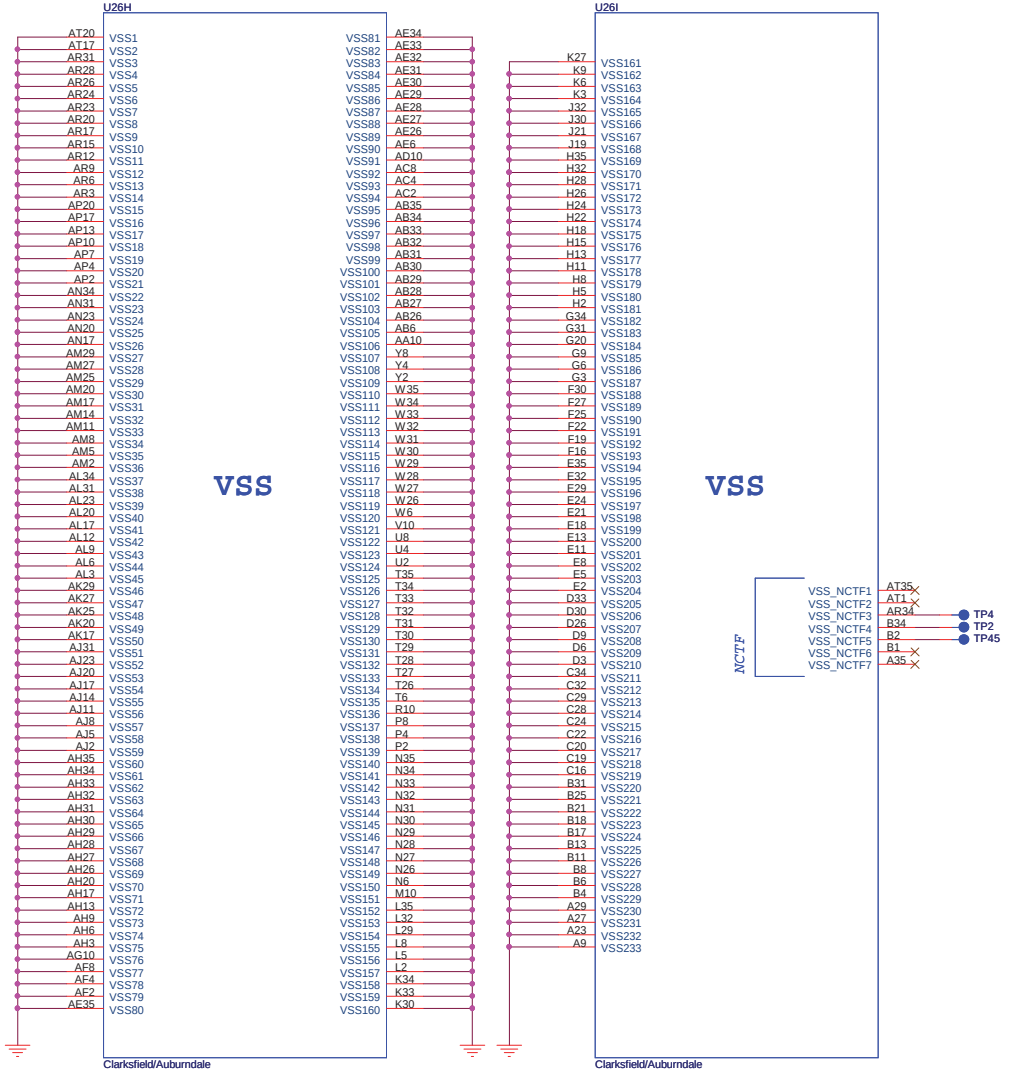
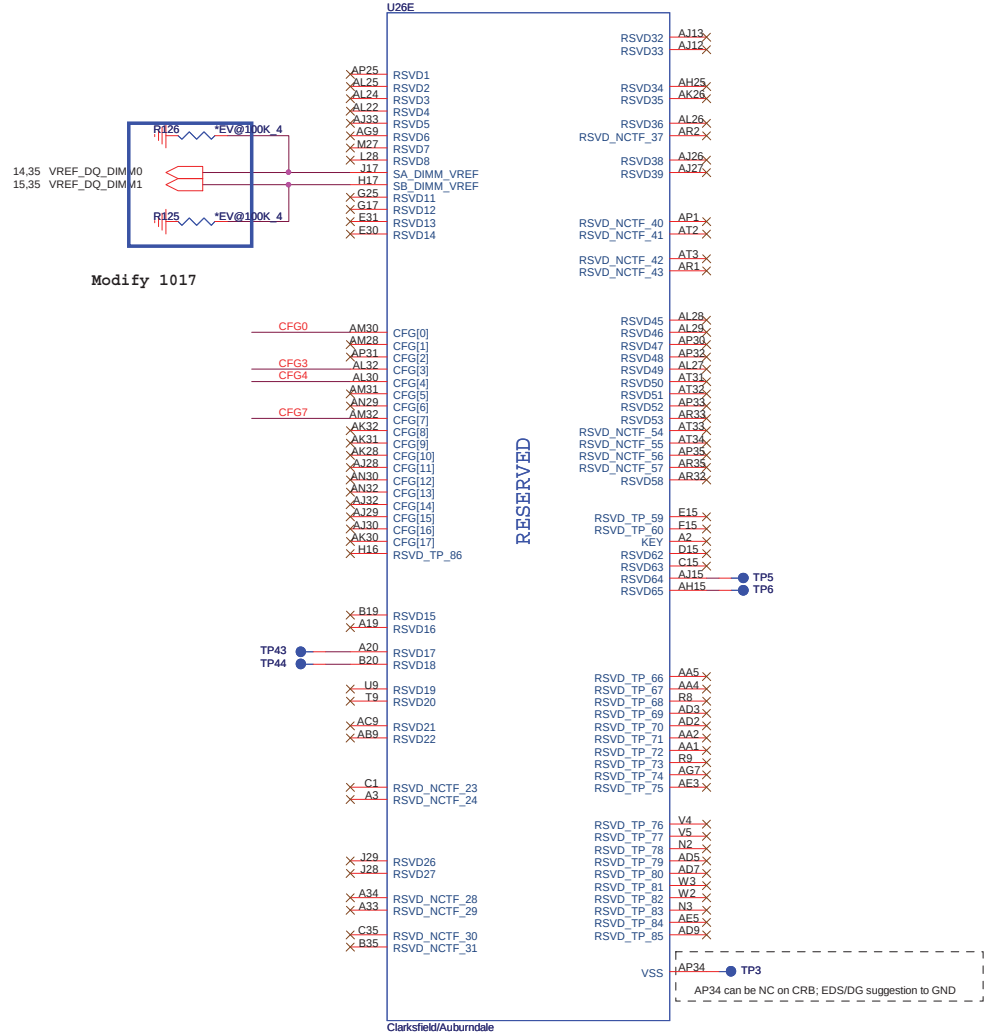
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R172 *3.01K_NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R159 *3.01K/F_4
CFG4 (Embended Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R157 *3.01K
This pin is for Auburndale only				CFG7 R161 *3.01K/F_4

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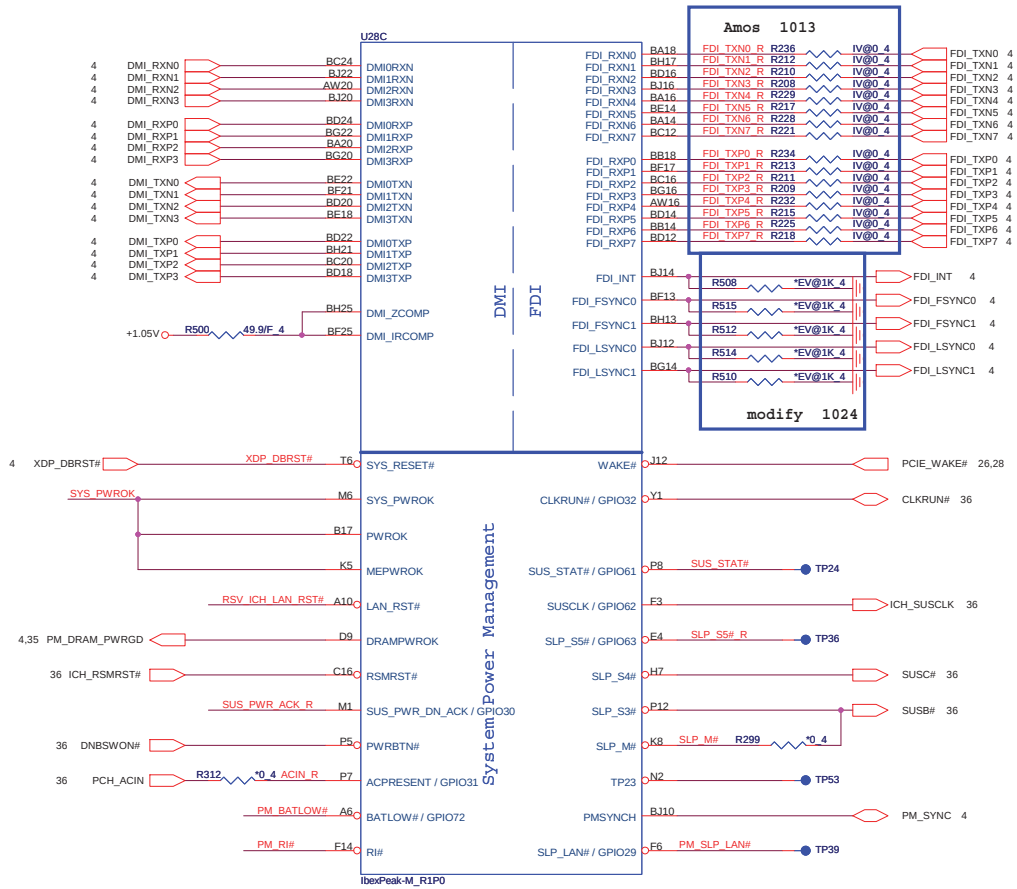
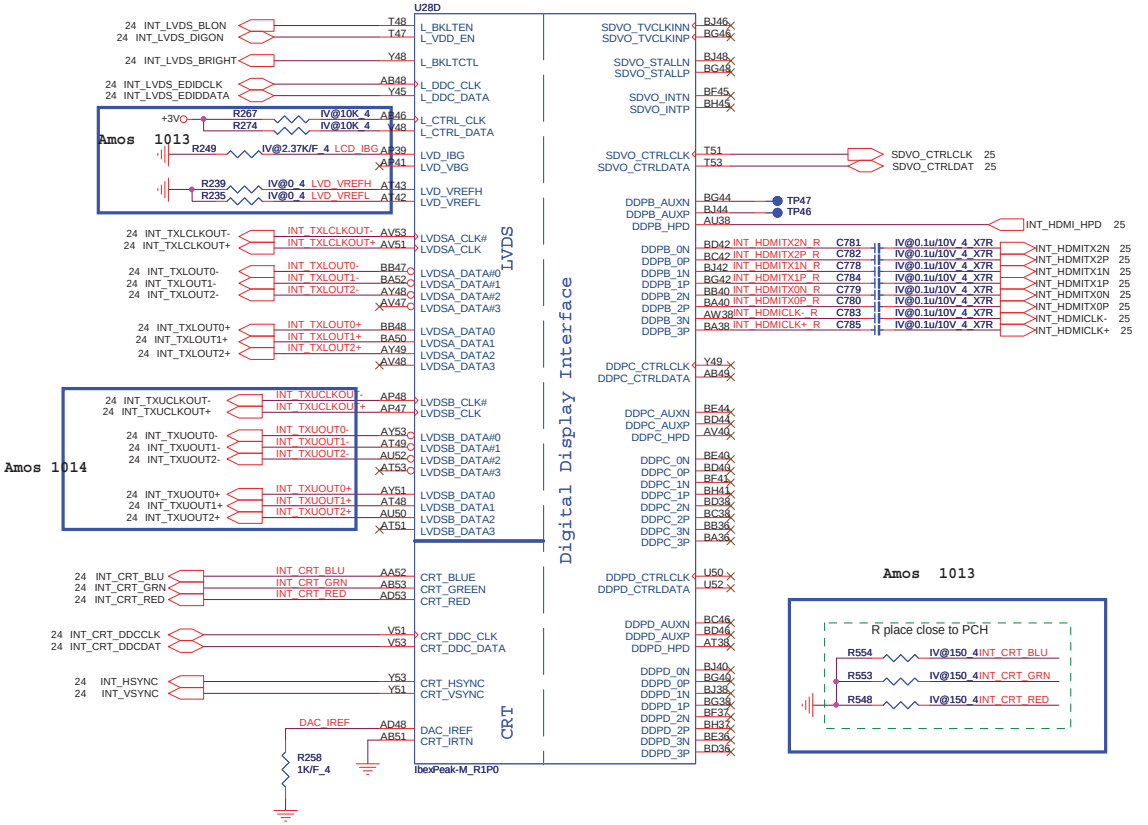
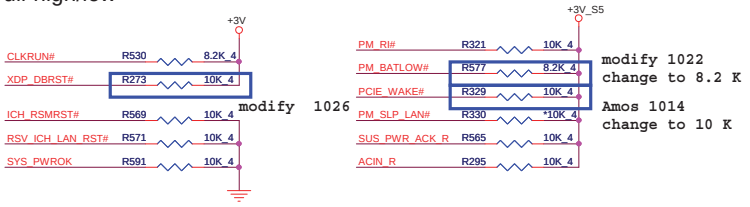
IBEX PEAK-M (DMI,FDI,GPIO)



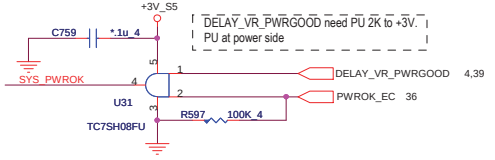
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



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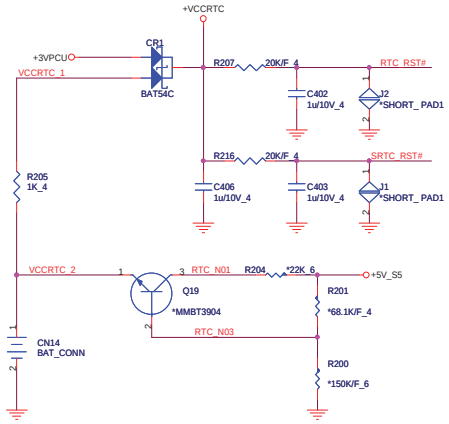
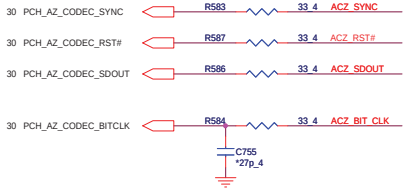
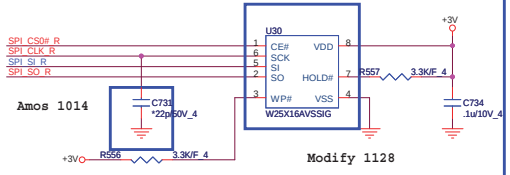
RTC Circuitry



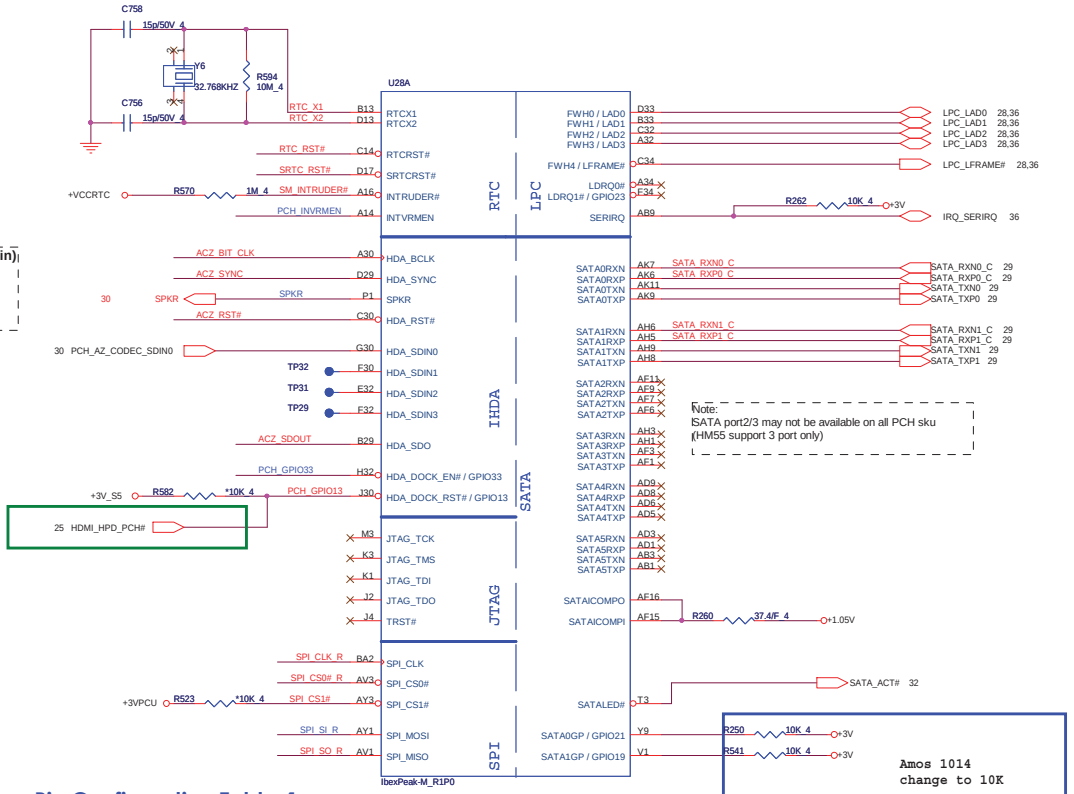
HDA Bus



MDC Bus



PCH SPI



HDA_SYNC (PCH strap pin)

Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V

PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R593 330K_6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R559 *1K_4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R307 *1K/F_4 SPKR
HDA_DOCK_EN #/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 J3 *SHORT_PAD1 R322 10K_4 +3V
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	10 PCI_GNT0# R315 1K_4 10 PCI_GNT1# R310 1K_4
GNT2#/ GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only Modify 1019	10 PCI_GNT2# R313 *1K/F_4
GNT3#/ GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	10 PCI_GNT3# R560 *10K/F_4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	10 NV_ALE R231 *1K/F_4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	10 NV_CLE R230 *1K/F_4 +1.8V

GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	11 RSV_GPIO8 R325 10K_4 +3V_S5 R320 *1K_4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	11 CR_WAKE# R282 1K_4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	11 PCH_GPIO27 R263 *10K_4

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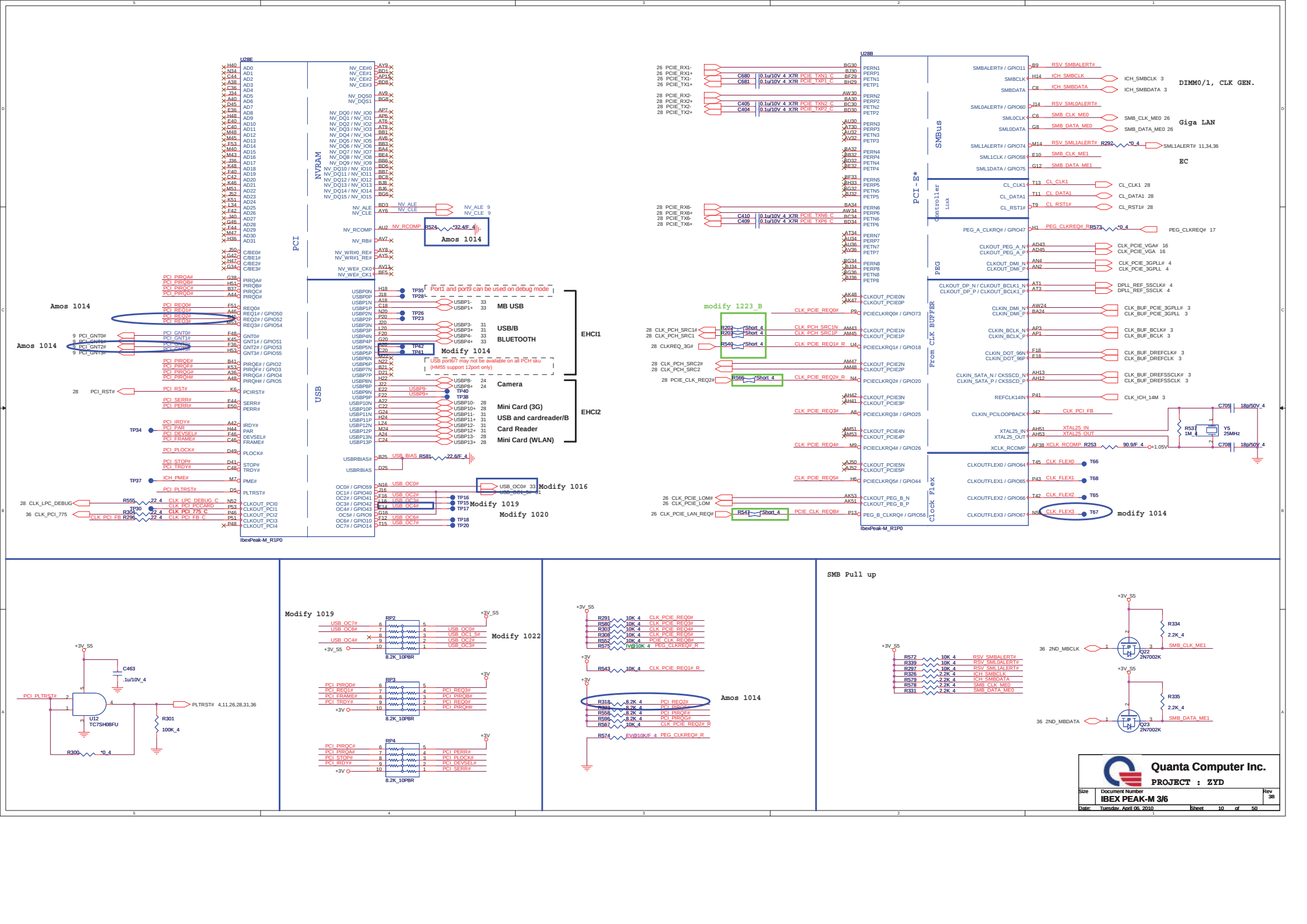
U28E
PCI
NVRAM
USB
IbexPeak-M_R1P0
Amos 1014
Port1 and port9 can be used on debug mode
USB port67 may not be available on all PCH sku
(HM55 support 12port only)
MB USB
USB/B
BLUETOOTH
Modify 1014
Camera
Mini Card (3G)
USB and cardreader/B
Card Reader
Mini Card (WLAN)
EHCI1
EHCI2
Modify 1016
Modify 1019
Modify 1020
U28B
PCI-E*
SMBus
Controller
Link
PEG
Prom CLK BUFFER
Clock Flex
modify 1223_B
DIMM0/1, CLK GEN.
Giga LAN
EC
modify 1014
Modify 1019
Modify 1022
SMB Pull up
Amos 1014
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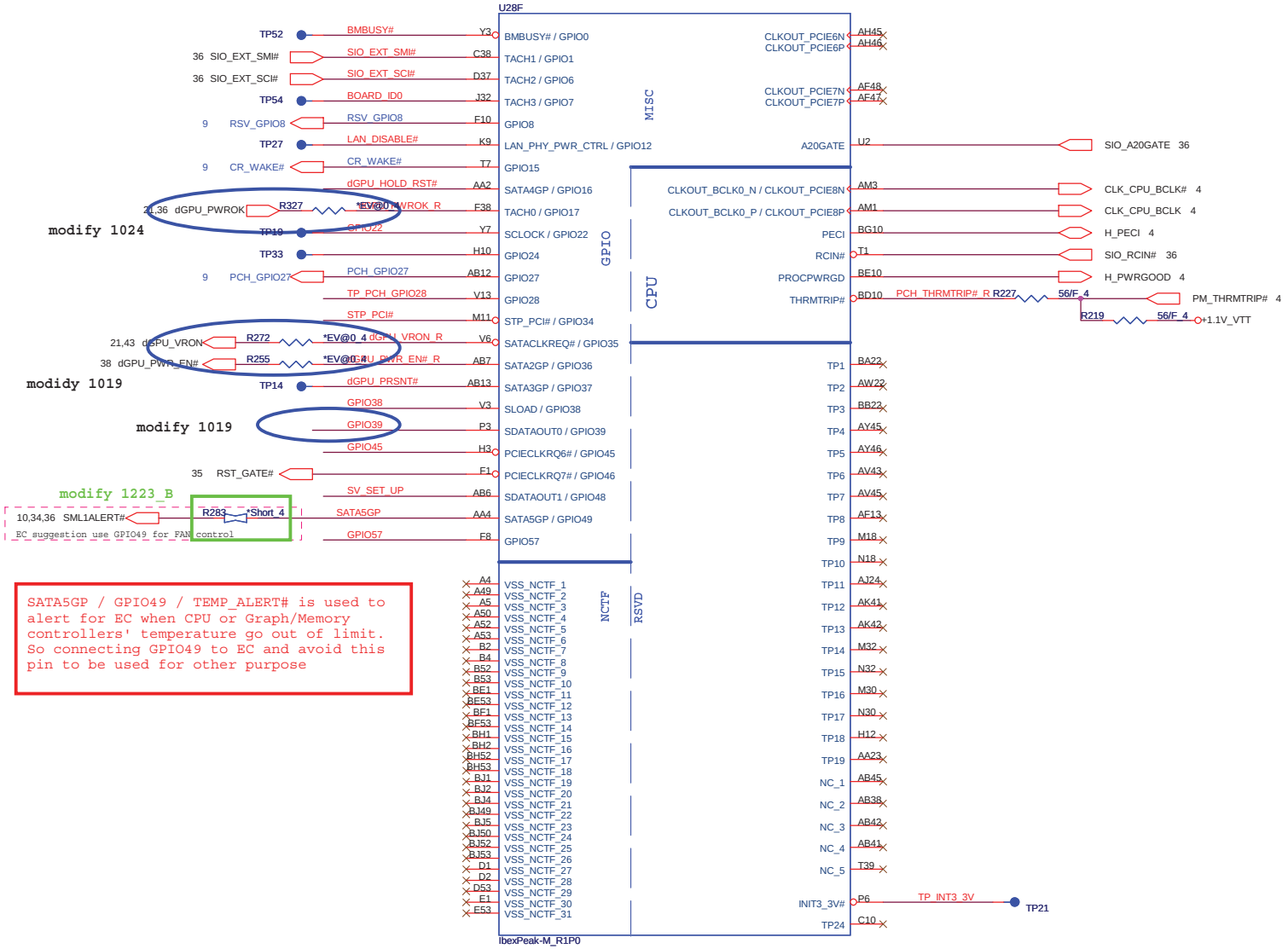
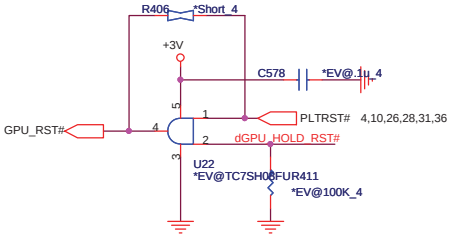
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



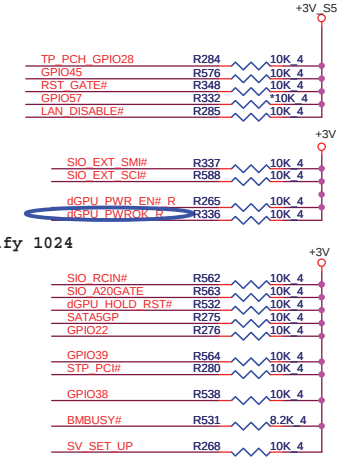
SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

16

GPU RST#

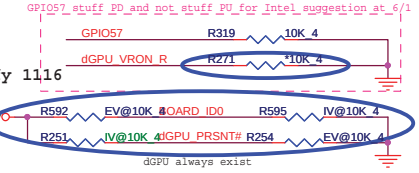


GPIO Pull-up/Pull-down



modify 1024

SV_SET_UP	1-X High = Strong (Default)



modify 1116

Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = IV
RSV_GPIO8	High = Disable Low = Enable

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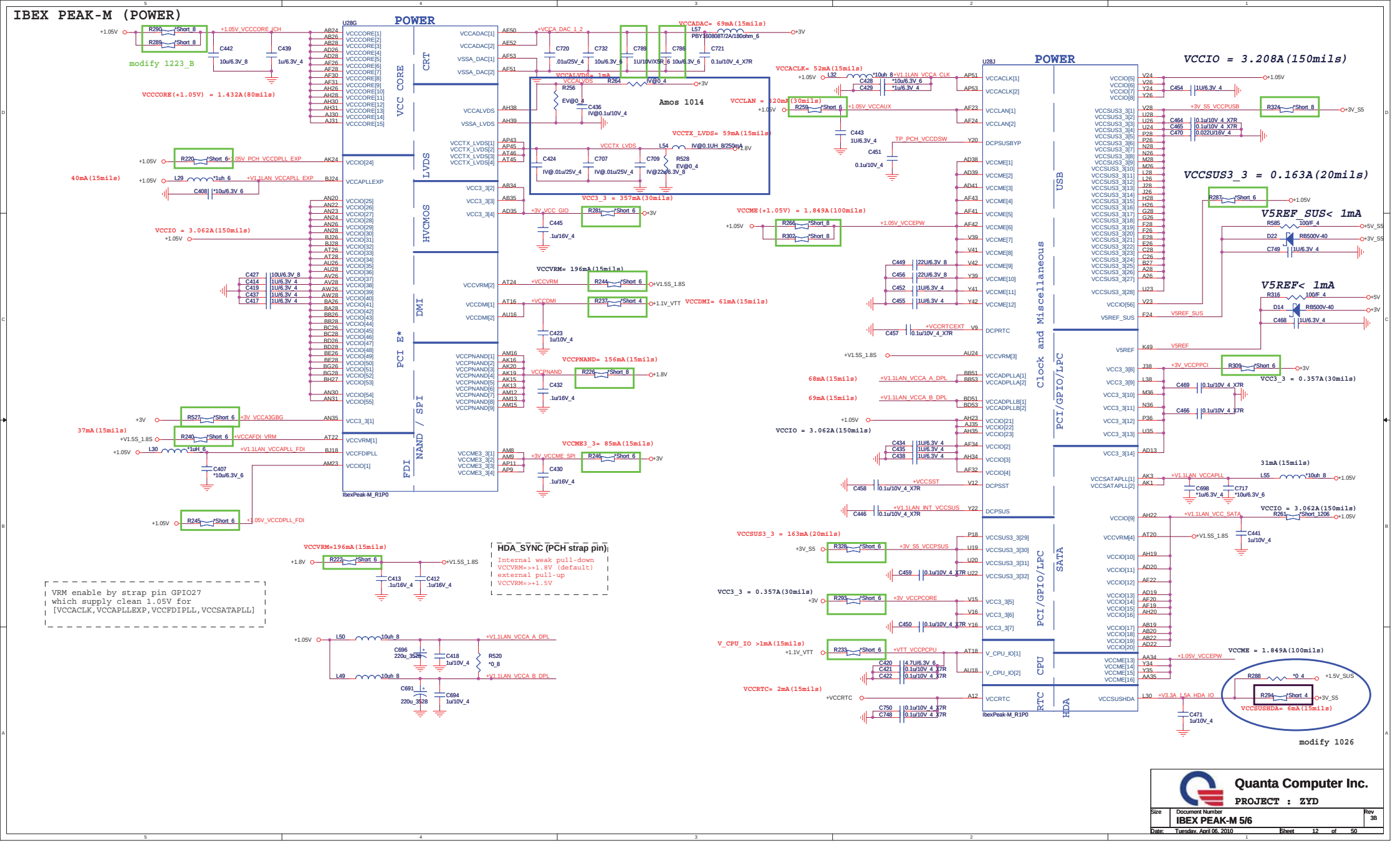
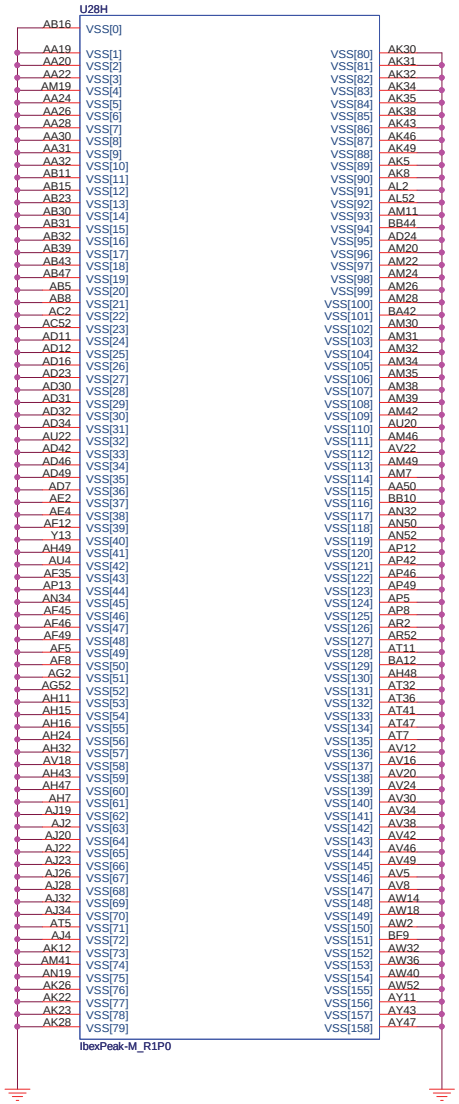
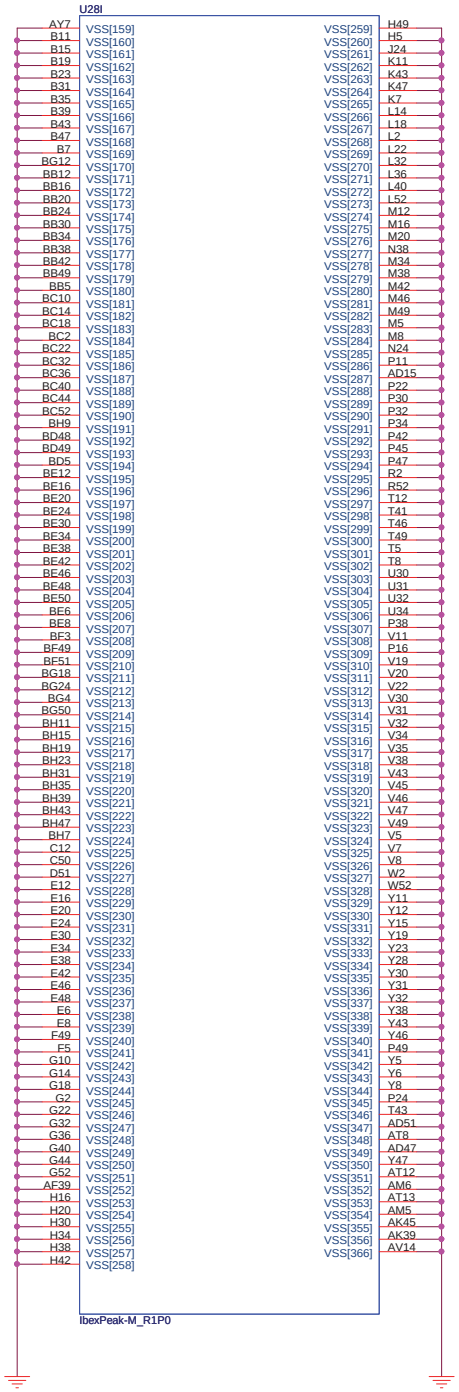
IBEX PEAK-M (POWER)



IBEX PEAK-M (GND)





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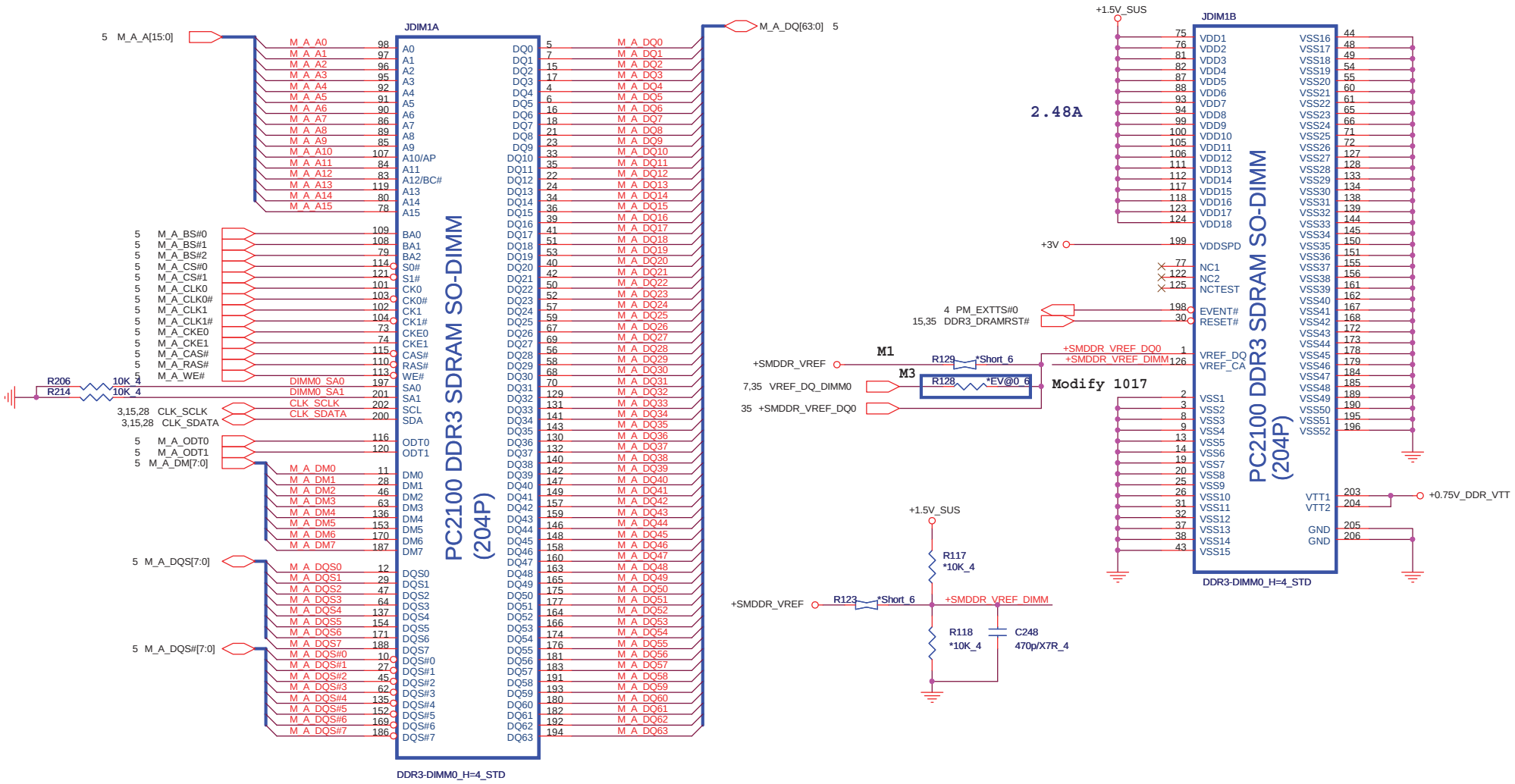
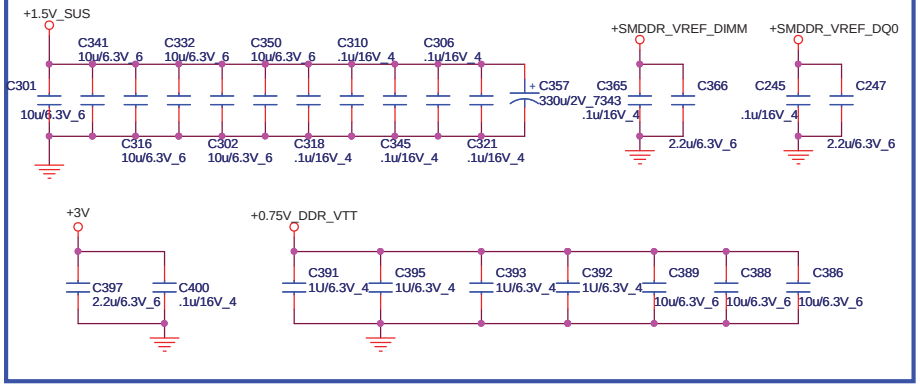


Place these Caps near So-Dimm0.



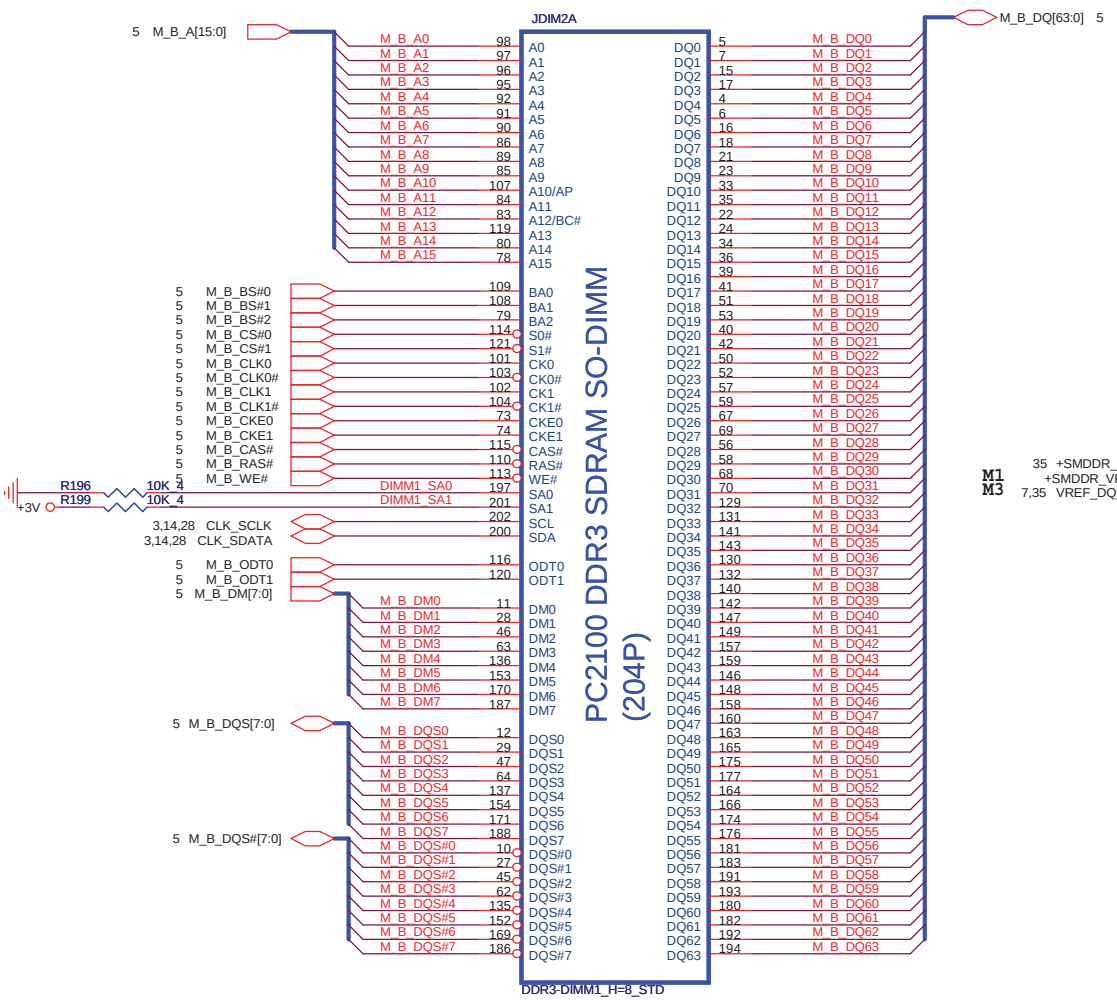
For Arrandale only designs--->Only method M1 should be enabled.
For Clarksfield only designs--->Both M1 AND M3 methods should be enabled simultaneously
For Common Motherboard designs--->Both M1 AND M3 methods should be enabled simultaneously.

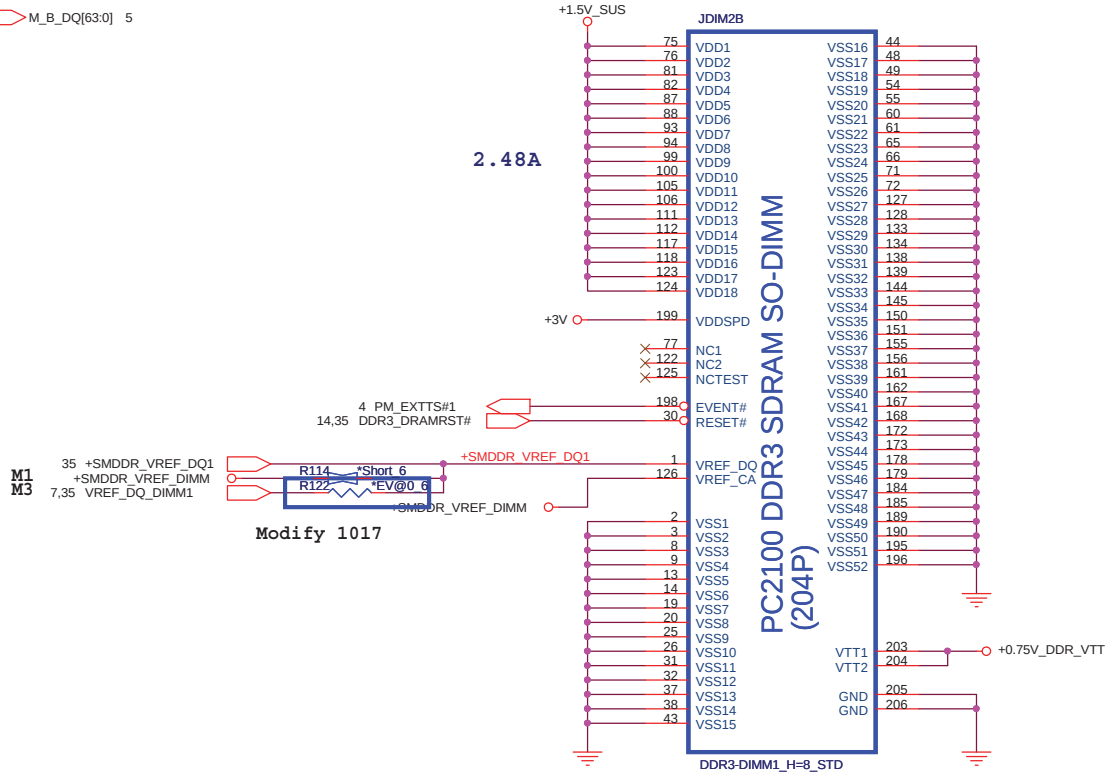
M1:PWR SMDRR_VREF
M1+:voltage divider(Default)
M3:CPU VREF_DQ_DIMM0

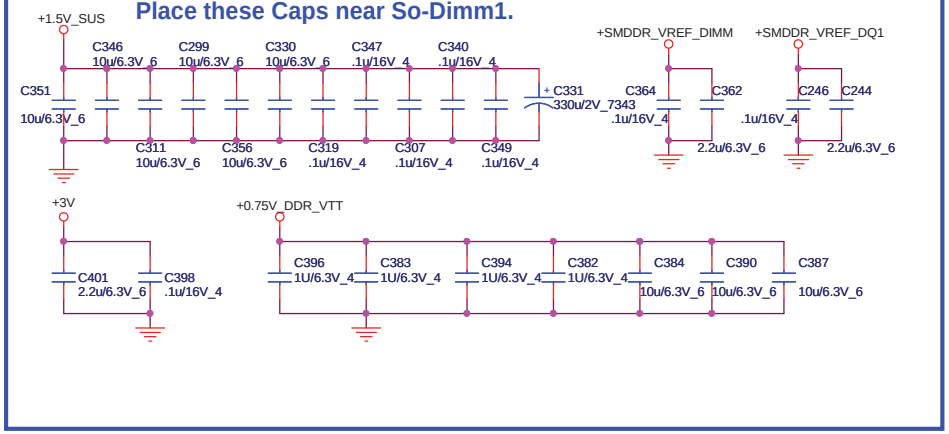
Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	DDRIII SO-DIMM-0	3B
Date: Tuesday, April 06, 2010	Sheet 14 of 50	

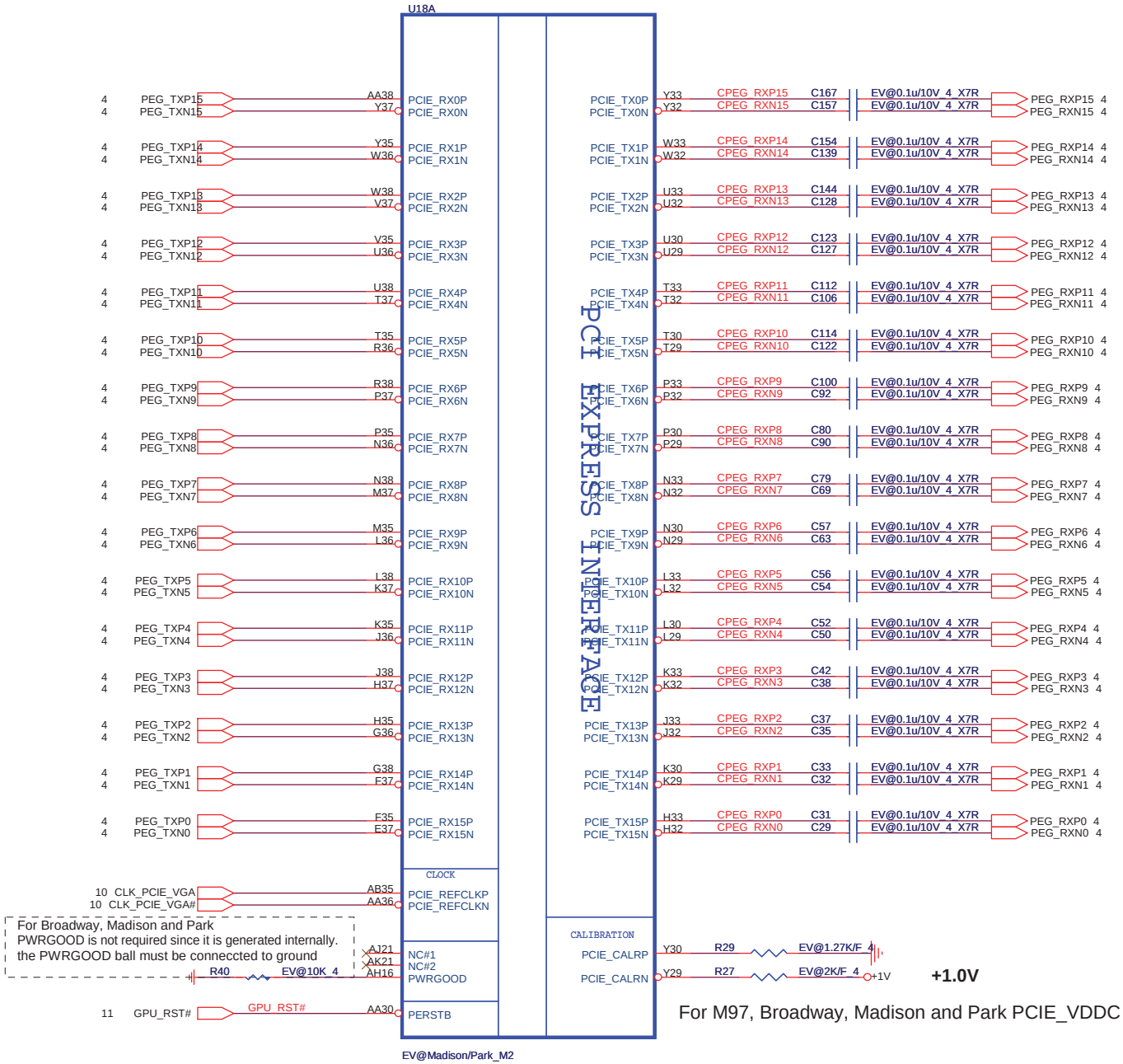






For Arrandale only designs--->Only method M1 should be enabled.
For Clarksfield only designs--->Both M1 AND M3 methods should be enabled simultaneously
For Common Motherboard designs--->Both M1 AND M3 methods should be enabled simultaneously.

Quanta Computer Inc.		
PROJECT : ZYD		
Size	Document Number: DDRIII SO-DIMM-1	Rev: 3B
Date: Tuesday, April 06, 2010	Sheet 15 of 50	



For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	Madison/Park M2 PCIE I/F	3B
Date: Tuesday, April 06, 2010	Sheet 16 of 50	

GPU Power-on sequence

1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU_PWROK

U18B

MUTI GFX

NC on Park

1.8V GPIO

NC on Park

DVPCNTL_MVP_0
DVPCNTL_MVP_1
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCLK
DVPDATA_0 … DVPDATA_23

23 RAM_STRAP0
23 RAM_STRAP1
23 RAM_STRAP2
T42

+3V_D
R50
R58 EV@10K/F_4
EV@10K/F_4

I2C
SCL
SDA

DPA
DPB
DPC
DPD

TXCAP_DPA3P / TXCAM_DPA3N
TX0P_DPA2P / TX0M_DPA2N
TX1P_DPA1P / TX1M_DPA1N
TX2P_DPA0P / TX2M_DPA0N
TXCBP_DPB3P / TXCBM_DPB3N
TX3P_DPB2P / TX3M_DPB2N
TX4P_DPB1P / TX4M_DPB1N
TX5P_DPB0P / TX5M_DPB0N
TXCCP_DPC3P / TXCCM_DPC3N
TX0P_DPC2P / TX0M_DPC2N
TX1P_DPC1P / TX1M_DPC1N
TX2P_DPC0P / TX2M_DPC0N
TXCDP_DPD3P / TXCDM_DPD3N
TX3P_DPD2P / TX3M_DPD2N
TX4P_DPD1P / TX4M_DPD1N
TX5P_DPD0P / TX5M_DPD0N

HDMICLK+ 25
HDMICLK- 25
HDMITX0P 25
HDMITX0N 25
HDMITX1P 25
HDMITX1N 25
HDMITX2P 25
HDMITX2N 25

DP Channel D is NC on PARK

U18G

LVDS CONTROL
VARY_BL
DIGON
EV_LVDS_BRIGHT 24
EV_LVDS_VDDEN 24
R53 *EV@10K_4
R57 *EV@10K_4

TXCLK_UP_DPF3P / TXCLK_UN_DPF3N → EV_TXUCLKOUT+ 24 / EV_TXUCLKOUT- 24
TXOUT_U0P_DPF2P / TXOUT_U0N_DPF2N → EV_TXUOUT0+ 24 / EV_TXUOUT0- 24
TXOUT_U1P_DPF1P / TXOUT_U1N_DPF1N → EV_TXUOUT1+ 24 / EV_TXUOUT1- 24
TXOUT_U2P_DPF0P / TXOUT_U2N_DPF0N → EV_TXUOUT2+ 24 / EV_TXUOUT2- 24
TXOUT_U3P / TXOUT_U3N

Amos 1014

LVTMDP

TXCLK_LP_DPE3P / TXCLK_LN_DPE3N → EV_TXLCLKOUT+ 24 / EV_TXLCLKOUT- 24
TXOUT_L0P_DPE2P / TXOUT_L0N_DPE2N → EV_TXLOUT0+ 24 / EV_TXLOUT0- 24
TXOUT_L1P_DPE1P / TXOUT_L1N_DPE1N → EV_TXLOUT1+ 24 / EV_TXLOUT1- 24
TXOUT_L2P_DPE0P / TXOUT_L2N_DPE0N → EV_TXLOUT2+ 24 / EV_TXLOUT2- 24
TXOUT_L3P / TXOUT_L3N

EV@Madison/Park_M2

GENERAL PURPOSE I/O

GPU_GPIO0 … GPU_GPIO13
GPIO3_SMBDAT
GPIO4_SMBCLK
IO_VID0
EV_LVDS_BLON
SOUT_GPIO8
SIN_GPIO9
SCLK_GPIO10
VCORE1.2ID0
ALT#_GPIO17
VCORE1.2ID1
SCS#_GPIO22
GPIO_0 … GPIO_20_PWRCNTL_1
GPIO_21_BB_EN
GPIO_22_ROMCSB
GPIO_23_CLKREQB
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
GENERICA … GENERICH
GENERICE_HPD4

3.3V GPIO

+3V_D
R59 EV@10K_4
R66 *EV@10K/F_4
R108 *EV@10K/F_4
R107 *EV@10K/F_4
10 PEG_CLKREQ#
27M_CLK
R101 *EV@10K/F_4
R408 *EV@10K/F_4
R102 *EV@10K/F_4
R407 *EV@10K/F_4
GPIO24_TRSTB
27M_CLK
T13 T32 T36 T16 T33 T46

modify 1022_Reserved workaround for A11 Revision

GenericF/G is NC on PARK

Amos 1013

HPD1
HDMI_HP_EV 25

VREFG
+1.8V_GPU
R86 EV@499/F_4
R87 EV@249/F_4
C222 EV@0.1u/10V_4_X7R

PLL/CLOCK

DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
XTALIN
XTALOUT
CLK_27M_SS
R422 *EV@0_4
C584 EV@27p/50V_4
Y3 EV@27MHZ
R421 EV@1M_4
C583 EV@27p/50V_4
XTALI_27M
XTALO_27M

THERMAL

DPLUS
DMINUS
GPU_D+
GPU_D-
TS_FDO
TSVDD
TSVSS
TS_VDD

DAC1

R
RB
G
GB
B
BB
HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1DI
VSS1DI

EV_CRT_RED 24
EV_CRT_GRN 24
EV_CRT_BLU 24
EV_HSYNC 23,24
EV_VSYNC 23,24
R393 EV@150/F_4
R390 EV@150/F_4
R388 EV@150/F_4
R32 EV@499/F_4

(1.8V@70mA AVDD)
(1.8V@100mA VDD1DI)
+1.8V_GPU
L42 EV@SBY100505T-121Y-N/0.3A/120ohm_4
L5 EV@SBY100505T-121Y-N/0.3A/120ohm_4
120 ohm/300mA
C562 EV@0.1u/10V_4_X7R
C561 EV@10u/6.3V_6
C560 EV@10u/6.3V_6
C791 EV@1u/6.3V_4
C187 EV@0.1u/10V_4_X7R
C188 EV@10u/6.3V_6
C189 EV@10u/6.3V_6
C790 EV@1u/6.3V_4

DAC2

R2
R2B
G2
G2B
B2
B2B
C
Y
COMP
H2SYNC
V2SYNC
VDD2DI
VSS2DI
A2VDD
A2VDDQ
A2VSSQ
R2SET

DAC2 will be NC on future ASIC

T12
V2SYNC 23
VDD1DI
(3.3V@130mA A2VDD)
C165 EV@0.1u/10V_4_X7R
R34 EV@715/F_4

(1.8V@2mA A2VDDQ)
L41 EV@SBY100505T-121Y-N/0.3A/120ohm_4
C559 EV@0.1u/10V_4_X7R
C552 EV@1u/6.3V_4

DDC/AUX

DDC1CLK / DDC1DATA
AUX1P / AUX1N
DDC2CLK / DDC2DATA
AUX2P / AUX2N
DDCCLK_AUX3P / DDCDATA_AUX3N
DDCCLK_AUX4P / DDCDATA_AUX4N
DDCCLK_AUX5P / DDCDATA_AUX5N
DDC6CLK / DDC6DATA
NC_DDCCLK_AUX7P / NC_DDCDATA_AUX7N

MXM_DDCCK 25
MXM_DDCDAT 25

HDMI

T41 T43 T35 T22 T28 T21 T17 T44 T34 T39

DDCxx_AUX4x is NC on PARK

EV_LVDS_DDCCLK 24
EV_LVDS_DDCDAT 24

LVDS

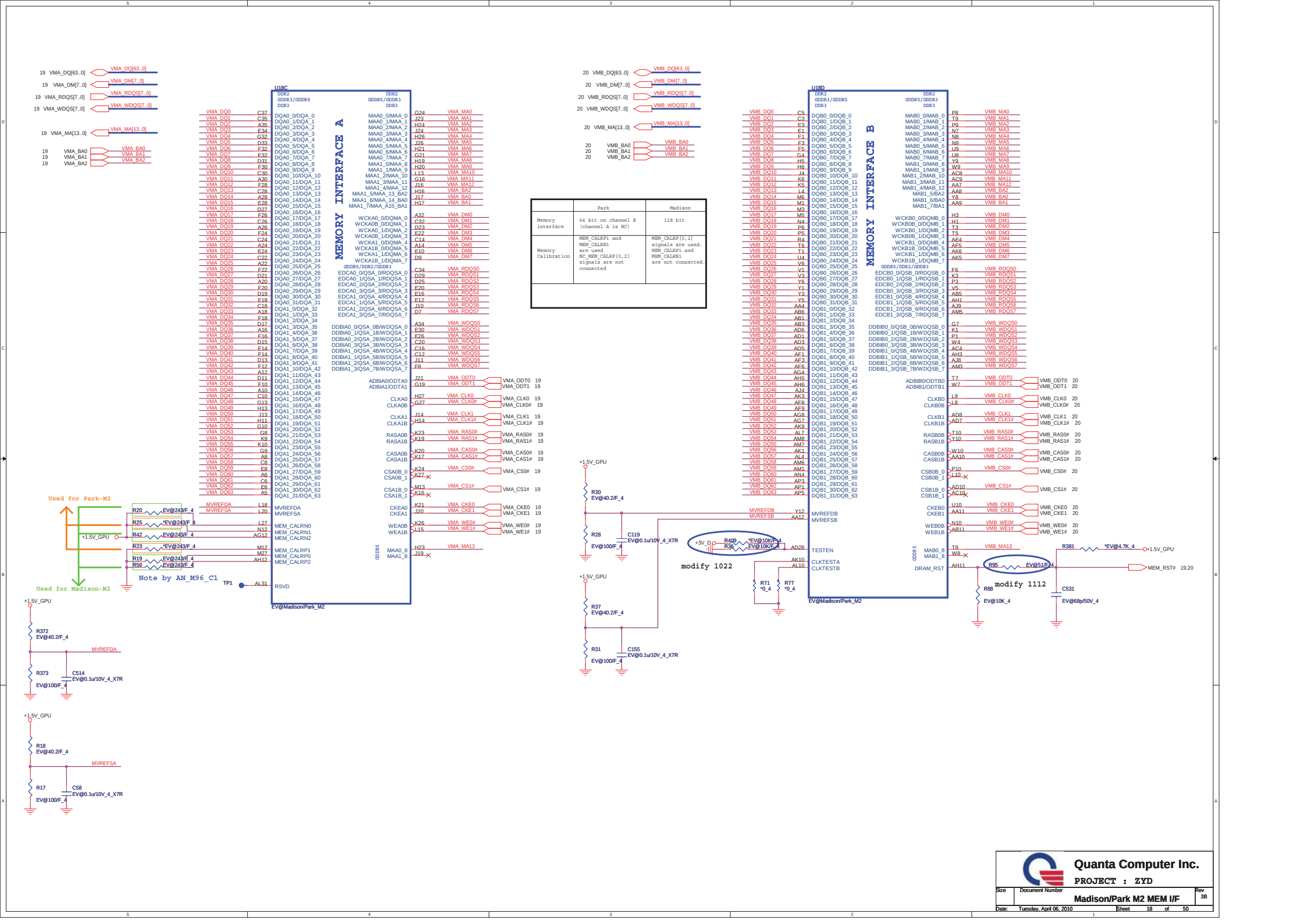
EV_CRTDCLK 24
EV_CRTDDAT 24

CRT

T38 T23

DDCxx_AUX7x is NC on M9x and PARK

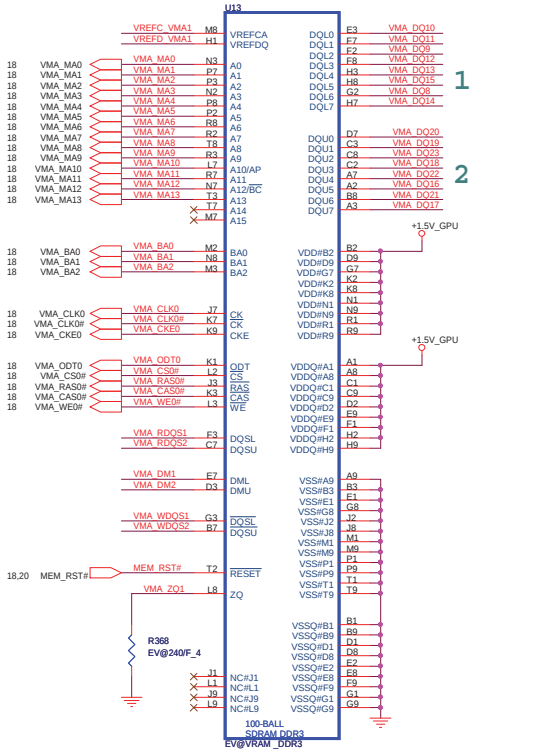
+1.8V(75mA)
+1.0V(125mA)
+1.8V(5mA)
120 ohm/300mA
L14 EV@SBY100505T-121Y-N/0.3A/120ohm_4
L22 EV@SBY100505T-121Y-N/0.3A/120ohm_4
L6 EV@SBY100505T-121Y-N/0.3A/120ohm_4
C213 C200 C196 EV@10u/6.3V_6 EV@0.1u/10V_4_X7R EV@1u/6.3V_4
C231 C216 C212 EV@10u/6.3V_6 EV@0.1u/10V_4_X7R EV@1u/6.3V_4
C207 C206 EV@10u/6.3V_6 EV@0.1u/10V_4_X7R


MEMORY INTERFACE A
MEMORY INTERFACE B
U18C
U18D
EV@Madison/Park_M2
Used for Park-M2
Used for Madison-M2
Note by AN_M96_C1
modify 1022
modify 1112
+1.5V_GPU
+3V_D
MEM_RST# 19,20
Quanta Computer Inc.
PROJECT : ZYD
Madison/Park M2 MEM I/F
Tuesday, April 06, 2010
Sheet 18 of 50

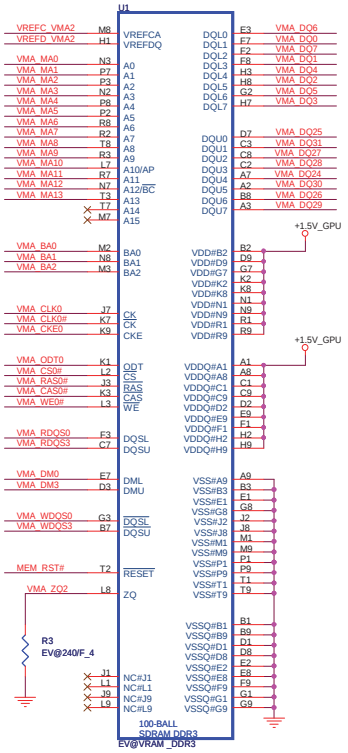
CHANNEL A: 512MB DDR3 (64M*16*4pcs)

Park, M92M Use Channel B Memory Interface Only

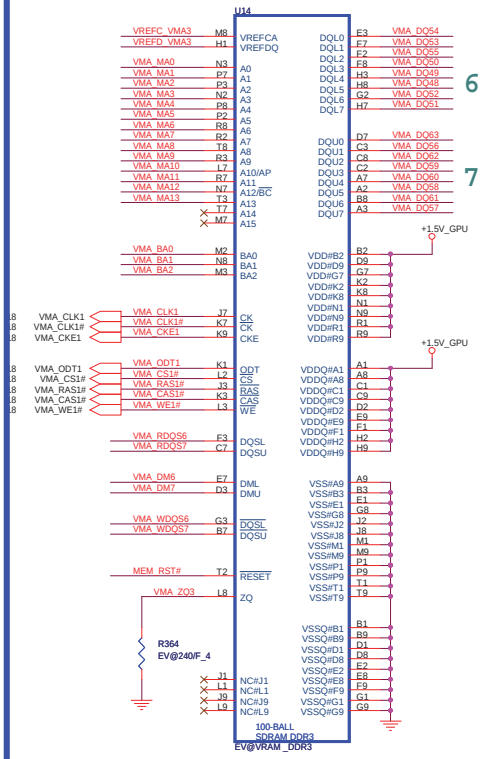
18 VMA_DQ[63..0] — VMA_DQ[63..0]
18 VMA_DM[7..0] — VMA_DM[7..0]
18 VMA_RDQS[7..0] — VMA_RDQS[7..0] QSA[7..0]
18 VMA_WDQS[7..0] — VMA_WDQS[7..0] QSA#[7..0]



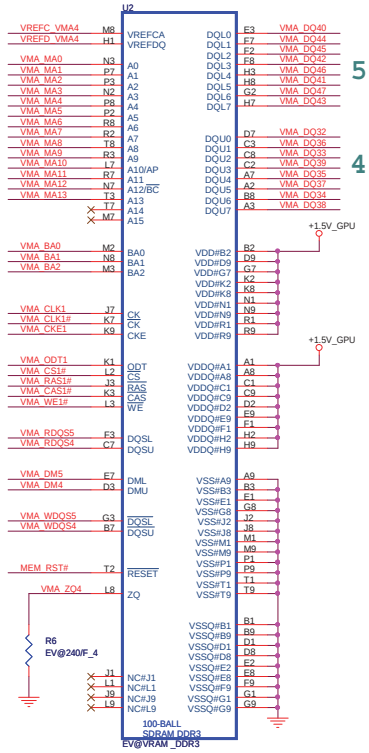
TOP Left



BOT Left

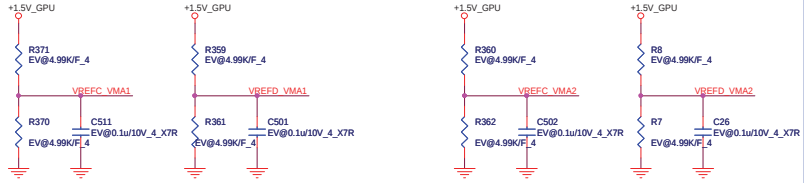


BOT Right

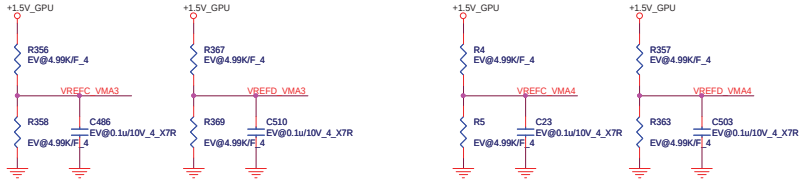


TOP Right

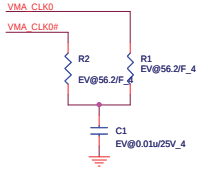
Group-A0 VREF



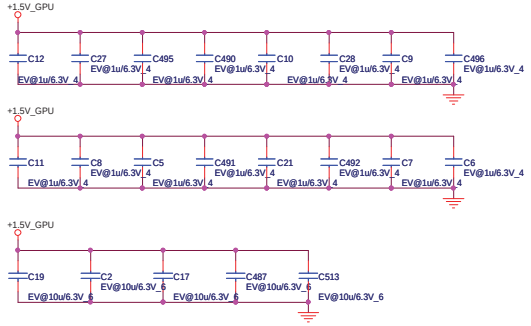
Group-A1 VREF



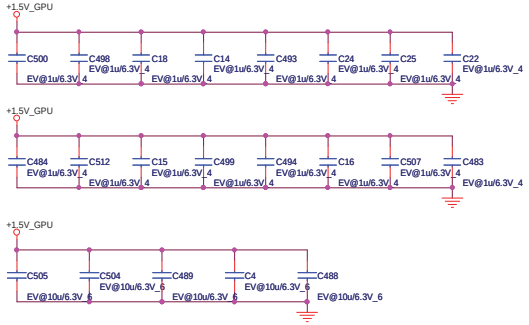
MEM_A0 CLK



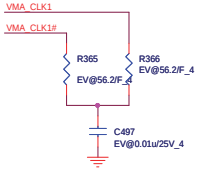
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



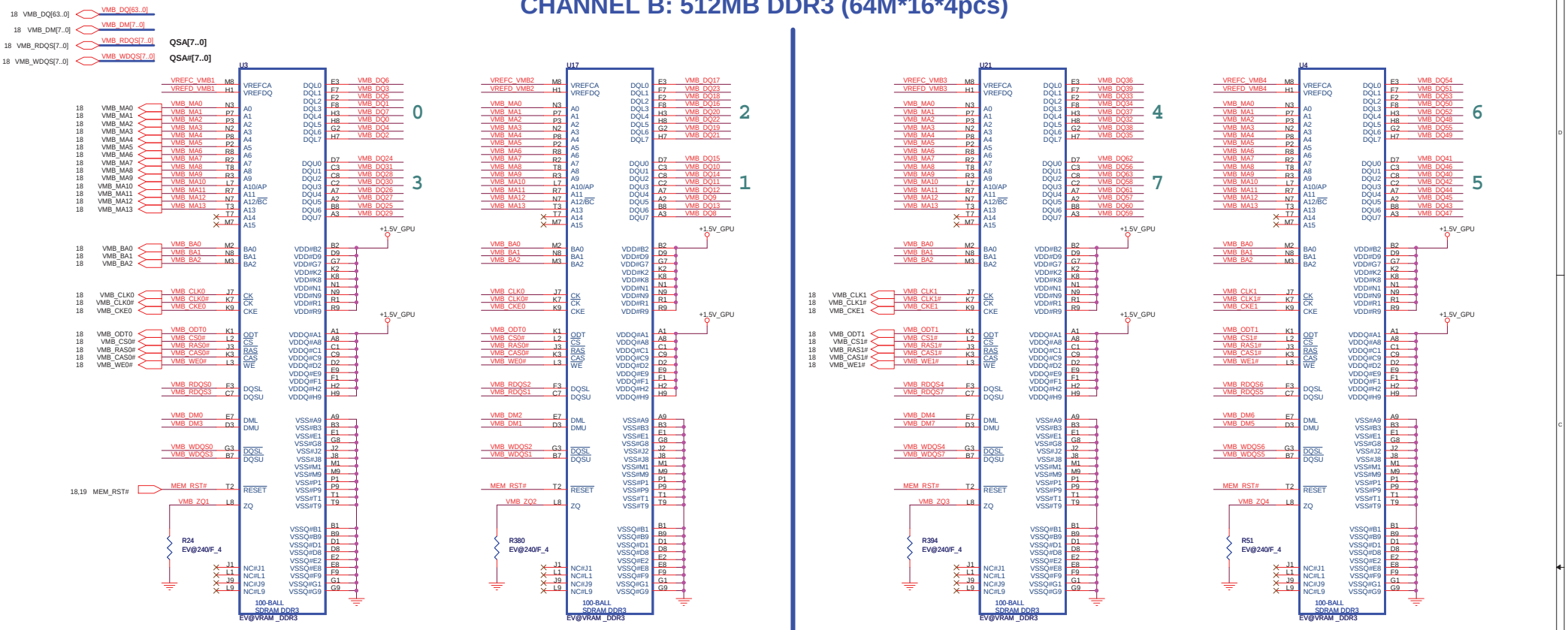
Quanta Computer Inc.

PROJECT : ZYD

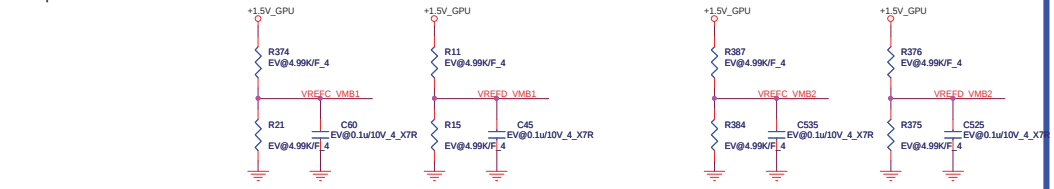
Size	Document Number	Rev
	MEMORY 1 channel A	3B

Date: Tuesday, April 06, 2010 Sheet 19 of 50

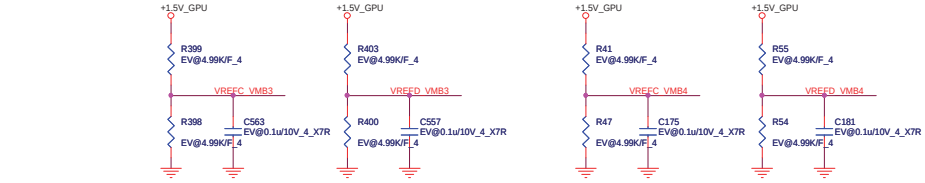
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



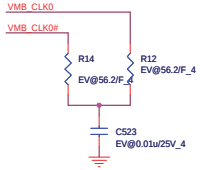
Group-B0 VREF



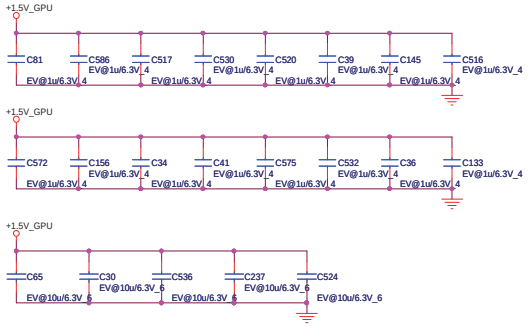
Group-B1 VREF



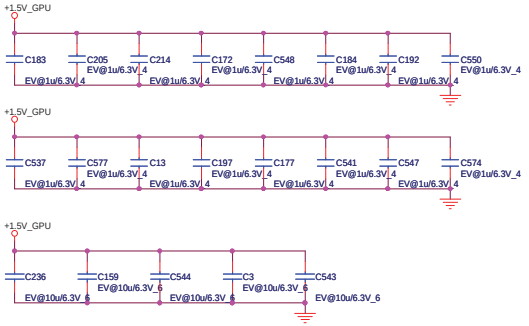
MEM_B0 CLK



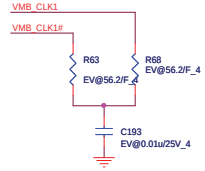
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	MEMORY 2 channel B	3B

Date: Tuesday, April 06, 2010 Sheet 20 of 50

For DDR3, MVDDQ = 1.5V (7.5A)

+1.5V_GPU

U18E

MEM I/O

PCIE

POWER

LEVEL TRANSLATION

I/O

PLL

VOLTAGE SENSE

CORE

ISOLATED CORE I/O

(1.8V@400mA PCIE_VDDR)

(1.0V@1.1A PCIE_VDDC)

(30A or more)

(1.8V@110mA VDD_CT)

(3.3V@60mA))

(For M97, Broadway, Madison and Park SPV10 = 1.0V)

(1.8V@40mA PCIE_PVDD)

(1.8V@75mA/Park & 150mA/Madison MPV18)

(1.8V@75mA SPV18)

(1.0V@120mA SPV10)

BIF_VDDC should be connected to VDDC if BACO feature not used.
For BACO, refer to the databook
Connect to VDDC in non-PowerXpress designs.

PIN different between Broadway and Madison

Pin	Broadway	Madison
N27 T27	VDDC	BIF_VDDC

VDDC and VDDCI are assigned to different sets of balls on M97, Madison and Park. As a result, VDDC and VDDCI will be shorted when a M96 is populated on a compatible design.

Modify 1022

VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator

(DDR3 1.12V@4A VDDCI) or more

modify 1230_B

VDDC_SENSE/VSS_SENSE and VDDCI_SENSE/VSS_SENSE route as differetial pair

EV@Madison/Park_M2

GND

PowerXpress control signal for Madison and Park only
If not used, can be disconnected.
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
PX_EN is used to turn ON/OFF some regulators for PowerXpress mode. An output high "3.3V" will turn the regulators OFF. An output low "0V" will turn the regulators ON. PX_EN outputs low (0V) by default.
If this signal is unused, it can be NC (not connected) or connected to ground.

Modify 1022

GPU +3V power

Q8 EV@PDTC143TT

Q9 EV@AO3413

0.5A

GPU all PWROK

Q10 EV@PDTC143TT

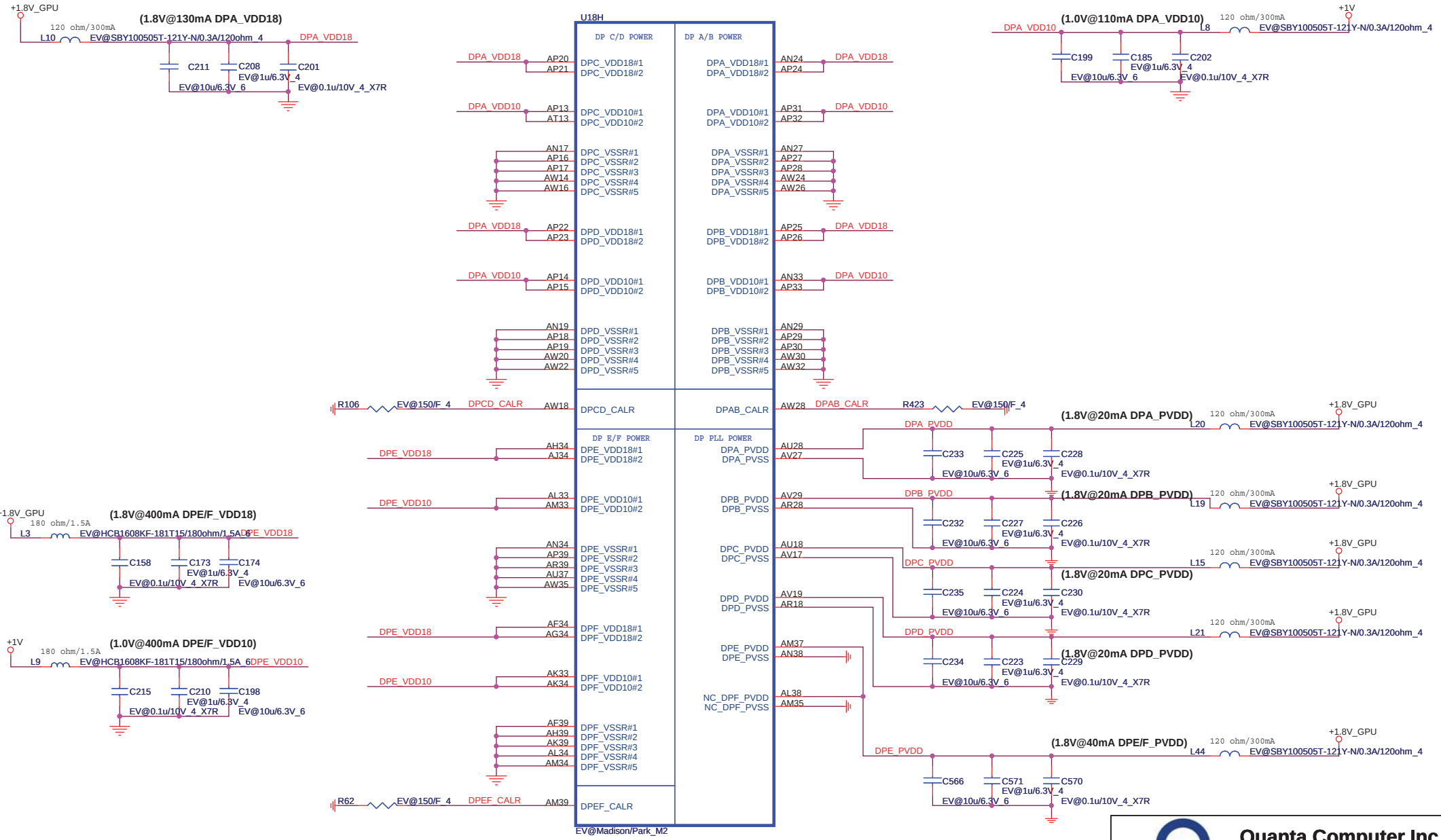
Q12 EV@2N7002E

dGPU_PWROK 11,36

Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	Madison/Park M2 MEM I/F	3B

Date: Tuesday, April 06, 2010 Sheet 21 of 50

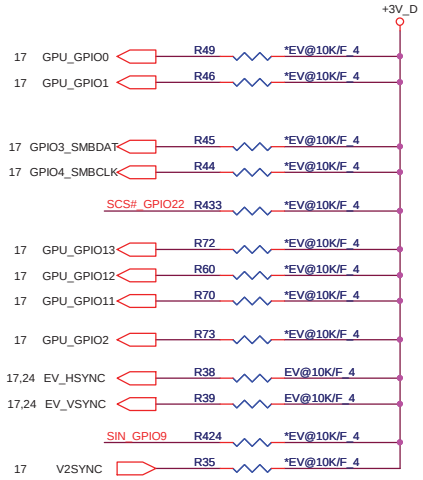


Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	Madison/Park M2 DPPW_GND	3B
Date: Tuesday, April 06, 2010	Sheet 22 of 50	

PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

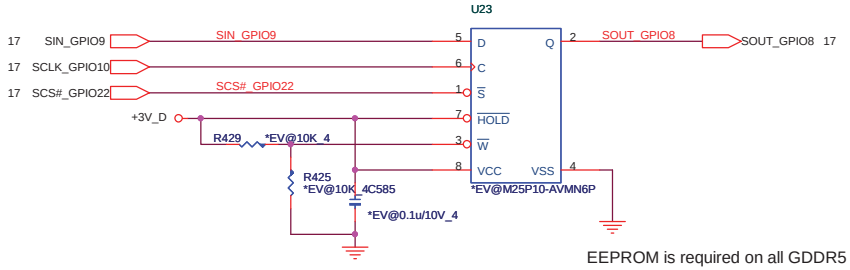
Audio Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

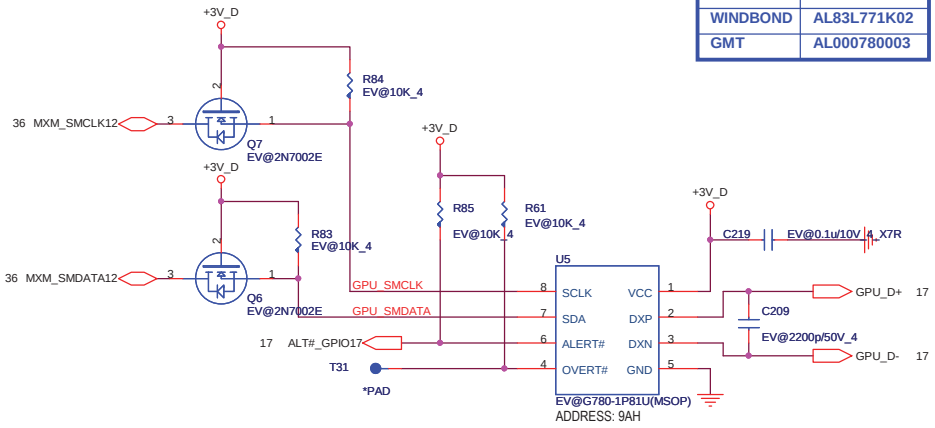
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	000	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM



EEPROM is required on all GDDR5 designs

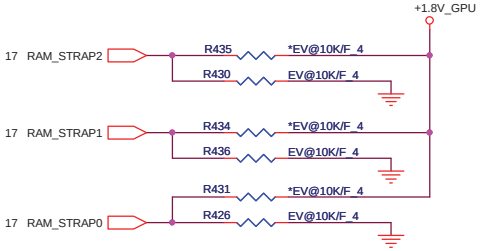
Thermal Sensor



NS	none
WINDBOND	AL83L771K02
GMT	AL000780003

DDR3 Memory Aperture size

DDR3 VRAM size						
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			512MB	1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	1	0	0
			2GB	1	0	1
Samsung			512MB	0	1	0
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1
AMD	23EY2387MA-12	AKD5LGGT700		0	1	0



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

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	Strip/Thermal	3B
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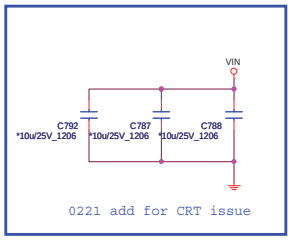
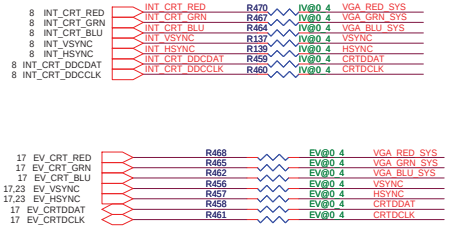
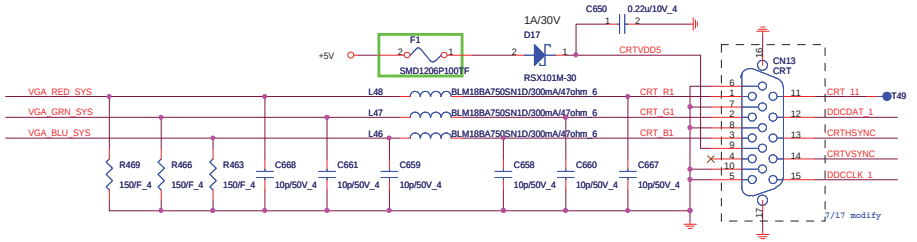
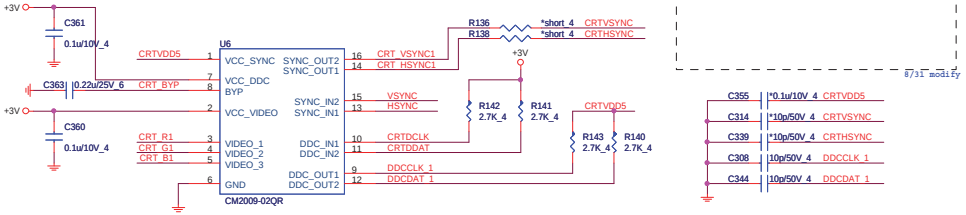
CRT(CRT)

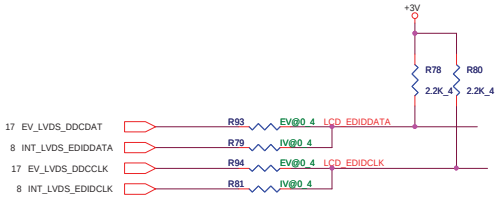


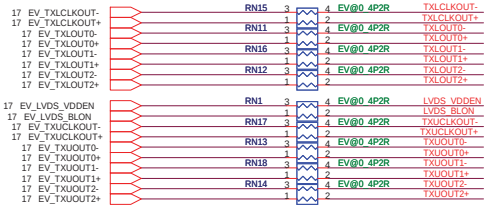


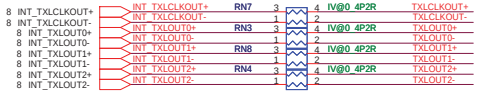


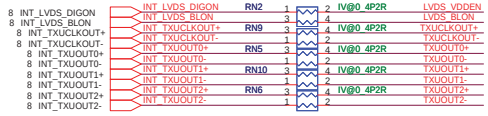


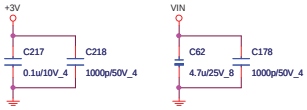
LVDS(LDS)

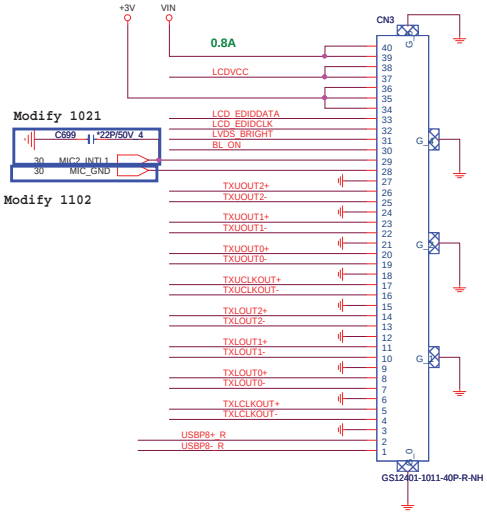




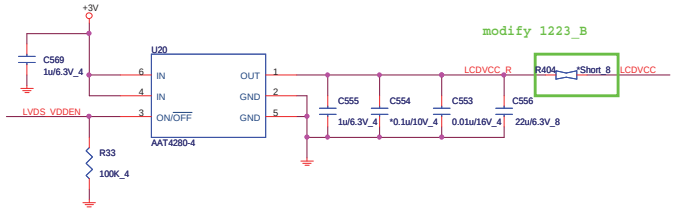




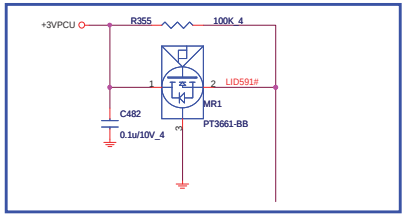




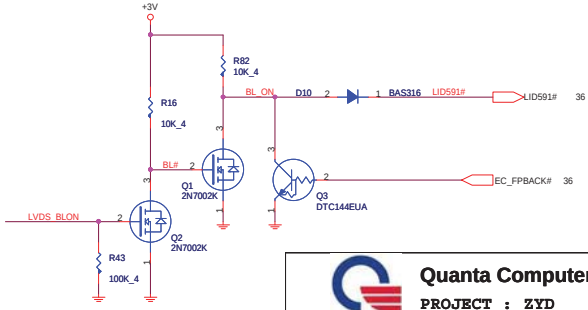
LCD Power(LDS)



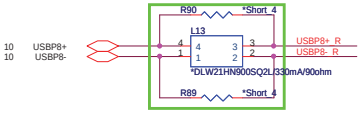
Hall Sensor(HSR)



Backlight Control(LDS)



CAMERA Module(CCD)



Amos 0325

Quanta Computer Inc.

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	CRT/LVDS	3B
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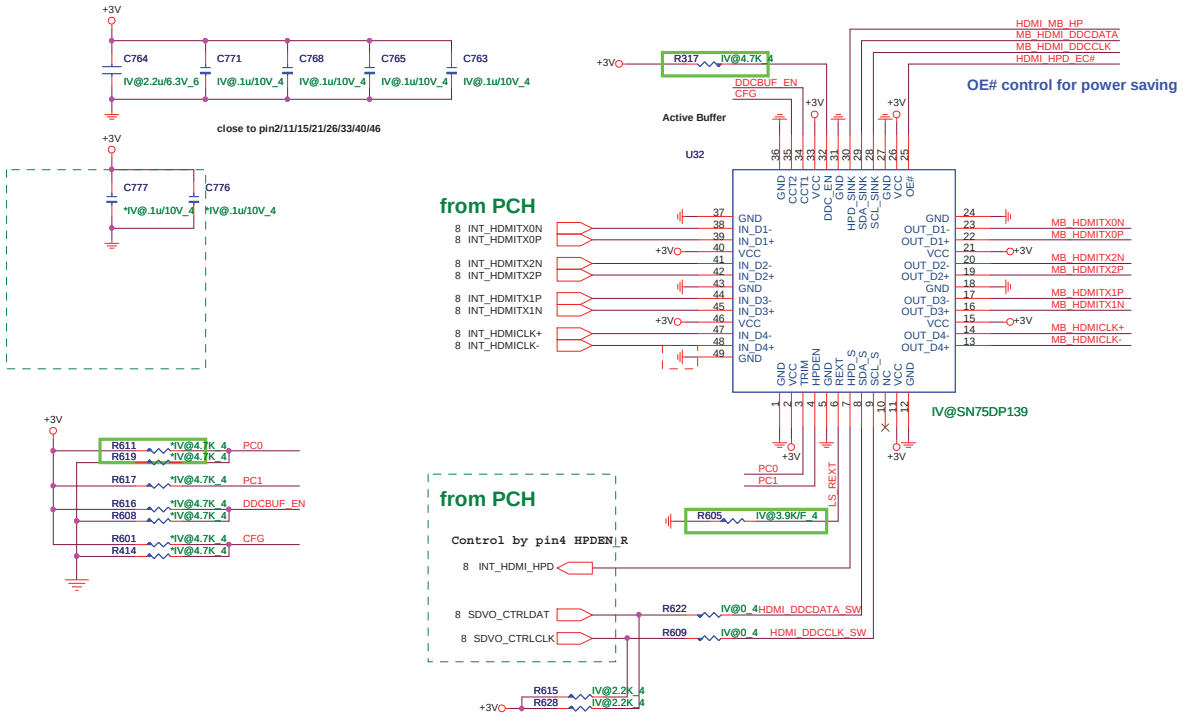
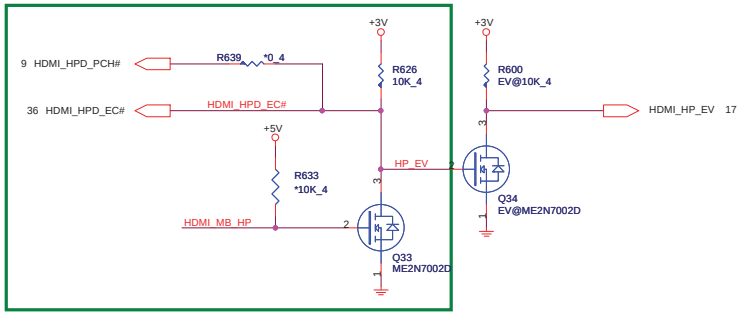
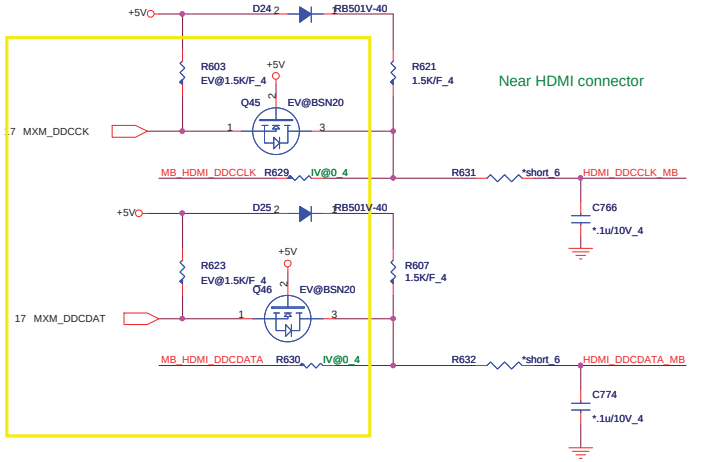
IV@ HDMI LEVEL SHIFTER



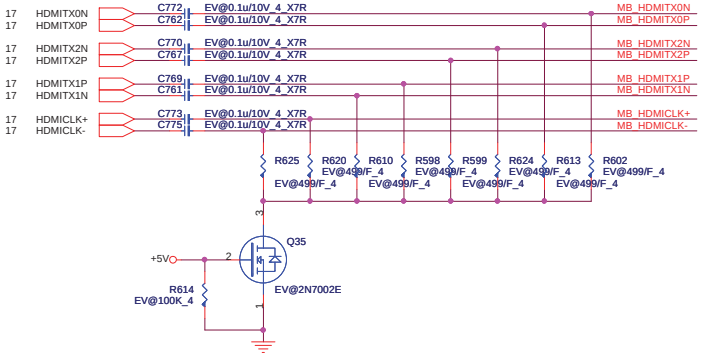
HDMI-detect



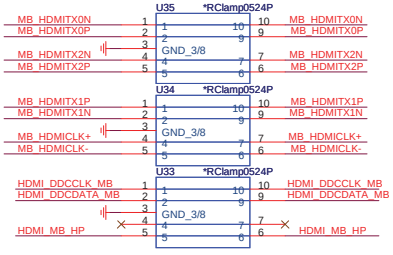
I2C



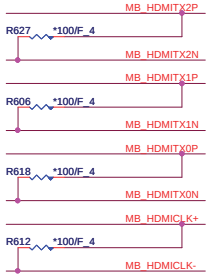
External Graphic HDMI source



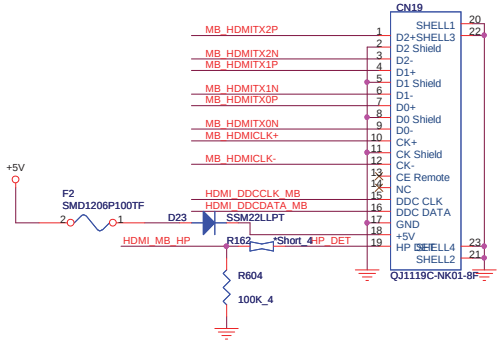
ESD Protect



EMI



HDMI connector



Quanta Computer Inc.			
PROJECT : ZYD			
Size	Document Number	HDMI (SN75DP139)	Rev 3B
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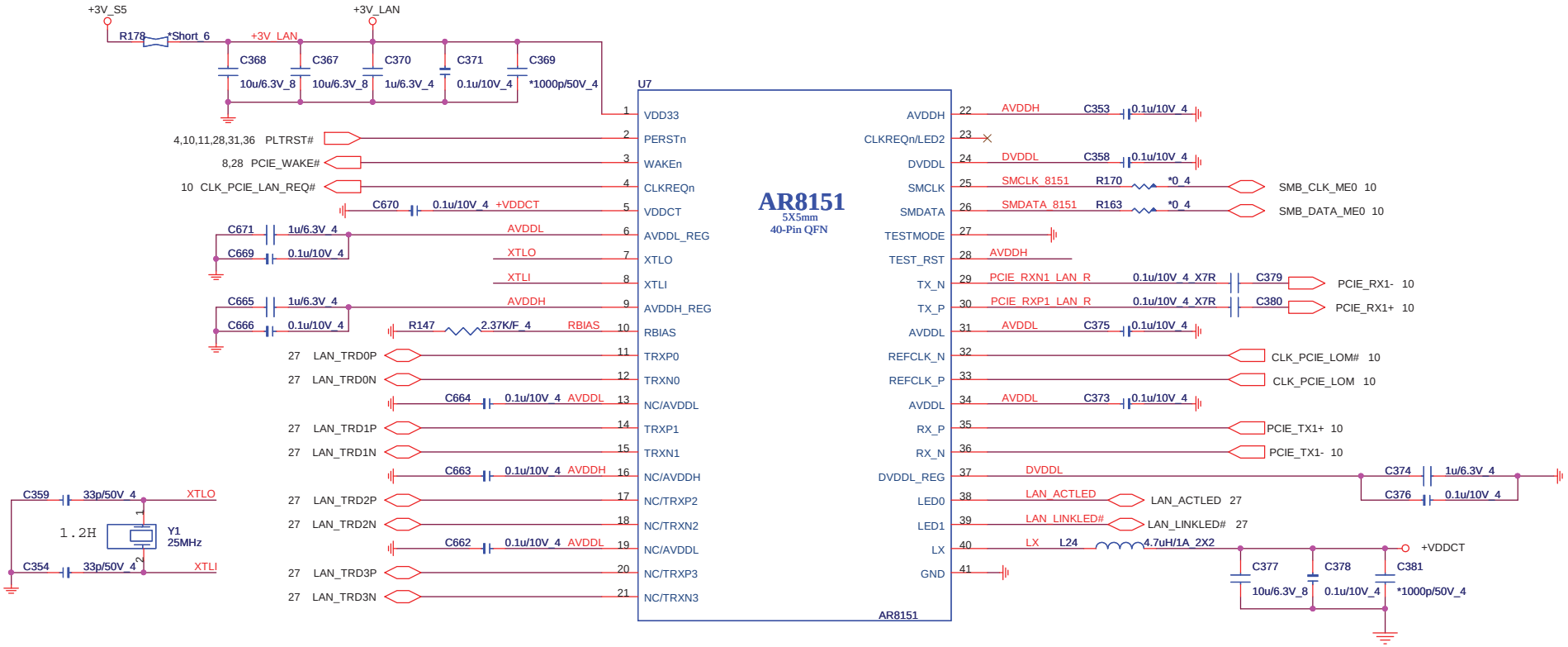
Giga-LAN AR8151



Quanta Computer Inc.

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Size	Document Number	Rev
	GLAN BCM57780	3B
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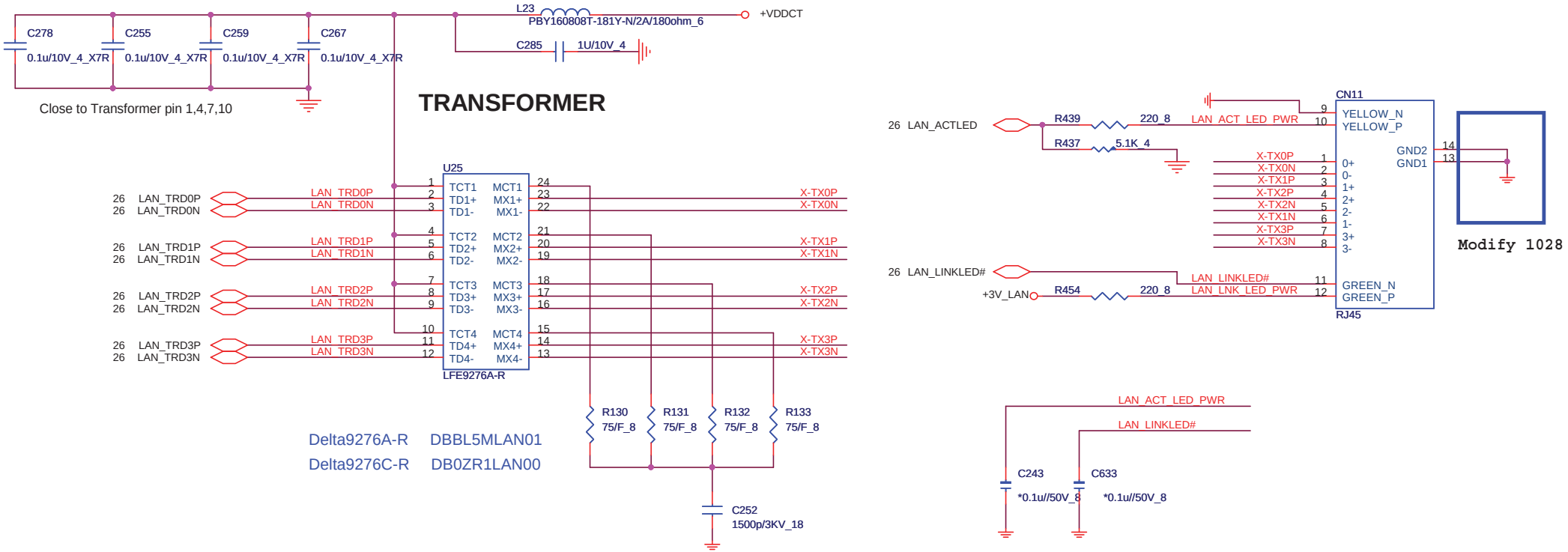

Quanta Computer Inc.		
PROJECT : ZYD		
Size	Document Number: LAN Transformer and RJ45	Rev: 3B
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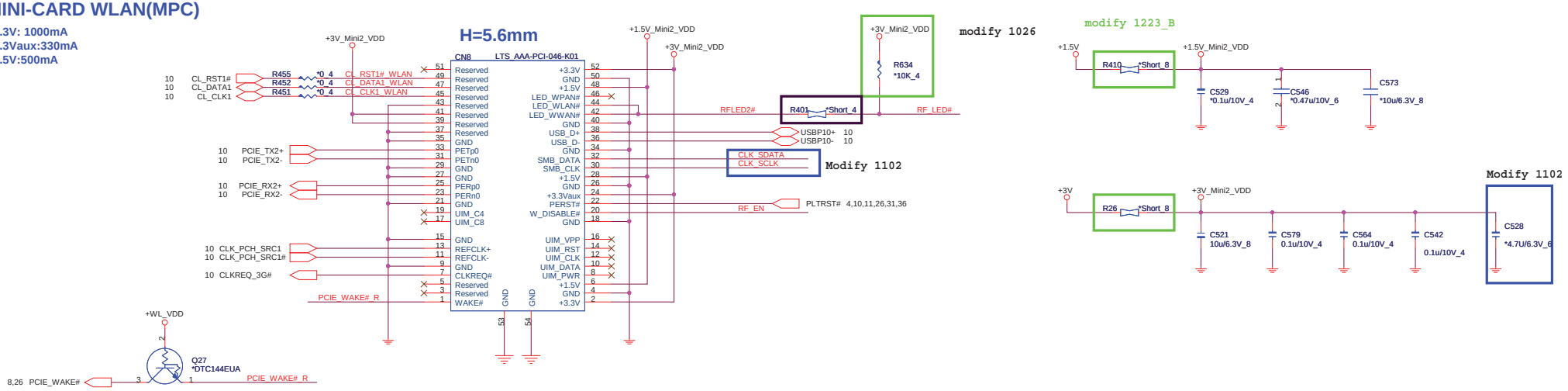
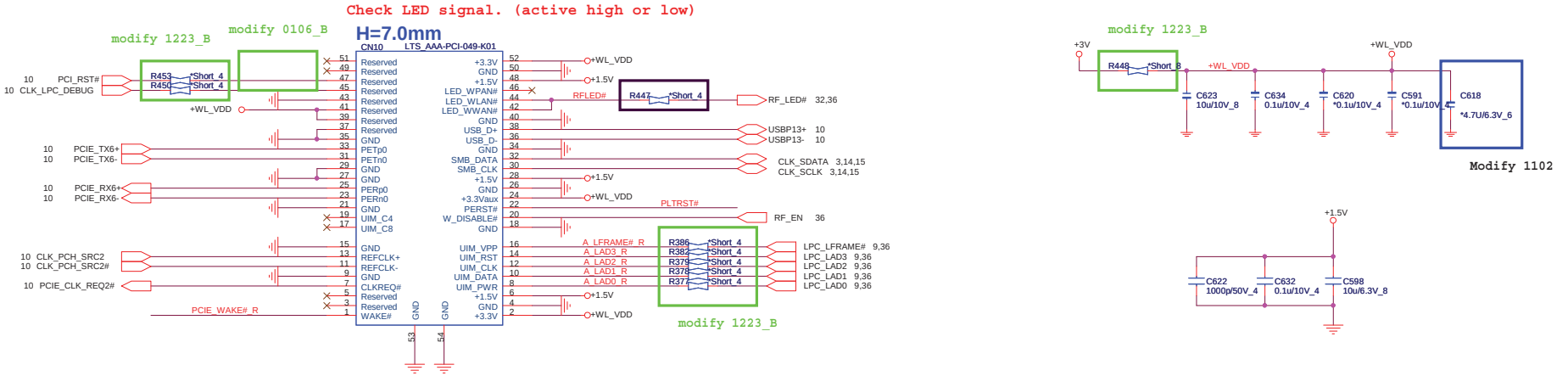
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



MINI-CARD (MNC)Reserve for BA70



Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	MINI PCI-E card/TV	3B

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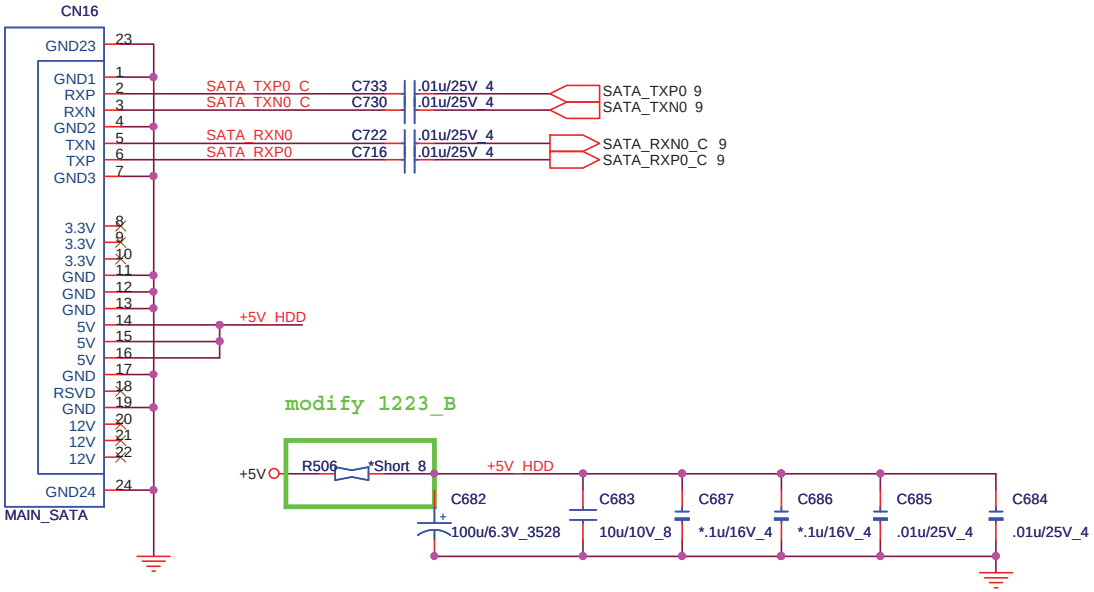
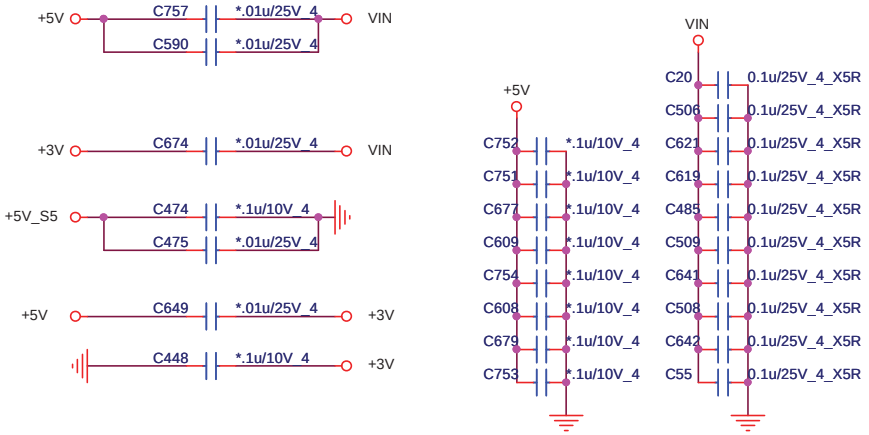
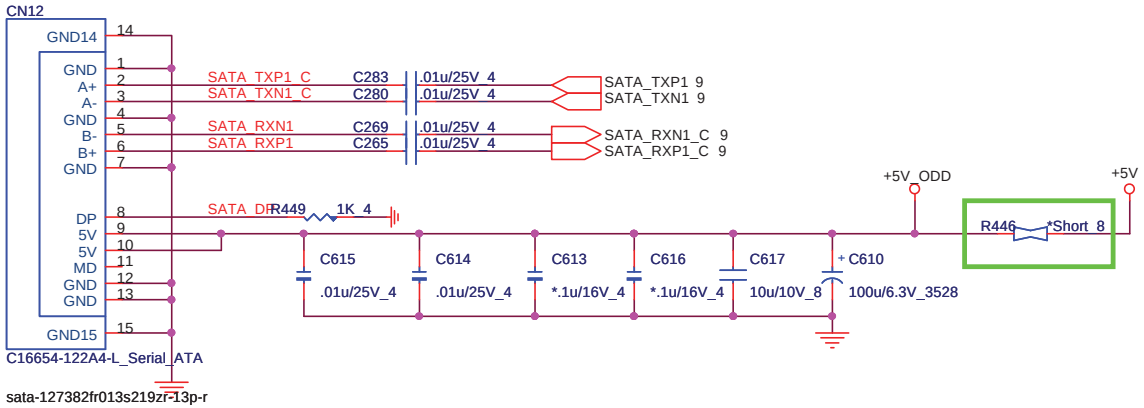
MAIN SATA HDD



EE RETURN-PATH CAPACITORS



ODD (SATA)



Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	3B
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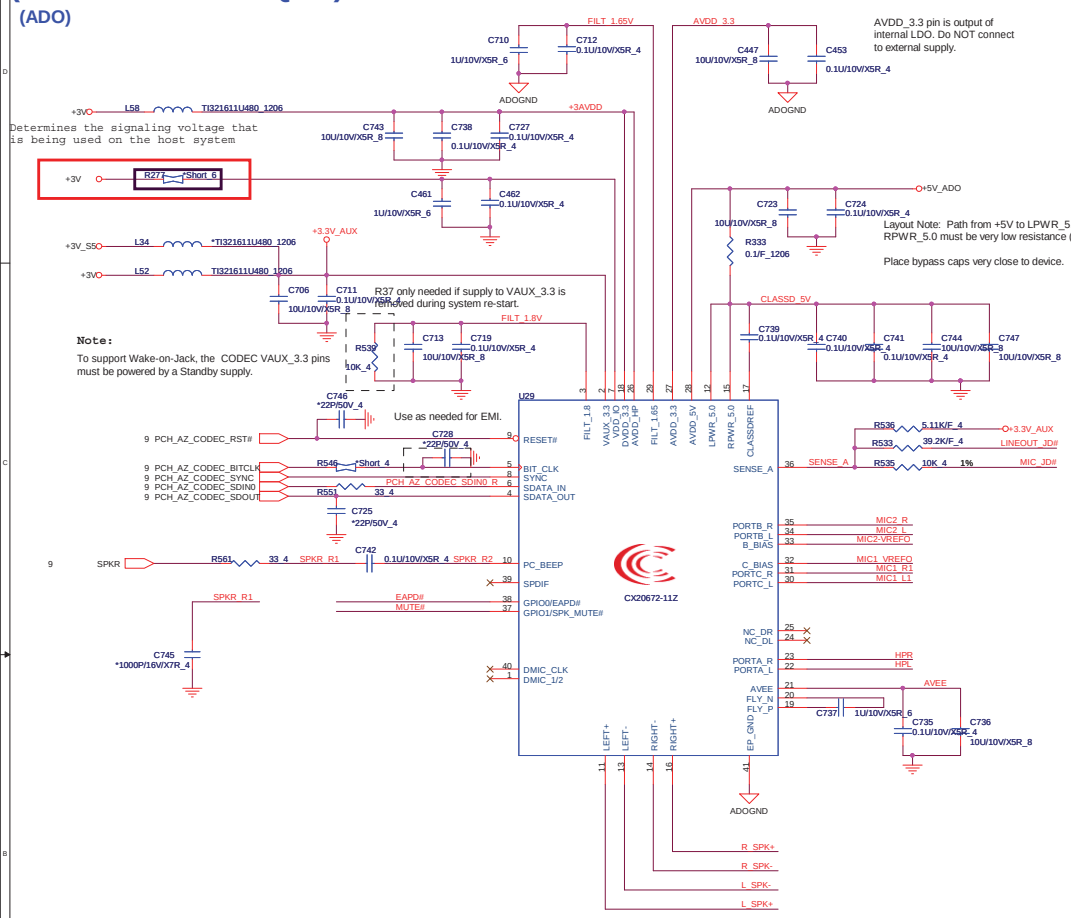
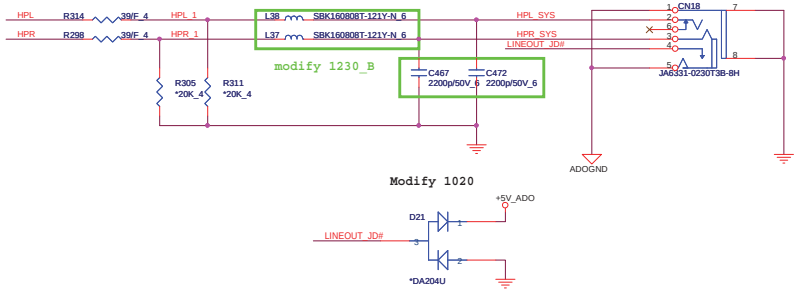
Codec(ADO)

(CX20672-11Z for QFN)

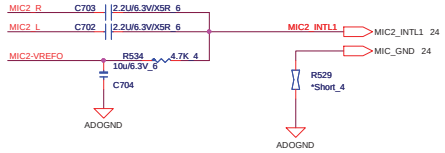
(ADO)



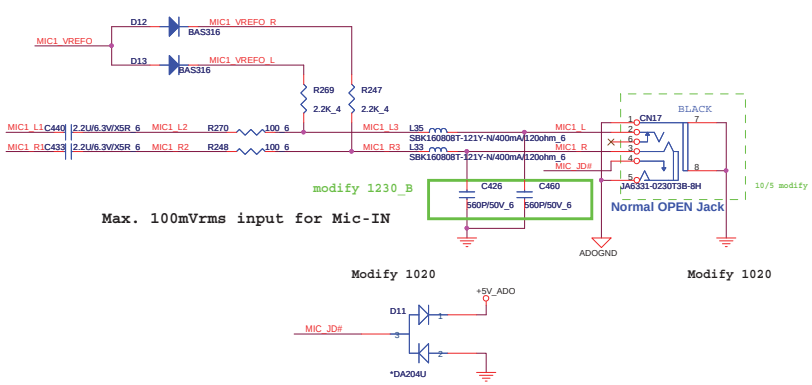
Headphone



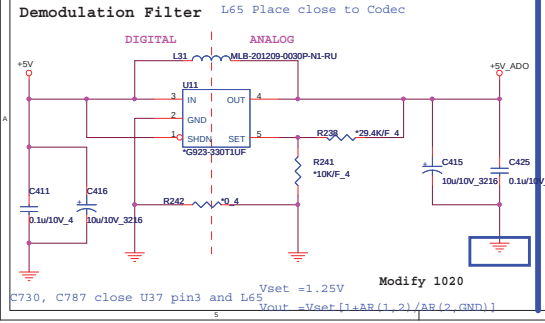
INT. MIC



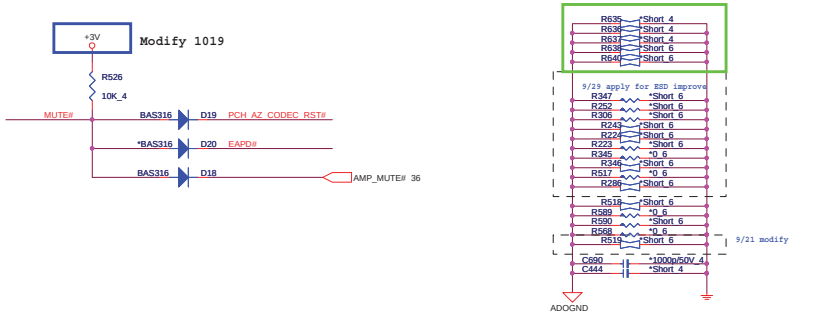
EXT. MIC



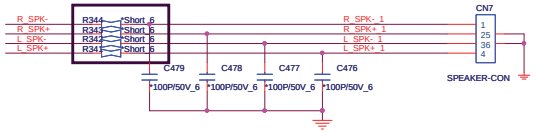
Power (ADO)



Mute(ADO)



Internal Speaker(AMP)



Quanta Computer Inc.

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	CX20672-11Z	3B

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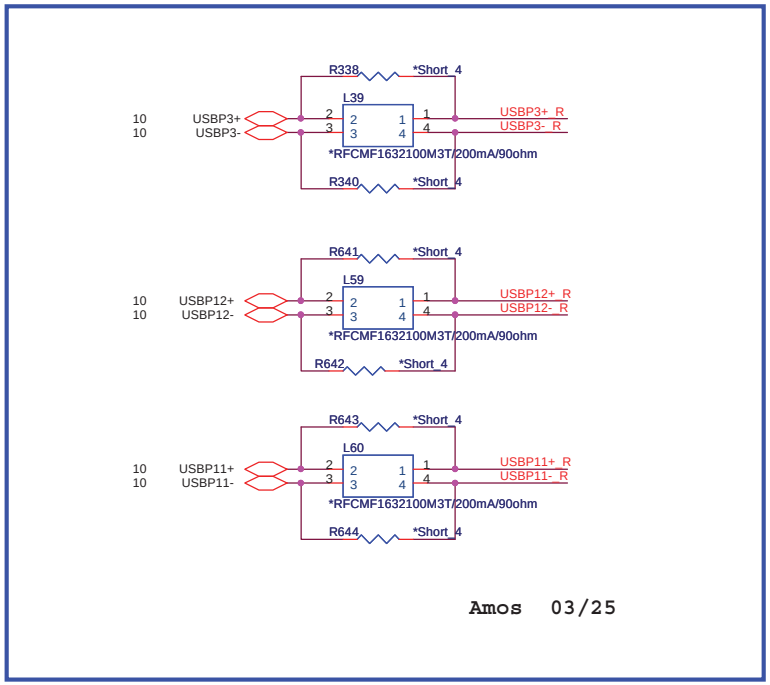
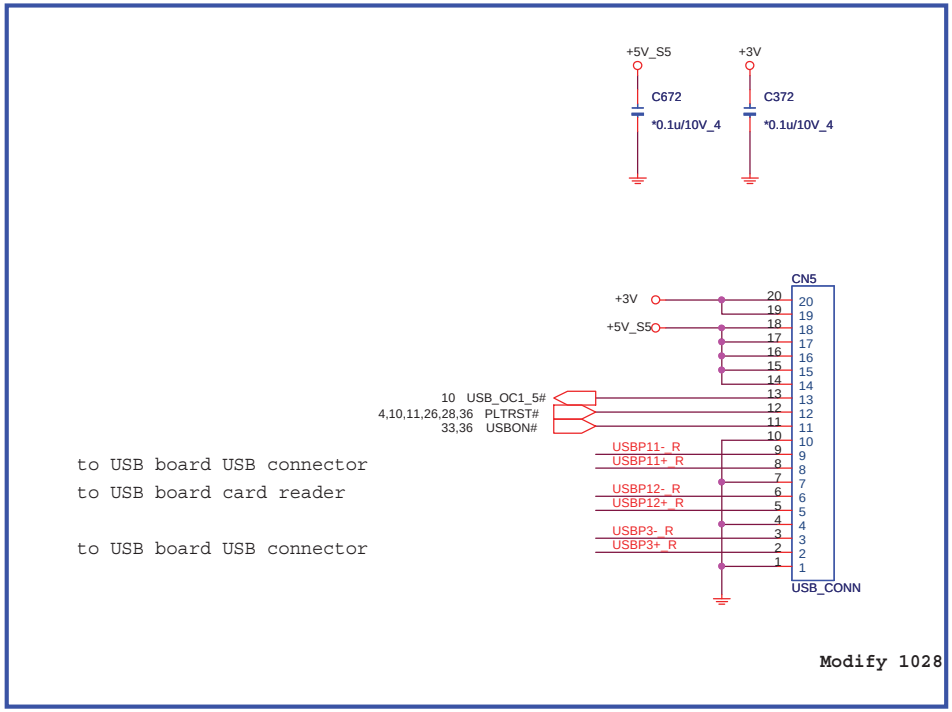
Cardreader CONN(MMC)





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PROJECT : ZYD		
Size	Document Number: CardReader &USB/B	Rev: 3B
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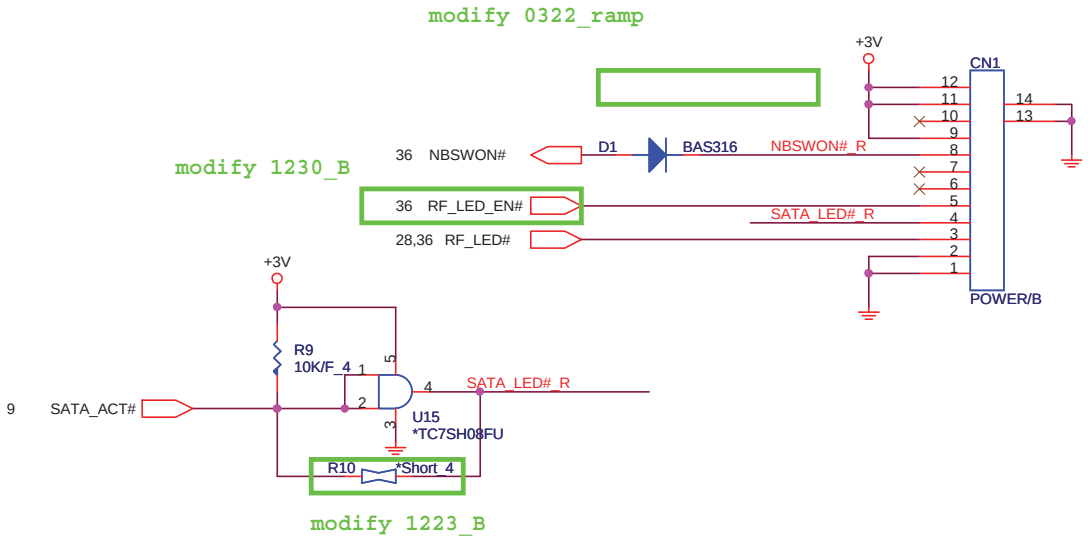
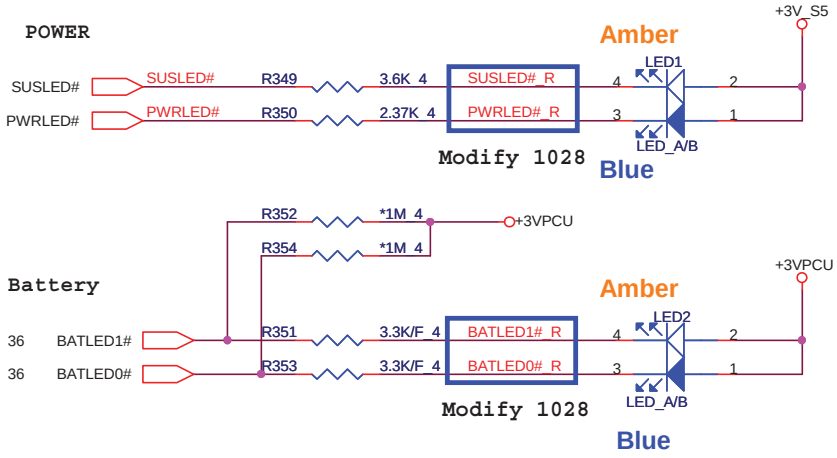
POWER BOARD CONN(UIF)



LED(UIF)



Quanta Computer Inc.

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	POWER/MMB/LAUNCH/LED	3B

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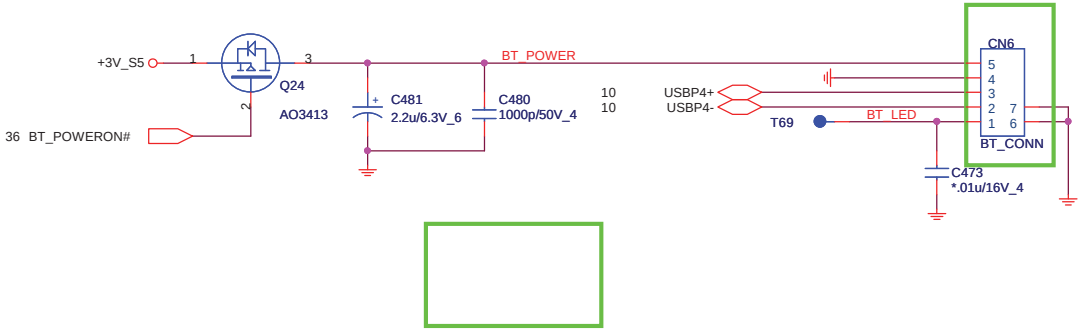
Modify 1022

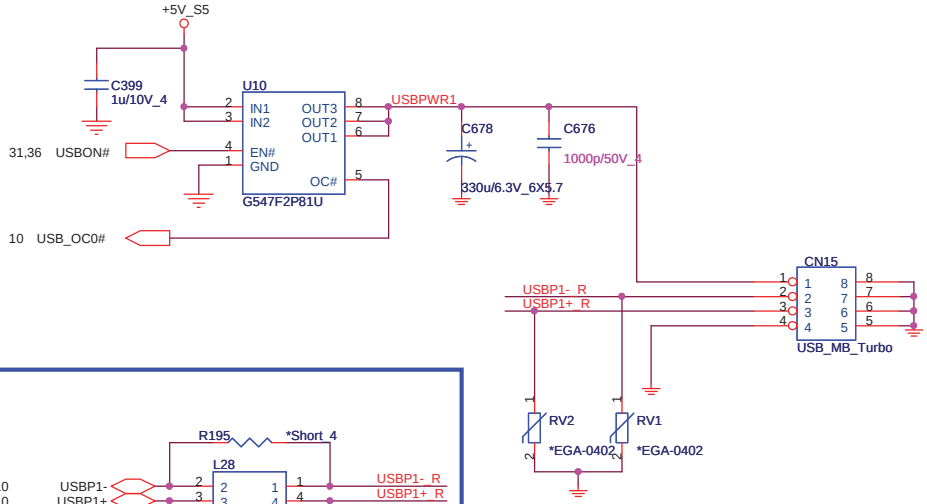
BLUETOOTH CONNECTOR(BTM)

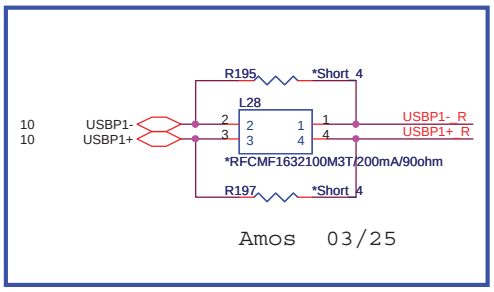
modify 1223_B



modify 0224_C

USBX1(USB)





Quanta Computer Inc.

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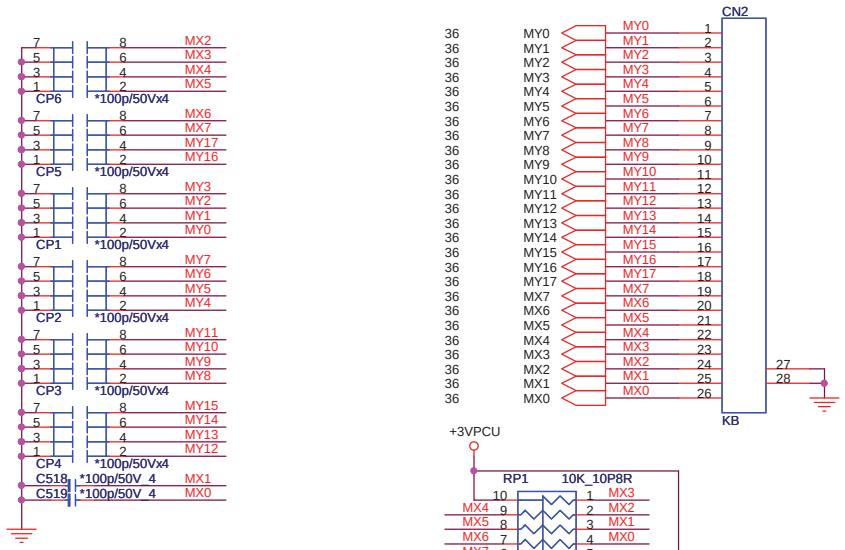
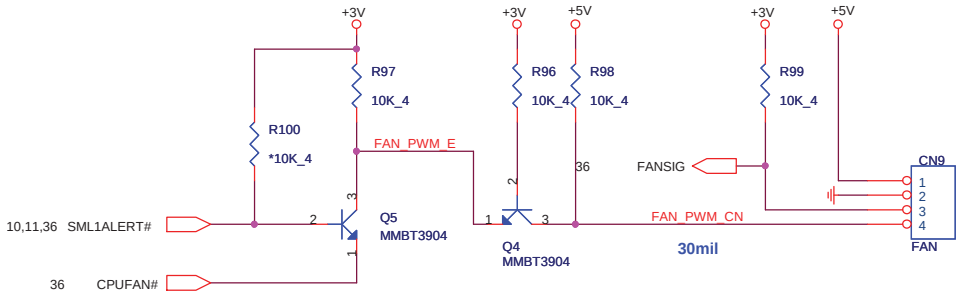
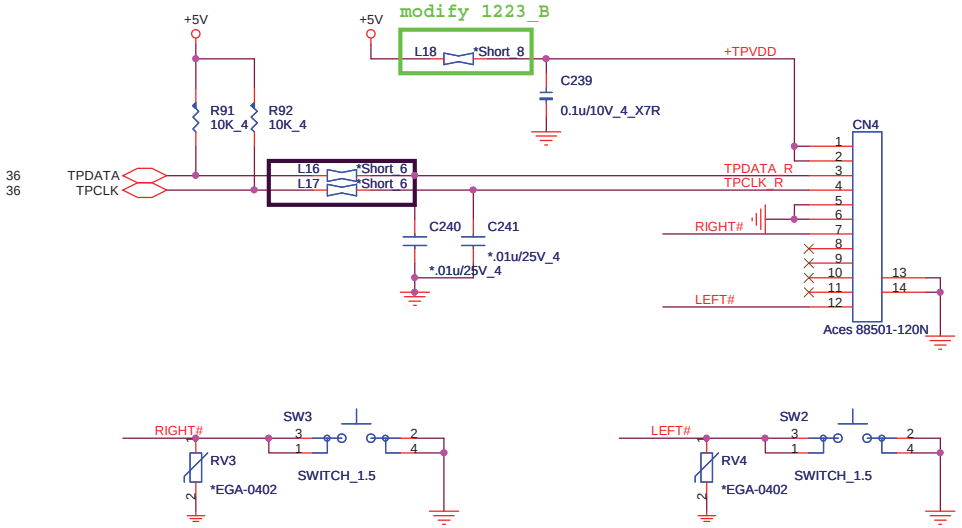
K/B

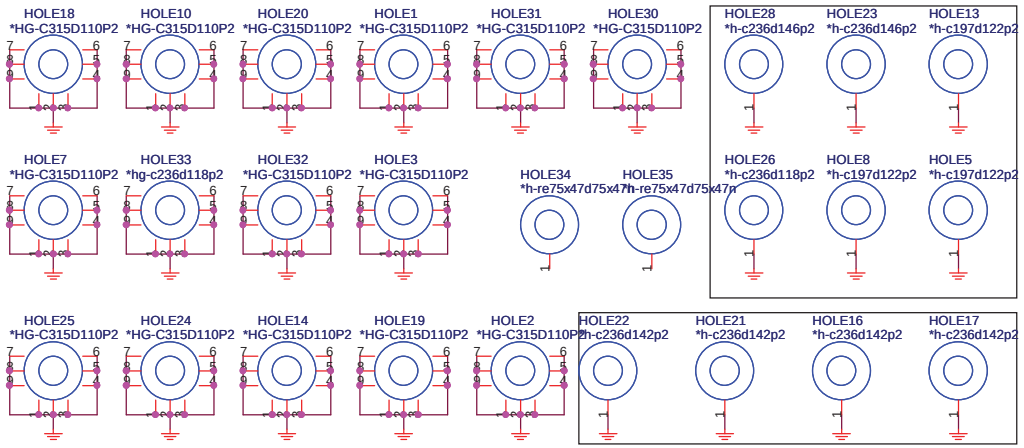


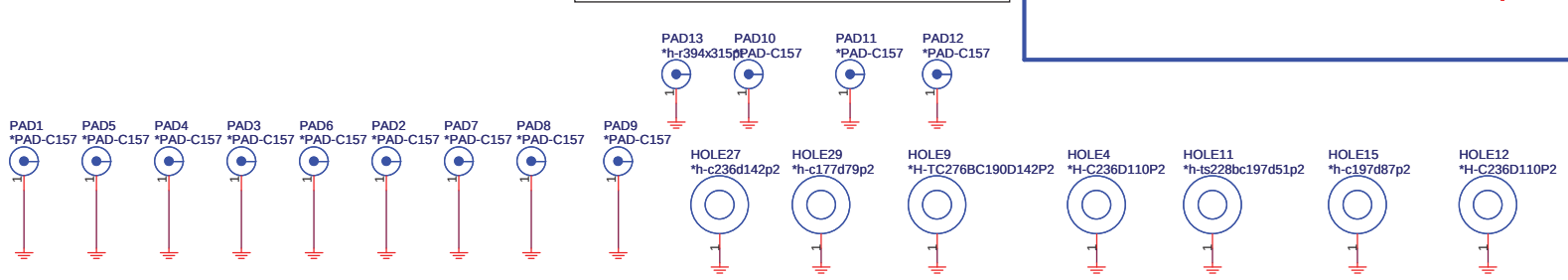
CPU FAN(THM)



TOUCHPAD & Switch CONN.(TPD)







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	KB/FAN/TP+FP	3B
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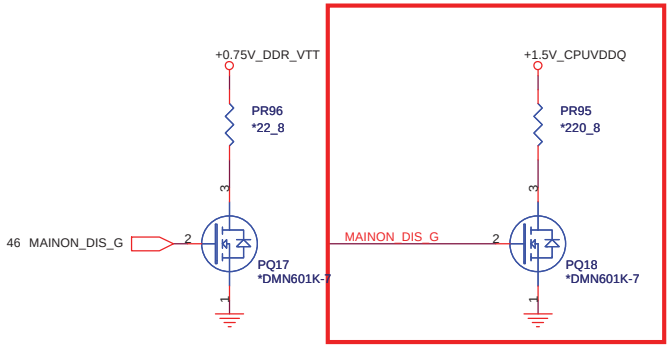
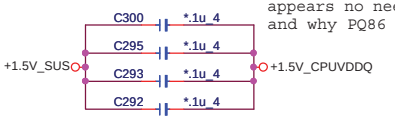
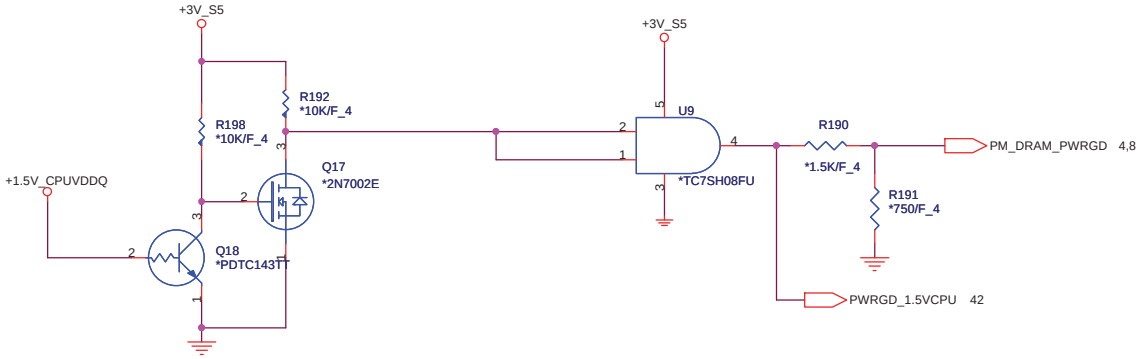
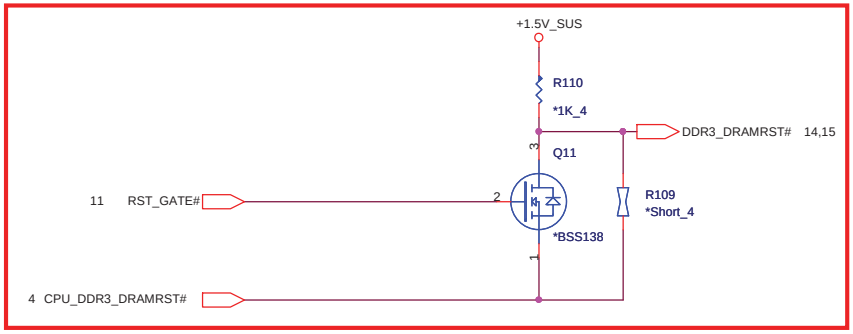
SM_DRAMRST# signal (to system memory) to be driven high
CKE signals (to system memory) to be driven low
VREFDQ and VREFCA voltage (on system memory) needs to be maintained
1.5-V power rail to system memory to be maintained.
All other DDR3 memory interface signals are don't care during S3 state for
memory self refresh.
SM_DRAMPWROK (to processor) is driven low during S3 as Processor VDDQ (1.5 V)
is turned off with this implementation.

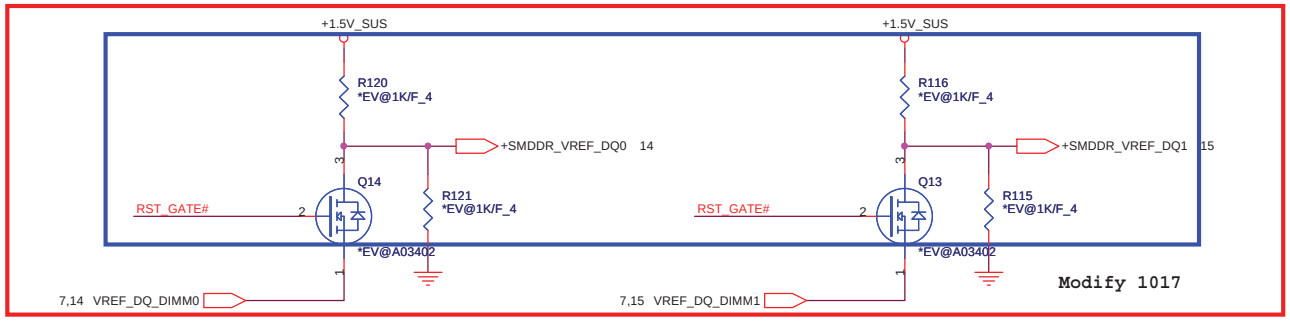


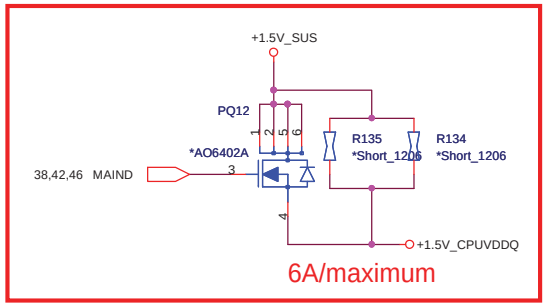
appears no need stuff if PQ12 don't stuff
and why PQ86 is 220ohm







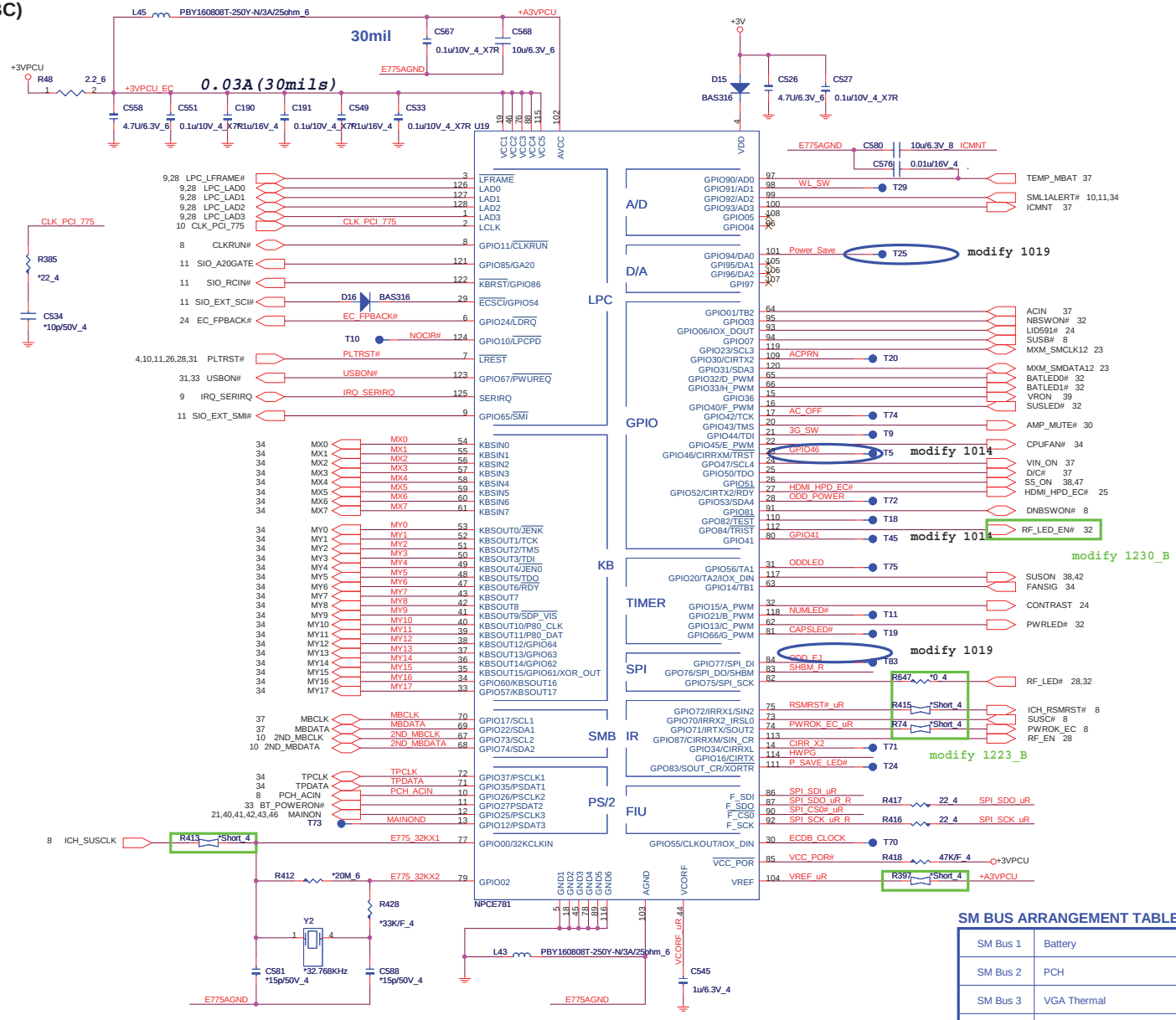




These isolation FETs are not required for ARD-only
designs. Only CFD and common motherboard designs need to implement this circuit to
meet the DDR3 VREF specification during S3.

Quanta Computer Inc.		
PROJECT : ZYD		
Size	Document Number: S3 power saving	Rev: 3B
Date: Tuesday, April 06, 2010	Sheet 35 of 50	

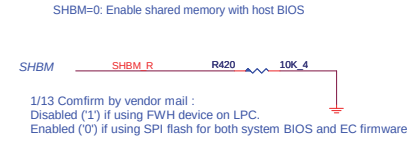
EC(KBC)



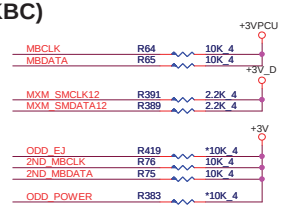
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA Thermal
SM Bus 4	

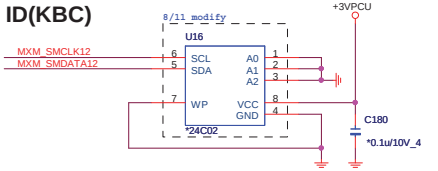
I/O ADDRESS SETTING(KBC)



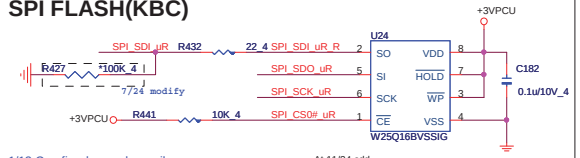
SM BUS PU(KBC)



ACER ID(KBC)



SPI FLASH(KBC)

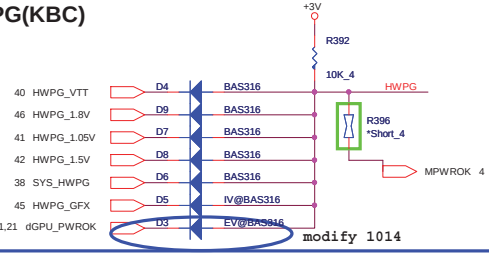


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

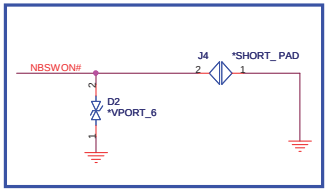
At 11/24 add

Winbond	W25X16AVSSIG	AKE38ZP0N01
MXIC	MX25L1605AM2C-15G	AKE37FP0Z13
EON	EN25F16-100HIP	AKE38ZA0Q00
AMIC	A25L016	AKE38ZN0800

HWPG(KBC)



POWER-ON Switch(KBC)



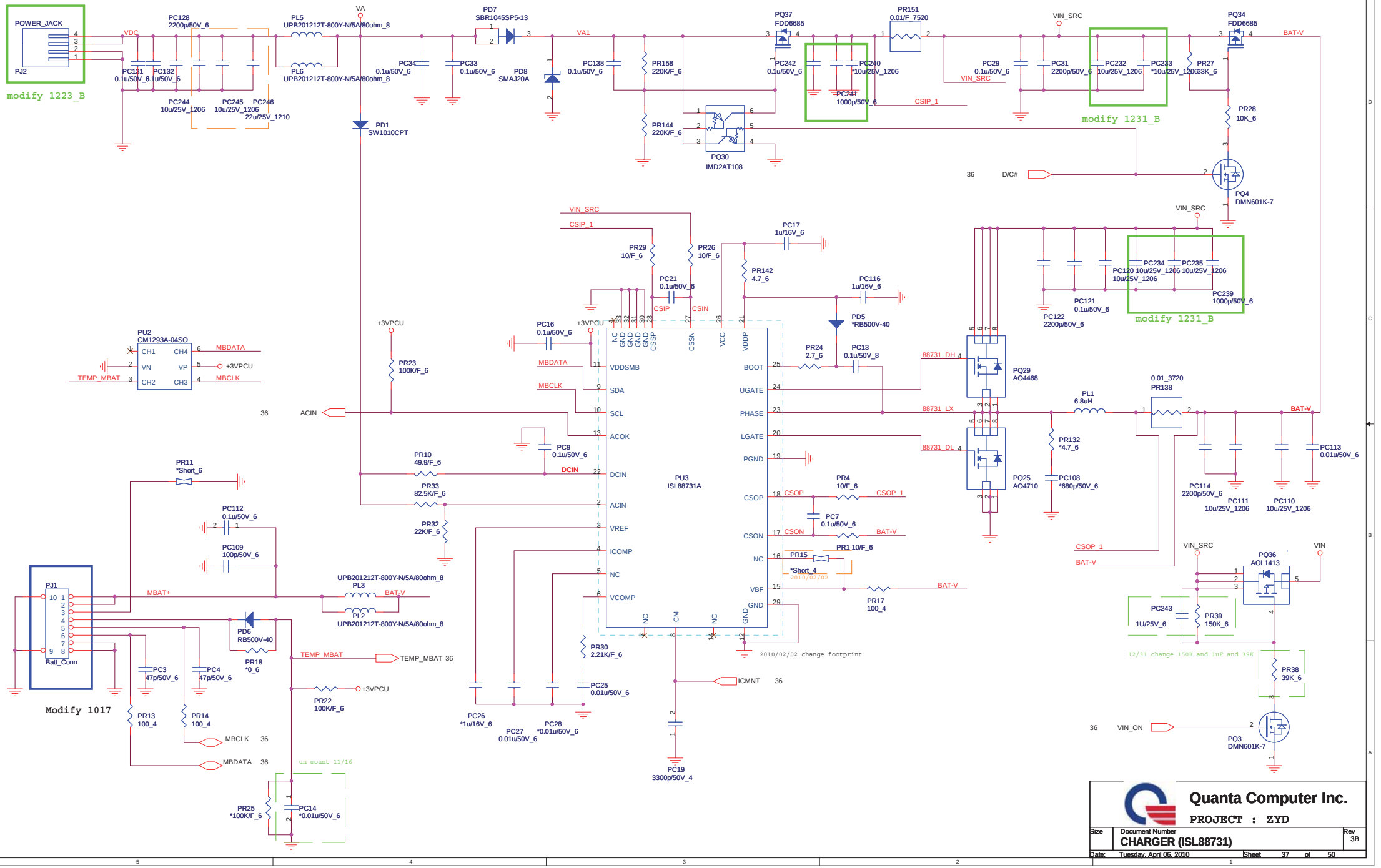
INTERNAL KEYBOARD STRIP SET(KBC)

Quanta Computer Inc.

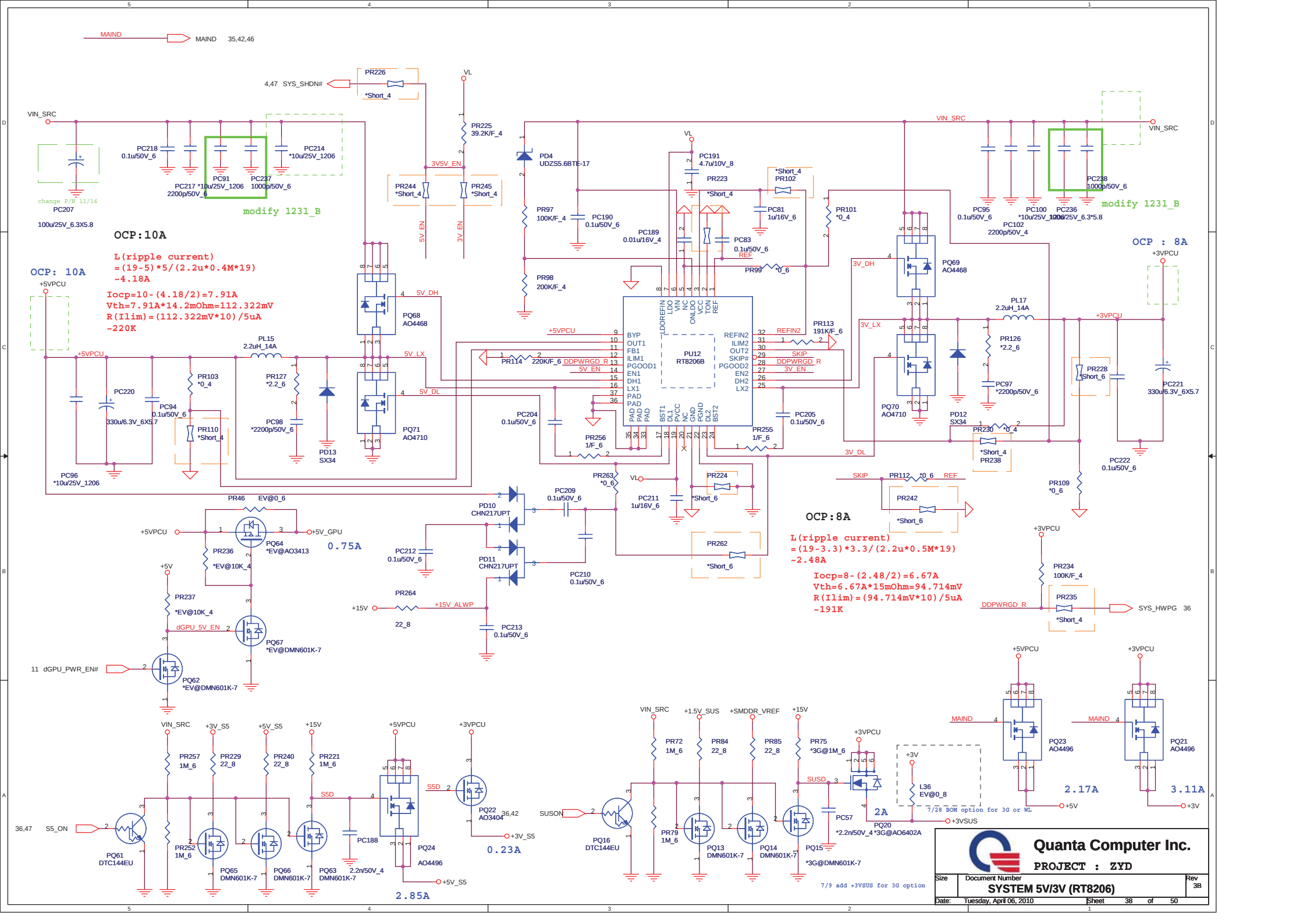
PROJECT : ZYD

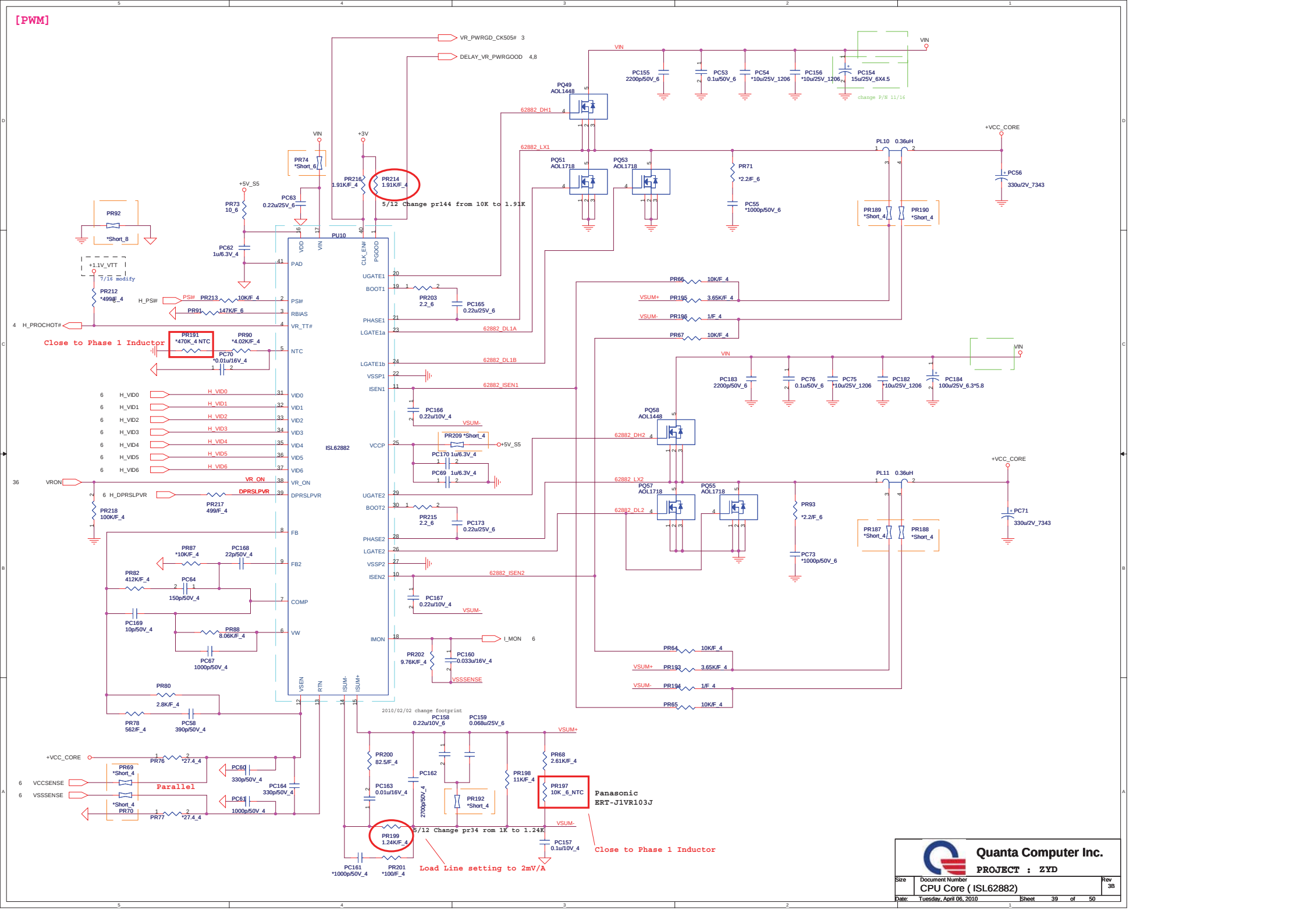
Size	Document Number	Rev
	WPCE781 & FLASH	3B

Date: Tuesday, April 06, 2010 Sheet 36 of 50

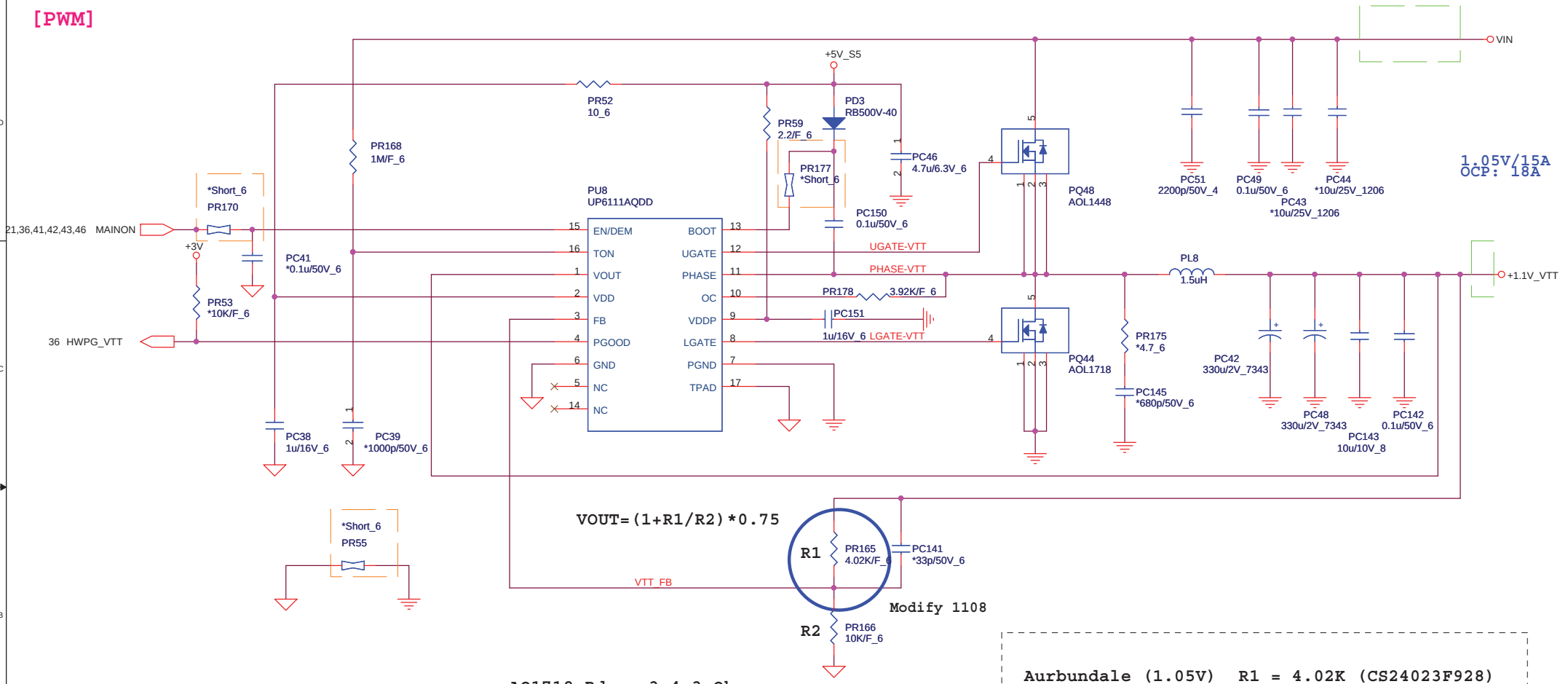


Quanta Computer Inc.		
PROJECT : ZYD		
Size	Document Number: CHARGER (ISL88731)	Rev: 3B
Date: Tuesday, April 06, 2010	Sheet 37 of 50	


MAIND
MAIND 35,42,46
4,47 SYS_SHDN#
PR226
*Short_4
VL
PR225
39.2K/F_4
3V5V_EN
PR244
*Short_4
PR245
*Short_4
5V_EN
3V_EN
VIN_SRC
PC218
0.1u/50V_6
PC91
PC237
1000p/50V_6
PC217 *10u/25V_1206
2200p/50V_6
PC214
*10u/25V_1206
change P/N 11/16
PC207
100u/25V_6.3X5.8
modify 1231_B
OCP:10A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*14.2mOhm=112.322mV
R(Ilim)=(112.322mV*10)/5uA
~220K
OCP: 10A
+5VPCU
PL15
2.2uH_14A
PR103
*0_4
PC220
330u/6.3V_6X5.7
PC94
0.1u/50V_6
PR110
*Short_4
PC96
*10u/25V_1206
PR127
*2.2_6
PC98
*2200p/50V_6
PD13
SX34
5V_DH
5V_LX
5V_DL
PQ68
AO4468
PQ71
AO4710
PD4
UDZS5.6BTE-17
PR97
100K/F_4
PC190
0.1u/50V_6
PR98
200K/F_4
PC189
0.01u/16V_4
PC191
4.7u/10V_8
PR223
*Short_4
PC81
1u/16V_6
PC83
0.1u/50V_6
REF
PR99
*0_6
PR102
*Short_4
PR101
*0_4
PU12
RT8206B
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
PAD
PAD
PAD
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
BST1
DL1
PVCC
NC
GND
PSN
DL2
BST2
PR114
220K/F_6
DDPWRGD_R
PR113
191K/F_6
REFIN2
SKIP
3V_EN
PC204
0.1u/50V_6
PC205
0.1u/50V_6
PR256
1/F_6
PR255
1/F_6
PR263
*0_6
PC211
1u/16V_6
PR224
*Short_6
PR262
*Short_6
PC209
0.1u/50V_6
PD10
CHN217UPT
PD11
CHN217UPT
PC212
0.1u/50V_6
PC210
0.1u/50V_6
PR264
22_8
+15V_ALWP
PC213
0.1u/50V_6
PR46
EV@0_6
PQ64
*EV@AO3413
0.75A
PR236
*EV@10K_4
PR237
*EV@10K_4
dGPU_5V_EN
PQ67
*EV@DMN601K-7
11 dGPU_PWR_EN#
PQ62
*EV@DMN601K-7
VIN_SRC
PC95
0.1u/50V_6
PC100
*10u/25V_1206
PC102
2200p/50V_4
PC236
1000p/50V_6
PC238
1000p/50V_6
modify 1231_B
OCP : 8A
+3VPCU
3V_DH
3V_LX
PQ69
AO4468
PQ70
AO4710
PL17
2.2uH_14A
PR126
*2.2_6
PC97
*2200p/50V_6
PD12
SX34
PR230
*0_4
*Short_4
PR238
PR228
*Short_6
PC221
330u/6.3V_6X5.7
PC222
0.1u/50V_6
PR109
*0_6
3V_DL
SKIP
PR112
*0_6
REF
PR242
*Short_6
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
PR234
100K/F_4
PR235
*Short_4
DDPWRGD_R
SYS_HWPG 36
+5V
+3V_S5
+5V_S5
+15V
+5VPCU
+3VPCU
PR257
1M_6
PR229
22_8
PR240
22_8
PR221
1M_6
S5D
PC188
PQ24
AO4496
PQ22
AO3404
36,42
+3V_S5
0.23A
+5V_S5
2.85A
36,47 S5_ON
PQ61
DTC144EU
PR252
1M_6
PQ65
DMN601K-7
PQ66
DMN601K-7
PQ63
DMN601K-7
2.2n/50V_4
VIN_SRC
+1.5V_SUS
+SMDDR_VREF
+15V
PR72
1M_6
PR84
22_8
PR85
22_8
PR75
*3G@1M_6
SUSD
SUSON
PQ16
DTC144EU
PR79
1M_6
PQ13
DMN601K-7
PQ14
DMN601K-7
PQ15
*3G@DMN601K-7
PC57
*2.2n/50V_4
2A
PQ20
*3G@AO6402A
+3V
L36
EV@0_8
7/28 BOM option for 3G or WL
+3VSUS
7/9 add +3VSUS for 3G option
MAIND
PQ23
AO4496
2.17A
+5V
PQ21
AO4496
3.11A
+3V
Quanta Computer Inc.
PROJECT : ZYD
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev
3B
Date: Tuesday, April 06, 2010
Sheet 38 of 50


[PWM]
VR_PWRGD_CK505# 3
DELAY_VR_PWRGOOD 4,8
ISL62882
PU10
5/12 Change pr144 from 10K to 1.91K
5/12 Change pr34 rom 1K to 1.24K
Close to Phase 1 Inductor
Load Line setting to 2mV/A
Parallel
Panasonic
ERT-J1VR103J
2010/02/02 change footprint
change P/N 11/16
7/16 modify
Quanta Computer Inc.
PROJECT : ZYD
CPU Core (ISL62882)
Tuesday, April 06, 2010
Sheet 39 of 50

[PWM]



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

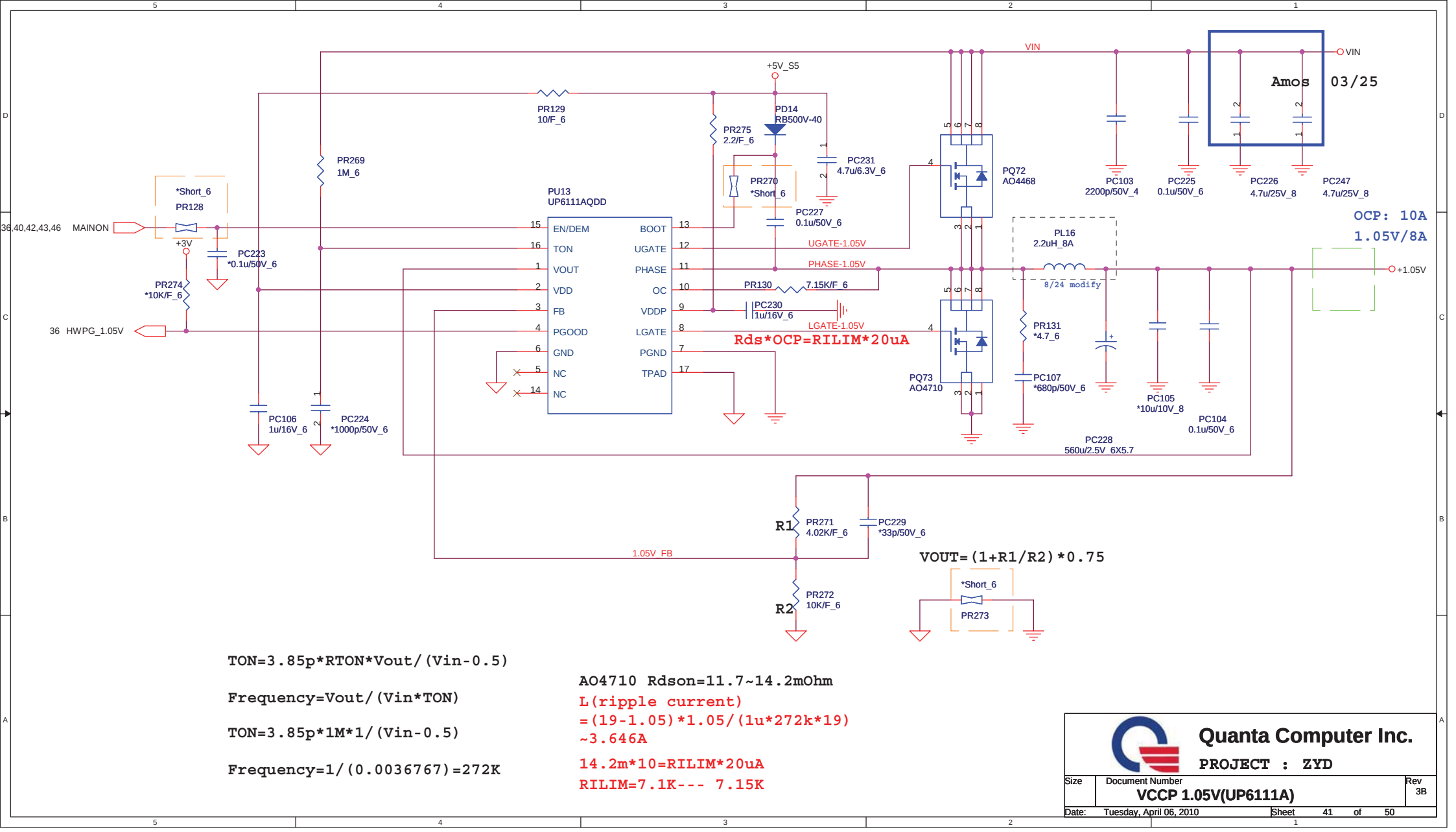
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.64A

4.3m*18=RILIM*20uA
RILIM=3.87K --- 3.92K

Aurbundale (1.05V) R1 = 4.02K (CS24023F928)
Clarksfield(1.1V) R1 = 4.75K (CS24753F919)

Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	+VTT (UP6111A)	3B
Date: Tuesday, April 06, 2010	Sheet 40 of 50	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

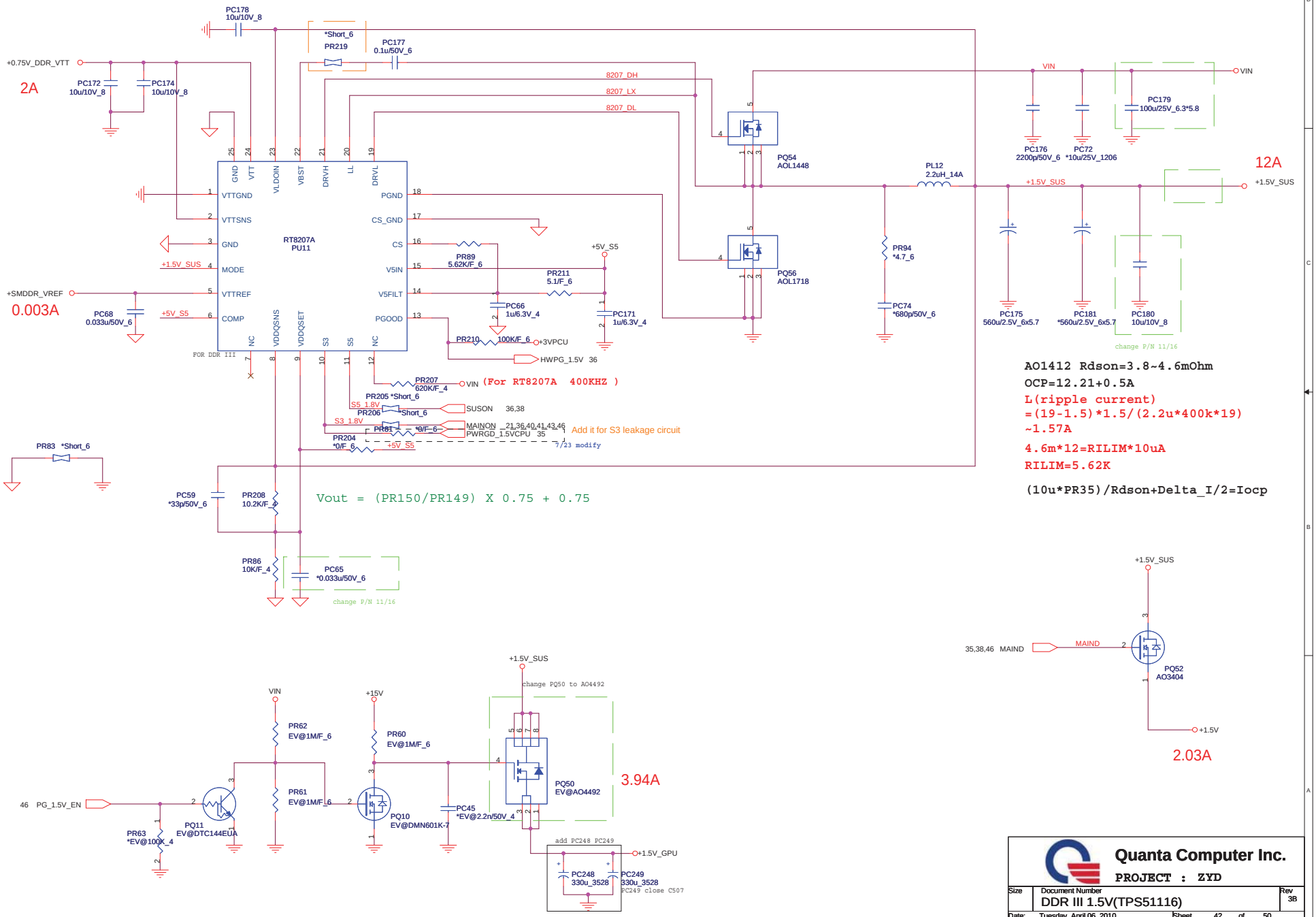
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K

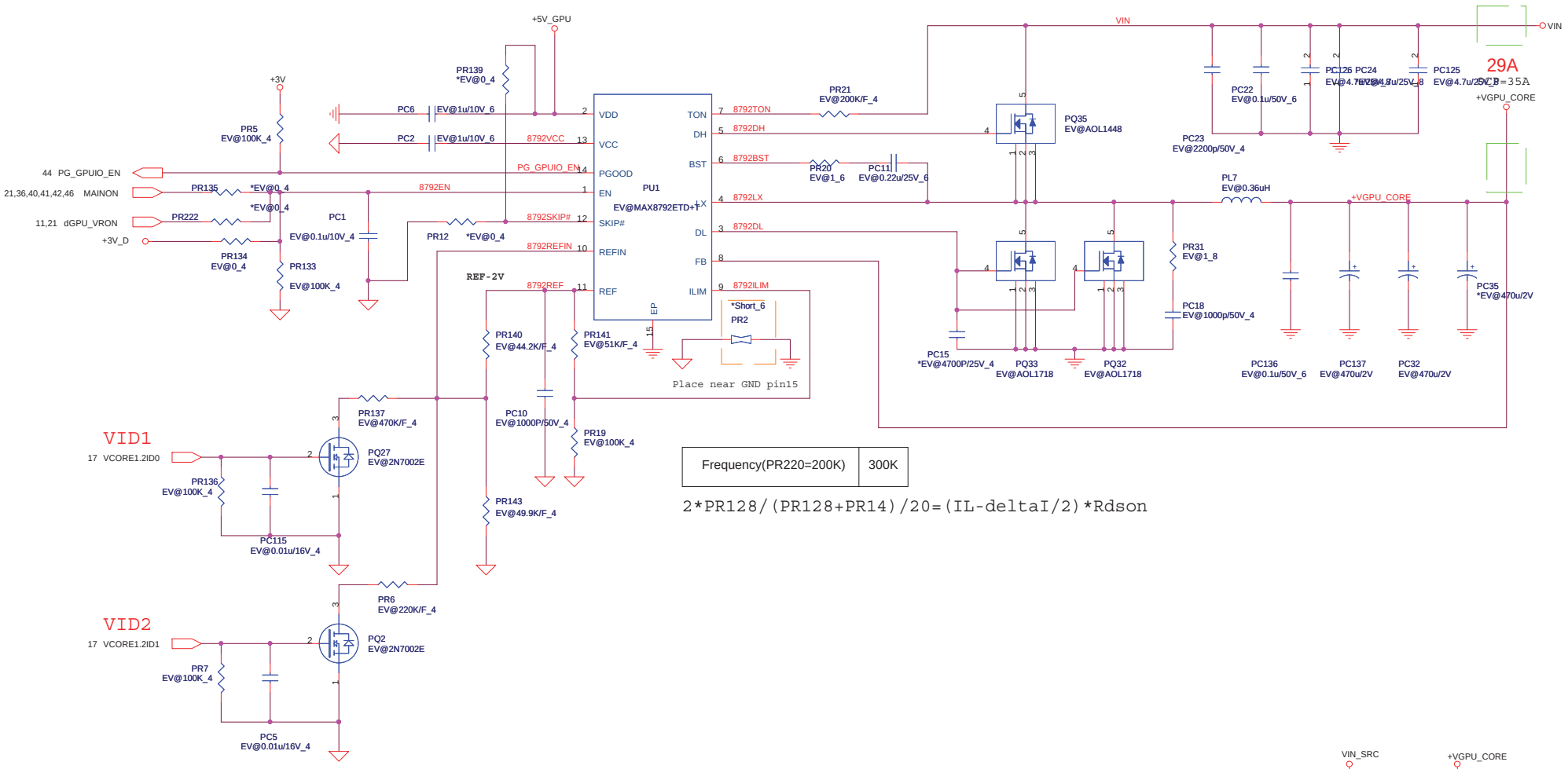
Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	VCCP 1.05V(UP6111A)	3B
Date: Tuesday, April 06, 2010	Sheet 41 of 50	



Quanta Computer Inc.		
PROJECT : ZYD		
Size	Document Number: DDR III 1.5V(TPS51116)	Rev: 3B
Date: Tuesday, April 06, 2010	Sheet 42 of 50	



Madison VID Table

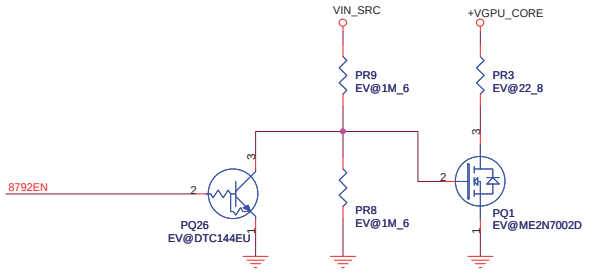
VID1	VID2		+VCC_GFX_CORE
VCORE1.2ID0	VCORE1.2ID1		
LOW (0)	LOW (0)		1.05V
HIGH (1)	LOW (0)		1.0V
LOW (0)	HIGH (1)		0.95V
HIGH (1)	HIGH (1)		0.90V

PR140 = 44.2K
PR143 = 49.9K
PR137 = 470K
PR6= 220K

PARK XT VID Table

VID1	VID2		+VCC_GFX_CORE
VCORE1.2ID0	VCORE1.2ID1		
LOW (0)	LOW (0)		1.12V
HIGH (1)	LOW (0)		1.05V
LOW (0)	HIGH (1)		0.95V
HIGH (1)	HIGH (1)		0.90V

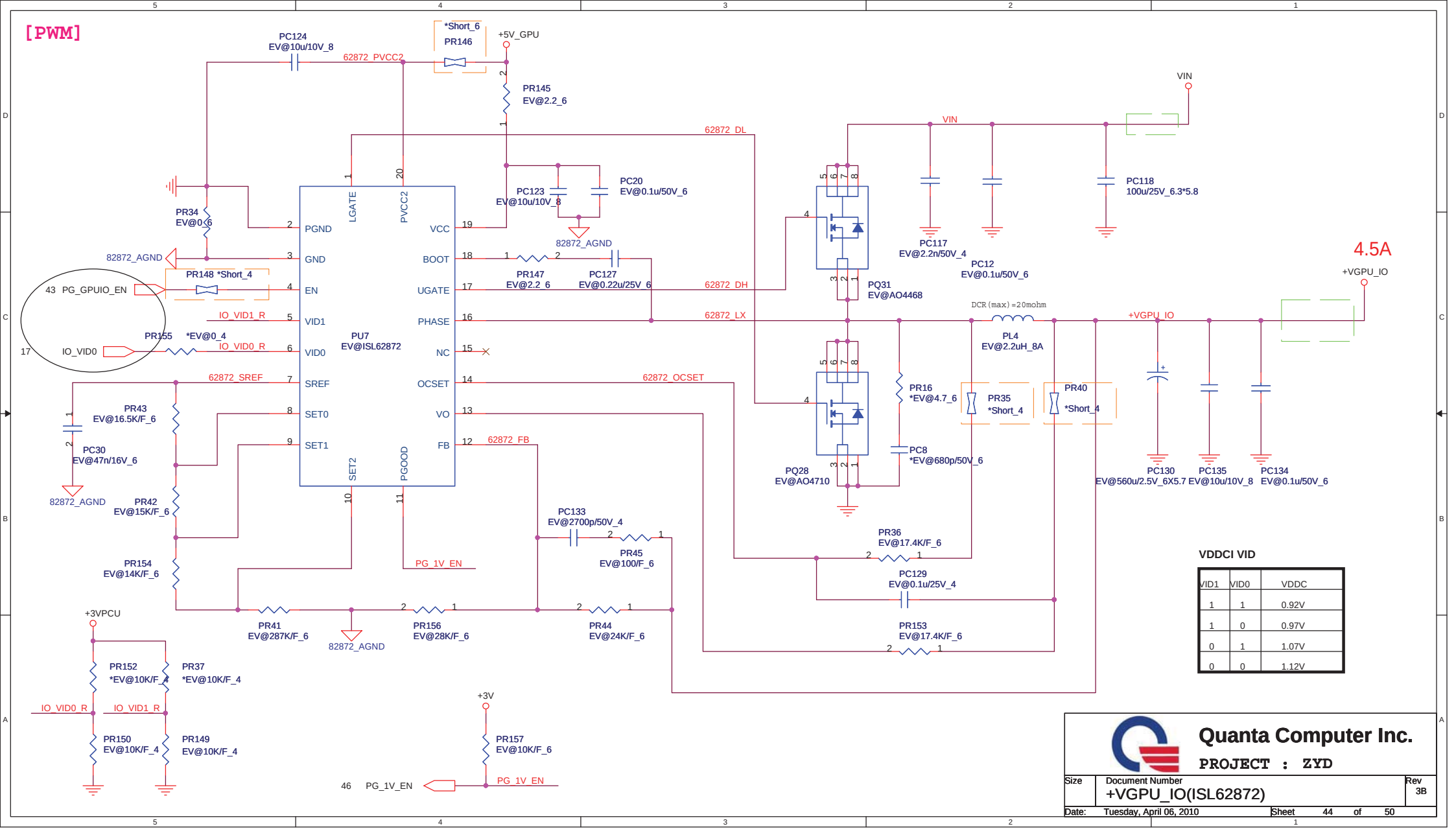
PR140= 39.2K CS33922FB15
PR143 = 49.9K
PR137 = 332K CS43322FB15
PR6 = 130K CS41302FB00



Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	GPU CORE(MAX8792)	3B

Date: Tuesday, April 06, 2010 Sheet 43 of 50



VDDCI VID

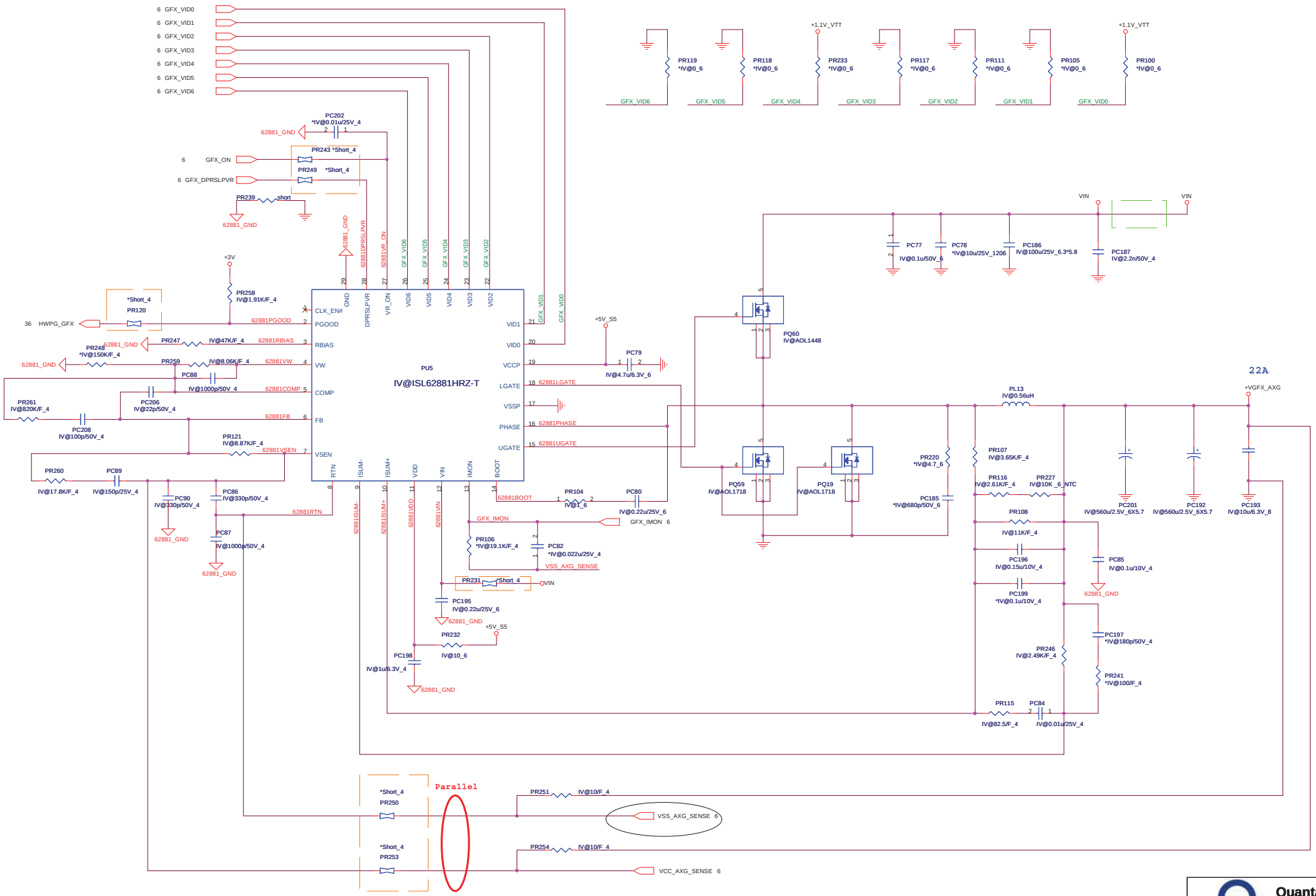
VID1	VID0	VDDC
1	1	0.92V
1	0	0.97V
0	1	1.07V
0	0	1.12V

Quanta Computer Inc.

PROJECT : ZYD

Size	Document Number	Rev
	+VGPU_IO(ISL62872)	3B
Date: Tuesday, April 06, 2010	Sheet 44 of 50	

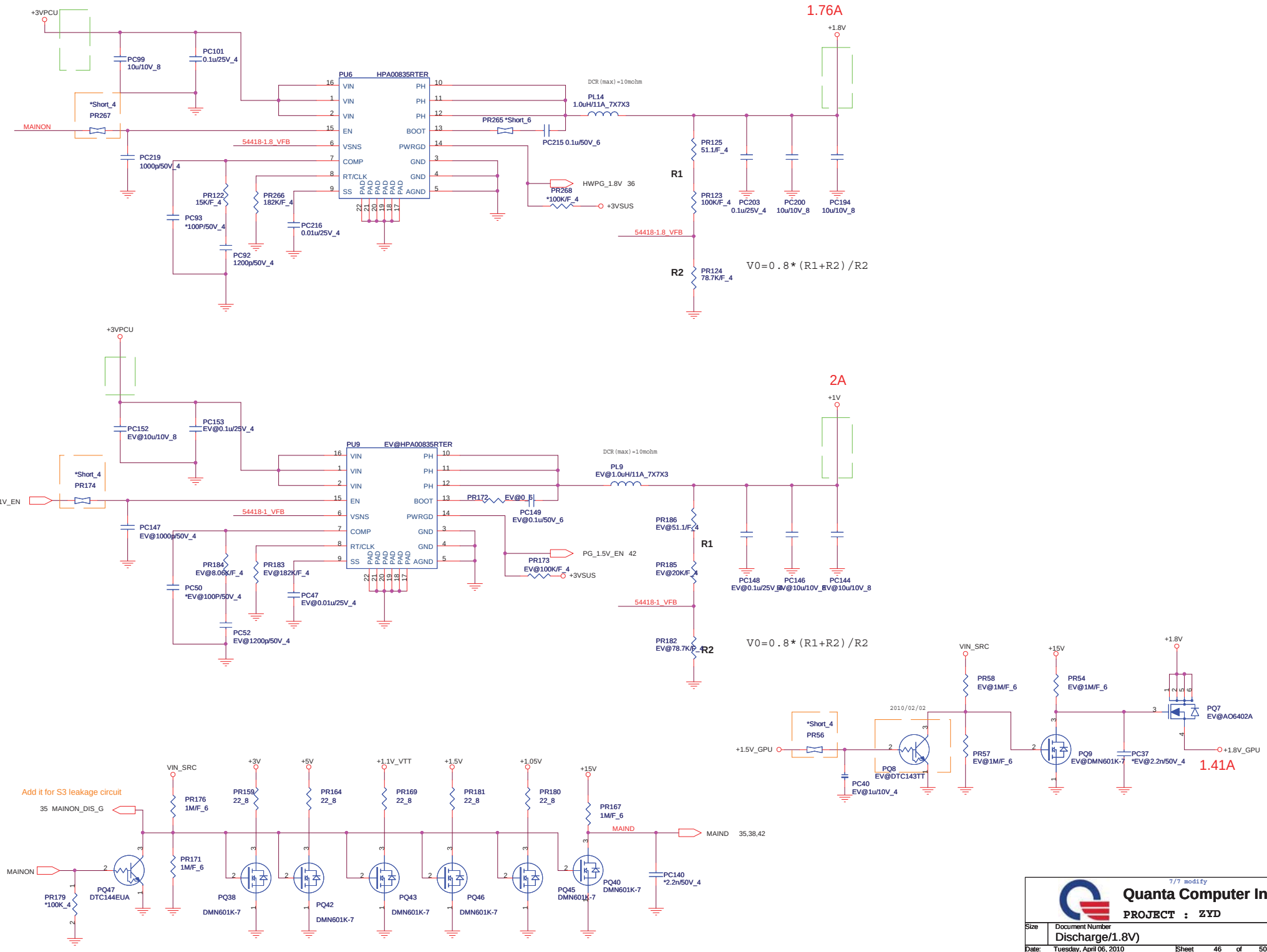
Int_VGA [PWM]



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZYD

Size	Document Number	Rev
	+VGFX_AXG (ISL62881)	3B
Date: Tuesday, April 06, 2010	Sheet 45 of 50	


1.76A
+3VPCU
PC99 10u/10V_8
PC101 0.1u/25V_4
*Short_4 PR267
MAINON
PU6 HPA00835RTER
VIN
PH
EN
BOOT
VSNS
PWRGD
COMP
GND
RT/CLK
SS
AGND
PAD
54418-1.8_VFB
PC219 1000p/50V_4
PR122 15K/F_4
PR266 182K/F_4
PC93 *100P/50V_4
PC92 1200p/50V_4
PC216 0.01u/25V_4
PR265 *Short_6
PC215 0.1u/50V_6
DCR(max)=10mohm
PL14 1.0uH/11A_7X7X3
+1.8V
PR125 51.1/F_4
PR123 100K/F_4
R1
R2
PR124 78.7K/F_4
PC203 0.1u/25V_4
PC200 10u/10V_8
PC194 10u/10V_8
PR268 *100K/F_4
HWPG_1.8V 36
+3VSUS
V0=0.8*(R1+R2)/R2
2A
+3VPCU
PC152 EV@10u/10V_8
PC153 EV@0.1u/25V_4
*Short_4 PR174
44 PG_1V_EN
PU9 EV@HPA00835RTER
54418-1_VFB
PC147 EV@1000p/50V_4
PR184 EV@8.06K/F_4
PR183 EV@182K/F_4
PC50 *EV@100P/50V_4
PC52 EV@1200p/50V_4
PC47 EV@0.01u/25V_4
PR172 EV@0_8
PC149 EV@0.1u/50V_6
PR173 EV@100K/F_4
PG_1.5V_EN 42
+3VSUS
DCR(max)=10mohm
PL9 EV@1.0uH/11A_7X7X3
+1V
PR186 EV@51.1/F_4
PR185 EV@20K/F_4
R1
R2
PR182 EV@78.7K/F_4
PC148 EV@0.1u/25V_4
PC146 EV@10u/10V_8
PC144 EV@10u/10V_8
V0=0.8*(R1+R2)/R2
VIN_SRC
+15V
+1.8V
PR58 EV@1M/F_6
PR54 EV@1M/F_6
2010/02/02
*Short_4 PR56
+1.5V_GPU
PQ8 EV@DTC143TT
PC40 EV@1u/10V_4
PR57 EV@1M/F_6
PQ9 EV@DMN601K-7
PC37 *EV@2.2n/50V_4
PQ7 EV@AO6402A
+1.8V_GPU
1.41A
Add it for S3 leakage circuit
+3V
+5V
+1.1V_VTT
+1.5V
+1.05V
35 MAINON_DIS_G
PR176 1M/F_6
PR159 22_8
PR164 22_8
PR169 22_8
PR181 22_8
PR180 22_8
PR167 1M/F_6
MAIND
MAIND 35,38,42
21,36,40,41,42,43 MAINON
PR171 1M/F_6
PR179 *100K_4
PQ47 DTC144EUA
PQ38 DMN601K-7
PQ42 DMN601K-7
PQ43 DMN601K-7
PQ46 DMN601K-7
PQ45 DMN601K-7
PQ40 DMN601K-7
PC140 *2.2n/50V_4
7/7 modify
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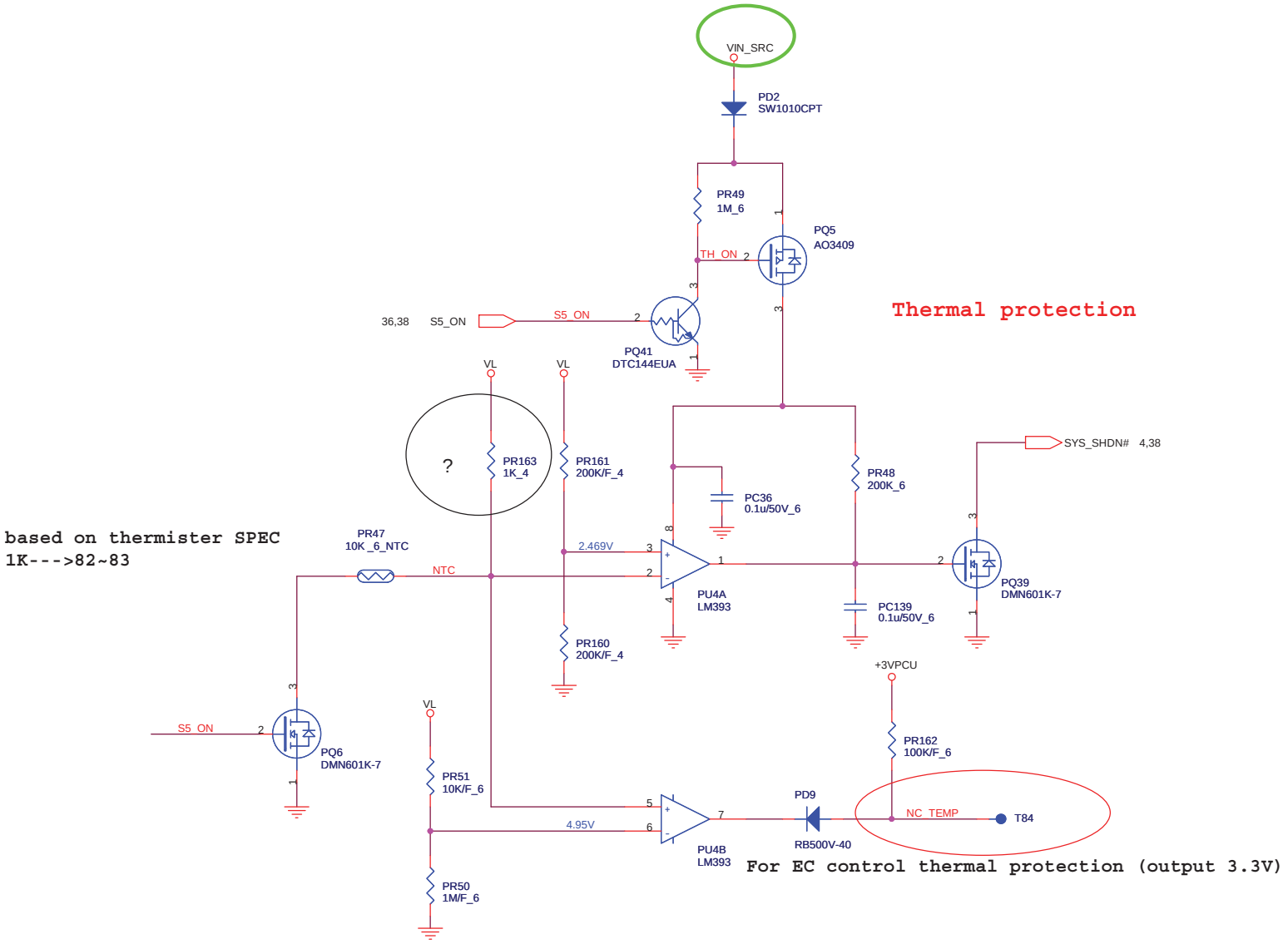

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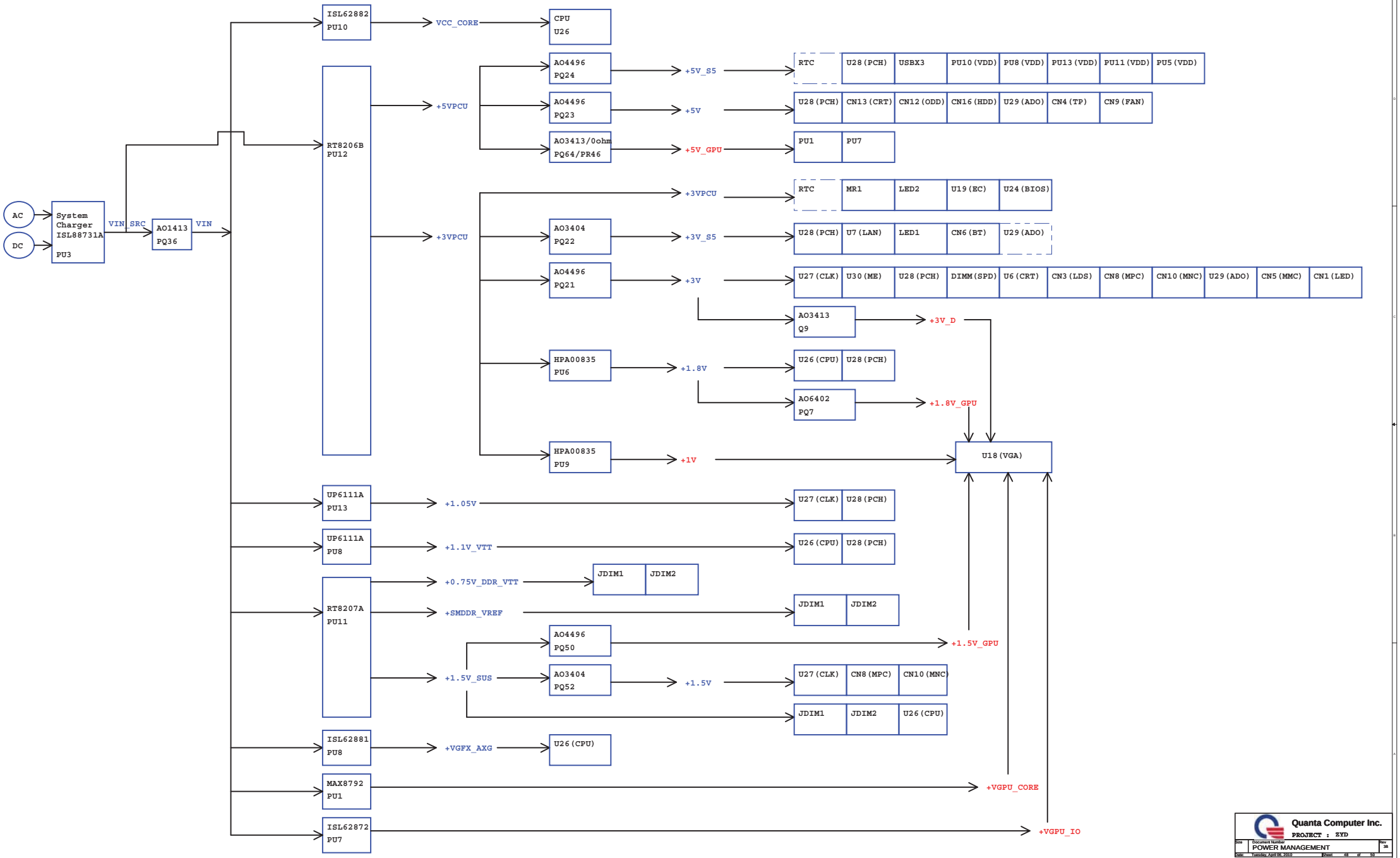

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Model	REV	CHANGE LIST	MODEL	ZYD	
				FROM	To
ZYD MB	1A	20091028 Page 30, Move the resisters and common chokes from M/B to daughter board		X	1A
		20091028 Page 30, Move the R1027 and R1059 to daughter board and change to 0402 (place closer).		X	1A
		20091028 Page 30, Move USB Power switch to daughter board		X	1A
		20091028 Page 30, Change card reader&USB board CONN P/N to DFFC20FR255		X	1A
		20091028 Page 26, Delete R203 and R171 to leave RJ45 chasiss contact to GND directly		X	1A
		20091028 Page 31, Add net name susled#_R, Pwrled#_R,BATLED0#_R, BATLED1#_R,RFLED#_R,RFLED2#_R		X	1A
		20091028 Page 35, Add SW1 for debug purpose		X	1A
		20091028 Page 33, update Hole footprints		X	1A
		20091029 Page 41, Change PR199, PR200 P/N from CS00003J951 to CS00003F916		X	1A
		20091102 Page 24, 29, Add Mic_GND for internal analog MIC		X	1A
		20091102 Page 27, Delete C204, C208, C558, R411, R385, R373, RP3, Q27, Q26. and change C578 from 0.47u to 4.7u		X	1A
		20091102 Page 10, Stuff R1001, R1002, R503		X	1A
		20091103 Page 33, Delete Hole4, Hole5, Hole8, Hole18		X	1A
		20091104 Page 33, update power schematic		X	1A
		20091104 Page 30, swap L38,L39,L58 USB nets for layout request.		X	1A
		20091108 Page 45, delete net name MAINON_G		X	1A
		20091108 Page 39, Change PR151 P/N from CS24703F908 to CS24023F928 for support Arrandale only		X	1A
		20091108 Page 33, Delete Hole36		X	1A
		20091110 Page 31, Move Wi-Fi LED to PB		X	1A
		20091111 Page 39, Delete Pl8 and Change PL9 footprint and value(1.5uH footprint:CHOKE-ETQP4LR36WFC-NB4)		X	1A
		20091111 Page 41, Stuff +1.5V_GPU power source for EV# only		X	1A
		20091111 Page 37, reserve PR275 for GPU power		X	1A
		20091112 Page 18, Follow ATI suggestion to modify R419 from 680ohm to 51 ohm.		X	1A
		20091112 Page 27, Remove LPC from Mini PCIE port CN24		X	1A
		20091112 Page 37,45, unstuff +3V_SUS components		X	1A
		20091113 Page 27, Two Wi-Fi LED share one net RF_LED#		X	1A
		20091113 Page 31, Delete Q21,Q23, R347		X	1A
		20091113 Page 29, Reserve three more resistors R373, R368, R385 for ESD solution		X	1A
		20091116 Page 34, unstuff PR95, PR96, PQ17, PQ15		X	1A
		20091116 Page 24, Change C650 from 0.22u/6.3V_4 to 0.22u/10V_4		X	1A
		20091116 Page 32, Change C399 from 1U/6.3V_4 to 1u/10V_4		X	1A
		20091116 Page 7, unstuff R159		X	1A
		20091116 Page 11, stuff R592 for DIS and stuff R595 for UMA		X	1A
		20091116 Page 11, Reserve pull low for unused pin dGPU_VRON_R		X	1A
		20091116 Page 8, Delete R414		X	1A
		20091116 Page 25, Delete R162		X	1A
		20091116 Page 36-45, PC14 un-mount; PC207 change P/N; PC154 change P/N and value.; PC155 un-mount; PC180 change P/N; PC119 change P/N; PC118 change P/N		X	1A
	2A	20091119 Page 36, Modify Bat CONN P/N and footprint		1A	2A
		20091119 Page 29, Modify Speaker CN7 P/N from DFHD04MR779 to DFHD04MR057		1A	2A
		20091120 Page 8~13, Modify PCH P/N from AJ0QMGS0T05 to AJSLGZS0T07		1A	2A
		20091124 Page 27, Short Pin42 and Pin44 of CN8 and CN10 to support Intel WiMAX/WiFi combo module		1A	2A
		20091128 Page 37, stuff L36 for discrete sku		1A	2A
		20091128 Page 9, change U30(ME ROM) P/N from AKE391P0N00 to AKE38ZP0N01		1A	2A
		20091202 Page 3, reserve 1U for CLK GEN +1.5V power		1A	2A
		20091203 Page 27, Stuff Q26 and Q28; unstuff R401 and R447; and add LPC bus to CN24 for debug purpose		1A	2A
		20091209 Page 42, add VID table for Park XT		1A	2A
		20091209 Page 3, change R257 from 0ohm to 33ohm		1A	2A
		20091209 Page 3,17,18 follow AMD suggestion to stuff R257, R101, R407,R409 amd remove R36 to fix AMD pre-production silicon bug		1A	2A
		20091214 Page 9, change R317 to a JP and stuff R322		1A	2A
		20091214 Page 32, change CN6 from DFHD05MRD98 to DFWF05MR027		1A	2A
		20091221 Page 29, change R533 from CS03923F916 to CS33922FB15		1A	2A
		20091223 Page 10, change R202, R203, R540, R566, R547 to short pad		1A	2A
		20091223 Page 36, change DC jack P/N to DFHS04FR741		1A	2A
		20091223 Page 32, change CN6 P/N to DFWF05MR012		1A	2A
		20091225 Page 50, change CN19 P/N to DFHD19MR083		1A	2A
		20091230 Page 12, Add C786 for CRT flicker issue		1A	2A
		20091230 Page 27, change transformer footprint to TRF-10-1-24P-SMT		1A	2A
		20091230 Page 17, change VGFU_CORE VID control pin		1A	2A
		20091230 Page 28, Exchange P/N for cn8 and cn10		1A	2A
		20091230 Page 28, Move controller link from CN10 to CN8		1A	2A
	3A	20100129 Page 32, remove power LED MOS Q25		2A	3A
		20100130 Page 18, Remove AMD option 2 workaround for Madison and Park; and change R36 from 1K to 10K		2A	3A
		20100130 Page 28, Change Mini card footprint to MIPCI-800055FB052GX-52P-LDV-NB4		2A	3A
		20100201 Page 32, restore power LED MOS Q25		2A	3A
		20100201 Page 25, Change Q33,Q34 to ESD protection part		2A	3A
		20100222 Page 24, Reserve C787 and C788 for CRT flicker issue		2A	3A
		20100222 Page 36, Remove SW1		2A	3A
		20100222 Page 12, Add C789 for VCCADAC		2A	3A
		20100222 Page 17, Reserve 10U*2 caps for +1.8V_GPU		2A	3A
		20100222 Page 30, Add short Pad R635,R636,R637,R638,R640 for EMI		2A	3A
		20100222 Page 24, unstuff L13 and stuff R89 and R90		2A	3A

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Model	REV	CHANGE LIST
ZYD MB	3B	20100322 Page 32, delete Q25 20100322 Page 44,45 modify PU5,PU7 footprint 20100324 Page 44,45 change PC184,PC179,PC207,PC125,PC236,PC118,PC186 P/N to CC71004MZ04 20100324 Page 43 change PC126, PC24, PC125 to CH5474KEA06(4.7uF 25V 0805) 20100324 Page 30 change R298,R314 to 39ohm 20100325 reserved EMI chock lacation for USB 1/3/11/12/8 20100325 Page 41 change PC226 to 0805 4.7uF/25V,and add PC247 ,BOM stuff. 20100325 Page 30 change R223,R347,C444,R252, R590 and R306 to short pad.

MODEL	ZYD	
	FROM	To
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B

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	PART NUMBER:		DRAWING BY:		REVISON:	3B