CT8 BLOCK DIAGRAM

CLAW HAMMER / RS480 / SB400

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

DDR-SODIMM1

DDR-SODIMM2

DDR 266,333,400MHz

CPU CLAW HAMMER

754 Pins (uPGA)

CPU THERMAL SENSOR GMT-781

14.318MHz

CPUCLK, CPUCLK#

CLOCK GEN

CY28RS480/ ICS951412

SBLINKCLK, SBLINKCLK#

NBSRCCLK, NBSRCCLK#

HTREFCLK

OSC14M

HyperThansport I/O BUS Link 16x16

CABLE DOCK

Daughter Board

TV, USB, BLUE TOOTH

Power Board

CRT port — R.G,B

LCD Panel — LVDS X1

S-VIDEO — TV-OUT

NORTH BRIDGE RS480M

705 BGA

INTEGRADED VGA FUNCTION

Based on Redeon 9600

A-LINK 2X PCI-E

32.768KHz

USB PORT 0, 1, 2 — USB 2.0

1st IDE - HDD — ATA 66/100/133

2nd IDE - CDROM — ATA 66/100/133

SB400

564 BGA

NBSRCCLK, NBSRCCLK#

33MHZ, 3.3V PCI

PCLK_7411

PCLK_MINI

PCLK_LAN

AC97

PWRCLKP

PWRCLKN

DIB_DATAN

DIB_DATAP

AC97

CX20468-31

MBAMC20493-010

LAN

Realtek

8100CL

MINI-PCI

24.576MHz

48MHz

CARDBUS / IEEE 1394 CONTROLLER/CF

TI 7411

24.576MHz

25MHz

32.768KHz

PCLK_591

3.3V LPC, 33MHz

PC97551

TQFP 176

FAN

Touchpad

Keyboard

FLASH

SMARTDAA MODEM,

WIRE

RJ11 JACK

AMP

TPA0312

JACK

HEADPHONE,

2ND HEADPHONE,

MIC

RJ45 JACK

5 IN 1

CARD READER SD/MMC, SM, MS, XD

CARDBUS SLOT X1

1394 CONN

SYSTEM POWER MAX1845 (1.2V/NB_CORE/1.25V)

CPU CORE MAX1544 POWER 1.2V

SYSTEM MAX1999 POWER(3/5V)

SYSTEM POWER MAX1845 (2.5VSUS/1.8VSUS)

BATT CHARGER MAX1722

DISCHARGE

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
GBIT ETHERNET	AD16	2	C
MINIPCI SLOT	AD18	1	E,F
CardBus/1394	AD25	4	B,D,G

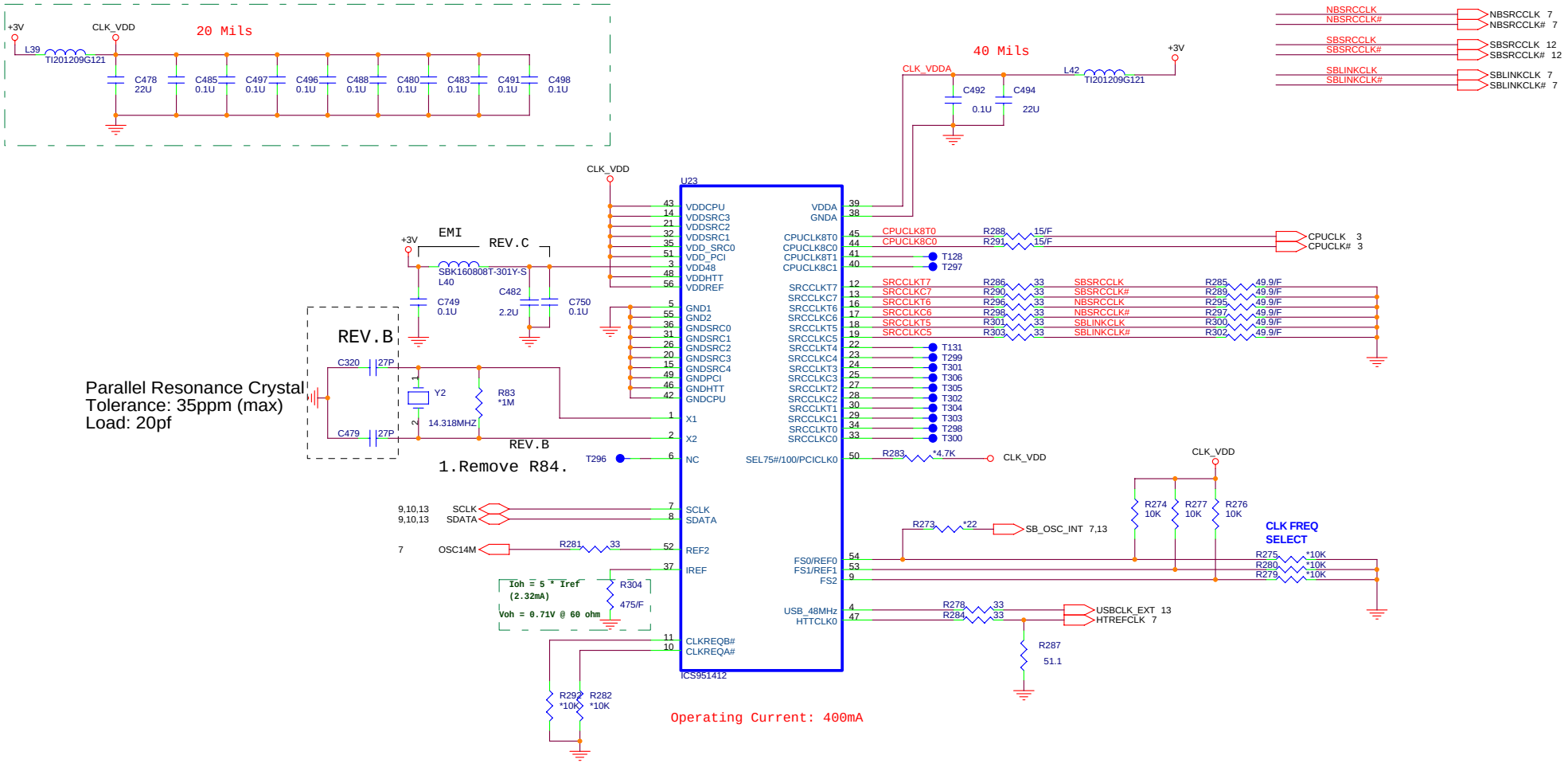
PROJECT : CT8

Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Thursday, April 14, 2005 Sheet 1 of 42

CLK



Layout Note:

1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS CKG. AS POSSIBLE

2- ROUTE ALL CPUCLK/#, NBSRCCLK/#, SBSRCCLK/#, SBLINKCLK/# AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO CKG. POWER PIN

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EXT CLOCK GENERATOR	3A

Date: Thursday, April 14, 2005 Sheet 2 of 42

CPU

20 Mils width to pin
100 Mils width to capacitor
250 Mils width to PWM

Near Socket754

STUFF WHEN CONFIGURED AS 16-BIT LINK

add c154,c283,c284,c285 4.7u
c9,c277 100u change to 220u

REV.B

50 Mils, routing as 15 mils width if the distance from bead to cpu pin less than 1000 mils.

Output current(Max):
300mA

H/W MONITOR

MAX6657/GMT-781

1.Remove R386,Q33, connect U18 pin 6 to TEMP_ALARM#.

Ra

Rb

2. Change C311 from 10u to 100u, remove C304.

Vout=1.25(1+Ra/Rb)
Ra=Rb(Vout/1.25-1)

PROJECT : CT8	
Quanta Computer Inc.	
Size: Custom	Document Number: CPU H.T/CTL I/F
Rev: 3A	
Date: Thursday, April 14, 2005	Sheet 3 of 42

CPU

U22E
AMD K8
GROUND

U22B
AMD K8
MEMORY

U22D
AMD K8
POWER

20 mils width to CPU pins.

LAYOUT: Place close to CPU.

60 mils

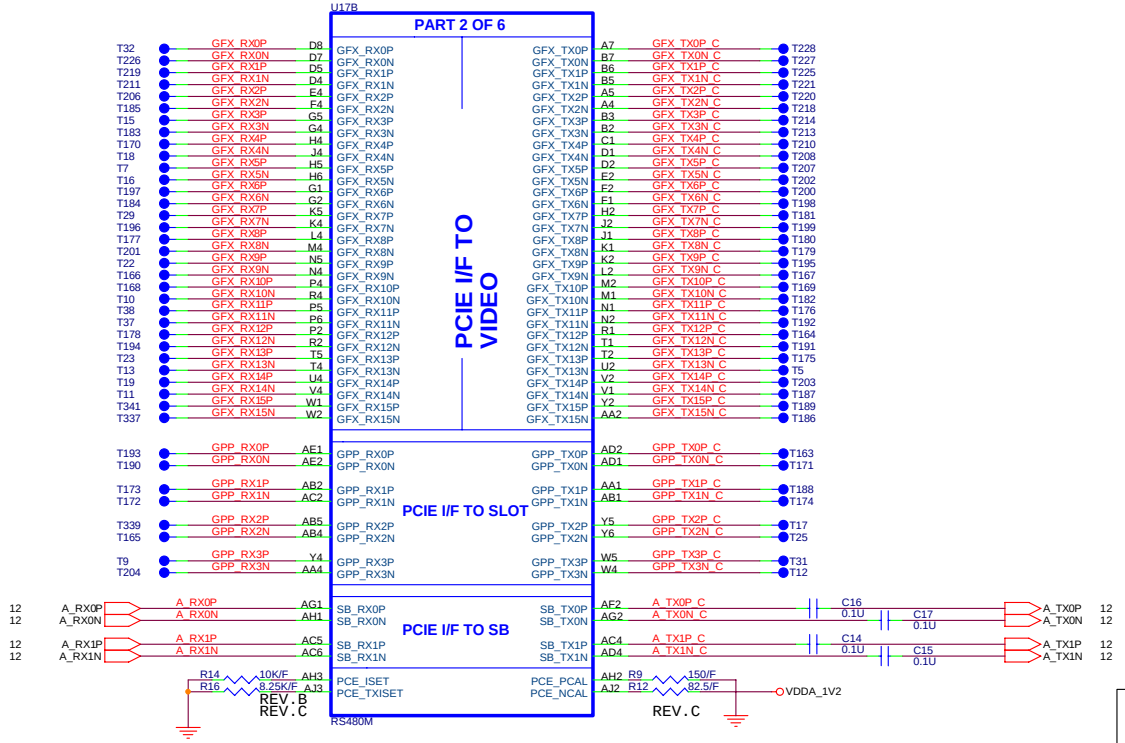
W/S 15/20 mils

REV . B

PROJECT : CT8	
Quanta Computer Inc.	
Size: Custom	Document Number: CPU DDR/POWER I/F
Rev: 2A	
Date: Thursday, April 14, 2005	Sheet 4 of 42

CLG

Link 0 Is Clawhammer <--> RS480



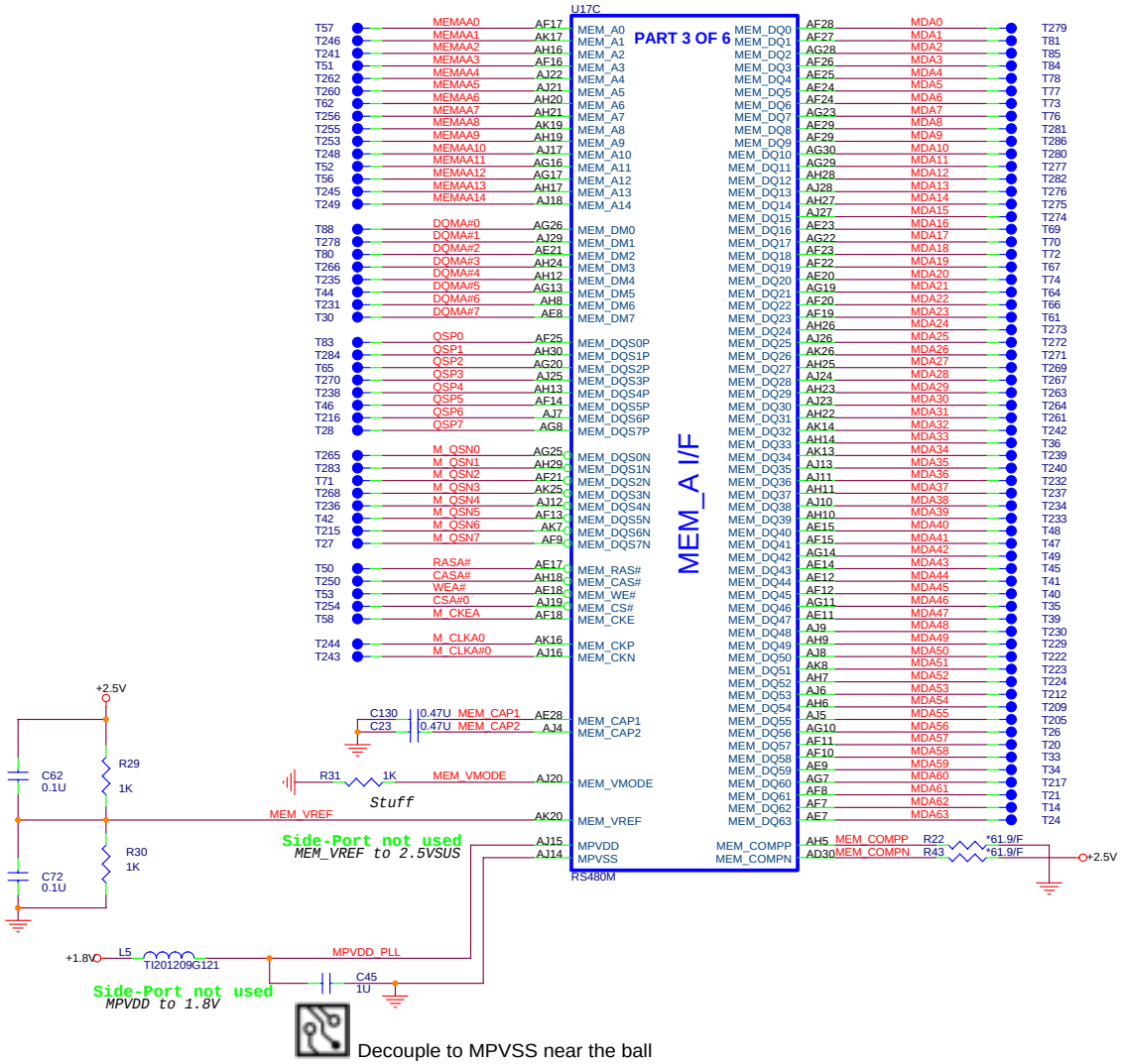
PROJECT : CT8

Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS480M-HT A-LINK0	3A

Date: Thursday, April 14, 2005 Sheet 5 of 42

CLG



PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS480M-SIDE PORT MEM I/F	1A

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CLG

EMI
REV.B

EMI
REV.B

REV.B
REV.C
EMI
ESD
REV.D

REV.C

U17D

PART 4 OF 6

RS480M

CRT/TVOUT

LVDS

PLL PWR

PM

CLOCKs

MIS.

AVDD	DAC VDD (2.5V)
AVDDDI	DIGITAL VDD (1.8V)
AVDDQ	DAC2 BANDGAP REF (1.8V)
PLLVDD	PLL VDD (1.8V)
HTPVDD	HT PLL VDD (1.8V)

PUT AVDD, AVDDDI, AVDDQ,PLVDD,HTPVDD DECOUPLING CAPS ON THEBOTTOM, CLOSE TO BALLS

ROUTING H_THRMDA AND HW_AGND AS DIFFERENTIAL PAIR

DO NOT SHARE GND VIA ON JOINT

DO NOT SHARE GND VIA ON JOINT

REV.B DEL Y1 AND U3 CIRCUIT.

LOAD_ROM#:LOAD ROM STRAP ENABLE strap

High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE

SPMEM_EN#:SIDE PORT MEMORY ENABLE strap

NC, SIDE PORT MEMORY DISABLE
Low, SIDE PORT MEMORY ENABLE

PROJECT : CT8
Quanta Computer Inc.

Size: Custom	Document Number: RS480M-VIDEO & CLKGEN	Rev: 3A
Date: Thursday, April 14, 2005	Sheet 7 of 42	

CLG

NB RS480 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR,VDDRCK	ON	ON	ON	ON	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

U17F RS480M

PAR 6 OF 6

GROUND

VSSA22 VSSA59 VSS30 VSS89

REV.B

VDDA_1V2 L15 FBMJ2125HM330-T

L15,L55 TI201209G121
CHANGE TO
FBMJ2125HM330-T

VDDHT 120 mils

U17E PART 5 OF 6 POWER RS480M

C152 22U, C105 0.1U, C84 0.1U, C101 0.1U, C107 0.1U
C99 0.1U, C94 0.1U, C104 0.1U, C110 0.1U, C95 0.1U
C96 0.1U, C88 0.1U, C87 0.1U, C83 0.1U

VDDA12 120 mils L55 FBMJ2125HM330-T VDDA_1V2

C34 1U, C27 0.1U, C28 0.1U, C32 0.1U, C26 0.1U, C10 22U

VDDA12_13

VDDA18 20 mils L4 TI201209G121 +1.8V

C29 22U, C24 0.1U, C25 0.1U, C33 0.1U, C22 0.1U

VDDA18_13

VDDA_1V2

C114 22U, C59 0.1U, C58 0.1U, C46 0.1U, C47 0.1U
C67 0.1U, C41 0.1U, C48 0.1U, C49 0.1U, C69 0.1U
C103 22U, C61 0.1U, C39 0.1U, C40 0.1U
C38 0.1U, C66 0.1U, C60 0.1U, C68 0.1U
C100 0.1U, C97 0.1U, C78 0.1U, C79 0.1U, C18 *220U

VDDHT30 VDDHT31

+2.5V

C115 22U, C52 0.1U, C74 0.1U, C50 0.1U, C70 0.1U, C31 0.1U, C21 0.1U
C85 0.1U, C55 0.1U, C116 0.1U, C113 0.1U, C93 0.1U, C35 0.1U
C77 0.1U, C42 0.1U, C43 0.1U, C73 0.1U, C89 0.1U, C36 0.1U

+1.8V L7 TI201209G121 VDD18 20 mils

C54 0.1U, C63 0.1U, C57 0.1U, C76 0.1U, C71 1U

+3V D2 BAV99 D1 BAV99 3.3V 2.7

Notice the trace width.

VDDA12_13
VSSA22 C13 4.7U
VDDA18_13
VSSA59 C12 4.7U
VDDHT30
VSS30 C144 4.7U
VDDHT31
VSS89 C122 4.7U

PUT DECOUPLING CAPS ON THE TOP, CLOSE TO BALLS
CONNECT VSSA22,VSSA59,VSS30,VSS89 to the ground.

PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS480M-POWER	2A
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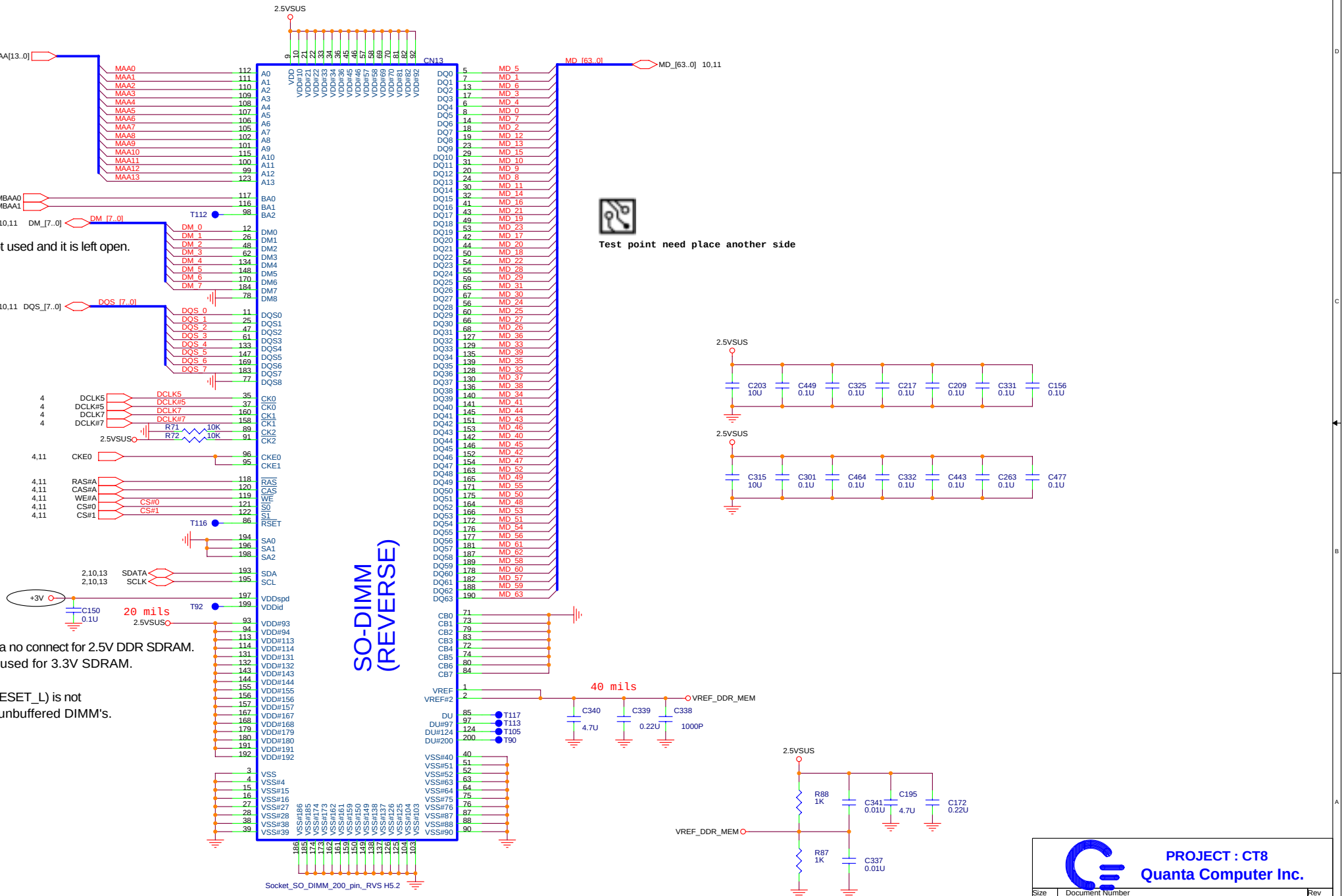
DDR

Unbuffered DDR Near SODIMM Socket

ALLEGRO ROOM PROPERTY
AMD CPU



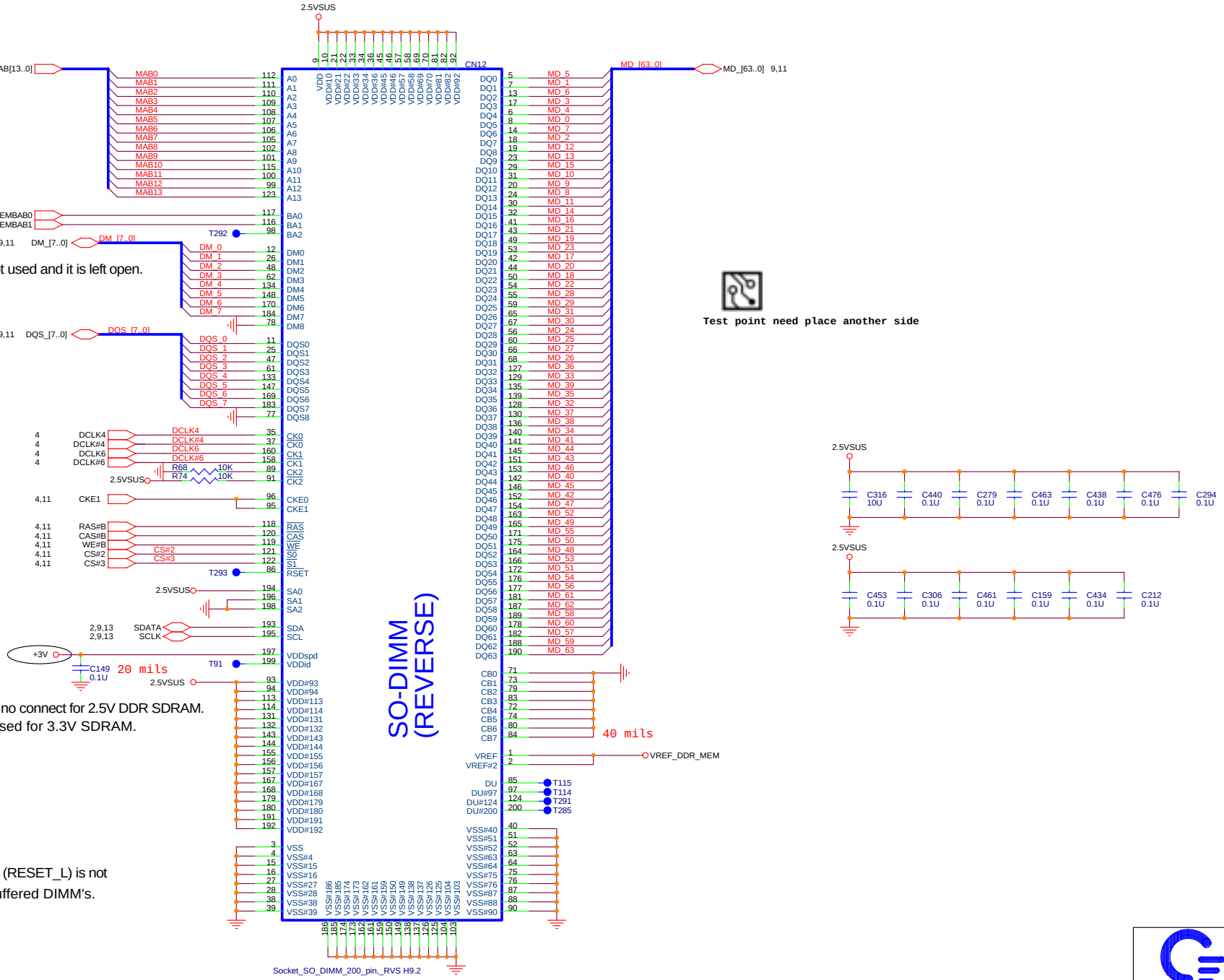
PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR NEAR SO-DIMM	1A
Date: Thursday, April 14, 2005	Sheet 9 of 42	

DDR

Unbuffered DDR Far SODIMM Socket

ALLEGRO ROOM PROPERTY
AMD CPU



NOTE: BA2 is not used and it is left open.

NOTE: VDDid is a no connect for 2.5V DDR SDRAM.
It is only used for 3.3V SDRAM.

NOTE: Pin 10 (RESET_L) is not used by unbuffered DIMM's.

Test point need place another side

PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR FAR SO-DIMM	1A
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DDR

4 MD[63..0] MD[63..0]
4 DQS[7..0] DQS[7..0]
4 DM[7..0] DM[7..0]

MD62	RN46	1	2 10X2	MD_62
MD58		3	4	MD_58
MD56	RN48	1	2 10X2	MD_56
MD61		3	4	MD_61
MD59	RN47	1	2 10X2	MD_59
MD63		3	4	MD_63
MD60	RN49	1	2 10X2	MD_60
MD57		3	4	MD_57
MD55	RN50	1	2 10X2	MD_55
MD50		3	4	MD_50
MD48	RN53	1	2 10X2	MD_48
MD53		3	4	MD_53
MD51	RN51	1	2 10X2	MD_51
MD54		3	4	MD_54
MD49	RN52	1	2 10X2	MD_49
MD52		3	4	MD_52
MD42	RN55	1	2 10X2	MD_42
MD47		3	4	MD_47
MD45	RN58	1	2 10X2	MD_45
MD40		3	4	MD_40
MD43	RN54	1	2 10X2	MD_43
MD46		3	4	MD_46
MD41	RN56	1	2 10X2	MD_41
MD44		3	4	MD_44
MD38	RN59	1	2 10X2	MD_38
MD34		3	4	MD_34
MD32	RN61	1	2 10X2	MD_32
MD37		3	4	MD_37
MD39	RN57	1	2 10X2	MD_39
MD35		3	4	MD_35
MD36	RN60	1	2 10X2	MD_36
MD33		3	4	MD_33
MD27	RN63	1	2 10X2	MD_27
MD26		3	4	MD_26
MD25	RN65	1	2 10X2	MD_25
MD24		3	4	MD_24
MD31	RN62	1	2 10X2	MD_31
MD30		3	4	MD_30
MD28	RN64	1	2 10X2	MD_28
MD29		3	4	MD_29
MD22	RN67	1	2 10X2	MD_22
MD18		3	4	MD_18
MD17	RN69	1	2 10X2	MD_17
MD20		3	4	MD_20
MD19	RN66	1	2 10X2	MD_19
MD23		3	4	MD_23
MD16	RN68	1	2 10X2	MD_16
MD21		3	4	MD_21
MD11	RN71	1	2 10X2	MD_11
MD14		3	4	MD_14
MD9	RN73	1	2 10X2	MD_9
MD8		3	4	MD_8
MD10	RN70	1	2 10X2	MD_10
MD15		3	4	MD_15
MD12	RN72	1	2 10X2	MD_12
MD13		3	4	MD_13
MD7	RN75	1	2 10X2	MD_7
MD2		3	4	MD_2
MD4	RN77	1	2 10X2	MD_4
MD0		3	4	MD_0
MD6	RN74	1	2 10X2	MD_6
MD3		3	4	MD_3
MD5	RN76	1	2 10X2	MD_5
MD1		3	4	MD_1

DQS0	R271	10-0402	DQS_0
DQS1	R269	10-0402	DQS_1
DQS2	R263	10-0402	DQS_2
DQS3	R252	10-0402	DQS_3
DQS4	R243	10-0402	DQS_4
DQS5	R241	10-0402	DQS_5
DQS6	R238	10-0402	DQS_6
DQS7	R236	10-0402	DQS_7

DM0	R272	10-0402	DM_0
DM1	R270	10-0402	DM_1
DM2	R264	10-0402	DM_2
DM3	R253	10-0402	DM_3
DM4	R245	10-0402	DM_4
DM5	R242	10-0402	DM_5
DM6	R239	10-0402	DM_6
DM7	R237	10-0402	DM_7

9,10 MD_[63..0]

MD_2	RN33	1	2 68X4
MD_7		3	4
MD_6		5	6
MD_3		7	8
MD_5	RN35	1	2 68X4
MD_1		3	4
MD_0		5	6
MD_4		7	8
MD_14	RN30	1	2 68X4
MD_11		3	4
MD_15		5	6
MD_10		7	8
MD_8	RN32	1	2 68X4
MD_9		3	4
MD_12		5	6
MD_13		7	8
MD_18	RN27	1	2 68X4
MD_22		3	4
MD_23		5	6
MD_19		7	8
MD_16	RN29	1	2 68X4
MD_21		3	4
MD_17		5	6
MD_20		7	8
MD_26	RN24	1	2 68X4
MD_31		3	4
MD_30		5	6
MD_27		7	8
MD_29	RN26	1	2 68X4
MD_28		3	4
MD_25		5	6
MD_24		7	8
MD_39	RN11	1	2 68X4
MD_35		3	4
MD_38		5	6
MD_34		7	8
MD_36	RN13	1	2 68X4
MD_33		3	4
MD_32		5	6
MD_37		7	8
MD_47	RN8	1	2 68X4
MD_42		3	4
MD_46		5	6
MD_43		7	8
MD_44	RN10	1	2 68X4
MD_41		3	4
MD_45		5	6
MD_40		7	8
MD_55	RN5	1	2 68X4
MD_50		3	4
MD_51		5	6
MD_54		7	8
MD_52	RN7	1	2 68X4
MD_49		3	4
MD_48		5	6
MD_53		7	8
MD_63	RN2	1	2 68X4
MD_59		3	4
MD_62		5	6
MD_58		7	8
MD_61	RN4	1	2 68X4
MD_56		3	4
MD_57		5	6
MD_60		7	8

DM_7	RN3	1	2 68X2
DQS_7		3	4
DM_5	RN9	1	2 68X2
DQS_5		3	4
DM_3	RN25	1	2 68X2
DQS_3		3	4
DM_1	RN31	1	2 68X2
DQS_1		3	4
DQS_6	RN6	1	2 68X2
DM_6		3	4
DQS_4	RN12	1	2 68X2
DM_4		3	4
DM_2	RN28	1	2 68X2
DQS_2		3	4
DM_0	RN34	1	2 68X2
DQS_0		3	4

9,10 DQS_[7..0] DQS_[7..0]
9,10 DM_[7..0] DM_[7..0]

VTT_DDR

4,9 MAA[13..0]

MAA0	RN18	1	2 47X4
MAA2		3	4
MAA8		5	6
MAA11		7	8
MAA1	RN20	1	2 47X4
MAA3		3	4
MAA5		5	6
		7	8
MAA7	RN22	1	2 47X4
MAA9		3	4
MAA4		5	6
MAA6		7	8
MAA12	R70		47
MAA13			

4,9 MEMBAA0

4,9 CKE0 R73 47
4,10 CKE1 R64 47

4,9 WE#A	RN16	1	2 47X4
MAA10		3	4
MAA13		5	6
4,9 CS#0	CS#0	7	8

4,9 MEMBAA1	RN15	1	2 47X4
4,9 RAS#A		3	4
CS#1	CS#1	5	6
4,9 CS#1		7	8
4,9 CAS#A			

VTT_DDR

4,10 MAB[13..0]

MAB2	RN21	1	2 47X4
MAB4		3	4
MAB6		5	6
MAB5		7	8
MAB3	RN19	1	2 47X4
MAB1		3	4
MAB10		5	6
		7	8
MAB11	RN23	1	2 47X4
MAB8		3	4
MAB9		5	6
MAB7		7	8
MAB12	R65		47

4,10 MEMBAB0

4,10 RAS#B	RN14	1	2 47X4
CS#3	CS#3	3	4
4,10 CS#3	CS#2	5	6
4,10 CS#2	MAB13	7	8

4,10 CAS#B	RN17	1	2 47X4
4,10 WE#B		3	4
4,10 MEMBAB1		5	6
MAB0		7	8

03/19 Modify ->Quanta stock haven't 68x4 (8P4R-0402)

Place on each end of the VTT island.

VTT_DDR
C127 10U
C129 10U

LAYOUT: Locate close to Clawhammer socket.

VTT_DDR
REV.B
C280 *220U
2.5VSUS
C145 100U/6.3V
C481 100U/6.3V
C128 4.7U
C265 0.22U

LAYOUT: Place on VTT fill near Clawhammer and near DIMMs

VTT_DDR
C188 1000P
C169 100P
C260 100P
C157 1000P
C218 1000P
C186 100P
C261 100P
C459 1000P

LAYOUT: Place a cap every 1 in. on VTT traces between Clawhammer and DDR.

VTT_DDR
C250 0.22U
C343 4.7U
C319 0.22U
C125 4.7U
C326 0.22U
C347 4.7U
C228 0.22U
C348 4.7U
C230 0.22U
C342 4.7U
C236 0.22U
C349 4.7U
C278 0.22U
C134 4.7U
C204 0.22U
C124 4.7U
C305 0.22U
C133 4.7U

LAYOUT: Place alternating caps to GND and VDD_2.5_SUS in a single line along VTT_DDR_SUS island.

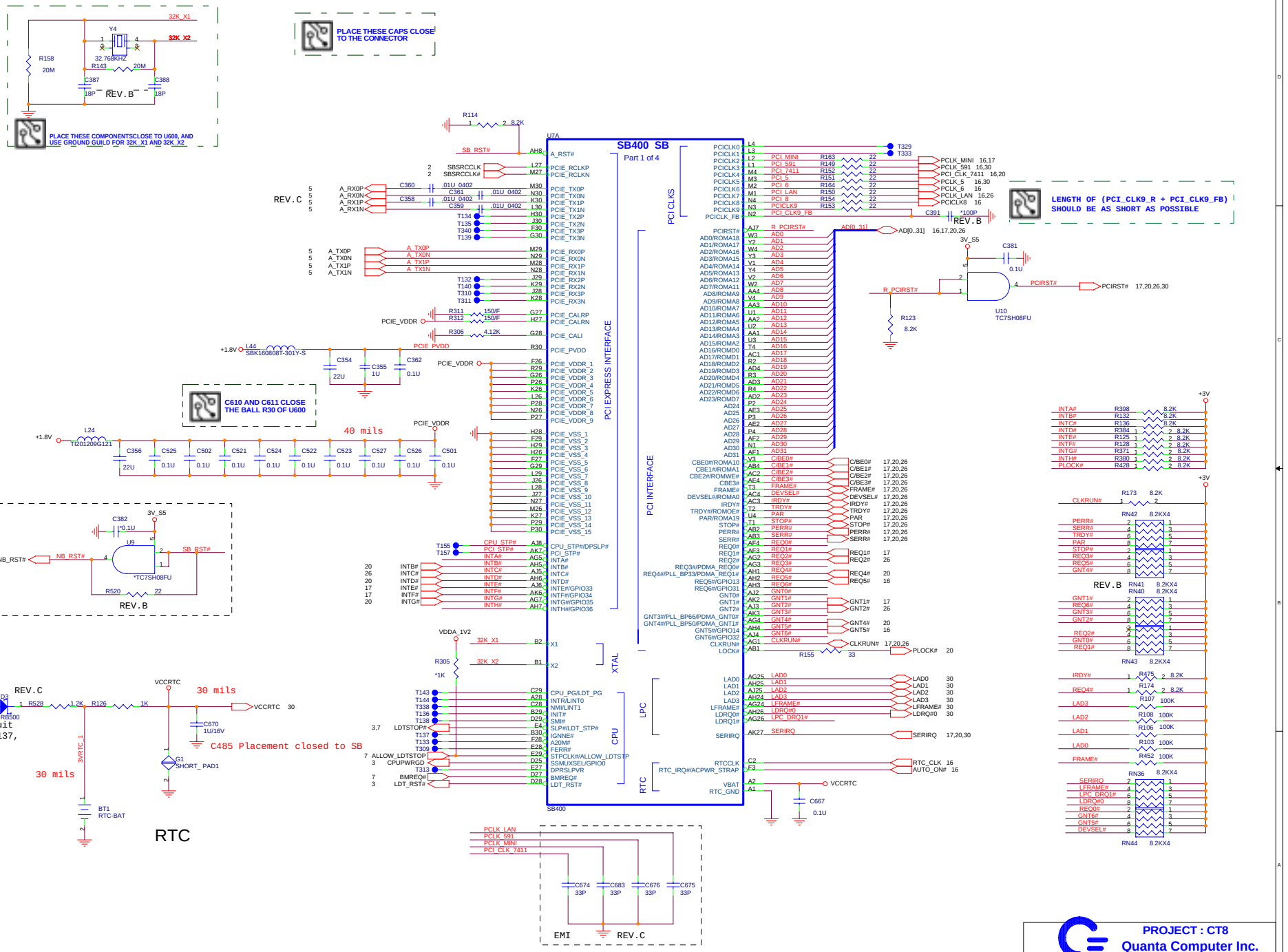
VTT_DDR
C233 0.1U C287 0.1U C335 0.1U C265 0.1U C219 0.1U C201 0.1U C302 0.1U C162 0.1U C442 0.1U C312 0.1U C327 0.1U C270 0.1U C170 0.1U C220 0.1U C275 0.1U C147 0.1U C282 0.1U C446 0.1U C241 0.1U C289 0.1U C235 0.1U C330 0.1U C202 0.1U C436 0.1U C151 0.1U C276 0.1U C259 0.1U C264 0.1U C174 0.1U C183 0.1U C291 0.1U C160 0.1U C334 0.1U C290 0.1U

VTT_DDR
2.5VSUS
C300 0.1U C210 0.1U C298 0.1U C346 0.1U C322 0.1U C274 0.1U C185 0.1U C227 0.1U C344 0.1U C309 0.1U C239 0.1U C317 0.1U C165 0.1U C132 0.1U C323 0.1U C211 0.1U C167 0.1U C153 0.1U C189 0.1U C173 0.1U C252 0.1U C333 0.1U C310 0.1U C345 0.1U C131 0.1U C249 0.1U C135 0.1U C197 0.1U C273 0.1U C242 0.1U C251 0.1U C269 0.1U C271 0.1U

PROJECT : CT8
Quanta Computer Inc.

Size: Custom	Document Number: DDR SO-DIMM TERMINATION	Rev: 2A
Date: Thursday, April 14, 2005	Sheet 11 of 42	

CLG


32K_X1
32K_X2
Y4
32.768KHZ
R158
20M
R143
20M
C387
18P
C388
18P
REV.B
PLACE THESE CAPS CLOSE TO THE CONNECTOR
PLACE THESE COMPONENTSCLOSE TO U600, AND USE GROUND GUILD FOR 32K_X1 AND 32K_X2
SB400 SB
Part 1 of 4
U7A
SB400
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
XTAL
LPC
CPU
RTC
SB_RST#
PCIE_VDDR
PCIE_PVDD
+1.8V
L44
SBK160808T-301Y-S
C354
22U
C355
1U
C362
0.1U
C610 AND C611 CLOSE THE BALL R30 OF U600
40 mils
L24
TI2012D9G121
C356
22U
C525
0.1U
C502
0.1U
C521
0.1U
C524
0.1U
C522
0.1U
C523
0.1U
C527
0.1U
C526
0.1U
C501
0.1U
C382
*0.1U
U9
*TC7SH08FU
NB_RST#
SB_RST#
R520
22
REV.B
3V_S5
VCCRTC
30 mils
C670
1U/16V
C485 Placement closed to SB
G1
SHORT_PAD1
BT1
RTC-BAT
RTC
REV.B
DEL D3
Remove charge circuit
Q16, R129, R133, R137,
R140
REV.C
3VPCU
D3
RB500
R528
1.2K
R126
1K
3VRTC_1
30 mils
VDDA_1V2
32K_X1
32K_X2
*1K
R305
EMI
PCLK_LAN
PCLK_591
PCLK_MINI
PCI_CLK_7411
C674
33P
C683
33P
C676
33P
C675
33P
REV.C
LENGTH OF (PCI_CLK9_R + PCI_CLK9_FB) SHOULD BE AS SHORT AS POSSIBLE
PCI_MINI
PCI_591
PCI_7411
PCI_5
PCI_6
PCI_LAN
PCI_8
PCI_CLK9
PCI_CLK9_FB
R163
R149
R152
R151
R164
R150
R154
R153
22
*100P
C391
REV.B
PCLK_MINI 16,17
PCLK_591 16,30
PCI_CLK_7411 16,20
PCLK_5 16,30
PCLK_6 16
PCLK_LAN 16,26
PCICLK8 16
T329
T333
R_PCIRST#
R123
8.2K
C381
0.1U
U10
TC7SH08FU
PCIRST# 17,20,26,30
AD[0..31] 16,17,20,26
C/BE0# 17,20,26
C/BE1# 17,20,26
C/BE2# 17,20,26
C/BE3# 17,20,26
FRAME# 17,20,26
DEVSEL# 17,20,26
IRDY# 17,20,26
TRDY# 17,20,26
PAR 17,20,26
STOP# 17,20,26
PERR# 17,20,26
SERR# 17,20,26
REQ1# 17
REQ2# 26
REQ4# 20
REQ5# 16
GNT1# 17
GNT2# 26
GNT4# 20
GNT5# 16
CLKRUN# 17,20,26
PLOCK# 20
R155
33
LAD0 30
LAD1 30
LAD2 30
LAD3 30
LFRAME# 30
LDRQ#0 30
LPC_DRQ1#
SERIRQ 17,20,30
RTC_CLK 16
AUTO_ON# 16
VCCRTC
C667
0.1U
+3V
INTA# R398 8.2K
INTB# R132 8.2K
INTC# R136 8.2K
INTD# R384 8.2K
INTE# R125 8.2K
INTF# R128 8.2K
INTG# R371 8.2K
INTH# R380 8.2K
PLOCK# R428 8.2K
CLKRUN# R173 8.2K
RN42 8.2KX4
PERR#
SERR#
TRDY#
PAR
STOP#
REQ3#
REQ5#
GNT4#
RN41 8.2KX4
RN40 8.2KX4
GNT1#
REQ6#
GNT3#
GNT2#
REQ2#
GNT0#
REQ1#
RN43 8.2KX4
IRDY# R475 8.2K
REQ4# R174 8.2K
LAD3 R107 100K
LAD2 R108 100K
LAD1 R106 100K
LAD0 R103 100K
FRAME# R452 100K
RN36 8.2KX4
SERIRQ
LFRAME#
LPC_DRQ1#
LDRQ#0
REQ0#
GNT6#
GNT5#
DEVSEL#
RN44 8.2KX4
PROJECT : CT8
Quanta Computer Inc.
Size C
Document Number SB400-PCIE/PCI/CPU/LPC
Rev 3A
Date: Thursday, April 14, 2005
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CLG

Please double check SB400 pin D5 & pin A27 define,
because cann't meet ATI library/symbols.

GPM6# R376 4.7K
SUSB# R336 4.7K
SUSC# R144 4.7K
DNBSWON# R135 4.7K
TEMP_ALARM# R369 4.7K
PCI_PME# R385 4.7K
RI# R178 10K
BATLOW# R377 4.7K
GPM7# R379 4.7K

REV.B 1. Remove R400.

CRT_SENSE# R313 4.7K
AGP_BUSY# R330 4.7K
AGP_STP# R324 4.7K
SDATA R96 2.2K
SCLK R97 2.2K

PWROK_SB is 33ms ~ 500ms after NB_PWRGD

R503 STUFF IS FULL FEATURE.
R504 STUFF IS DE-FEATURE.

30 mils
R419 10K R418 10K
30 SCI# 1SS355 D4 SCI_#
30 SWI# 1SS355 D15 SWI#_1

AC_SDIN2 R432 8.2K
SDINB R412 10K
BITCLK R446 10K
REV.B

U7D
SB400 SB
Part 4 of 4
SB400

ACPI / WAKE UP EVENTS
TALERT#/TEMP_ALERT#/GPIO10
BLINK/GPM6#
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST1
TEST0
GA20IN
KBRST#
SMBALERT#/THRMTRIP#/GEVENT2#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
VOLT_ALERT#/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#

CLK / RST
RSMRST#
14M_X1/OSC
14M_X2
SIO_CLK

GPIO
ROM_CS#/GPIO1
GHI#/GPIO6
VGATE/GPIO7
AGP_STP#/GPIO4
AGP_BUSY#/GPIO5
FANOUT0/GPIO3
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
DDC2_SCL/GPIO11
DDC2_SDA/GPIO12

(NOT USED)
NC1
NC4
NC3
NC2

AC97
AC_BITCLK
AC_SDOUT
AC_SDIN0
AC_SDIN1
AC_SDIN2
AC_SYNC
AC_RST#
SPDIF_OUT

USB INTERFACE
48M_X1/USBCLK
48M_X2
USB_RCOMP
USB_VREFOUT
USB_ATEST1
USB_ATEST0
USB_OC0#/GPM0#
USB_OC1#/GPM1#
USB_OC2#/FANOUT1/GPM2#
USB_OC3#/GPM3#
USB_OC4#/GPM4#
USB_OC5#/GPM5#
USB_OC6#/FAN_ALERT#/GEVENT6#
USB_OC7#/CASE_ALERT#/GEVENT7#
USB_HSDP7+ / USB_HSDM7-
USB_HSDP6+ / USB_HSDM6-
USB_HSDP5+ / USB_HSDM5-
USB_HSDP4+ / USB_HSDM4-
USB_HSDP3+ / USB_HSDM3-
USB_HSDP2+ / USB_HSDM2-
USB_HSDP1+ / USB_HSDM1-
USB_HSDP0+ / USB_HSDM0-

USB PWR
AVDDTX_0 AVDDTX_1 AVDDTX_2 AVDDTX_3
AVDDRX_0 AVDDRX_1 AVDDRX_2 AVDDRX_3
AVDDC
AVSSC
AVSS_USB_1 ... AVSS_USB_24

R361 0 USBCLK_EXT 2
R362 *0 C609 *20P
R356 *10M Y8 *XTAL-48MHZ
R355 *0 C570 *20P
USB_RCOMP R111 11.8K
KBSMI# KBSMI# 30
USB_OCP_1# BATLOW# BATLOW# 30
BT_OFF#
USB_OCP_4#
USB_OCP_5#
USB_OCP_6#
USB_OCP_7#
REV.D

RN38 10KX4
USB_OCP_1# BT_OFF# USB_OCP_5# USB_OCP_4#
REV.D
USB_OCP_5# R533 *10K
USB_OCP_4# R534 *10K
USB_OCP_6# R127 10K
USB_OCP_7# R131 10K
KBSMI# R102 4.7K

USBP5+ USBP5- 33
USBP4+ USBP4- 32
USBP2+ USBP2- 33
USBP1+ USBP1- 22
USBP0+ USBP0- 22

3V_S5
REV.C +3V R503 10K R504 *10K
REV.B R99 10K R318 10K +3V RF_OFF# MB_ID
REV.D T146 SB_14M_X2 T147
REV.B AGP_STP# AGP_BUSY# R316 10K
REV.B DEL R161

23 SPK
2,9,10 SCLK
2,9,10 SDATA
31 CRT_SENSE#
18 LCDID0
18 LCDID1
18 LCDID2

T158 T331 T330 T159

17,23 BITCLK
16,17,23 SDOUT1
23 SDINA
17 SDINB
17,23 SYNC1
17,23 -CODEC_RST
16 SPDIF_OUT
R146 33 AC_DATA_OUT_R
AC_SDIN2
R148 33 AC_SYNC_R
R443 33 #CODEC_RST
+3V R147 10K
REV.B

BT_OFF# BT_OFF# 33
RF_OFF# RF_OFF# 17
REV.B

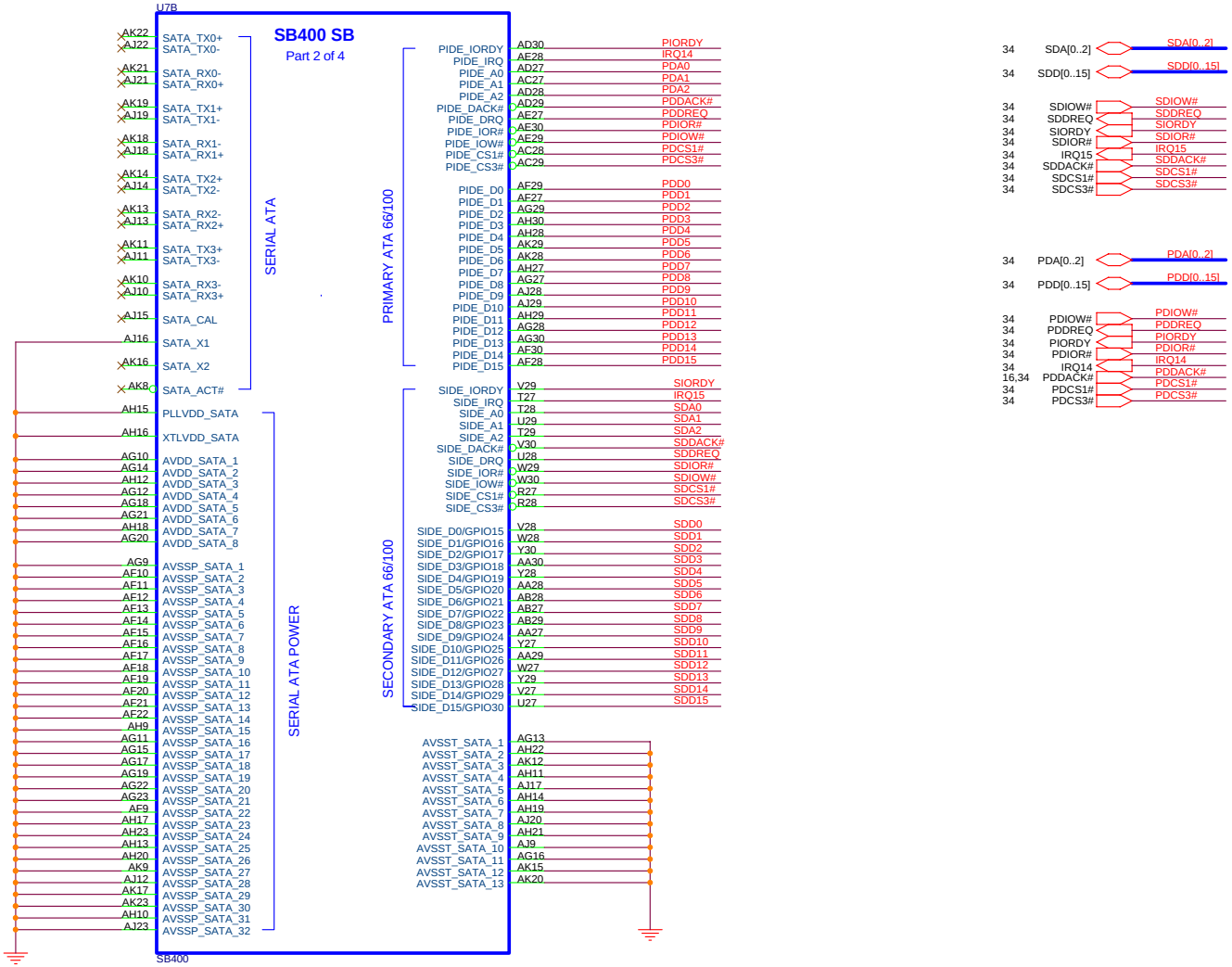
AVDDTX_USB 20 mils L27
C372 22U C545 0.1U C555 0.1U C612 0.1U C589 0.1U C566 0.1U C571 0.1U
TI201209G121
3VSUS
04/06 Modify
AVDDRX_USB 20 mils L28
C599 0.1U C553 0.1U C575 0.1U C563 0.1U C581 0.1U C574 0.1U C552 22U
TI201209G121
3.3V_AVDDC 20 mils L29
C374 22U C376 1U C569 0.1U
SBK160808T-301Y-S

C641 AND C642 CLOSE THE BALL A16 OF U600

PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB400-ACPI/GPIO/USB/AC97	3A
Date: Thursday, April 14, 2005	Sheet 13 of 42	

CLG



PROJECT : CT8

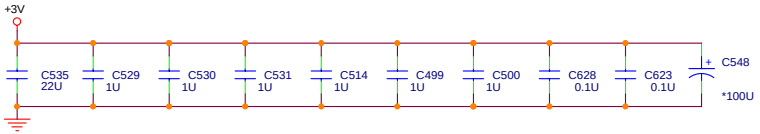
Quanta Computer Inc.

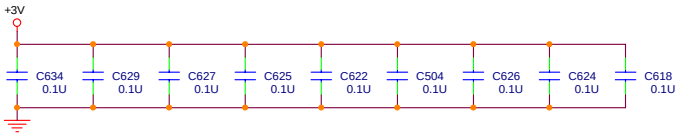
Size	Document Number	Rev
Custom	SB400-SATA/IDE	1A

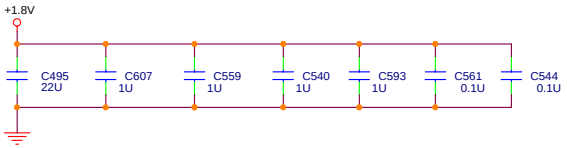
Date: Thursday, April 14, 2005 Sheet 14 of 42

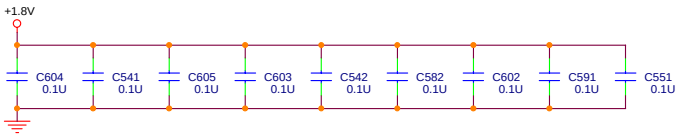
CLG

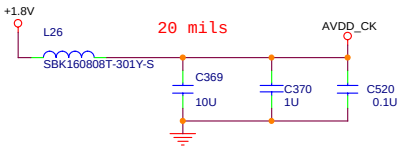
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

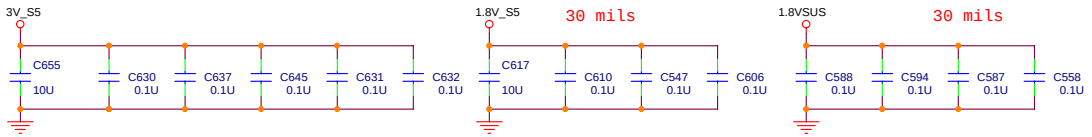


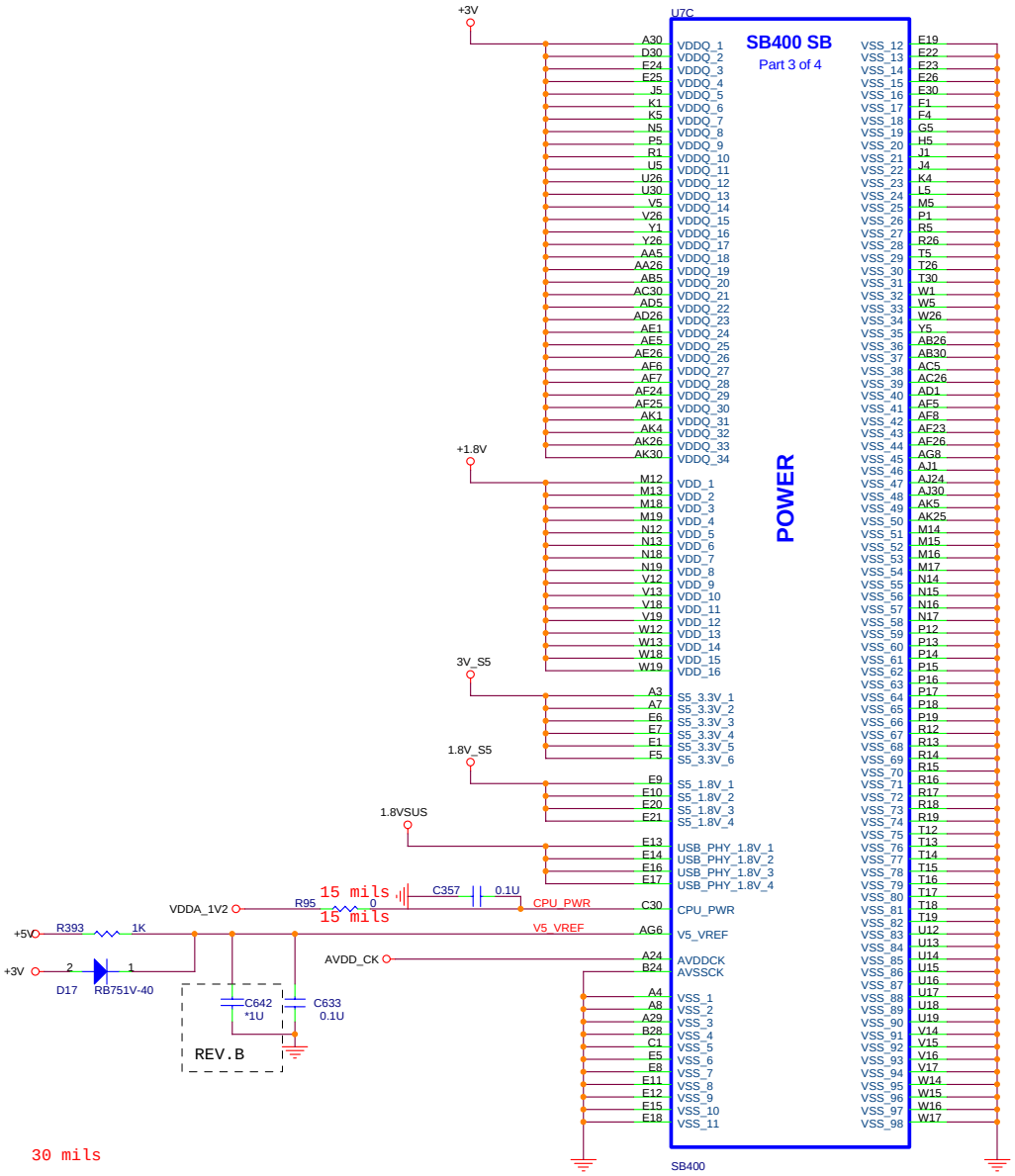










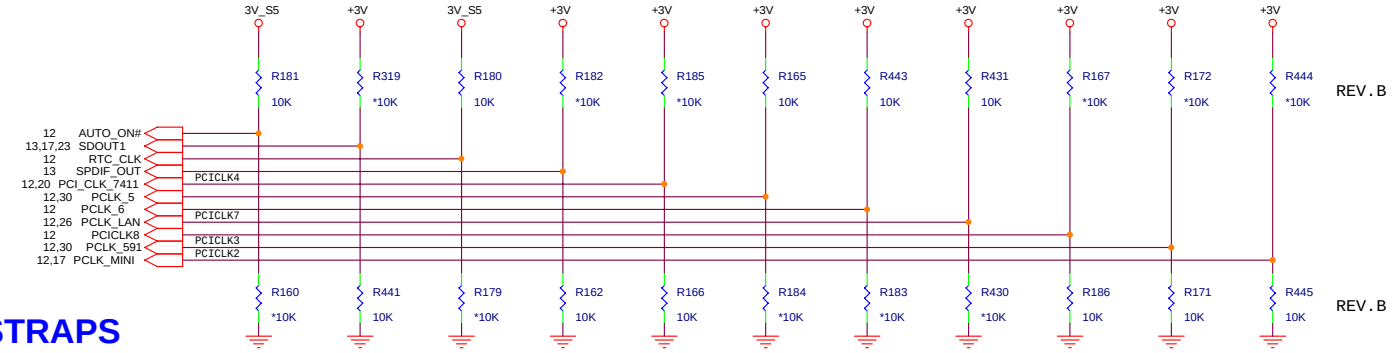


PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB400-POWER & DECOUPLING	2A

Date: Thursday, April 14, 2005 Sheet 15 of 42

CLG



REQUIRED STRAPS

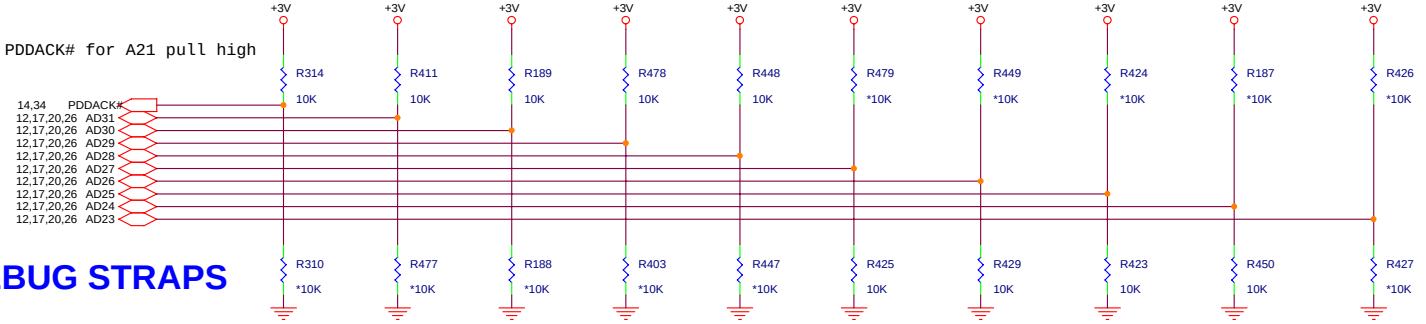
	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK_7411	PCLK_5	PCLK_6	PCLK_LAN	PCI_CLK8	PCLK_591
					PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7	PCI_CLK8	PCI_CLK3
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz OSC MODE DEFAULT	14MHz OSC MODE DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM L,H = NORMAL LPC ROM DEFAULT L,L = FWH ROM		USB PHY PWRDOWN DISABLE DEFAULT
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz XTAL MODE	14MHz XTAL MODE	CPU I/F = P4			USB PHY PWRDOWN ENABLE

Need to check

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

DEBUG STRAPS

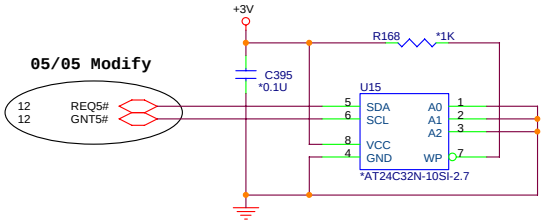
PDDACK# for A21 pull high



	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE SHORT RESET	PLL CHARGE PUMP CTRL BIT 1 HI DEFAULT	PLL CHARGE PUMP CTRL BIT 0 HI DEFAULT	PLL VCO CTRL BIT 1 HI DEFAULT	PLL VCO CTRL BIT 0 HI DEFAULT	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BY PASS USB PLL
PULL LOW	USE LONG RESET DEFAULT	PLL CHARGE PUMP CTRL BIT 1 LO	PLL CHARGE PUMP CTRL BIT 0 LO	PLL VCO CTRL BIT 1 LO	PLL VCO CTRL BIT 0 LO	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	USE USB PLL DEFAULT

Need to check

05/05 Modify

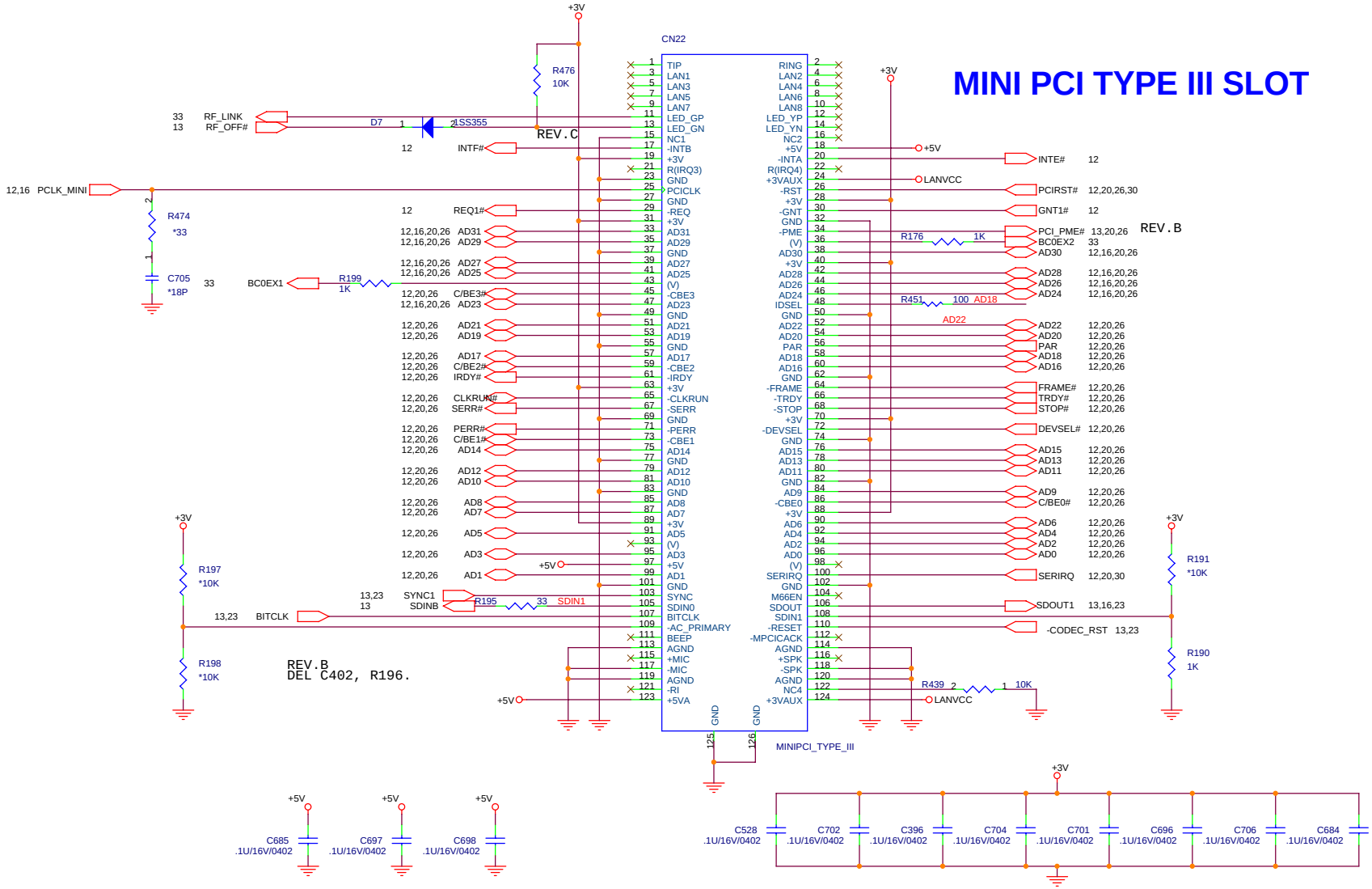


SB PCIE EEPROM STRAPS

PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB400-STRAPS	2A
Date: Thursday, April 14, 2005	Sheet 16 of 42	

MINI PCI TYPE III SLOT

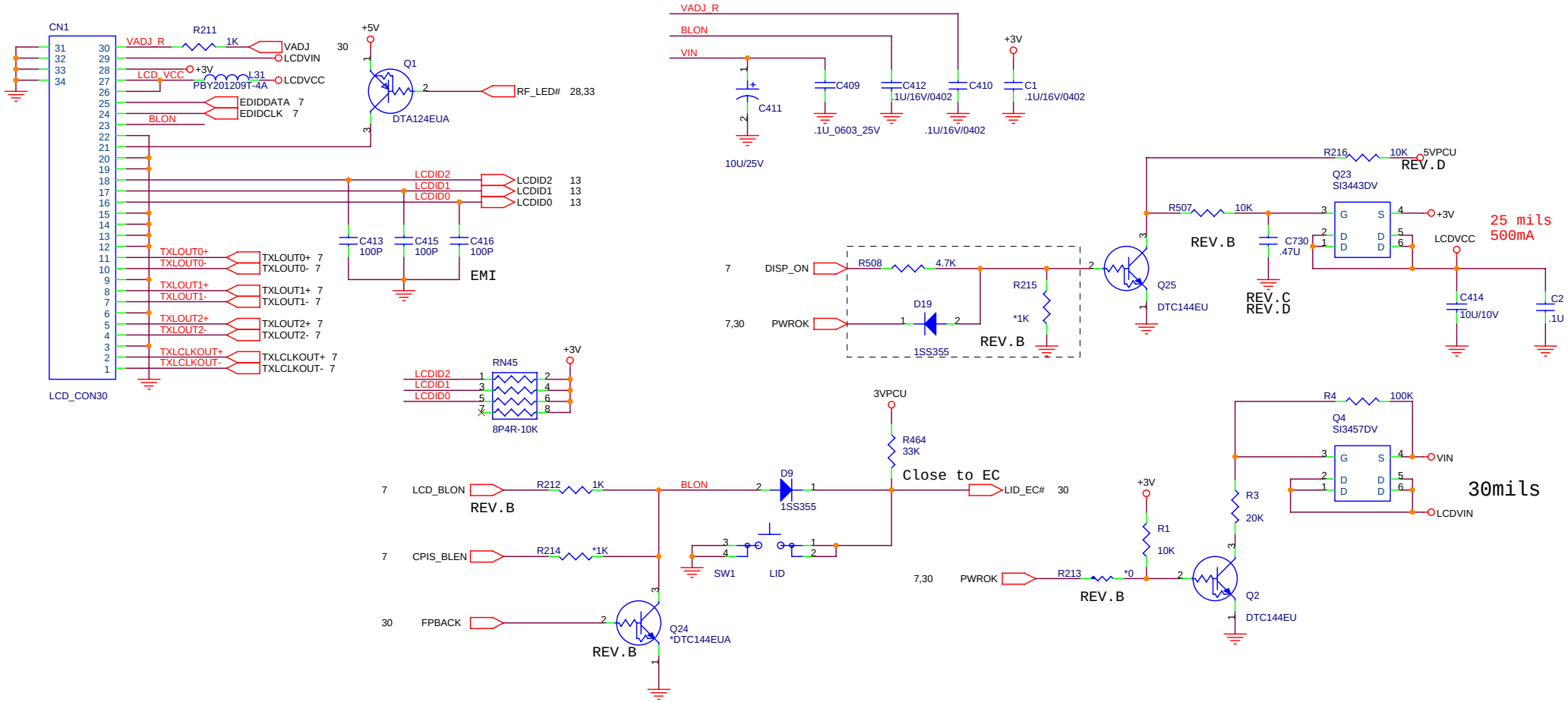


REV.B

1. Remove R175, Q19.
2. CN22 pin 34 connect to PCI_PME#.

PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom		3A
Date: Thursday, April 14, 2005	Sheet 17 of 42	

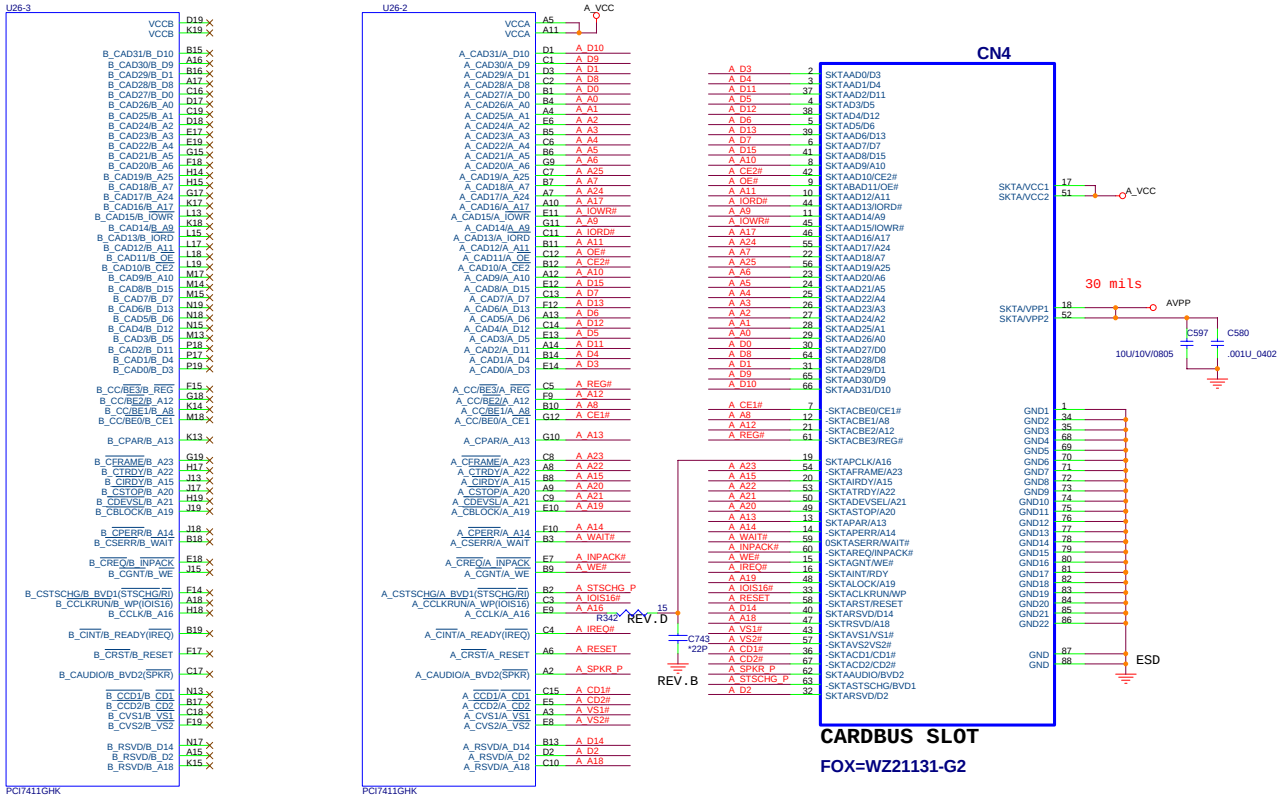


PROJECT : CT8			
Quanta Computer Inc.			
Size B	Document Number		Rev 3A
Date: Thursday, April 14, 2005		Sheet 18 of 42	

CardBus Connector

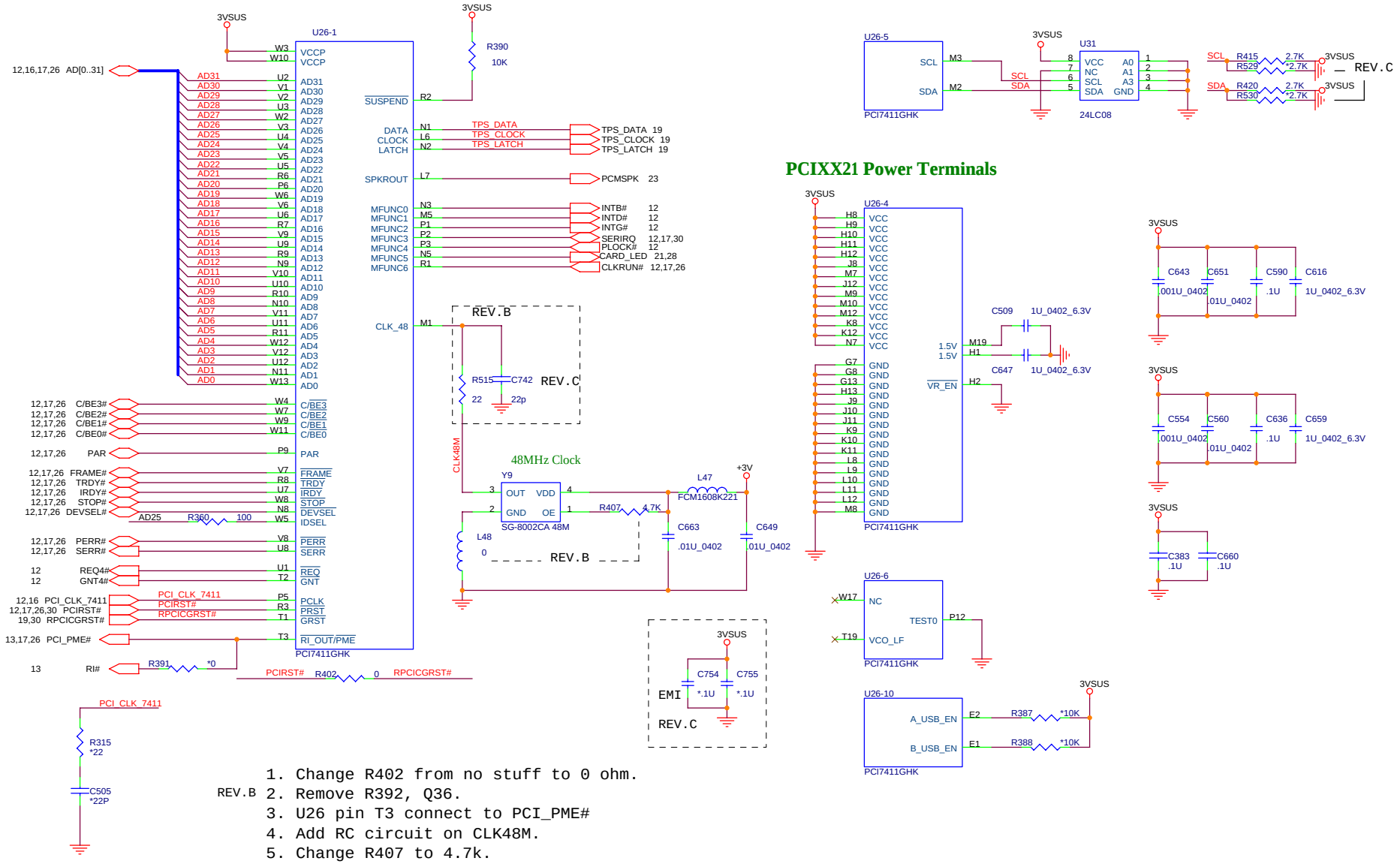
REV.B

REMOVE PCI1510 CIRCUIT AND PARTS.



PROJECT : CT8			
Quanta Computer Inc.			
Size: C	Document Number		Rev: 2A
Date: Thursday, April 14, 2005		Sheet 19 of 42	

CardBus



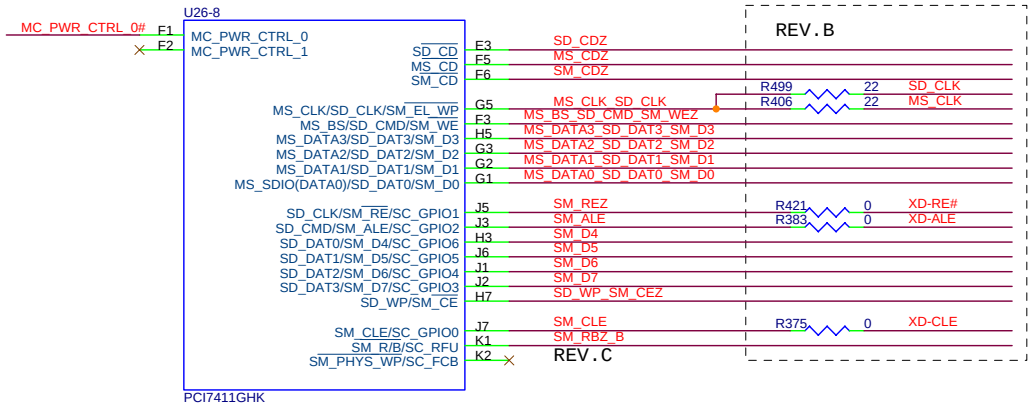
PCIXX21 Power Terminals

REV.B
1. Change R402 from no stuff to 0 ohm.
2. Remove R392, Q36.
3. U26 pin T3 connect to PCI_PME#
4. Add RC circuit on CLK48M.
5. Change R407 to 4.7k.
6. Change L48 to 0 ohm.

PROJECT : CT8
Quanta Computer Inc.

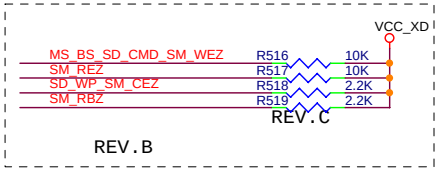
Size	Document Number	Rev
Custom		3A
Date: Thursday, April 14, 2005	Sheet 20 of 42	

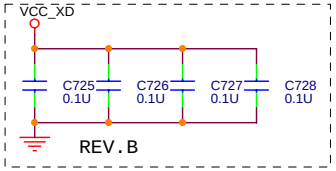
CARD POWER CONTROL



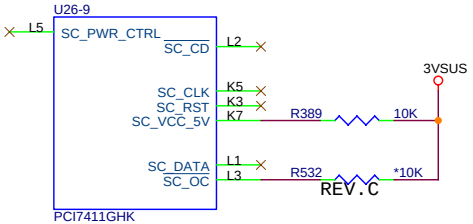
REV.B

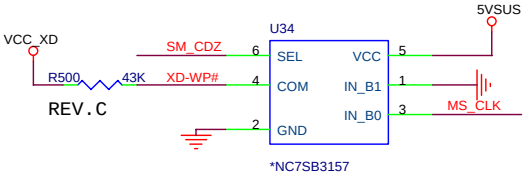
1. Remove R397, D16, R489.
2. Add a Quick Switch U34 to isolate clock.
3. Change R501 to 0 ohm.
4. CN5 pin 35, 43 connect to the same net.
5. ADD R516, R517, R518, R519.

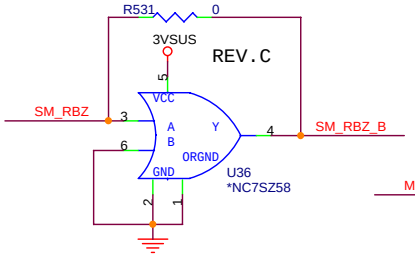


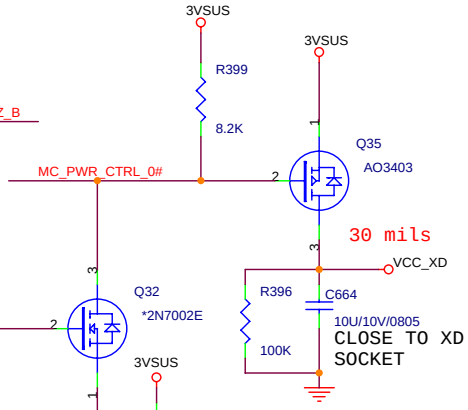


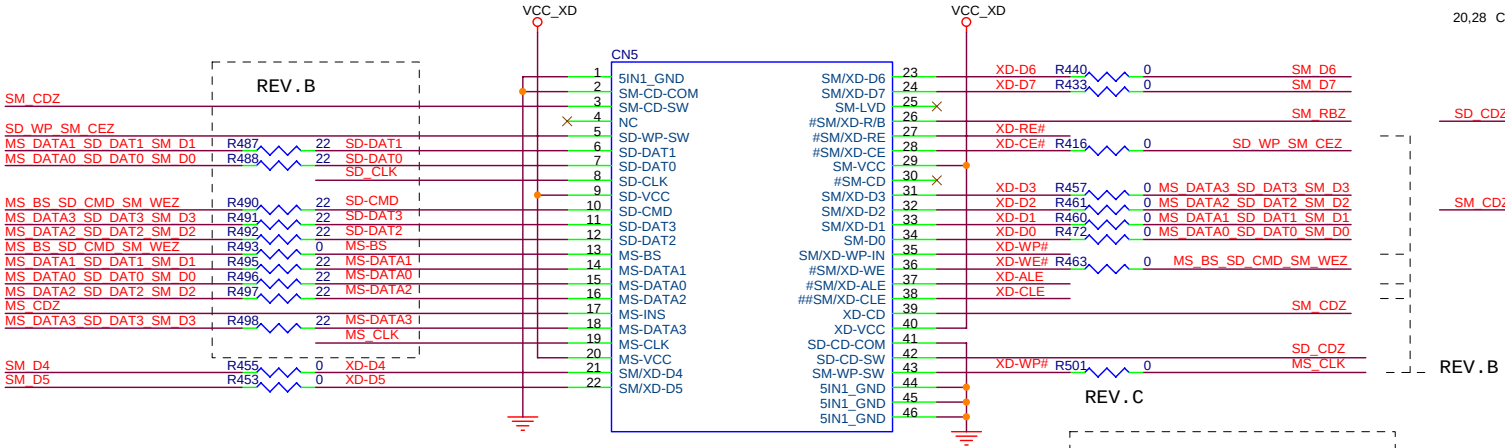
R499,421,383,375 move to chip side.





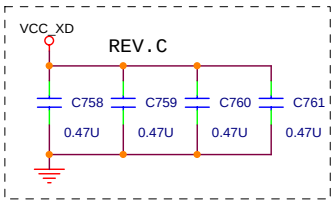


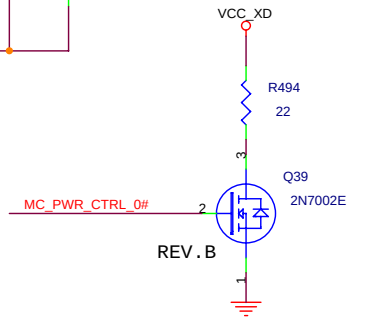




rev.f

5 IN1 CARD READER





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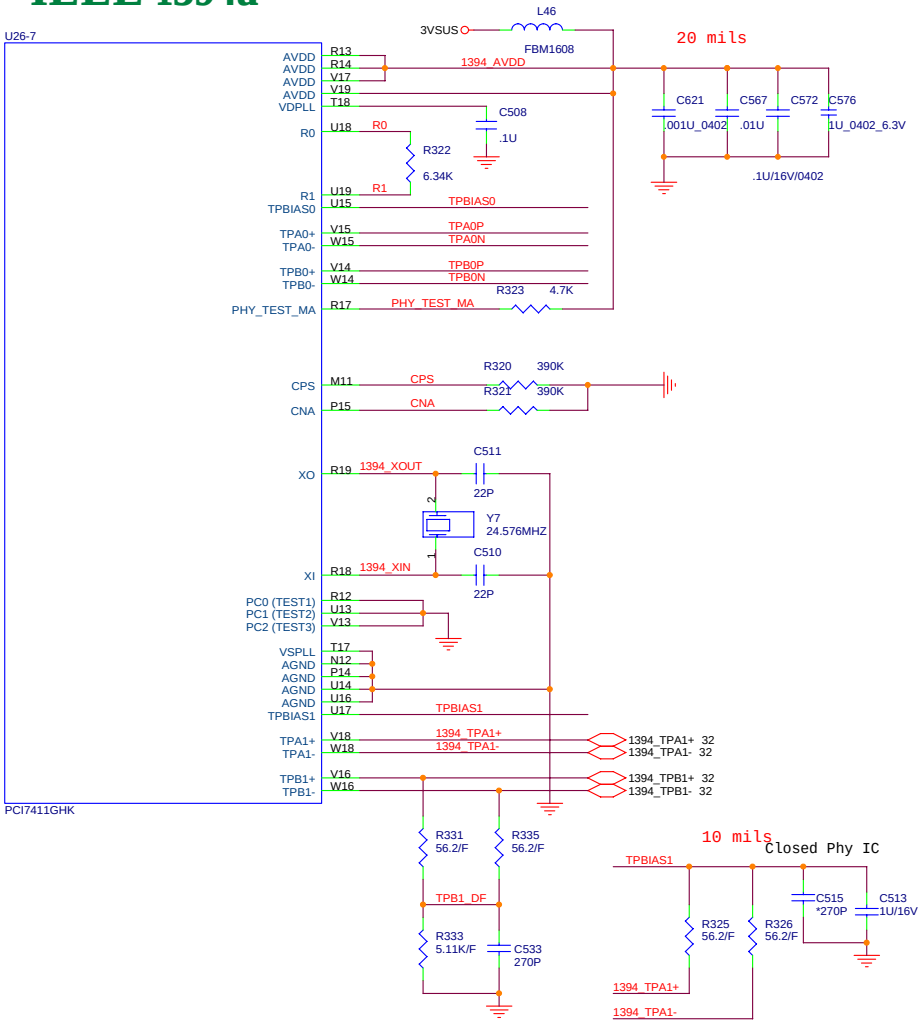
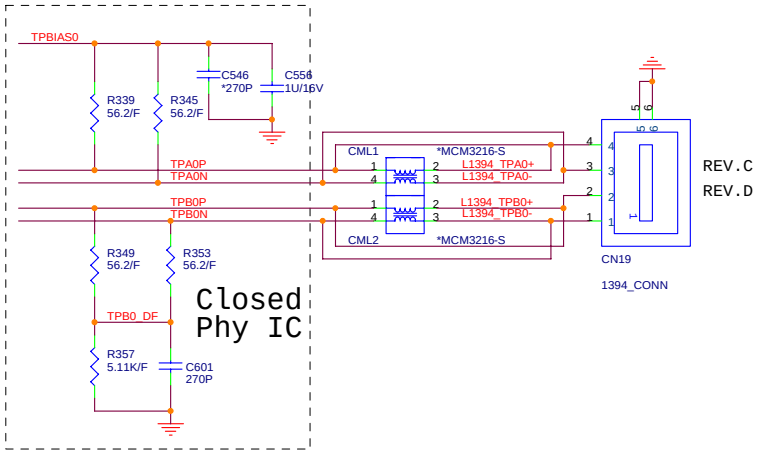
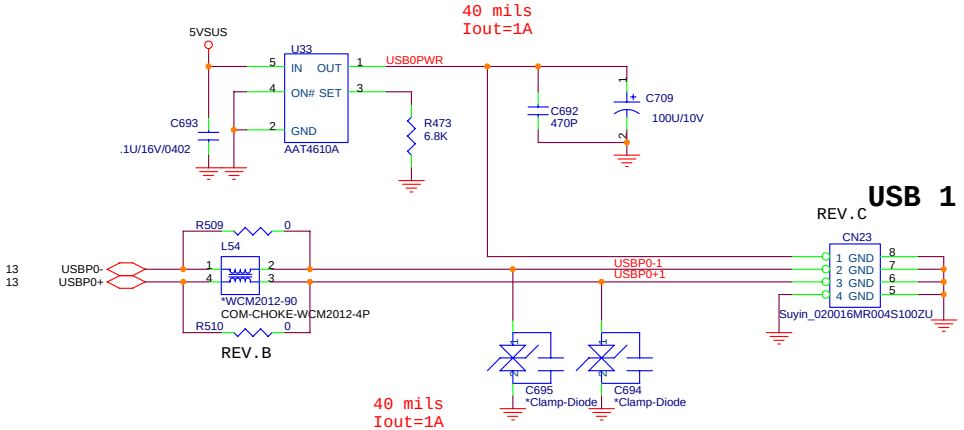
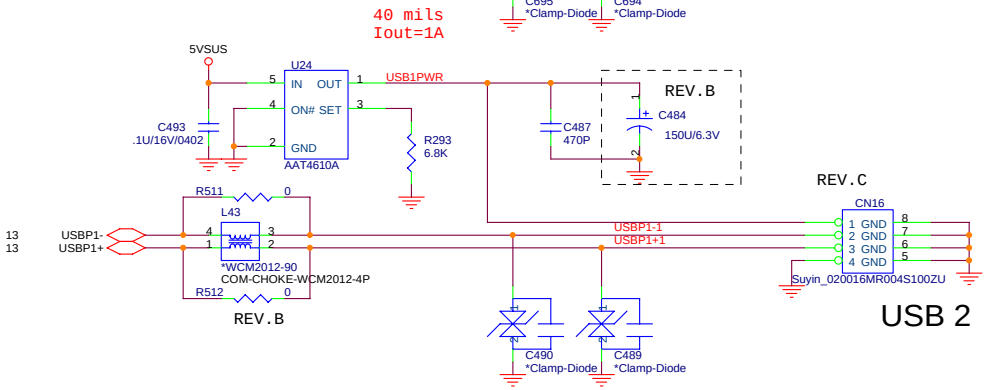
IEEE 1394a



IEEE 1394 CONNECTOR







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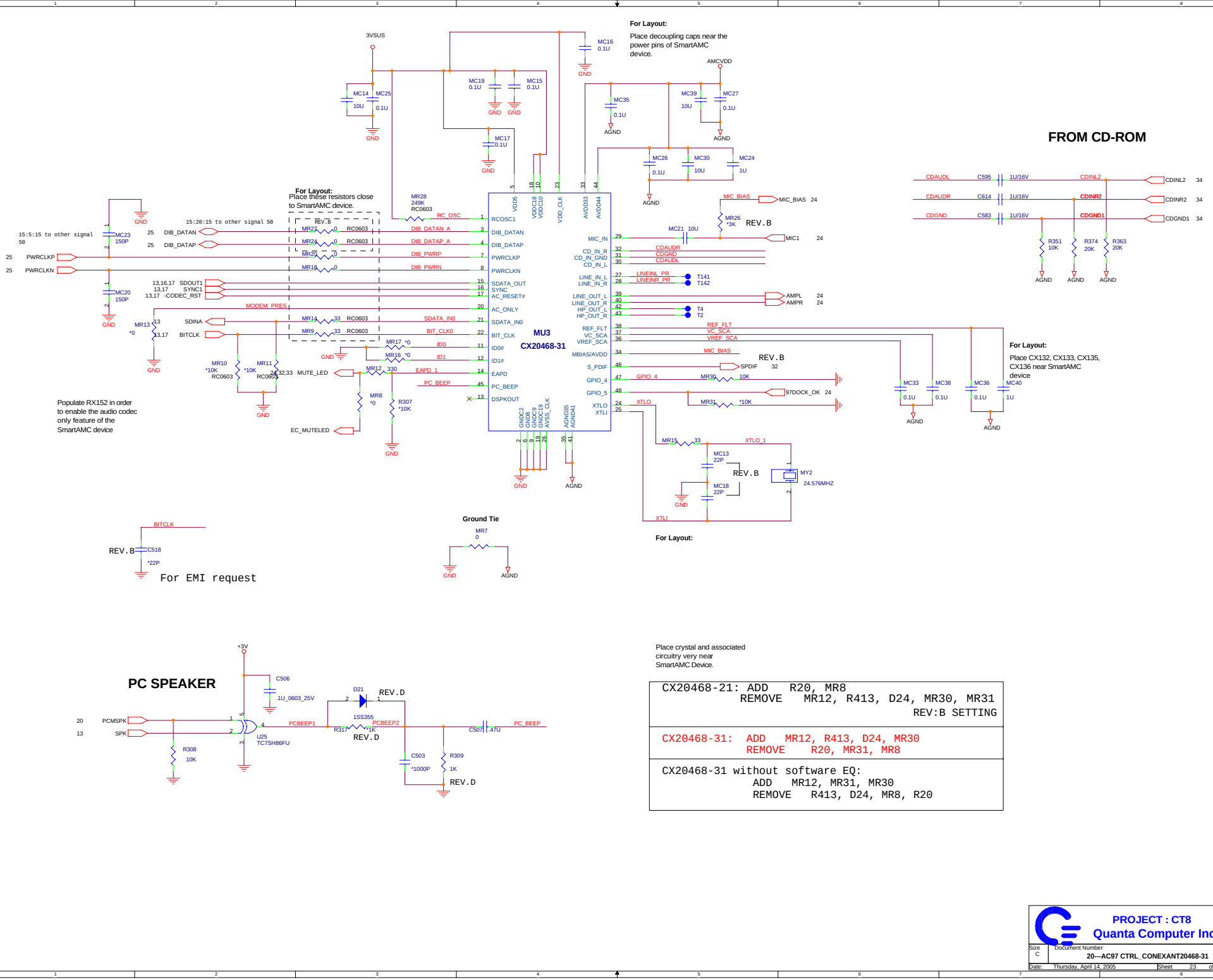
For Layout:
Place decoupling caps near the power pins of SmartAMC device.
3VSUS
AMCVDD
MC16 0.1U
MC19 0.1U
MC15 0.1U
MC14 10U
MC25 0.1U
MC17 0.1U
MC35 0.1U
MC39 10U
MC27 0.1U
MC26 0.1U
MC30 10U
MC24 1U
AGND
GND
FROM CD-ROM
CDAUDL C595 1U/16V CDINL2 CDINL2 34
CDAUDR C614 1U/16V CDINR2 CDINR2 34
CDGND C583 1U/16V CDGND1 CDGND1 34
R351 10K
R374 20K
R363 20K
For Layout:
Place these resistors close to SmartAMC device.
REV.B
MR28 249K RC0603
RC_OSC
MU3
CX20468-31
VDD5
VDDC18
VDDC10
VDD_CLK
AVDD33
AVDD44
RCOSC1
DIB_DATAN
DIB_DATAP
PWRCLKP
PWRCLKN
SDATA_OUT
SYNC
AC_RESET#
AC_ONLY
SDATA_IN0
BIT_CLK
IDO#
ID1#
EAPD
PC_BEEP
DSPKOUT
MIC_IN
CD_IN_R
CD_IN_GND
CD_IN_L
LINE_IN_L
LINE_IN_R
LINE_OUT_L
LINE_OUT_R
HP_OUT_L
HP_OUT_R
REF_FLT
VC_SCA
VREF_SCA
MBIAS/AVDD
S_PDIF
GPIO_4
GPIO_5
XTLO
XTLI
MIC_BIAS
MIC1
CDAUDR
CDGND
CDAUDL
LINEINL_PR
LINEINR_PR
T141
T142
AMPL
AMPR
T4
T2
SPDIF
97DOCK_OK
DIB_DATAN
DIB_DATAP
DIB_PWRP
DIB_PWRN
SDOUT1
SYNC1
-CODEC_RST
MODEM_PRES
SDINA
BITCLK
SDATA_IN0
BIT_CLK0
ID0
ID1
MUTE_LED
EAPD_1
PC_BEEP
EC_MUTELED
MR27 0 RC0603
MR24 0 RC0603
MR20 0
MR19 0
MR14 33 RC0603
MR9 33 RC0603
MR17 *0
MR16 *0
MR12 330
MR8 *0
R307 *10K
MR10 *10K RC0603
MR11 *10K RC0603
MR13 *0
MC23 150P
MC20 150P
MR26 *3K
MC21 10U
MR30 10K
MR31 *10K
MC33 0.1U
MC38 0.1U
MC36 0.1U
MC40 1U
For Layout:
Place CX132, CX133, CX135, CX136 near SmartAMC device
Populate RX152 in order to enable the audio codec only feature of the SmartAMC device
MR15 33
XTLO_1
MC13 22P
MC18 22P
MY2 24.576MHZ
Ground Tie
MR7 0
For Layout:
BITCLK
REV.B
CS18 *22P
For EMI request
PC SPEAKER
+3V
C506 .1U_0603_25V
D21 1SS355
PCBEEP1
PCBEEP2
R317 *1K
C507 .47U
PC_BEEP
PCMSPK
SPK
U25 TC7SH86FU
R308 10K
C503 *1000P
R309 1K
REV.D
Place crystal and associated circuitry very near SmartAMC Device.
CX20468-21: ADD R20, MR8
REMOVE MR12, R413, D24, MR30, MR31
REV:B SETTING
CX20468-31: ADD MR12, R413, D24, MR30
REMOVE R20, MR31, MR8
CX20468-31 without software EQ:
ADD MR12, MR31, MR30
REMOVE R413, D24, MR8, R20
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20---AC97 CTRL_CONEXANT20468-31
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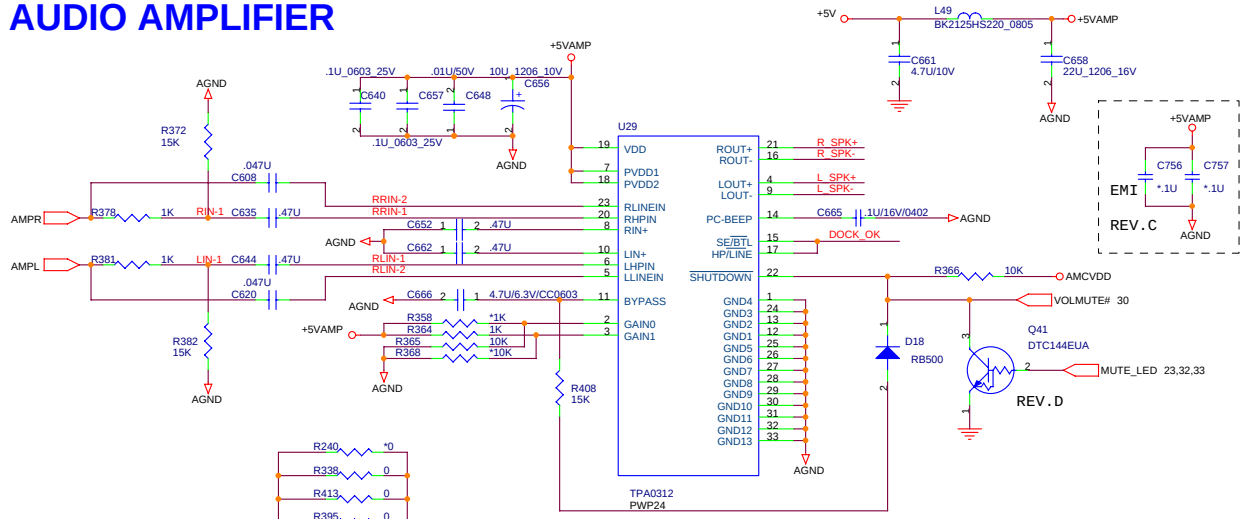
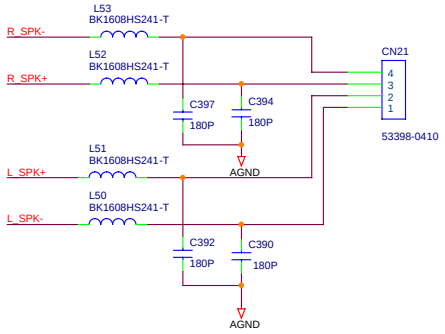
AUDIO AMPLIFIER

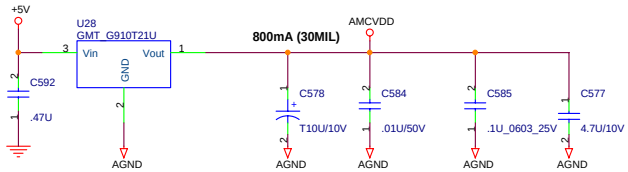


0312 Gain Table

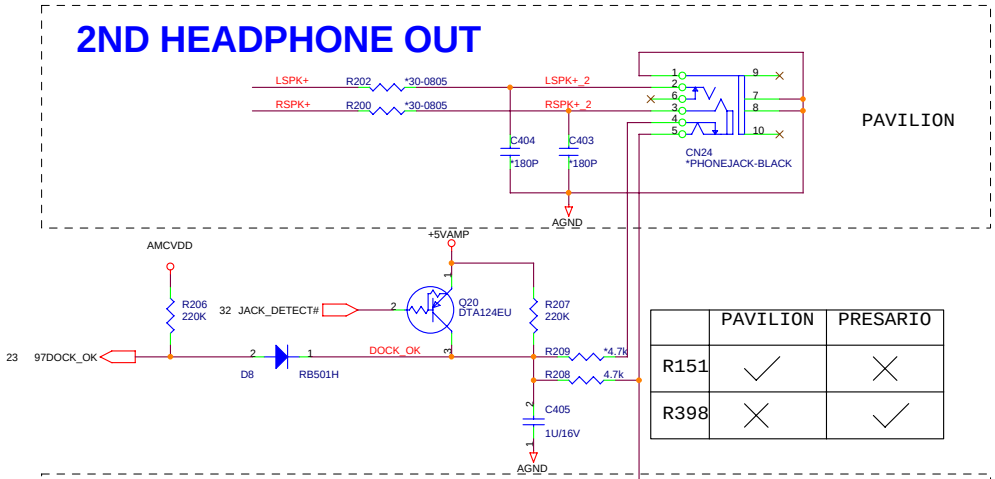
GAIN0	GAIN1	SE/BTL	AV(inv)
0	0	0	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

SPEAKER OUT



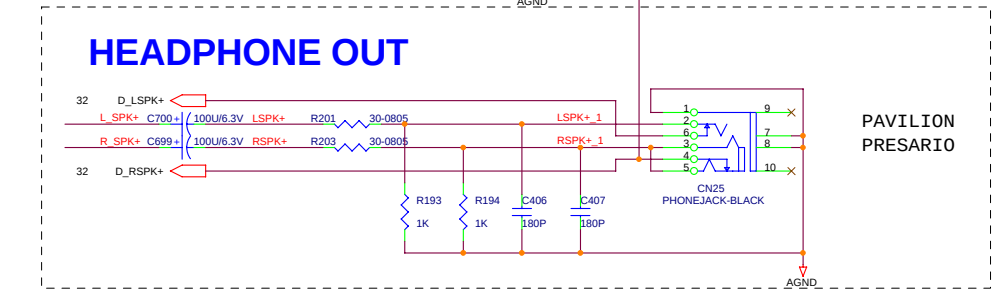


2ND HEADPHONE OUT

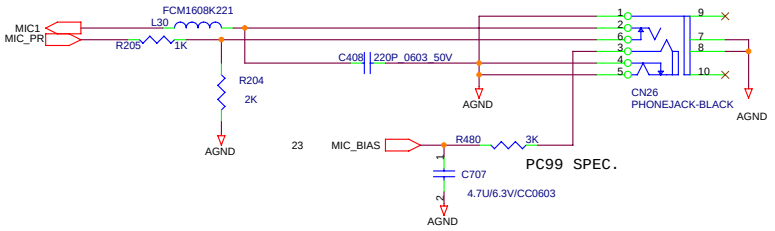


	PAVILION	PRESARIO
R151	✓	✗
R398	✗	✓

HEADPHONE OUT



MICROPHONE



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	AUDIO AMP_ TI-TPA0312	3A
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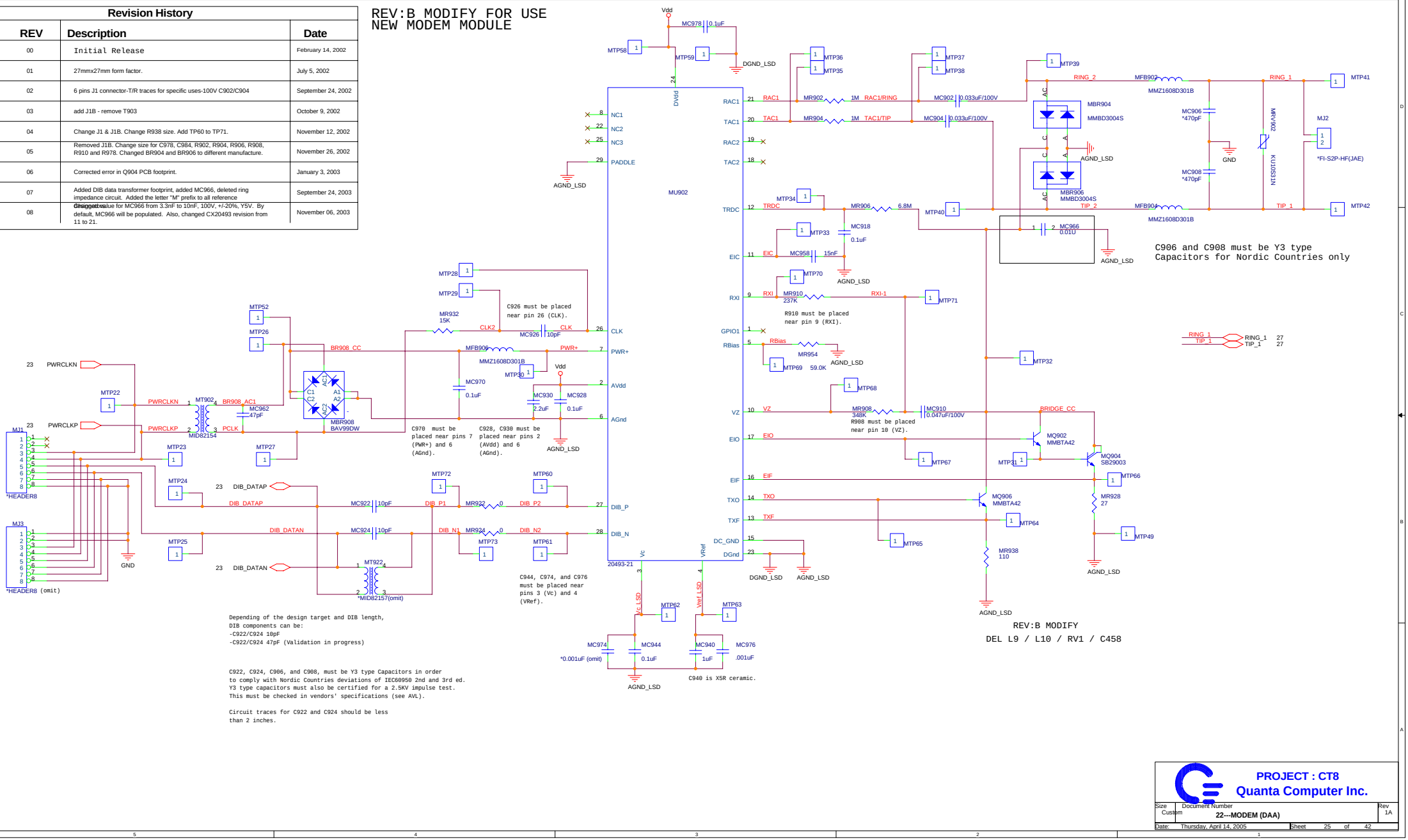
Revision History

REV	Description	Date
00	Initial Release	February 14, 2002
01	27mmx27mm form factor.	July 5, 2002
02	6 pins J1 connector-T/R traces for specific uses-100V C902/C904	September 24, 2002
03	add J1B - remove T903	October 9, 2002
04	Change J1 & J1B. Change R938 size. Add TP60 to TP71.	November 12, 2002
05	Removed J1B. Change size for C978, C984, R902, R904, R906, R908, R910 and R978. Changed BR904 and BR906 to different manufacture.	November 26, 2002
06	Corrected error in Q904 PCB footprint.	January 3, 2003
07	Added DIB data transformer footprint, added MC966, deleted ring impedance circuit. Added the letter "M" prefix to all reference designators.	September 24, 2003
08	Changed value for MC966 from 3.3nF to 10nF, 100V, +/-20%, Y5V. By default, MC966 will be populated. Also, changed CX20493 revision from 11 to 21.	November 06, 2003

REV:B MODIFY FOR USE
NEW MODEM MODULE



Depending of the design target and DIB length, DIB components can be:
-C922/C924 10pF
-C922/C924 47pF (Validation in progress)

C922, C924, C906, and C908, must be Y3 type Capacitors in order to comply with Nordic Countries deviations of IEC60950 2nd and 3rd ed. Y3 type capacitors must also be certified for a 2.5KV impulse test. This must be checked in vendors' specifications (see AVL).

Circuit traces for C922 and C924 should be less than 2 inches.

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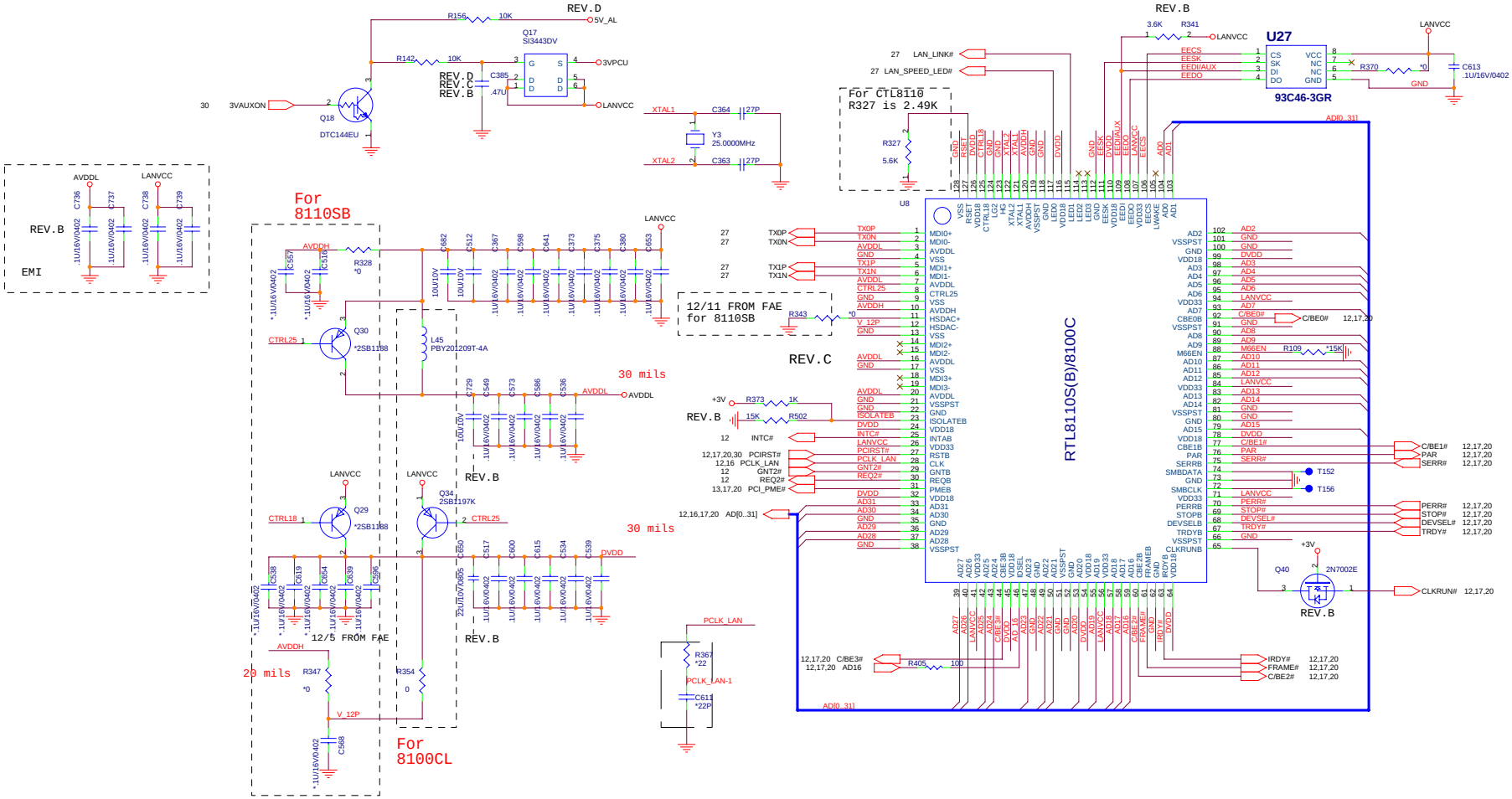
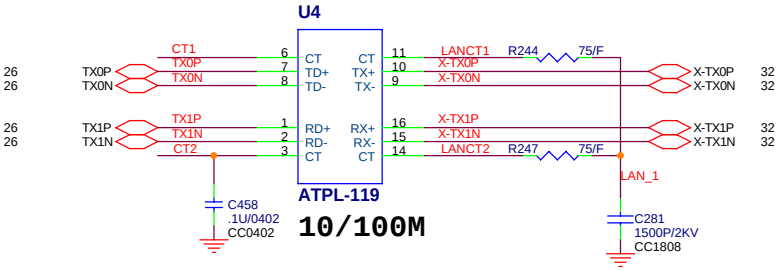
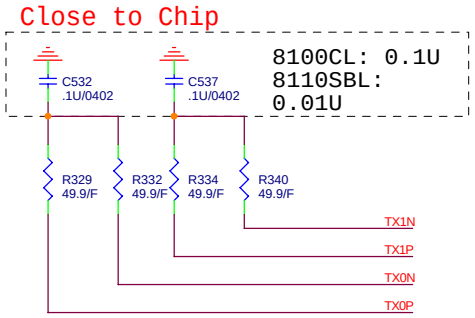
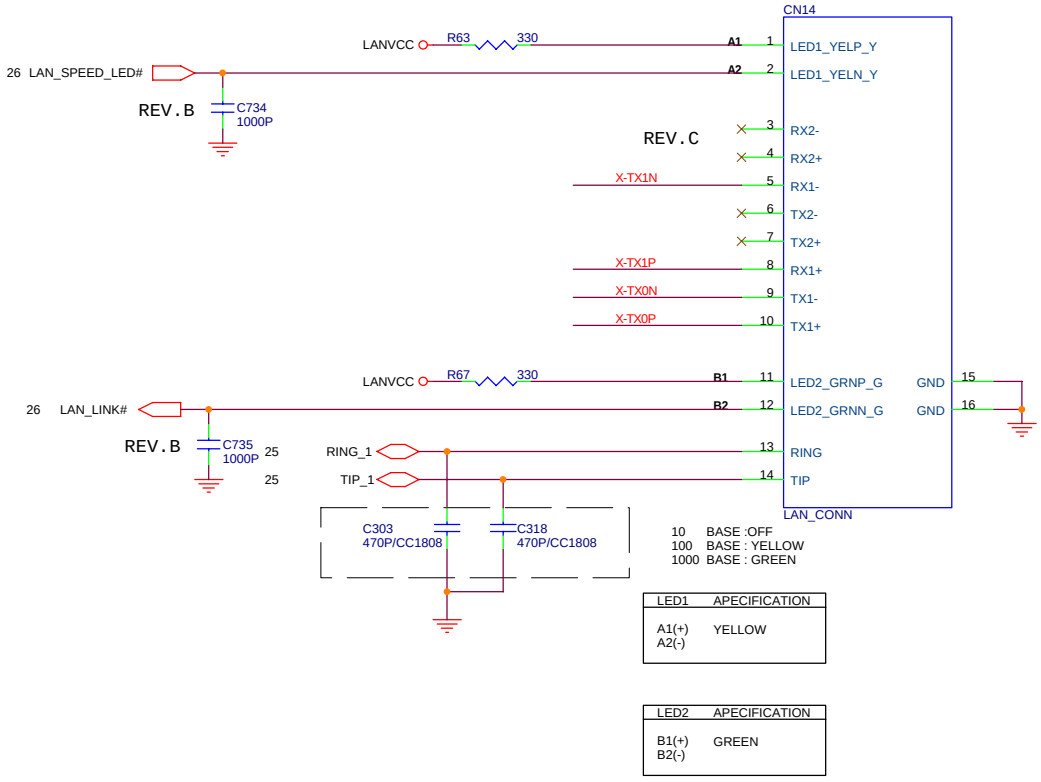
	8100CL(10/100M)	8110SB(1G)
DVDD33	3.3VD 26,41,56,71,84,94,107	3.3VD 26,41,56,71,84,94,107
AVDDL	3.3VA 3,7,20	2.5VA 3,7,20,16
DVDD	2.5VD 32,54,78,99	1.8VD 32,54,78,99,24,45,64,110,116,126
AVDD25	2.5VA 12	NC
AVDDH	NC	3.3VA 10,120









LED1	APECIFICATION
A1(+) A2(-)	YELLOW

LED2	APECIFICATION
B1(+) B2(-)	GREEN

REV.C
Del 1G circuit.

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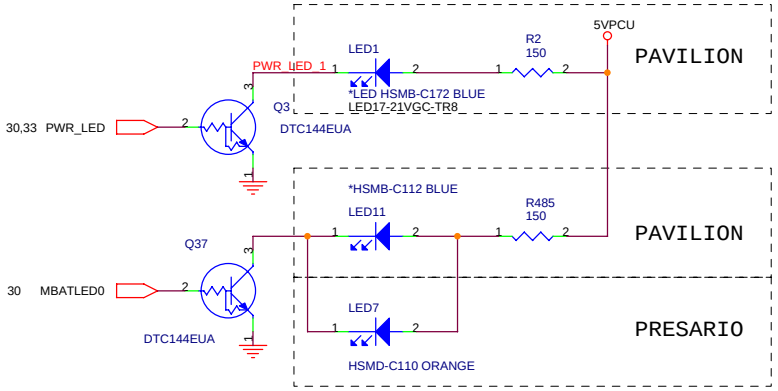
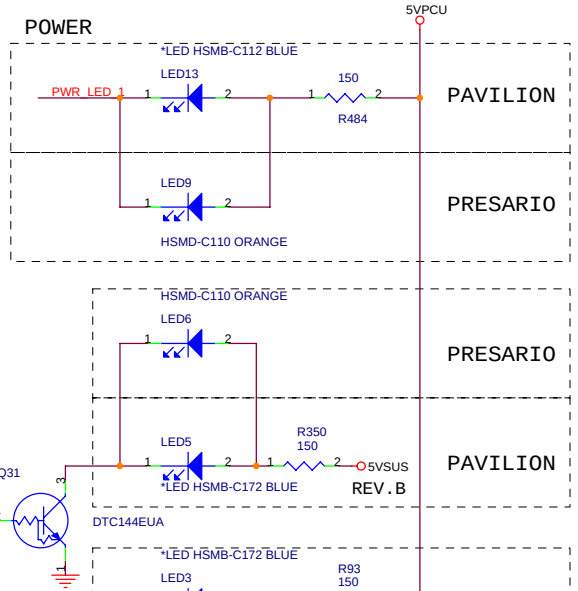
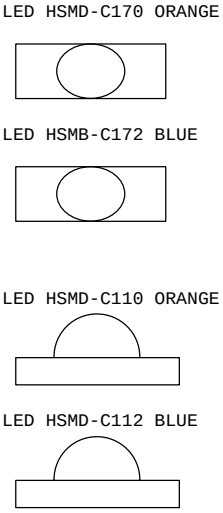
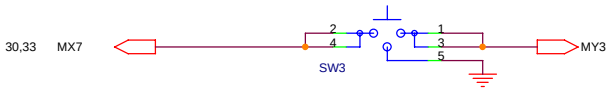
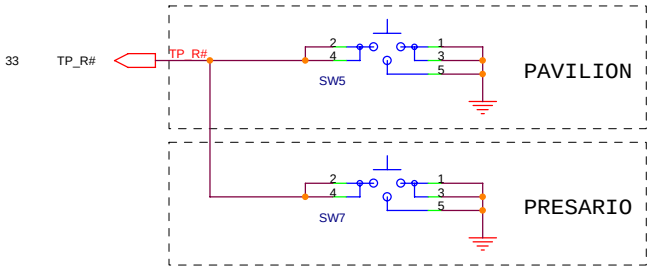


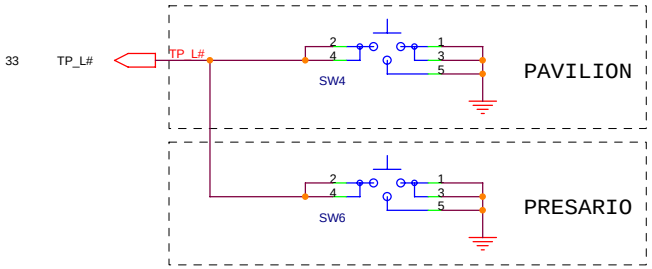


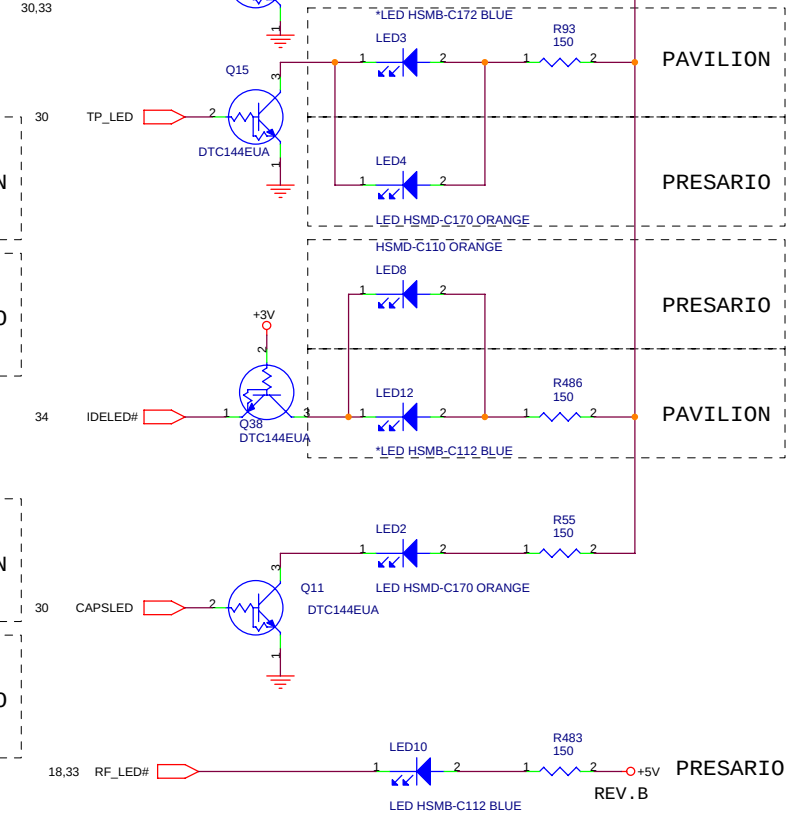


Touchpad control









REV.B: LED7 AND LED8 SWAP

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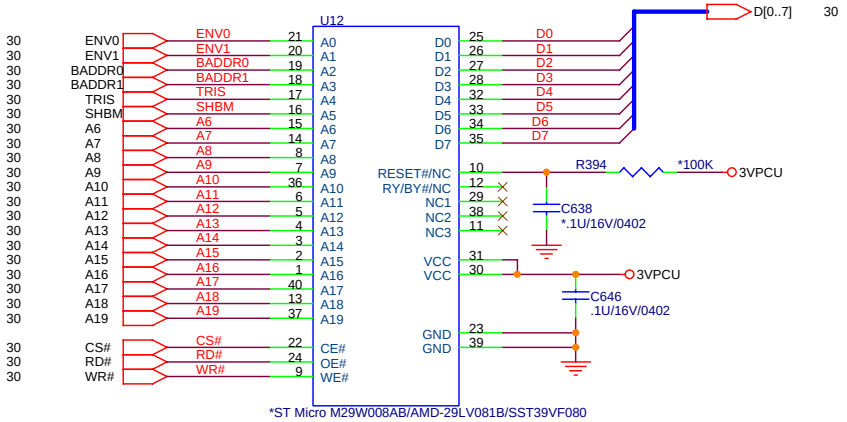
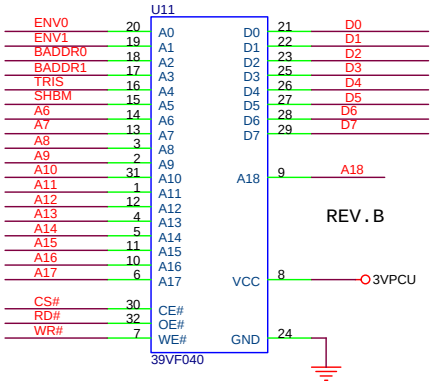
8Mbit (1M Byte), TSSOP40



AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
2.SIO has internal 20 mS delay of VCC1_PWROK

4Mbit (512k Byte), TSSOP32



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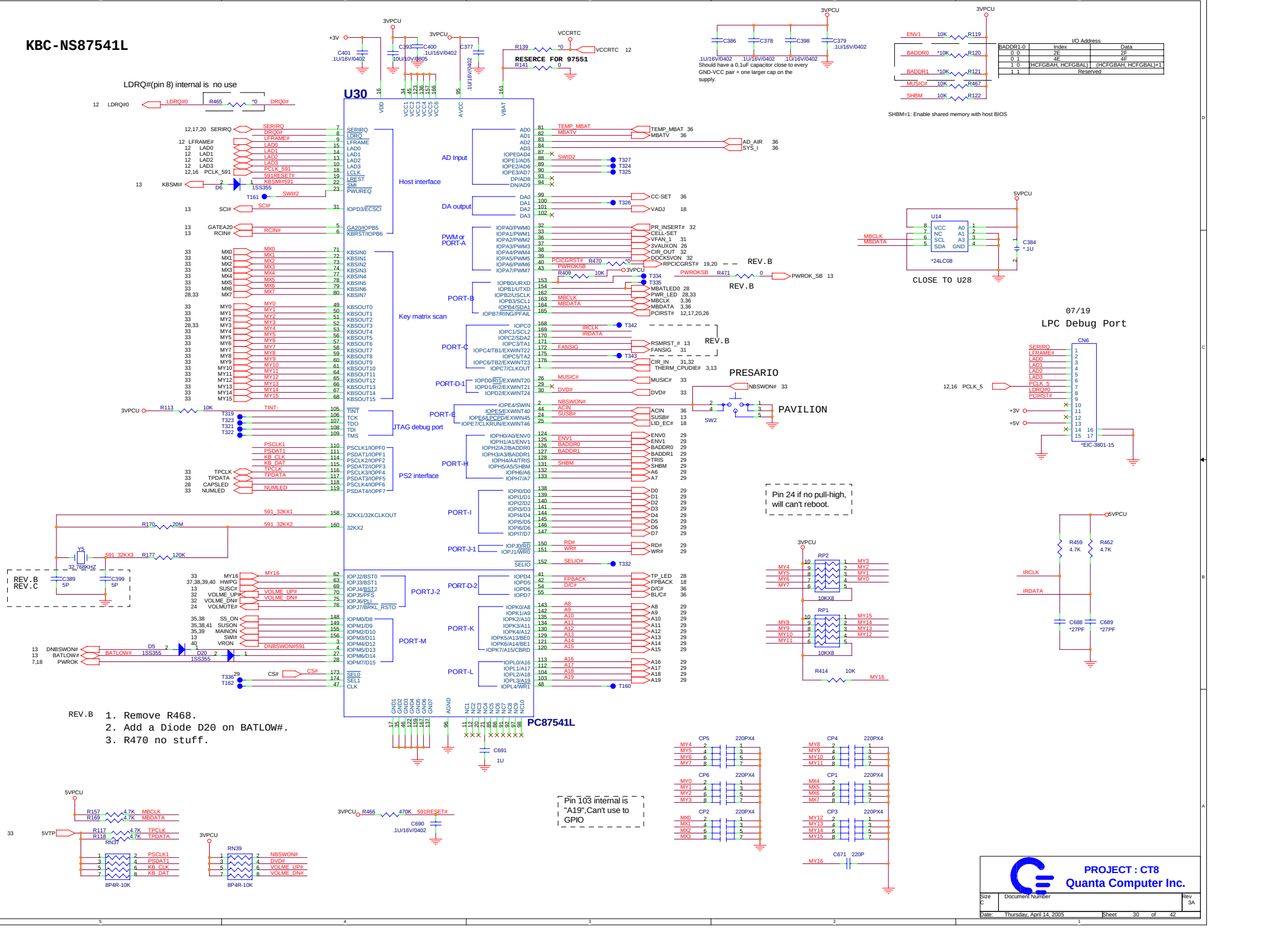
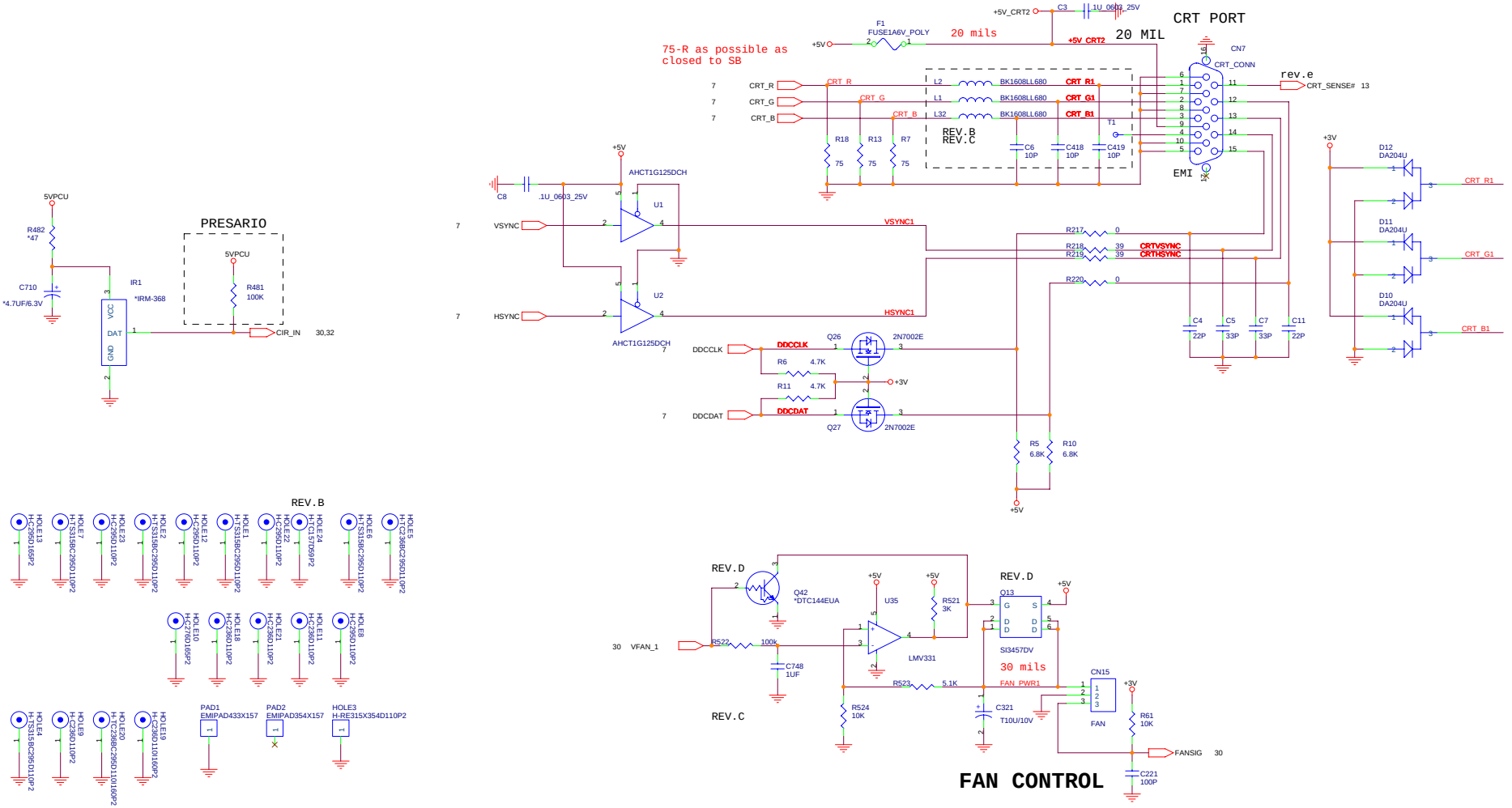
KBC-NS87541L





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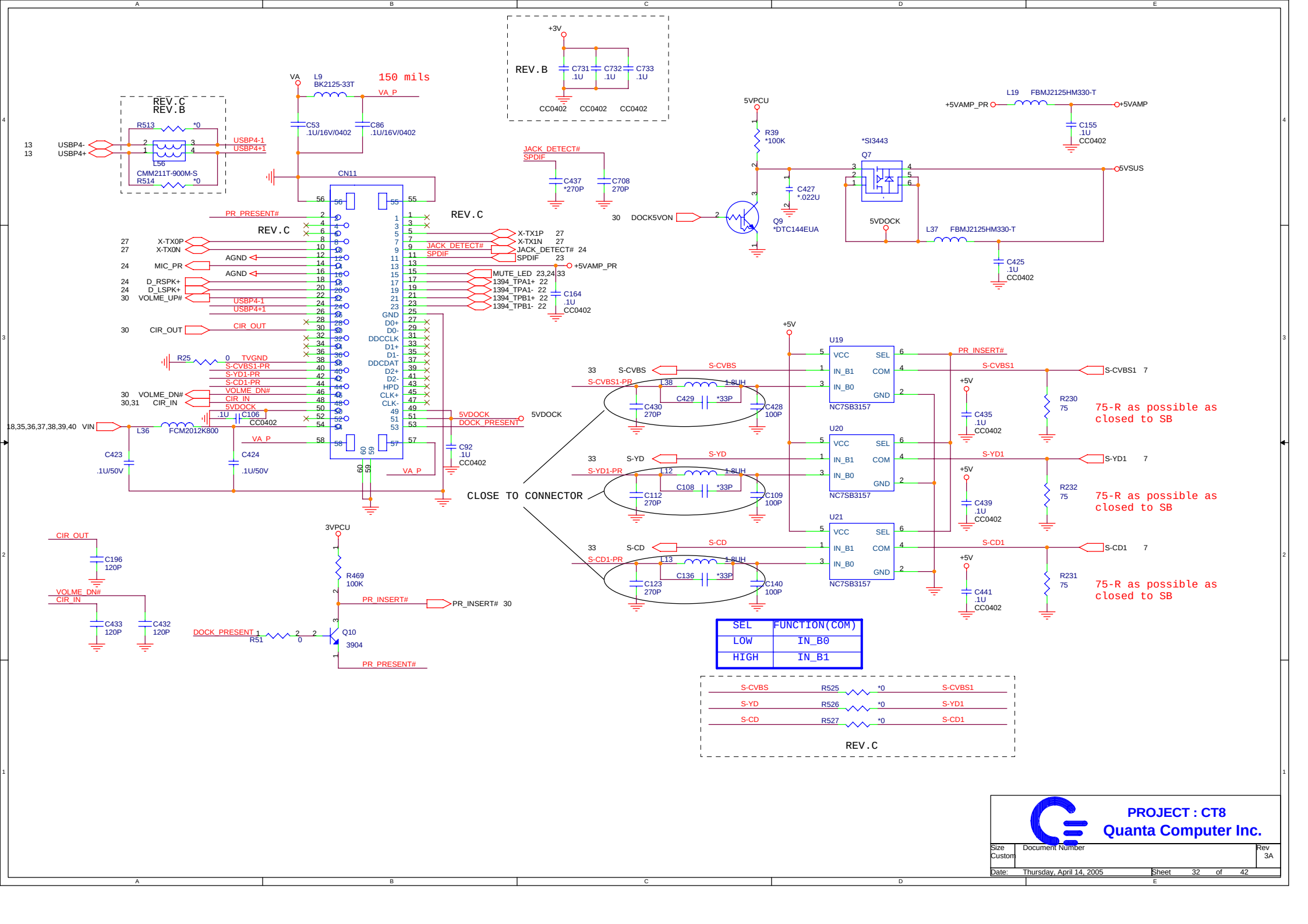

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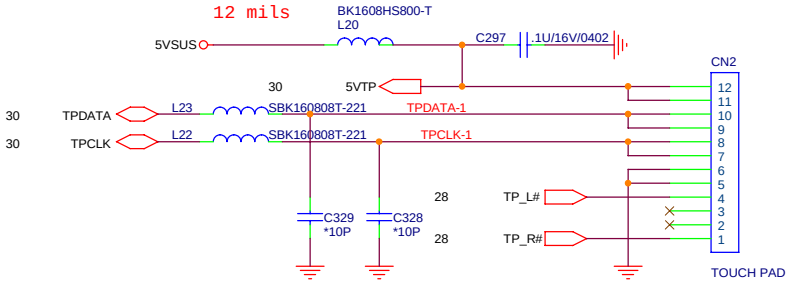
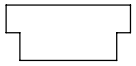
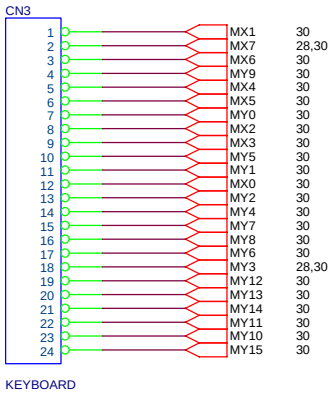
TOUCH PAD CONNECTOR

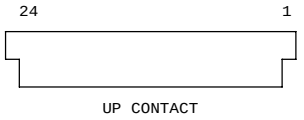




CHECK PIN DEFINE

KEYBOARD CONNECTOR



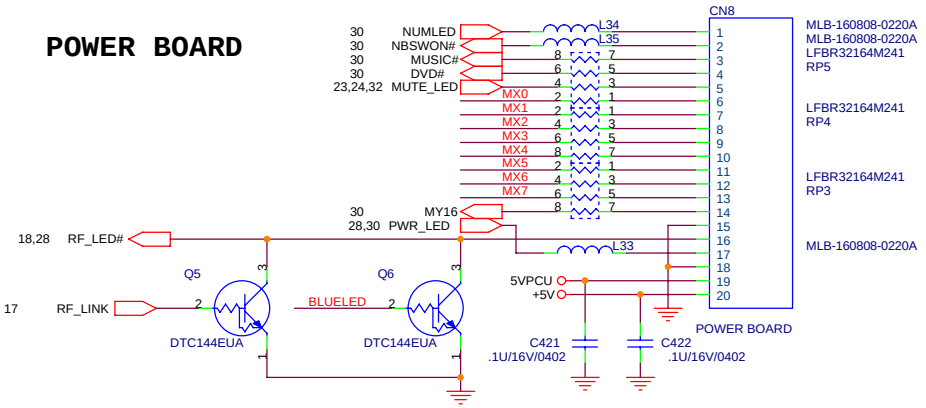


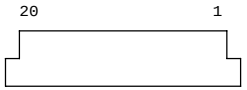
AV BOARD

REV.B

DEL CN20, C681, C677,CC673

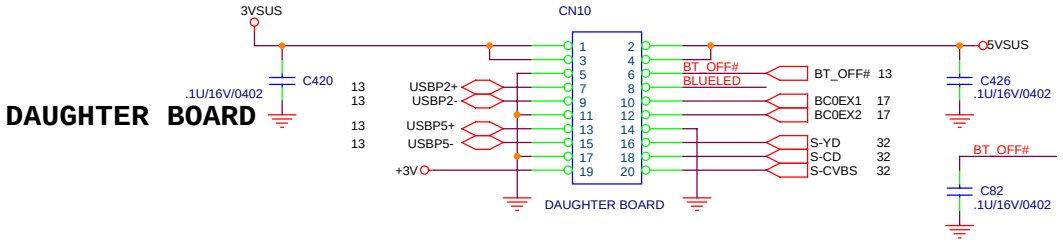
POWER BOARD

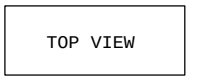




MX0	MX1	MX2	MX3	MX4	MX5	MX6	MX7
BACK	PLAY/PAUSE	FORWARE	STOP	VOL UP	MUTE	VOL DN	WIRELESS

DAUGHTER BOARD





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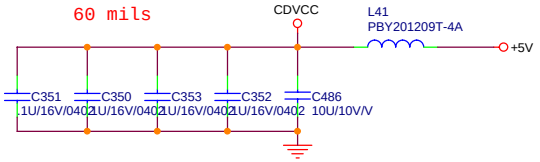
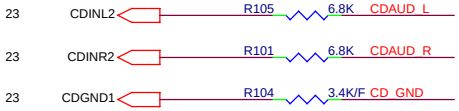
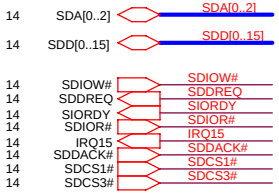
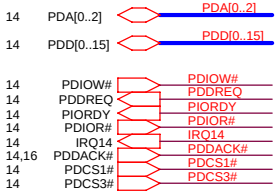
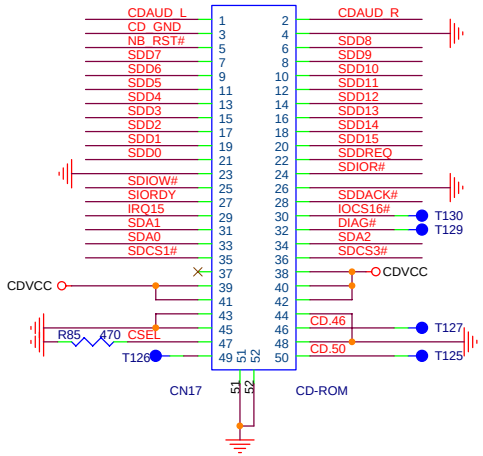
CD-ROM

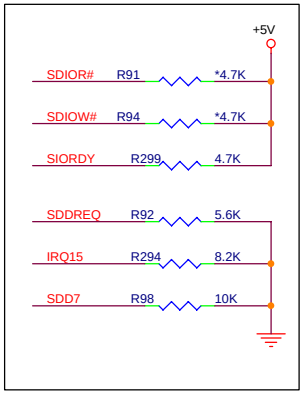


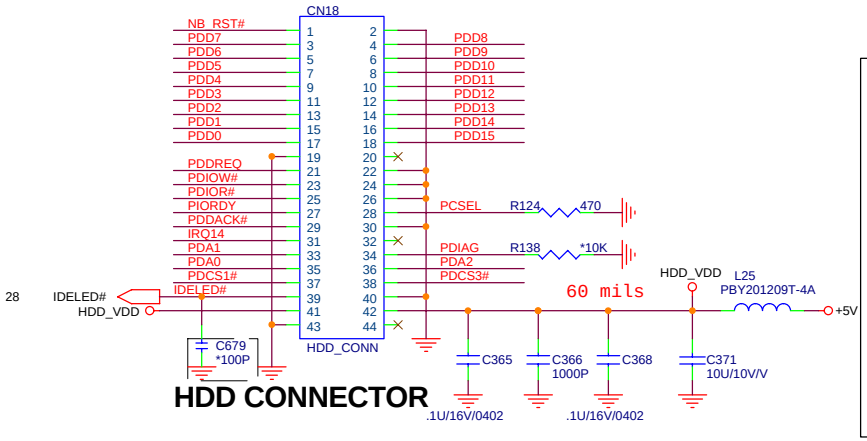




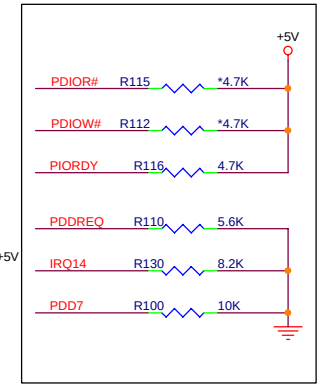








HDD CONNECTOR



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Quanta Computer Inc.

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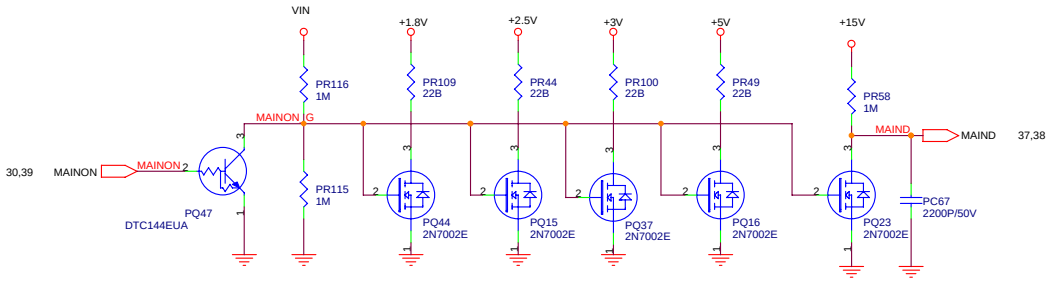

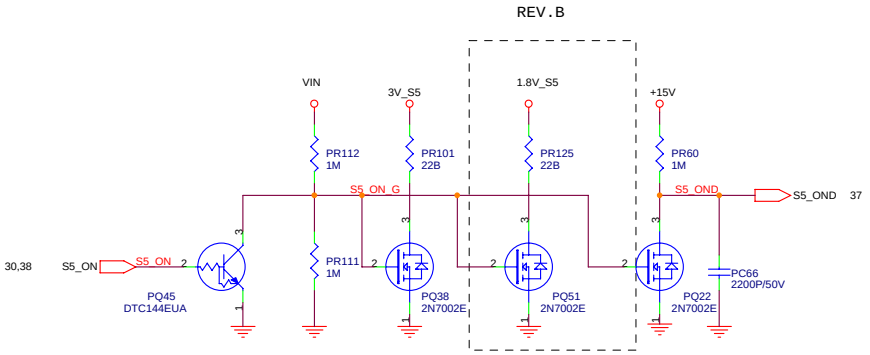

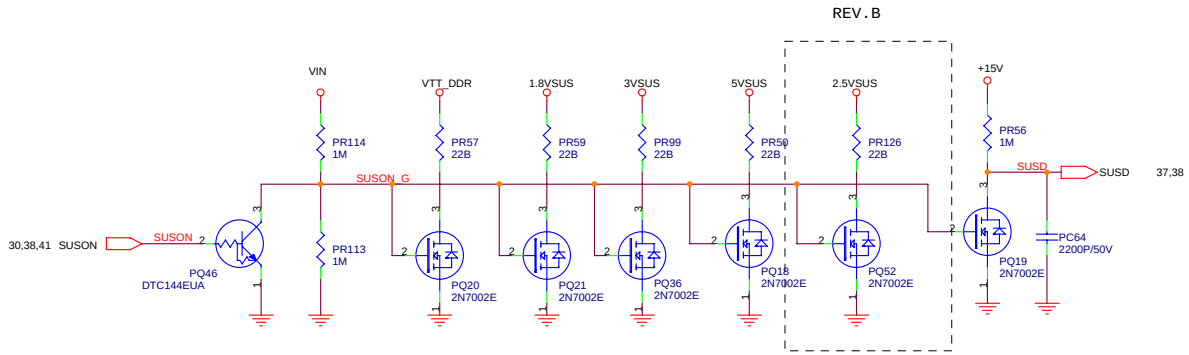

PROJECT : CT8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**30---DISCHARGE**	2A
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BATTERY CHARGER

ADAPTER 18.5V 65W 3.51A

From Docking CNN

VA — PD2 SBM1040 — PR25 10K

VA2 — PD8 SBM1040 — PR66 10K — PC73 .1U/50V

JP1 POWER JACK — PL8 FBMJ3216HS480NT(6A) — PL1 FBMJ3216HS480NT(6A) — PC75 .1U/50V

VA3 — PR63 0.033/1W/3720 — VIN

VIN — PQ24 AO4413 — PR30 200K — PR31 100K

VIN 18,32,35,37,38,39,40 — 20 MIL TO CABLE DOCK

REV.C — PQ33 AO4413

PQ10 DTA124EUA — PC47 0.47U/25V — PC37 .047U/50V

PR43 10K — PC44 .1U/50V — PR38 4.7 — PR32 4.7 — PC38 .1U/50V

PQ8 SI4814 — PC18 .1U/50V

PL4 FBMJ3216HS800 — PC16 10U/25V — PC17 10U/25V — PC19 10U/25V

PL10 15uH/4.4A/CDRH104R — PR89 0.05/1W/3720 — PR24 4.7 — PR22 4.7 — PC29 .1U/50V — PC26 .1U/50V

PC99 10U/25V — PC100 MBAT+ 10U/25V — PC98 10U/25V

ACOK — PR11 100K — PD1 CH501H-40 — PQ11 2N7002K — D/C# 30

3VPCU — PD16 SW1010C — REV.B

VIN — PR117 47.5K/F — PR118 37.4K/F

3VPCU 5VPCU 3VPCU — PU8 LMV339 — PR120 47K — PQ50 2N7002E — PR119 100K — PQ48 2N7002E — BL/C# 30

Battery Low 7.5V

1772_5.4V — PR42 33 — PD6 CH501H-40 — REV.B

CSSN — CSSP — SYS_I 30 — PR39 12.4K/F

PC32 1U/10V/X7R — CSIP — CSIN

PU1 MAX1772EEI — INP CSSP CSSN BST DHI LX DLOV DLO PGND CSIP CSIN BATT CELLS VCTL — DCIN LDO CLS REF CCS CCI CCV GND GND ICHG ACIN ACOK REFIN ICTL

10K/F — PR14 — REF4.096 — PR13 2.61K/F

1772_5.4V — PR15 100K — PR12 100K — REV.C

VA — PD3 CH501H-40 — VA2 — PD9 CH501H-40

5VPCU — PR130 100K — PQ54 2N7002K — AD_AIR 30 — REV.C

PR61 75K/F — PR41 75K/F — PR129 *0 — PR40 13.7K/F — PC145 .01U/50V — PR62 12.4K/F — REV.D ESD

PQ53 2N7002K — PD17 CH501H-40 — PR127 30 — 1M — PC144 1U/25V — REV.C

ACOK — PQ6 DTA124EUA — PR121 10K — PR122 15K — ACIN

PC101 1U/50V — PC46 1U/10V/X7R — REF4.096 — PR35 100K/F — REF4.096 — PR36 121K/F — REV.B

1772_5.4V — PR23 1K — PC36 — PC33 — PC30 — PC23 .1U/50V

3VPCU — PC22 .1U/50V — 3VPCU 12,18,26,29,30,32,37

PR17 10K — CC-SET — CC-SET 30 — CC-SET = 1.05V/A

CELL-SET

HI = LDO = 4 CELL

LOW = LDO/2 = 3 CELL

1ST_BAT_CONN — CN9 — PC25 .01U/50V — PR18 10K/F — 3VPCU

PL9 FBMJ3216HS480NT(6A) — TEMP_MBAT 30 — PC24 .01U/50V — MBAT+ — PR27 100K/F

PR19 100 — PR20 100 — MBCLK — MBCLK 3,30 — MBDATA — MBDATA 3,30

MBATV — MBATV 30 — PC31 .01U/50V — PR28 14K/F

PD5 ZD5.6V — PD4 ZD5.6V

PROJECT : CT8

Quanta Computer Inc.

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Custom	MAX1772/CHARGING	3A
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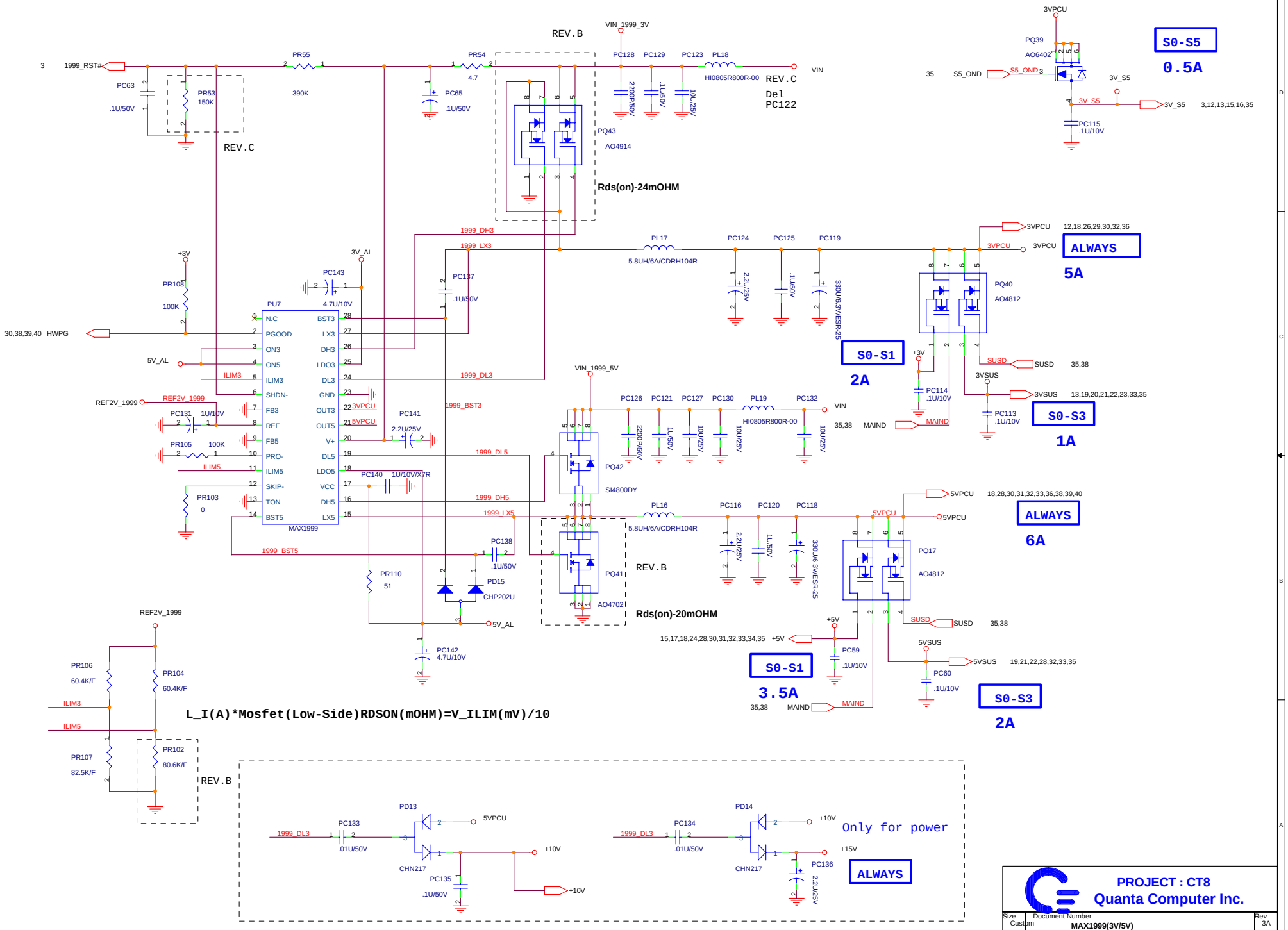
REV.B
VIN_1999_3V
PR55
390K
PR54
4.7
PC63
.1U/50V
PR53
150K
REV.C
PC65
.1U/50V
PC128
220P/50V
PC129
.1U/50V
PC123
10U/25V
PL18
HI0805R800R-00
VIN
REV.C
Del
PC122
PQ43
AO4914
Rds(on)-24mOHM
3VPCU
PQ39
AO6402
S5_OND
3V_S5
PC115
.1U/10V
S0-S5
0.5A
1999_DH3
1999_LX3
PL17
5.8UH/6A/CDRH104R
PC124
2.2U/25V
PC125
.1U/50V
PC119
330U/6.3V/ESR-25
PQ40
AO4812
ALWAYS
5A
S0-S1
2A
PC137
.1U/50V
PC143
4.7U/10V
PR108
100K
PU7
MAX1999
30,38,39,40 HWPG
5V_AL
3V_AL
REF2V_1999
PC131
1U/10V
PR105
100K
ILIM3
ILIM5
PR103
0
1999_BST3
1999_DL3
1999_DL5
1999_DH5
1999_LX5
1999_BST5
PC141
2.2U/25V
PC140
1U/10V/X7R
PC138
.1U/50V
PD15
CHP202U
PR110
51
PC142
4.7U/10V
VIN_1999_5V
PC126
220P/50V
PC121
.1U/50V
PC127
10U/25V
PC130
10U/25V
PL19
HI0805R800R-00
PC132
10U/25V
PQ42
SI4800DY
PL16
5.8UH/6A/CDRH104R
PC116
2.2U/25V
PC120
.1U/50V
PC118
330U/6.3V/ESR-25
PQ41
AO4702
REV.B
Rds(on)-20mOHM
PQ17
AO4812
PC114
.1U/10V
PC113
.1U/10V
PC59
.1U/10V
PC60
.1U/10V
S0-S3
1A
S0-S3
2A
ALWAYS
6A
S0-S1
3.5A
REF2V_1999
PR106
60.4K/F
PR104
60.4K/F
PR107
82.5K/F
PR102
80.6K/F
REV.B
L_I(A)*Mosfet(Low-Side)RDSON(mOHM)=V_ILIM(mV)/10
PD13
CHN217
PC133
.01U/50V
PC135
.1U/50V
5VPCU
+10V
PD14
CHN217
PC134
.01U/50V
PC136
2.2U/25V
+15V
Only for power
ALWAYS
PROJECT : CT8
Quanta Computer Inc.
MAX1999(3V/5V)
Size Custom
Rev 3A
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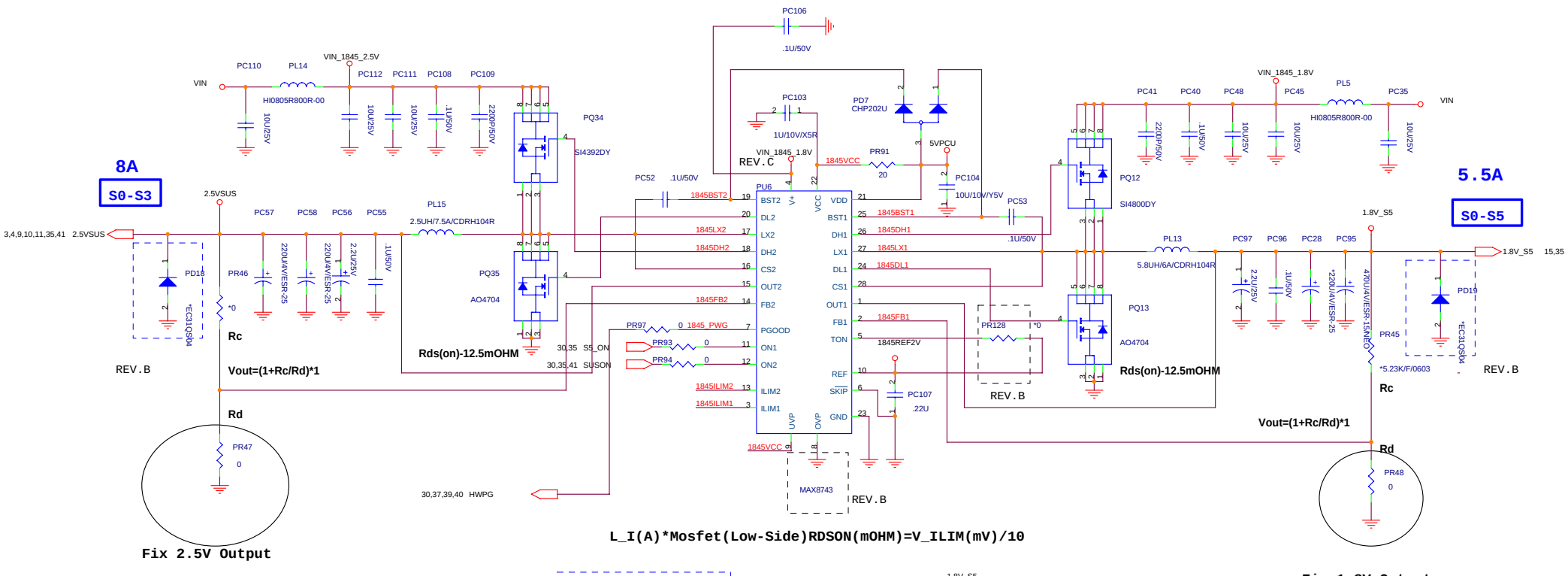
8A
S0-S3
2.5VSUS
Fix 2.5V Output
Vout=(1+Rc/Rd)*1
Rds(on)-12.5mOHM
REV.B
REV.C
MAX8743
L_I(A)*Mosfet(Low-Side)RDSON(mOHM)=V_ILIM(mV)/10
5.5A
S0-S5
1.8V_S5
Fix 1.8V Output
VIN_1845_2.5V
VIN_1845_1.8V
VIN
HI0805R800R-00
SI4392DY
SI4800DY
AO4704
5VPCU
1845VCC
1845REF2V
0.25A
S0-S1
AO6402
AO4812
+2.5V
+1.8V
1.8VSUS
0.2A
S0-S3
PROJECT : CT8
Quanta Computer Inc.
Size Custom
Document Number MAX1845(2.5VSUS/1.5V_S5)
Rev 3A
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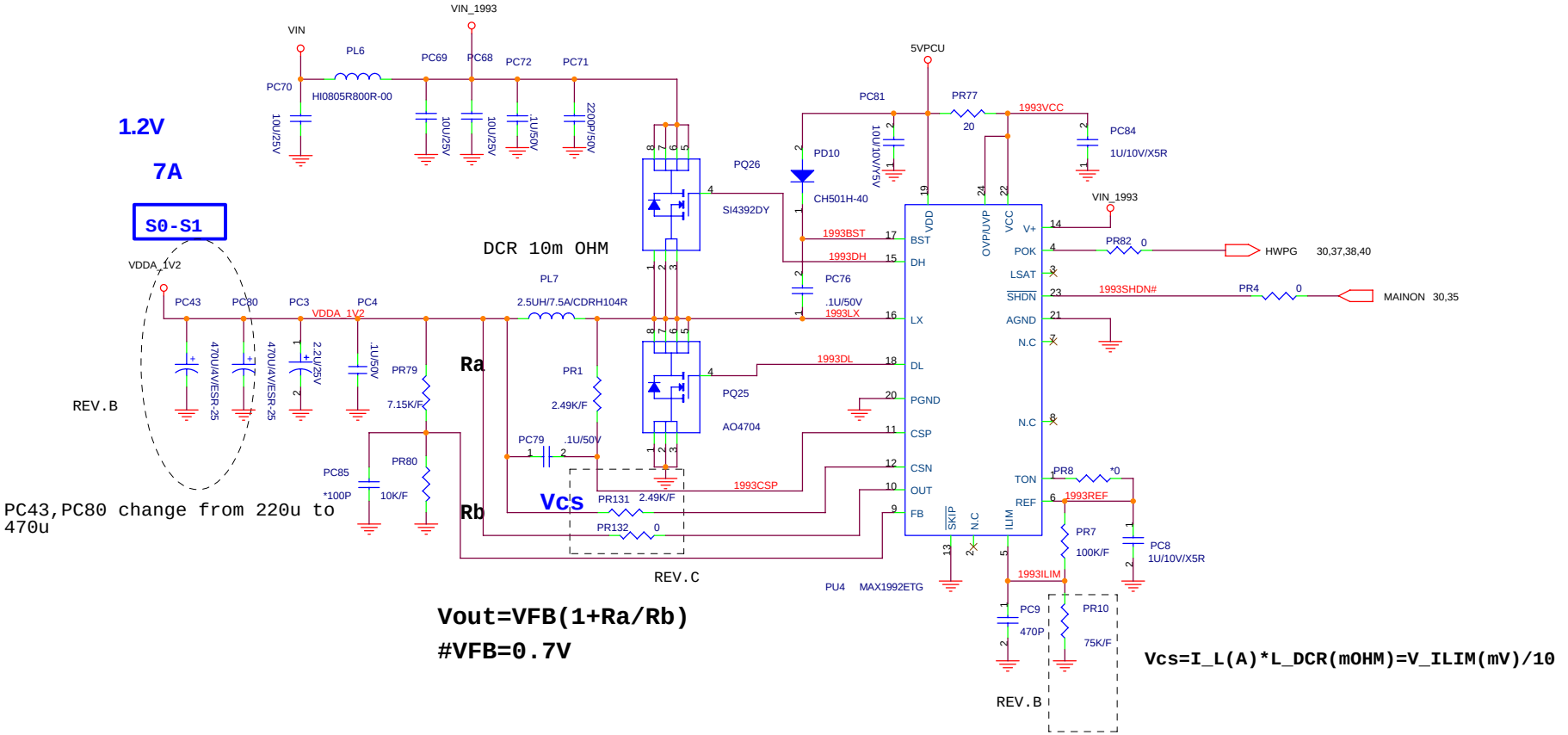

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Quanta Computer Inc.

Size	Document Number	Rev
A3	MAX1993/VCC_NB	3A
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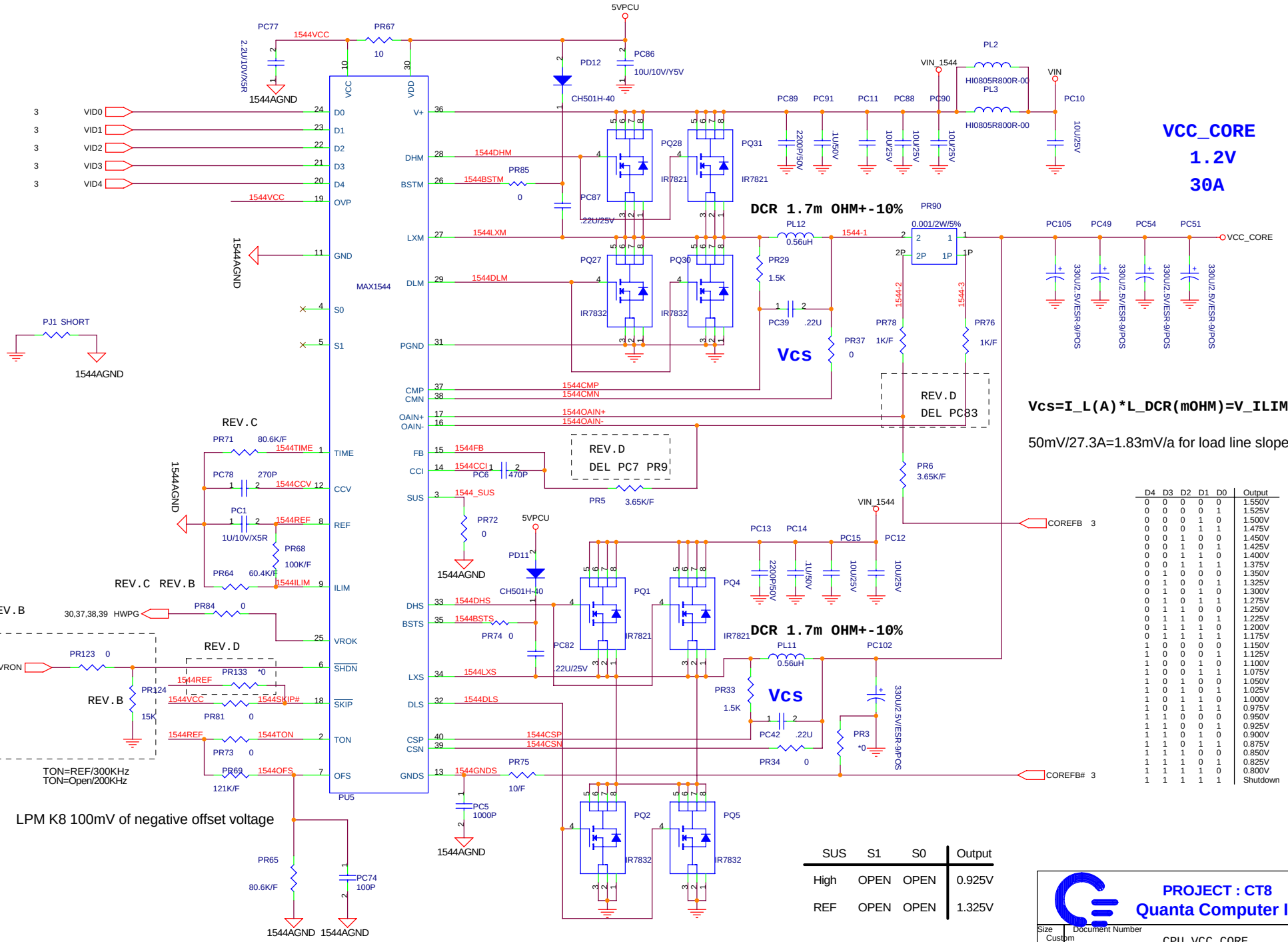
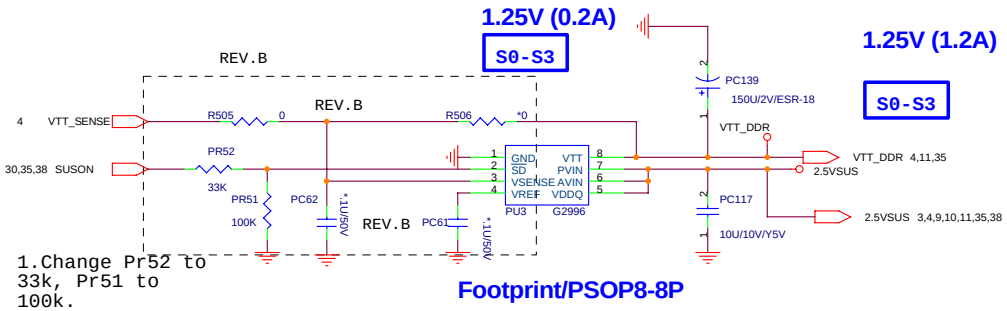


SUS	S1	S0	Output
High	OPEN	OPEN	0.925V
REF	OPEN	OPEN	1.325V

D4	D3	D2	D1	D0	Output
0	0	0	0	0	1.550V
0	0	0	0	1	1.525V
0	0	0	1	0	1.500V
0	0	0	1	1	1.475V
0	0	1	0	0	1.450V
0	0	1	0	1	1.425V
0	0	1	1	0	1.400V
0	0	1	1	1	1.375V
0	1	0	0	0	1.350V
0	1	0	0	1	1.325V
0	1	0	1	0	1.300V
0	1	0	1	1	1.275V
0	1	1	0	0	1.250V
0	1	1	0	1	1.225V
0	1	1	1	0	1.200V
0	1	1	1	1	1.175V
1	0	0	0	0	1.150V
1	0	0	0	1	1.125V
1	0	0	1	0	1.100V
1	0	0	1	1	1.075V
1	0	1	0	0	1.050V
1	0	1	0	1	1.025V
1	0	1	1	0	1.000V
1	0	1	1	1	0.975V
1	1	0	0	0	0.950V
1	1	0	0	1	0.925V
1	1	0	1	0	0.900V
1	1	0	1	1	0.875V
1	1	1	0	0	0.850V
1	1	1	0	1	0.825V
1	1	1	1	0	0.800V
1	1	1	1	1	Shutdown



1.Change Pr52 to 33k, Pr51 to 100k.
2.PC61,PC62 no stuff.

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Size	Document Number	Rev
Custom	VTT_DDR/VDDA_1V2	2A
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MODEL	REV	CHANGE LIST
CT8 M/B	1A	First Release
	2A	PAGE 2 : 1. C330, C479 CHANGE VALUE FROM 33p TO 27p for meet 35ppm. 2. DEL R84 0ohm (don't need reserve). PAGE 3 : 1. ADD CON1 HDT CONNECTOR for AMD requirement. 2. ADD C721 100P、C722 4.7U, C723 3300P、C724 0.22U for high frequency decoupling. 3. Remove R386,Q33, connect U18 pin 6 to TEMP_ALARM# (no need level shift). 4. Change C311 from 10u to 100u and remove C304, that ensures VDD to VDDA power down sequence is met. 5. Add c154,c283,c284,c285 4.7u、c9,c277 100u change to 220u for VDDA_1V2 power noise. PAGE 4 : 1. C148, C163 VALUE CHANGE FROM 330U TO 220U for Mechanic interference. 2. C225, C243, C267 PART NUMBER CHANGE TO CH733LM8812 for Mechanic interference. PAGE 5 : 1. R16 VALUE CHANGE FROM 10K TO 8.5K for ATI requirement. PAGE 7 : 1. ADD C711~C720, C745~C747 0.1U FOR EMI 2. DEL R19, CHANGE R17 VALUE TO 4.7K PULL +1.8V for side-port memory is not used. 3. DEL Y1 CIRCUIT because no need reserve is ATI requirement. 4. ADD C740、C741 FOR EMI 5. CHANGE NET NAME FROM PWROK_NB TO PWROK for meet ATI power OK sequence. PAGE 8 : 1. ADD L55 for VDDA_1V2 frequency decoupling. 2. L15,L55 TI201209G121 CHANGE TO FBMJ2125HM330-T. PAGE11 : 1. C280 VALUE CHANGE FROM 330U TO 220U for Mechanic interference. PAGE12 : 1. DEL R129、C391、C382、U9、D3, because no need reserve is ATI requirement. 2. Remove Rtc charge circuit Q16, R133, R137, R140. because RTC battery is not support charge function. 3. C387、C388 CHANGE VALUE FROM 12p TO 18p for meet 10ppm SPEC. 4. ADD RN40、RN41, R520 for PCI command signal pull high. PAGE13 : 1. CHANGE R99 for blue tooth on/off and R318 for wire less on/off function. 2. DEL R401、C668, R400 for ATI power OK sequence. 3. DEL R161 0ohm for BITCLK. 4. ADD R503、R504 FOR F/F AND D/F. 5. CHANGE R147 PULL HIGH FROM 3V_S5 TO +3V for leakage current. and R446 contact to BITCLK because change net name. PAGE15 : 1. Del C642 for meet IXP power on sequence. PAGE16 : 1. Del R444 10K, Add R445 10K for ATI USB clock from outside. PAGE17 : 1. DEL R175, Q19 and CN22 PIN34 CONNECT TO PCI_PME#. because no need LANVCC to control PME signal. 2. Del R196, C402, no need reserve. PAGE18 : 1. CHANGE R213 SIGNAL to PWROK and DEL Q21, Q22, Q24, R210for ATI LCD back light bug. 2. Reserve R215 1K PULL DOWN. 3. ADD R507、C730、R508、D19 for ATI LCD back light bug. PAGE19 : 1. DEL PC11510 CIRCUIT AND PARTS. 2. ADD C743 for tune clock waveform. PAGE20 : 1. R402 stuff for PCI reset timing. 2. Remove R392, Q36 and U26 pin T3 connect to PCI_PME# for PME timing. 3. Add R515, C742 circuit on CLK48M for tune clock waveform. 4. Change R407 to 4.7k for limit current. 5. Change L48 to 0 ohm for EMI PAGE21 : 1. ADD R494 22ohm AND Q39 2N7002E for VCC_XD discharge. 2. CHANGE R487, R488, R490, R491, R492, R493, R495, R496, R497, R498, R499 VALUR FROM 0 TO 22 for signal waveform.. 3. ADD R516, R517, R518 for TI requirement. 4. Remove R397, D16, R489. 5. Add a Quick Switch U34 to isolate clock. 6. Change R501 to 0 ohm. 7. CN5 pin 35、43 connect to the same net. 8. C725~C728 0.1U for power noise. PAGE22 : 1. C484 VALUE CHANGE FROM 100U TO 150U for USB power meet SPEC. 2. ADD R509、R510、R511、R512 FOR EMI. PAGE23 : 1. MC13、MC18 CHANGE VALUE FROM 33p TO 22p for tune clock range. 2. CHANGE MR24, MR27 FROM 1K TO 0ohm for Conexant requirement. 3. ADD SPDIF. 4. Del MR26 for meet PC99 SPEC. 5. Del C518 for tune BITCLK waveform.. PAGE26 : 1. ADD R502 15K pull low for tune ISOLATEB voltage. 2. R341 change 4.7K to 3.6K for REALTEK recommend. 3. Add C729 10u and C650 change value from 10u to 22u for REALTEK recommend. 4. Change C385 from 2200p to 3300p for tune 3VPCU drop level. 5. Add C736、C737、C738、C739 for EMI. 6. DEL R134 no need reserve, ADD Q40 for leakage current. PAGE27 : 1. ADD C734、C735 1000P FOR EMI. 2. DEL R246, R249 for 1G LAN. PAGE28 : 1. R483 change signal from 5VPCU to +5V and R350 pull 5VSUS for leakage current. PAGE29 : 1. U11 change package to TSSOP32 for Mechanic interference. PAGE30 : 1. C389 8p, C399 5.6p change value to 15p for clock tolerance. 2. Del signal BT_OFF#, RF_OFF# for HP implement guide. 3. ADD R471 and DEL R468、R470 for ATI power OK sequence. 4. Add D20 for EC leakage current. PAGE31 : 1. ADD HOLE24, AND D21、C744 BOM NO STUFF for tune FAN clock. 2. CHANGE L1, L2, L32 to BK1608LL121、C6、C418, C419 TO 10P for CRT timing. PAGE32 : 1. ADD R513, R514 2、C731、C732、C733 FOR EMI. PAGE33 : 1. DEL CN20, C681, C677,CC673 because no need AV function. PAGE35 : 1. ADD PR126、PR125、PQ51、PQ52 for 2.5VSUS and 1.8V_S5 discharge circuit. PAGE36 : 1. CHANGE PQ24 FROM SI4425 TO AO4407, CHANGE PQ33 FROM AO4411 TO AO4407, CHANGE PR36 FROM 130K TO 121K, PQ11 CHANGE TO 2N7002K, PD6 CHANGE TO CH501H-40. and add PQ53, PD17, PR127, PC144 for prevent AC discharge MOSFET damage when adapter over watt. 2. Change PD16 bypass from 3VPCU to 3VPCU. PAGE37 : 1. CHANGE PQ41 FROM AO4704 TO AO4702, CHANGE PR102 FROM 47.5K TO 80.6K, CHANGE PQ43 FROM SI4834 TO AO4914 for Modify 5VPCU OCP point. PAGE38 : 1. Change PWM IC from MAX1845 to MAX8743 to avoid negative voltage.Modify 2.5VSUS, 1.8V_S5 OCP point. 2. ADD PR128 NO STUFF for adjust work frequency. PAGE39 : 1. CHANGE PR10 FROM 60.4K TO 75K for Change VCCA_1V2 OCP point. 2. PC43,PC80 change from 220u to 470u PAGE40 : 1. ADD PR124 15K. DEL PR70, PC2 for VR_ON signal add pull down resistor. 2. Change PR64 from 37.4k to 49.9k for update over current from 32A to 39A. PAGE41 : 1. ADD R505, R506 and Change VSENSE from VTT_DDR to CPU VTT_SENSE 2. Change PR52 to 33k, PR51 to 100k for timing. 3. PC61,PC62 no stuff.
	3A	PAGE 2 : 1. Add CAP C749, C750 0.1u for EMI. PAGE 3 : 1. Modify C311 component. PAGE 5 : 1. Change R16 to 8.25k/F and R12 to 82.5 ohm for A-link drive. PAGE 7 : 1. Del C740 for VGA Clock waveform. 2. L17 change from bead to 150ohm for ATI VCO issue(PA_RS480L1). PAGE12 : 1. Add D3 for meet SVTP SPEC. 2. Change C674, C675、C676, C683 value from 15p to 33p for EMI. 3. C358, C359, C360, C361 change value from 0.1u to 0.01u for ATI PA_IXP400AC11. PAGE13 : 1. R503 change pull up source from 3VPCU to +3V for real power plane. PAGE17 : 1. CN22 pin15 pull down for customer request. PAGE18 : 1. Change C730 from 3300p to 0.1u for power drop. PAGE20 : 1. Add R529、R530 2.7K pull down for option FF and DF. 2. Reserve C754、C755 for EMI. 3. Change C742 to 22p for waveform quality. PAGE21 : 1. Add C758~C761 0.1u for bypass noise. 2. Change R501 from 3.3K to 0 for signal level. 3. Add R500, R531, U36 for signal driving. 4. Change R518, R519 to 2.2K for signal level. PAGE22 : 1. change CN19, CN23, CN16 footprint for new part. PAGE24 : 1. reserve C751, C752, C753, C756, C757 0.1u for EMI. PAGE26 : 1. Del 1G signal. 2. Change C385 from 3300p to 0.1u for power drop. PAGE27 : 1. Del 1G circuit, because no support 1G function. PAGE30 : 1. C89, C390 change value from 15p to 5p for frequency tolerance. PAGE31 : 1. Modify FAN circuit for diminish electronic magnetic noice. 2. Change L1, L2, L32 to BK1608LL680 for CRT waveform can meet SPEC. PAGE32 : 1. Del 1G signal. 2. Add R525、R526, R527 0ohm for option FF or DF TV. 3. Add common choke for USB. PAGE36 : 1. Change PC47 to 0.47U,PC37 to 0.047U for reduce Adapter in inrush current. 2. Del PQ49 for fix 3 CELL battery and cost down. 3. Change PQ53 for 2N7002K for ESD protect. 4. Add PR130,PQ54 for delay AD_AIR signal to EC After 3VPCU ready. PAGE37 : 1. Change PR53 to 150K for Meet MAX1999 SHDN signal input trip Max level. 2. Del PC122 for meddle mechanic. PAGE38 : 1. Modify VIN_1845_1.8V signal, because that is single net. PAGE39 : 1. Add PR132 0 ohm,PR131 2.49K/F for reserve debug. PAGE40 : 1. Change PR64 to 60.4K Modify CPU over current protect point. 2. Change PR71 to 80.6K for Modify CPU power slew rate
	3B	PAGE 3 : 1. Add C762~C767 0.1u for ESD. PAGE 7 : 1. Change C740 value from 1000p to 330p for ESD. PAGE13 : 1. Modify BT_OFF# from GPIO1 to GPM3 for keep status in S3. 2. Add R533、R534 10k pull low for M/B ID. PAGE18 : 1. Change R216 power source from +3V to 5VPCU and change C730 value to .47u for glitch. PAGE19 : 1. Change R342 value from 33ohm to 15ohm for meet PCMCIA SPEC timing. PAGE23 : 1. Add D21 1ss355 and change R309 value from 2.2k to 1k for eliminate GPRS card noise. 2. Del R317 for GPRS noise. PAGE24 : 1. Add Q41 DTC144EU for GPRS noise. PAGE26 : 1. Change R156 power source from 3VPCU to 5V_AL and change C385 value from .1u to .47u for power glitch. PAGE31 : 1. Add Q43 (no stuff) DTC144EU and Q13 SI3457 for FAN driver. PAGE36 : 1. Add PC145 .01u for ESD. PAGE40 : 1. Add PR133 (No stuff) for power saving. 2. Del PC7, PR9, PC83 for ESD.

Model	CT8 Mother Board	
Page	FROM	TO
1	1A	
2	3A	
3	3A	3B
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10	1A	
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14	1A	
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17	3A	
18	3A	3B
19	2A	3B
20	3A	
21	3A	
22	3A	
23	2A	3B
24	3A	3B
25	1A	
26	3A	3B
27	3A	
28	2A	
29	2A	
30	3A	
31	3A	3B
32	3A	
33	2A	
34	1A	
35	2A	
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40	3A	3B
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