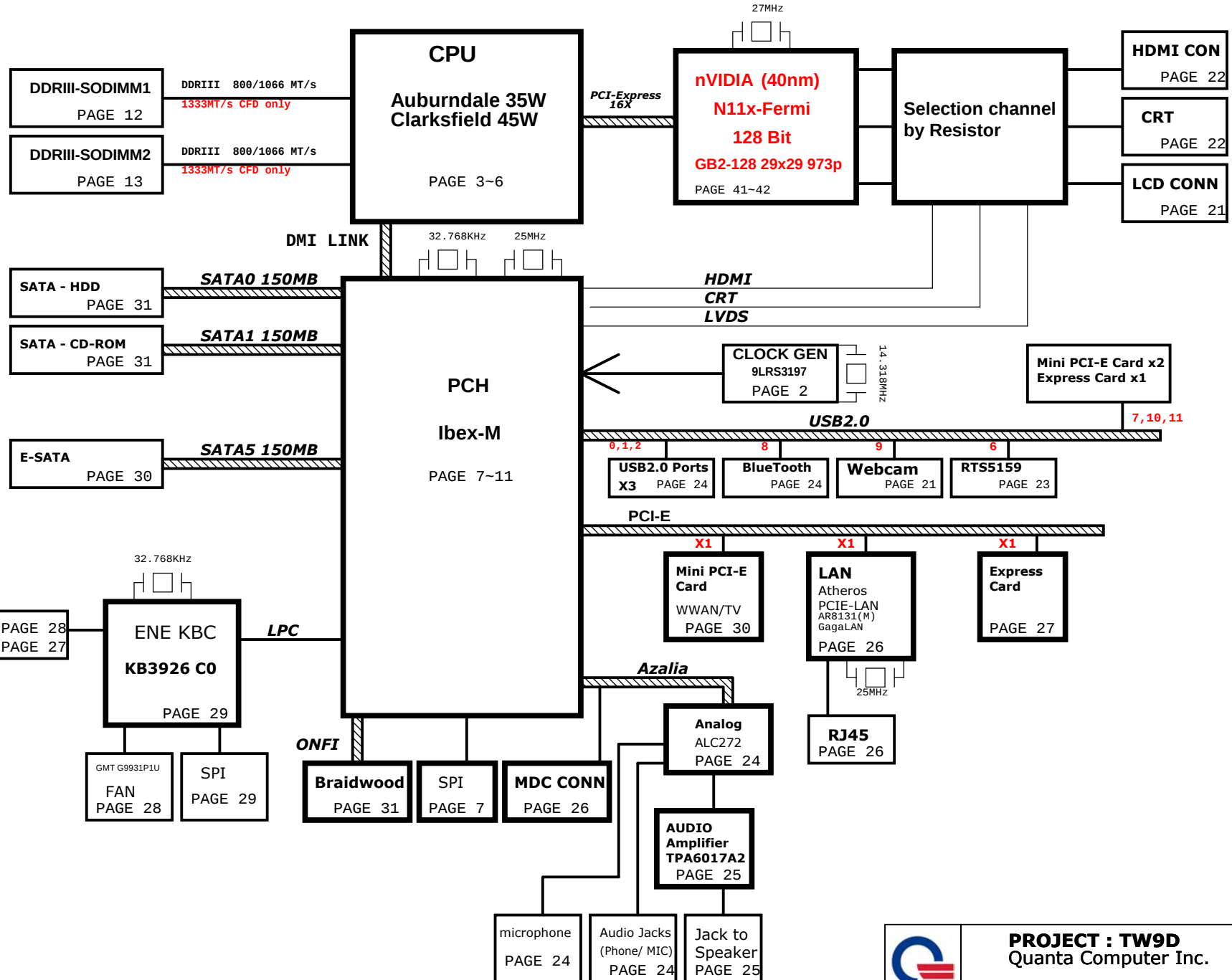
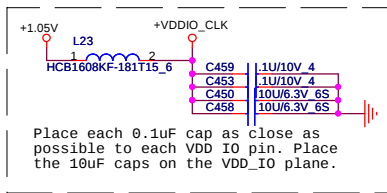


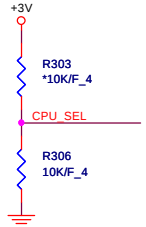
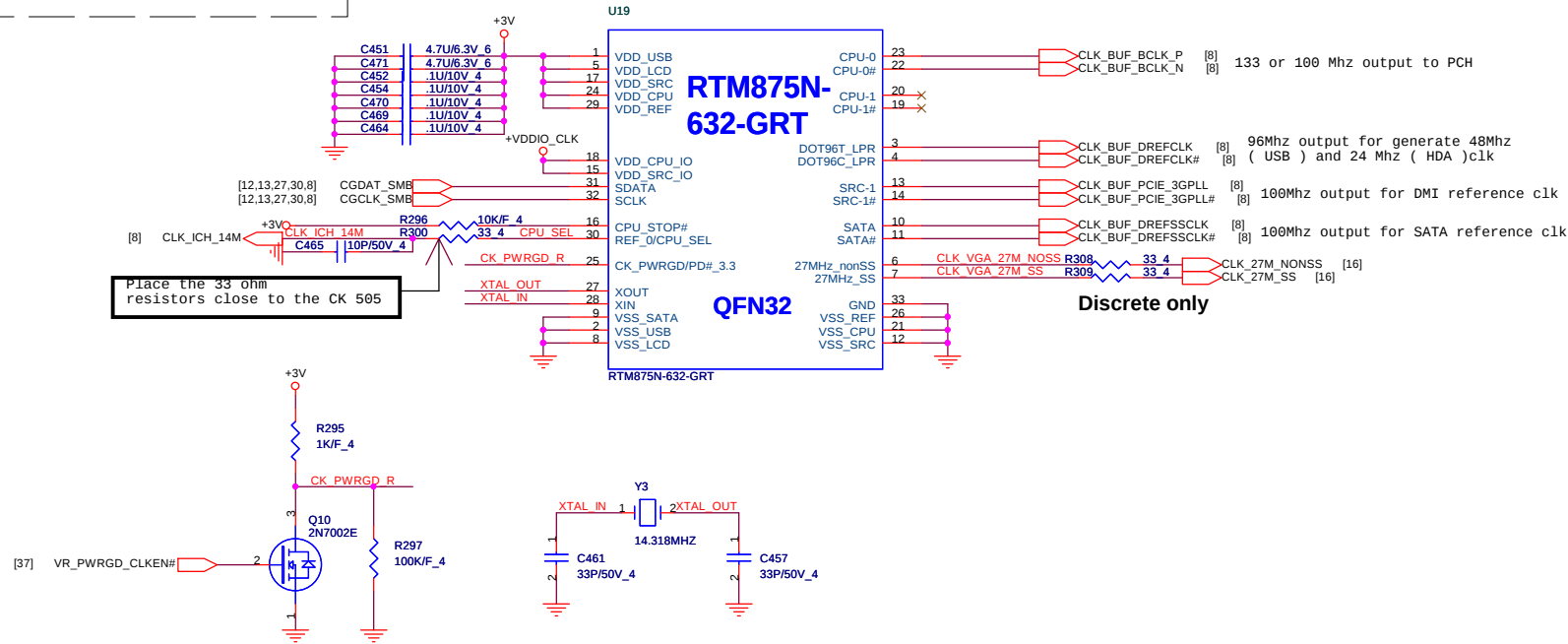
TW9D (15.6W) BLOCK DIAGRAM

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : VCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT



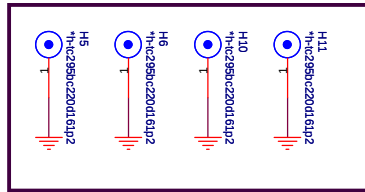


CLOCK GENERATOR



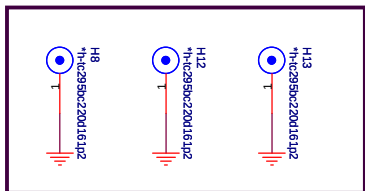
	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

CPU bracket Hole.



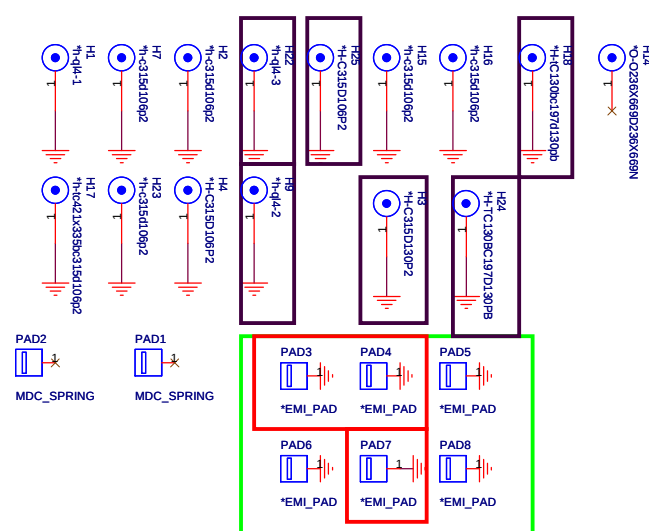
B-stage change

VGA bracket Hole.

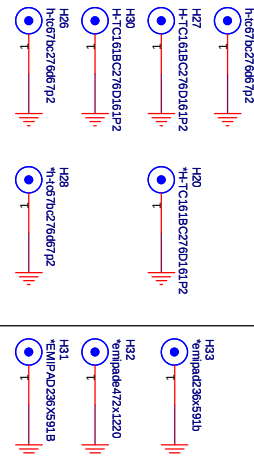


B-stage change

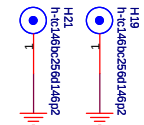
PAD and HOLE



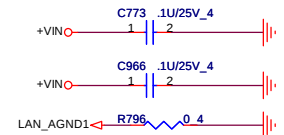
MINI CARD Hole.



MDC Hole.

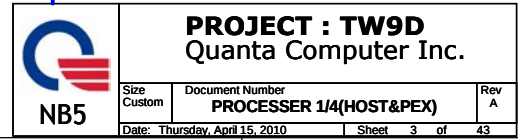


EMI solution.

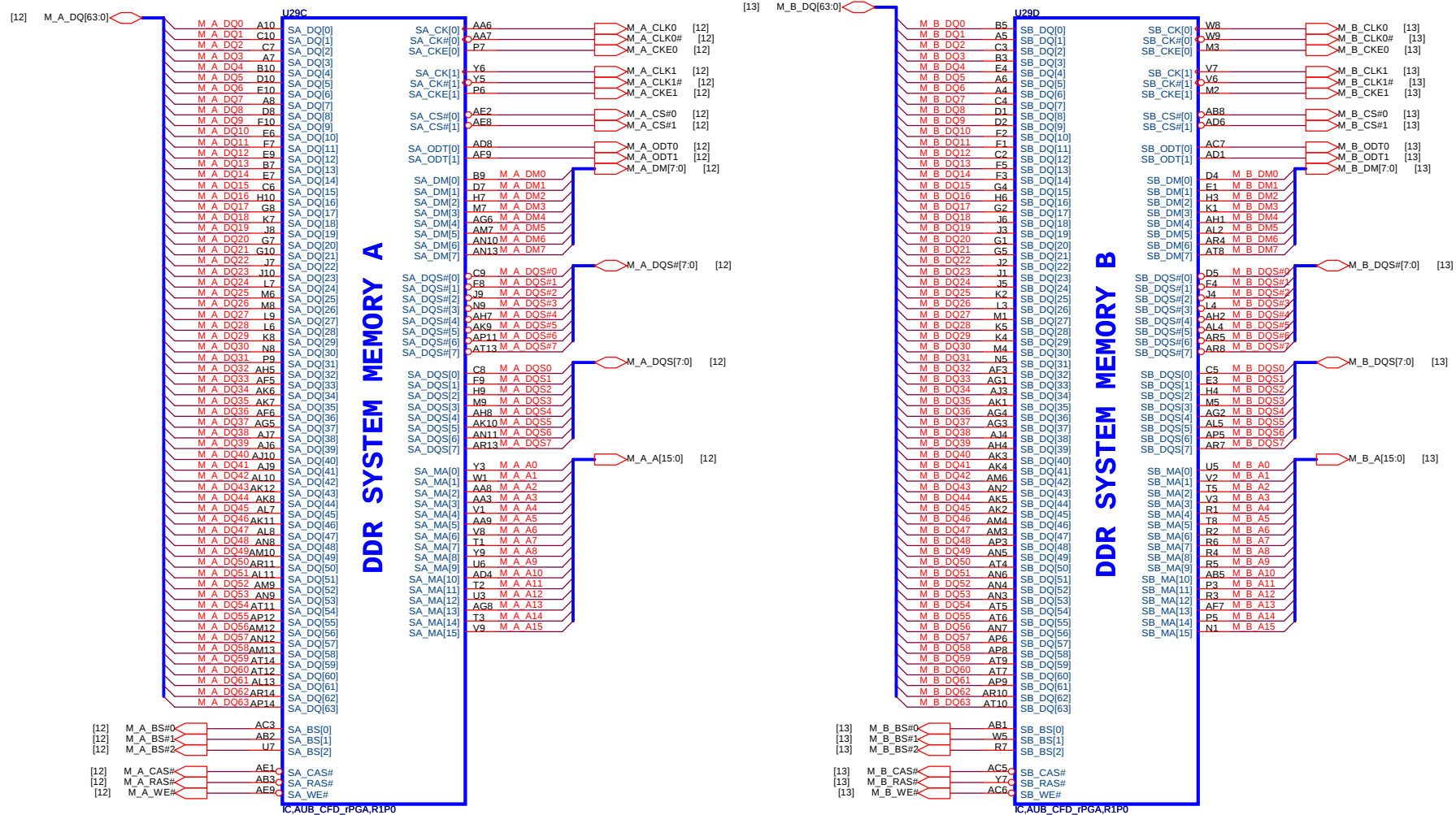


PROJECT : TW9D
Quanta Computer Inc.

Size Custom	Document Number	Rev A
	CLOCK & Screw Holes	
Date: Thursday, April 15, 2010	Sheet 2 of 43	



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

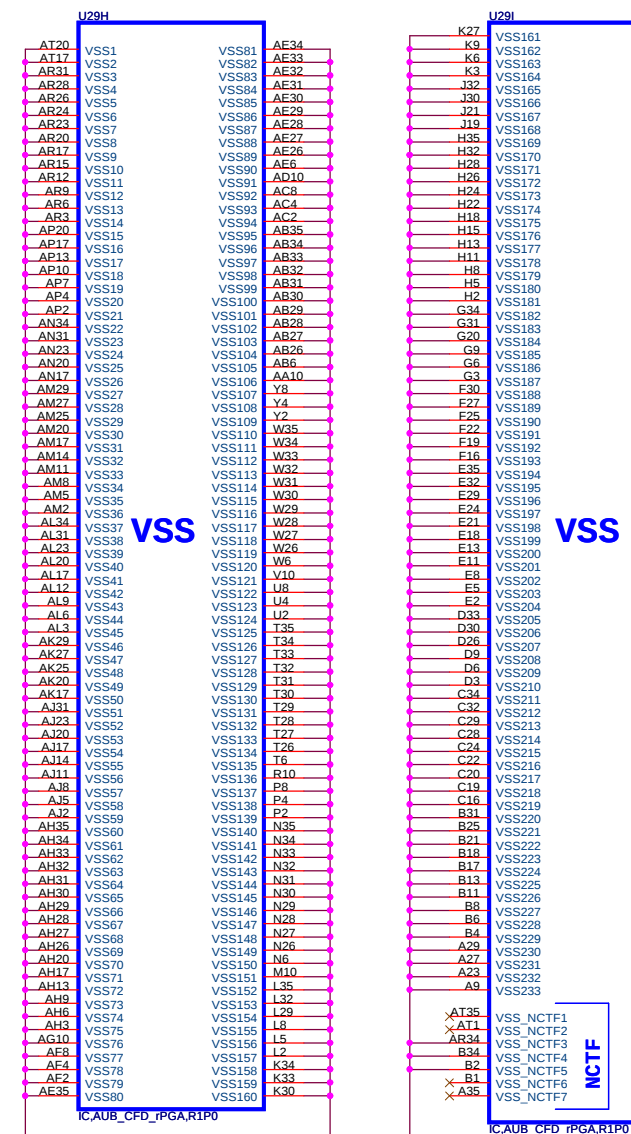


PROJECT : TW9D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSOR 2/4(DDR)	A
Date: Thursday, April 15, 2010	Sheet 4 of 43	

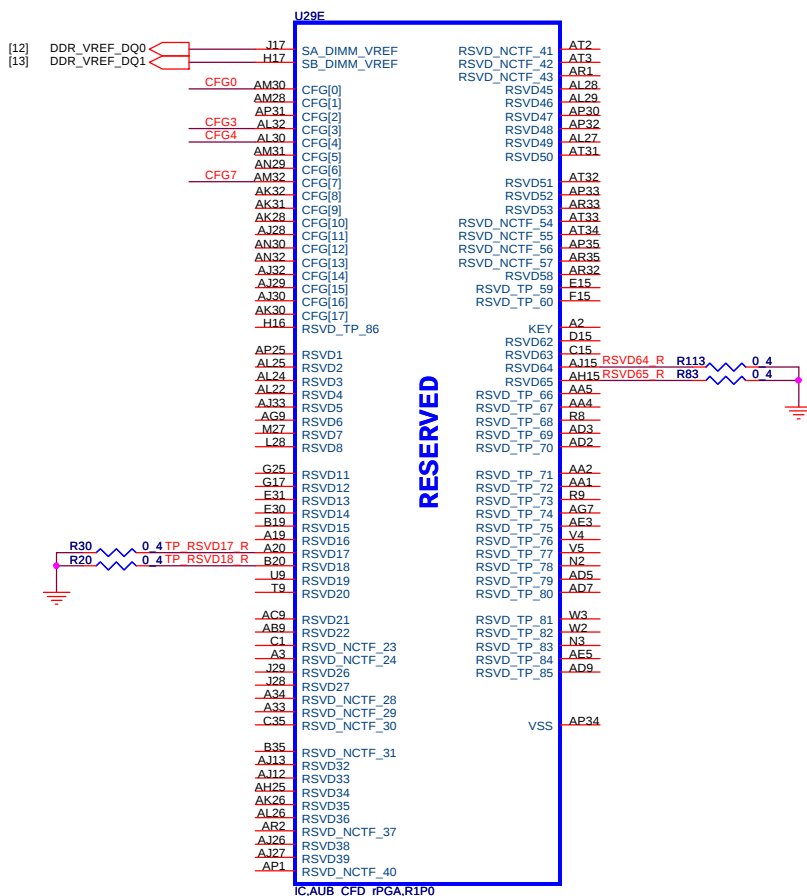


AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.0k Ω +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



For Discrete only



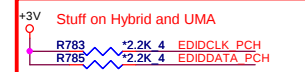
```
CFG[ 1:0 ] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG
```



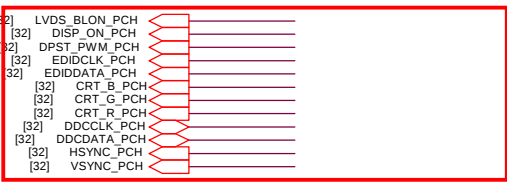
PROJECT : TW9D
Quanta Computer Inc.

Size Custom	Document Number PROCESSER 4/4(GND)	Rev A
Date: Thursday, April 15, 2010		Sheet 6 of 43

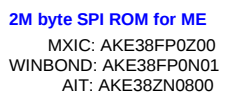
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1



IBEX PEAK-M (LVDS,DDI)



1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.



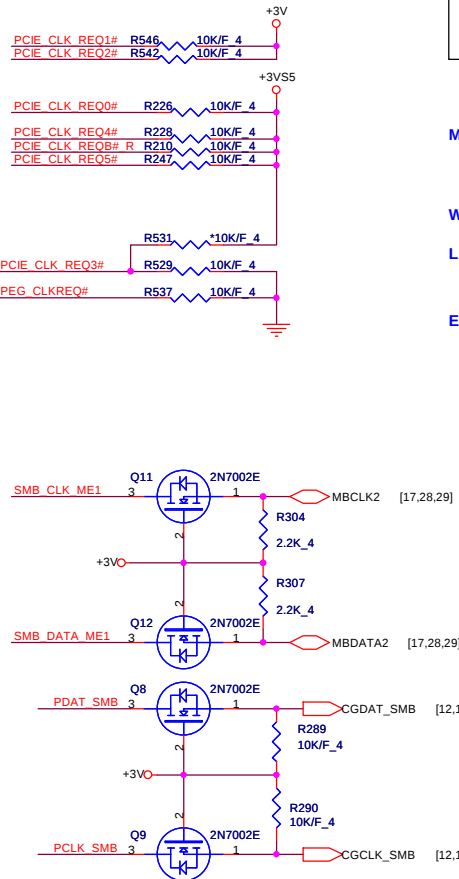
SPI ROM Socket
DG008000031

PROJECT - T

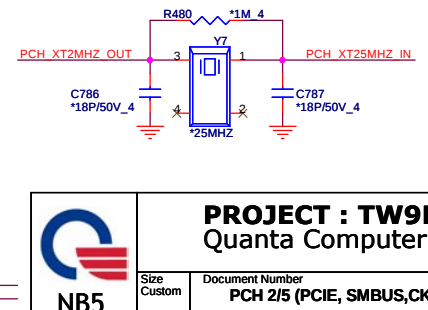
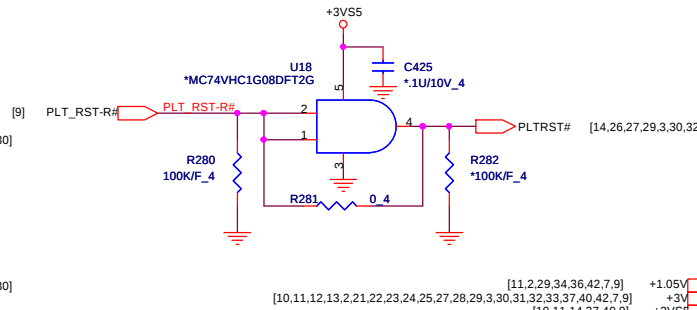
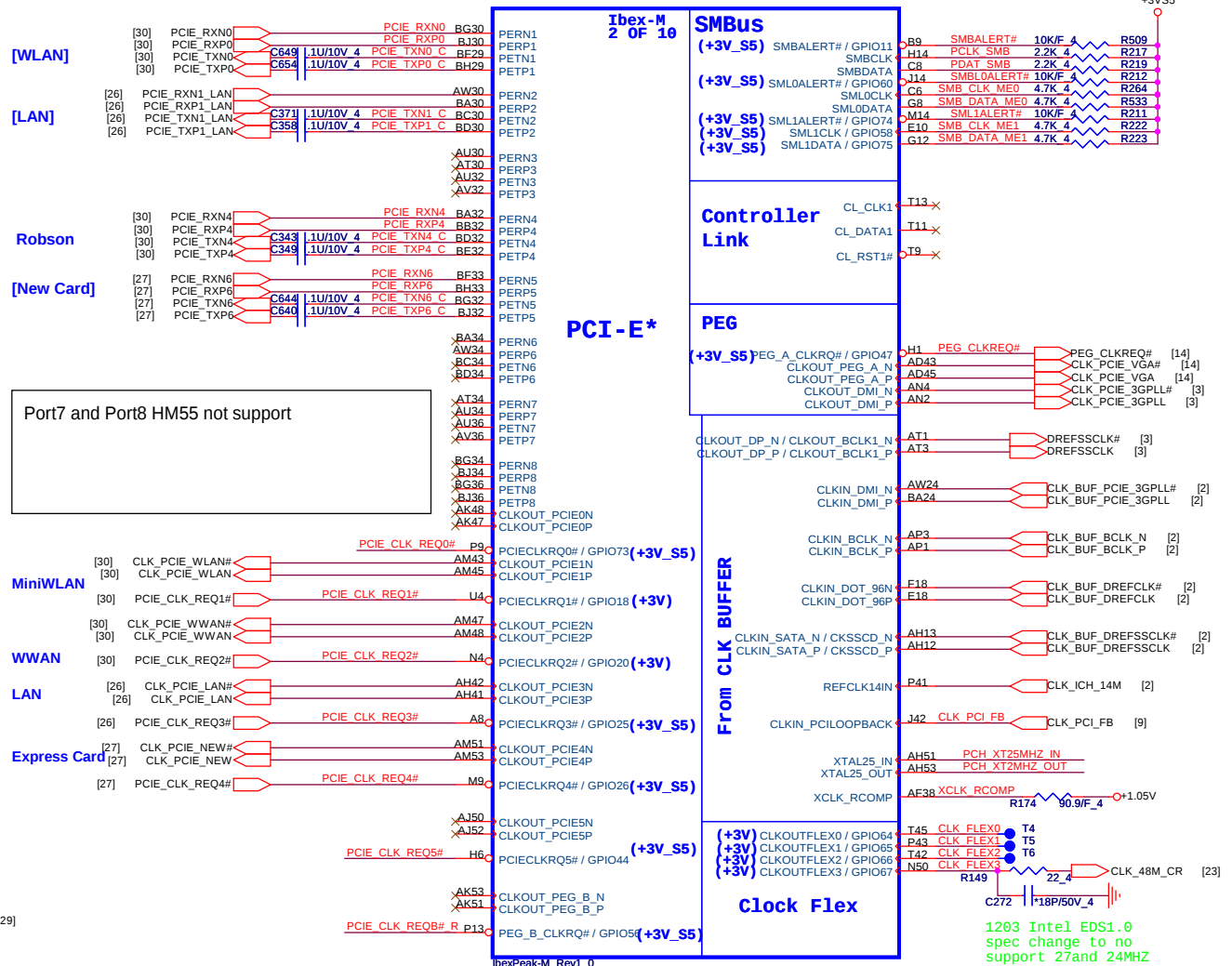
PROJECT : TW9D
Quanta Computer Inc.



Size Custom	Document Number PCH 1/5 (SATA,HDA,LPC)	Rev A
Date: Thursday, April 15, 2010	Sheet 7 of 43	



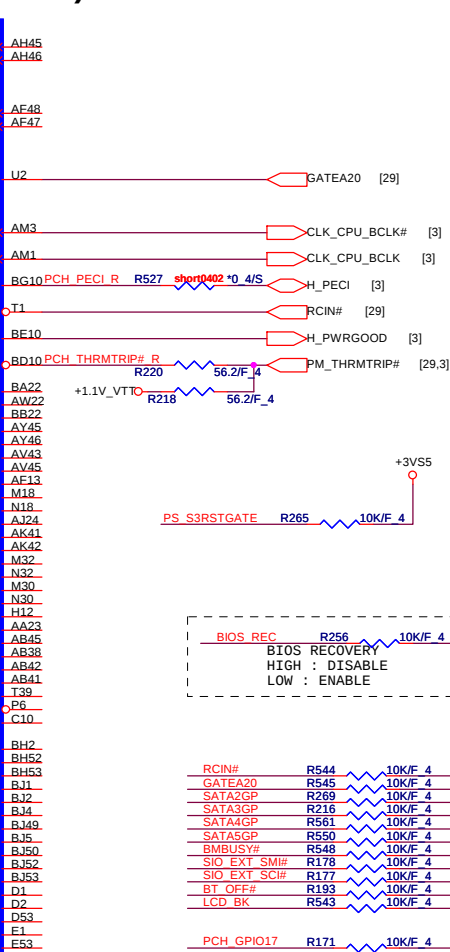
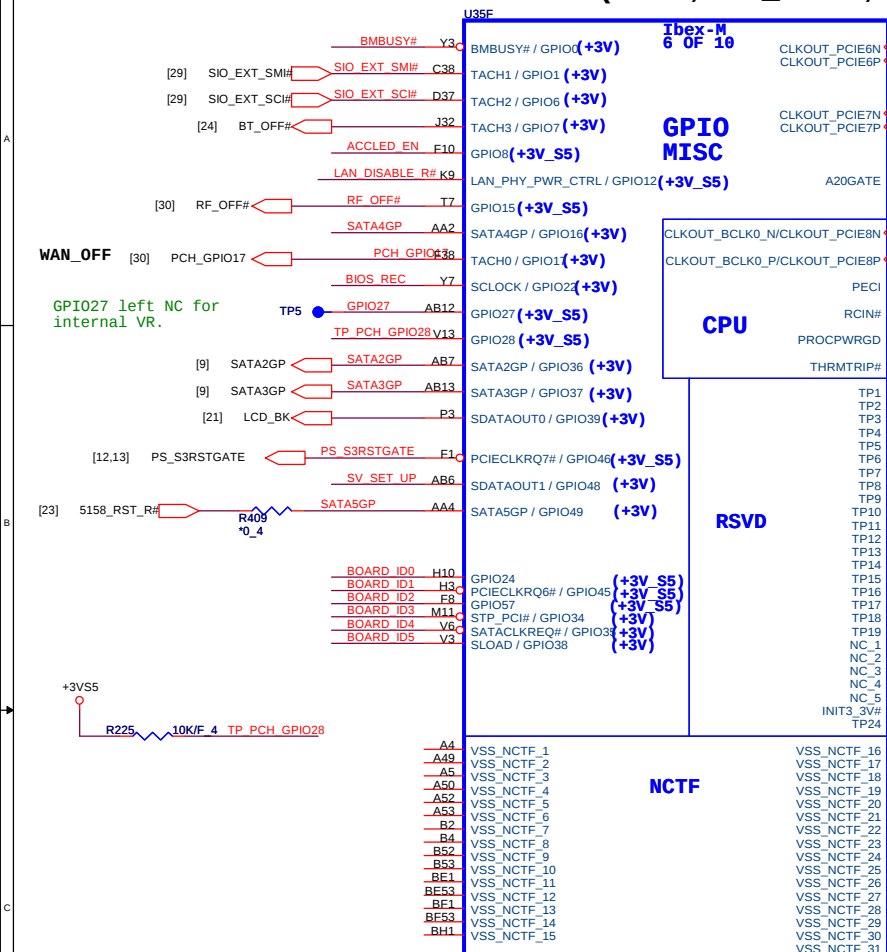
U35B



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)

10



[30,9] GNT3# R461 *10K NC

A16 swap override Strap/Top-Block Swap Override jumper

GNT3#

Low = A16 swap override/Top-Block Swap Override enabled
High = Default

SV SET UP R271 10K/F 4 +3V

SV_SET_UP 1-X High = Strong (Default)

[9] GNT0# GNT0# R155 *1K/F 4

[9] GNT1# GNT1# R157 *1K/F 4

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SP1

[31,9] NV_ALE R534 *1K/F 4
[31,9] NV_CLE R535 *1K/F 4 +1.8V

Danbury Technology Enabled

NV_ALE High = Enable
Low = Disable

DMI Termination Voltage

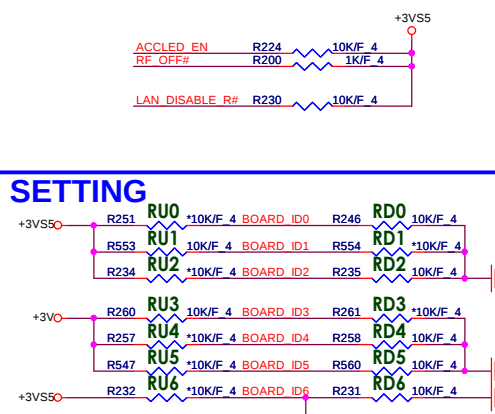
NV_CLE Set to Vcc when LOW
Set to Vcc/2 when HIGH

No Reboot Strap

[24,7] SPKR SPKR *1K/F 4 R556 +3V

[29,7] PCH_GPIO33 R194 *10K/F 4 +3V

BOARD ID SETTING



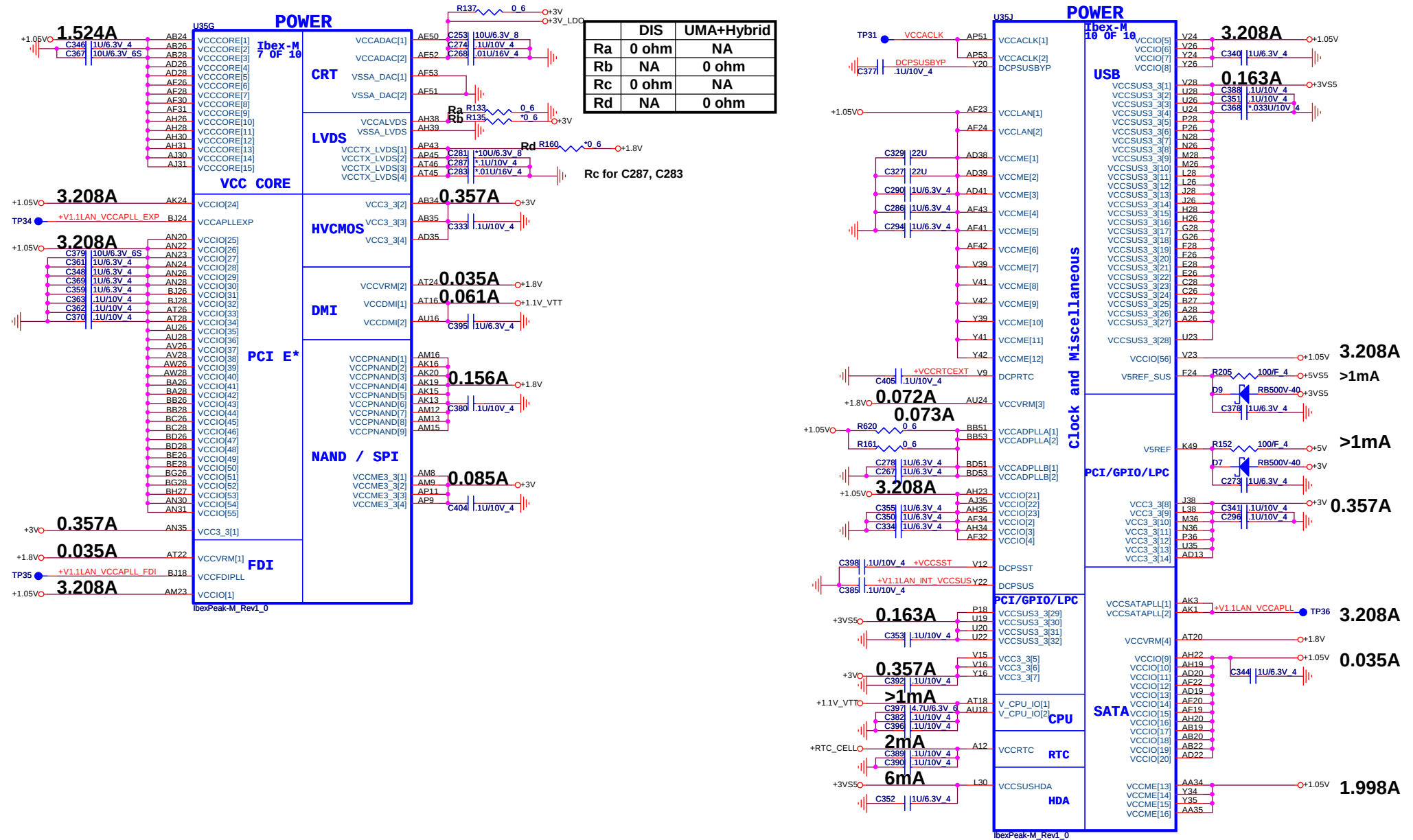
Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6
LG/CB	0=LG 1=CB						
UMA/Dis.		0=UMA 1=Dis.					
15.6" / 14"			0=QL4/TW9 1=QL2/SW9				
			0=TW9(A) 1=TW9F				
Switchable						1=YES 0=NO	

Board ID	ID6	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RDO (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RDO (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RDO (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

[11,3,34,38,5] +1.1V_VT
[11,31,36,40,42,5] +1.8V
[11,37,40,42,7,8,9] +3V
[11,14,27,40,8,9] +3VSS

PROJECT : TW9D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/5 (GPIO & Strap)	A
Date: Thursday, April 15, 2010	Sheet 10 of 43	

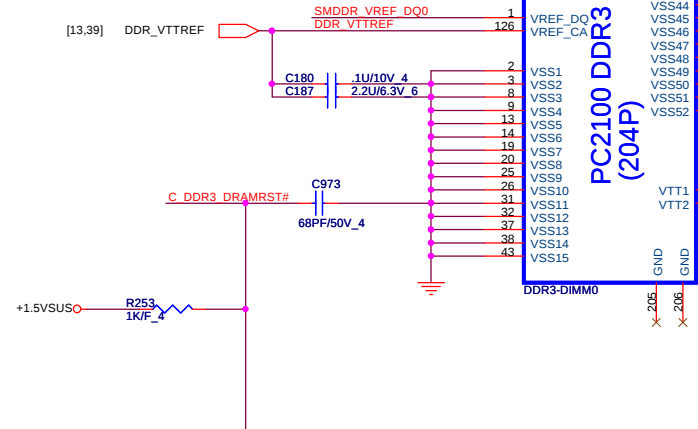
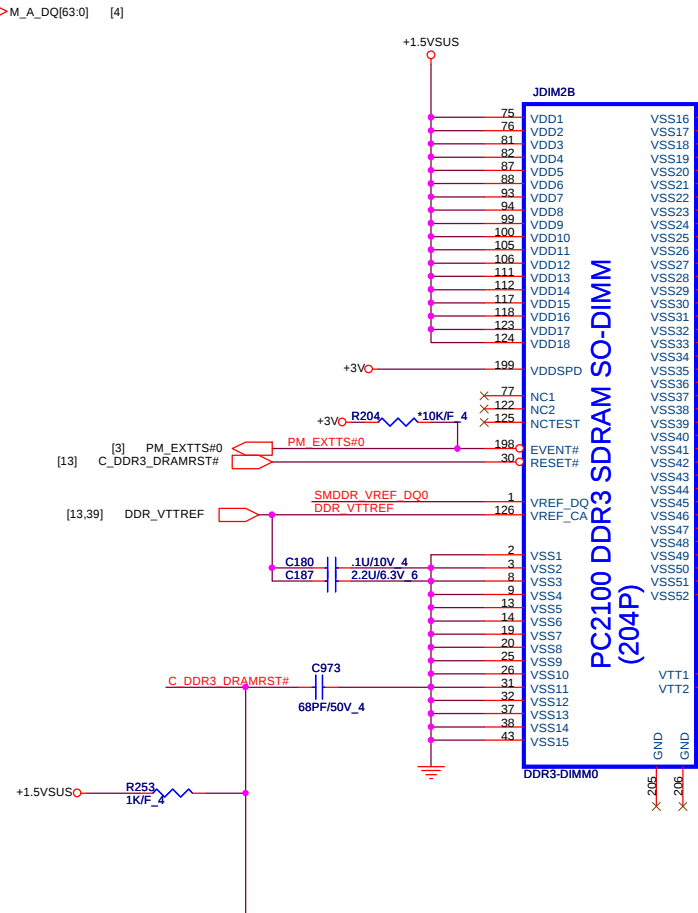


[2,29,34,36,42,7,8,9]	+1.05V
[10,3,34,38,5]	+1.1V_VTT
[10,31,36,40,42,5]	+1.8V
[10,12,13,2,21,22,23,24,25,27,28,29,3,30,31,32,33,37,40,42,7,8,9]	+3V
[10,14,27,40,8,9]	+3VSS
[22,24,25,27,28,30,32,40]	+5V
[40]	+5VSS



PROJECT : TW9D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/5 (POWER)	A
Date: Thursday, April 15, 2010		Sheet 11 of 43



[3] DDR3_DRAMRST#

R96 100K/F_4

C232 4700P/25V_4

R100 *0.4

Q39 BSS138

PS_S3RSTGATE

[6] DDR_VREF_DQ0

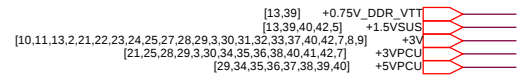
R103 100K/F_4

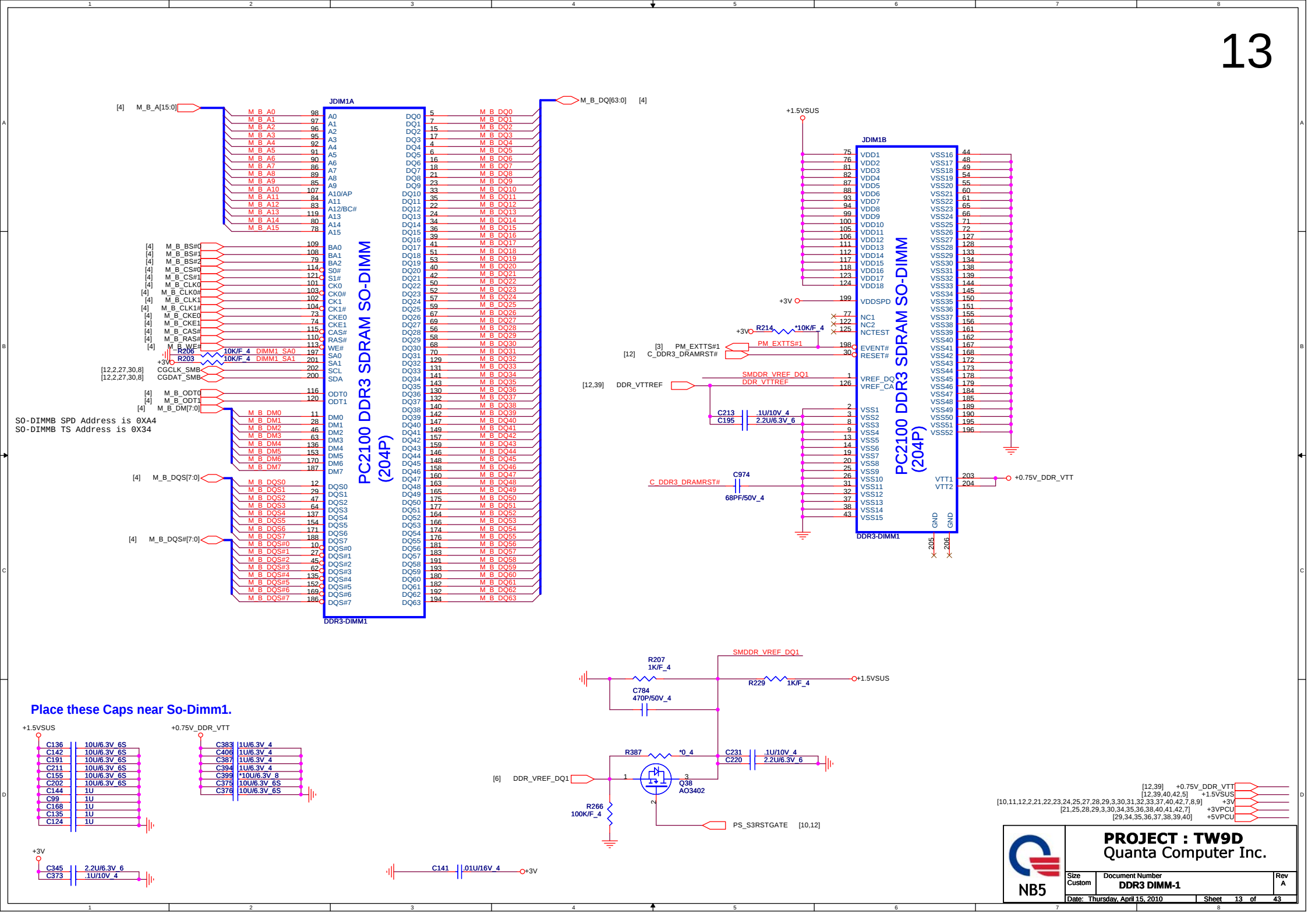
R26 *0.4

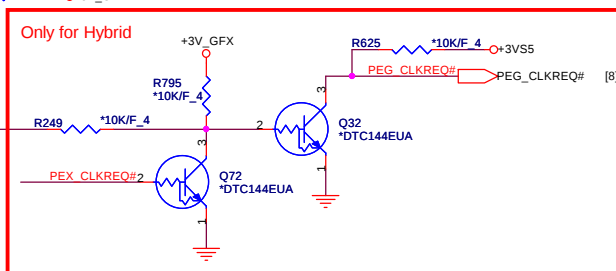
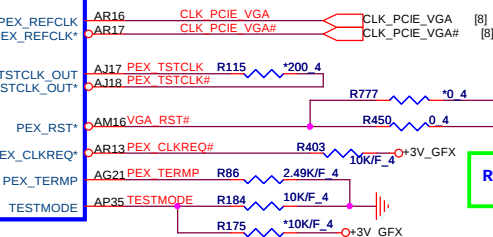
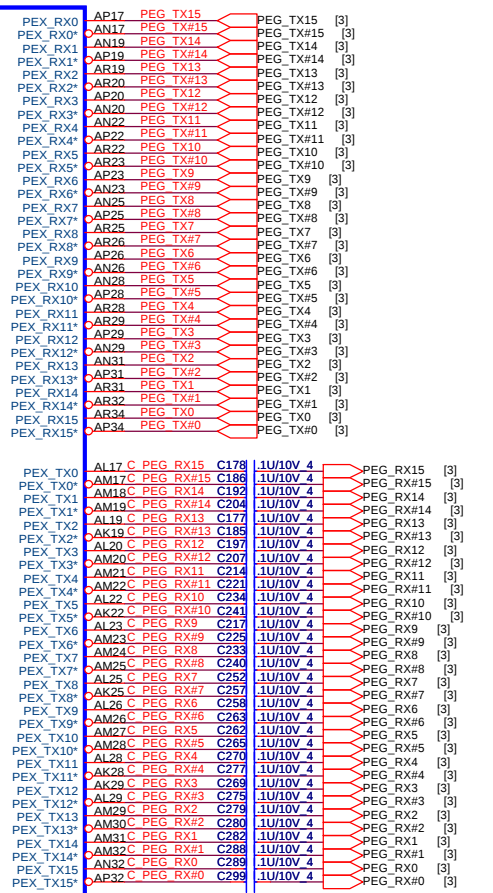
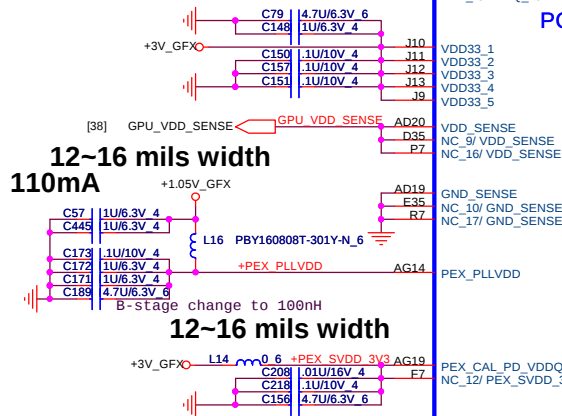
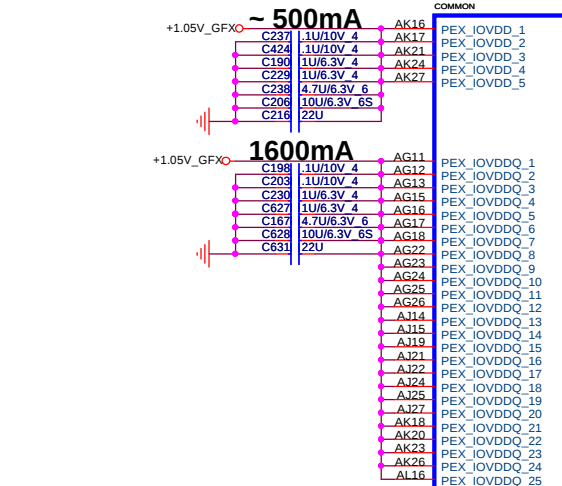
Q37 AO3402

PS_S3RSTGATE

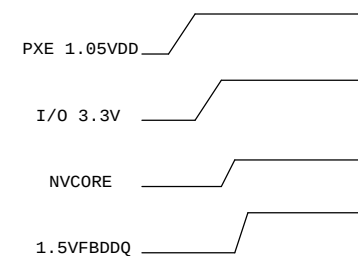
SMDR_VREF_DQ0





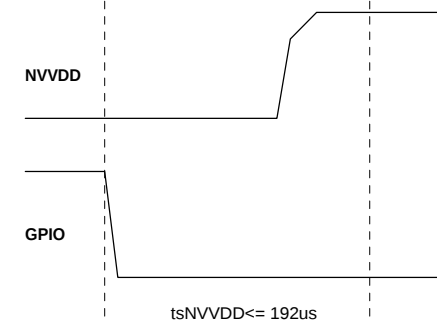


power up sequence

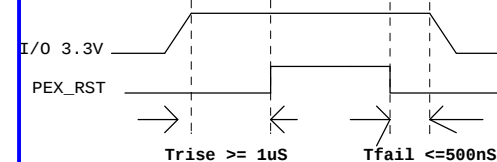


NB9M: VGACORE +0.90V (Normal) , +1.09V

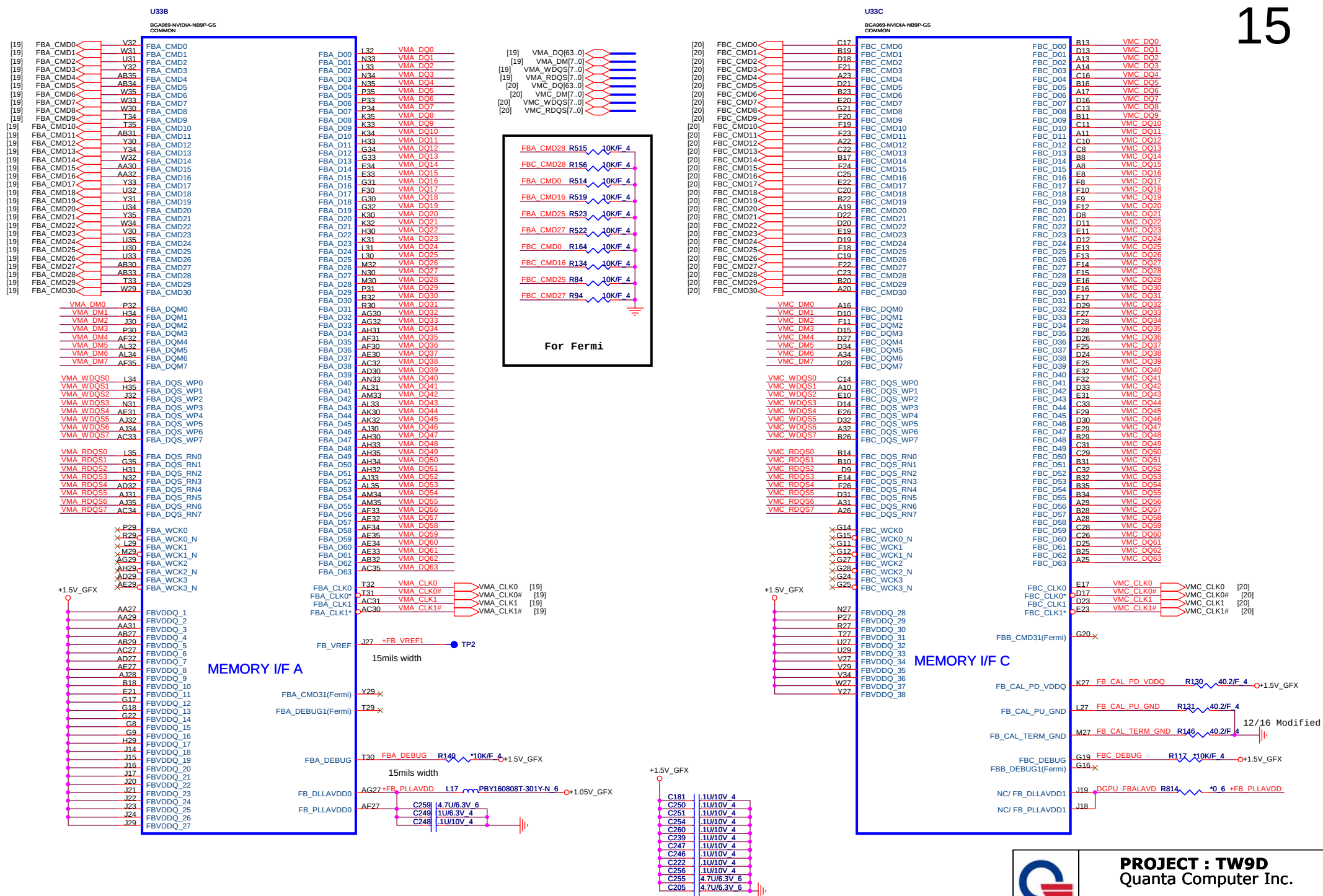
NVVDD Maximum Settling Time

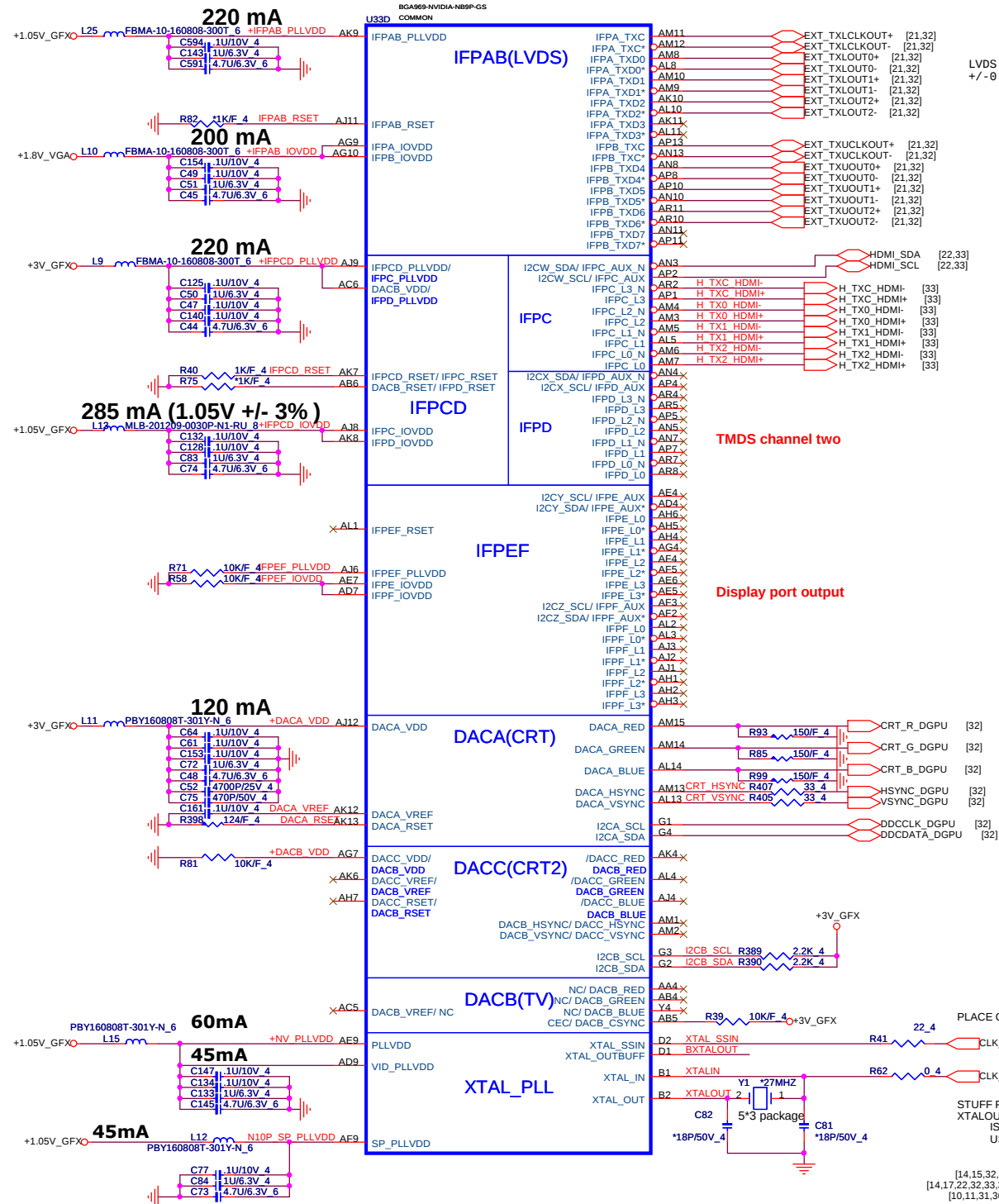


PEX_RST timing



[15,16,32,42] +1.05V_GFX
[16,17,22,32,33,38,42] +3V_GFX

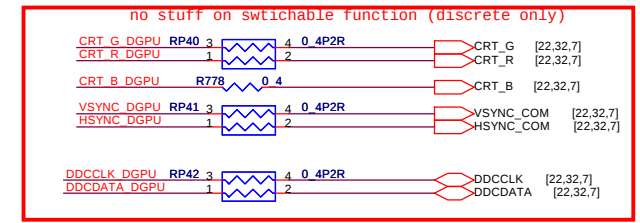




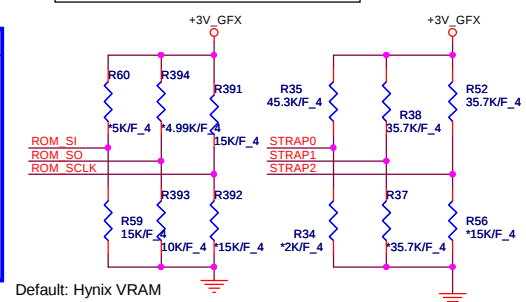
LVDS clk spread : Center
+/-0.5% (30-33KHZ)

TMDs channel two

Display port output



10 kΩ pull-down only if no spread chip used.



4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1% (0402)]
10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1% (0402)]
35.7K/F 4: CS33572FB18 [RES CHIP 35.7K 1/16W +1% (0402)]
45.3K/F 4: CS34532FB13 [RES CHIP 45.3K 1/16W +1% (0402)]
20K/F 4: CS32002FB29 RES CHIP 20K 1/16W +1% (0402)

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

	RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
01	0000	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Reserved	IDGH1G-04A1F1C-16X	PD 10K
00	0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda		
02	0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
	0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K
	0101		Reserved		
	0110				
	XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
	XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

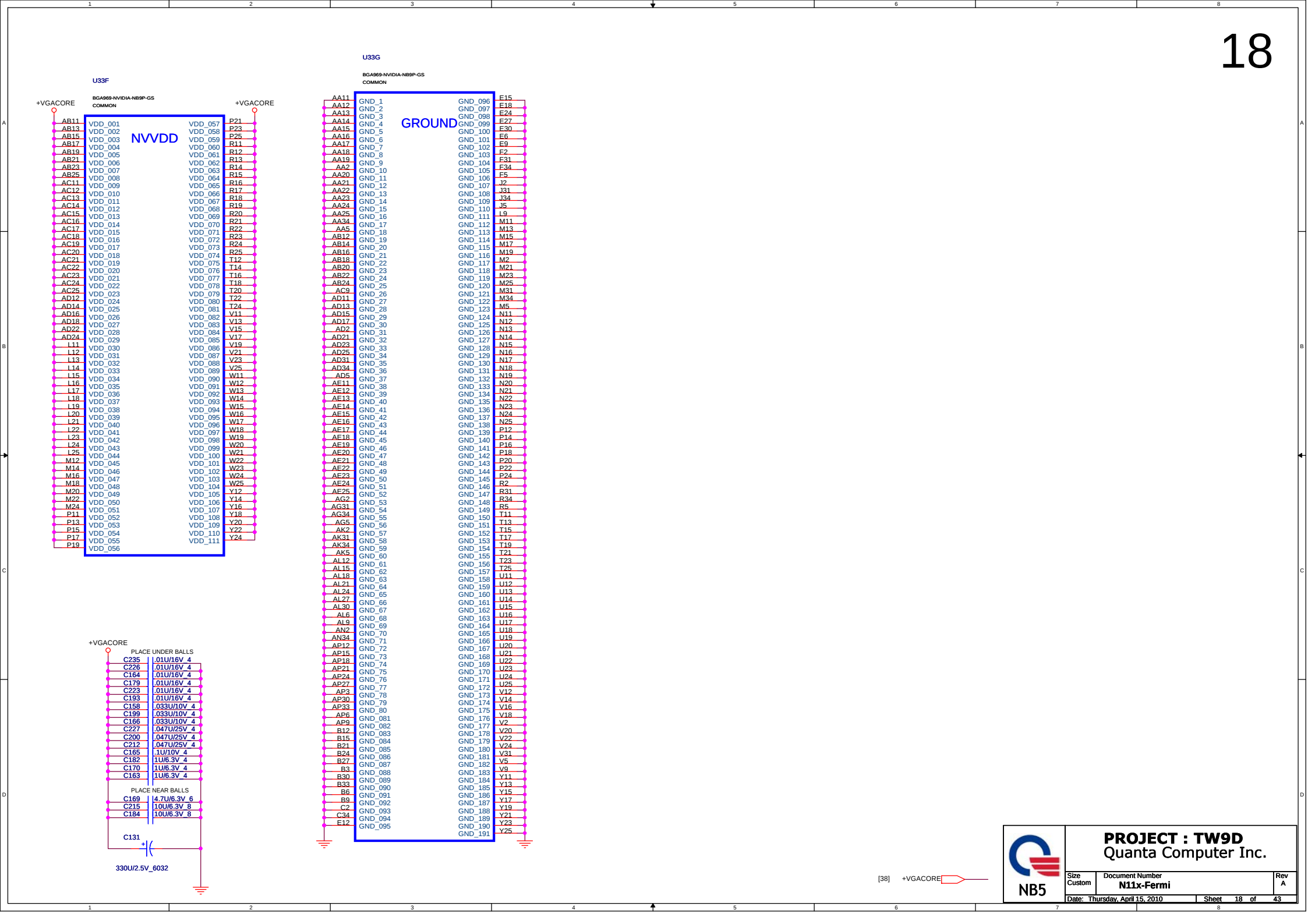
GPIO ASSIGNMENTS

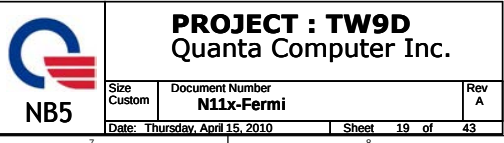
GPI/O	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

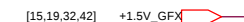
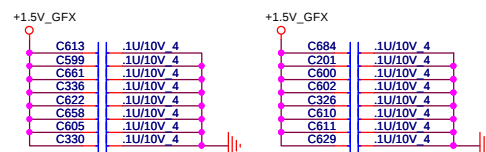
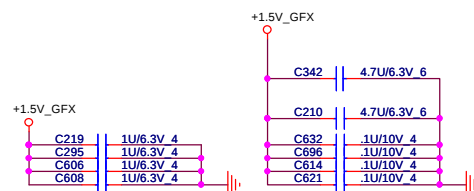
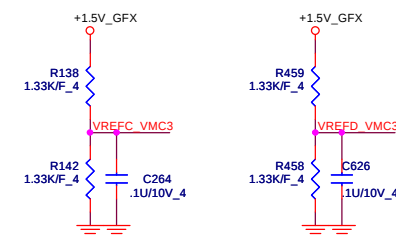
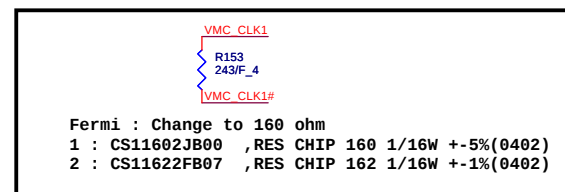
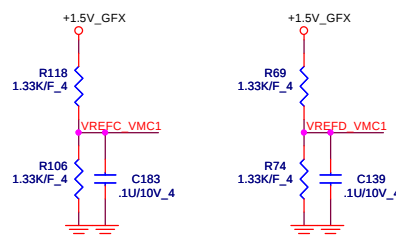
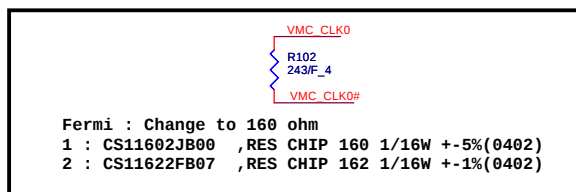
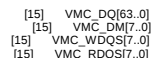


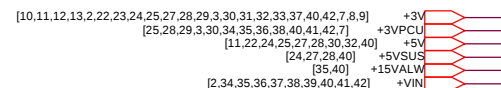
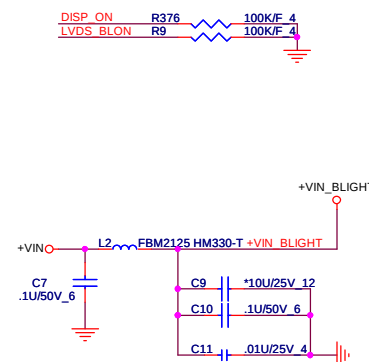
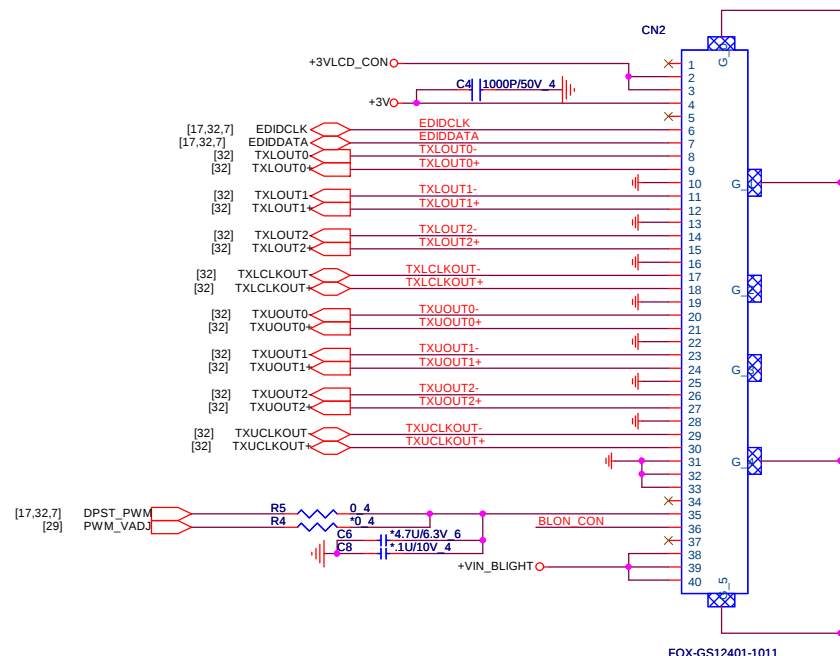
PROJECT : TW9D
Quanta Computer Inc.

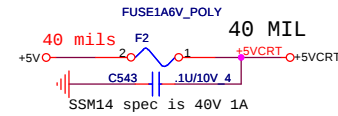
Size Custom	Document Number N11x-Fermi	Rev A
Date: Thursday, April 15, 2010		Sheet 17 of 43



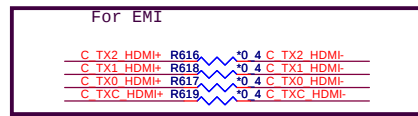
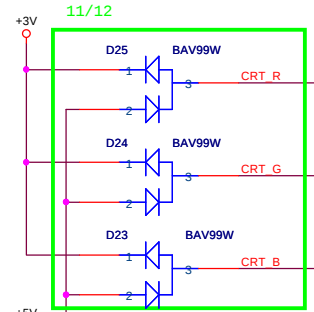
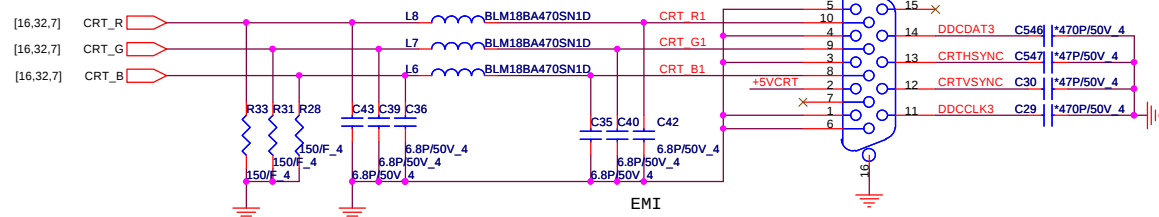




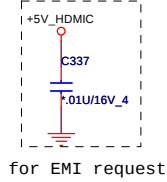
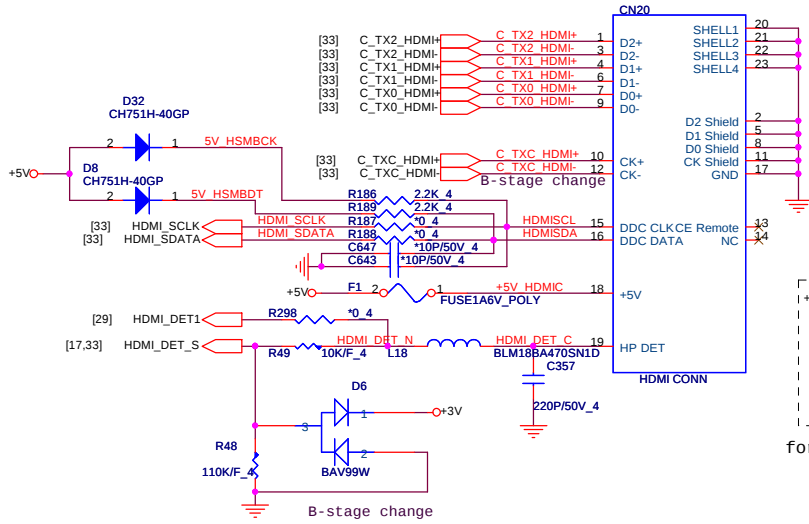
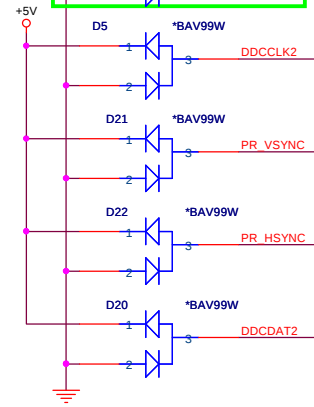
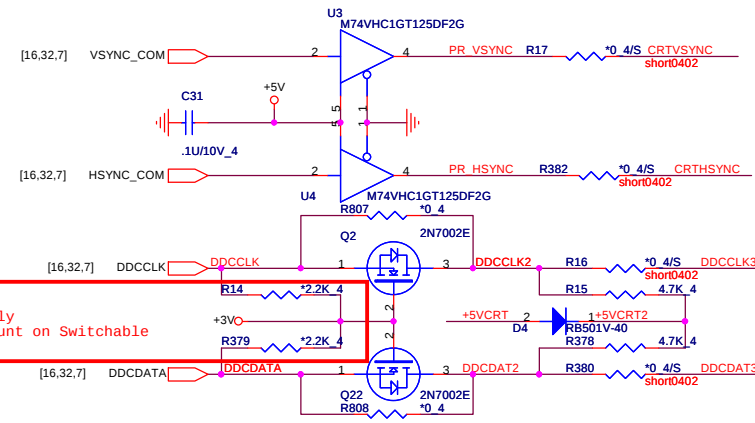




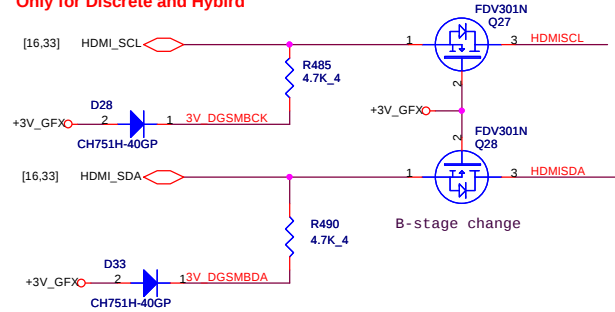
CRT PORT



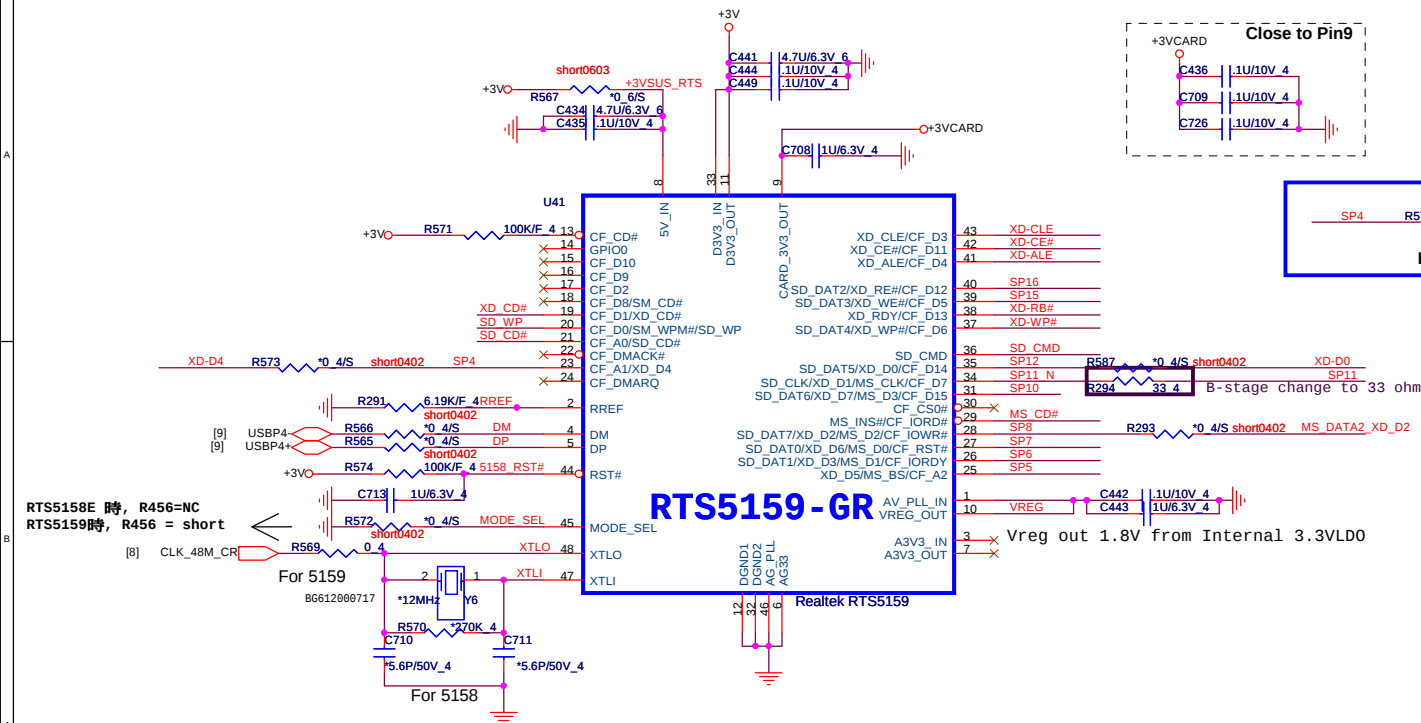
HDMI PORT



Only for Discrete and Hybrid

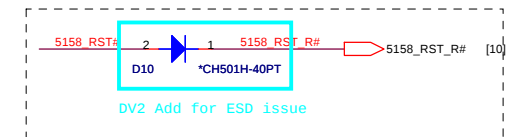
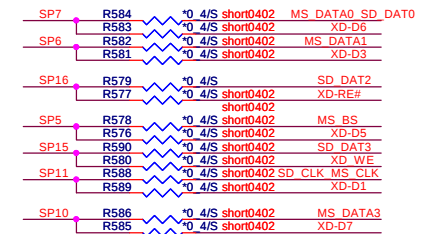


Note:

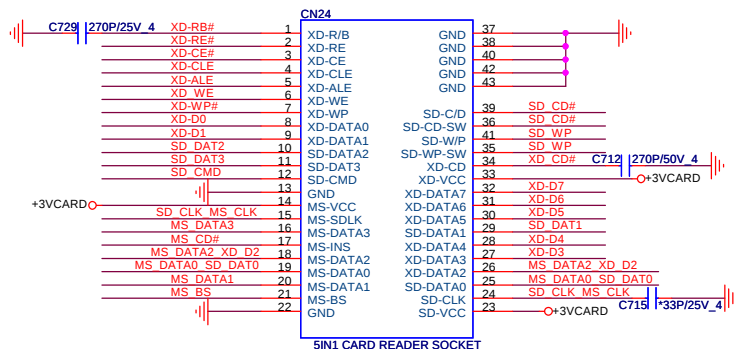


	SD/MMC	MS	XD
SP0			
SP1			XD CD#
SP2	SD WP		
SP3	SD CD#		
SP4	SD DAT1		XD D4
SP5		MS BS	XD D5
SP6		MS D1	XD D3
SP7	SD DAT0	MS D0	XD D6
SP8	SD DAT7	MS D2	XD D2
SP9		MS INS#	
SP10	SD DAT6	MS D3	XD D7
SP11	SD CLK	MS SCLK	XD D1
SP12	SD DAT5		XD D0
SP13	SD DAT4		XD WP#
SP14			XD RB#
SP15	SD DAT3		XD WE#
SP16	SD DAT2		XD RE#
SP17			XD ALE
SP18			XD CE#
SP19			XD CLE

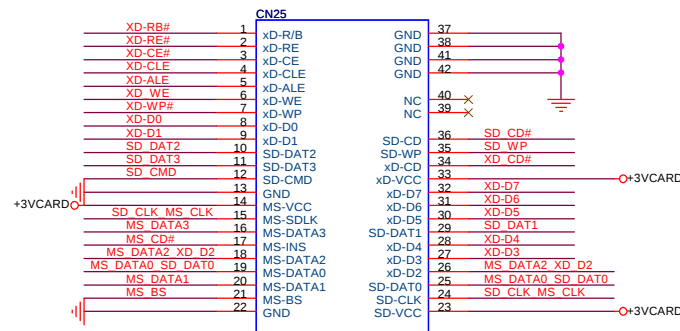
For RTS5159



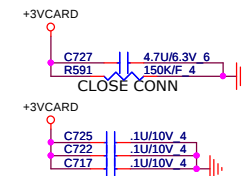
5 IN1 CARD READER
XD, MMC/SD, MS/MSP



PV change footprint



*TAI TWUM 5IN1 CARD READER SOCKET
PV change footprint

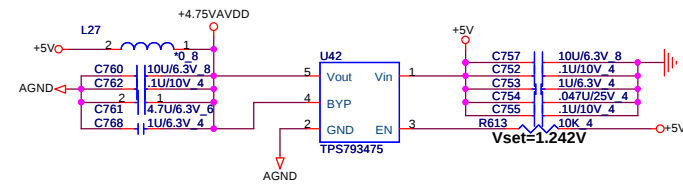
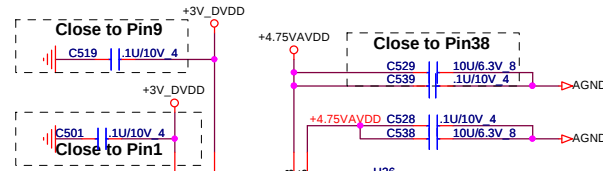
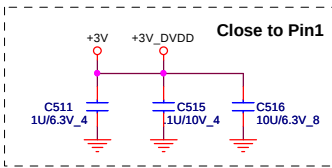


PROJECT : TW9D
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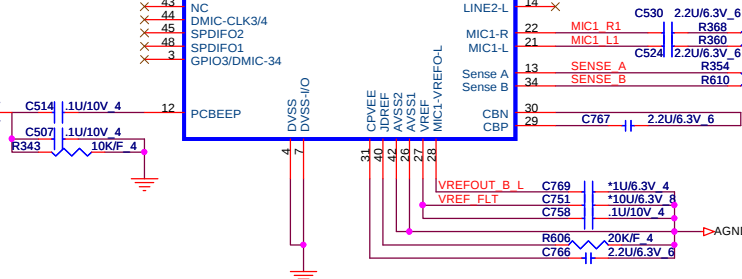
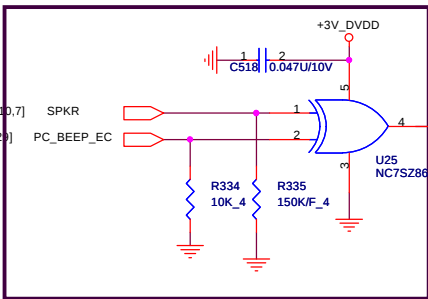
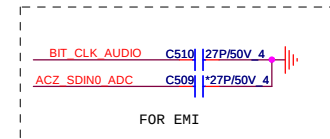
Size Custom	Document Number RTS5159 &CR SOCKET
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Rev
A

Date: Thursday, April 15, 2010	Sheet 23 of 43
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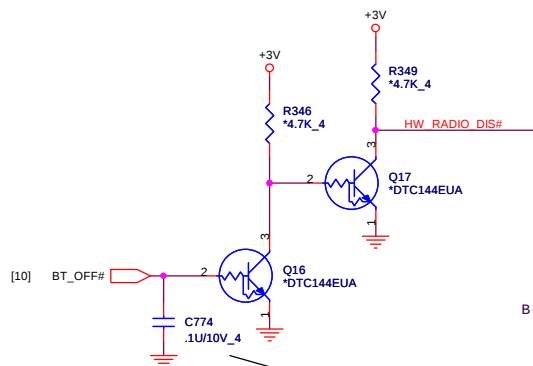
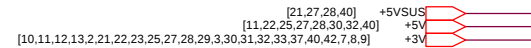
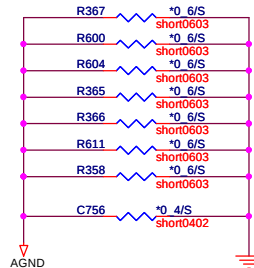


TO Internal Speakers

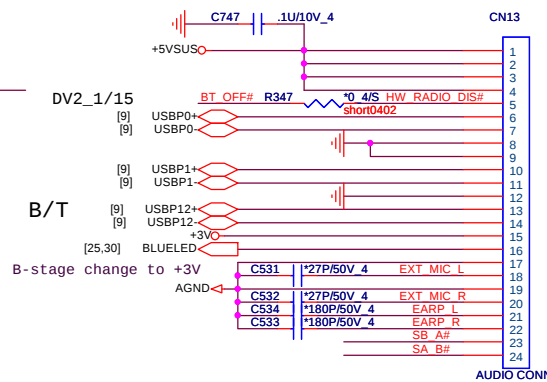


TO AUDIO/B CON.

TO Audio Jack MIC

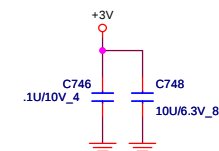
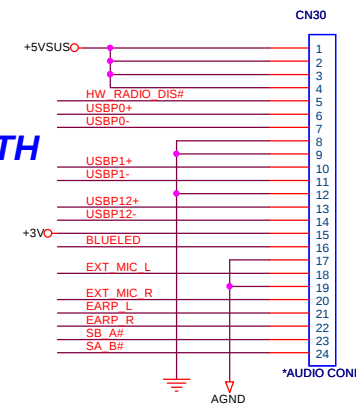


For EMI Request



Audio

B-stage change footprint CN13,CN30 to co-layout



SB_A# -->EXT HP

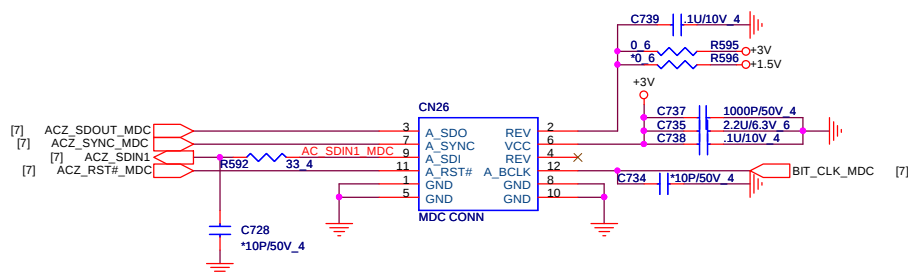
SA_B# -->EXT MIC

Audio JACK: Normal Open



PROJECT : TW9D
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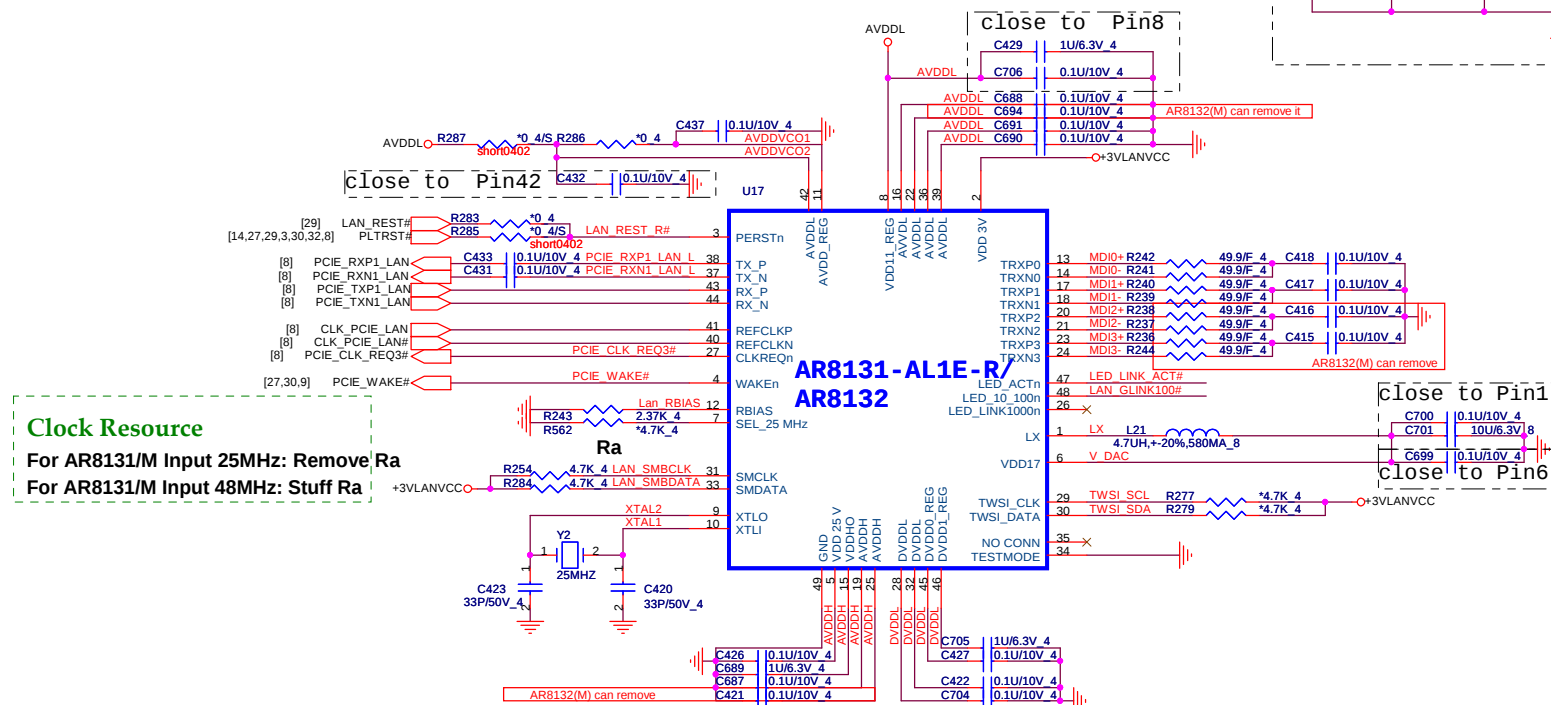
Size	Document Number	Rev
Custom	Azalia ALC272/BT CONN	A
Date: Thursday, April 15, 2010	Sheet 24 of 43	



LED

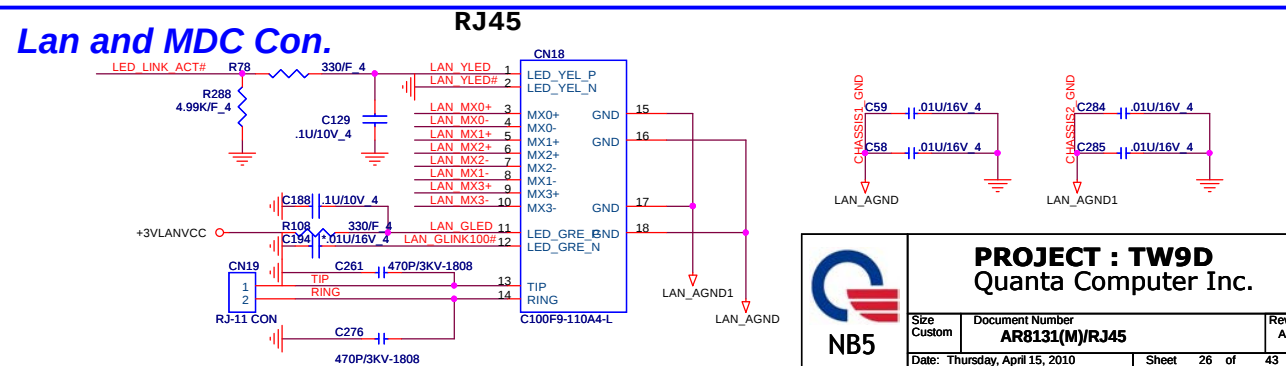
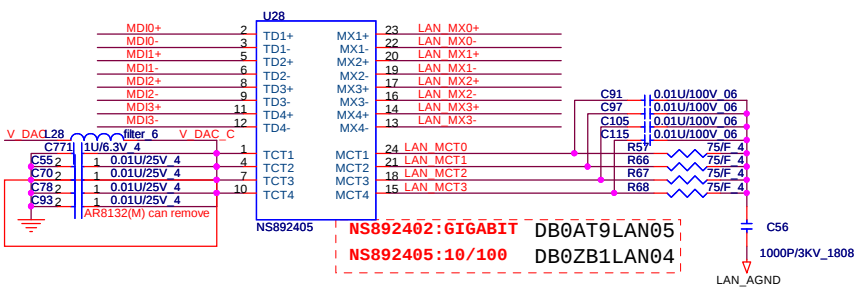


Size Custom	Document Number AMP_TPA6017/SPK/MDC/LED	Rev A
Date: Thursday, April 15, 2010		Sheet 25 of 43

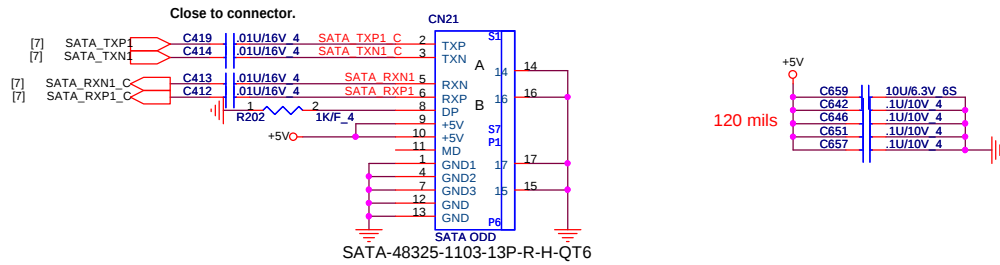


[10,11,12,13,2,21,22,23,24,25,27,28,29,3,30,31,32,33,37,40,42,7,8,9] +3V
[40] +3VLANVCC

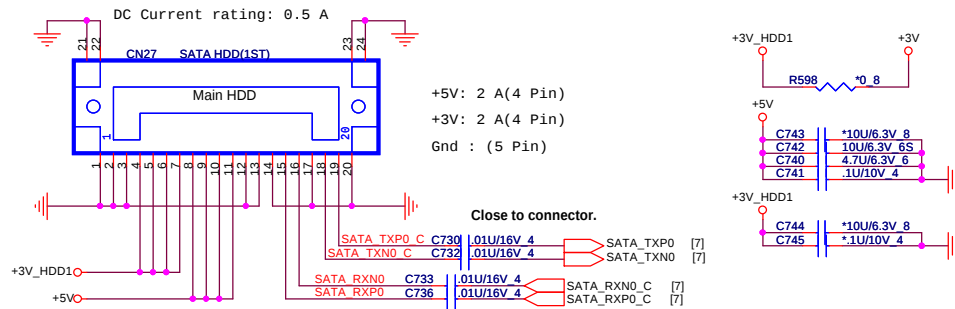
Lan and MDC Con.



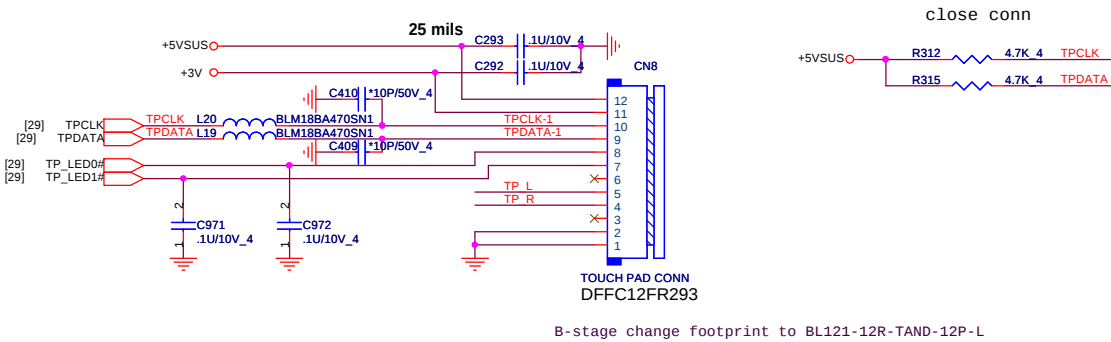
SATA ODD



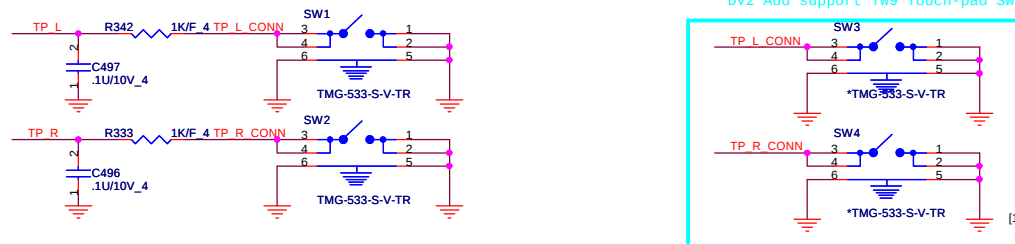
SATA_1 CONNECTOR



TOUCH PAD CONNECTOR

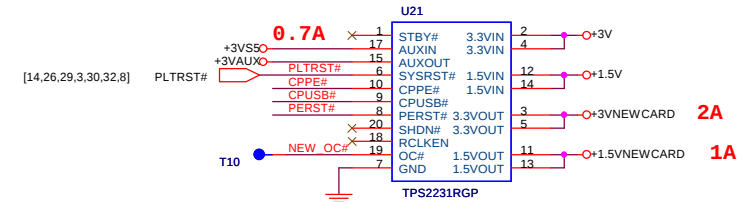
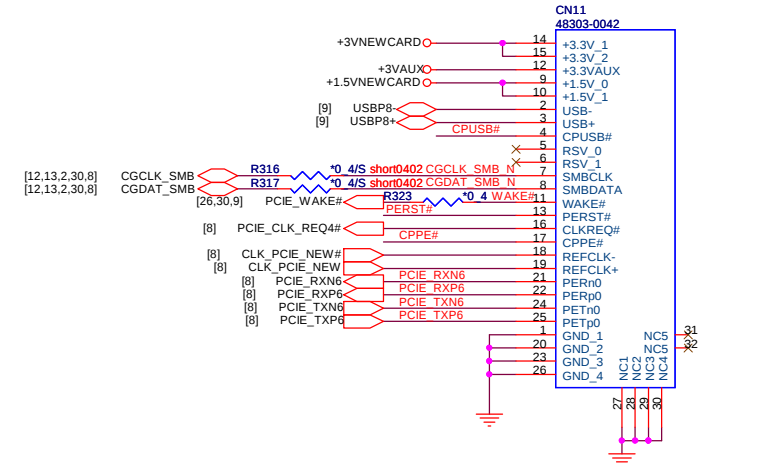


TOUCH PAD L/R SW1,SW2 in QL4 use, SW3,SW4 in TW9 use

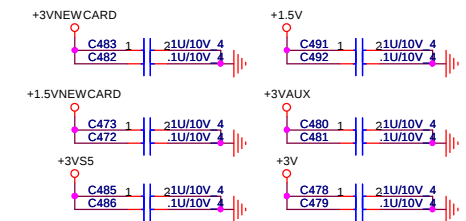


NEWCARD

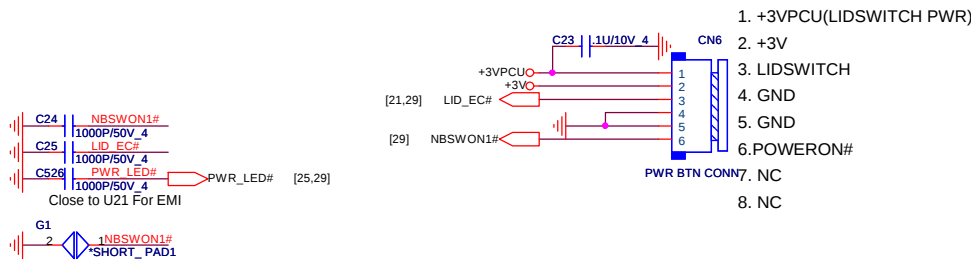
NEWCARD (PCIEXPRESS*1 + USB*1)



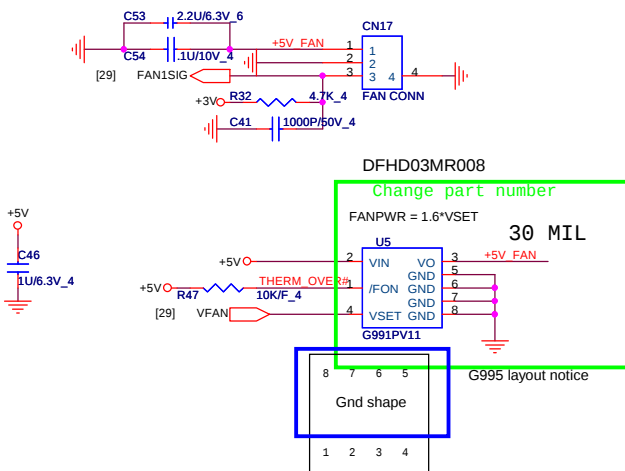
Change net name from 3V_NEWAUX to 3VAUX



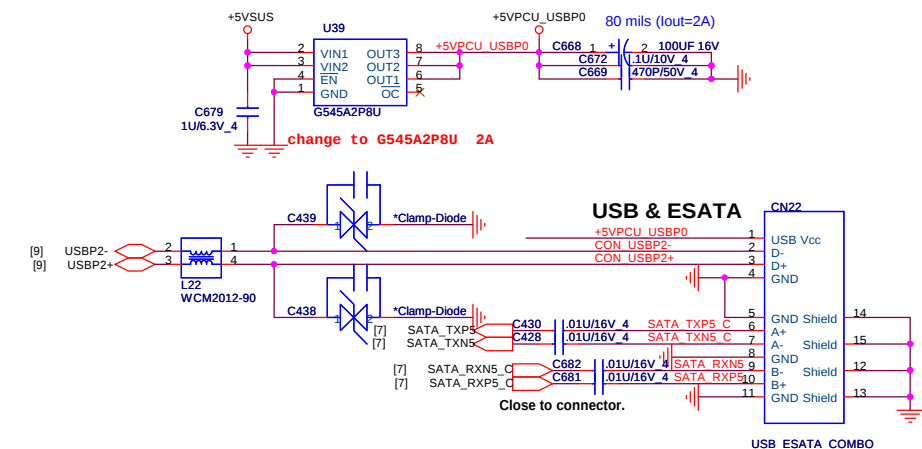
POWER BOTTOM CONNECT



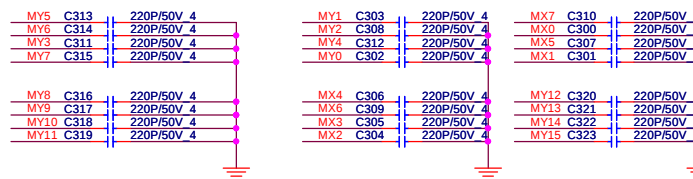
CPU FAN



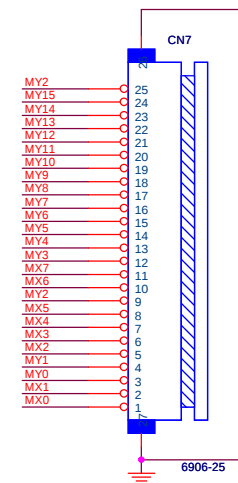
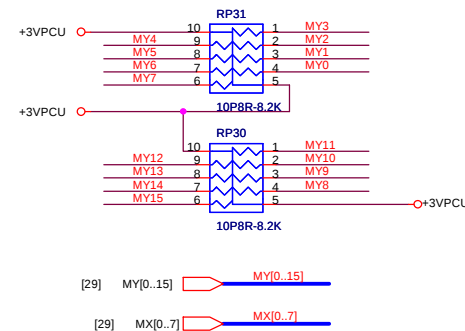
E-SATA/USB COMBO



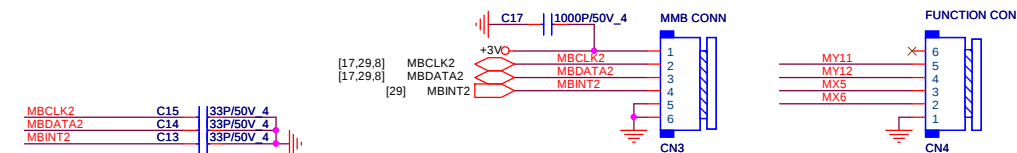
KEYBOARD Con.



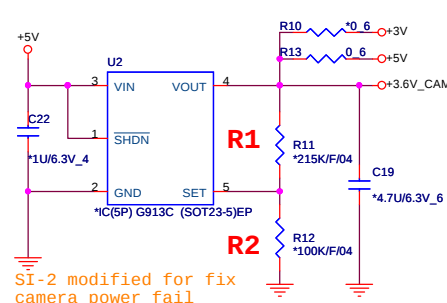
KEYBOARD PULL-UP



Capacity board Con.

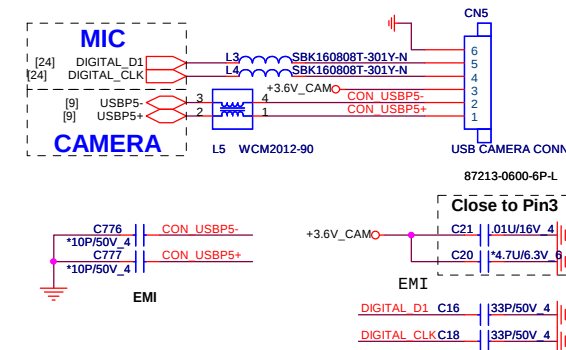


USB CAMERA POWER



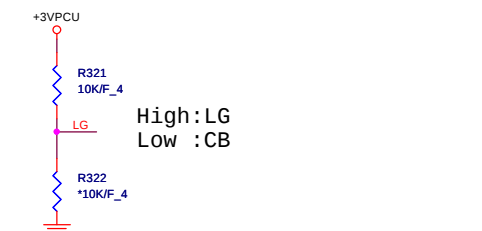
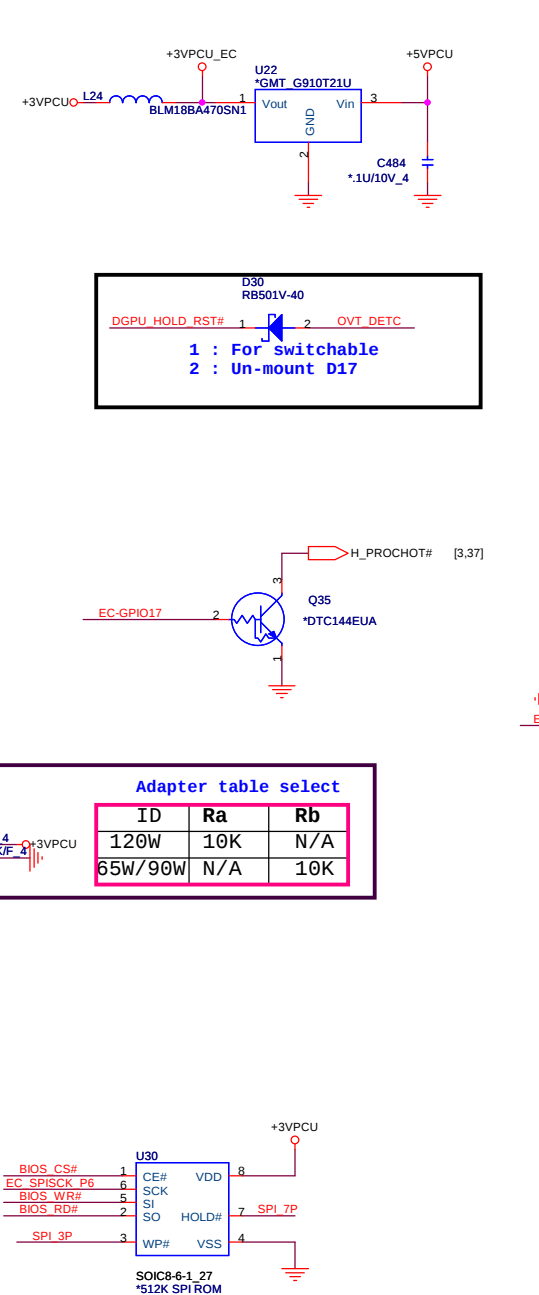
SI-2 modified for fix camera power fail

$$V_{out} = 1.25 (1 + R1/R2)$$

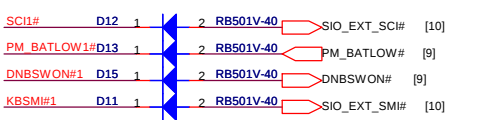
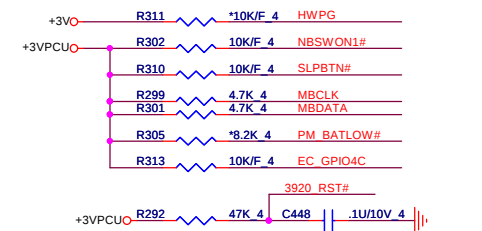


PROJECT : TW9D
Quanta Computer Inc.

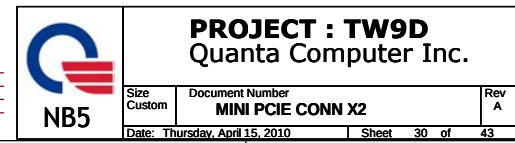
Size	Document Number	Rev
Custom	KB/PWR/ESATA/FAN/CAM/MIC	A
Date: Thursday, April 15, 2010	Sheet 28 of 43	

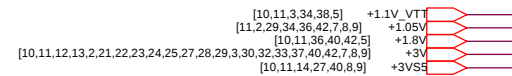
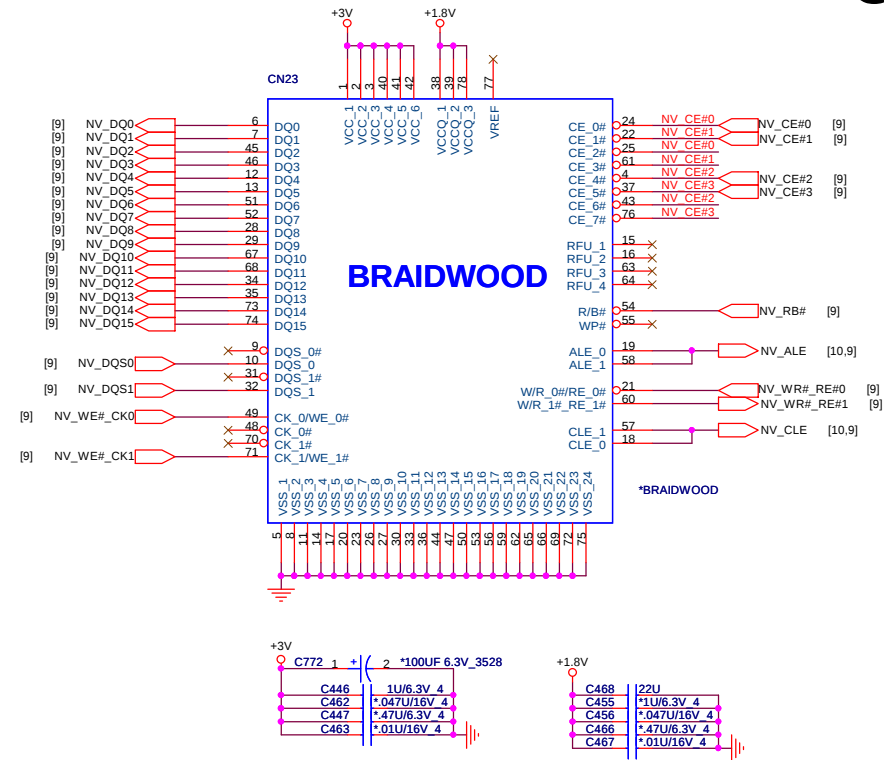


The diagram illustrates the SPI interface between the X6179-10XXXX-8P-SOCKET and the 512K SPI ROM AKE3KZP0001. The X6179-10XXXX-8P-SOCKET is connected to the 512K SPI ROM AKE3KZP0001 via a 33.4 ohm resistor (R334) and a 10K resistor (R329). The 3VPCU is connected to the X6179-10XXXX-8P-SOCKET via a 33.4 ohm resistor (R332) and a 10K resistor (R329). The X6179-10XXXX-8P-SOCKET is connected to the 512K SPI ROM AKE3KZP0001 via a 33.4 ohm resistor (R334) and a 10K resistor (R329). The 512K SPI ROM AKE3KZP0001 is connected to the X6179-10XXXX-8P-SOCKET via a 33.4 ohm resistor (R334) and a 10K resistor (R329).



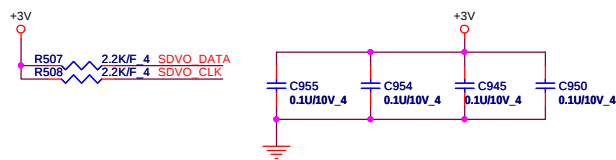
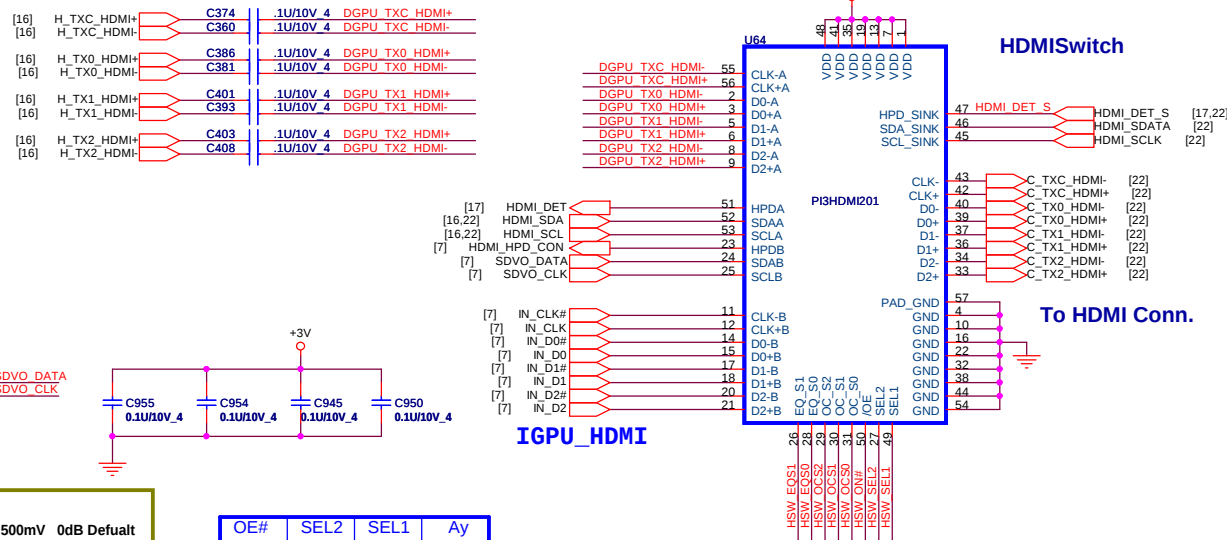
30





Size Custom	Document Number HDMI Switch / Power CTRL	Rev A
Date: Thursday, April 15, 2010		Sheet 32 of 43

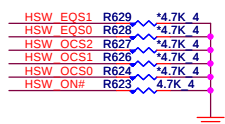
DGPU HDMI



OC SETTING

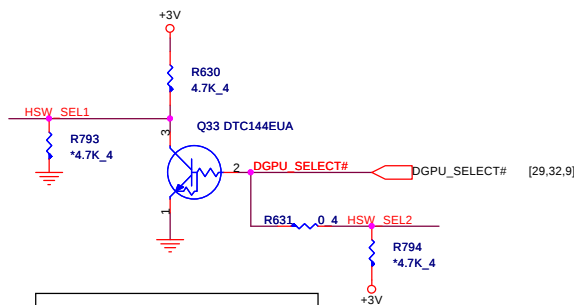
S2 S1 S0 = 1 : 1 : 1	500mV	0dB	Default
S2 S1 S0 = 1 : 1 : 0	750mV	0dB	
S2 S1 S0 = 1 : 0 : 1	1000mV	0dB	
S2 S1 S0 = 1 : 0 : 0	600mV	0dB	
S2 S1 S0 = 0 : 1 : 1	500mV	0dB	
S2 S1 S0 = 0 : 1 : 0	500mV	1.5dB	
S2 S1 S0 = 0 : 0 : 1	500mV	3.5dB	
S2 S1 S0 = 0 : 0 : 0	500mV	6dB	

OE#	SEL2	SEL1	Ay
0	X	1	A
0	1	0	B



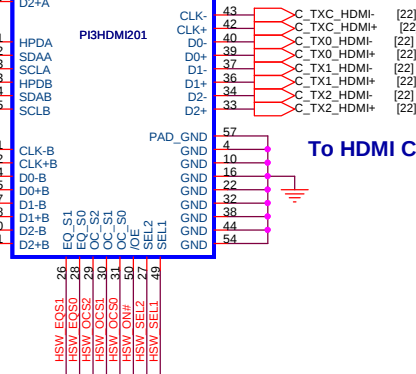
EQ SETTING

S1 S0 = 1 : 1 3dB Default
S1 S0 = 1 : 0 8dB
S1 S0 = 0 : 1 3dB
S1 S0 = 0 : 0 15dB

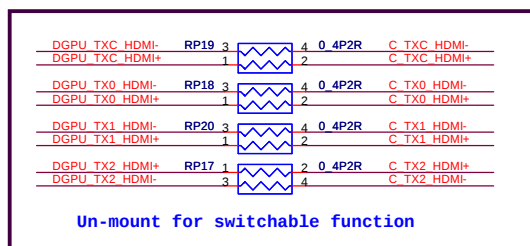
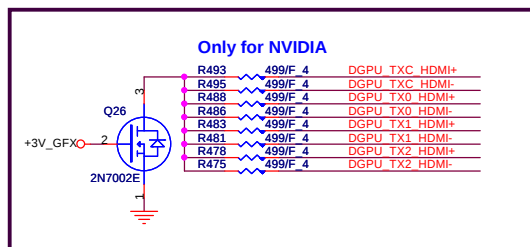


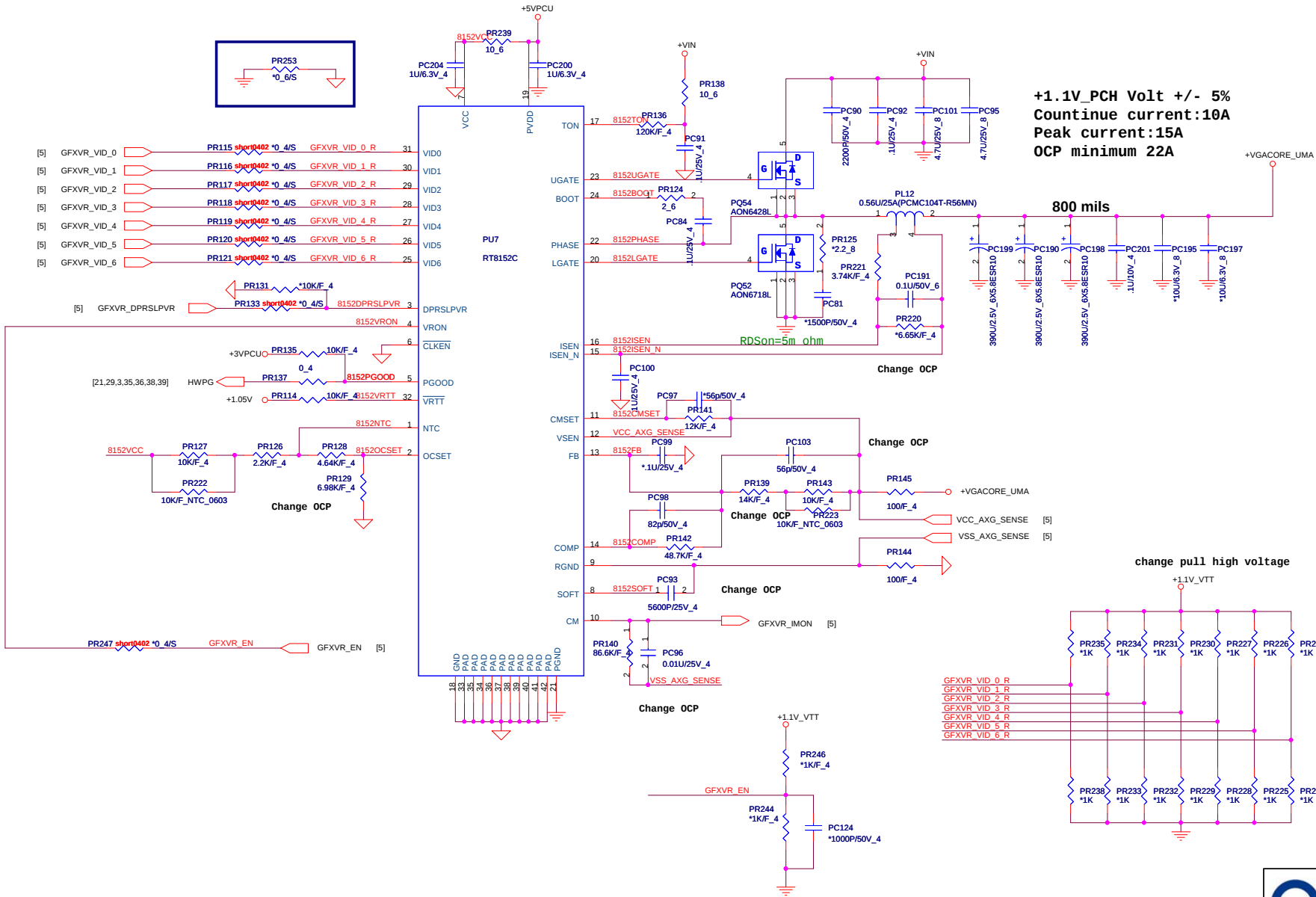
Mount R793 and R794 for UMA only

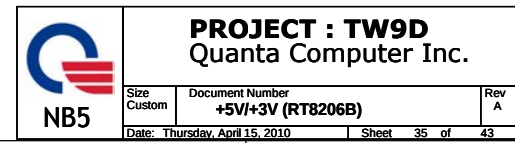
HDMI Switch

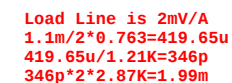


To HDMI Conn.









OCP
 $40\mu A / 2 * 1.21K = 24.2mV$
 $24.4mV / 0.763 = 31.72mV$
 $31.72mV * 2 / 1.1m = 57.66A$

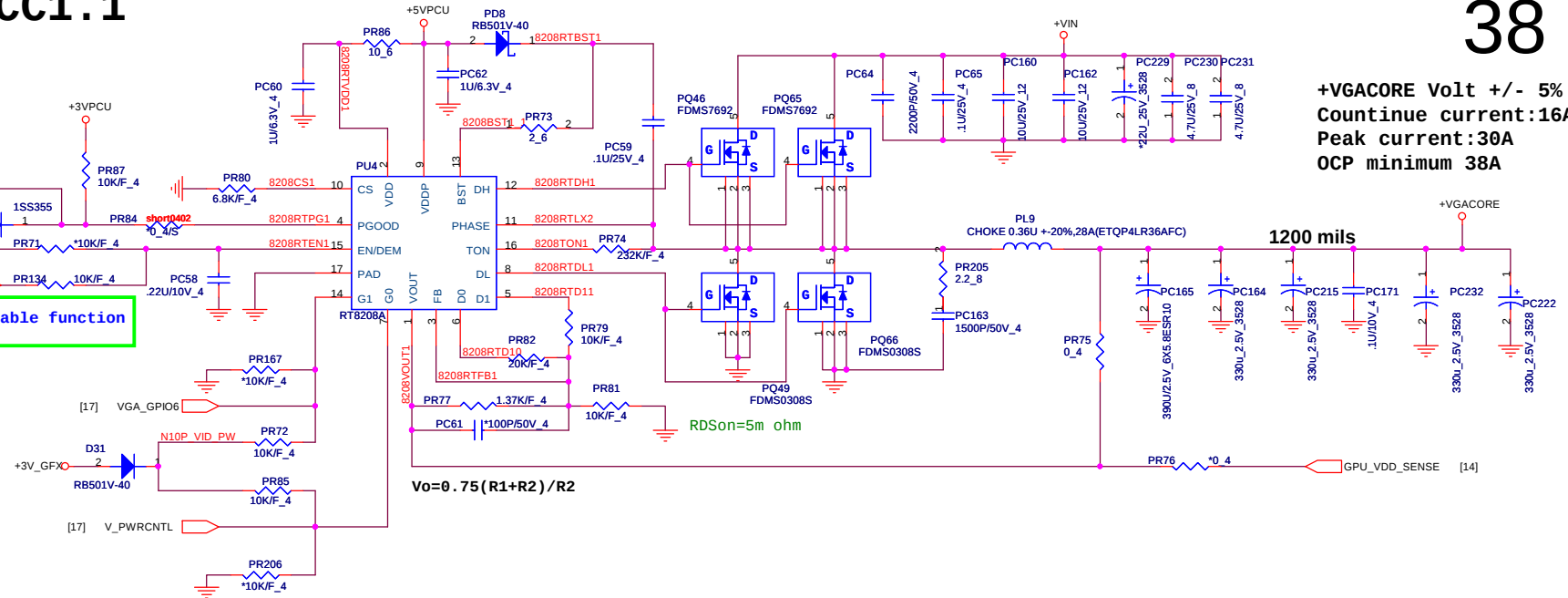
VGA Core & VCC1.1

38

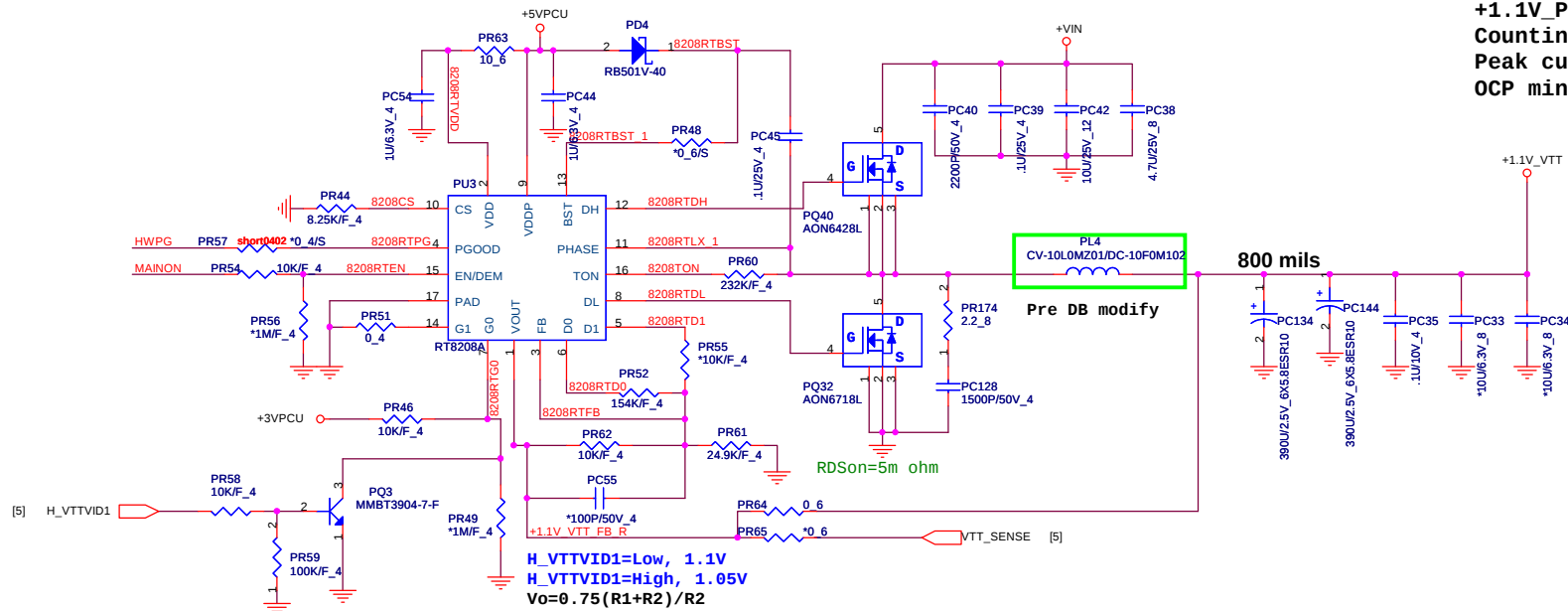
+VGACORE Volt +/- 5%
Countinue current:16A
Peak current:30A
OCP minimum 38A

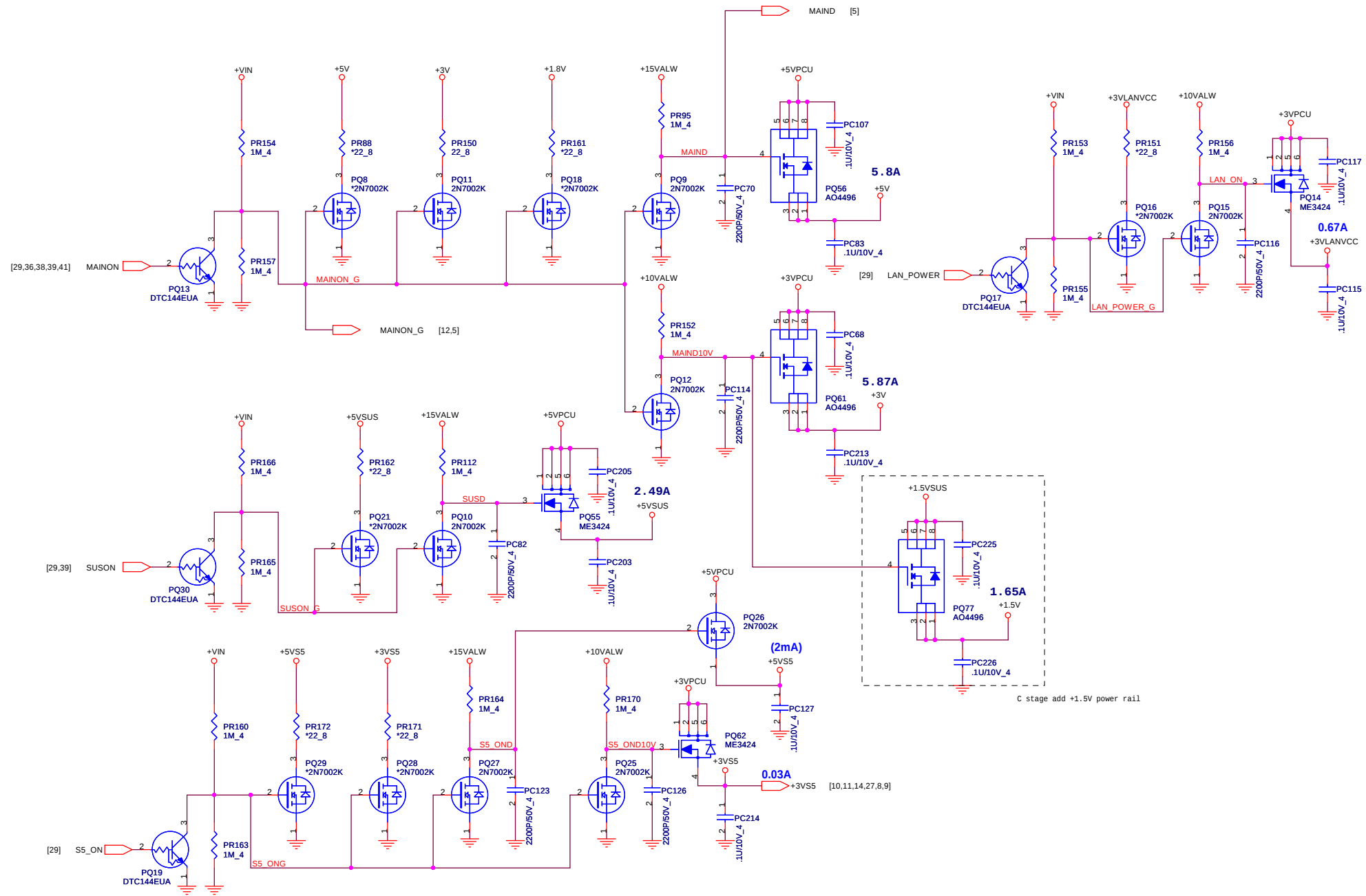
VGA_GPIO6	V_PWRCNTL	N10P-GE
GPI06	GPI05	
0	0	0.85V
0	1	0.90V
1	0	0.95V
1	1	1.0V

PD9 / PR71 un-mount for switchable function



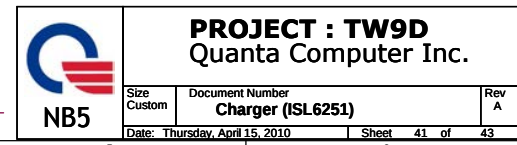
+1.1V_PCH Volt +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A

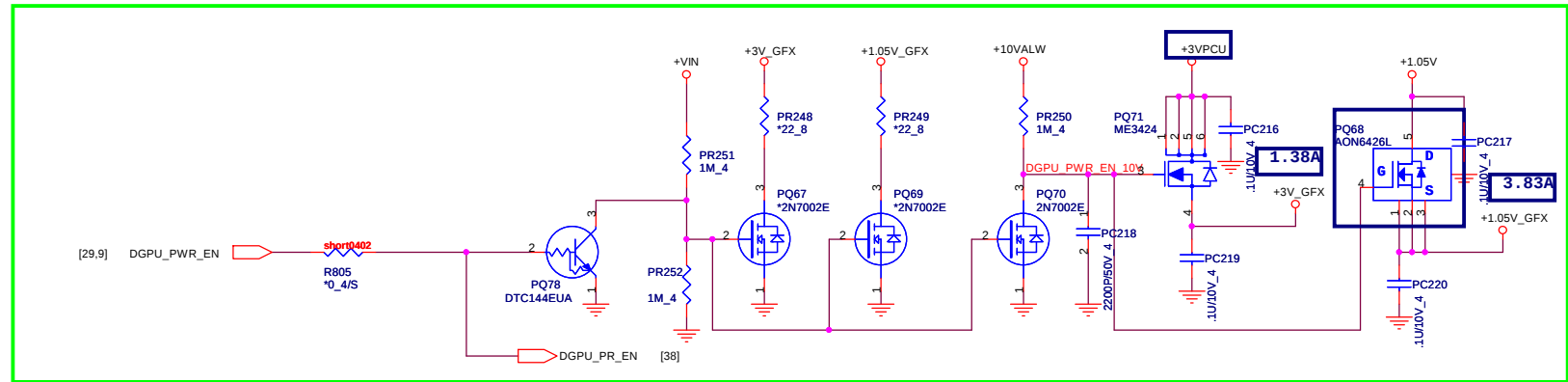




PROJECT : TW9D
Quanta Computer Inc.

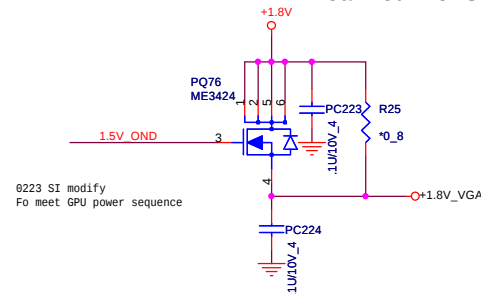
Size	Document Number	Rev
Custom	DISCHARGE/3VS5/5VS5/LAN	A
Date: Thursday, April 15, 2010	Sheet 40 of 43	



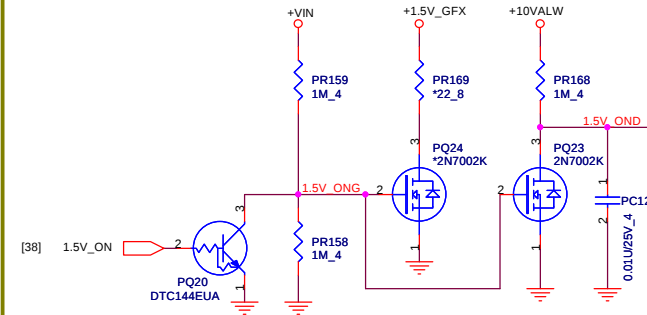


For Discrete or switchable Only

+1.8 Volt +/- 0.1V
Continue current: 0.3A
Peak current: 1A

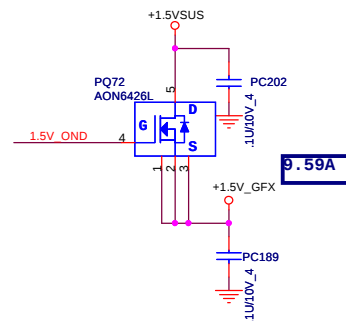


For Discrete or switchable Only



Change PC119 to 0.01u/25v as Discrete power sequence

For Discrete or switchable Only



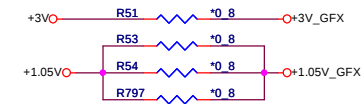
R51 co-lay PQ71
R53/R54 co-lay PQ68

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

For Hybrid DGPU Power Rails Sequence

1. +3V_GFX, +1.05V_GFX
2. +VGA_CORE -> DGPU_PG
3. 1.5V_GFX, +1.8V_GFX

For Discrete Only



PROJECT : TW9D
Quanta Computer Inc.

Size
A3

Document Number
Switchable Power

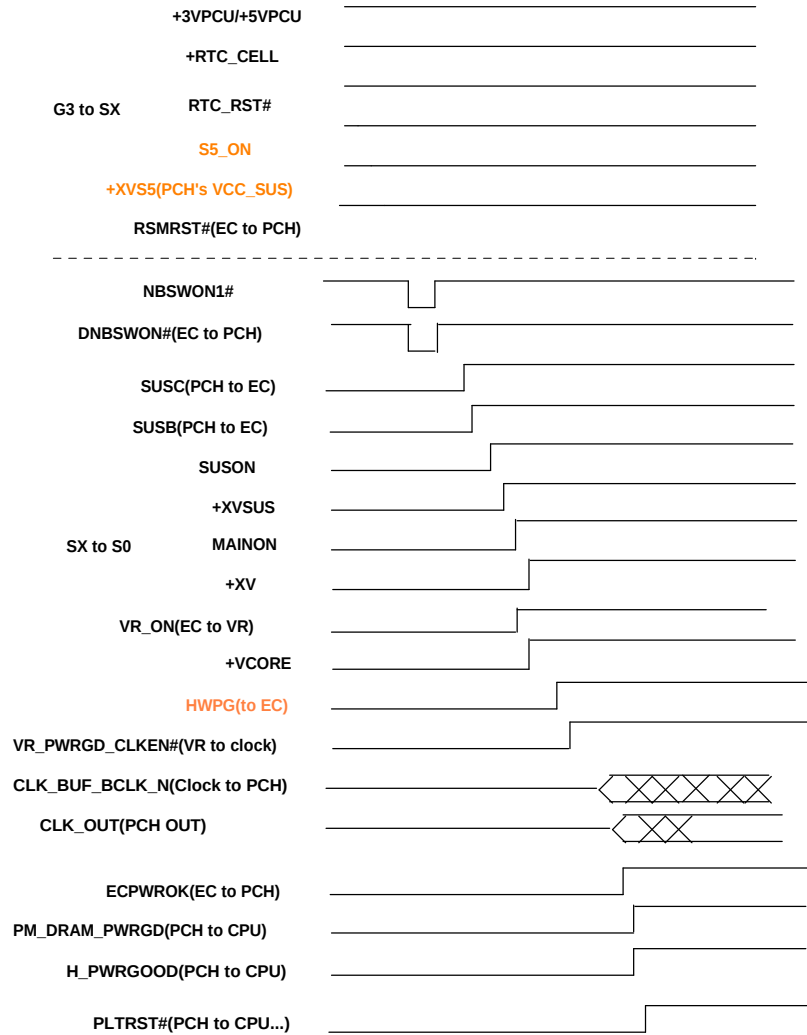
Rev
A

Date: Thursday, April 15, 2010

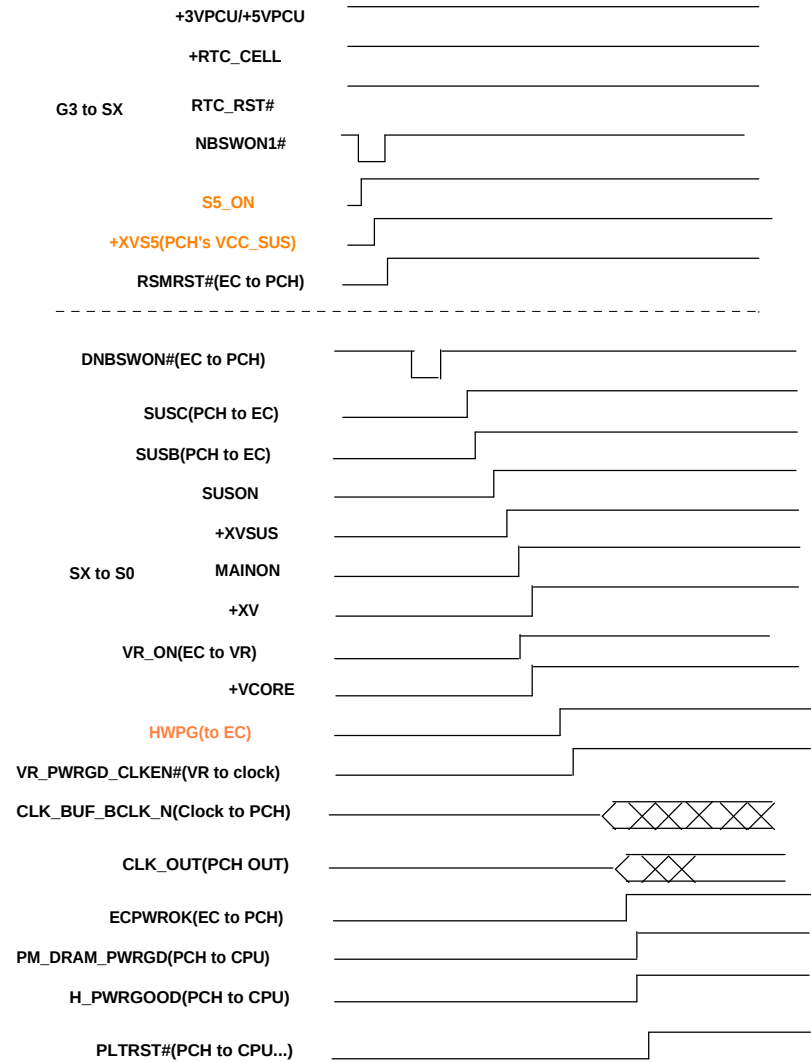
Sheet 42 of 43

Power up sequence

LAN/RTC WAKE UP ENABLE.



LAN/RTC WAKE UP DISABLE.



PROJECT : TW9D
Quanta Computer Inc.

Size Custom	Document Number Power up sequence	Rev A
Date: Thursday, April 15, 2010		Sheet 43 of 43