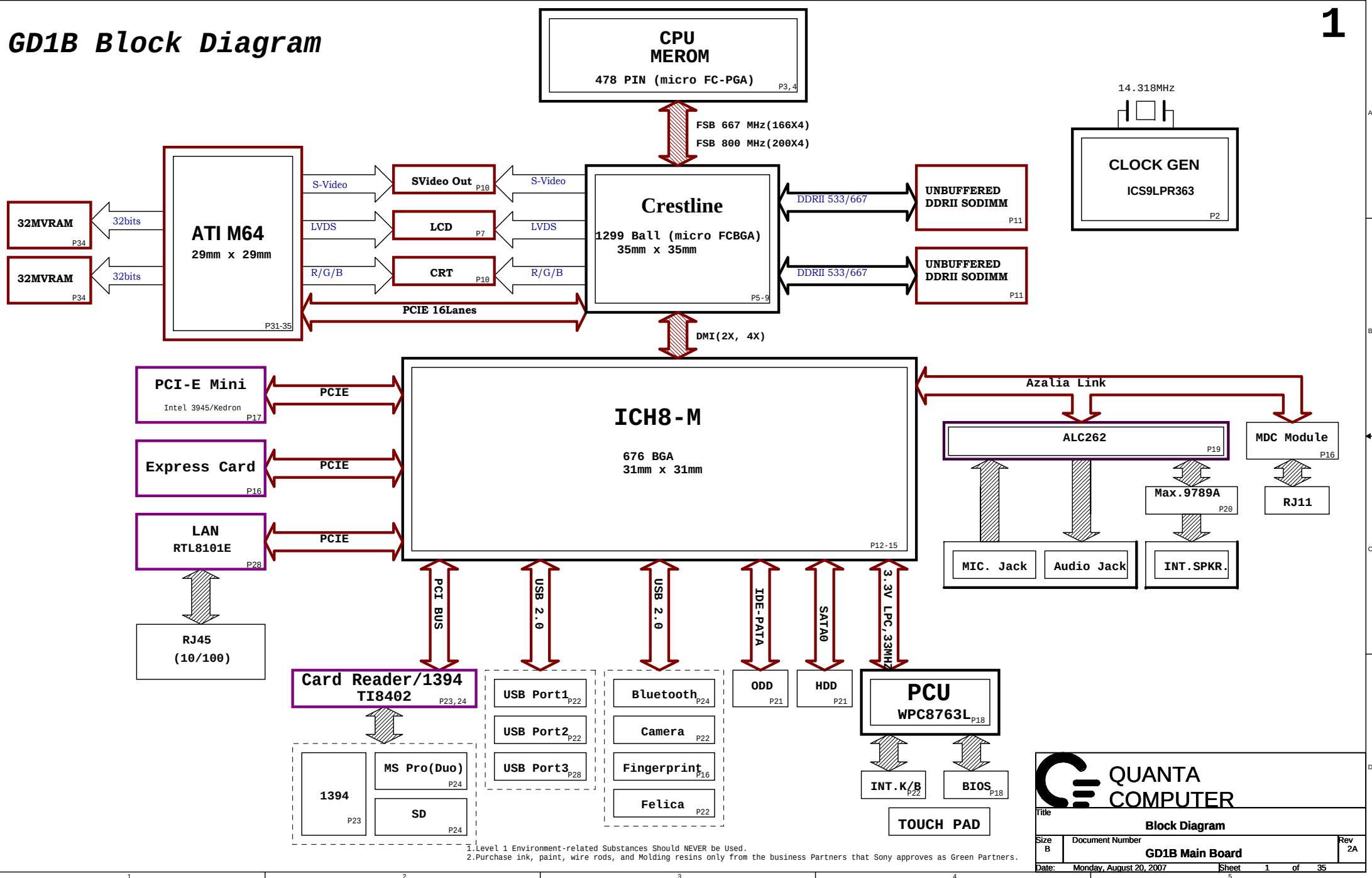


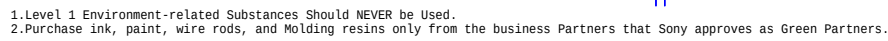
GD1B Block Diagram

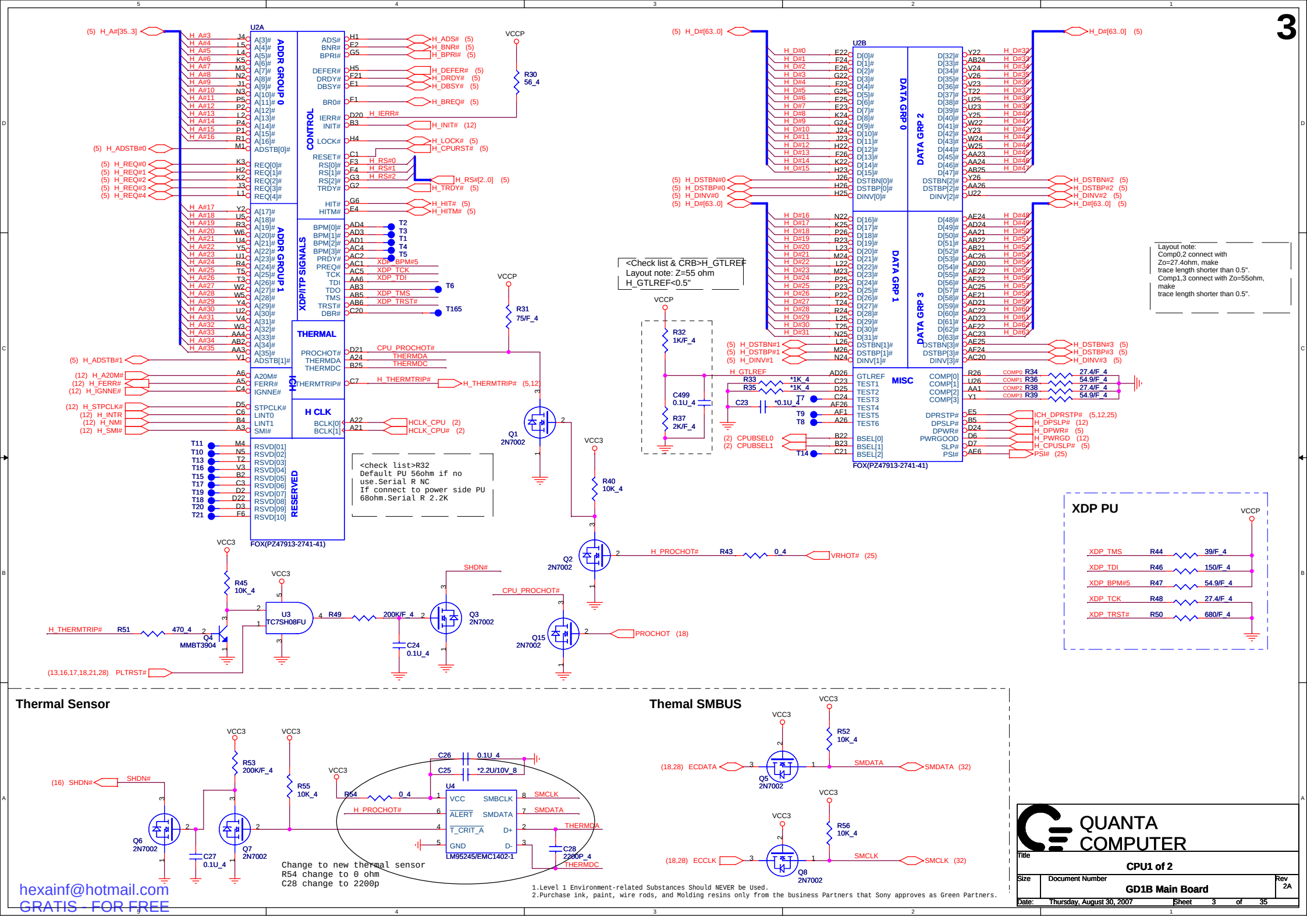
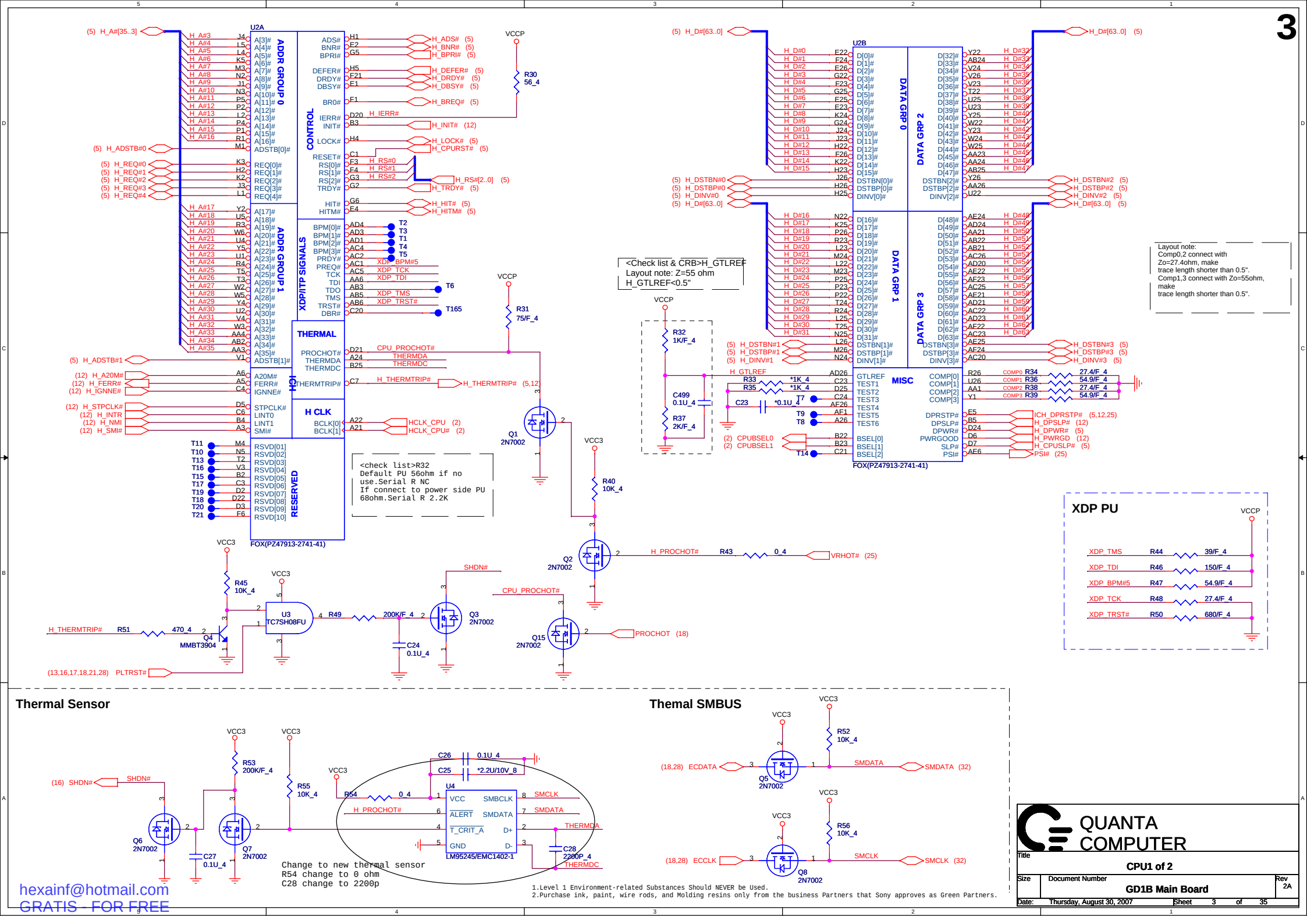
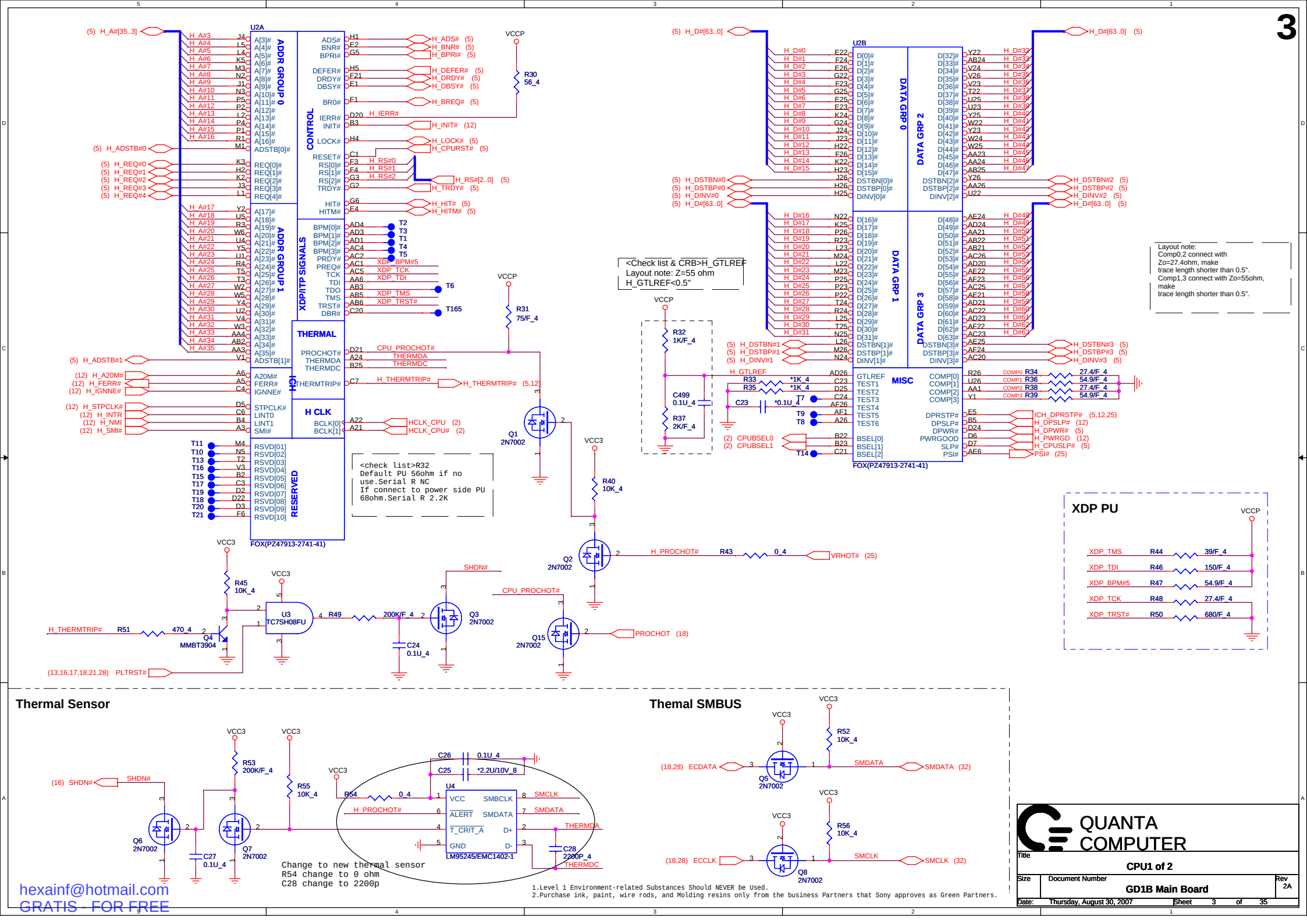
1



1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER		
Title Block Diagram		
Size B	Document Number GD1B Main Board	Rev 2A
Date: Monday, August 20, 2007	Sheet 1	of 35



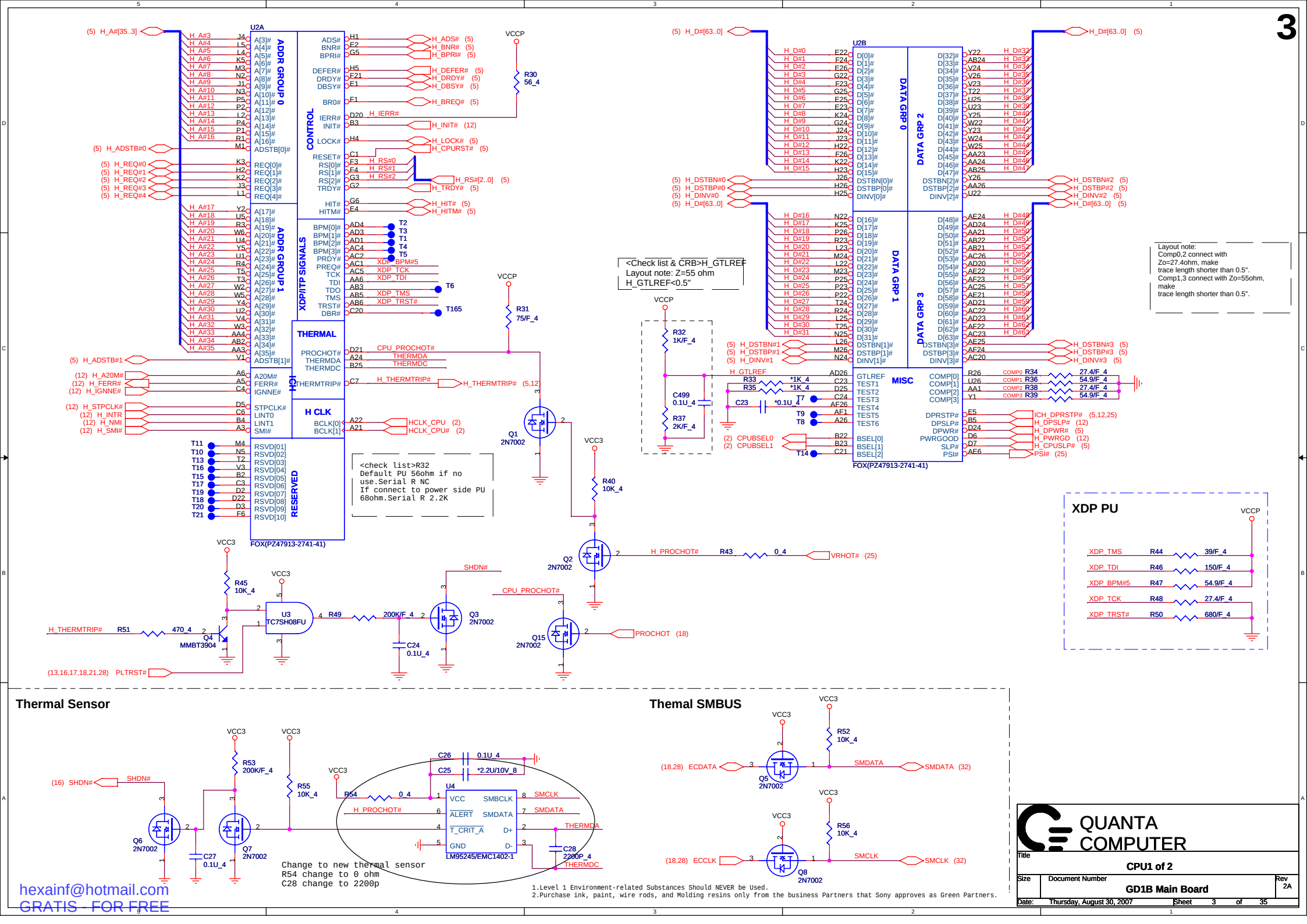
[illegible]

hexainf@hotmail.com
GRATIS FOR FREE

Change to new thermal sensor
R54 change to 0 ohm
C28 change to 2200p

1.Level 1 Environment-related Substances should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER
CPU1 of 2
GD1B Main Board
Rev 2A
Thursday, August 30, 2007
Sheet 3 of 35



hexainf@hotmail.com
GRATIS FOR FREE

Change to new thermal sensor
R54 change to 0 ohm
C28 change to 2200p

1.Level 1 Environment-related Substances should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA
COMPUTER

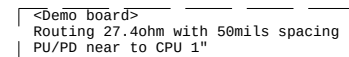
File
CPU1 of 2

Size
Document Number
GD1B Main Board

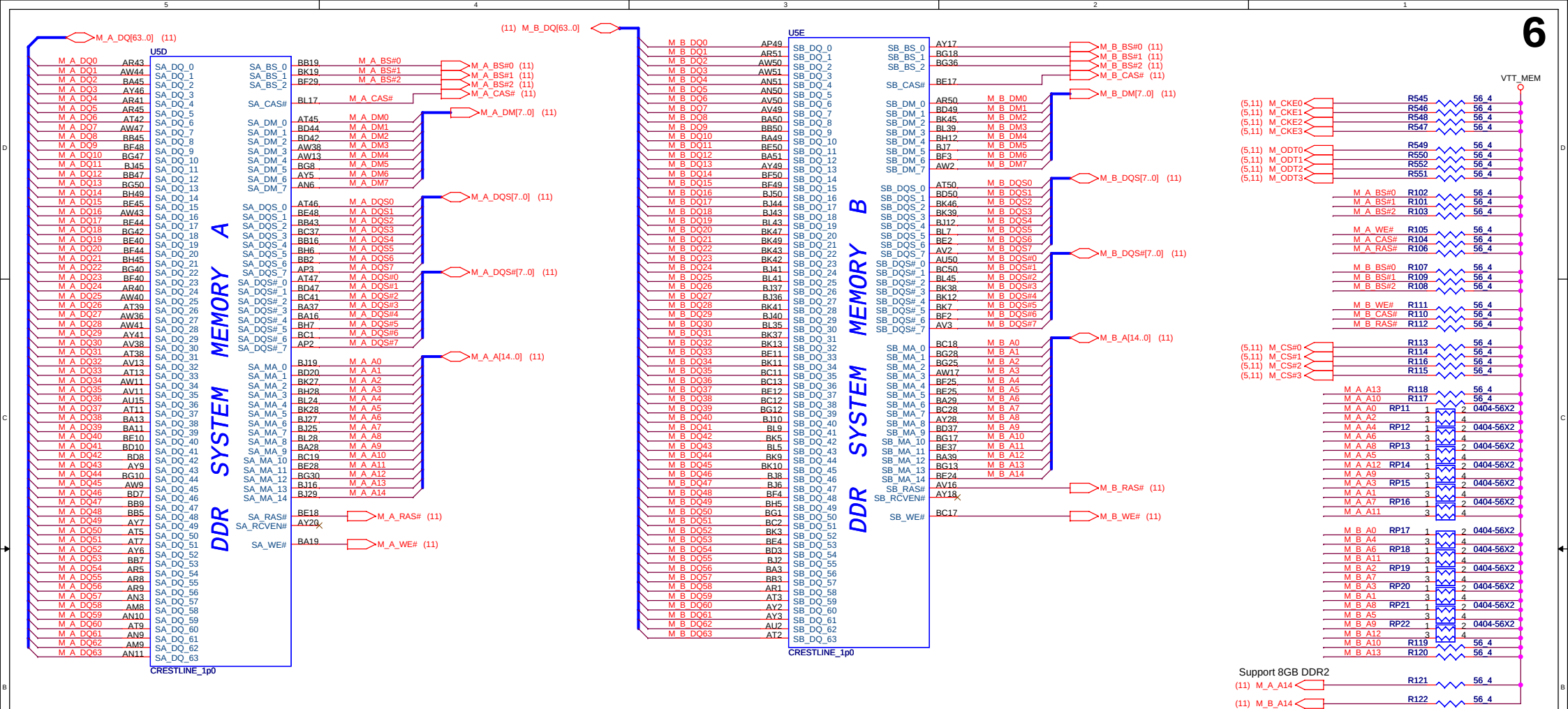
Date
Thursday, August 30, 2007

Sheet
3 of 35

Rev
2A

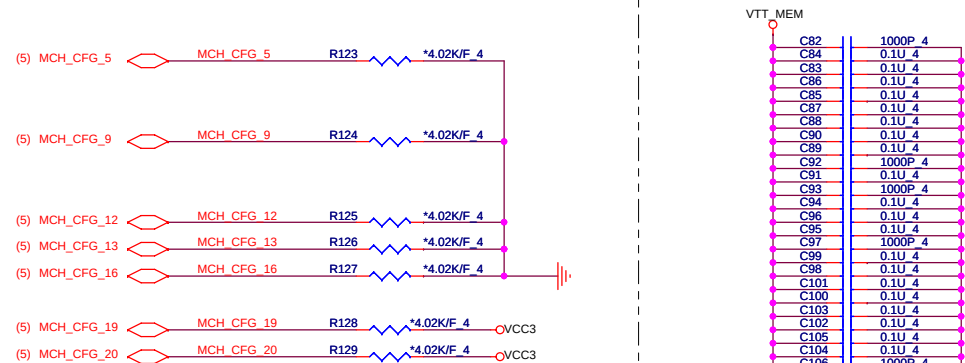






GMCH Strap pin description

Low		High
CGF5	DMix2	* DMix4
CGF6		RSDV for 945GMS
CGF7	RSDV	* CPU type: Mobile CPU
CGF9	PCIE Graphics lan : Reverse Lane	* PCIE Graphics lan : Normal operation
CGF10		reserved
CGF11		reserved
CGF16	FSB Dynamic ODT Disabled	* FSB Dynamic ODT Enabled
CGF18	* GMCH core: 1.05V	GMCH core: 1.5V
CGF19	* DMI LANE Normal	DMI LANE Reversed
CGF20	* only SDVO or PCIE x1 is operational	SDVO and PCIE x1 are operation simultaneously via the PEG port
CGF[13:12]	00 = Partial clock gating disable 01 = XOR mode enabled 10 = All-Z mode enabled * 11 = Normal Operation(Default)	
int.Pull-down : CGF 18,19,20		
int.Pull-high : CGF CGF 3-17		



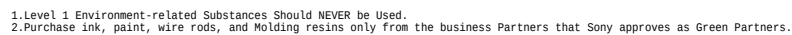
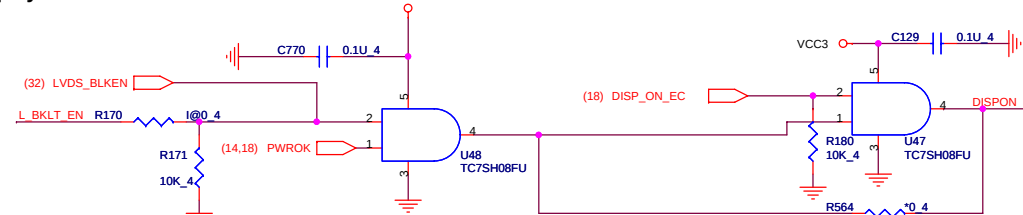
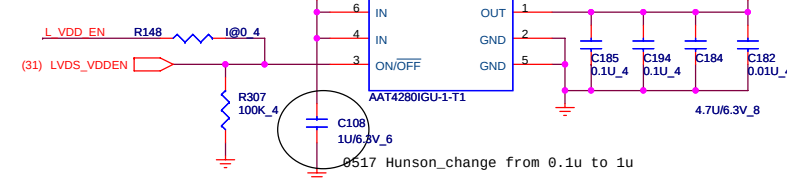
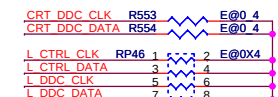
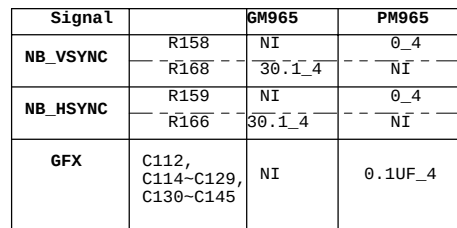
- Place one cap close to every 2 pull-up resistors terminated to VccSus0_9 (Total 0.1u x 26)

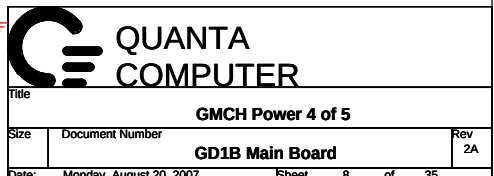


Title **GMCH DDR II 2 of 5**

Size	Document Number
	GD1B Main Board

Date: Monday, August 20, 2007 Sheet 6 of 35

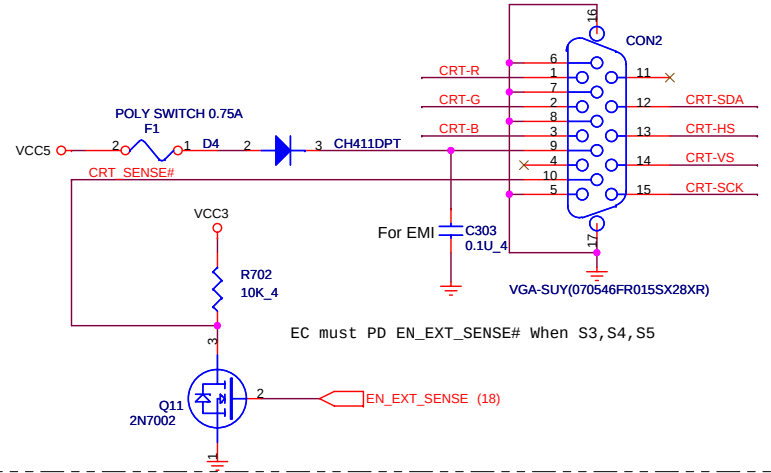
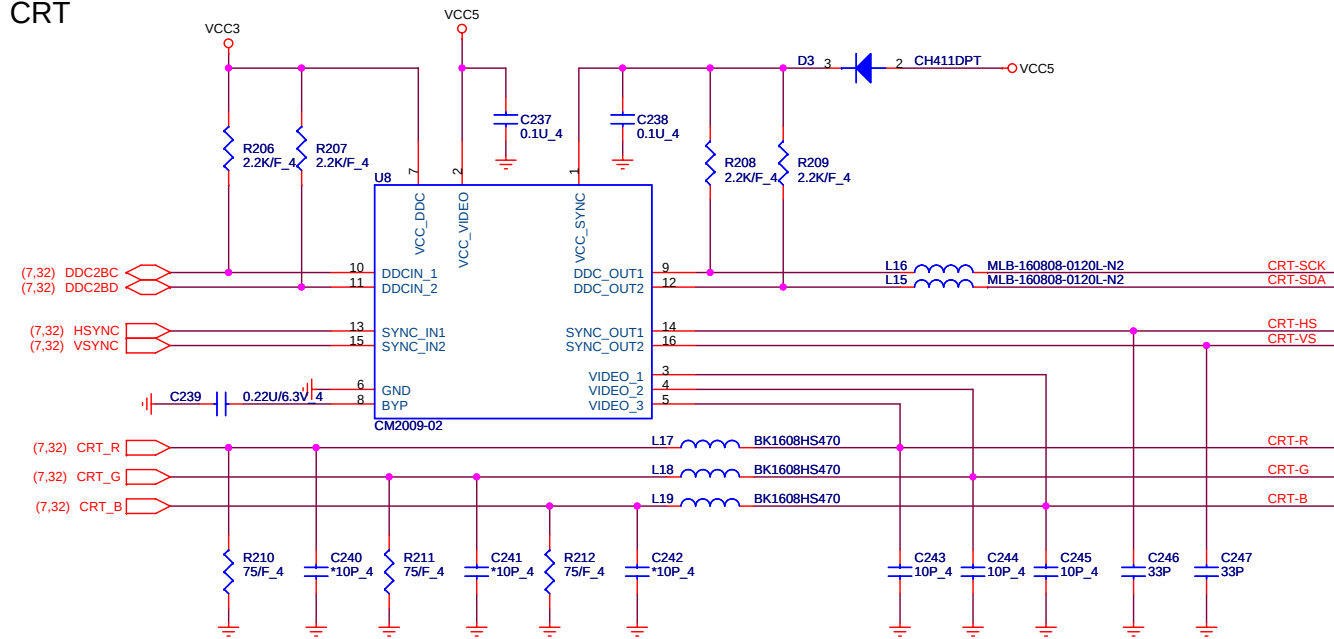




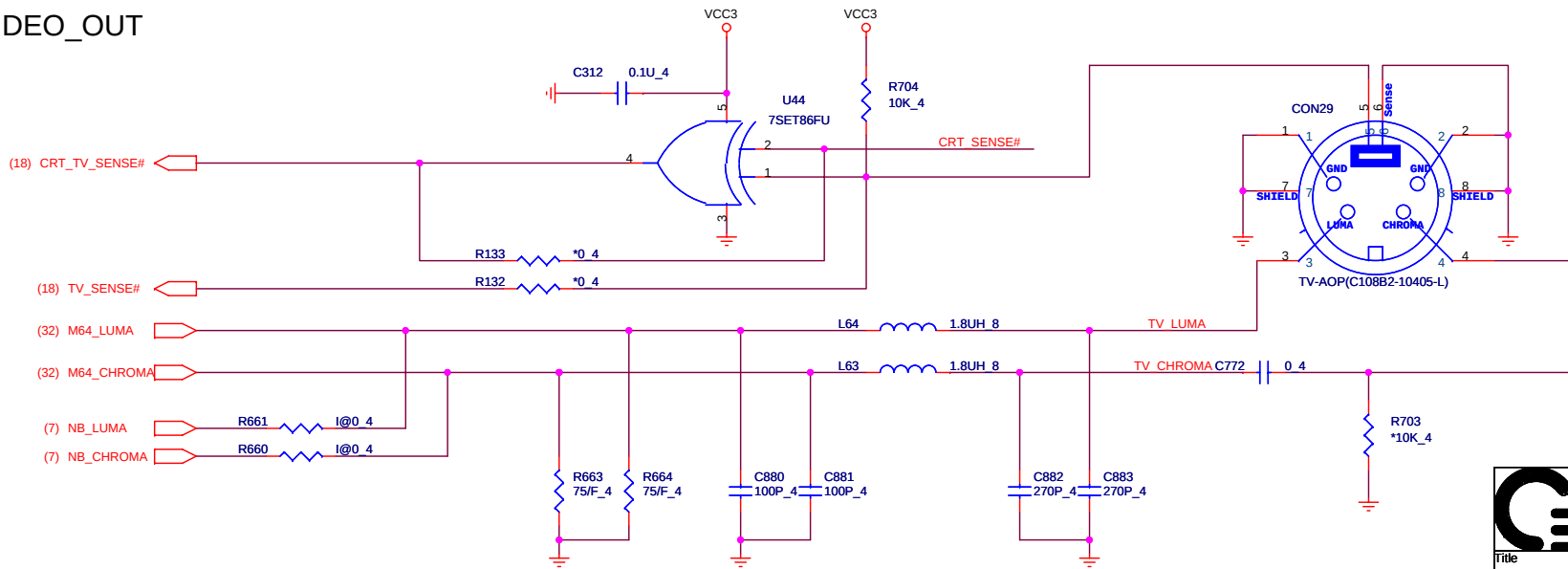
Title			
GMCH Power 4 of 5			
Size	Document Number		Rev
	GD1B Main Board		2A
Date:	Monday, August 20, 2007	Sheet	0 of 25

CRT

10



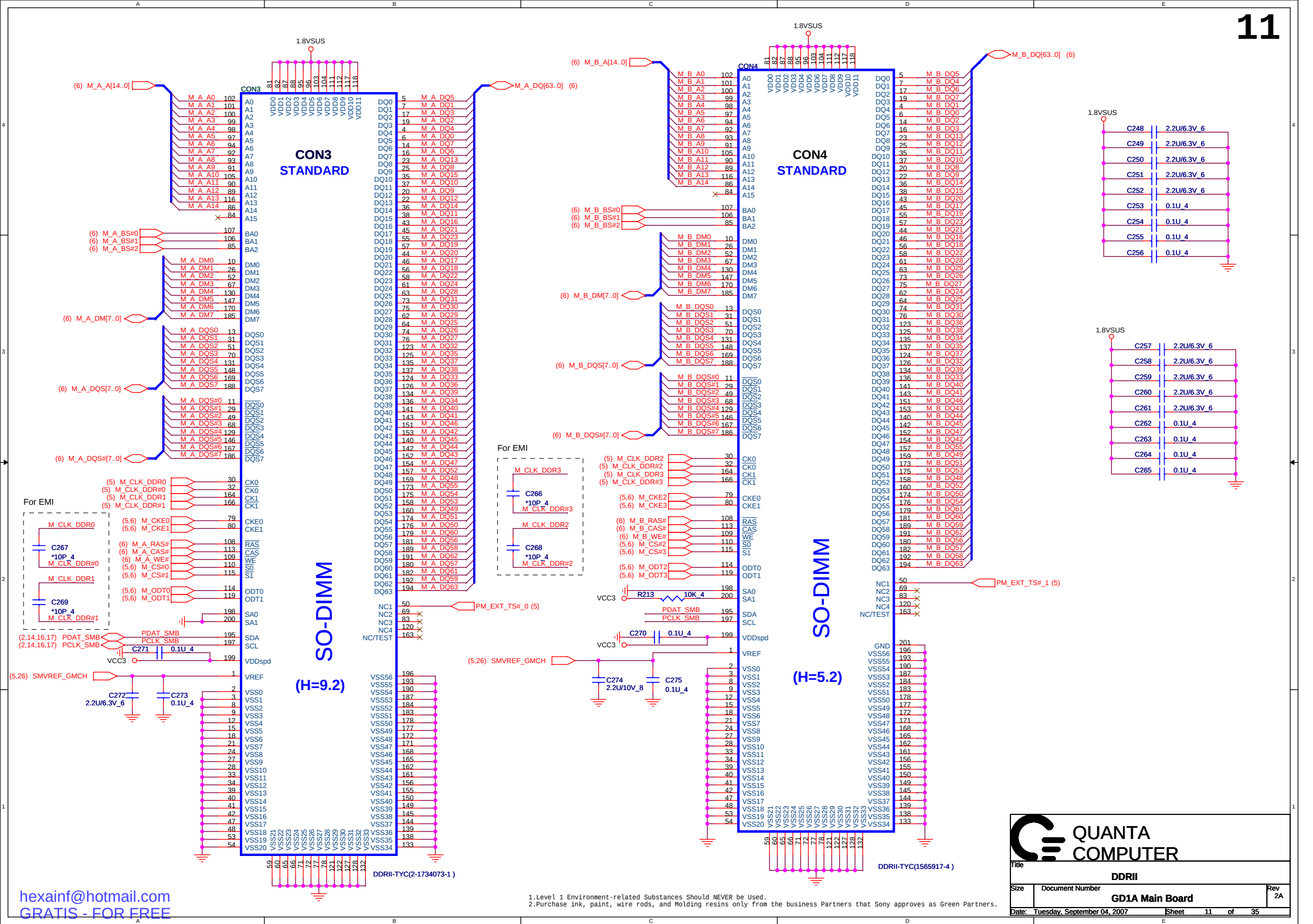
S-VIDEO_OUT

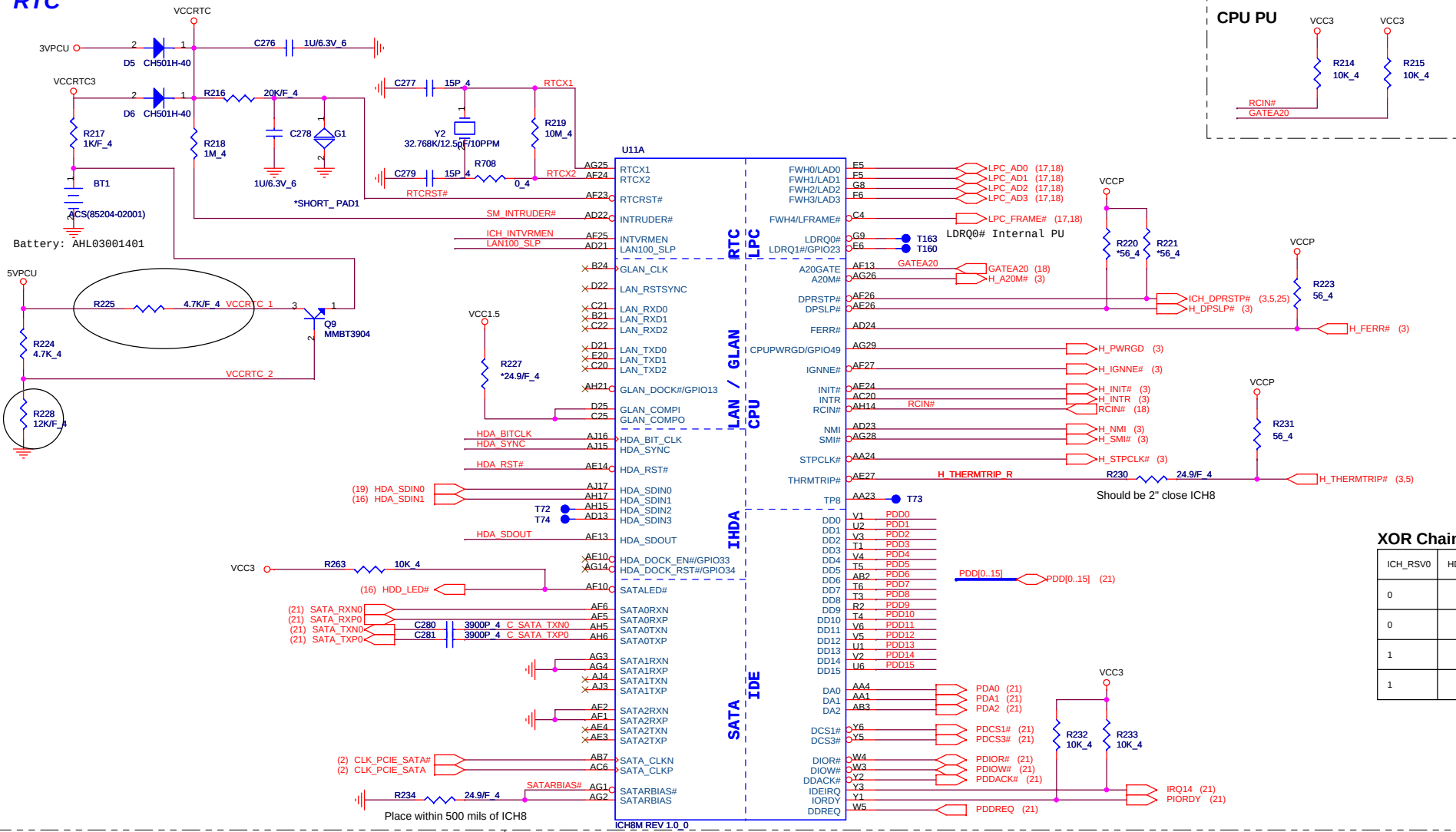


**QUANTA
COMPUTER**

Title		
CRT & S-VIDEO		
Size	Document Number	Rev
B	GD1B Main Board	2A
Date:	Monday, August 20, 2007	Sheet 10 of 35

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.





XOR Chain Entrance Strap

ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIE port config bit 1

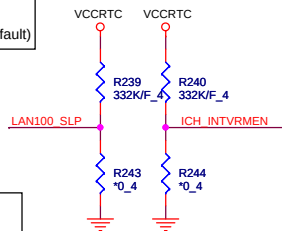
ICH8 strap

ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1.05)

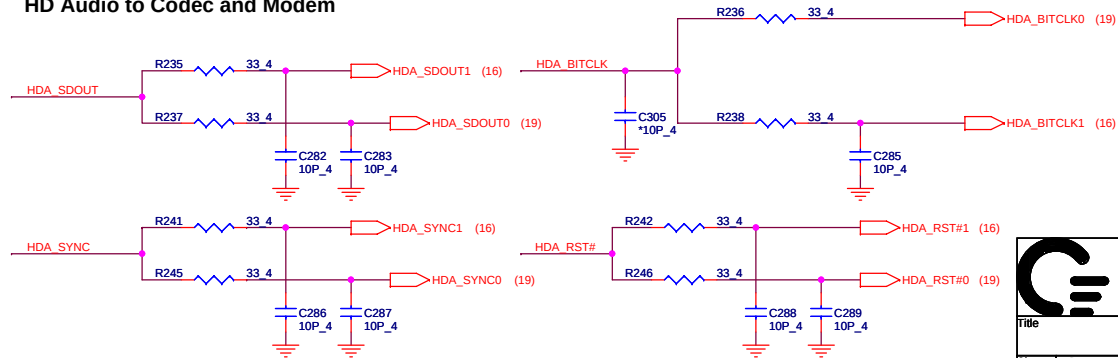
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---

ICH_INTVRMEN	Low = Disable High = Enable(Default)
--------------	---

ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)



HD Audio to Codec and Modem



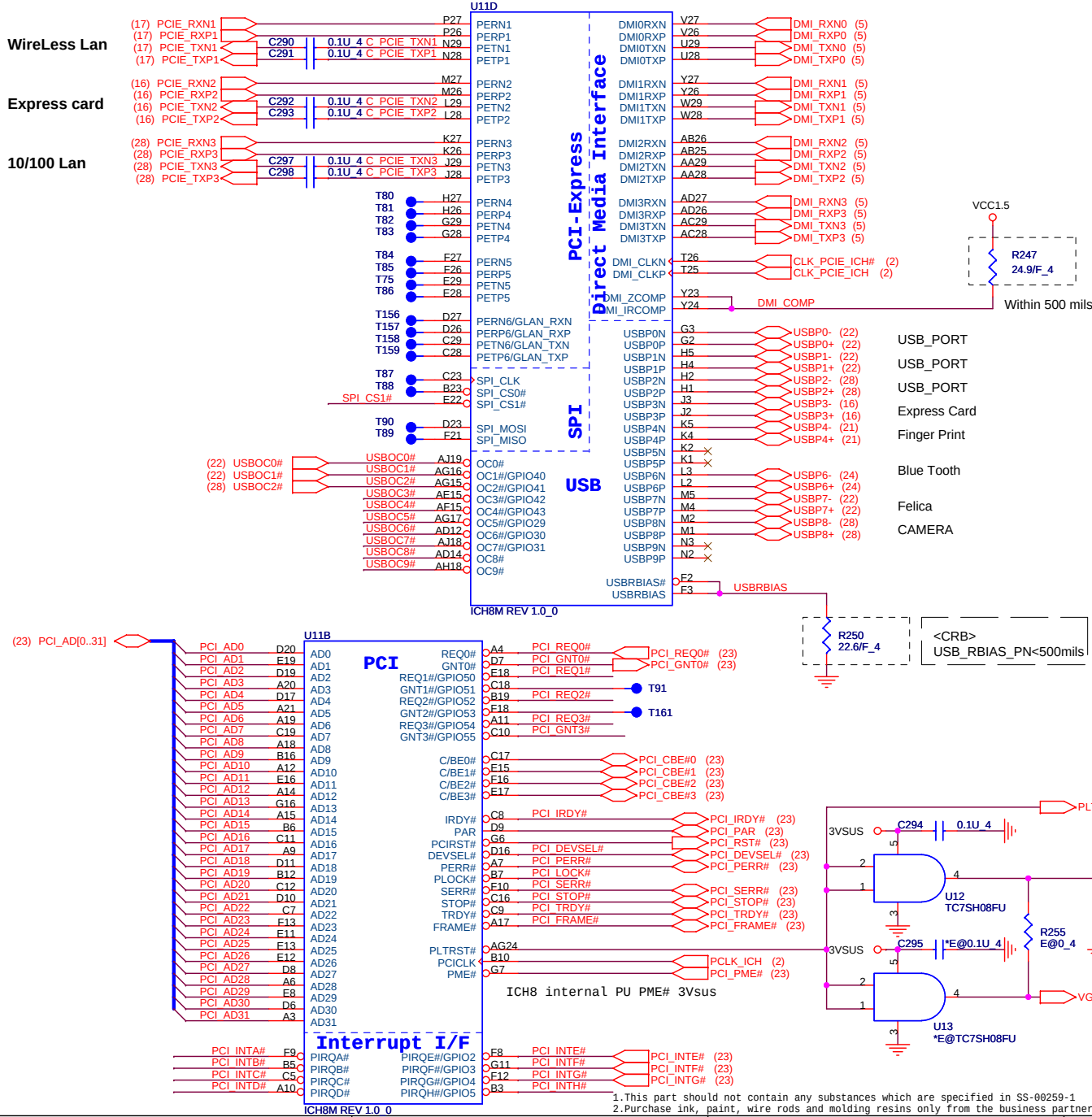
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

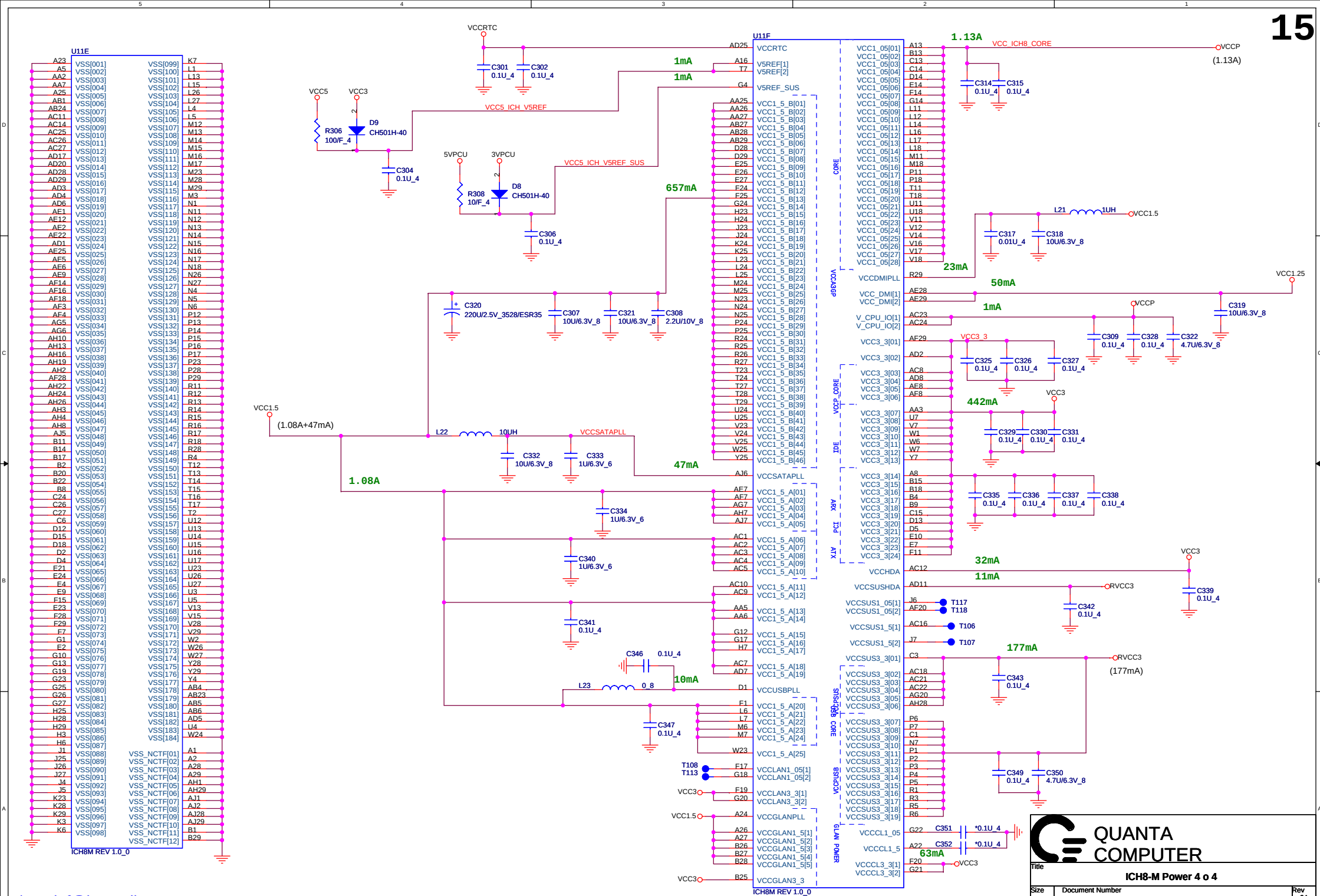
QUANTA COMPUTER

Title: ICH8-M HOST 1 of 4

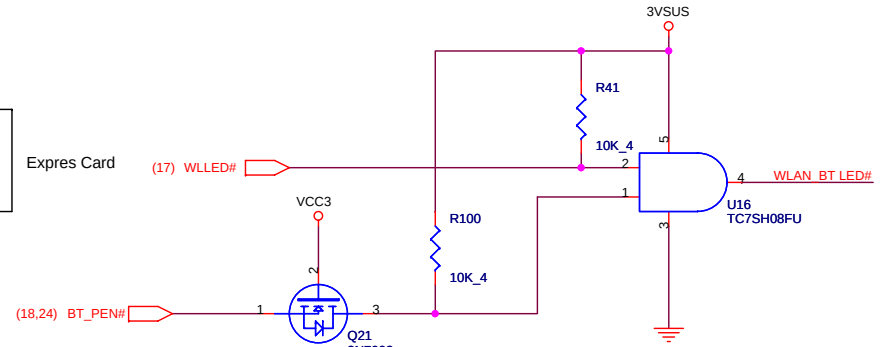
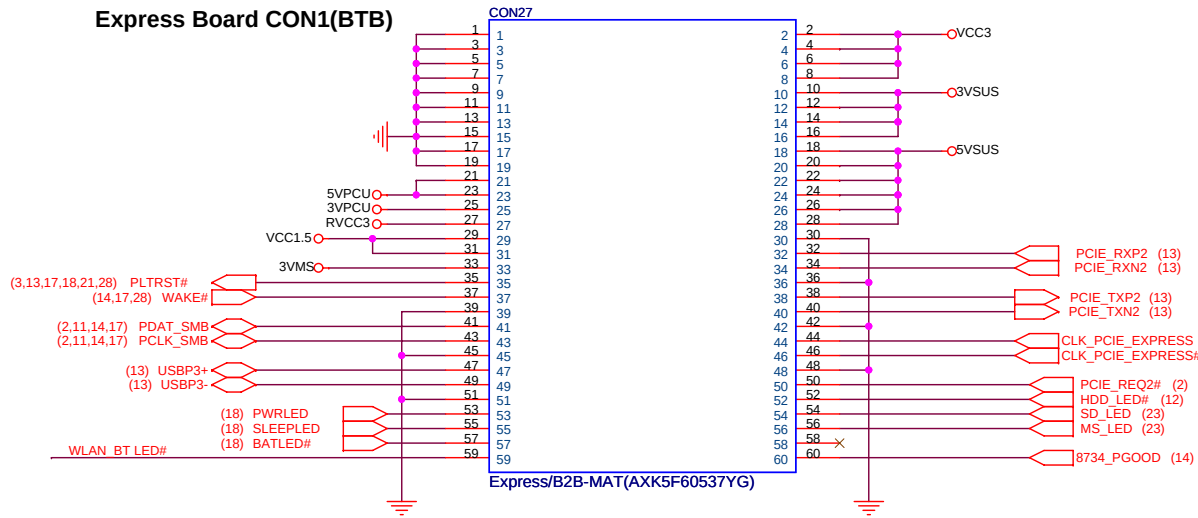
Size: Document Number: Rev 3A

Date: Monday, August 20, 2007 Sheet 12 of 35

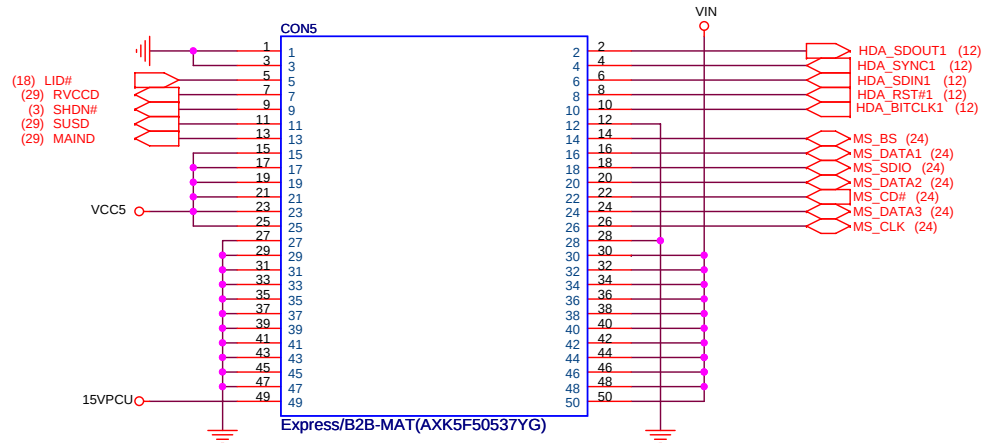




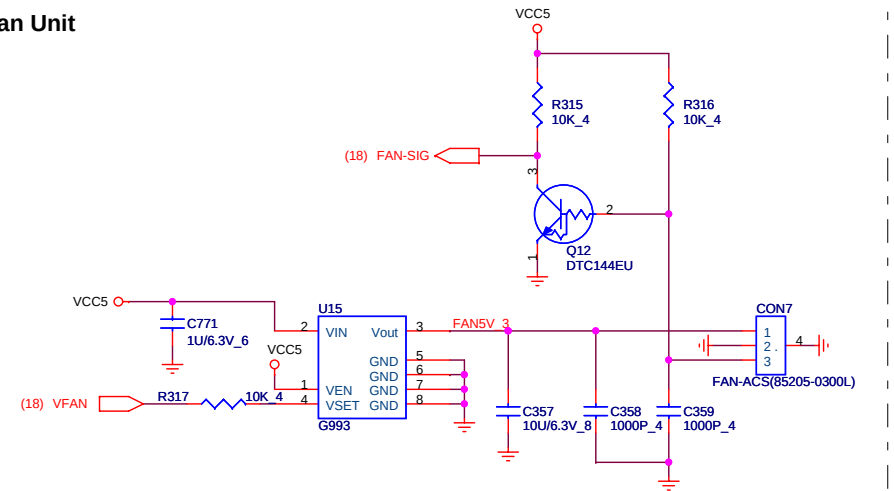
Express Board CON1(BTB)



Express Board CON2(BTB)



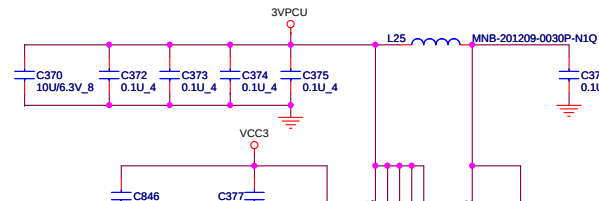
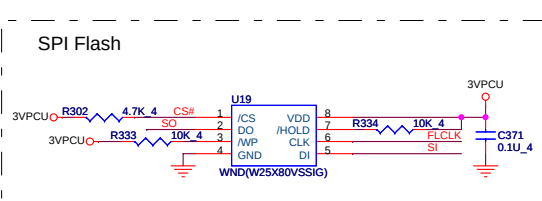
Fan Unit



Title		
Express Card		
Size	Document Number	Rev
B	GD1B Main Board	2A
Date:	Monday, August 20, 2007	Sheet 16 of 35

- This part should not contain any substances which are specified in SS-00259-1.
- Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

SPI Flash



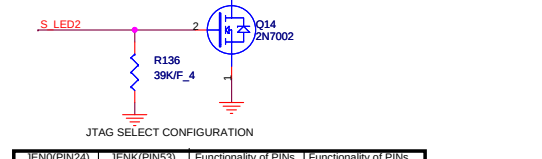
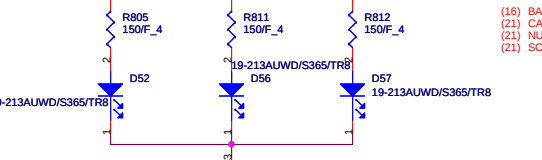
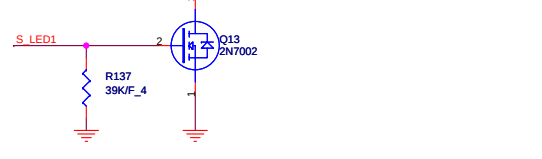
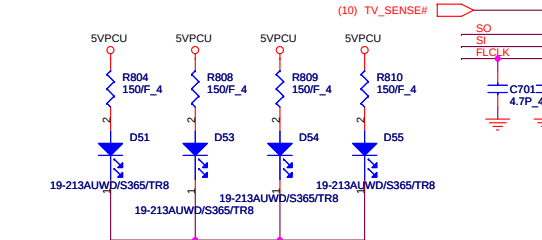
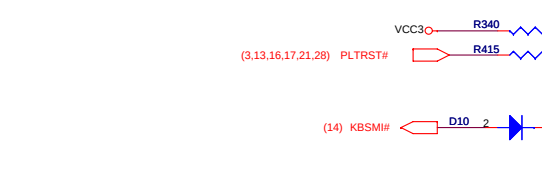
I/O Address	Index	Data
BADDR1-0	1 0	2E 2F
	1 1	4E 4F
0 0	[HCFGBAH, HCFGBAL]	[HCFGBAH, HCFGBAL]+1
0 1		XOR-TREE TEST

DOCK_RST# *BADDR0
DK_BAY_PWEN: BADDR1

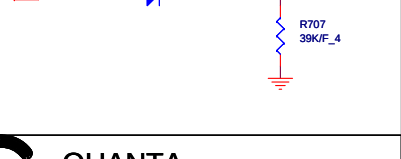
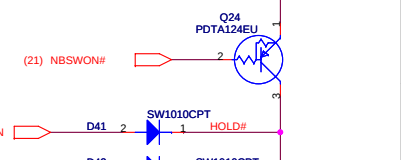
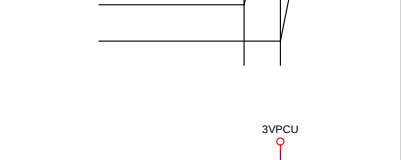
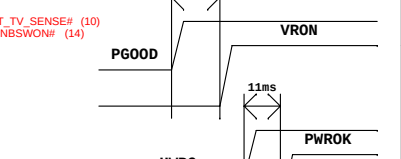
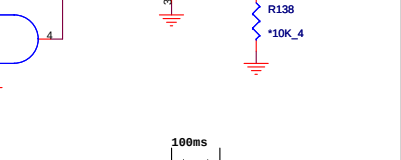
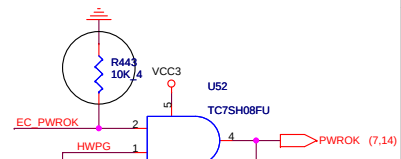
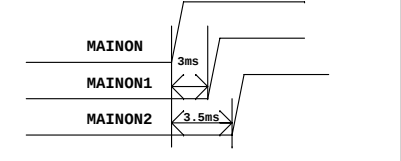
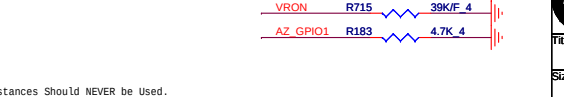
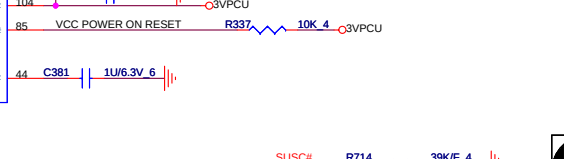
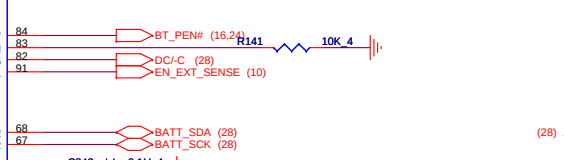
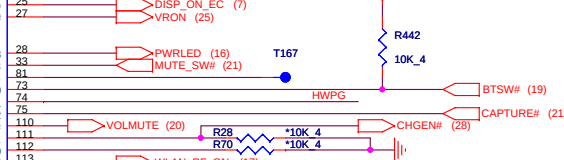
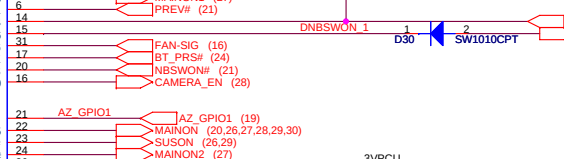
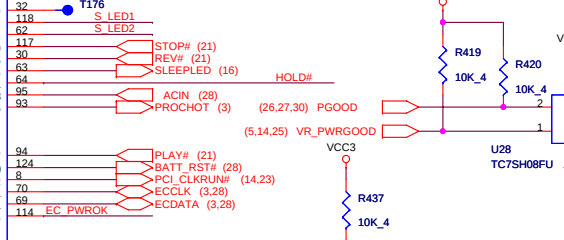
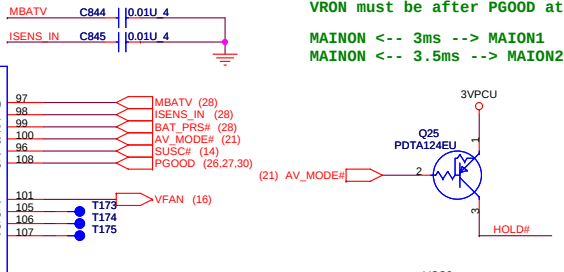
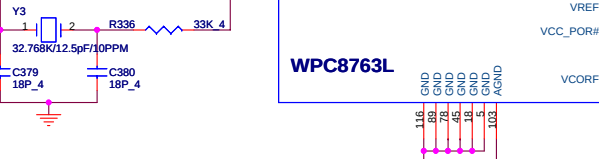
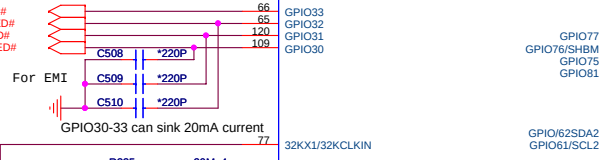
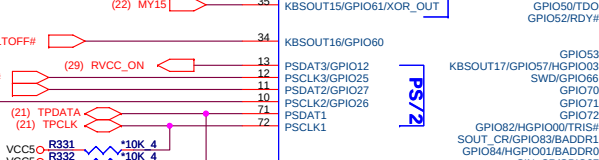
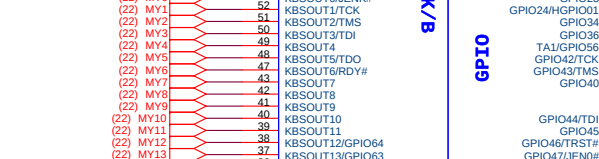
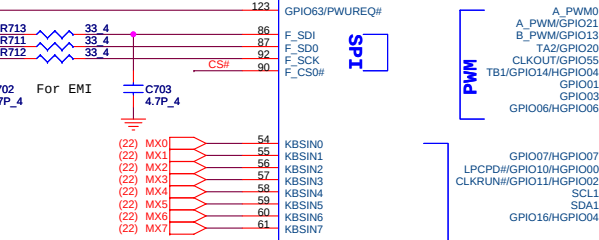
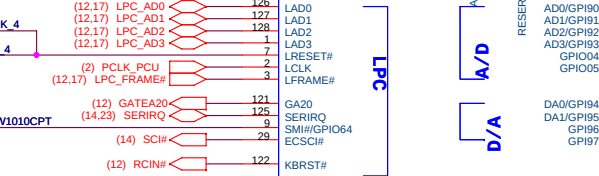
BT_PEN# : SHBM(If = 0 Enable share host BIOS memory)

PWROK must be after HWPG at least 10ms
VRON must be after PGOOD at least 99ms

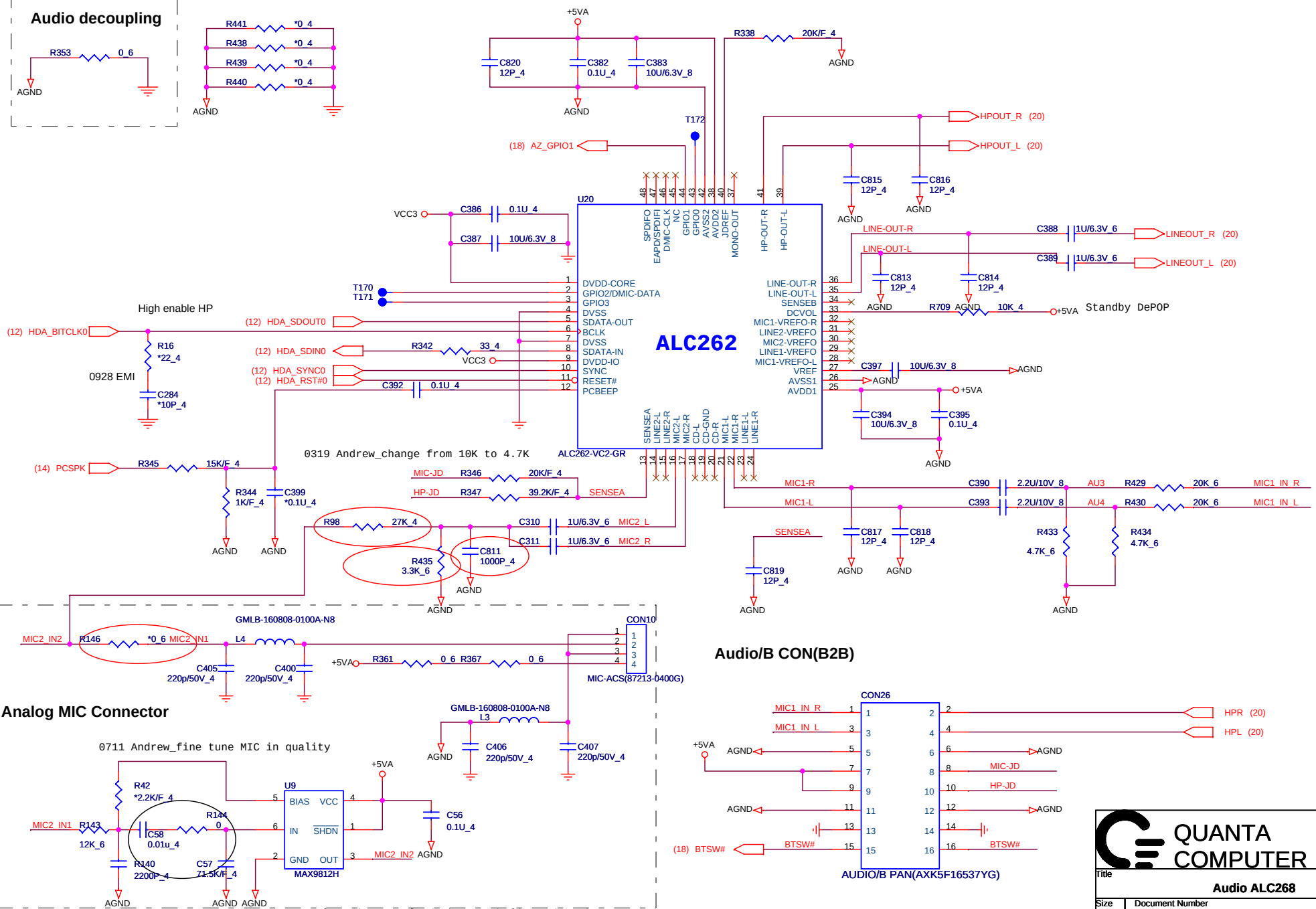
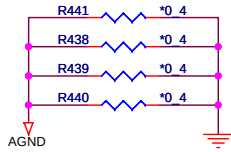
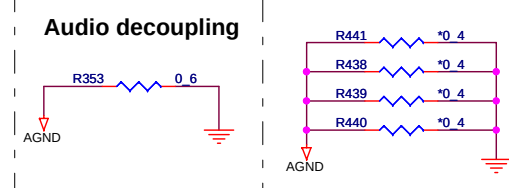
MAINON <-- 3ms --> MAION1
MAINON <-- 3.5ms --> MAION2



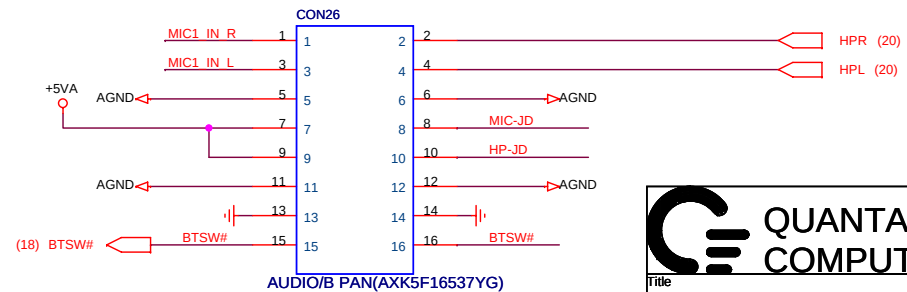
JEN0(PIN24)	JENK(PIN53)	Functionality of PINS (17,20,21,23,25,27)	Functionality of PINS (47,48,50,51,52)
NC	NC	GPIO	KEYBOARD OUTPUT
10K PD	NC	JTAG Signal	KEYBOARD OUTPUT
NC	10K PD	GPIO	JTAG Signal
10K PD	10K PD	Illegal Strap combination	



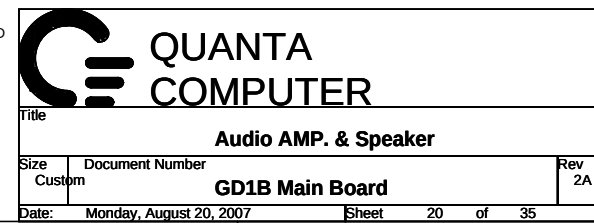
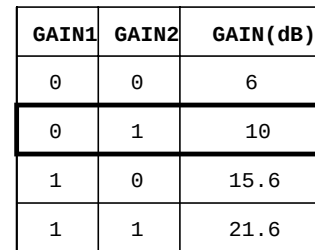
Audio decoupling



Audio/B CON(B2B)

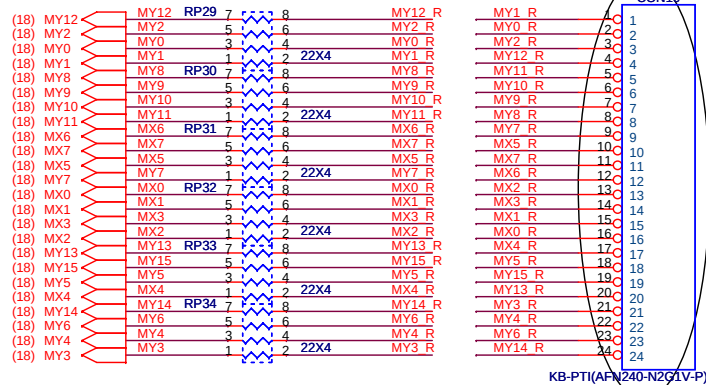
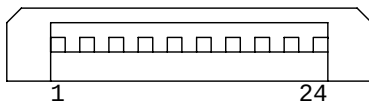


Title			Audio ALC268
Size	Document Number	Rev	
Custom	GD1B Main Board	2A	
Date:	Wednesday, August 22, 2007	Sheet	19 of 35



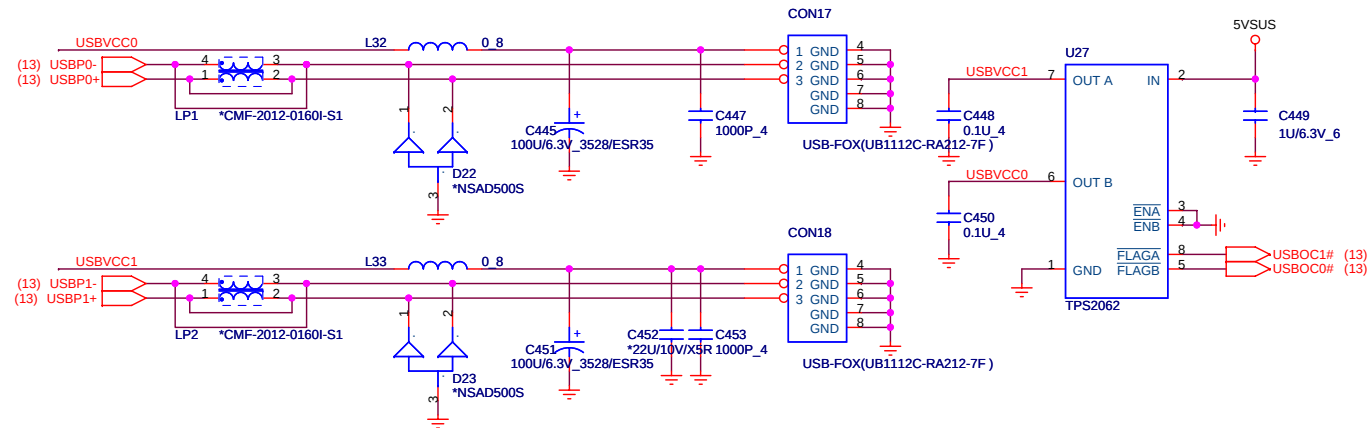
1. Level 1 Environment-related Substances should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners

Keyboard

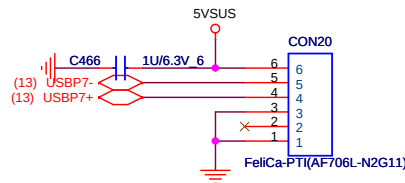


0711 Eric_modify FP for 2nd IR

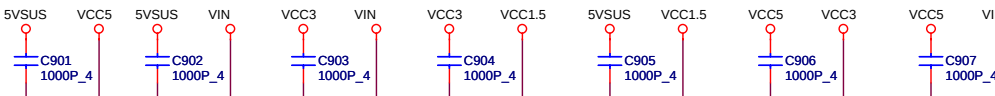
USB Port x 2



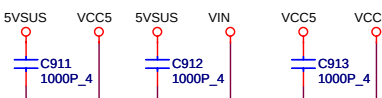
Felica



ODD

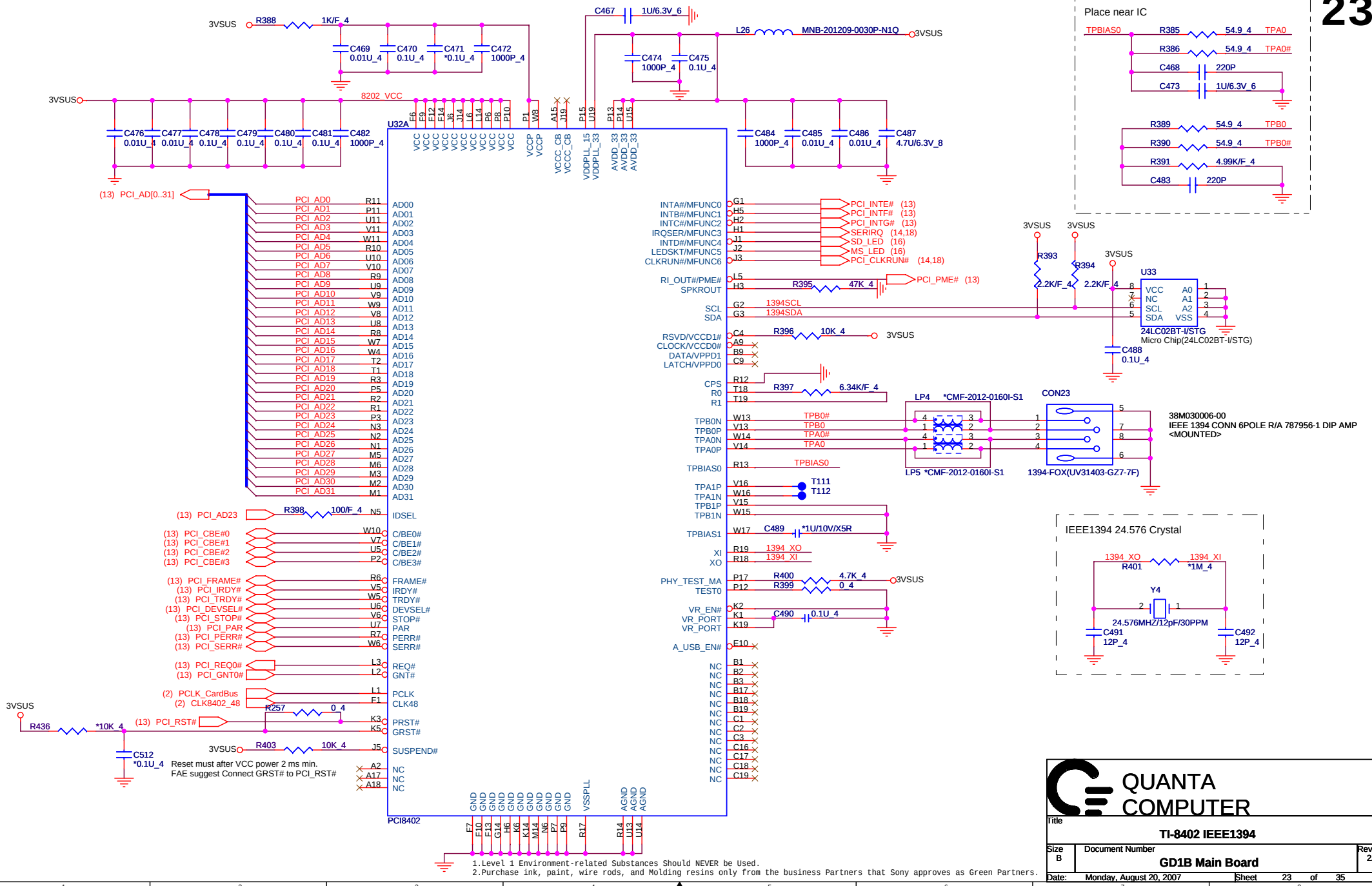


PCI Bus



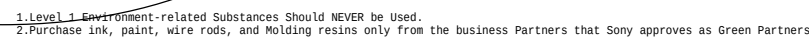
Title			K/B ,USB Device
Size	Document Number		Rev
B	GD1B Main Board		3A
Date:	Monday, August 20, 2007	Sheet	22 of 35

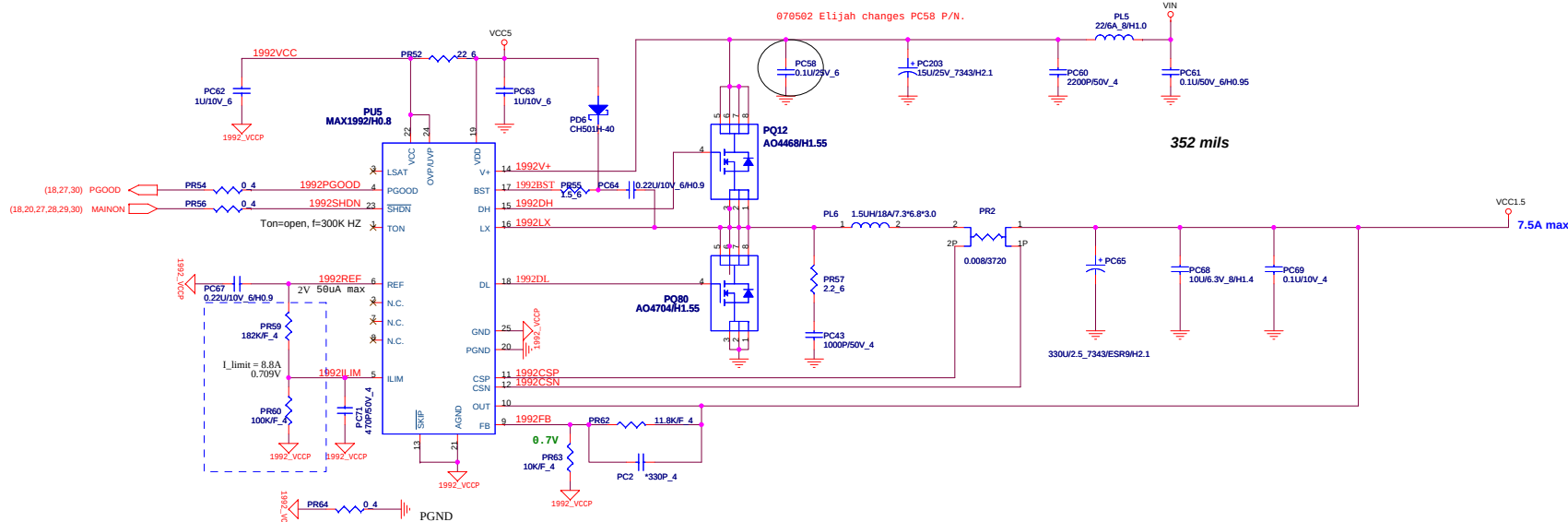
- 1.Level 1 Environment-related Substances Should NEVER be Used.
- 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

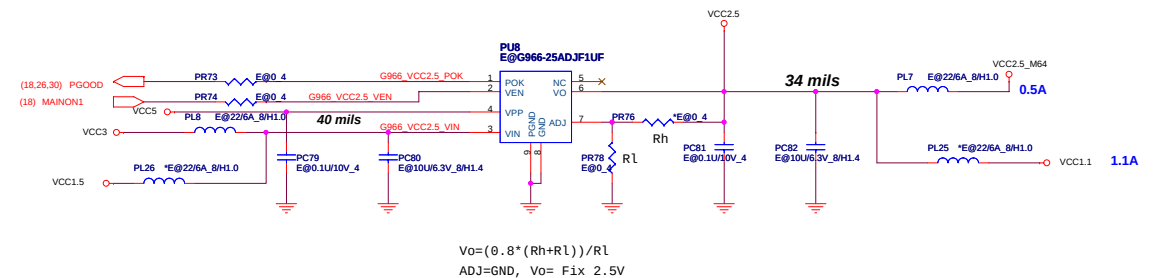
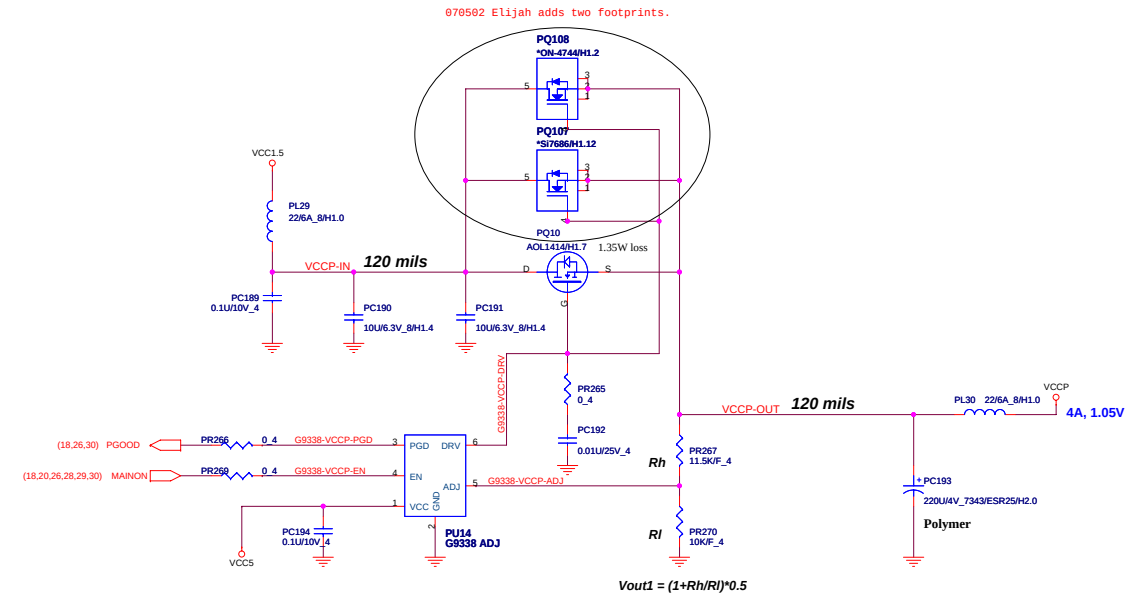


QUANTA
COMPUTER

Title		TI-8402 IEEE1394
Size	Document Number	GD1B Main Board
B		Rev 2A
Date:	Monday, August 20, 2007	Sheet 23 of 35





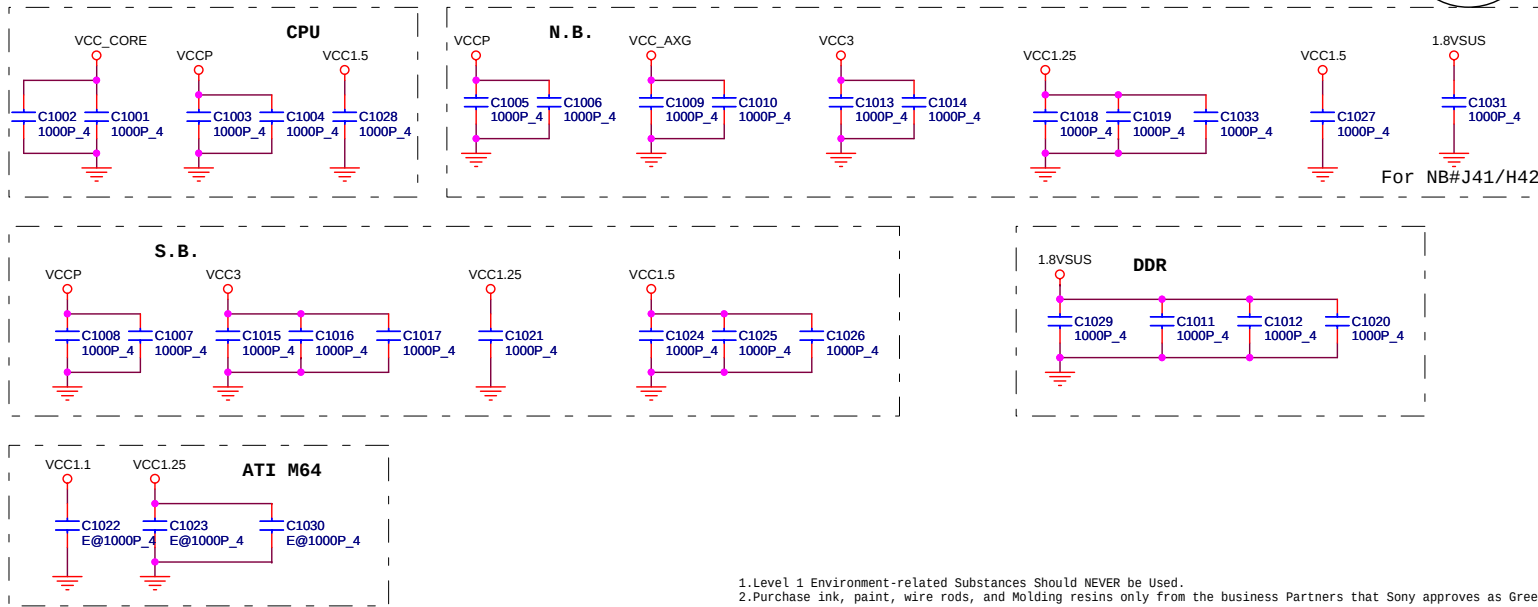
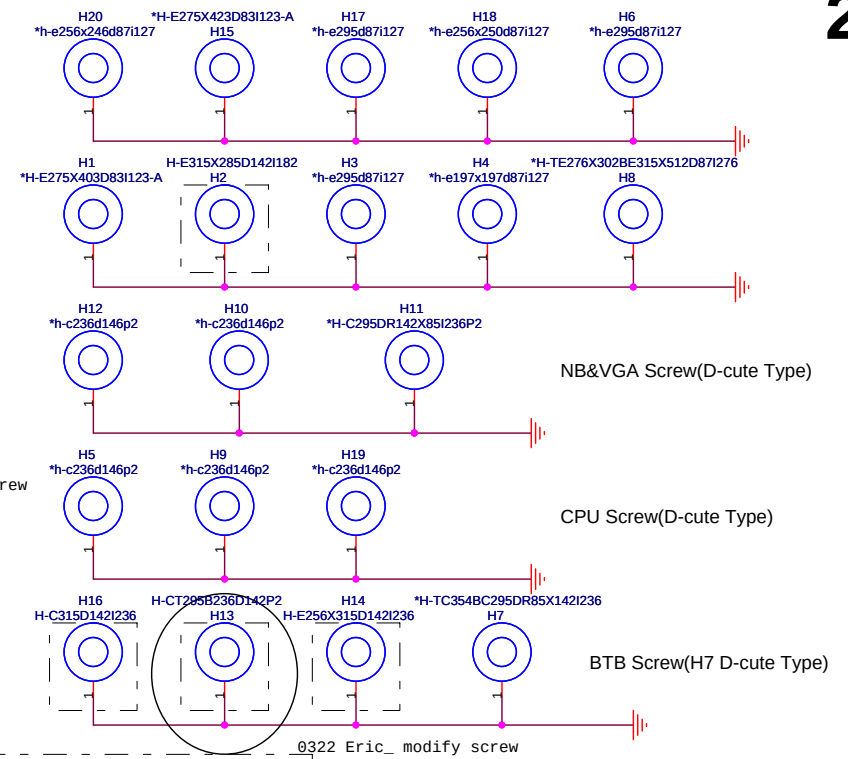
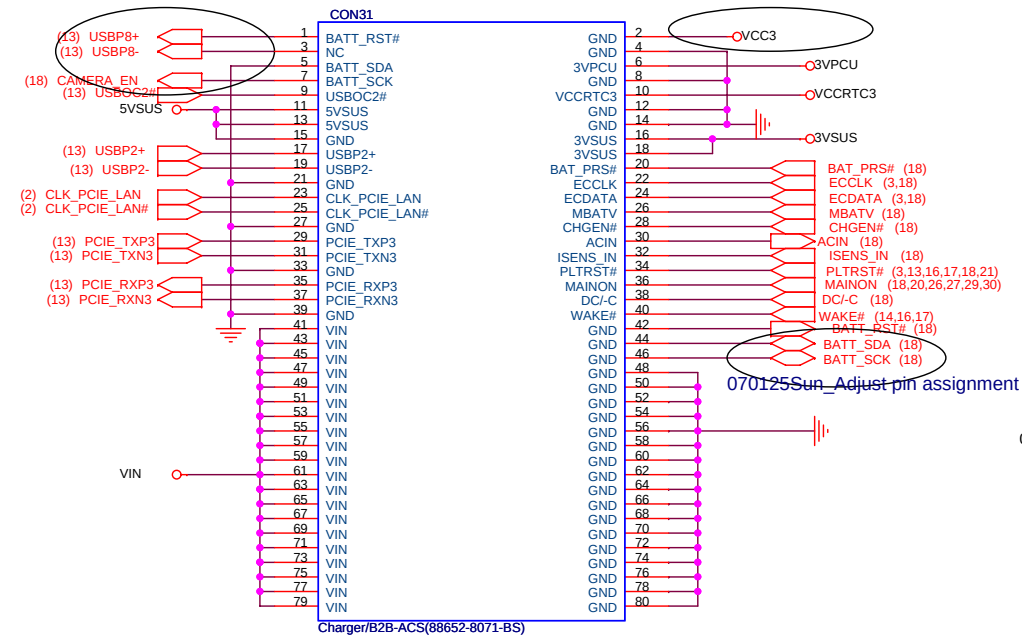


$$V_o = (0.8 * (R_h + R_l)) / R_l$$

ADJ=GND, $V_o = \text{Fix } 2.5V$

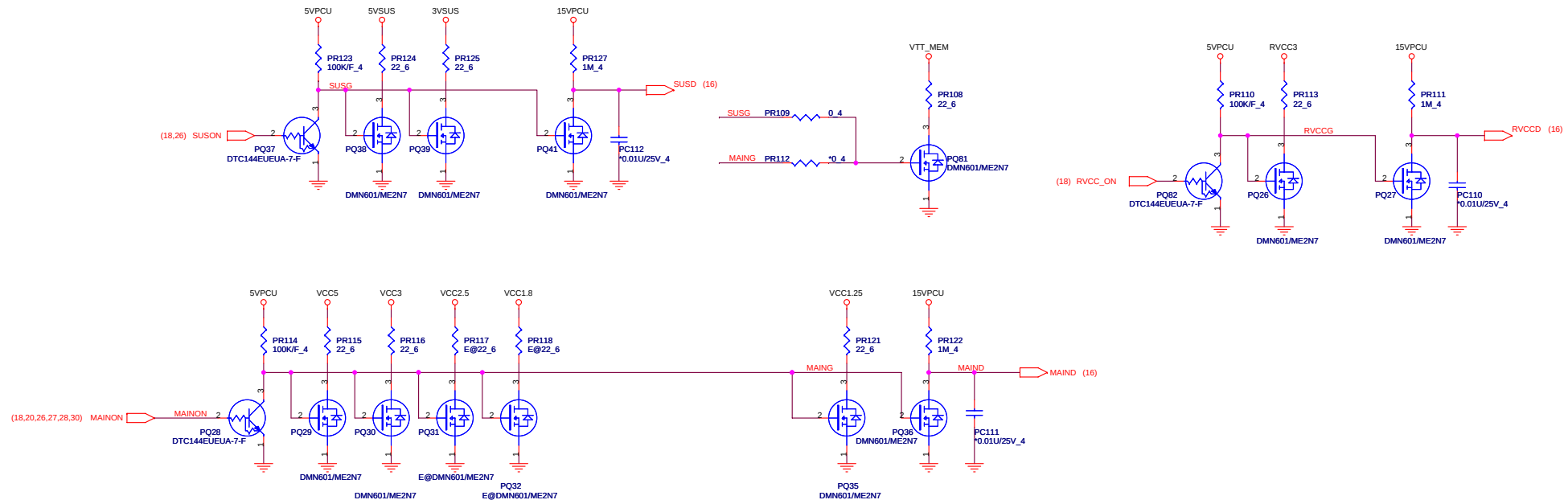
070125Sun_Adjust pin assignment

070125Sun_Adjust pin assignment



- Level 1 Environment-related Substances Should NEVER be Used.
- Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

			
QUANTA COMPUTER			
Title			
Power Charger & LAN CON			
Size B	Document Number		Rev 2A
GD1A Main Board			
Date:	Tuesday, September 04, 2007	Sheet	28 of 35



1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

 QUANTA COMPUTER		
Title Discharge, SUSG, RVCCD, MAIND		
Size	Document Number	Rev
Custom	GD1A Main Board	2A
Date: Tuesday, September 04, 2007	Sheet	29 of 35

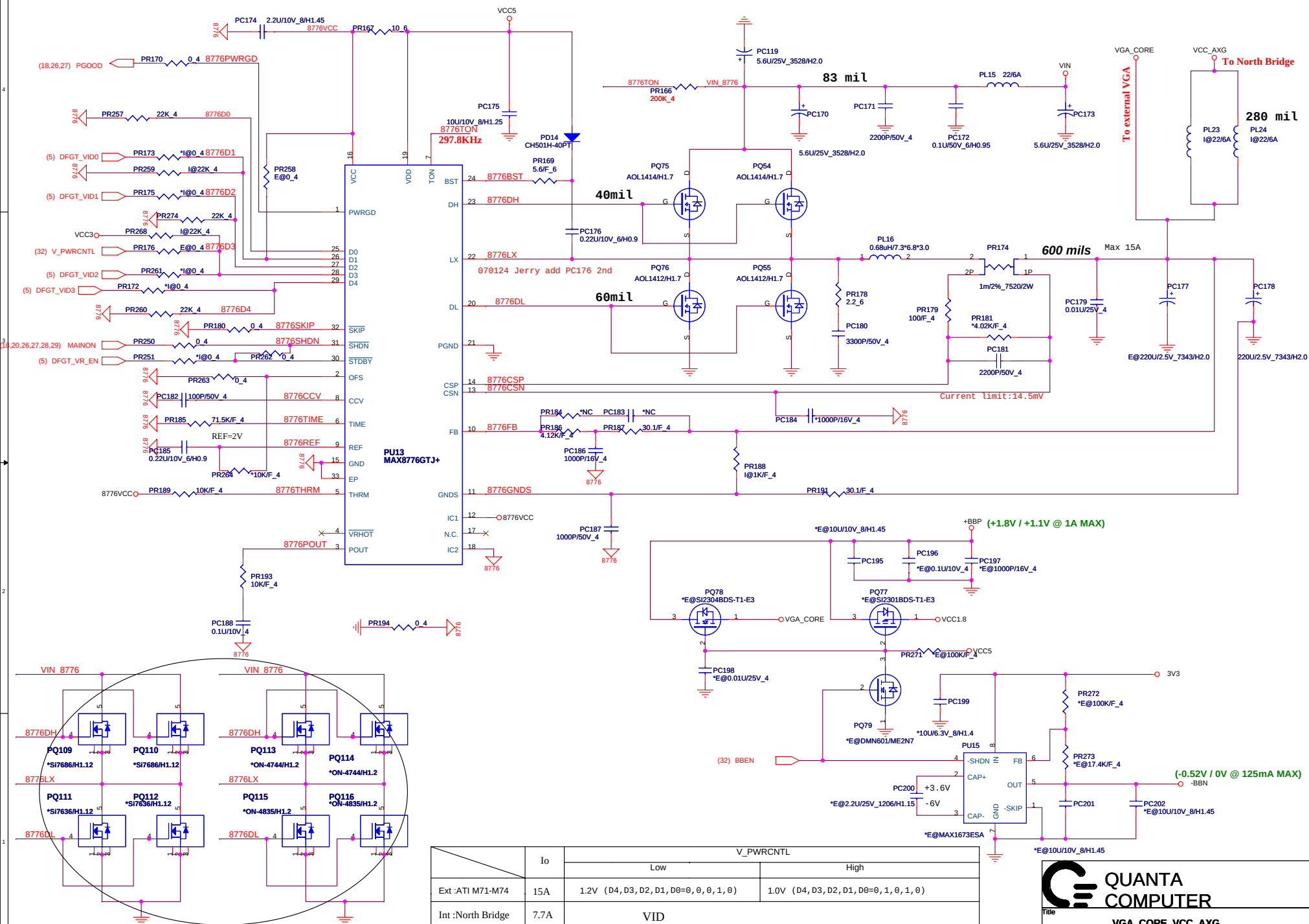


QUANTA
COMPUTER

VGA_CORE, VCC_AXG

GD1B Main Board

Date: Monday, August 20, 2007 Sheet 30 of 35

Rev
2A

070502 Elijah adds PQ109 - PQ116 footprints.

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners

	Io	V_PWRCNTL	
		Low	High
Ext :ATI M71-M74	15A	1.2V (D4, D3, D2, D1, D0=0, 0, 0, 1, 0)	1.0V (D4, D3, D2, D1, D0=0, 1, 0, 1, 0)
Int :North Bridge	7.7A	VID	

U3001A			
PART 1 OF 7			
GFX_TXP0	AK33	PCIE_RX0P	PCIE_TX0P
GFX_TXN0	AJ33	PCIE_RX0N	PCIE_TX0N
GFX_TXP1	AJ35	PCIE_RX1P	PCIE_TX1P
GFX_TXN1	AJ34	PCIE_RX1N	PCIE_TX1N
GFX_TXP2	AH35	PCIE_RX2P	PCIE_TX2P
GFX_TXN2	AH34	PCIE_RX2N	PCIE_TX2N
GFX_TXP3	AG35	PCIE_RX3P	PCIE_TX3P
GFX_TXN3	AG34	PCIE_RX3N	PCIE_TX3N
GFX_TXP4	AE33	PCIE_RX4P	PCIE_TX4P
GFX_TXN4	AE33	PCIE_RX4N	PCIE_TX4N
GFX_TXP5	AE35	PCIE_RX5P	PCIE_TX5P
GFX_TXN5	AE34	PCIE_RX5N	PCIE_TX5N
GFX_TXP6	AD35	PCIE_RX6P	PCIE_TX6P
GFX_TXN6	AD34	PCIE_RX6N	PCIE_TX6N
GFX_TXP7	AC35	PCIE_RX7P	PCIE_TX7P
GFX_TXN7	AC34	PCIE_RX7N	PCIE_TX7N
GFX_TXP8	AB33	PCIE_RX8P	PCIE_TX8P
GFX_TXN8	AA33	PCIE_RX8N	PCIE_TX8N
GFX_TXP9	AA35	PCIE_RX9P	PCIE_TX9P
GFX_TXN9	AA34	PCIE_RX9N	PCIE_TX9N
GFX_TXP10	Y35	PCIE_RX10P	PCIE_TX10P
GFX_TXN10	Y34	PCIE_RX10N	PCIE_TX10N
GFX_TXP11	W35	PCIE_RX11P	PCIE_TX11P
GFX_TXN11	W34	PCIE_RX11N	PCIE_TX11N
GFX_TXP12	V33	PCIE_RX12P	PCIE_TX12P
GFX_TXN12	U33	PCIE_RX12N	PCIE_TX12N
GFX_TXP13	U35	PCIE_RX13P	PCIE_TX13P
GFX_TXN13	U34	PCIE_RX13N	PCIE_TX13N
GFX_TXP14	T35	PCIE_RX14P	PCIE_TX14P
GFX_TXN14	T34	PCIE_RX14N	PCIE_TX14N
GFX_TXP15	R35	PCIE_RX15P	PCIE_TX15P
GFX_TXN15	R34	PCIE_RX15N	PCIE_TX15N

P
C
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Clock

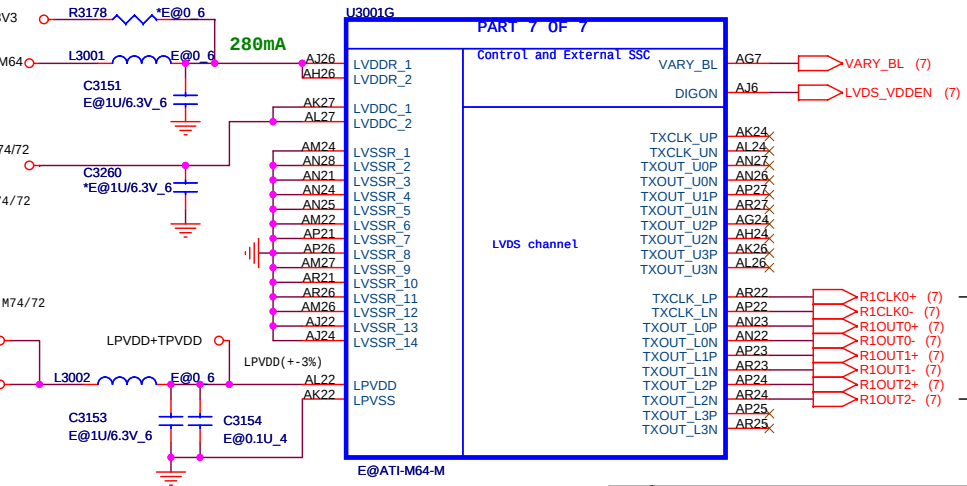
PCIE_REFCLKP
PCIE_REFCLKN
RSVD_1
RSVD_2
PERSTB

E@ATI-M64-M

Calibration

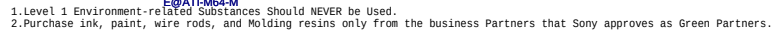
PCIE_CALRN
PCIE_CALRP
PCIE_CALI

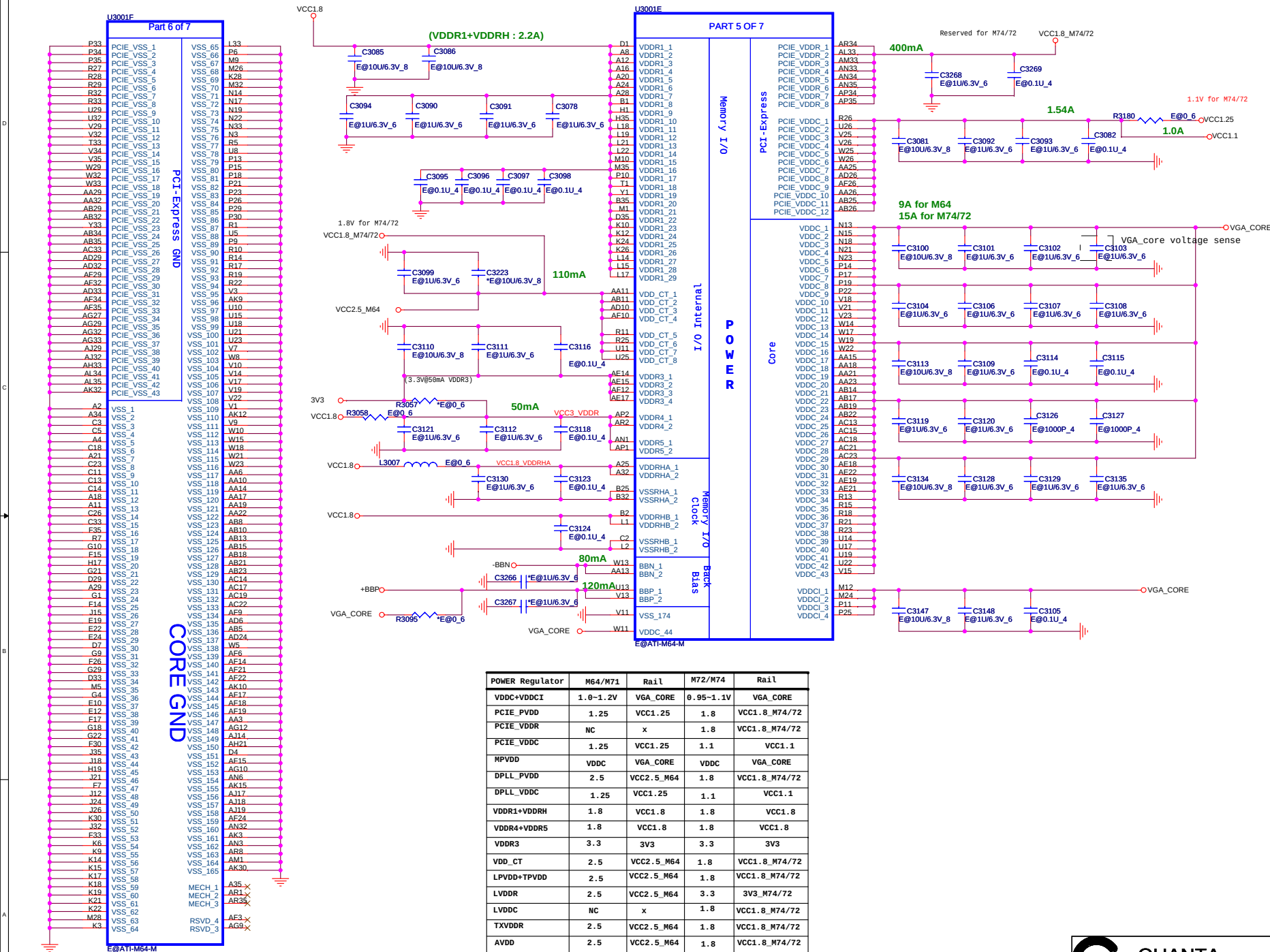
AG26 R3000 E@2K/F 4 VCC1.25
AJ27 R3001 E@562/F 4 1.27K for M74/72
AK29 R3002 E@1.47K/F 4 18K for M74/72



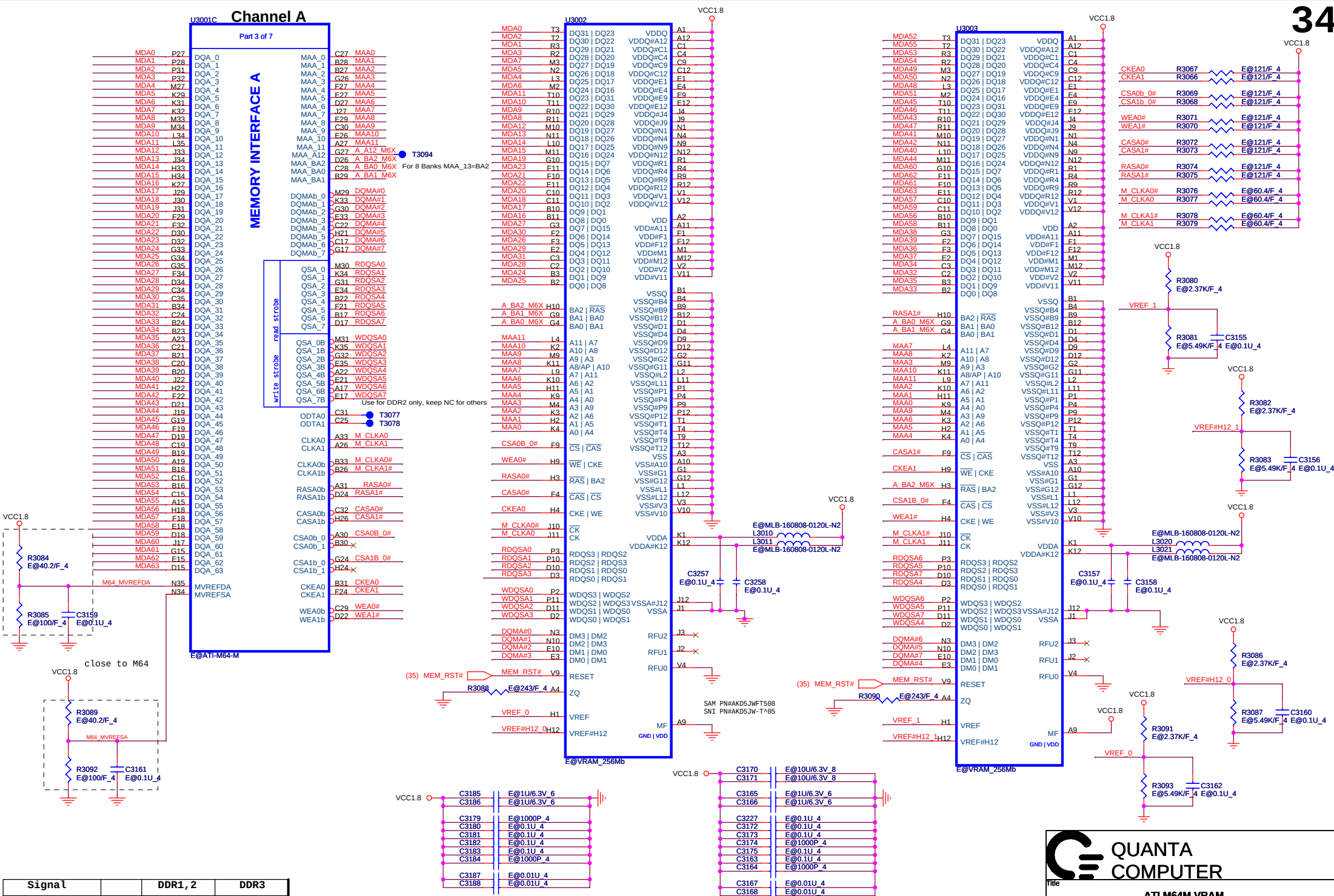
Title		
ATI M64M PCIE		
Size B	Document Number	Rev 2A
GD1B Main Board		
Date:	Monday, August 20, 2007	Sheet 31 of 35

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.





POWER Regulator	M64/M71	Rail	M72/M74	Rail
VDDC+VDDCI	1.0-1.2V	VGA_CORE	0.95-1.1V	VGA_CORE
PCIE_PVDD	1.25	VCC1.25	1.8	VCC1.8_M74/72
PCIE_VDDR	NC	x	1.8	VCC1.8_M74/72
PCIE_VDDC	1.25	VCC1.25	1.1	VCC1.1
MPVDD	VDDC	VGA_CORE	VDDC	VGA_CORE
DPLL_PVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
DPLL_VDDC	1.25	VCC1.25	1.1	VCC1.1
VDDR1+VDDRH	1.8	VCC1.8	1.8	VCC1.8
VDDR4+VDDR5	1.8	VCC1.8	1.8	VCC1.8
VDDR3	3.3	3V3	3.3	3V3
VDD_CT	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
LPVDD+TPVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
LVDDR	2.5	VCC2.5_M64	3.3	3V3_M74/72
VDDC	NC	x	1.8	VCC1.8_M74/72
TXVDDR	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
AVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
VDD1DI+VD2DI	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
A2VDD	2.5	VCC2.5_M64	3.3	3V3_M74/72
A2VDDQ	NC	x	1.8	VCC1.8_M74/72



QUANTA COMPUTER

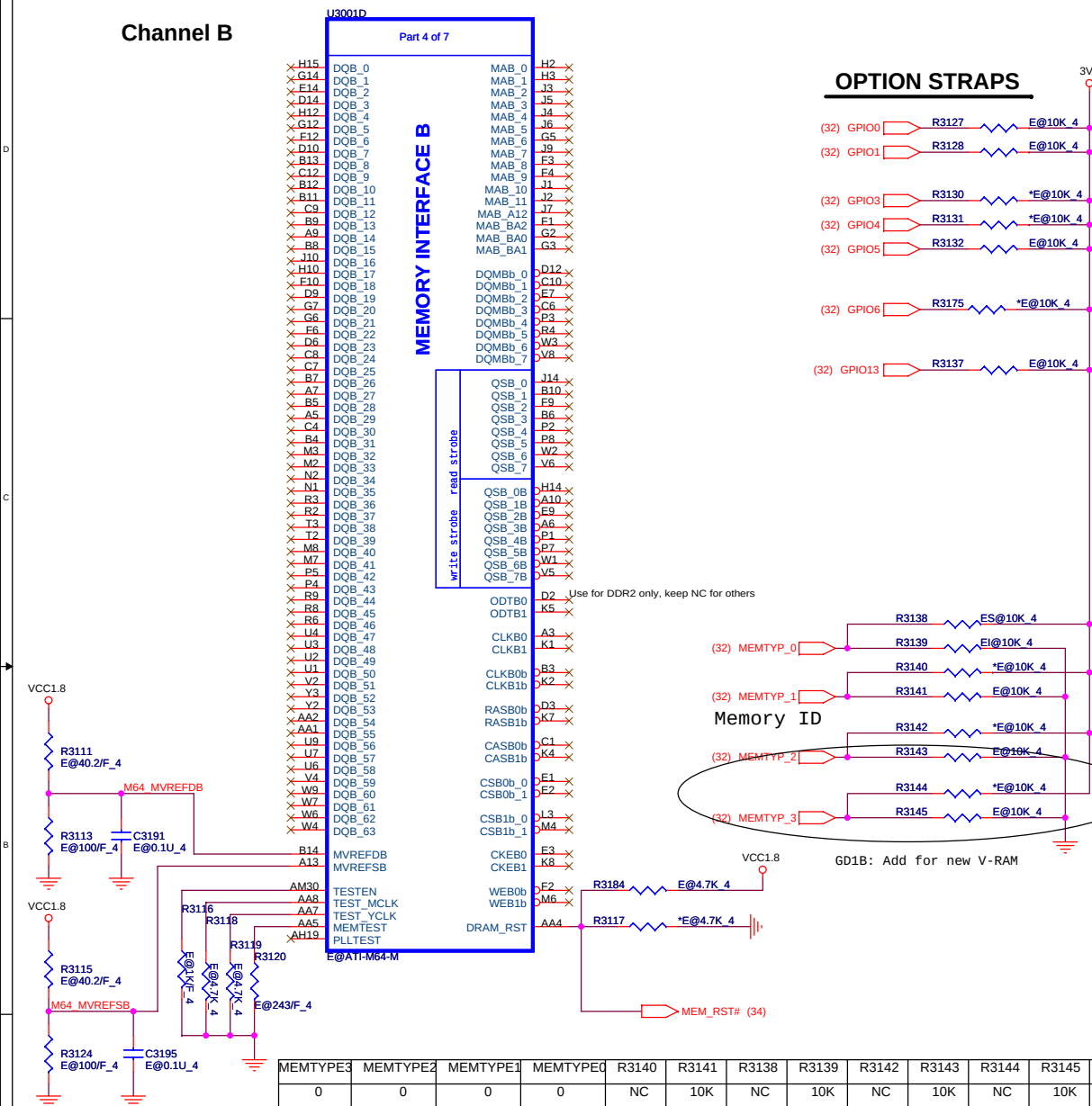
ATI M64M VRAM

Size Custom Document Number **GD1B Main Board** Rev 2A

Date: Monday, August 20, 2007 Sheet 34 of 35

1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Channel B



M64-M Strap

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: full Tx output swing	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	(recommended) Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled (recommended)	0 (internal pull-down)
Reserved	GPIO(3:2)	ATI internal use only. Other logic must not affect this signal during RESET.(GPIO2=VDD_VCL)	00
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0 (internal pull-down)
PLL_IBIAS_RD	GPIO[6:5]	Bias Current for the PCI Express PHY PLL	01
Reserved	GPIO8	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
ROMIDCFG(3:0)	GPIO(9,13,11)	If no ROM attached, controls chip IDis. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128MB 001x - No ROM, MEM_AP_SIZE=01 256MB 010x - No ROM, MEM_AP_SIZE=10 64MB(Default) 011x - No ROM, MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	GPIO[9,13,12,11] 0000 (internal pull-down)
VIP_DEVICE	VSYN	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port device present. 1-No slave VIP port devices reporting presence during reset	0 (internal pull-down)
Reserved	PCIE_TEST	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
Reserved	HSYN	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0

VRAM Straps

REV. 0.1

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE[10]	GPIO 27,26	Memory identification for BIOS 00 - Infineon GDDR3 : 2M x 32 bits x 4 banks(Default) 01 - SAMSUNG GDDR3 : 2M x 32 bits x 4 banks 10 - RESERVED 11 - RESERVED	00

MEMENTYPE3	MEMENTYPE2	MEMENTYPE1	MEMENTYPE0	R3140	R3141	R3138	R3139	R3142	R3143	R3144	R3145	
0	0	0	0	NC	10K	NC	10K	NC	10K	NC	10K	000 - Infineon GDDR3 : 2M x 32 bits x 4 banks
0	0	0	1	NC	10K	10K	NC	NC	10K	NC	10K	001 - SAMSUNG GDDR3(G) : 2M x 32 bits x 4 banks
0	0	1	0	10K	NC	NC	10K	NC	10K	NC	10K	010 - Hynix GDDR3: 2M x 32 bits x 4 banks
0	0	1	1	10K	NC	10K	NC	NC	10K	NC	10K	011 - SAMSUNG GDDR3(I) : 2M x 32 bits x 4 banks
0	1	0	0	NC	10K	NC	10K	10K	NC	NC	10K	100 - Samsung GDDR3 : 16Mx32
0	1	0	1	NC	10K	10K	NC	10K	NC	NC	10K	101 - Hynix GDDR3 : 16Mx32
0	1	1	0	10K	NC	NC	10K	10K	NC	NC	10K	101 - Qimonda GDDR3 : 16Mx32
0	1	1	1	10K	NC	10K	NC	10K	NC	NC	10K	