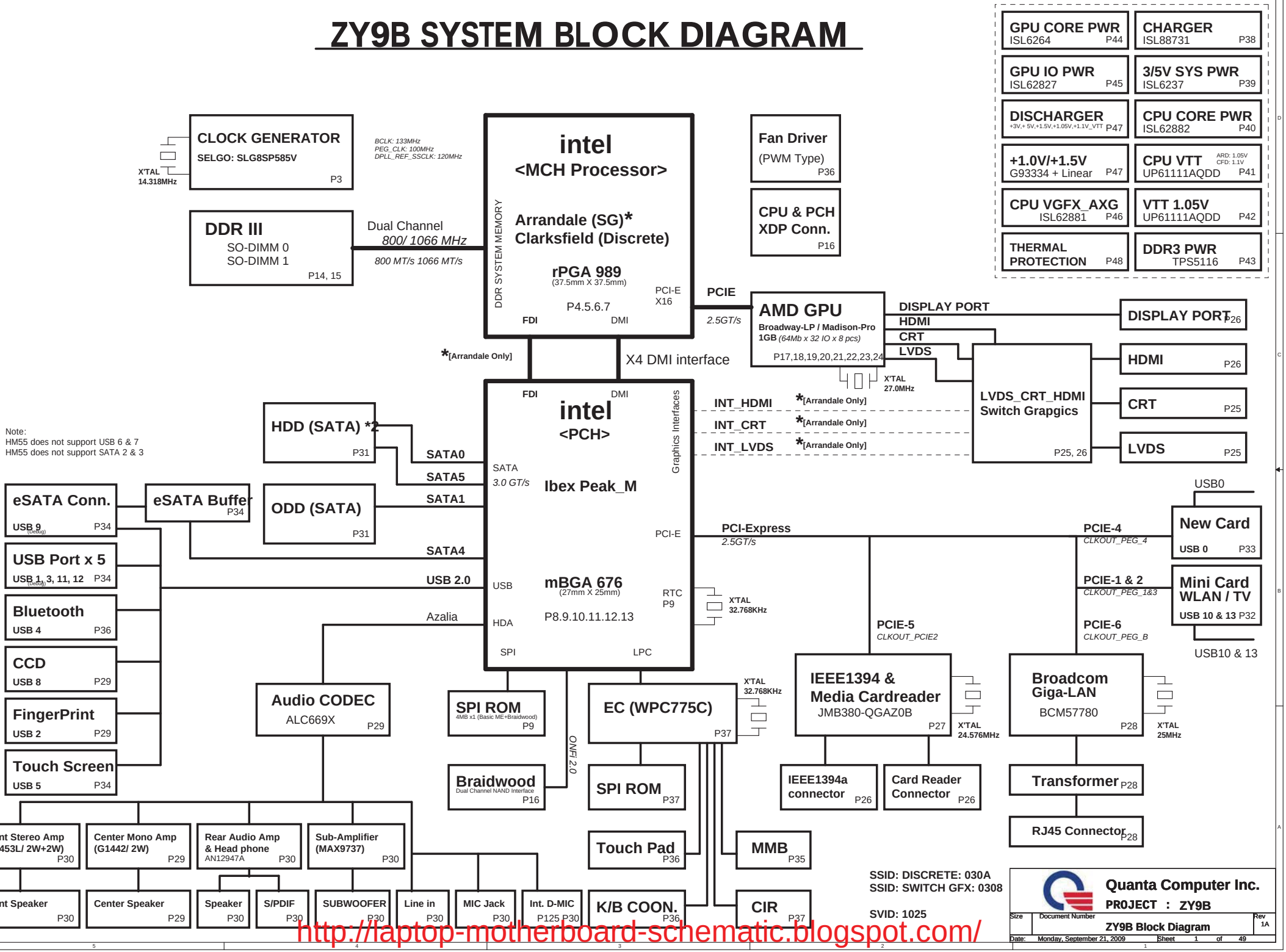
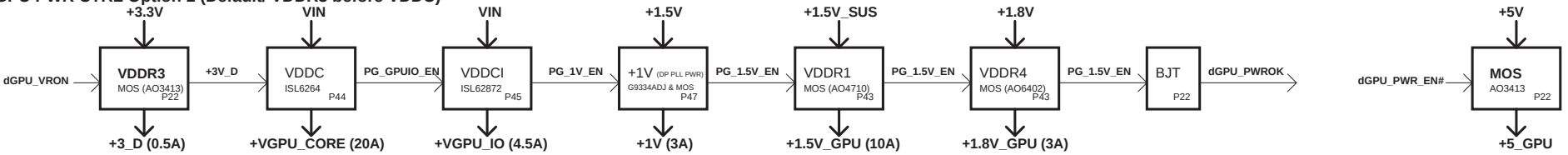
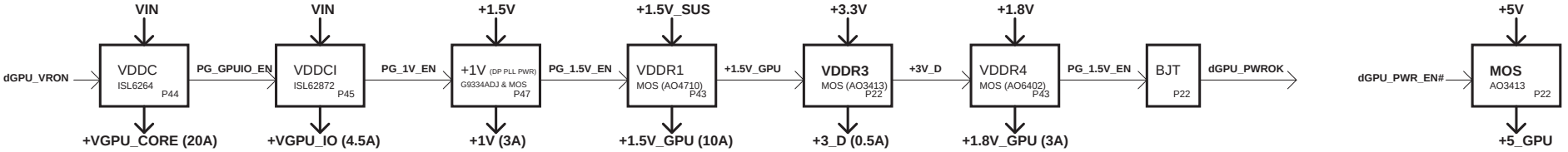
ZY9B SYSTEM BLOCK DIAGRAM



GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



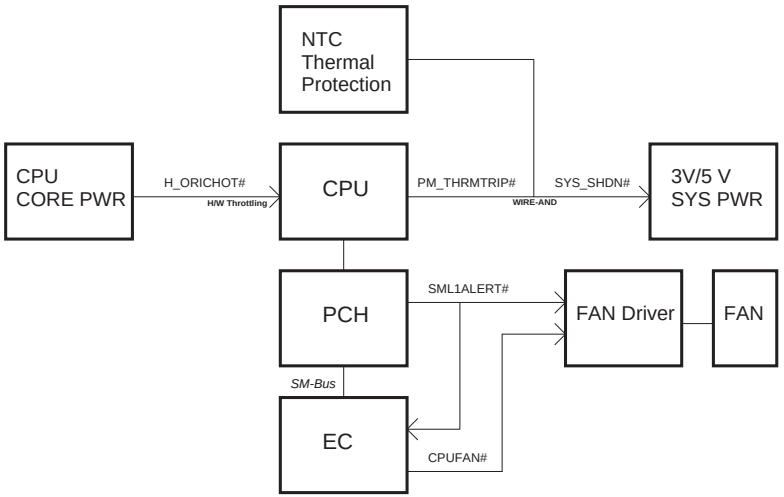
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



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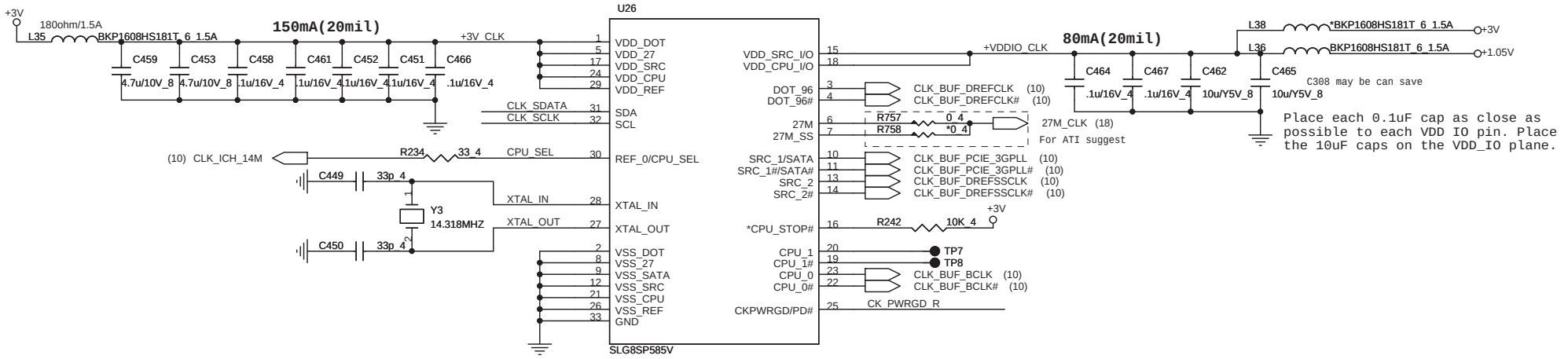
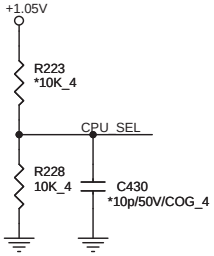
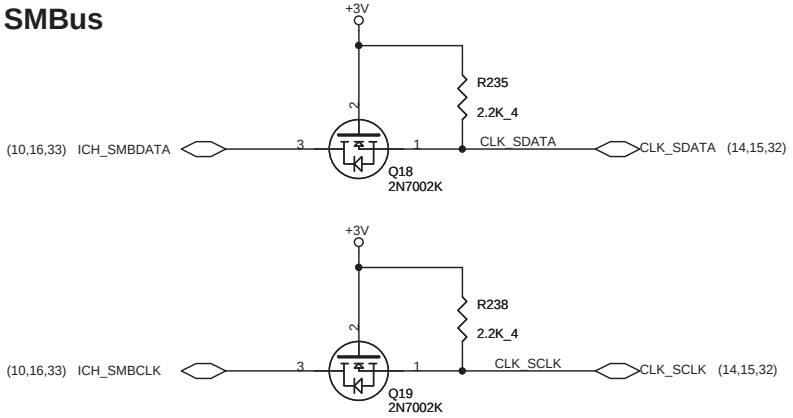


CPU_CLK select

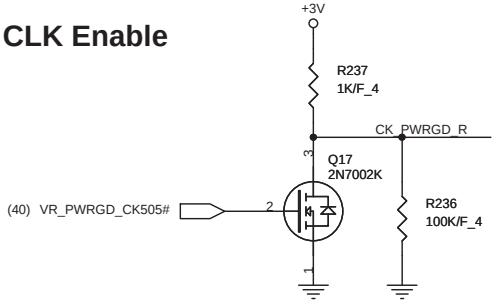


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable



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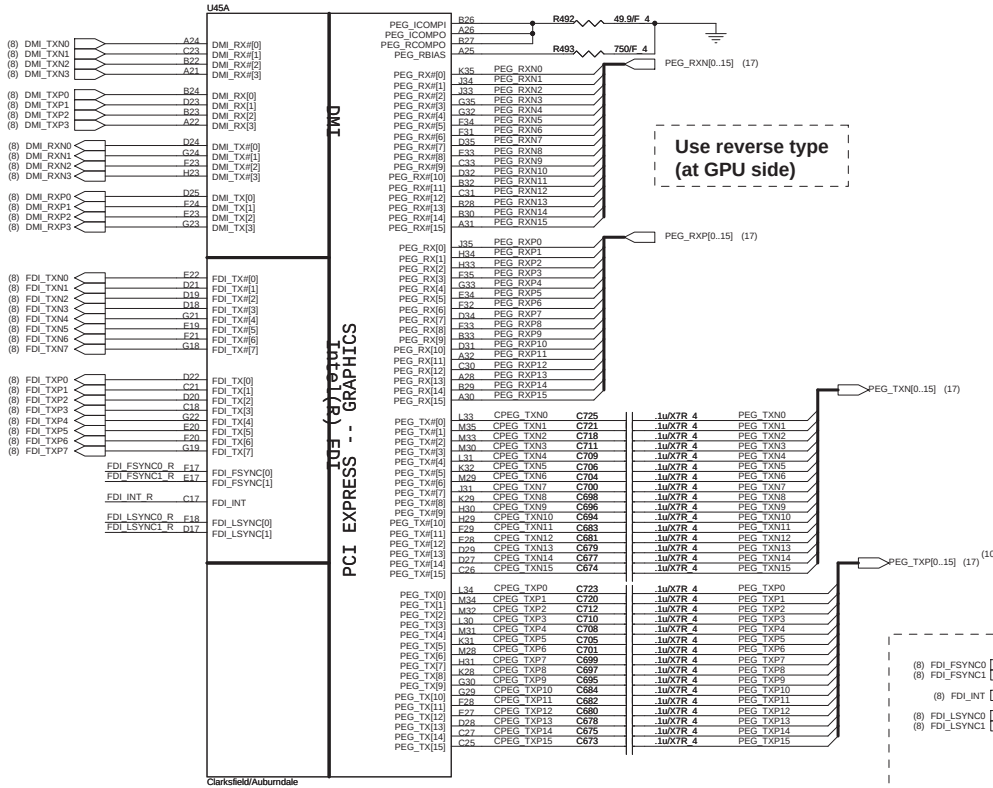
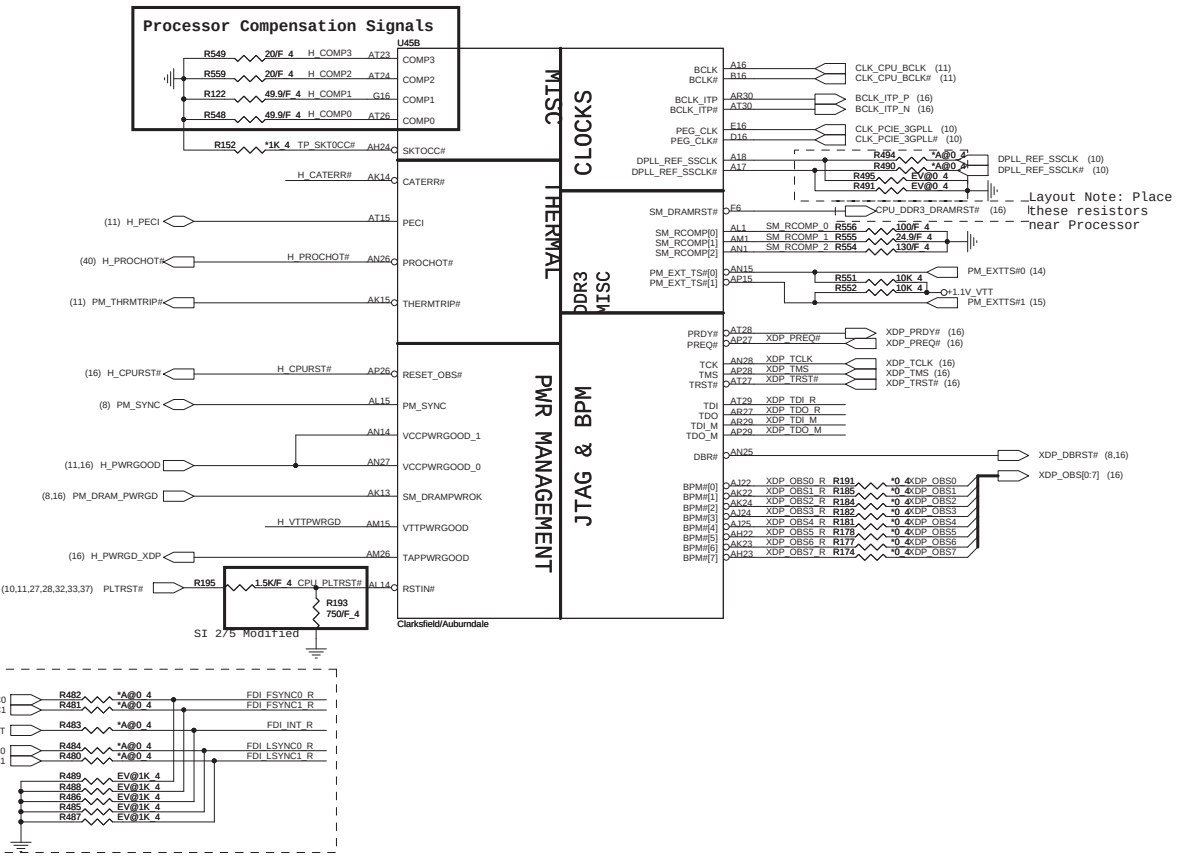
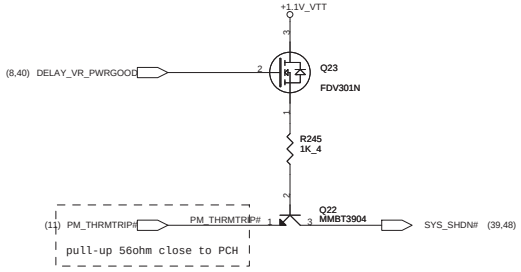
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



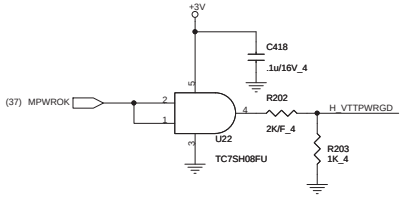
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



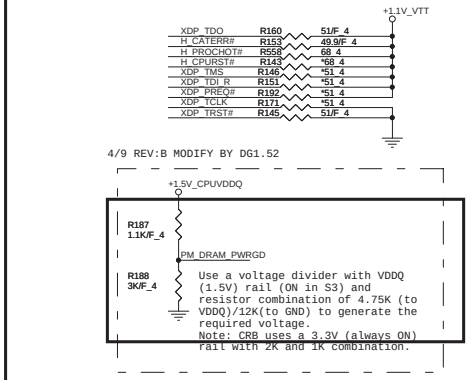
Thermaltrip protect



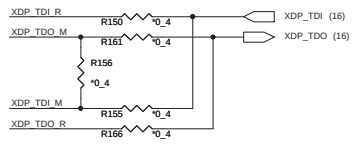
VTT PWR_Good



Processor pull-up



JTAG MAPPING



Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

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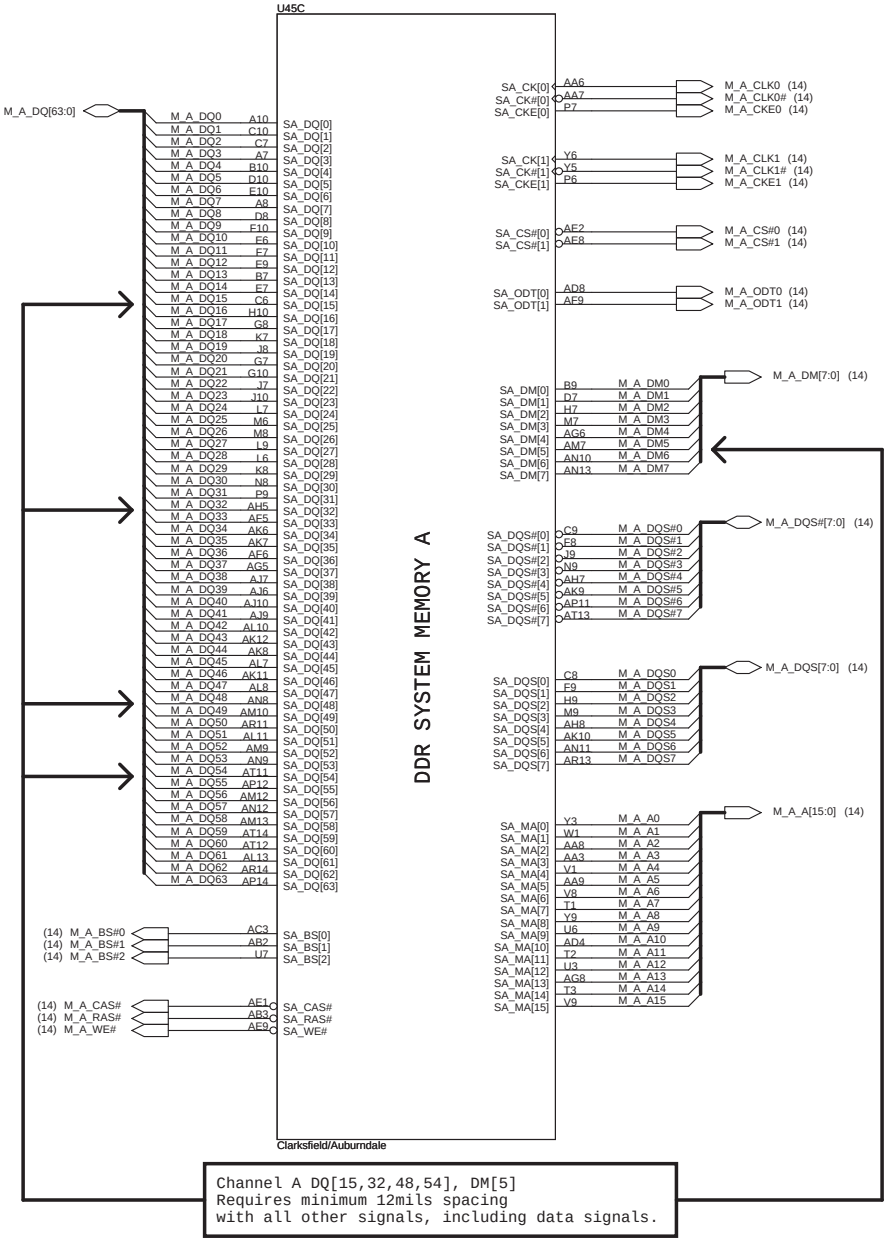
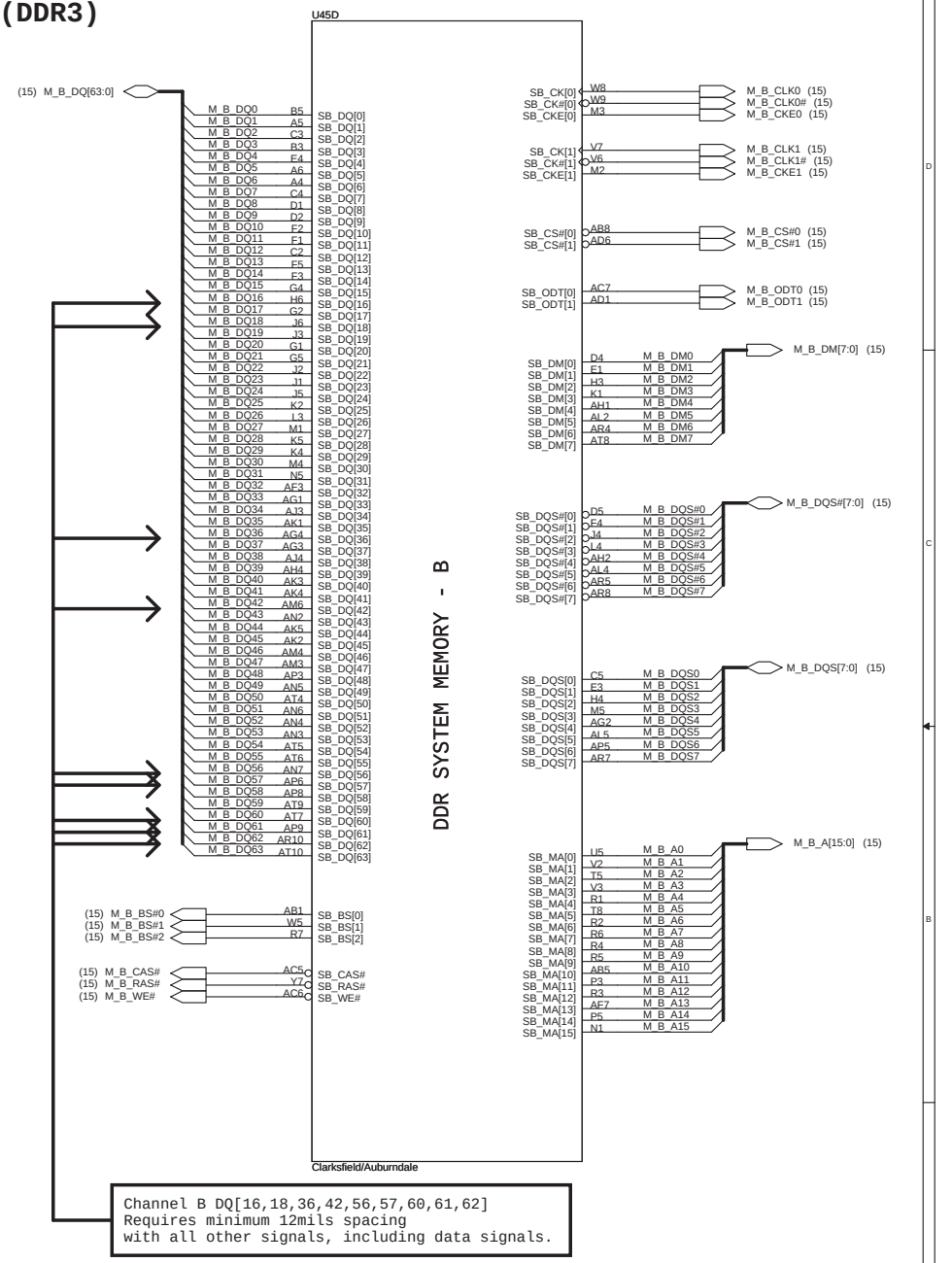
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.



Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

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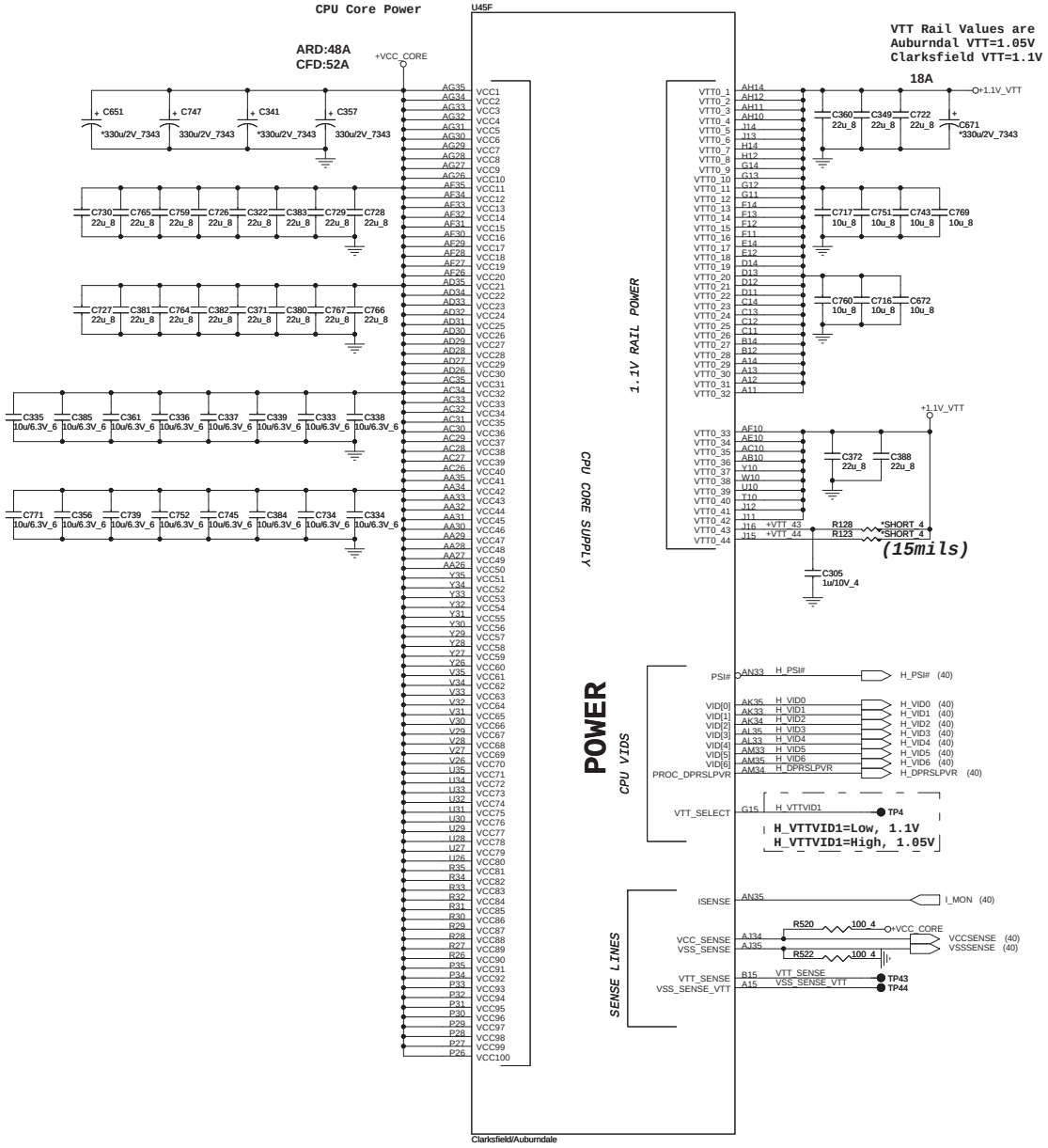
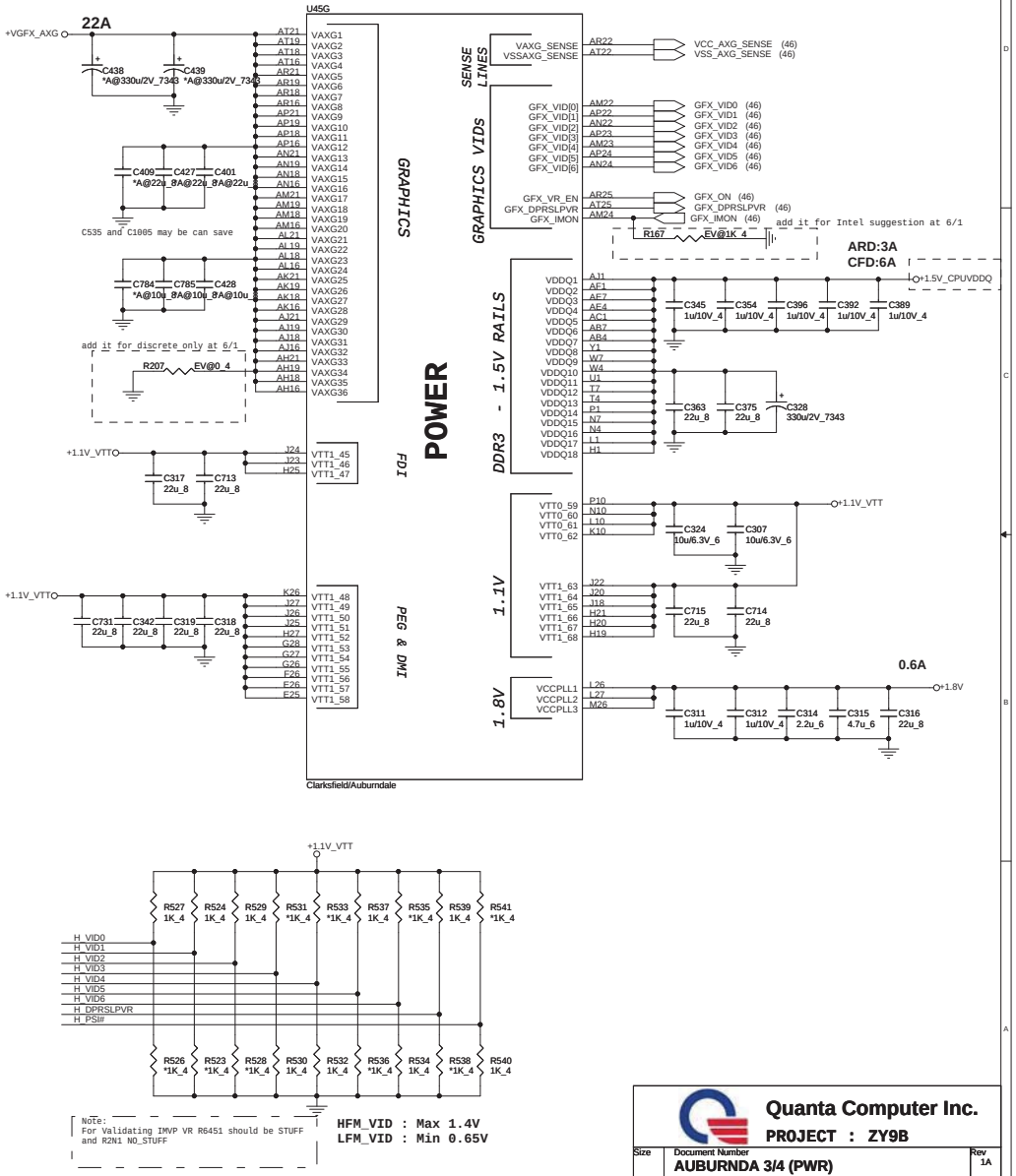


AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)



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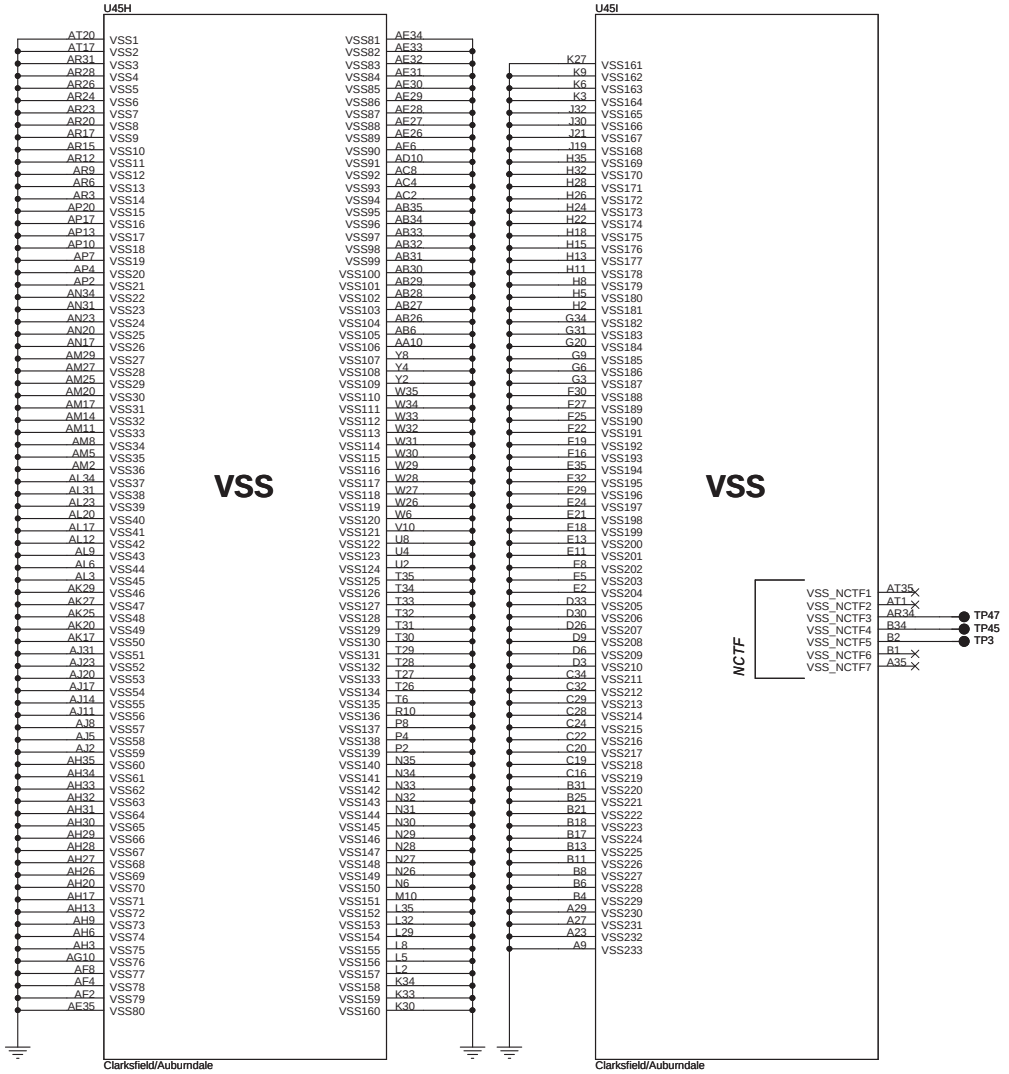
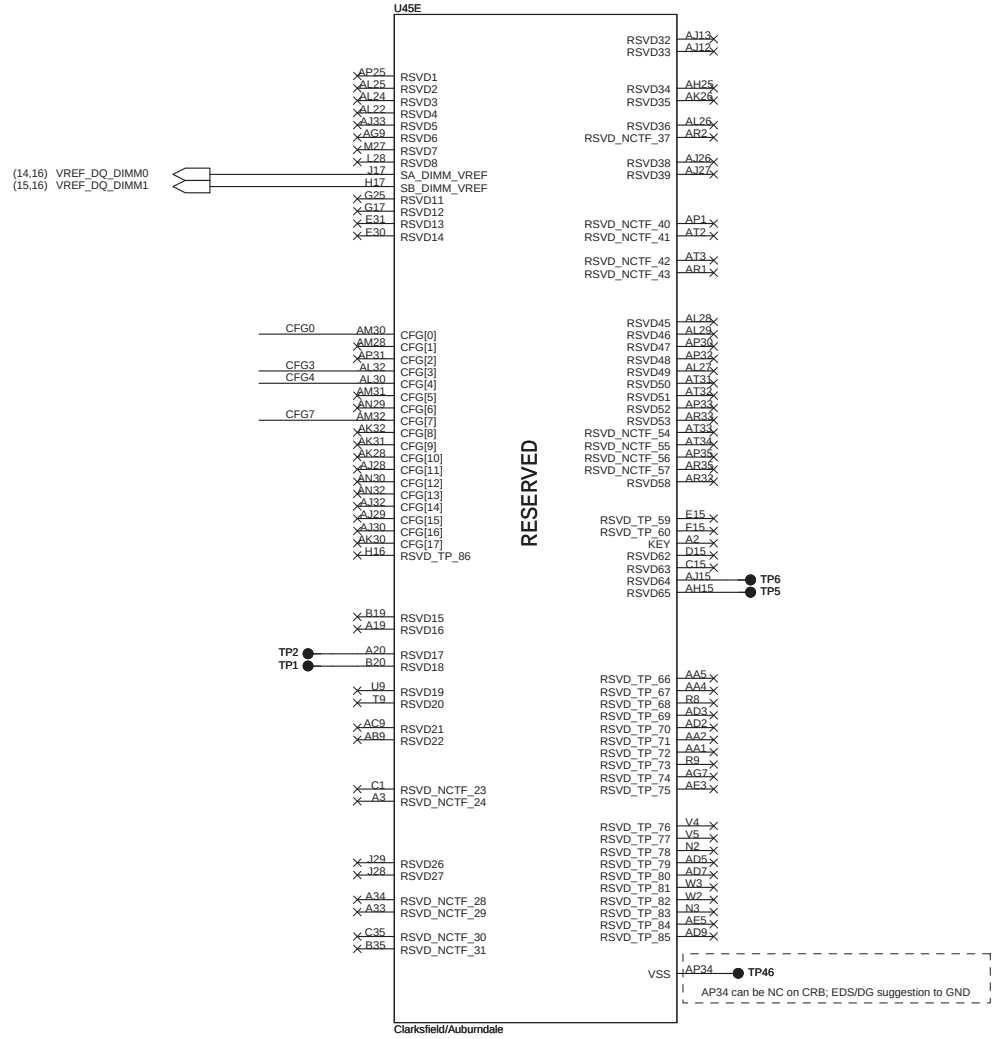
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

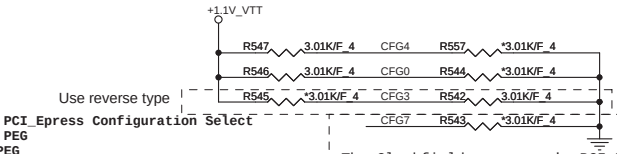


AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

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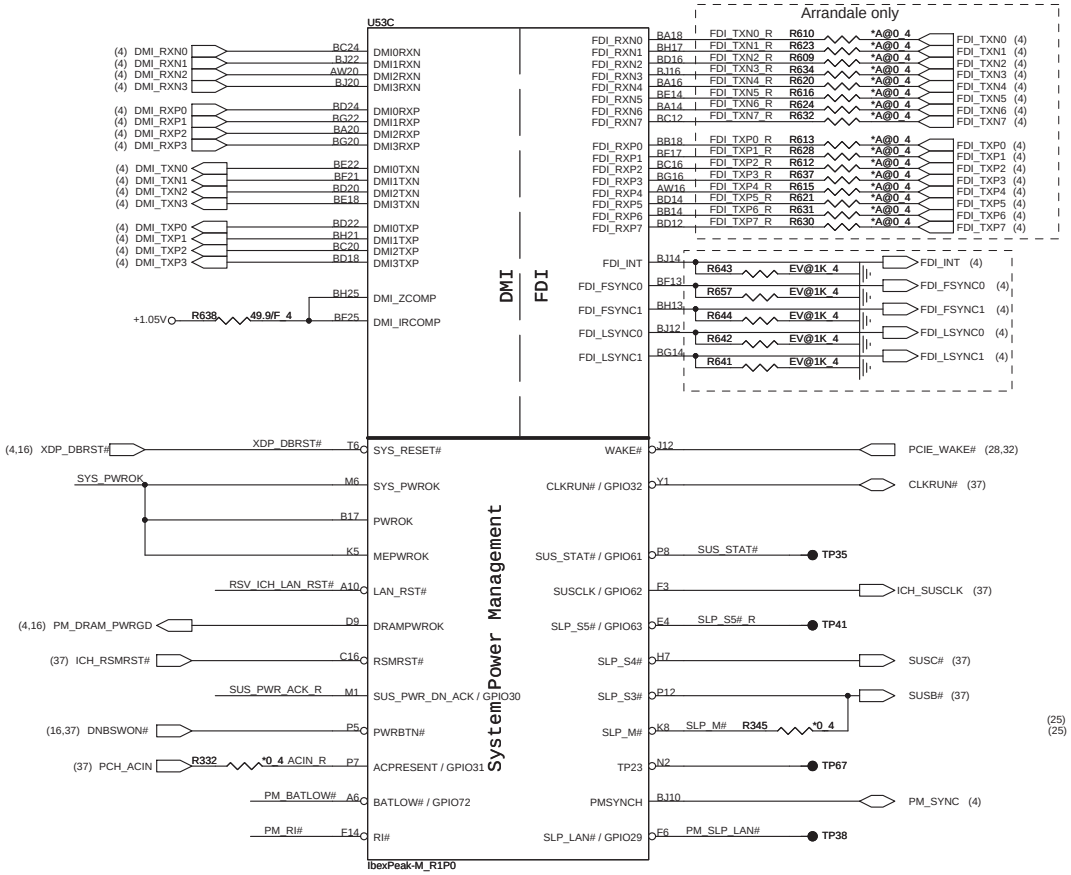
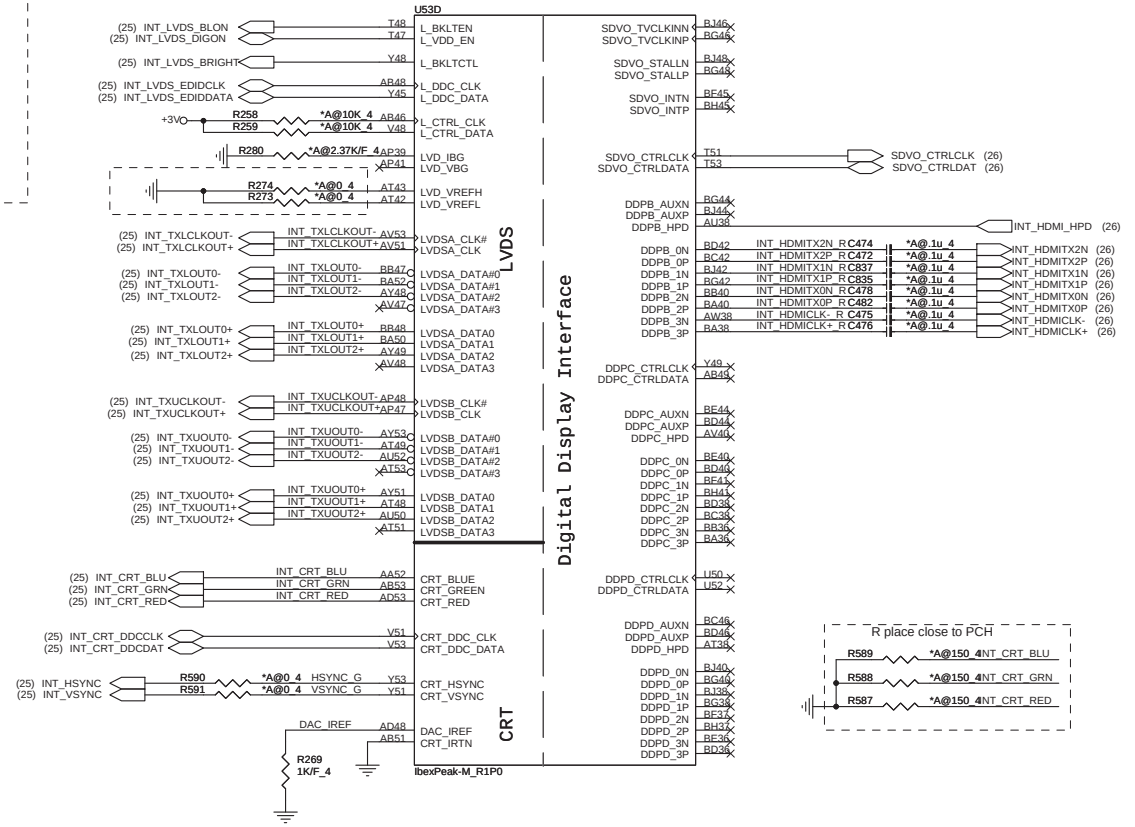
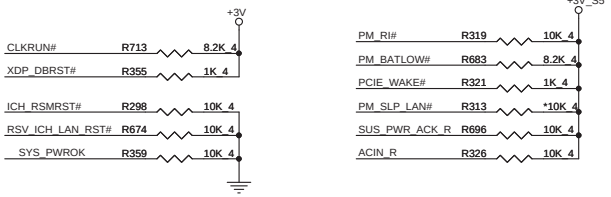
IBEX PEAK-M (DMI,FDI,GPIO)



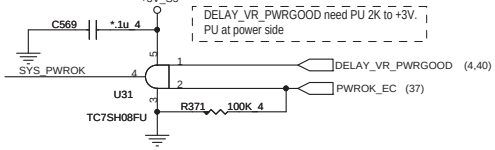
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



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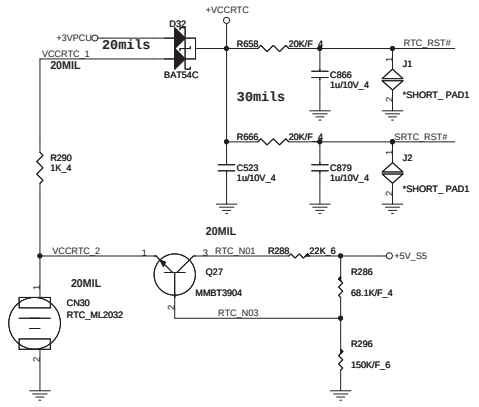
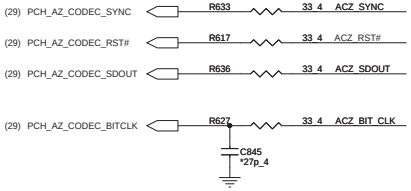
RTC Circuitry

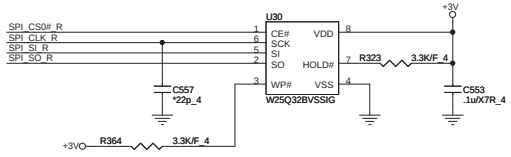


HDA Bus

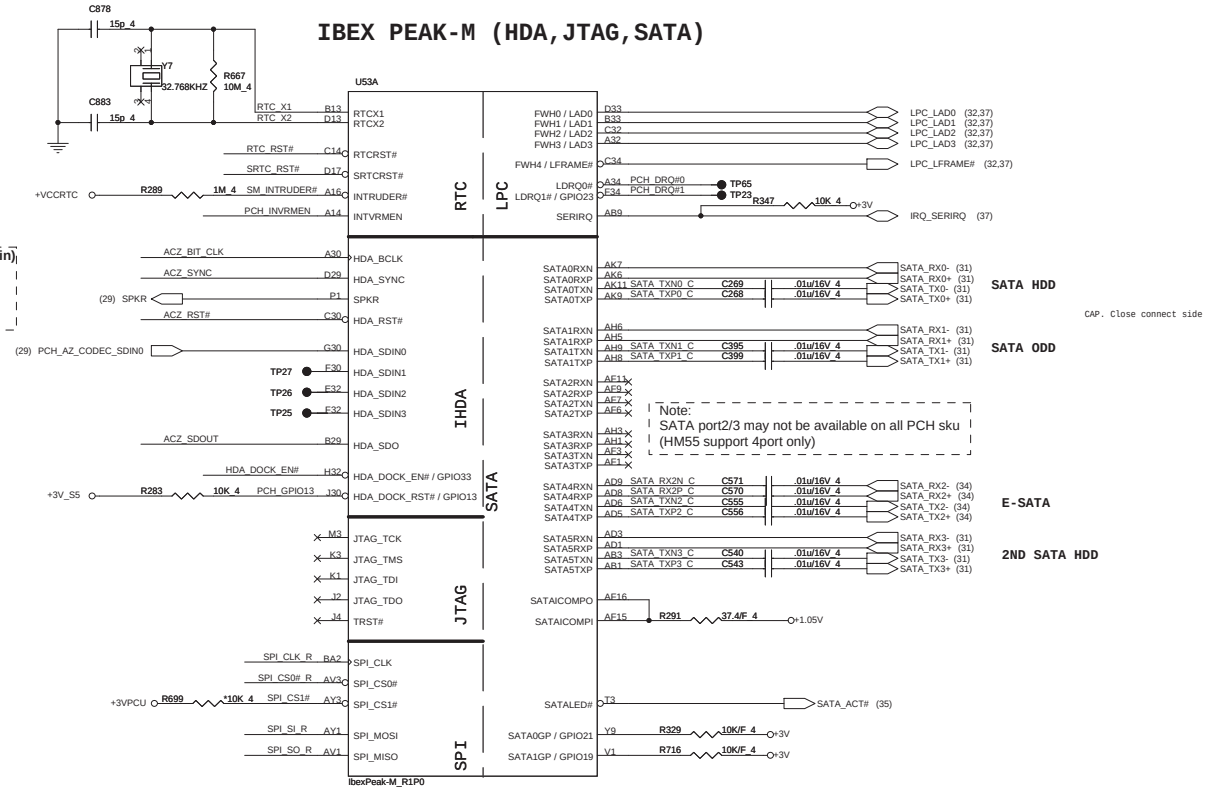


Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

PCH SPI



IBEX PEAK-M (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	ZY9B note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R702 *10K_4 SPKR
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R584 *10K_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+VCCRTC R662 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI 1 / 0 / PCI 0 / 0 / **LPC**	**Default weak pull-up on GNT0/1#** **[Need external pull-down for LPC BIOS]** +3V R270 *1K_4 R256 *1K_4 R272 1K_4 R271 1K_4 PCI_GNT0# (10) PCI_GNT1# (10)
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V R698 *1K_4 NV_ALE NV_ALE (10,16)
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V R697 *1K_4 NV_CLE NV_CLE (10,16)
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V R279 *1K_4 R276 *10K_4 HDA_DOCK_EN#
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R352 *1K_4 SPI_SI_R
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)	
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_S5 R340 10K_4 RSV_GPIO8 (11)
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use defaul (0 = 1.8V supply)
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+V... R330 1K_4 ... (11,27)

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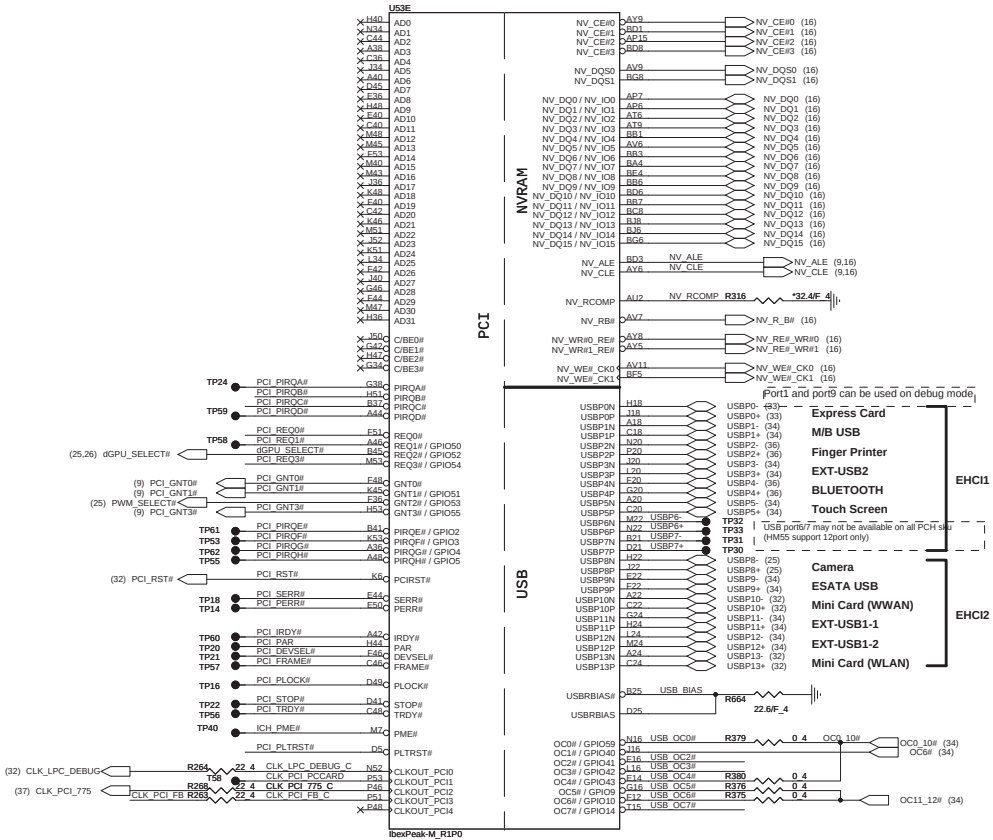
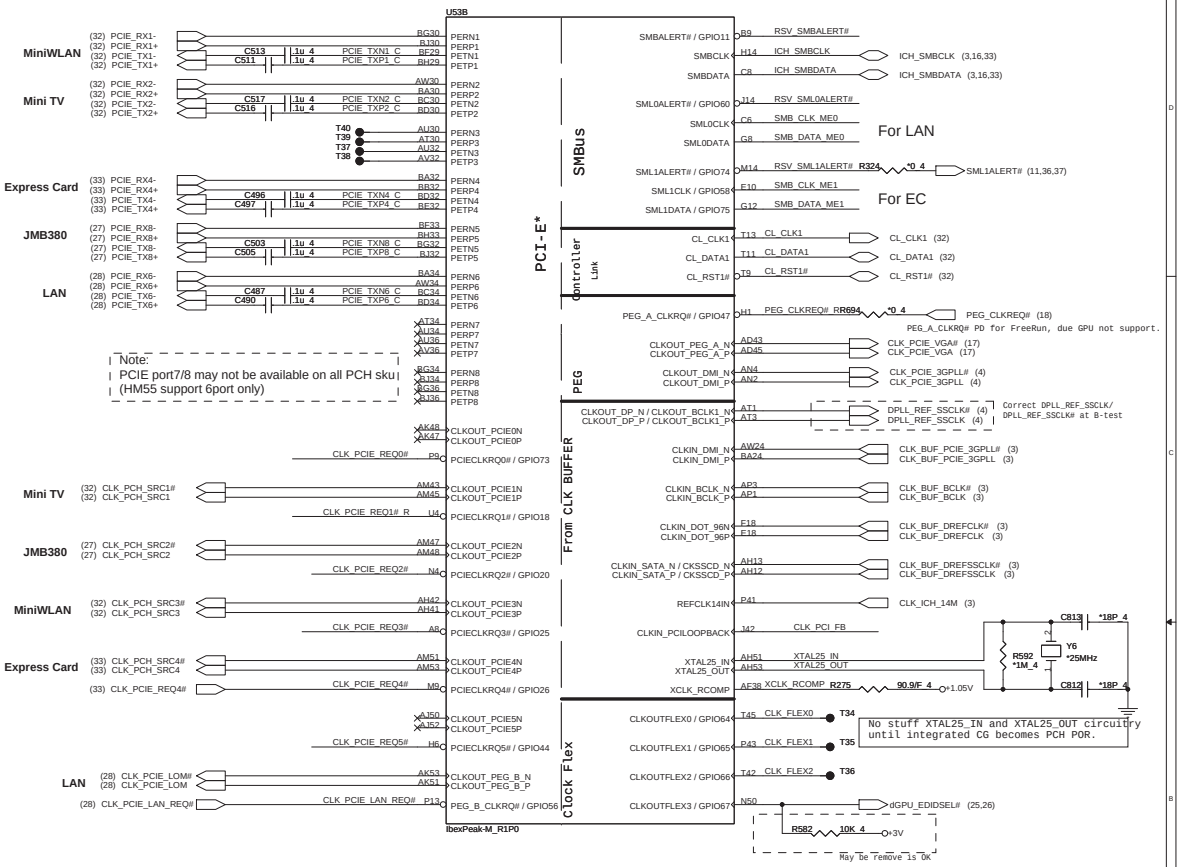
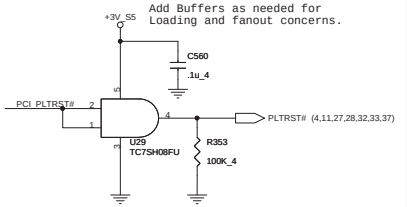
IBEX PEAK-M (PCI,USB,NVRAM)



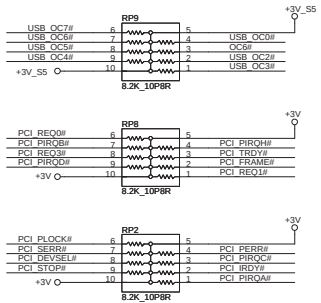
IBEX PEAK-M (PCI-E,SMBUS,CLK)



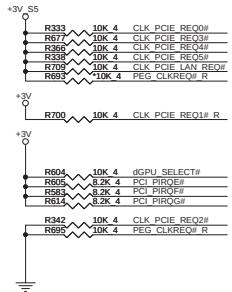
PLTRST#



PCI/USBOC# Pull-up



CLK_REQ/Strap Pin



PEG_A_CLKRQ# PD for FreeRun, due GPU not support.

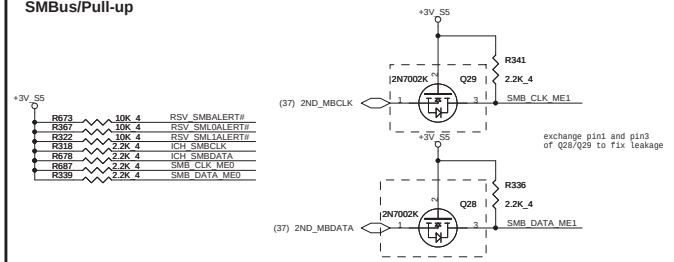
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap		
GNT0#	GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

SMBus/Pull-up



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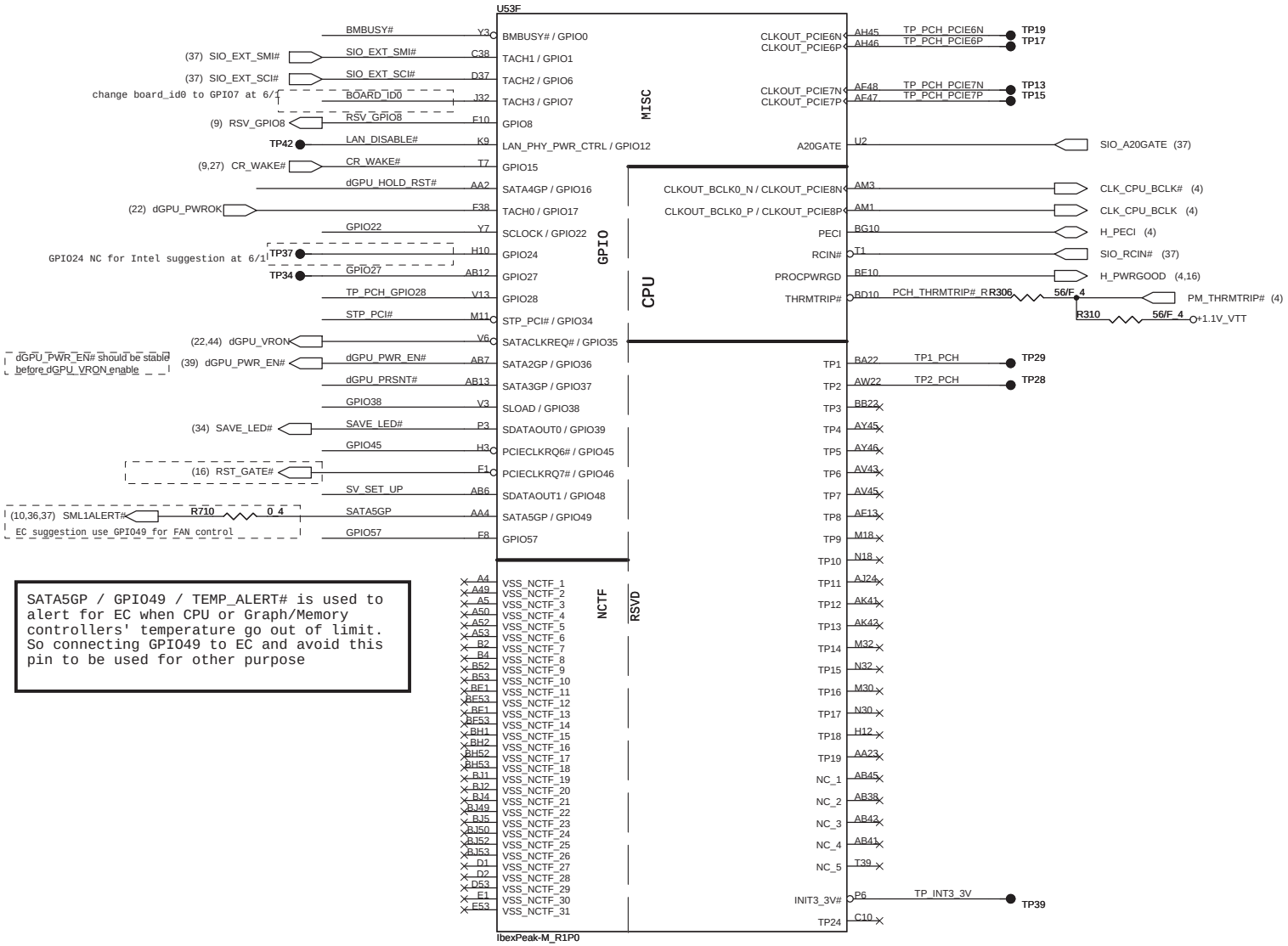
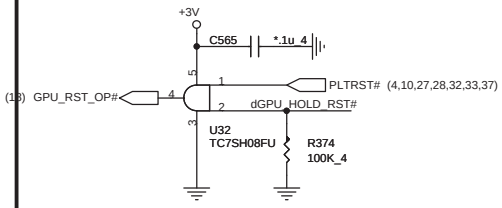
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

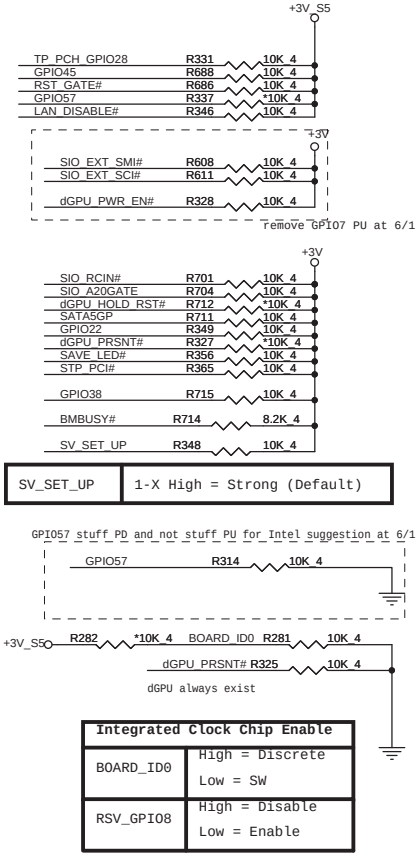


SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

GPU RST#



GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)

Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = SW
RSV_GPIO8	High = Disable Low = Enable

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	IBEX PEAK-M 4/6	1A
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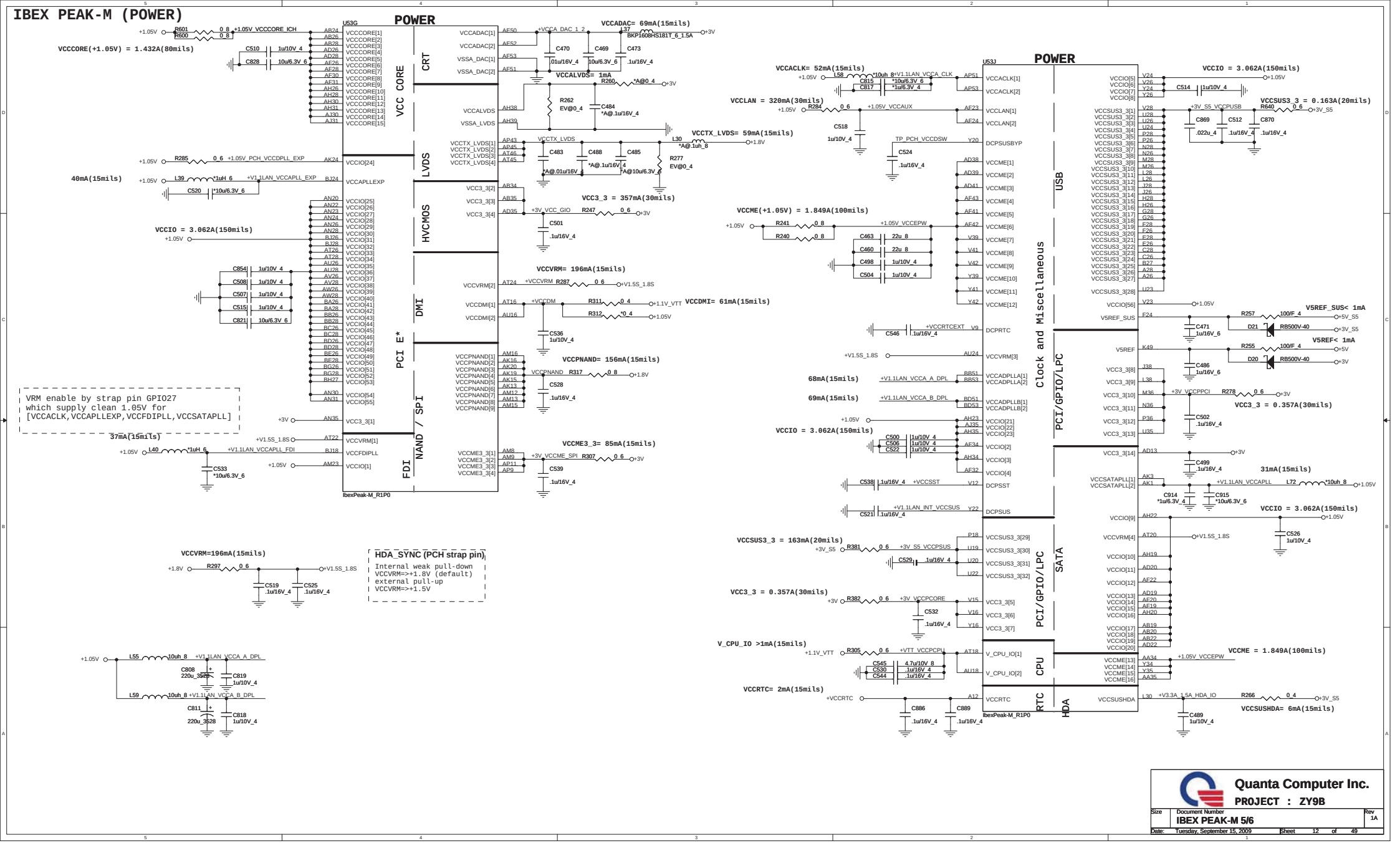
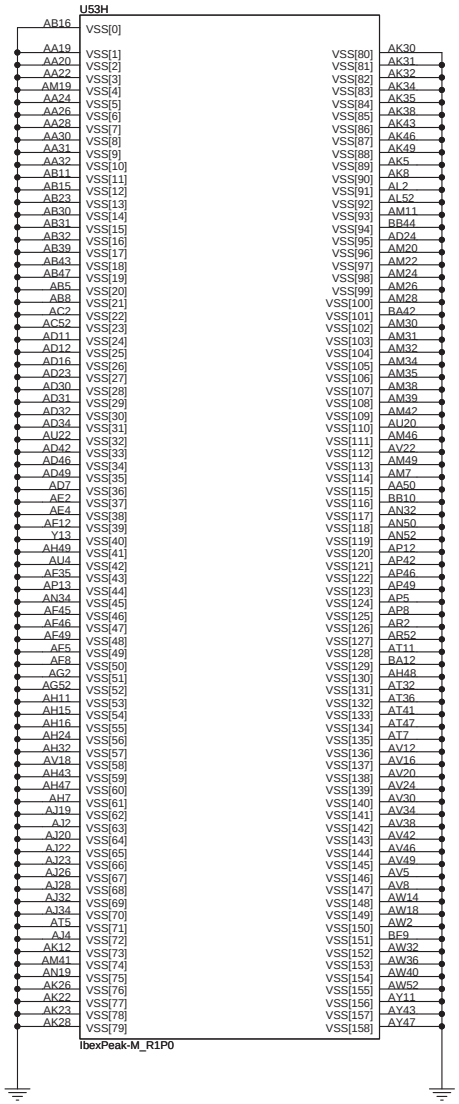
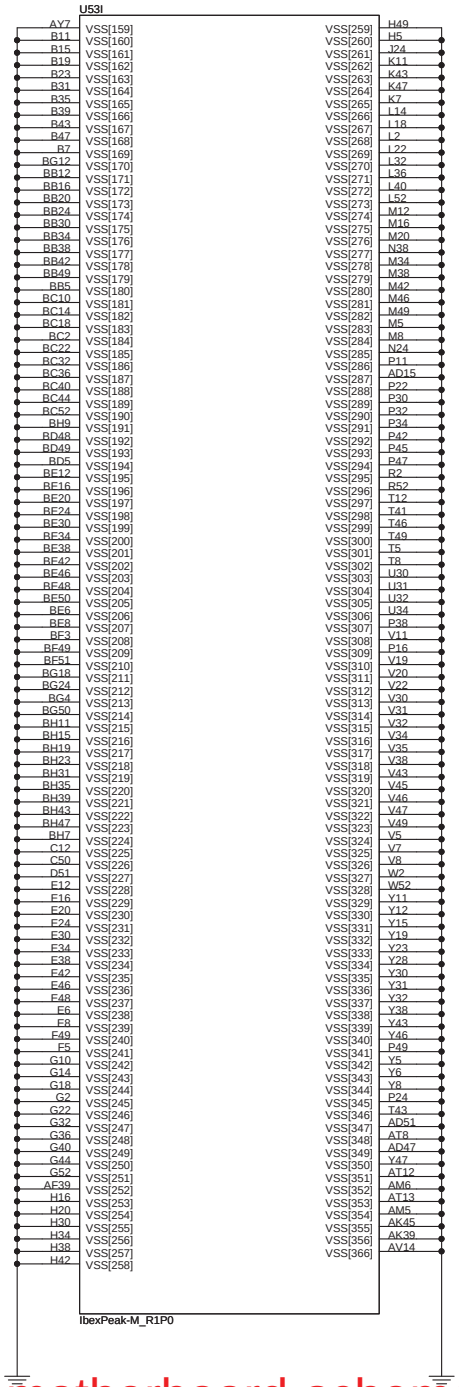
IBEX PEAK-M (POWER)



IBEX PEAK-M (GND)





Quanta Computer Inc.
PROJECT : ZY9B

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A
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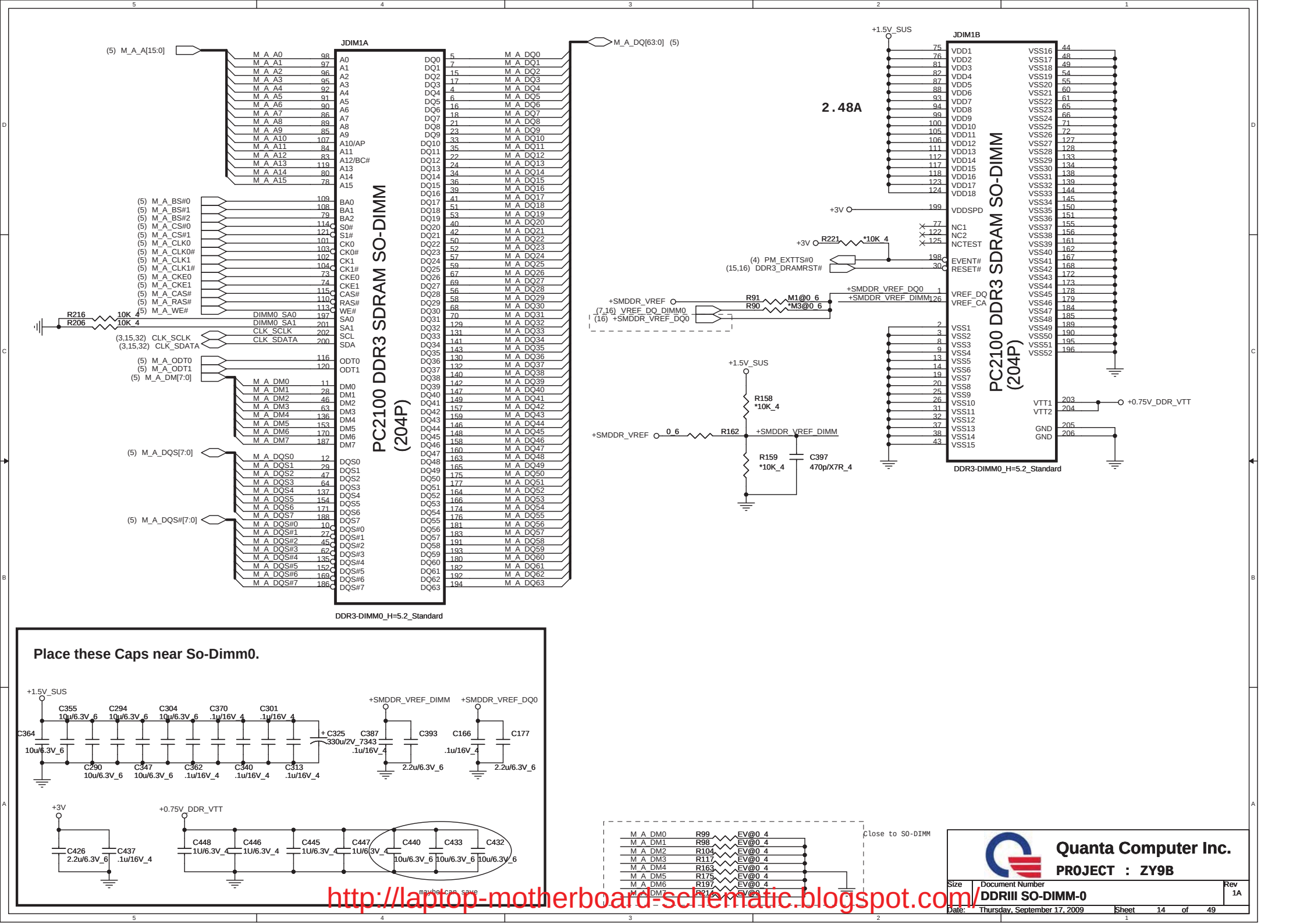

Place these Caps near So-Dimm0.

Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A

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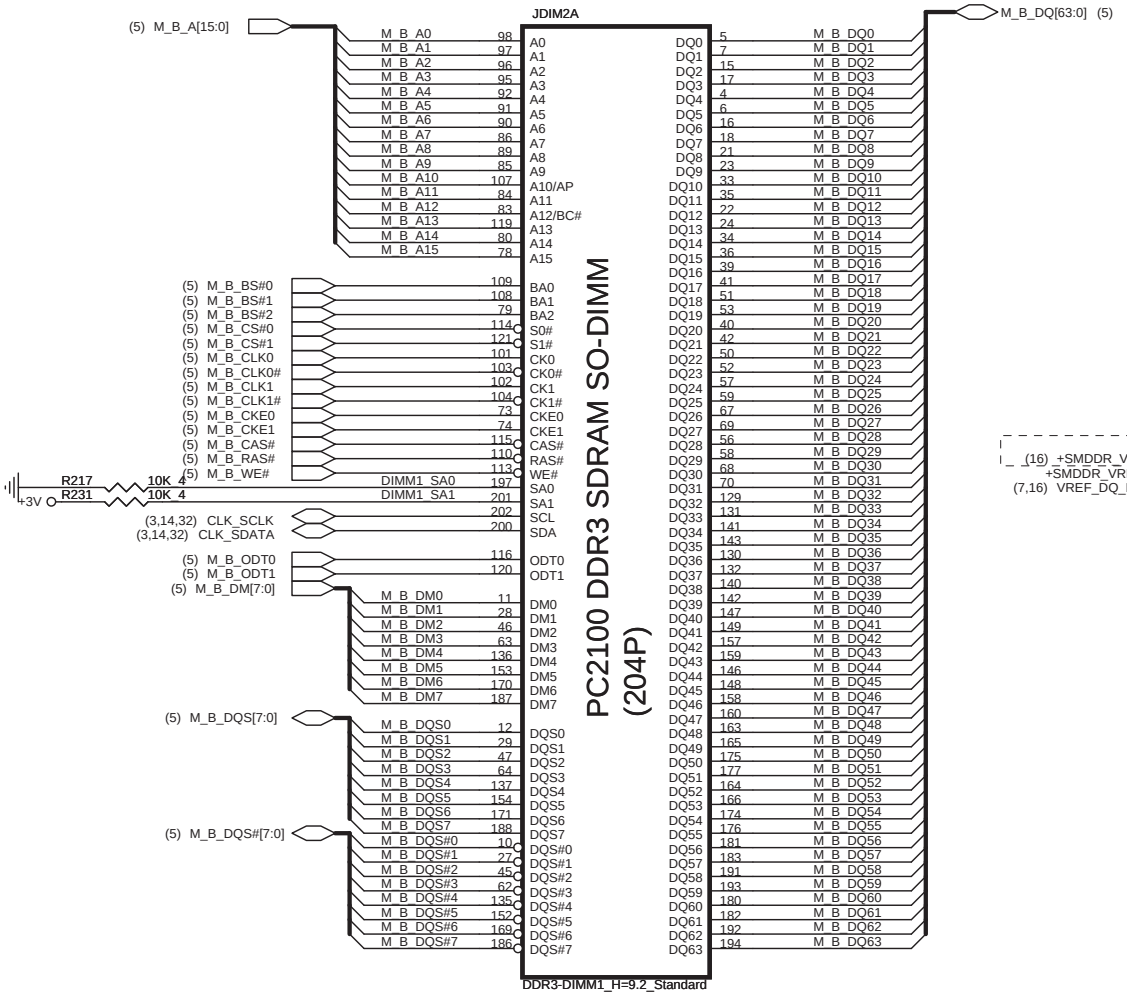

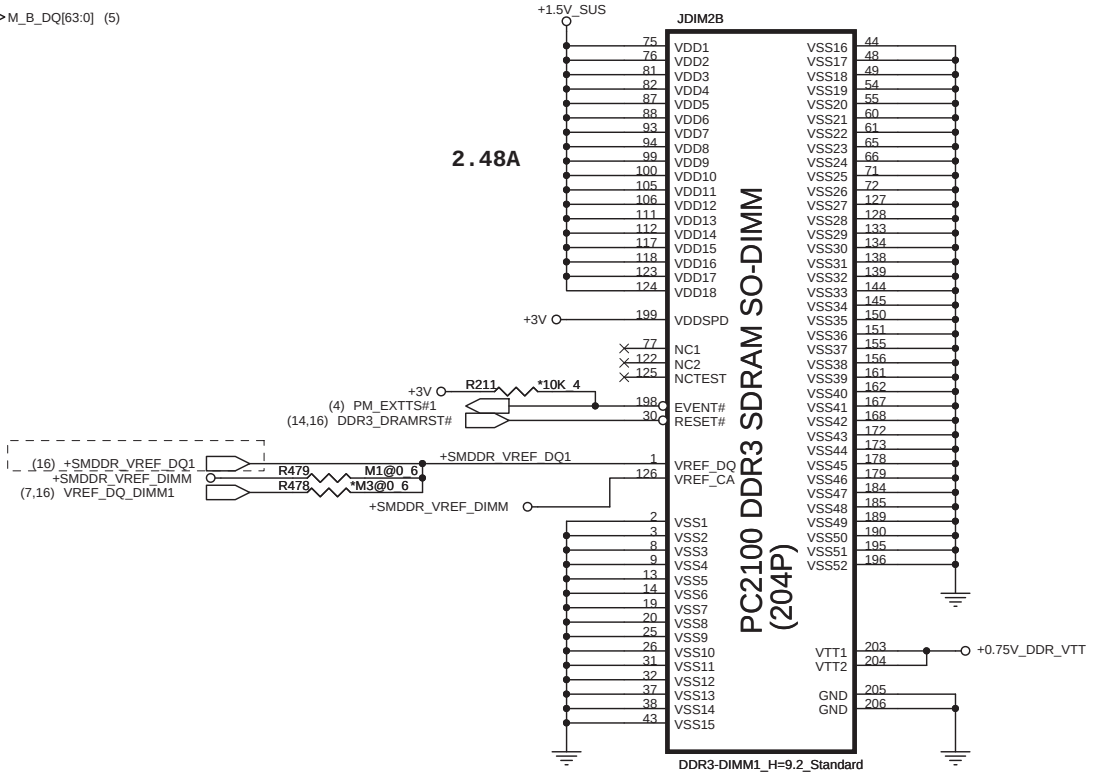

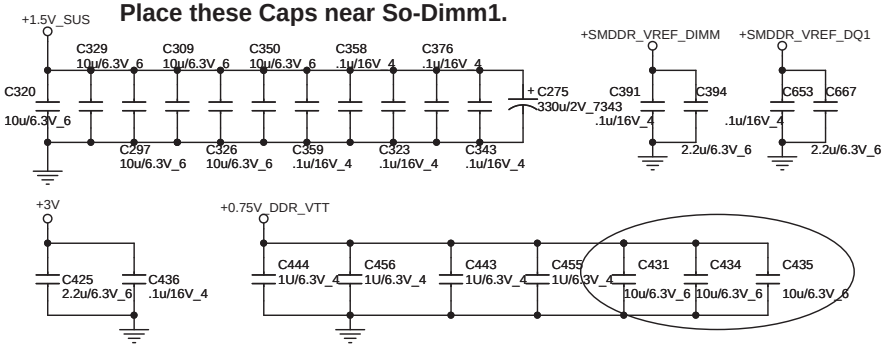

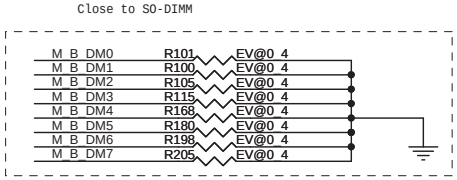

Quanta Computer Inc.
PROJECT : ZY9B

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
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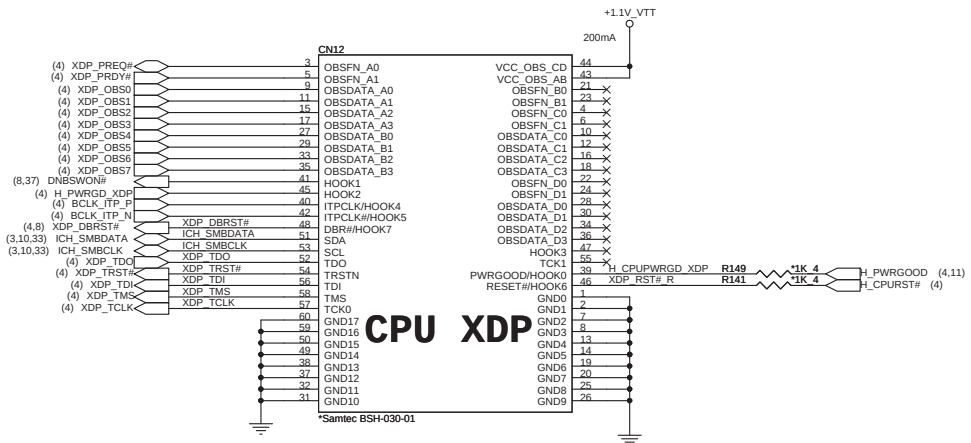
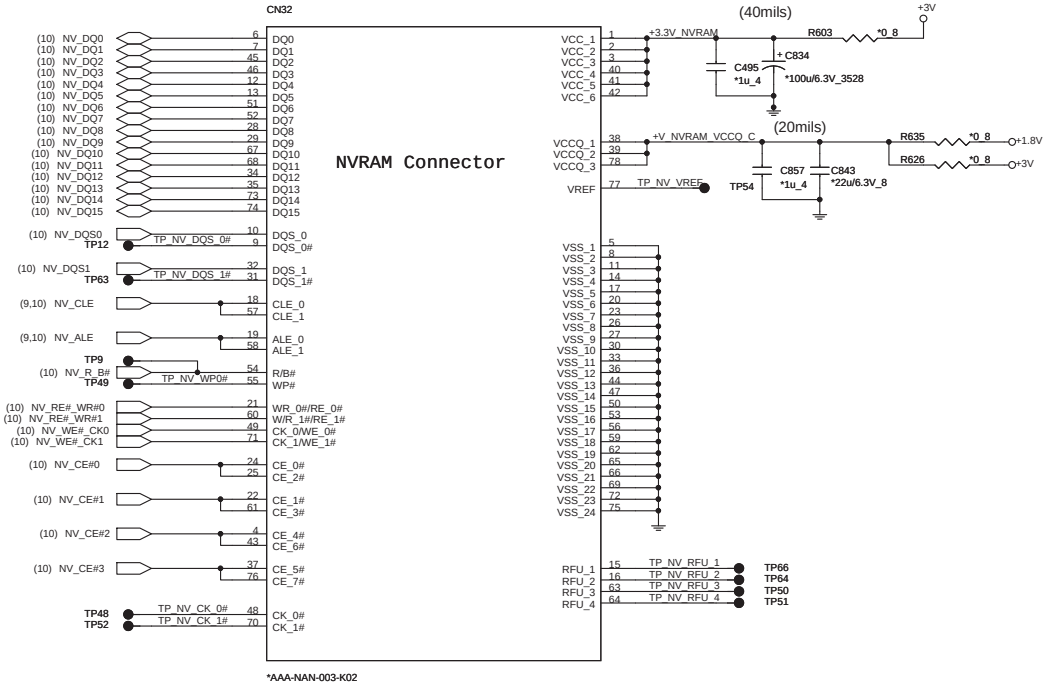
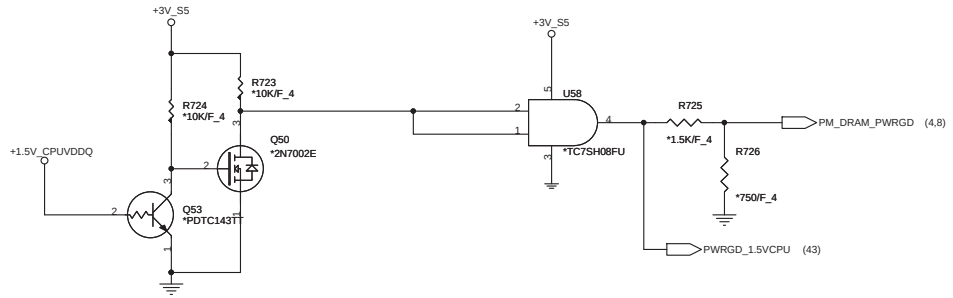
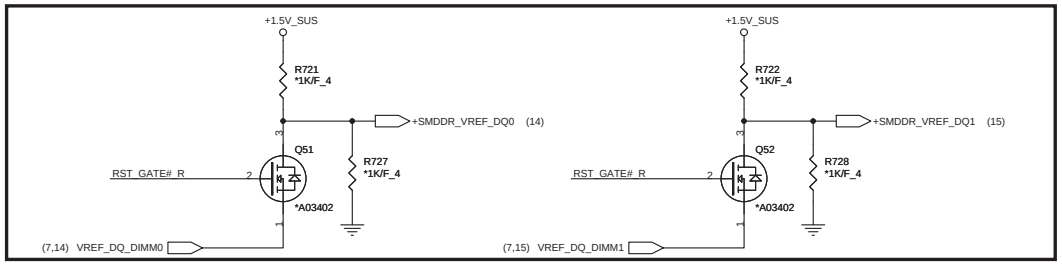
CPU XDP Connector

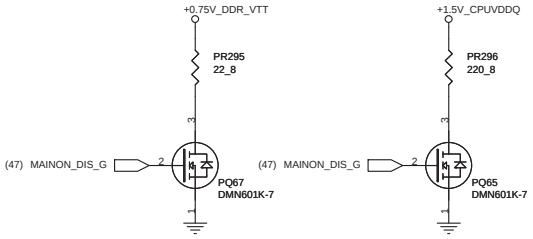


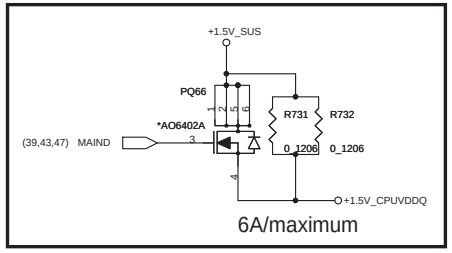
Braidwood

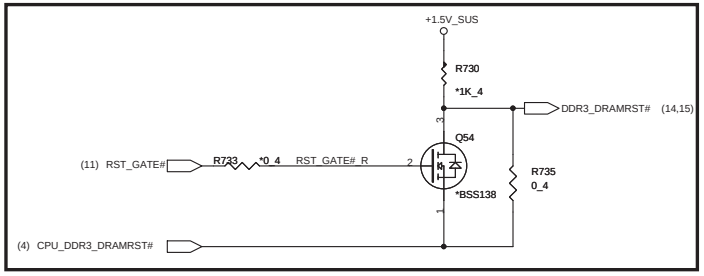


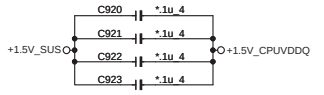




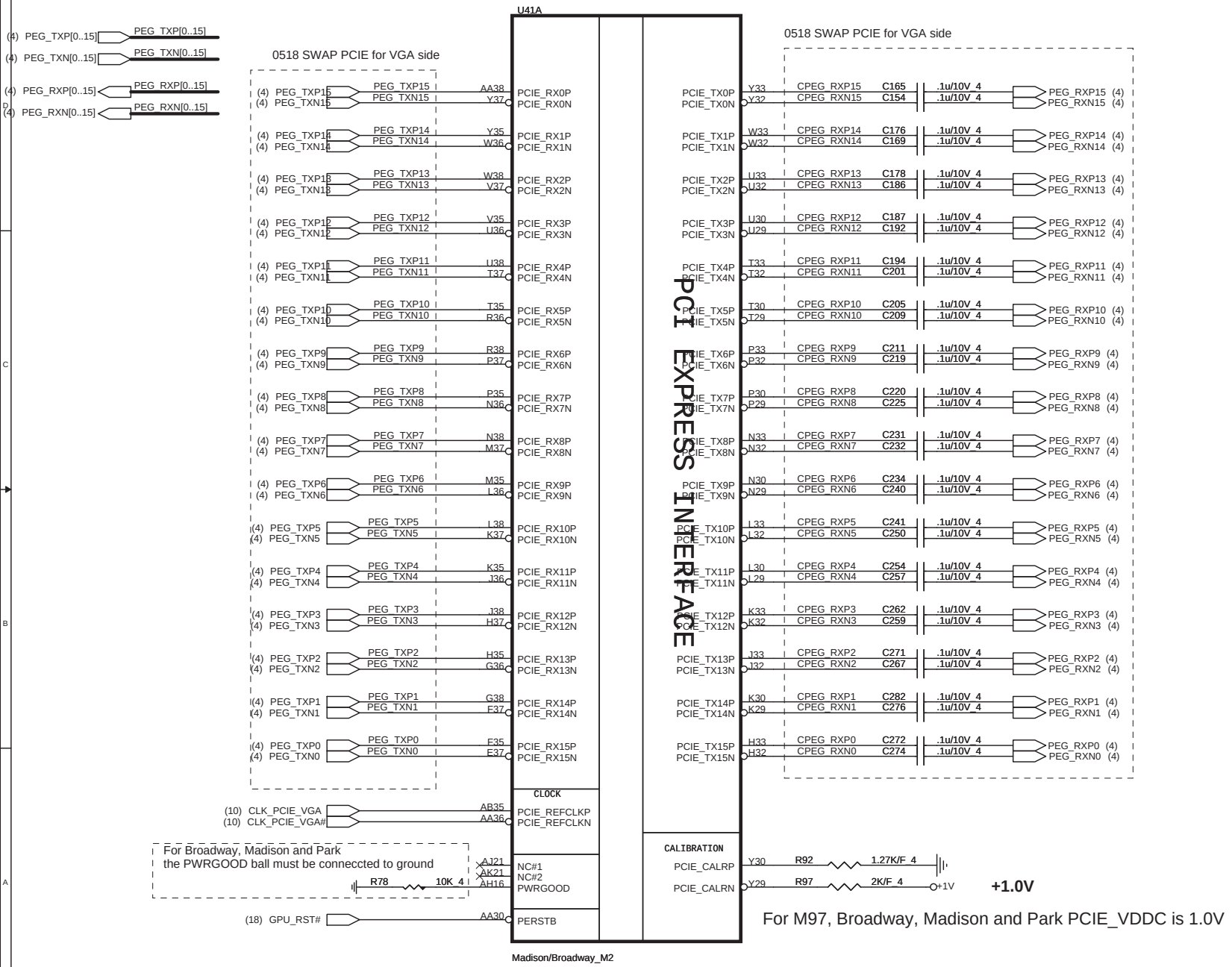






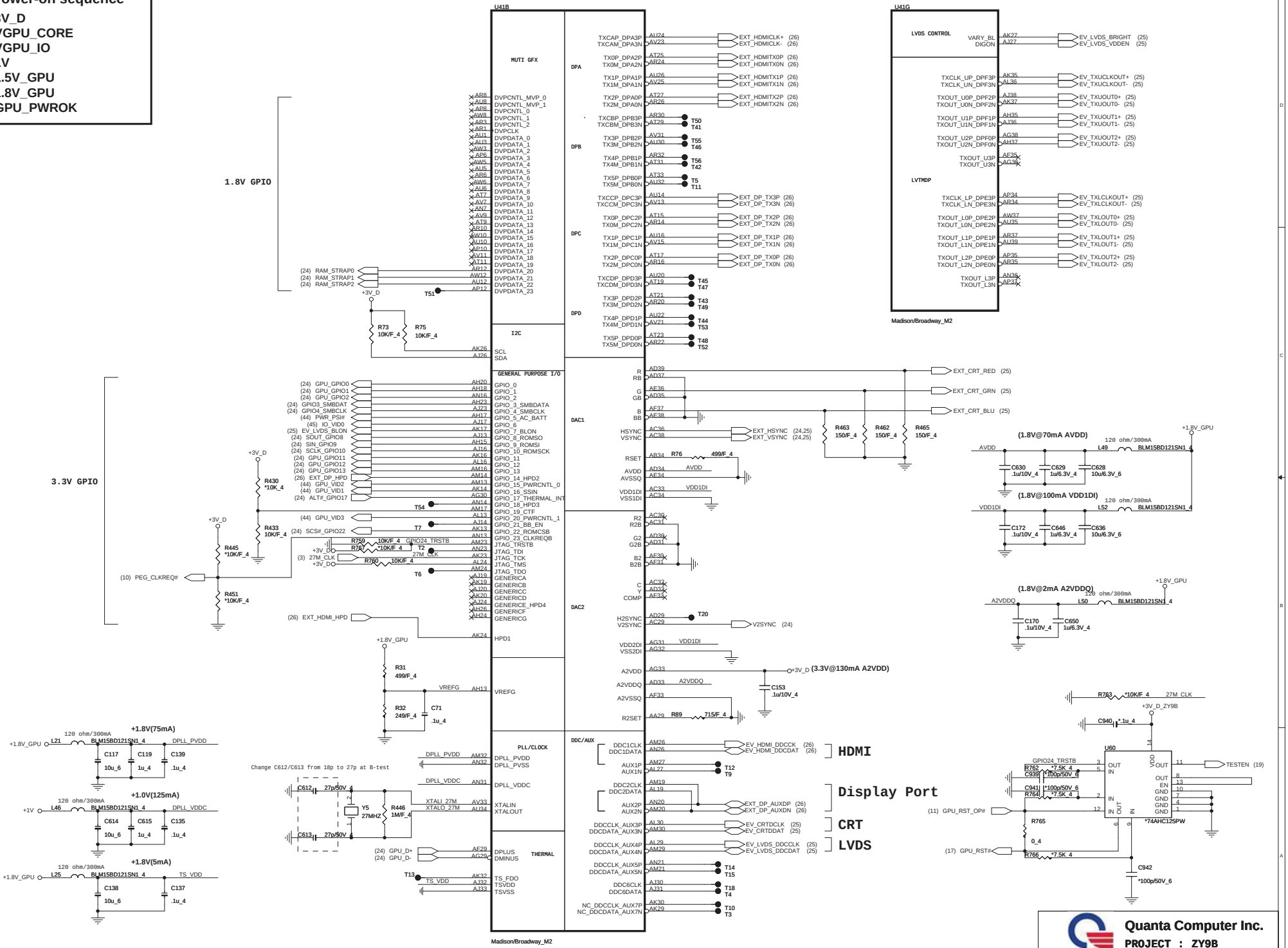


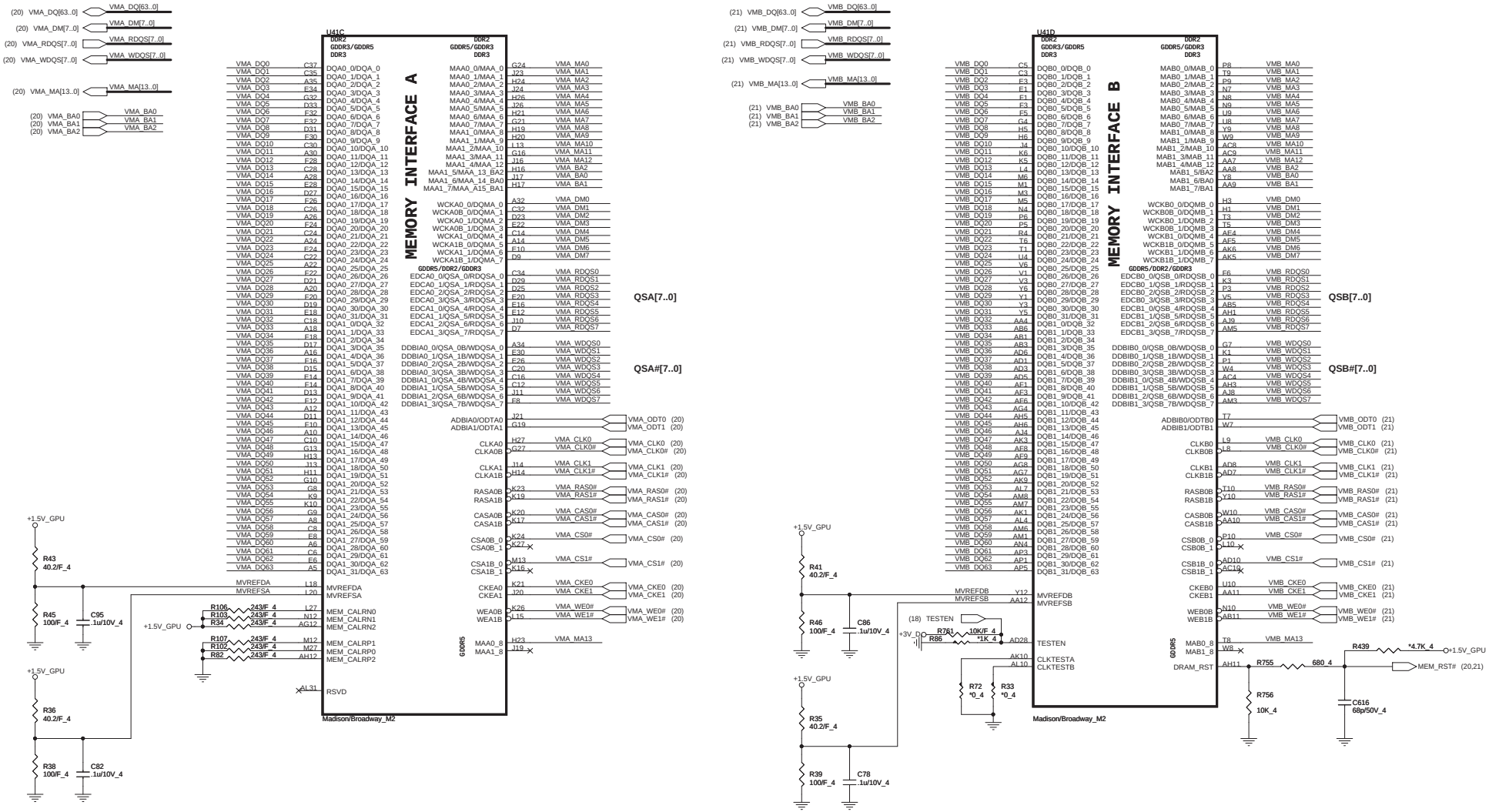
Quanta Computer Inc.		
PROJECT : ZY9		
Size	Document Number: XDP/BRAIDWOOD	Rev: 1A
Date: Thursday, September 17, 2009	Sheet 16 of 49	



GPU Power-on sequence

1 => +3V_D
2 => +VGPU_CORE
3 => +VGPU_IO
4 => +1V
5 => +1.5V_GPU
6 => +1.8V_GPU
7 => dGPU_PWROK





Quanta Computer Inc.			
PROJECT : ZY9B			
Size	Document Number	Madison/Broadway-MEM I/F	Rev 1A
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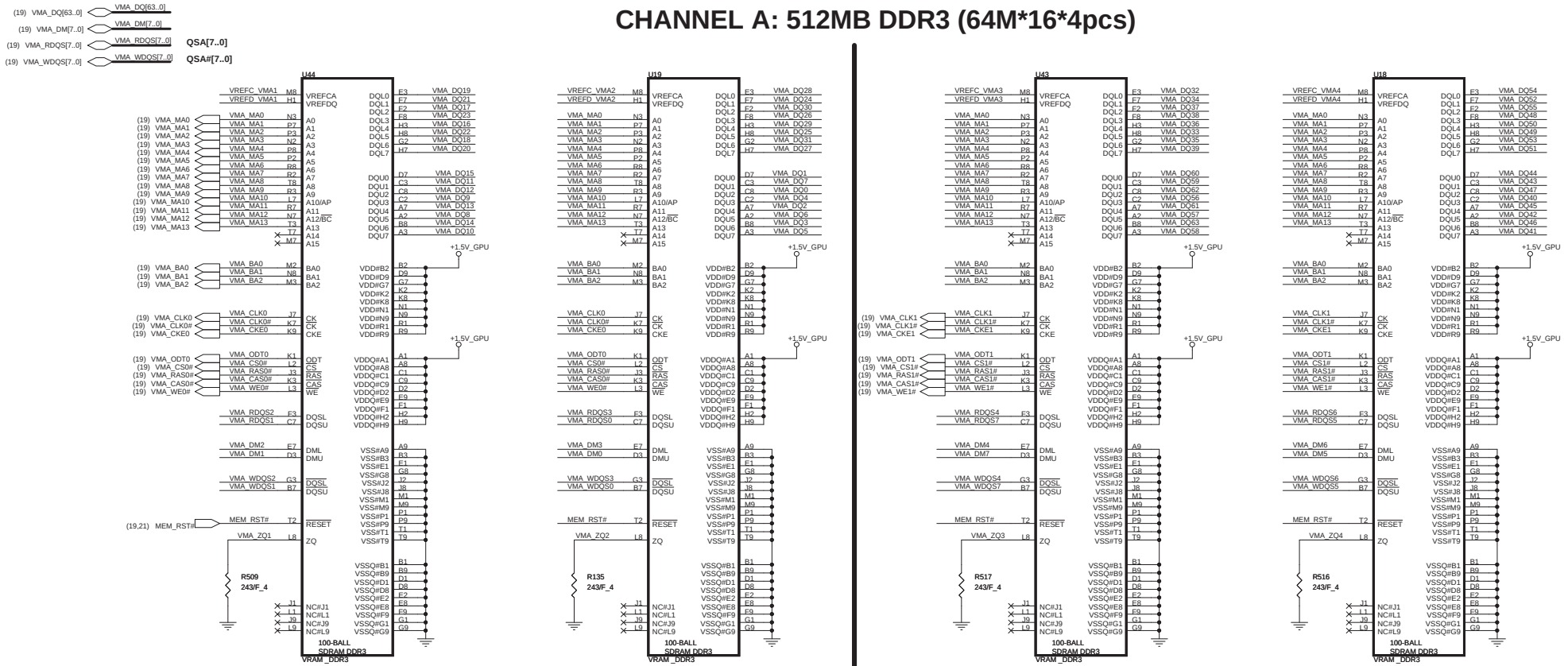
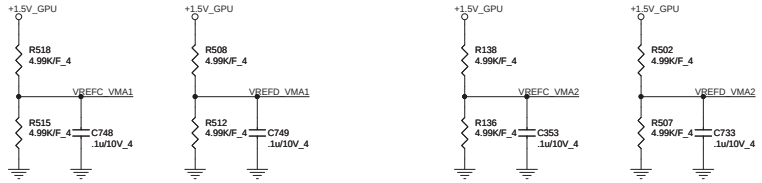
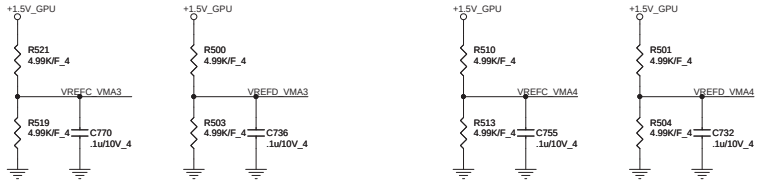
CHANNEL A: 512MB DDR3 (64M*16*4pcs)



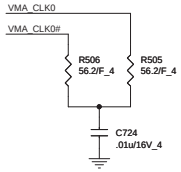
Group-A0 VREF



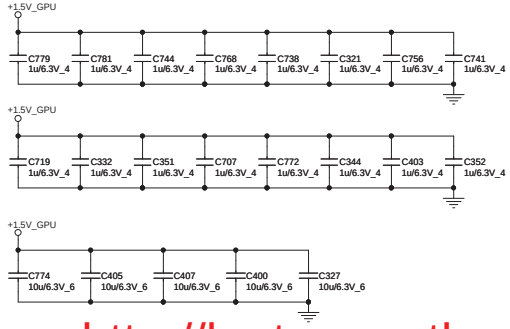
Group-A1 VREF



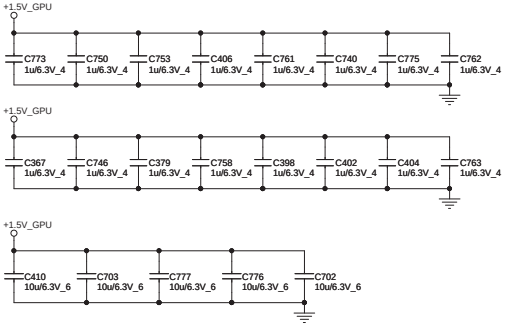
MEM_A0 CLK



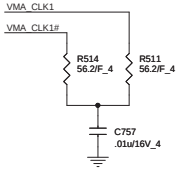
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



Quanta Computer Inc.
PROJECT : ZY9B

Size	Document Number	Rev
	MEMORY 1 channel A	1A
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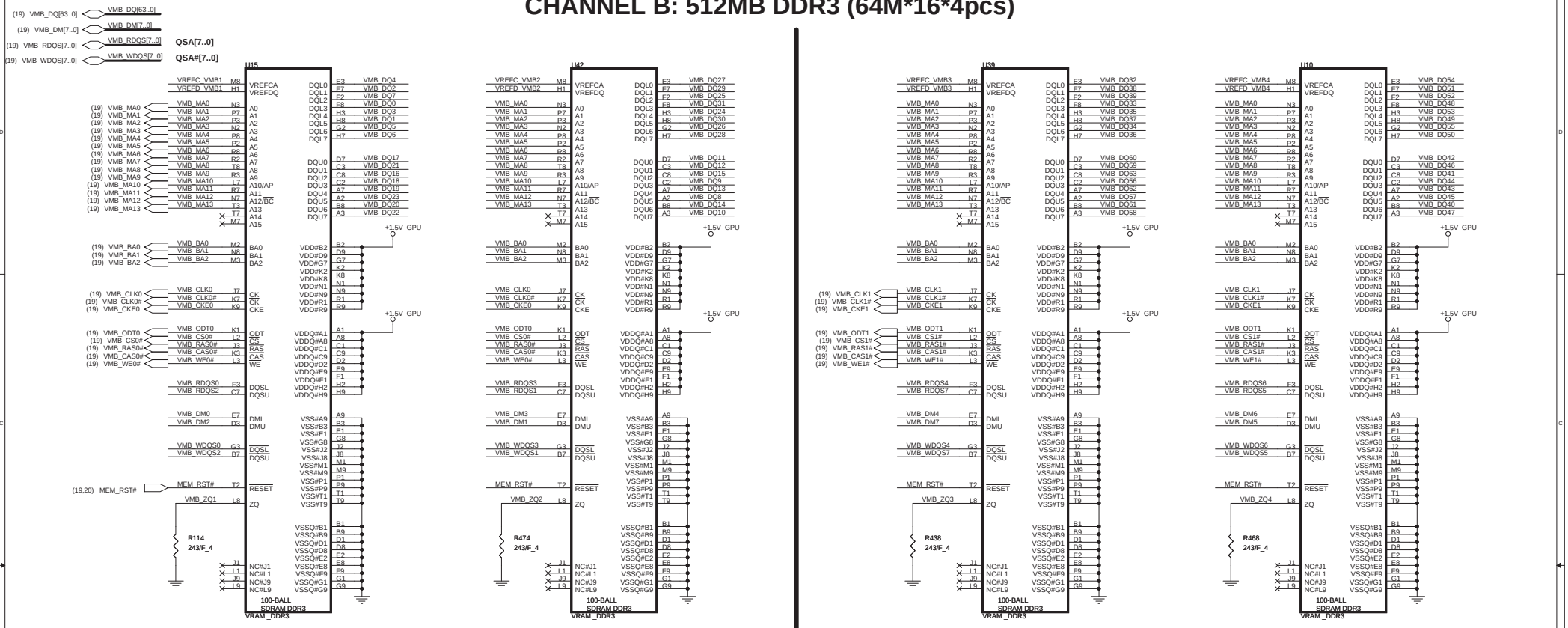
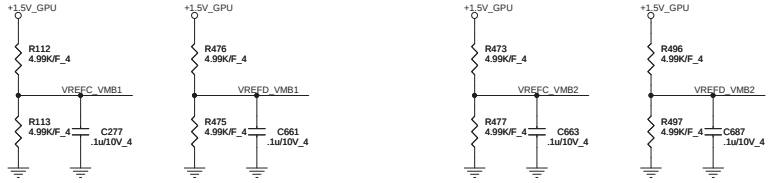
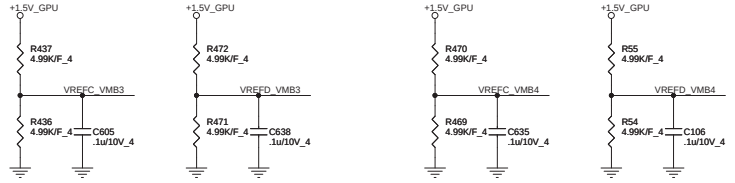
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



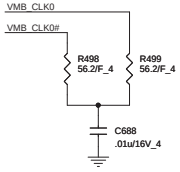
Group-B0 VREF



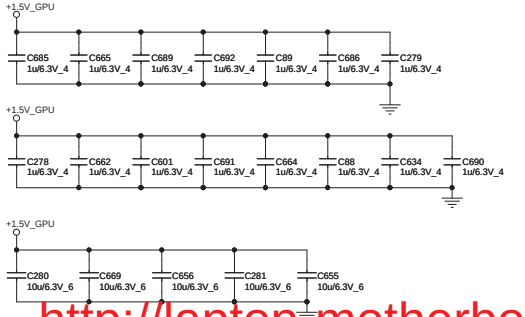
Group-B1 VREF



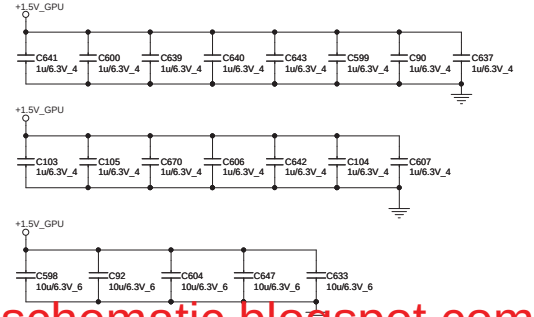
MEM_B0 CLK



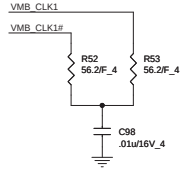
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.			
PROJECT : ZY9B			
Size	Document Number	MEMORY 2 channel B	Rev 1A
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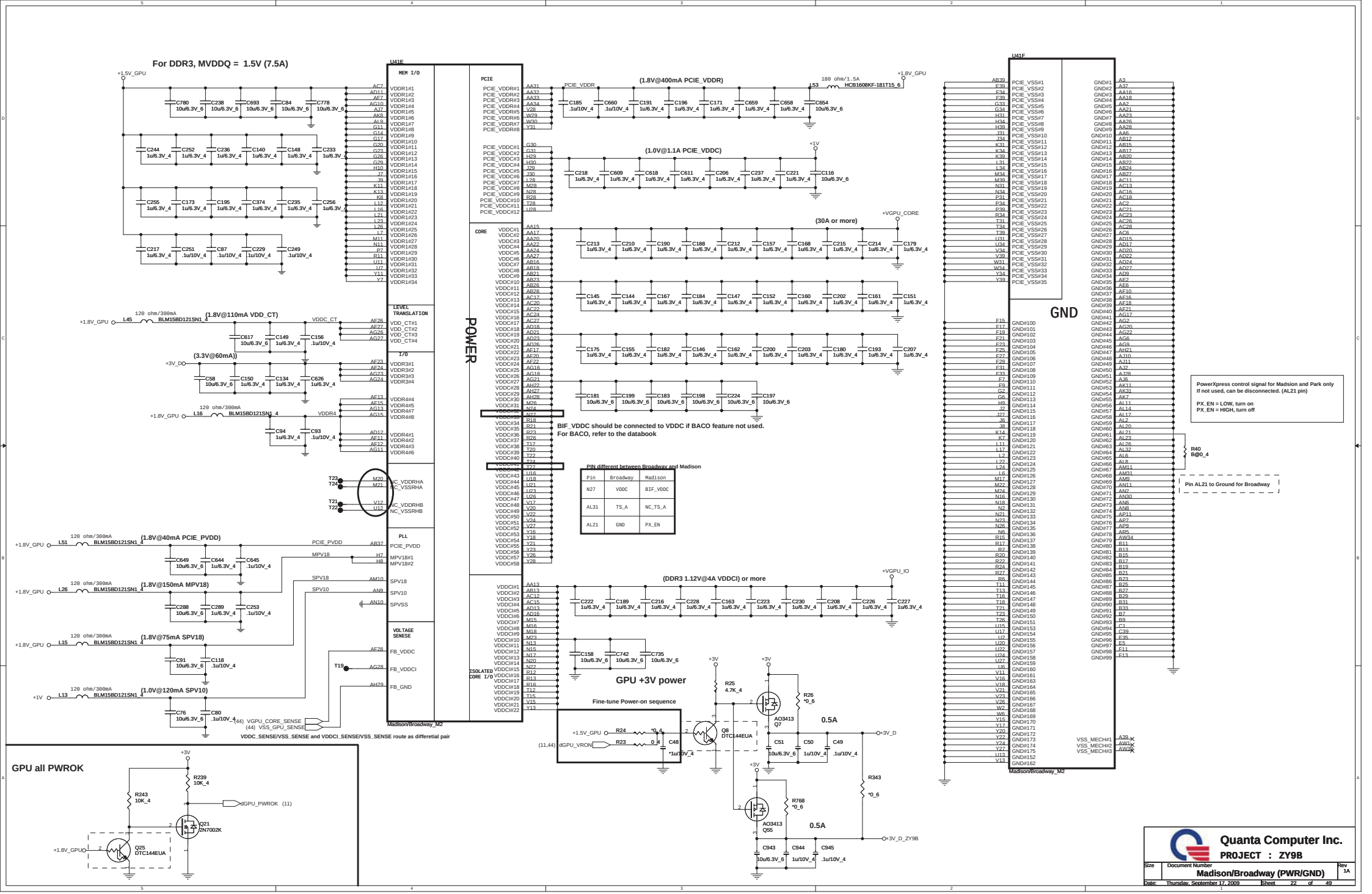
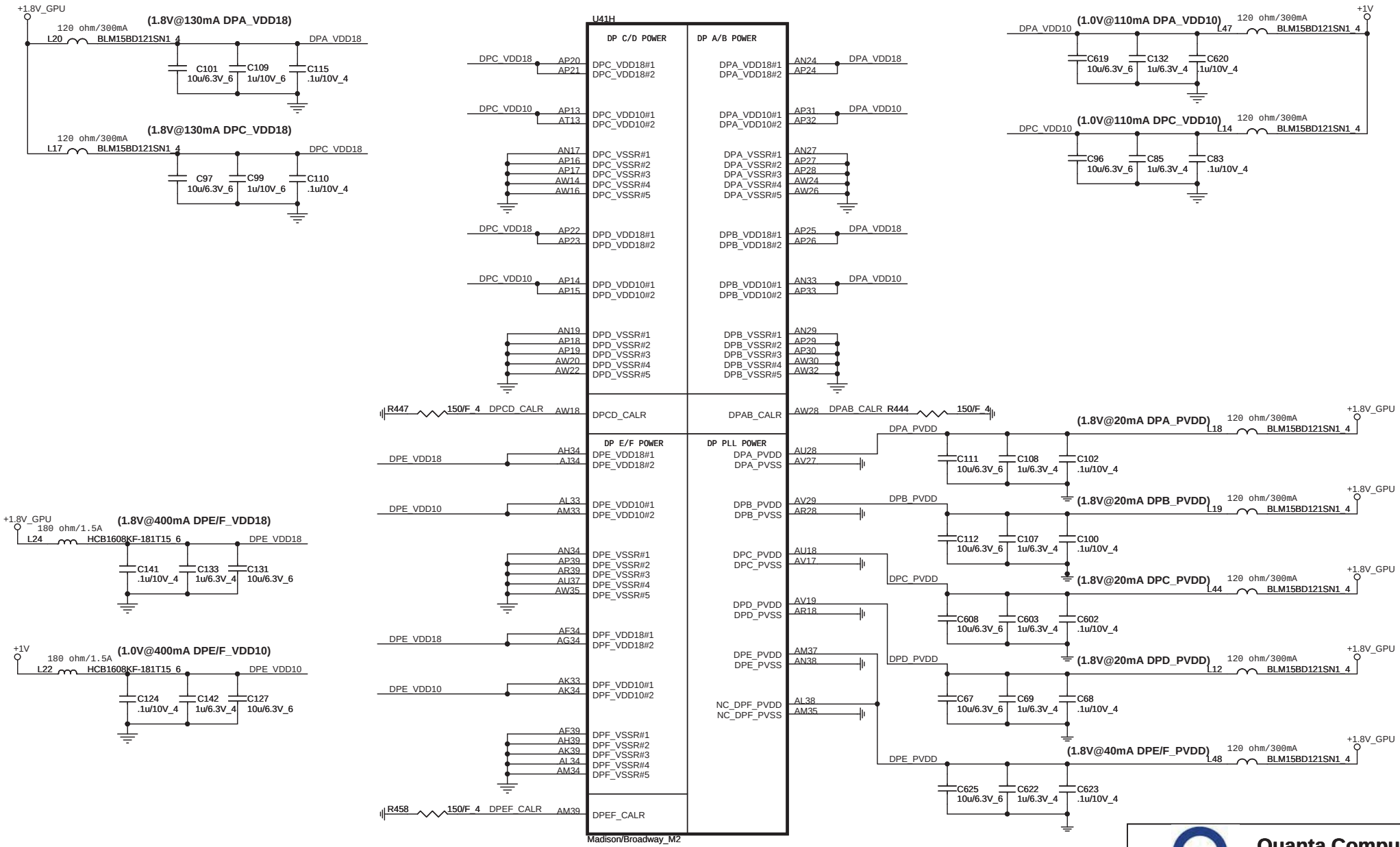
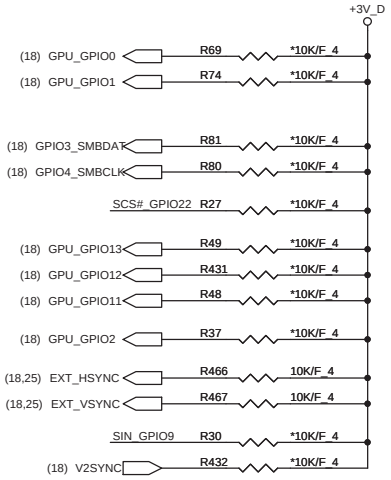




PIN STRAPS



Memory Aperture size	
GPIO[13:11]	**Size**
000	**128MB**
001	256MB
010	64MB
011	32MB

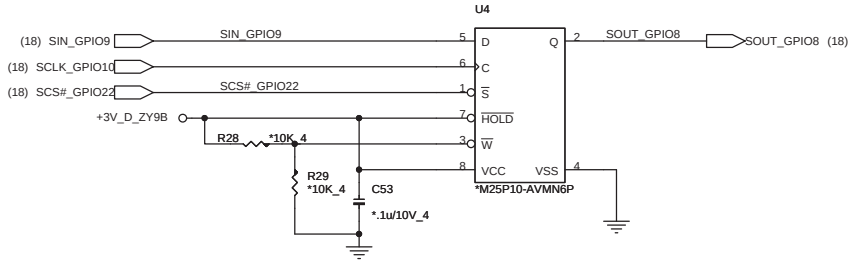
Audio Table		
EXT_HSYNC	**EXT_VSYNC**	**Discription**
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	**Both DP & HDMI**

CONFIGURATION STRAPS

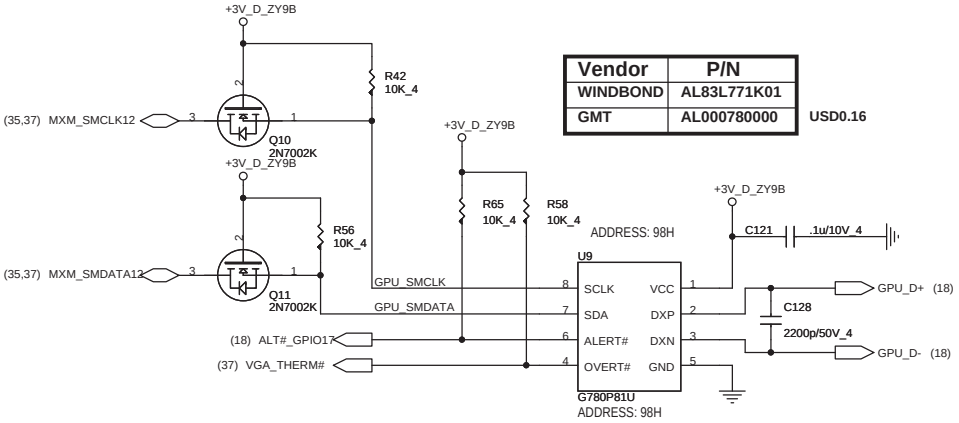
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	**0**	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	**0**	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	**0**	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	**000**	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	**0**	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	**11**	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	**0**	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	**0**	

EEPROM



Thermal Sensor



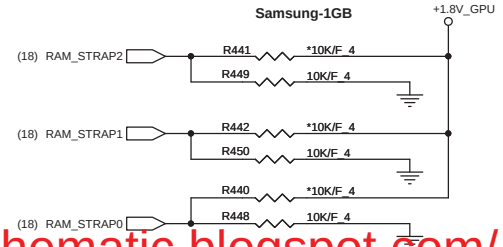
Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

USD0.16

DDR3 VRAM SIZE Strap

DDR3 VRAM size

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	512MB	1	1	0
			1GB	1	0	0
			2GB			
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	512MB	0	1	0
			1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

Quanta Computer Inc.
PROJECT : ZY9B

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	Strip/Thermal	1A
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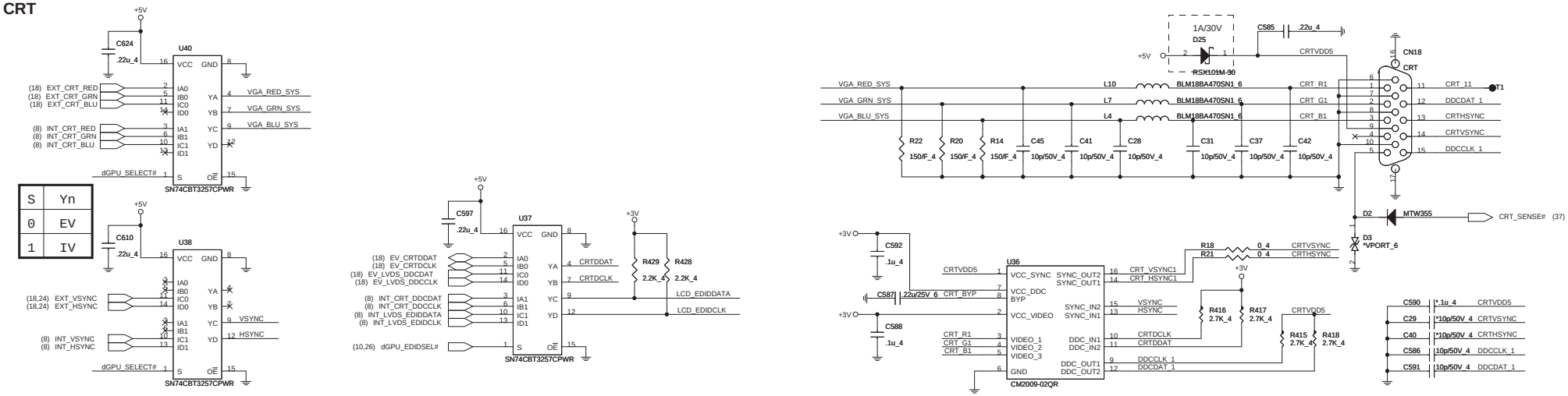
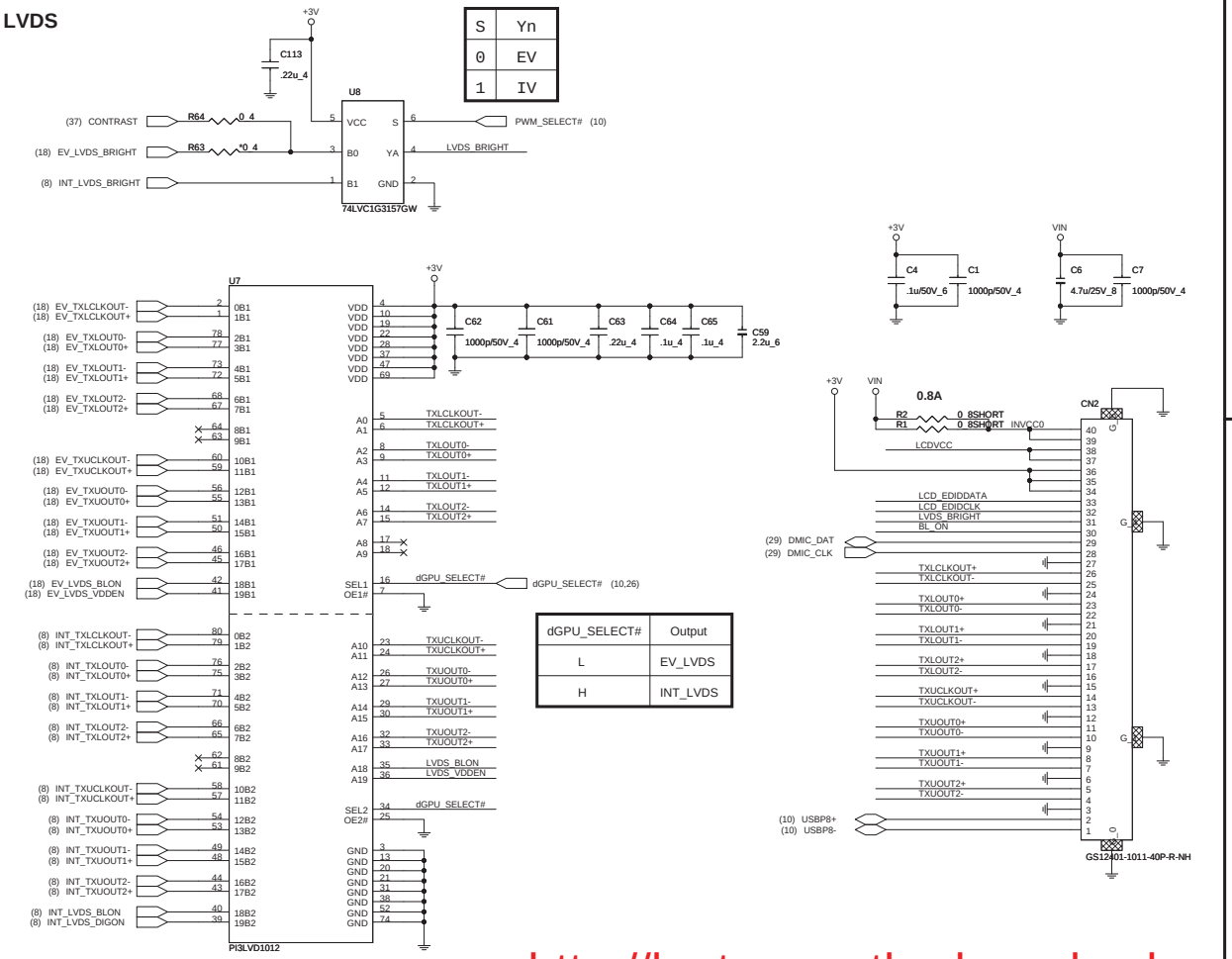
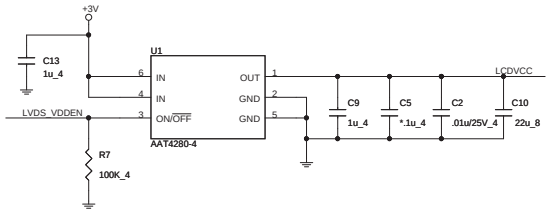
CRT



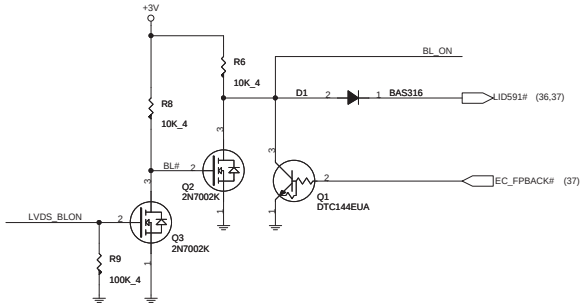
LVDS



LCD Power



Backlight Control



Quanta Computer Inc.
PROJECT : ZY9B

Size	Document Number	Rev
	CRT/LVDS/LID	1A

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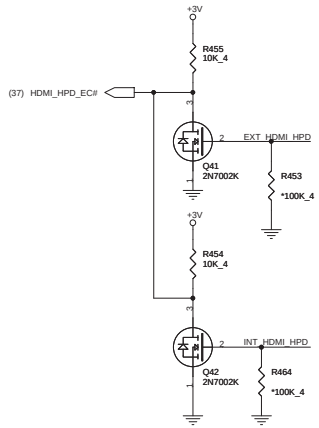
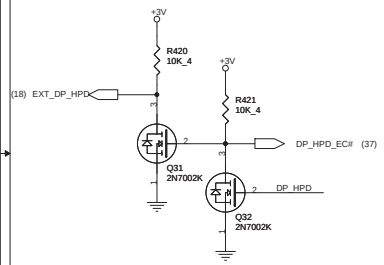
HDMI Hot-PLUG to EC and GPU

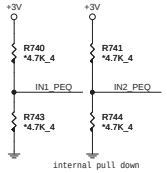


DP Hot-PLUG to EC and GPU

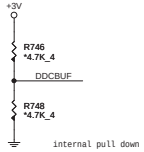


HDMI

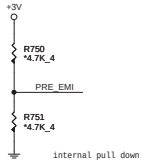
Input EQ setting	
INn_PEQ	Output
L	Middle EQ
H	High EQ
M	Low EQ



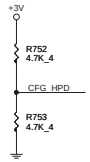
DDC Buffer setting	
DDC_BUF	Output
L	Passive DDC
H	Active Set-1
M	Active Set-2

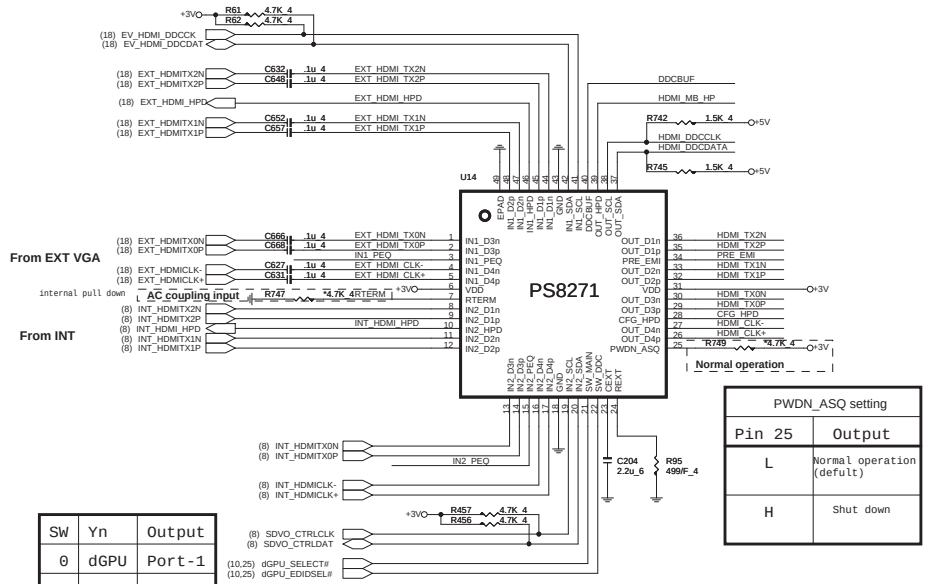


Pre-emphasis and EMI setting	
PRE_EMI	Output
L	No_PRE&EMI
H	PRE enable
M	EMI control



Hot-plug detect	
CFG_HPD	Output
L	Follow SW_MAIN
H	Follow SW_DDC
M	SW or DDC

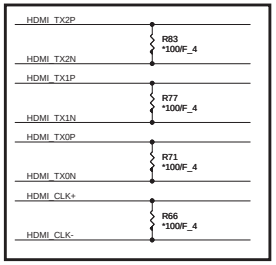




SW	Yn	Output
0	dGPU	Port-1
1	UMA	Port-2

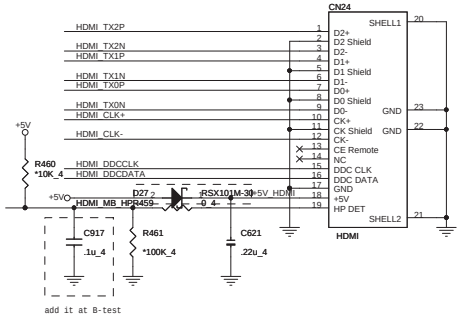
PWDN_ASQ setting	
Pin 25	Output
L	Normal operation (defult)
H	Shut down

EMI reserve for HDMI

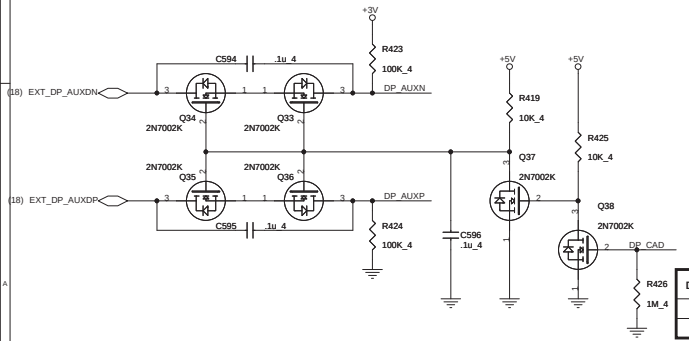


Close CN24

HDMI connector

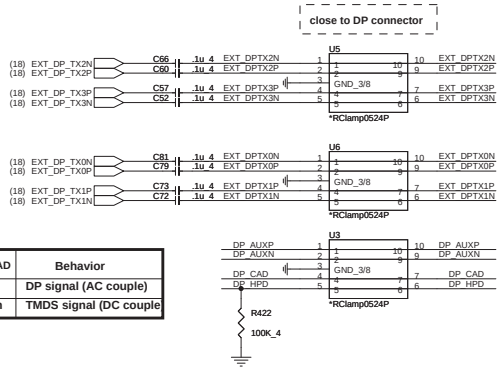


DisplayPort

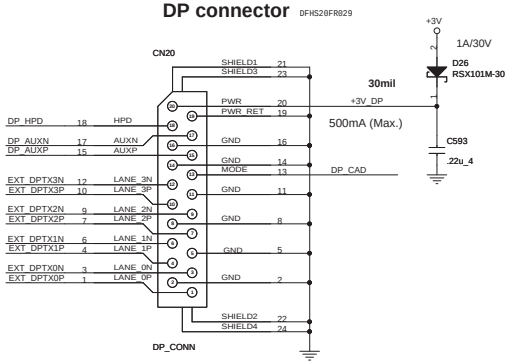


DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple

ESD Protect

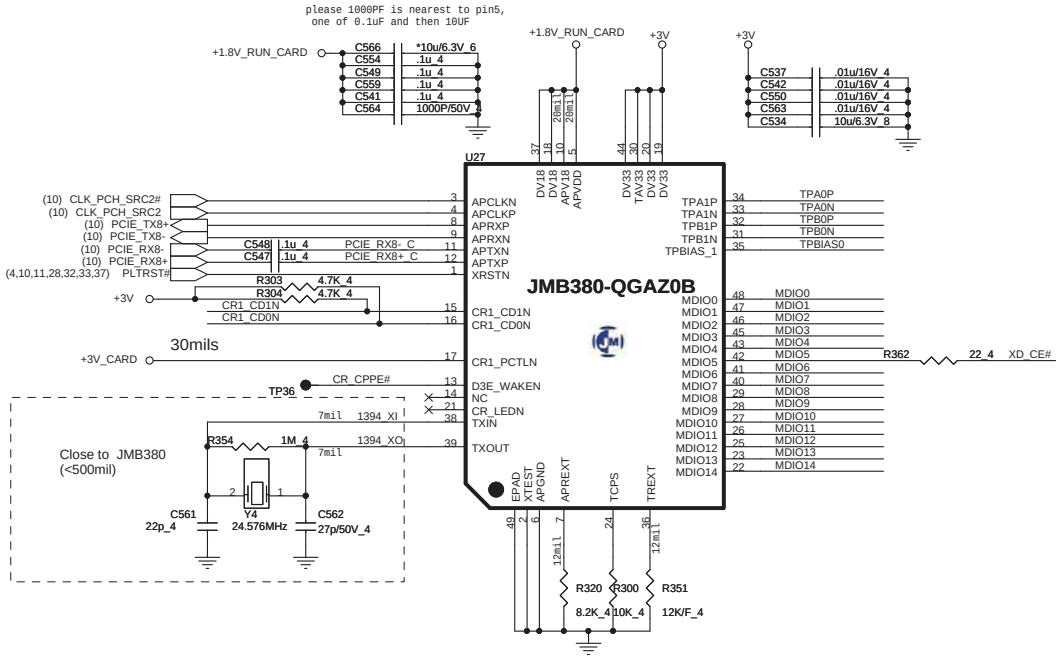


DP connector

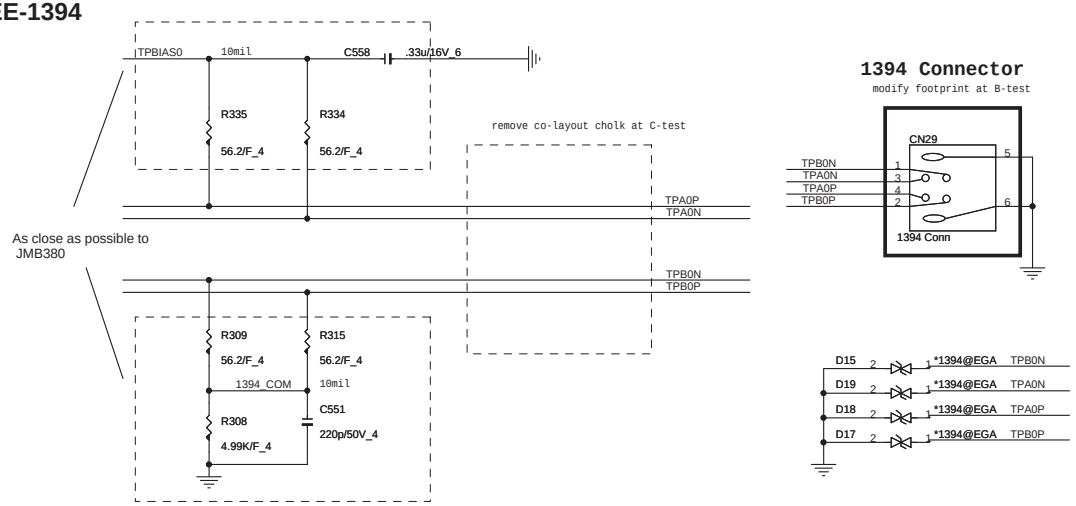


Quanta Computer Inc.	
PROJECT : ZY9B	
Size: Document Number: HDMI/DP	Rev 1A
Date: Monday, September 21, 2009	Sheet 26 of 49

Cardreader/1394

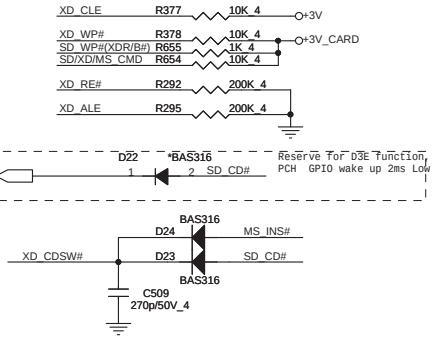


IEEE-1394



1394 Connector

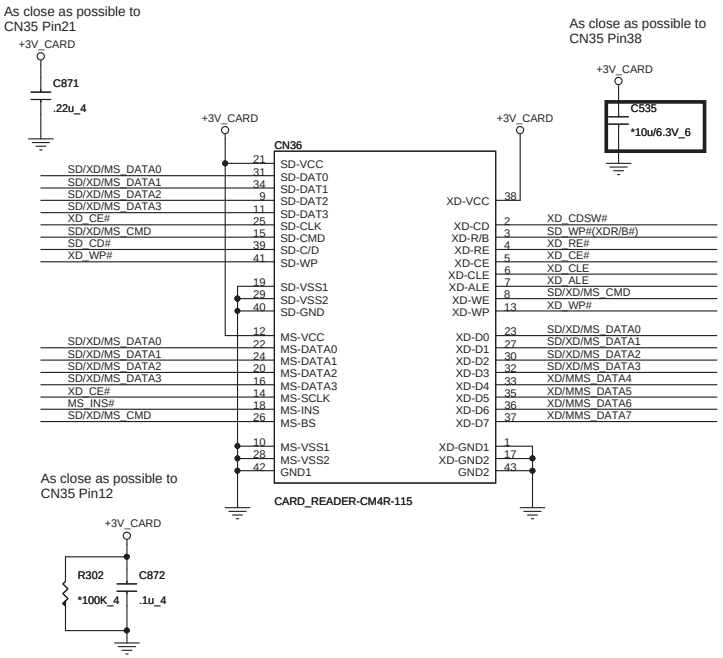
modify footprint at B-test



JMB 380 pin Note:

	SD/MMC	MS	XD
MDID0	SD_DAT0	MS_D0	XD_D0
MDID1	SD_DAT1	MS_D1	XD_D1
MDID2	SD_DAT2	MS_D2	XD_D2
MDID3	SD_DAT3	MS_D3	XD_D3
MDID4	SD_CMD	MS_BS	XD_WE#
MDID5	SD_CLK	MS_SCLK	XD_CE#
MDID6	SD_WP		XD_WP#
MDID7			XD_CLE
MDID8	SD_DAT4		XD_D4
MDID9	SD_DAT5		XD_D5
MDID10	SD_DAT6		XD_D6
MDID11	SD_DAT7		XD_D7
MDID12			XD_RE#
MDID13			XD_R/B#
MDID14			XD_ALE
CR1_LEDN	SD1_LED#	MS1_LED#	XD_LED#
CR1_PCTLN	SD1_PCTL#	MS1_PCTL#	XD1_PCTL#
CR1_CD0	SD1_CD#		XD_CV#
CR1_CD1		MS1_CD#	XD_CD#

5 IN 1 CARD READER



EMI reserve

MDIO0	R651	0_4	SD/XD/MS_DATA0
MDIO1	R648	0_4	SD/XD/MS_DATA1
MDIO2	R652	0_4	SD/XD/MS_DATA2
MDIO3	R650	0_4	SD/XD/MS_DATA3
MDIO4	R653	0_4	SD/XD/MS_CMD
MDIO6	R361	0_4	XD_WP#
MDIO7	R360	0_4	XD_CLE
MDIO8	R649	0_4	XD/MMS_DATA4
MDIO9	R647	0_4	XD/MMS_DATA5
MDIO10	R646	0_4	XD/MMS_DATA6
MDIO11	R645	0_4	XD/MMS_DATA7
MDIO12	R299	0_4	XD_RE#
MDIO13	R656	0_4	SD_WP#(XDR/B#)
MDIO14	R301	0_4	XD_ALE
CR1_CD1N	R294	0_4	MS_INS#
CR1_CD0N	R293	0_4	SD_CD#

Quanta Computer Inc.

PROJECT : ZY9B

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	JMB380 Card Reader & 1394	1A

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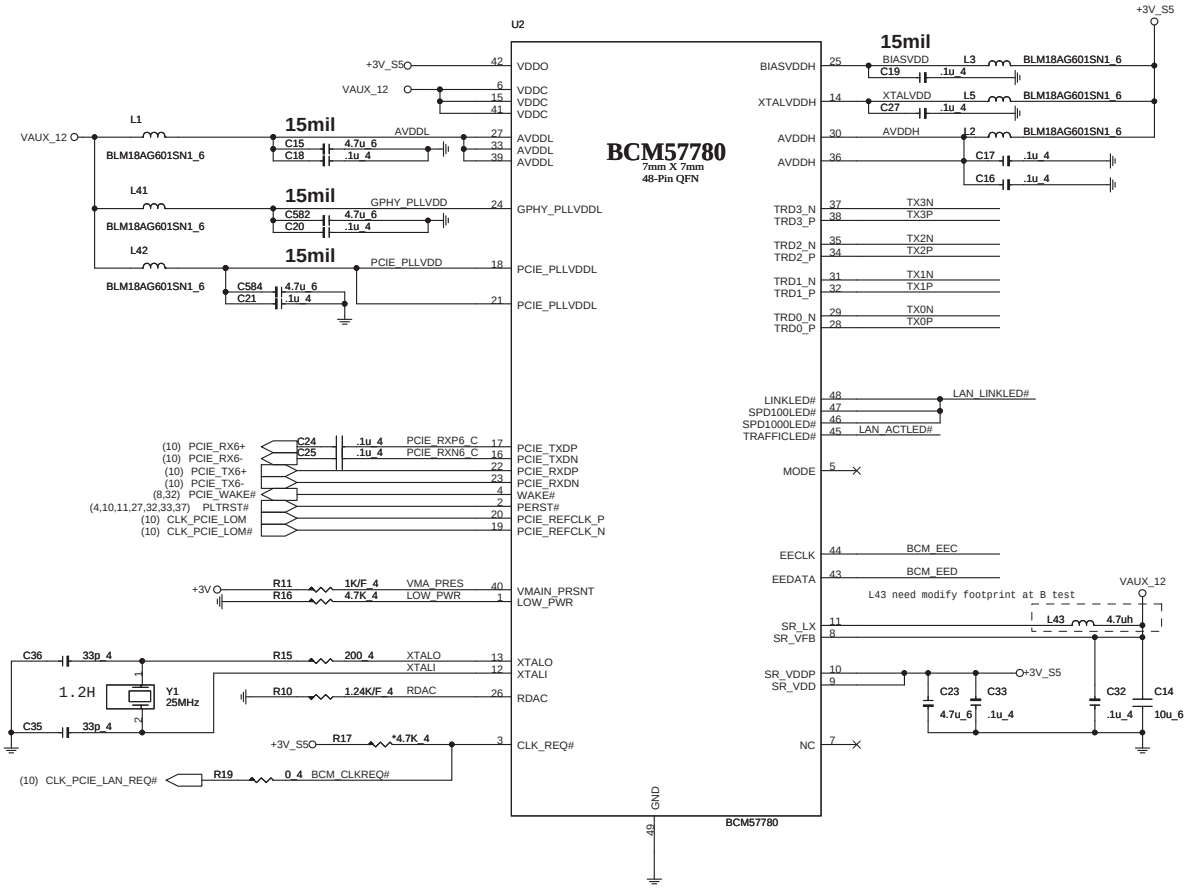
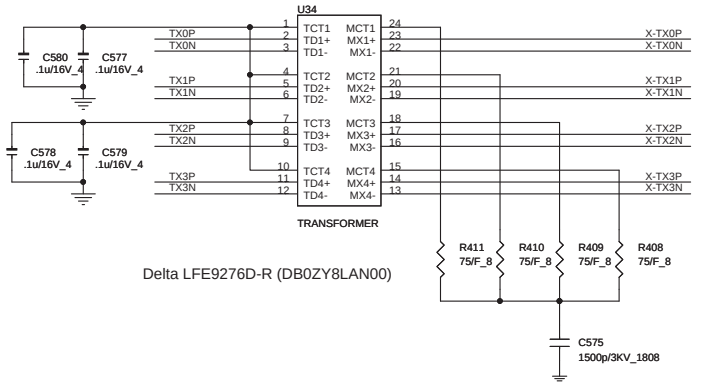
Giga-LAN BCM57780

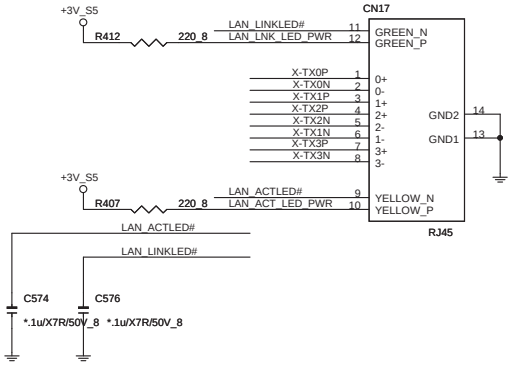


TRANSFORMER

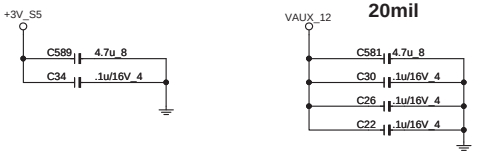


Delta LFE9276D-R (DB0ZY8LAN00)

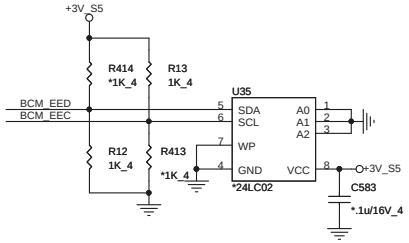
RJ45



LAN POWER



EEPROM



EEPROM Strapping

EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

Quanta Computer Inc.
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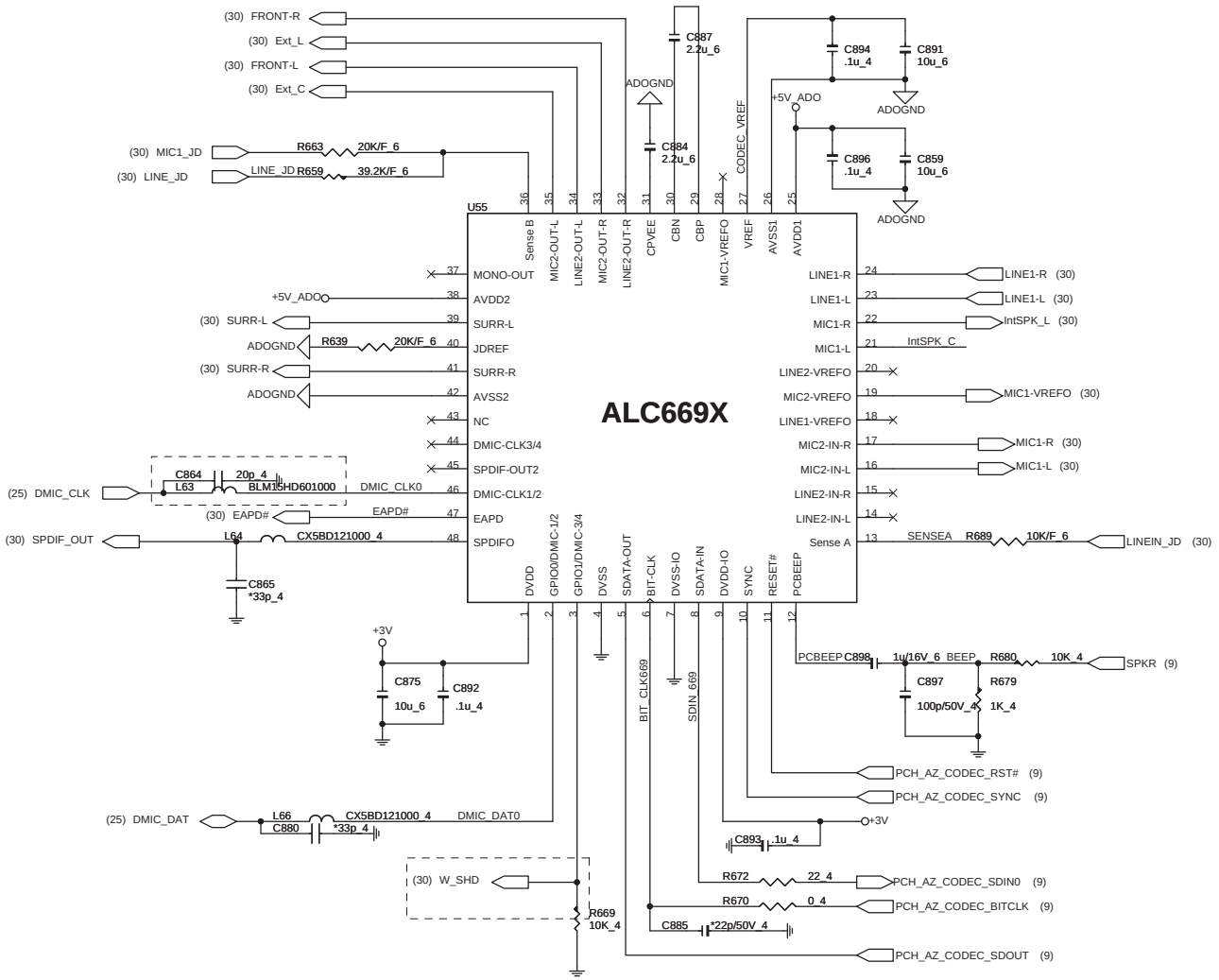
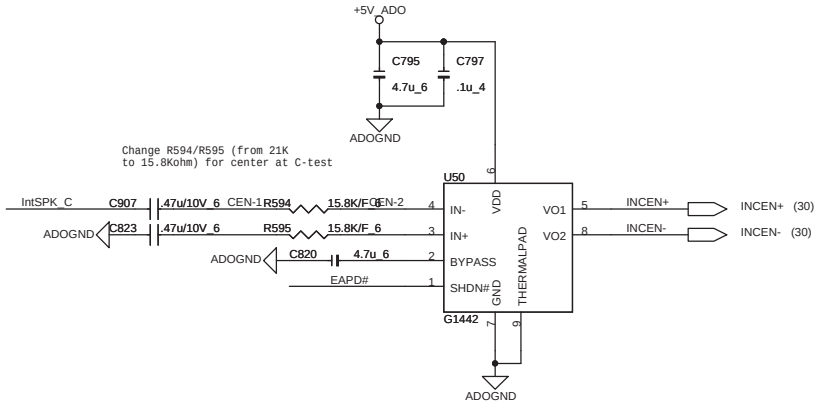
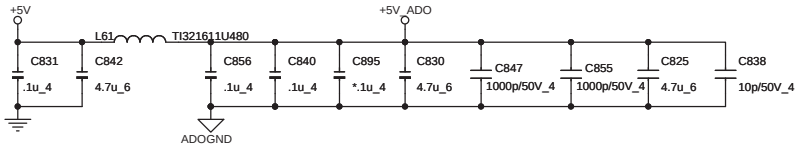
CODEC(ALC669X)



CENTER MONO



CODEC/AMP Power



Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	REALTEK ALC889X/MONO-AMP	1A
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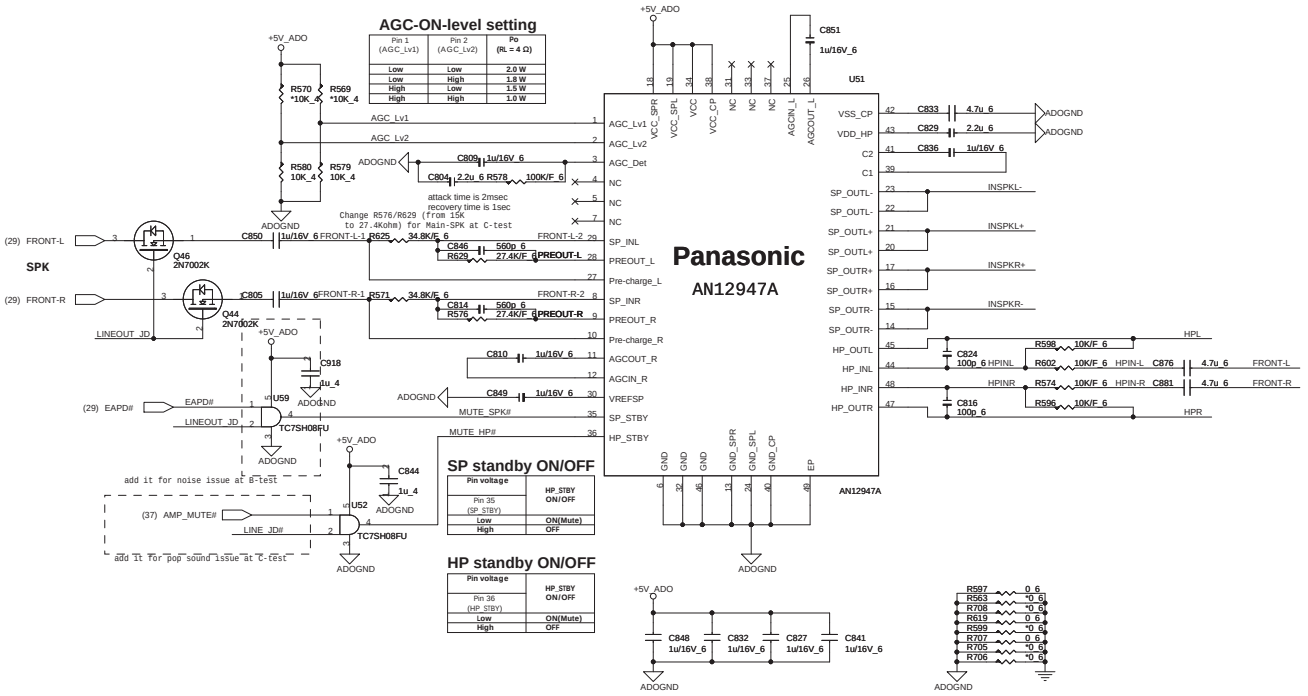
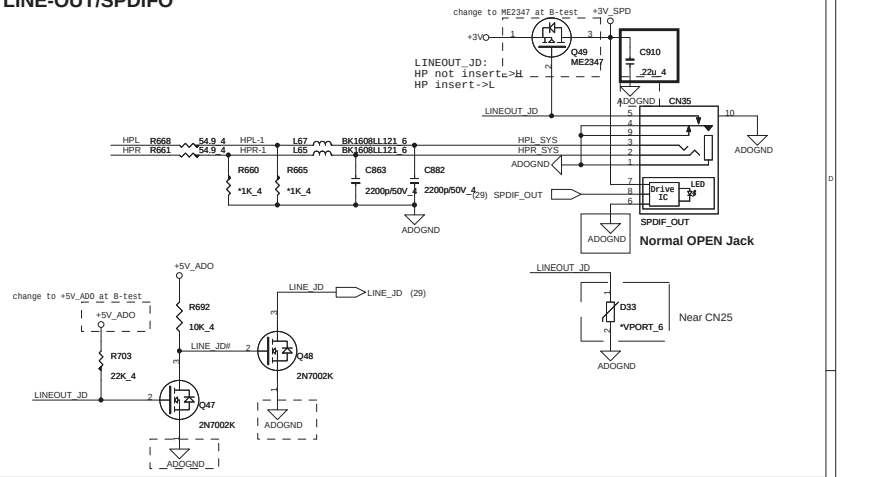
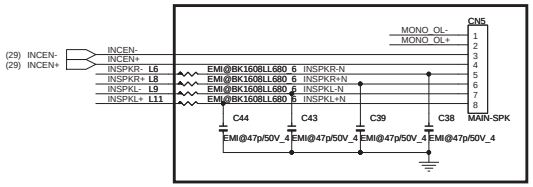
SPEAKER/HP AMP.



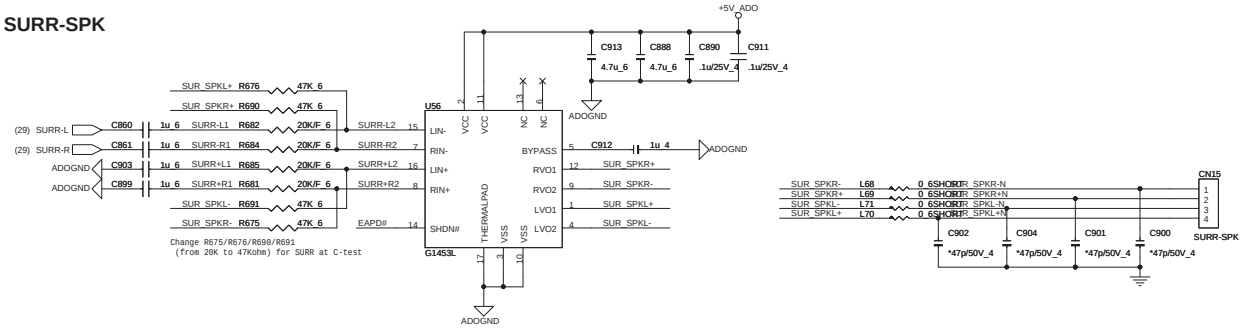
LINE-OUT/SPDIFO



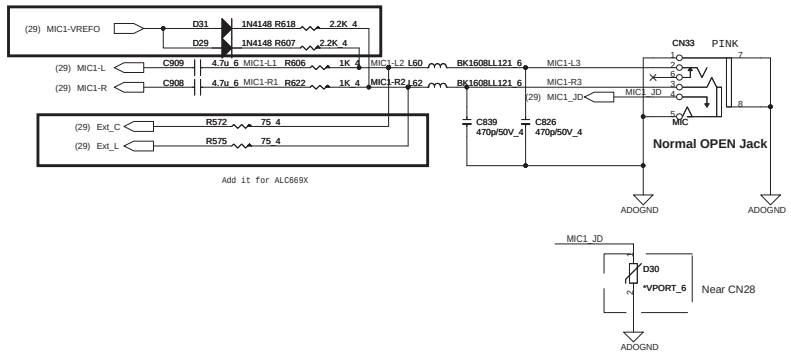
Main SPK/Center/Subwoofer EMI



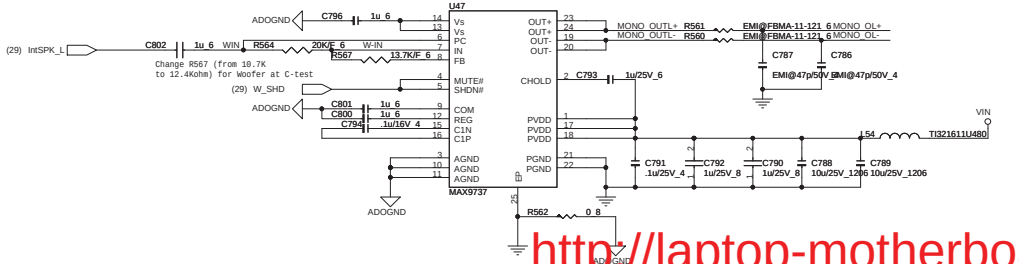
SURR-SPK



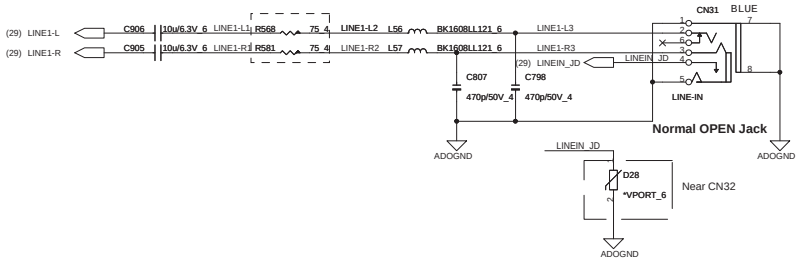
MIC



SUBWOOFER



LINE IN



Quanta Computer Inc.
PROJECT : ZY9B
AMP/AUDIO JACK/WOOFER
Rev 1A
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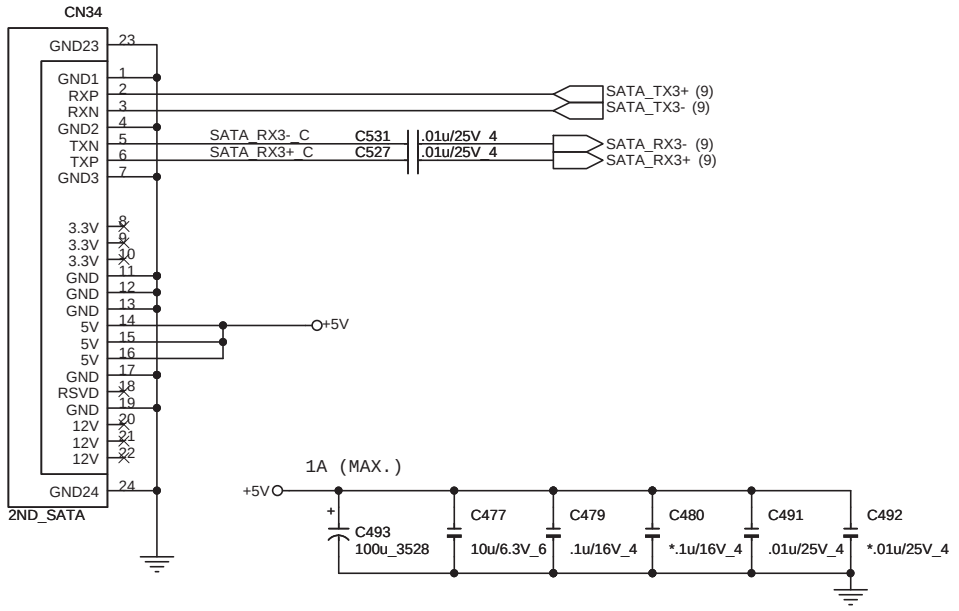
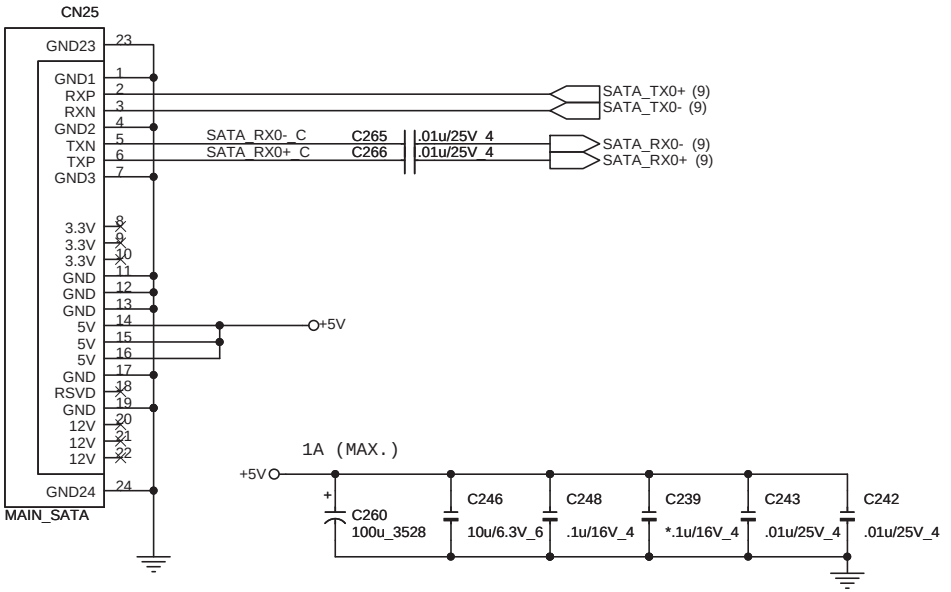
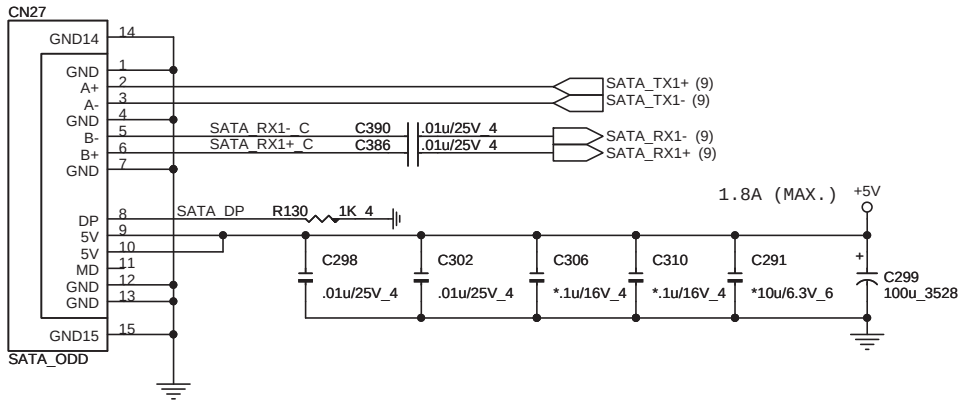
2nd SATA HDD (edge of board)



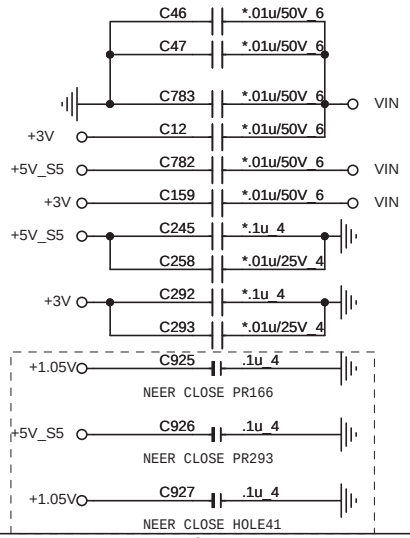
MAIN SATA HDD

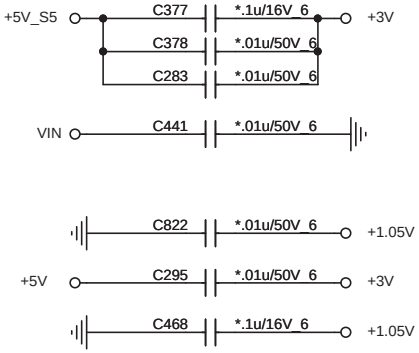


ODD (SATA)



EE RETURN-PATH CAPACITORS





Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	SATA-HDD/ODD	1A
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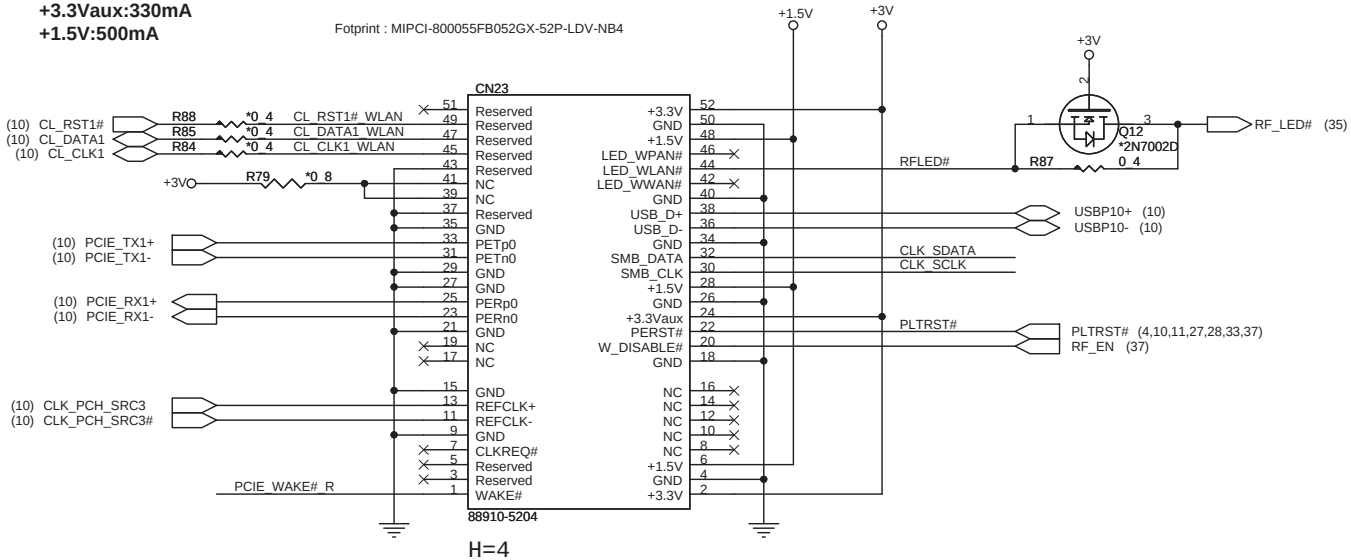
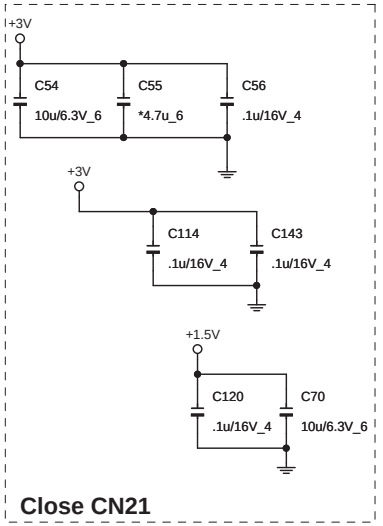
Wireless

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

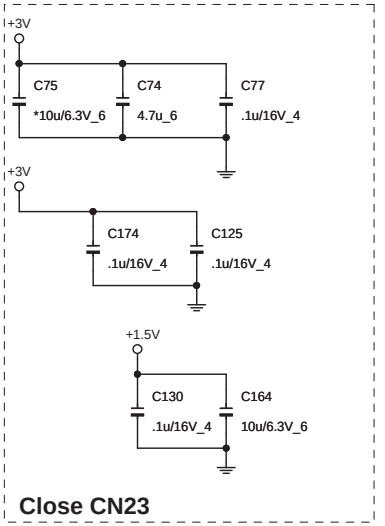
Fotprint : MIPCI-800055FB052GX-52P-LDV-NB4



H=4

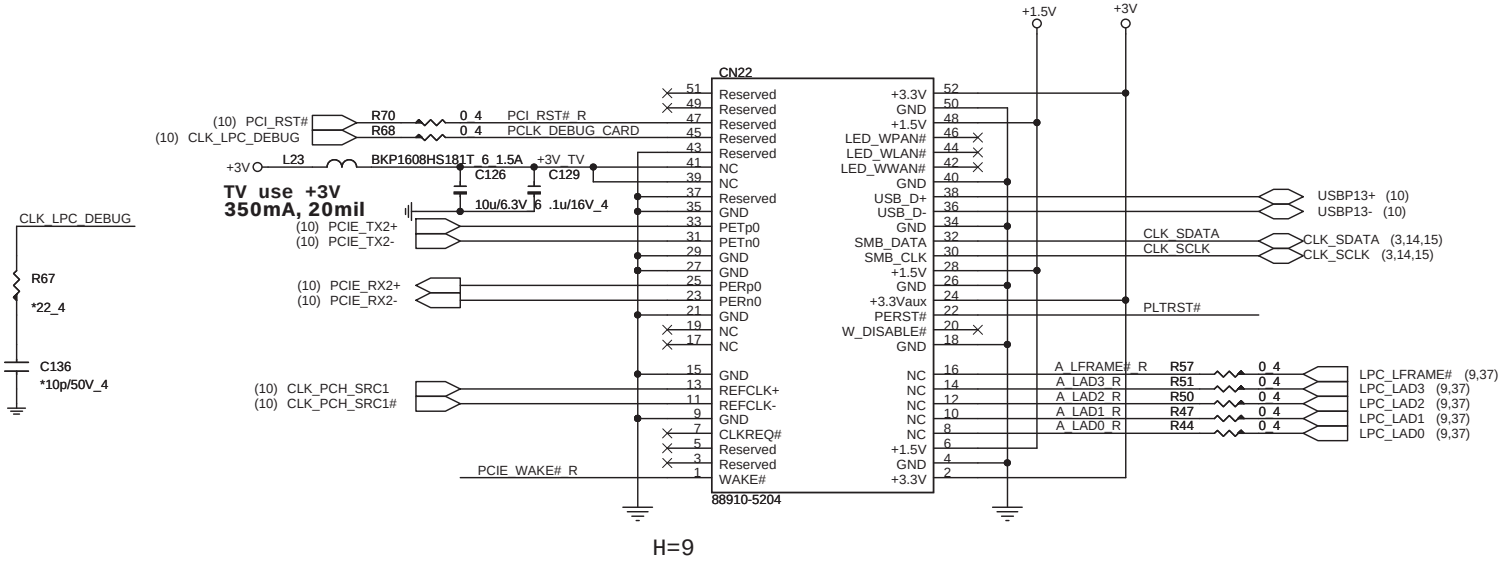


Close CN21

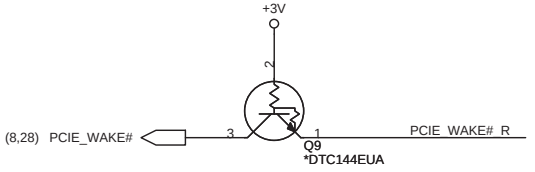


Close CN23

TV and Debug



H=9



Quanta Computer Inc.
PROJECT : ZY9B

Size	Document Number	Rev
	MINI PCI-E card/TV	1A
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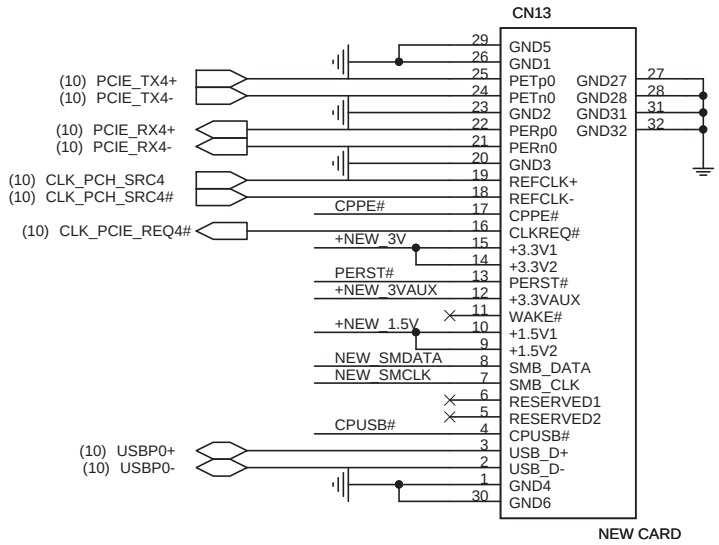
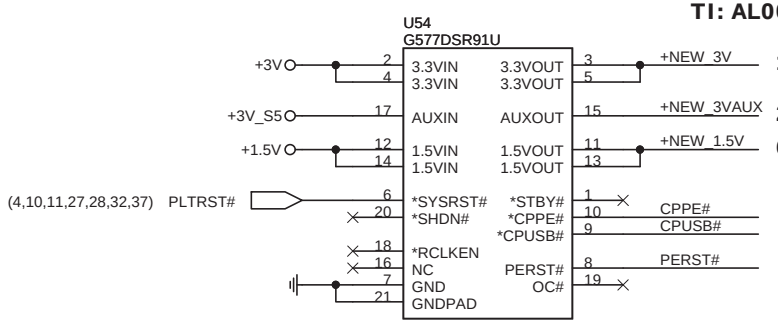
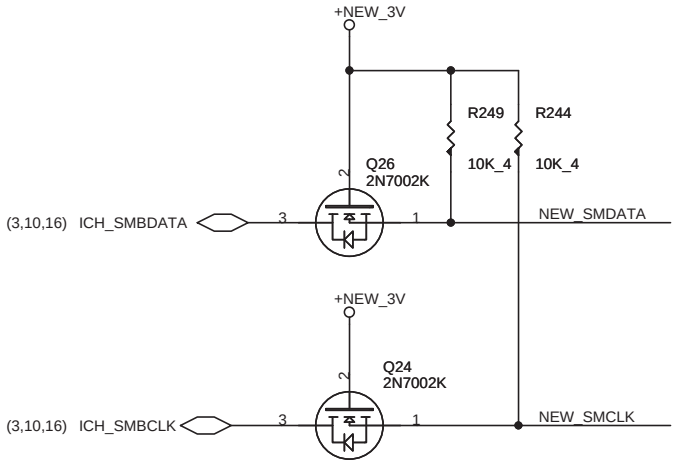
NEW CARD

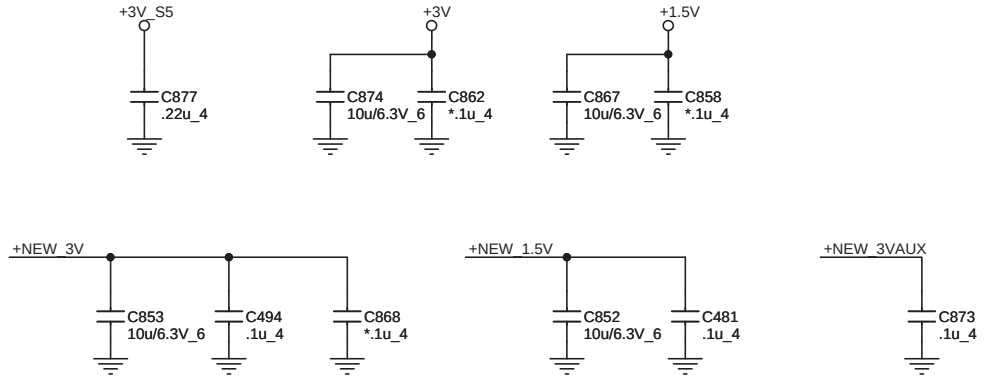


NEW CARD'S POWER SWITCH **GMT: AL000577002**

TI: AL002231000







Quanta Computer Inc.

PROJECT : ZY9B

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	NEW CARD	1A
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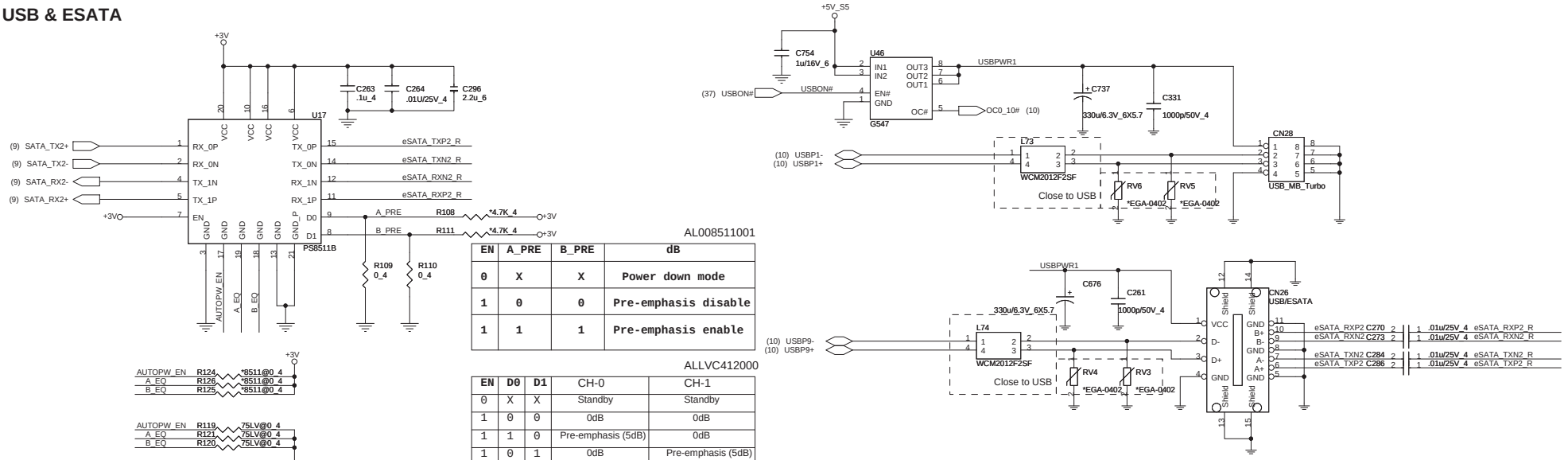
USB & ESATA



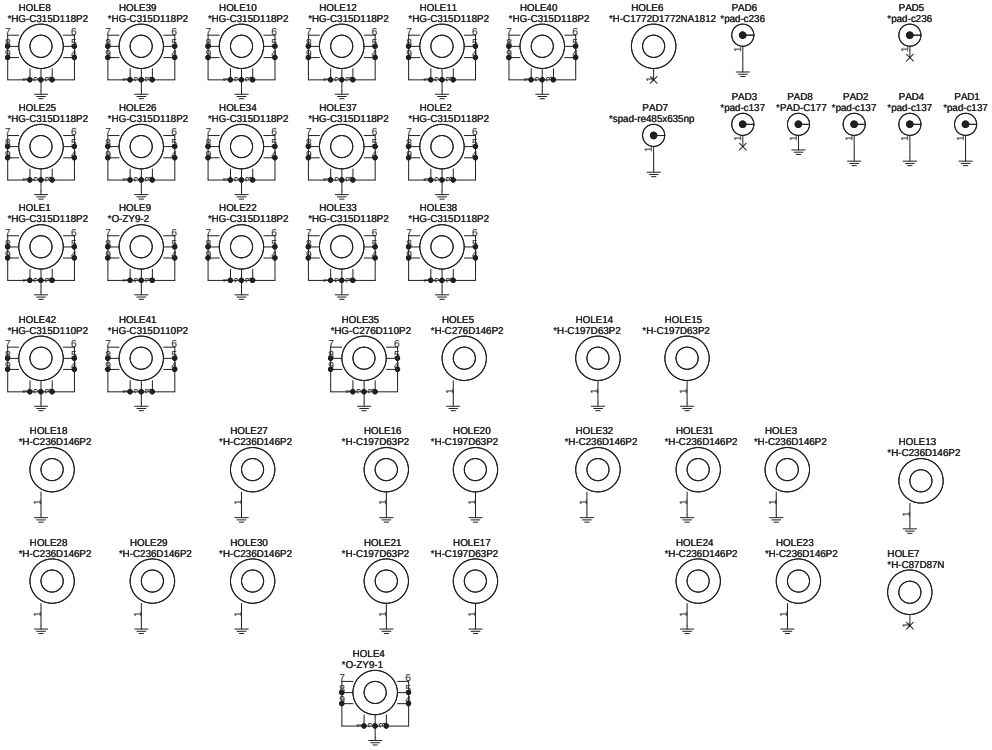
AL008511001

EN	A_PRE	B_PRE	dB
0	X	X	Power down mode
1	0	0	Pre-emphasis disable
1	1	1	Pre-emphasis enable

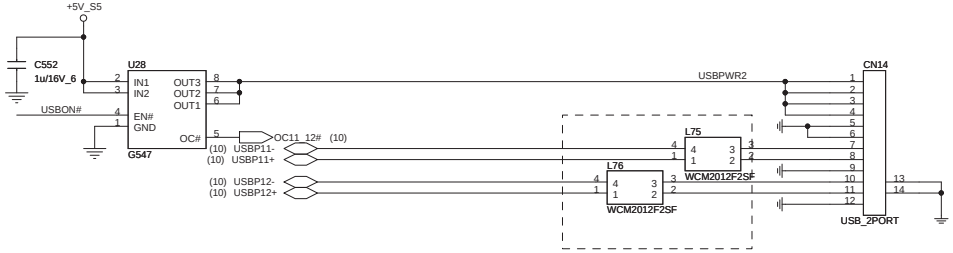
ALLVC412000

EN	D0	D1	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)

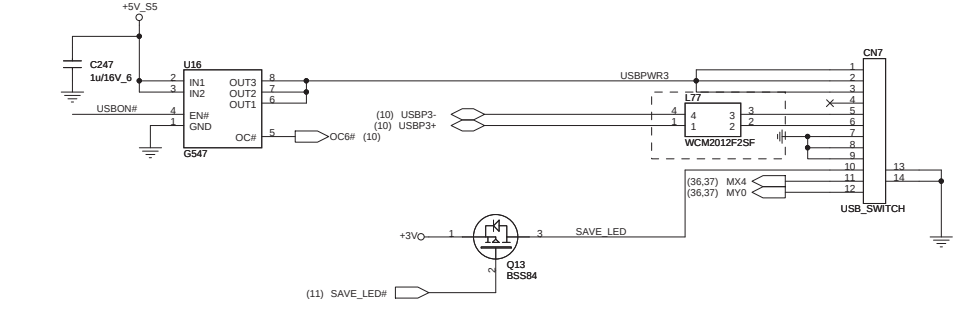
HOLES



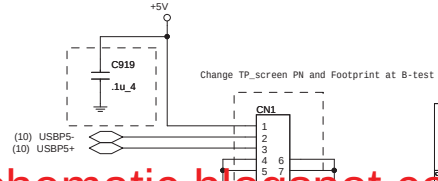
USB_2PORT/B



USB_SWITCH/B

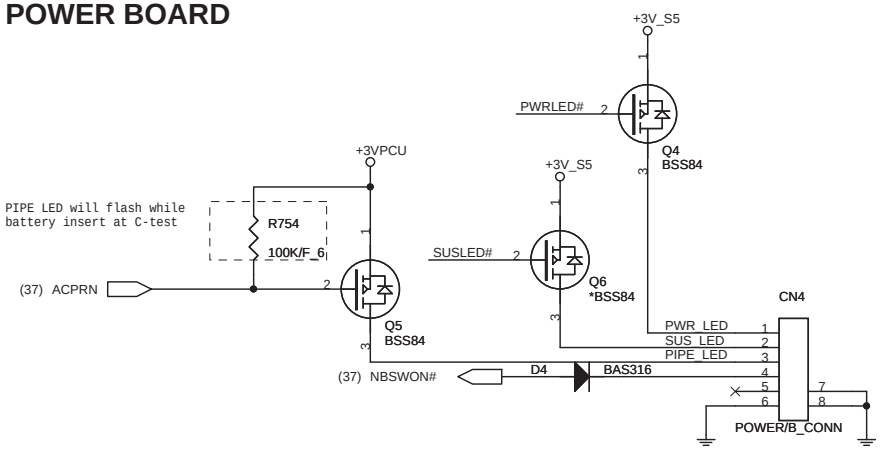


TP_Screen

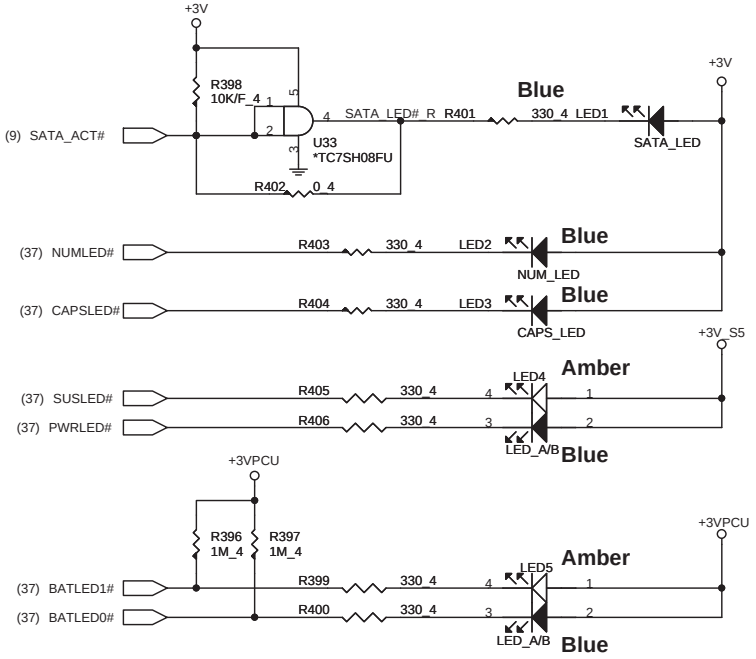


Quanta Computer Inc.
PROJECT : ZY9B
Size: | Document Number: USB/eSATA/TP_Screen | Rev: 1A
Date: Thursday, September 17, 2009 | Sheet 34 of 49

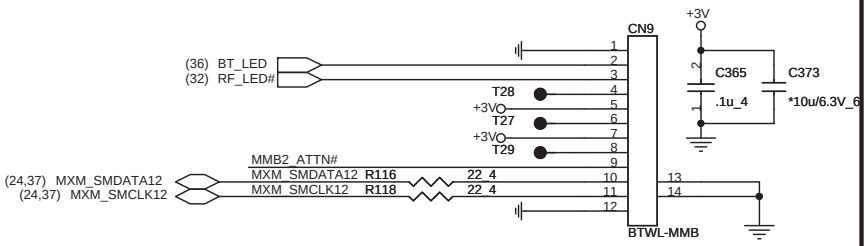
POWER BOARD



M/B LED

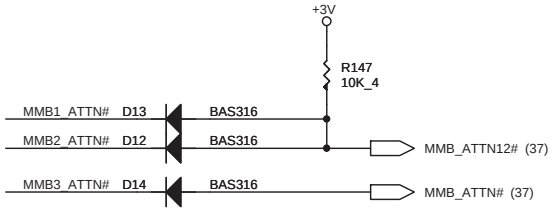


Left side MMB

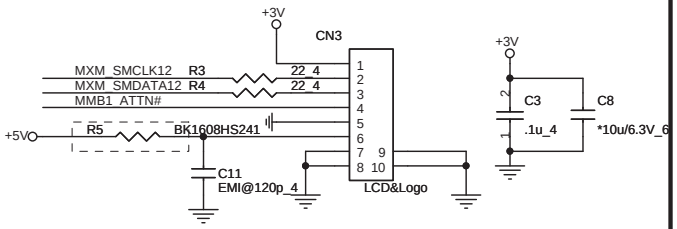


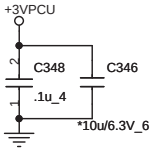
MXMCLK=MXM_SMCLK; MXMDATA=MXM_SMDATA12
MMB1 and MMB2 need add ISOLATE circuit where are on MXM page.

MMB Status

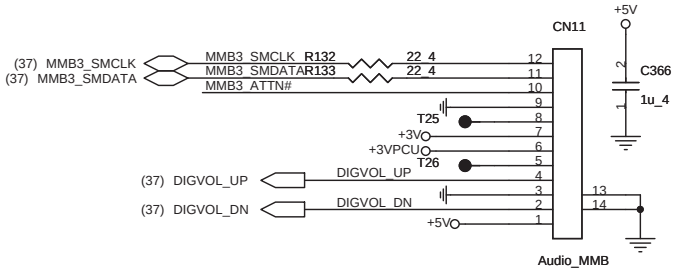


LCD BL_ON/OFF MMB & Backlight Logo LED



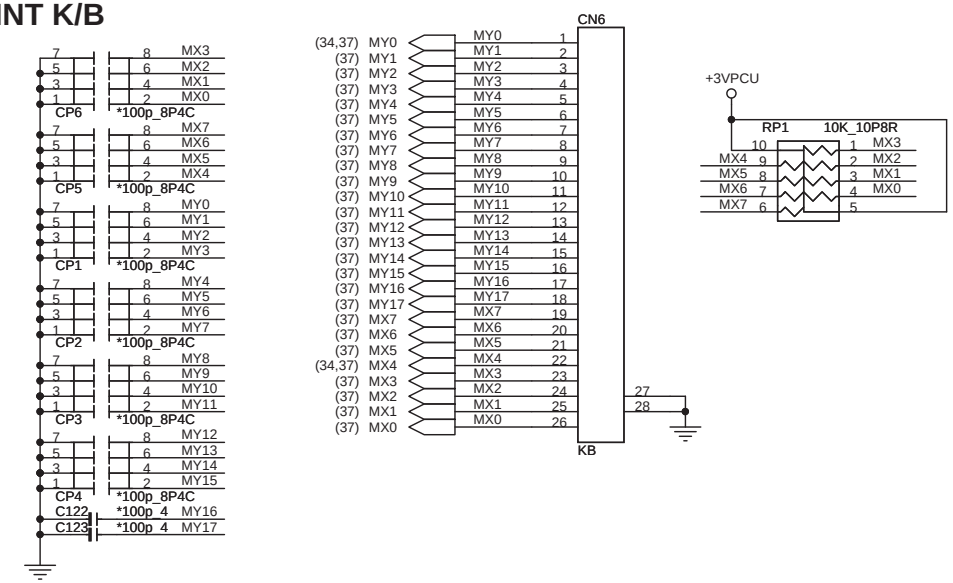


Right Side MMB

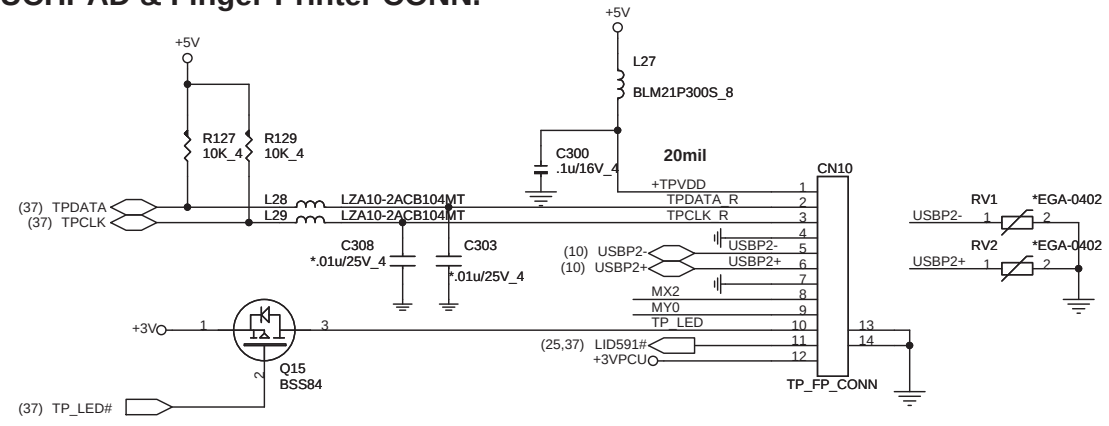


Quanta Computer Inc.		
PROJECT : ZY9B		
Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	1A
Date: Thursday, September 17, 2009	Sheet 35 of 49	

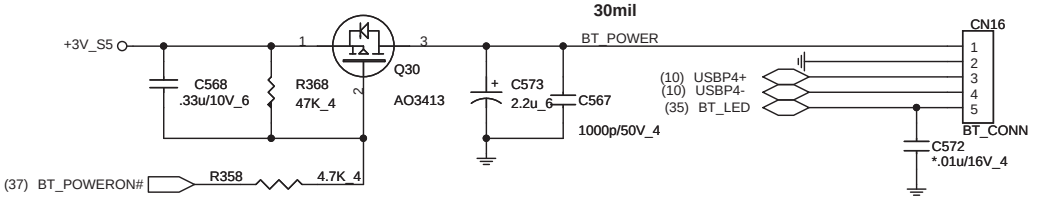
INT K/B



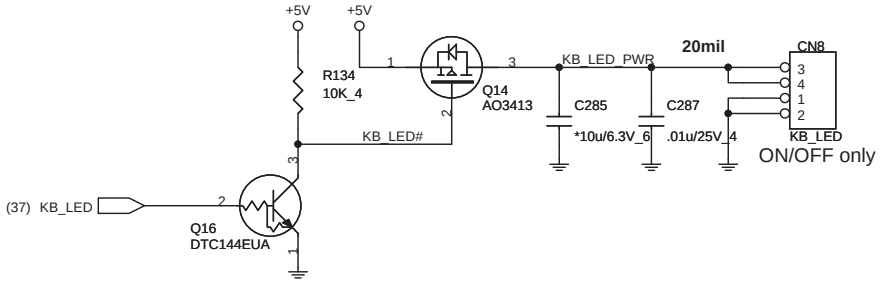
TOUCHPAD & Finger-Printer CONN.



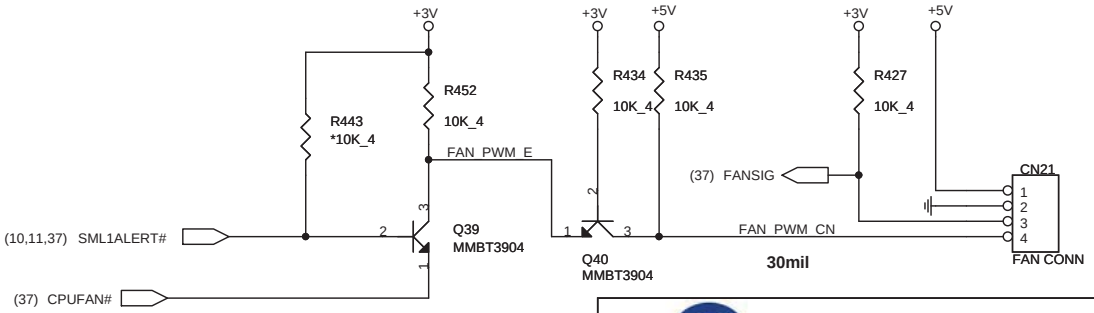
BLUETOOTH CONNECTOR



Keyboard LED control



CPU FAN



Quanta Computer Inc.		
PROJECT : ZY9B		
Size	Document Number: KB/FAN/TP+FP/BT	Rev: 1A
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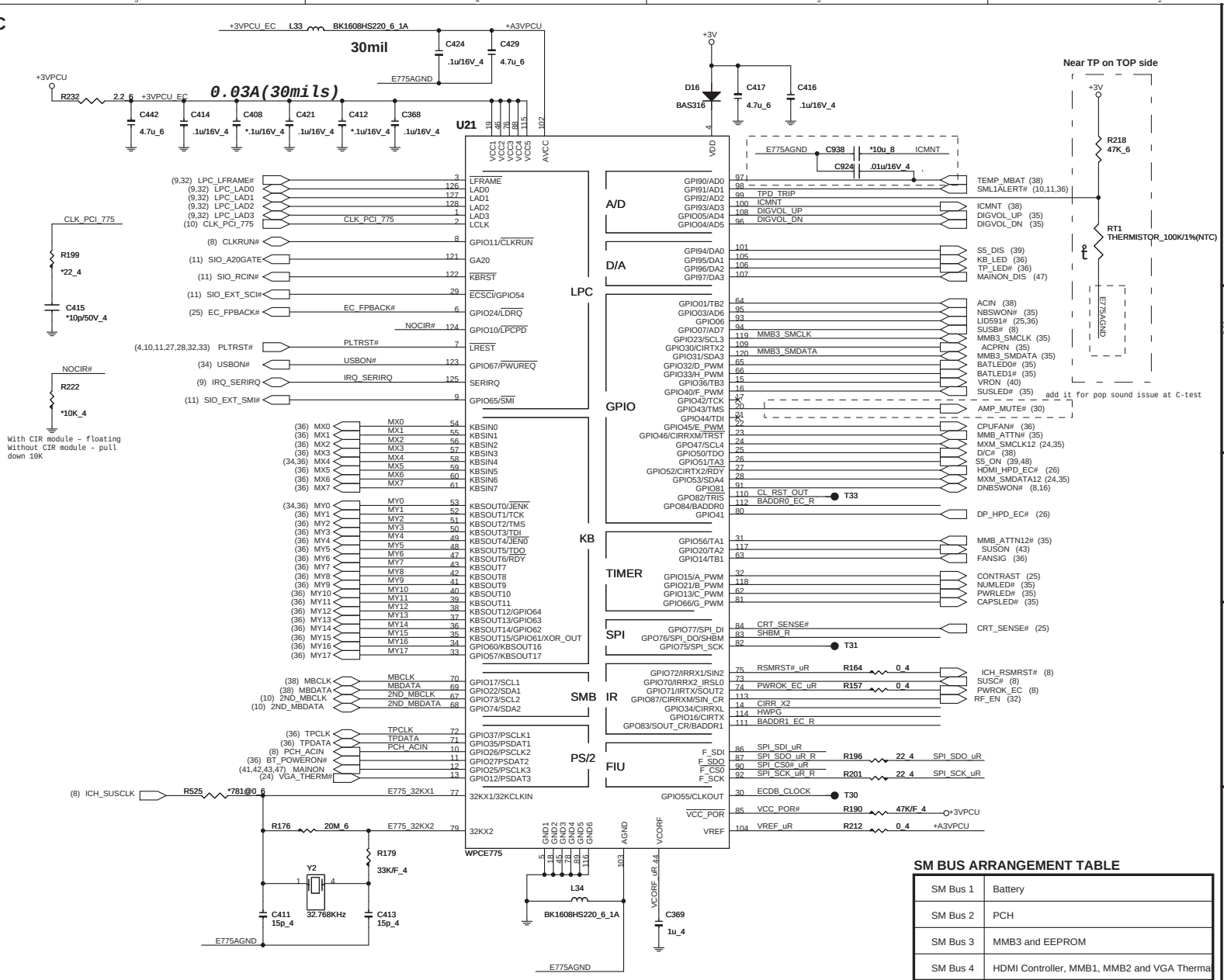
EC



I/O ADDRESS SETTING

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 — BADDR0_EC_R — R227 — 10K_4
BADDR1 — BADDR1_EC_R — R220 — *10K_4
SHBM — SHBM_R — R183 — 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

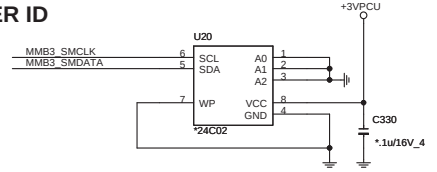
SM BUS PU

Change pull-up resistor (R148 /R154) from 10K to 4.7Kohm

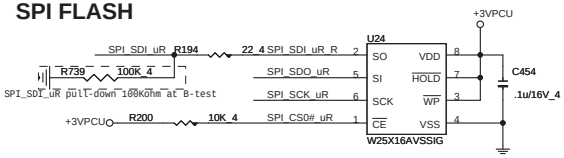
MBCLK — R154 — 4.7K_4
MBDATA — R148 — 4.7K_4
MMB3_SMCLK — R224 — 10K_4
MMB3_SMDATA — R213 — 10K_4

CRT_SENSE# — R189 — *10K_4
2ND_MBCLK — R140 — 10K_4
2ND_MBDATA — R144 — 10K_4
MXM_SMCLK12 — R169 — 2.2K_4
MXM_SMDATA12 — R170 — 2.2K_4

ACER ID



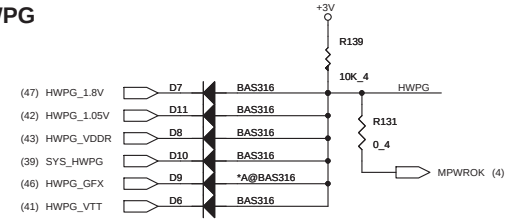
SPI FLASH



1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

At 11/24 add
Winbond W25X16AVSSIG AKE38ZP0N01
MXIC MX25L1605AM2C-15G AKE37FP0Z13
EON EN25F16-100HIP AKE38ZA0Q00
AMIC A25L016 AKE38ZN0800

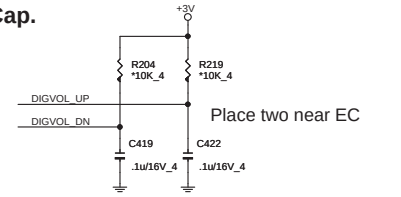
HWPG



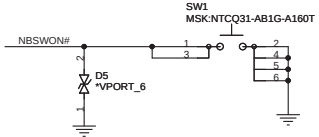
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	MMB3 and EEPROM
SM Bus 4	HDMI Controller, MMB1, MMB2 and VGA Therma

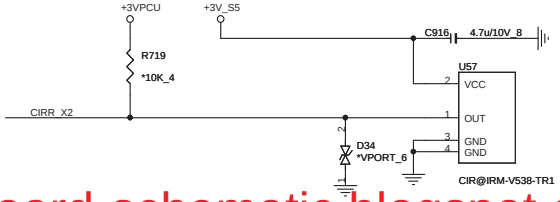
VR Cap.



POWER-ON Switch



CIR

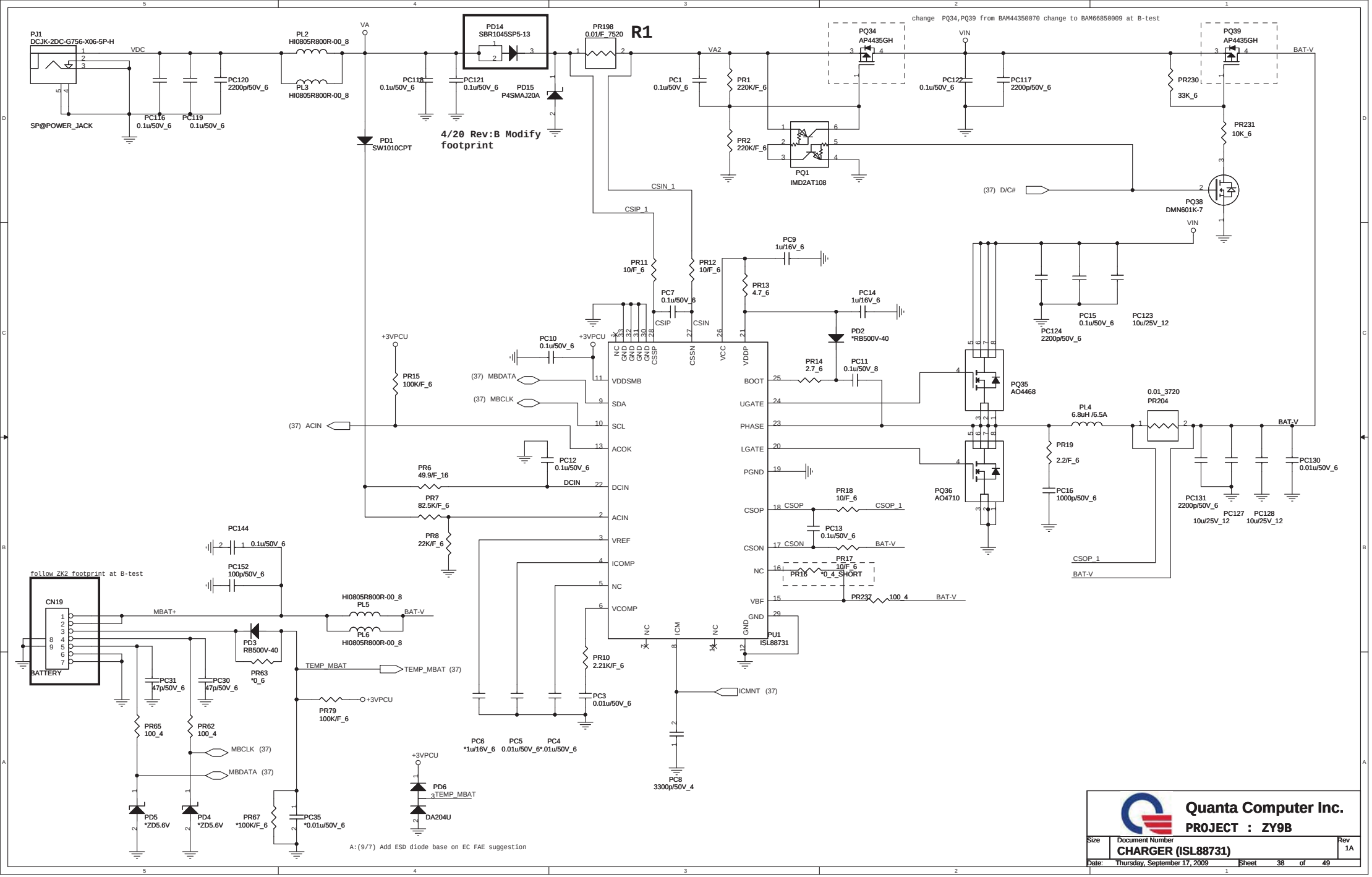


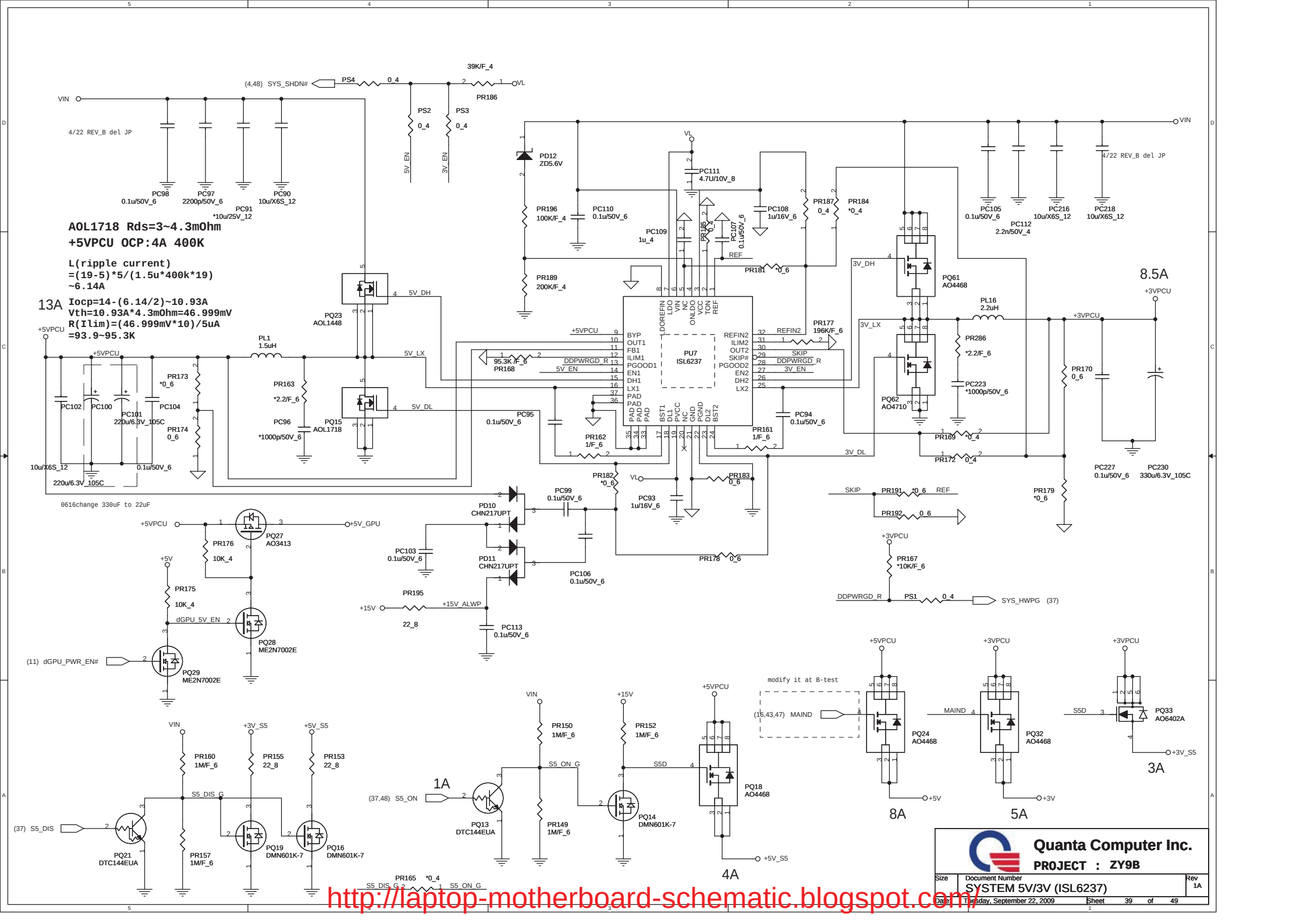
INTERNAL KEYBOARD STRIP SET

MY0 — R137 — 10K_4

Quanta Computer Inc.
PROJECT : ZY9B

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A
Date: Thursday, September 17, 2009	Sheet 37 of 49	




AOL1718 Rds=3~4.3mOhm
+5VPCU OCP:4A 400K
L(ripple current)
=(19-5)*5/(1.5u*400k*19)
~6.14A
13A Iocp=14-(6.14/2)~10.93A
Vth=10.93A*4.3mOhm=46.999mV
R(Ilim)=(46.999mV*10)/5uA
=93.9~95.3K
PU7 ISL6237
8.5A
1A
3A
8A
5A
4A
Quanta Computer Inc.
PROJECT : ZY9B
SYSTEM 5V/3V (ISL6237)
Rev 1A
Tuesday, September 22, 2009
Sheet 39 of 49
http://laptop-motherboard-schematic.blogspot.com/

[PWM]

VID 1.2875V

+3VPCU PR238 *0_4 H_VID0
PR236 *0_4 H_VID1
PR235 *0_4 H_VID2
PR234 *0_4 H_VID3
+3VPCU PR233 *0_4 H_VID4
PR232 *0_4 H_VID5
PR228 *0_4 H_VID6

VR_PWRGD_CK505# (3)
DELAY_VR_PWRGOOD (4,8)

VIN
PR87 0_6
PR78 1.91K/F_4
PR225 1.91K/F_4
5/12 Change pr144 from 10K to 1.91K
+5V_S5
PR86 10_6
PC160 .22u/25V_6
PR210 0_8
PC157 1U/6.3V_4
+3V
PR217 *499/F_4
(6) H_PSI#
PSI# PR223 10K/F_4
PR221 147K/F_6
(4) H_PROCHOT#
Close to Phase 1 Inductor
PR245 *470K_4 NTC
PR50 *4.02K/F_4
PC135 *0.01u/16V_4

PU8
ISL62882
VDD VIN CLK_EN# PGOOD
PAD
UGATE1
BOOT1
PHASE1
LGATE1a
LGATE1b
VSSP1
ISEN1
VCCP
UGATE2
BOOT2
PHASE2
LGATE2
VSSP2
ISEN2
IMON
PSI# RBIAS VR_TT# NTC
VID0 VID1 VID2 VID3 VID4 VID5 VID6
VR_ON DPRSLPVR
FB FB2 COMP VW
VSEN RTN ISUM- ISUM+

(6) H_VID0 H_VID0
(6) H_VID1 H_VID1
(6) H_VID2 H_VID2
(6) H_VID3 H_VID3
(6) H_VID4 H_VID4
(6) H_VID5 H_VID5
(6) H_VID6 H_VID6
(37) VRON VR_ON
(6) H_DPRSLPVR DPRSLPVR
PR82 100K/F_4
PR80 499/F_4

PR46 *10K/F_4
PC138 22P_4
PR60 412K/F_4
PC29 150P/50V_4
PC137 10P/50V_4
PR211 8.06K/F_4
PC136 1000P/50V_4
5/12 Change pr24 rom 2.87K to 2.8K
PR52 2.8K/F_4
PR51 562/F_4
PC27 390P/50V_4

PC140 0.22U/10V_4 VSUM-
contact PC140 2nd pin to VSUM- at B-test
PR91 *0_4_SHORT +5V_S5
PC165 1U/6.3V_4
PC55 1U/6.3V_4
PC139 0.22U/10V_4 VSUM-
contact PC140 2nd pin to VSUM- at B-test
PR89 8.25K/F_4
PC161 0.22U/10V_4
I_MON (6)
VSSSENSE (6)
5/12 Change pc92 rom 0.33u_4 to 0.22u_6
5/12 stuff pc26 0.068u_6

PR239 2.2_6
PC162 .22u/25V_6
PR240 2.2_6
PC163 .22u/25V_6

PC153 0.22u/10V/X7R_6
PC43 0.068u/25V/X7R_6
VSUM+
PR229 82.5/F_4
PC151
PC147 .01U/16V_4
2700P/50V_4
PR76 0_4
PR227 11K/F_4
PR75 2.61K/F_4
PR243 10K_6_NTC
Panasonic
ERT-J1VR103J
5/12 Change pr34 rom 1K to 1.24K
PR64 1.24K/F_4
PC41 .1u_4
Close to Phase 1 Inductor
PC145 *1000P/50V_4
PR224 *100/F_4
Load Line setting to 2mV/A
5/12 un-stuff PC76,PR140

+VCC_CORE
PR53 *27.4_4
PC148 330P/50V_4
PC149 330P/50V_4
PC142 1000P/50V_4
PR218 *27.4_4
(6) VCCSENSE PR73 0_4
(6) VSSSENSE PR74 0_4
Parallel

PC166 0.1u/50V_6
PC170 10u/X6S_12
PC167 10u/X6S_12
PC159 100U/25V L-F
PQ43 AOL1448
PQ46 AOL1718
PQ51 AOL1718
PR241 2.2/F_6
PC171 1000p/50V_6
PL10 0.36uH
PR99 0_4
PR103 0_4
PC179 330u/2V
+VCC_CORE

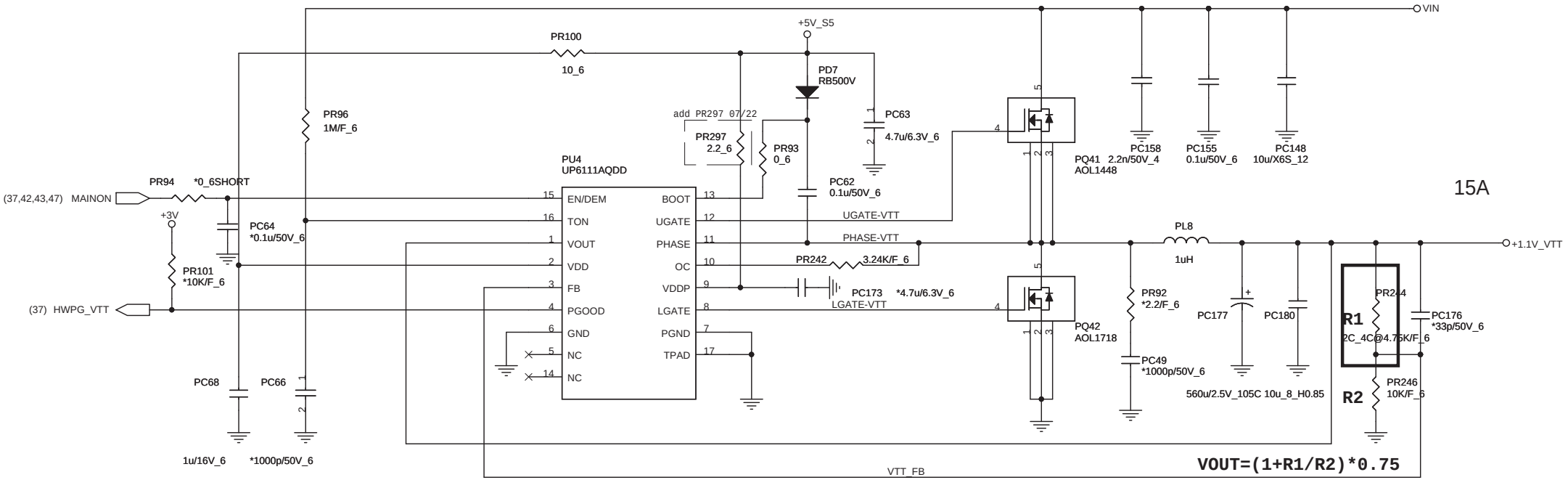
PR57 10K/F_4
VSUM+ PR56 3.65K/F_4
VSUM- PR219 1/F_4
PR212 10K/F_4

PC164 0.1u/50V_6
PC172 10u/X6S_12
PC169 10u/X6S_12
PC154 *100U/25V L-F
modify correct PC154 footprint at B-test
PQ44 AOL1448
PQ47 AOL1718
PQ52 AOL1718
PR95 2.2/F_6
PC65 1000p/50V_6
PL9 0.36uH
PR97 0_4
PR102 0_4
PC178 330u/2V
+VCC_CORE

PR54 10K/F_4
VSUM+ PR55 3.65K/F_4
VSUM- PR220 1/F_4
PR213 10K/F_4

Quanta Computer Inc.
PROJECT : ZY9B
Size Document Number CPU Core (ISL62882) Rev 1A
Date: Thursday, September 17, 2009 Sheet 40 of 49

[PWM]



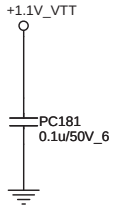
5/4
PR157 change to 4.75K

AO1718 Rdson=3~4.3mOhm

BOM change notice
Arrandale (1.05V) R1 = 4.02K (CS24023F928)
Clarksfield(1.1V) R1 = 4.75K (CS24753F919)

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.64A

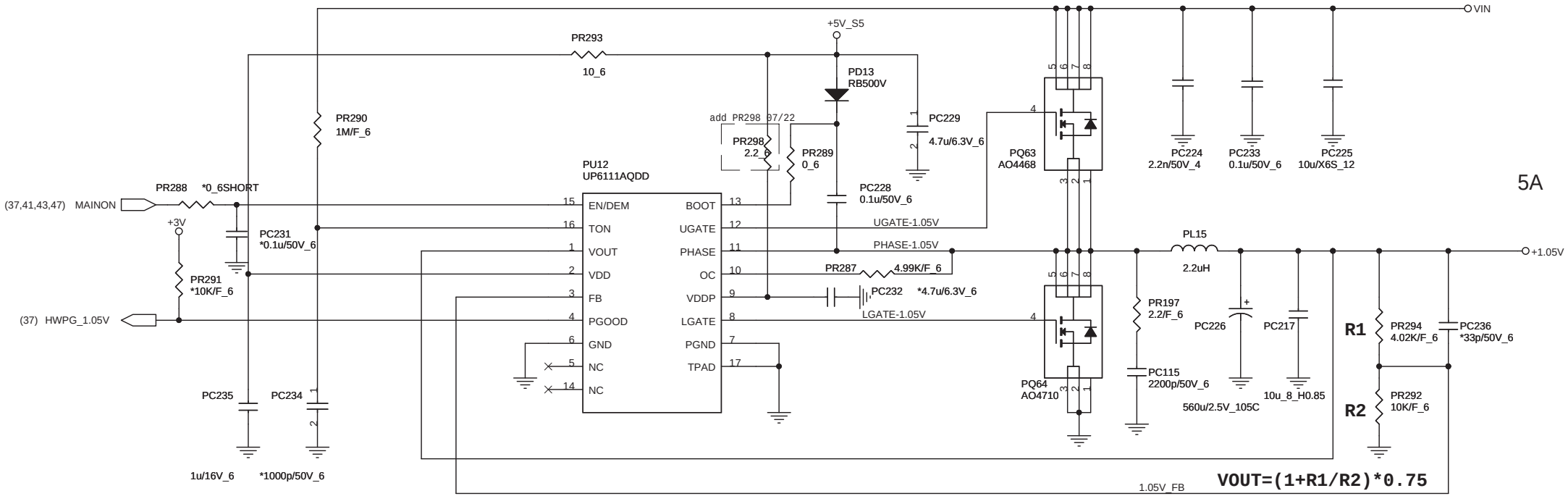
4.3m*15=RILIM*20uA
RILIM=3.24K(3.22K)



Quanta Computer Inc.
PROJECT : ZY9B

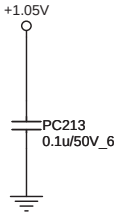
Size	Document Number	Rev
	+VTT (UP6111A)	1A
Date: Thursday, September 17, 2009	Sheet 41 of 49	

[PWM]



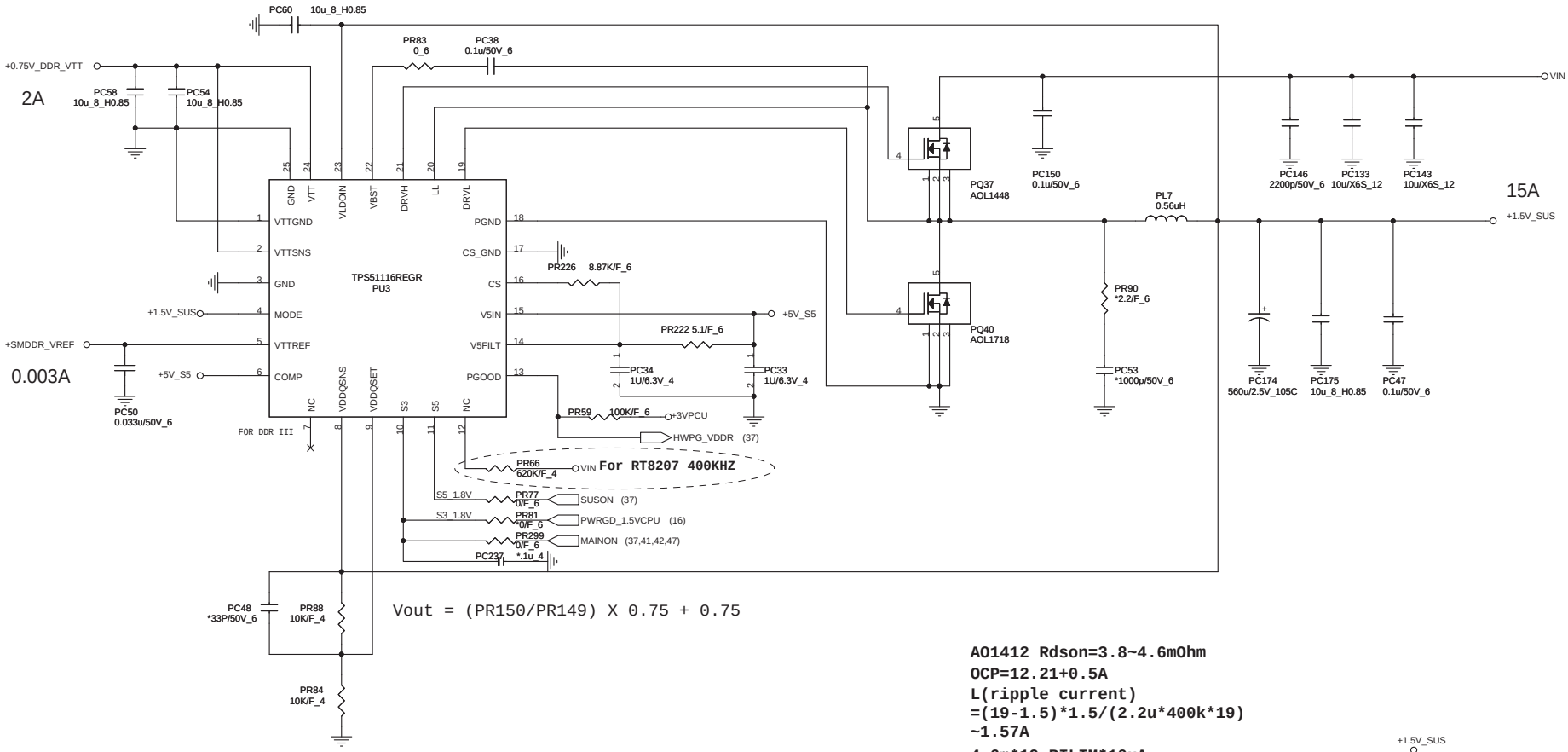
AO4710 Rdson=11.8~14.2mOhm
OCP=7.2-0.8A
L(ripple current)
=(19-1.05)*1.05/(2.2u*272k*19)
~1.6577A

14.2m*7=RILIM*20uA
RILIM=4.99K(4.97K)



Quanta Computer Inc.		
PROJECT : ZY9B		
Size	Document Number: +1.05V(UP6111AQDD)	Rev: 1A
Date: Monday, September 21, 2009	Sheet 42 of 49	

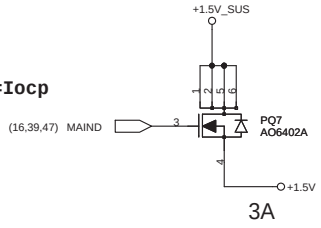
[PWM]

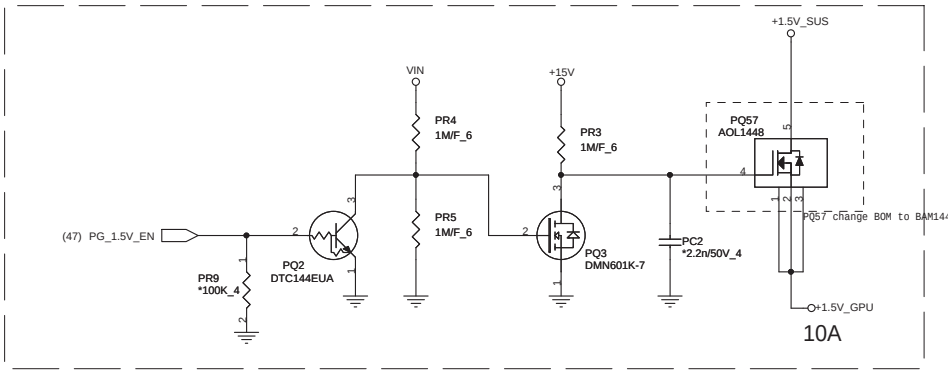


Vout = (PR150/PR149) X 0.75 + 0.75

AO1412 Rdson=3.8~4.6mOhm
OCP=12.21+0.5A
L(ripple current)
=(19-1.5)*1.5/(2.2u*400k*19)
~1.57A
4.6m*19=RILIM*10uA
RILIM=8.74K --- 8.87K

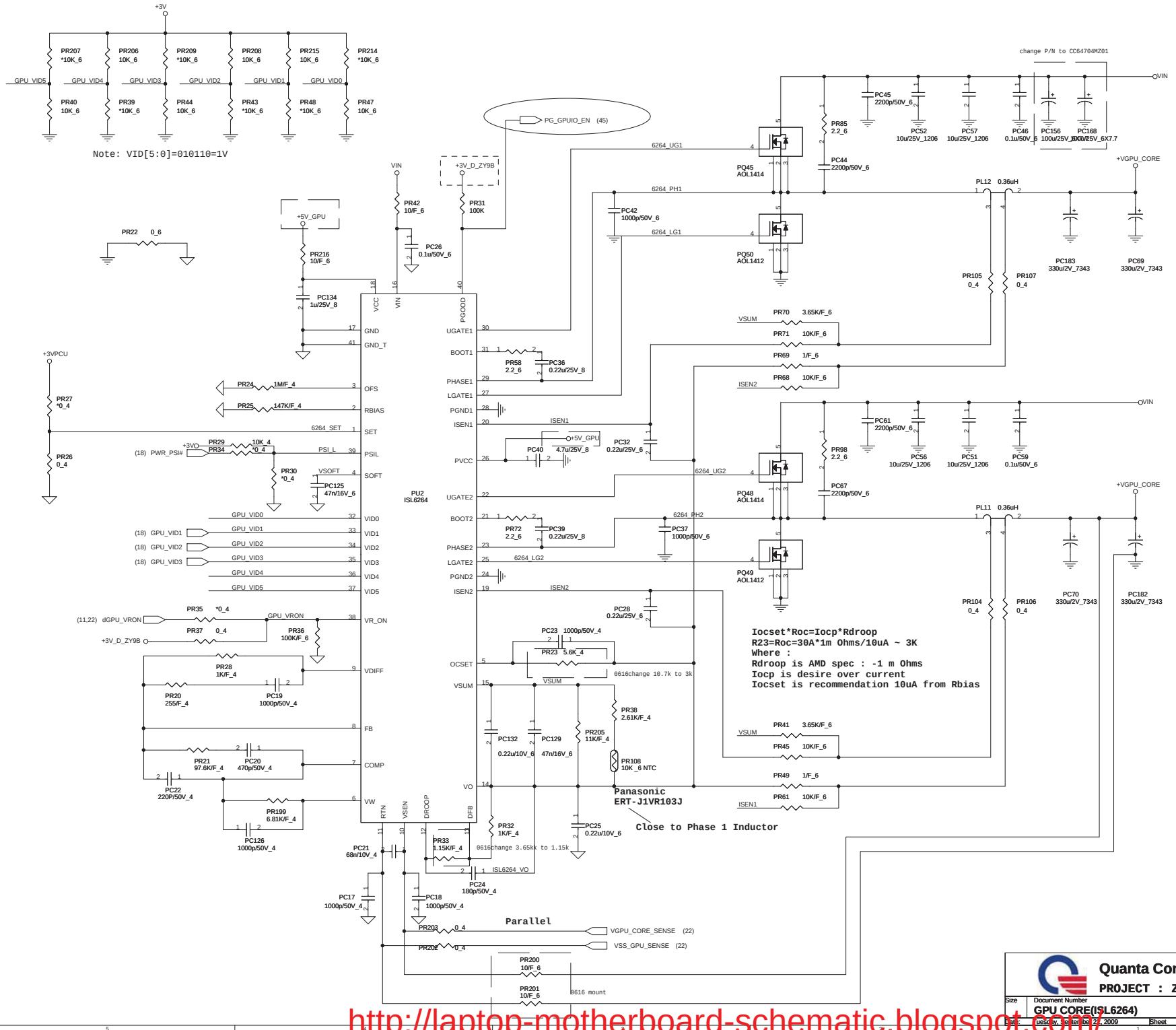
(10u*PR35)/Rdson+Delta_I/2=Iocp

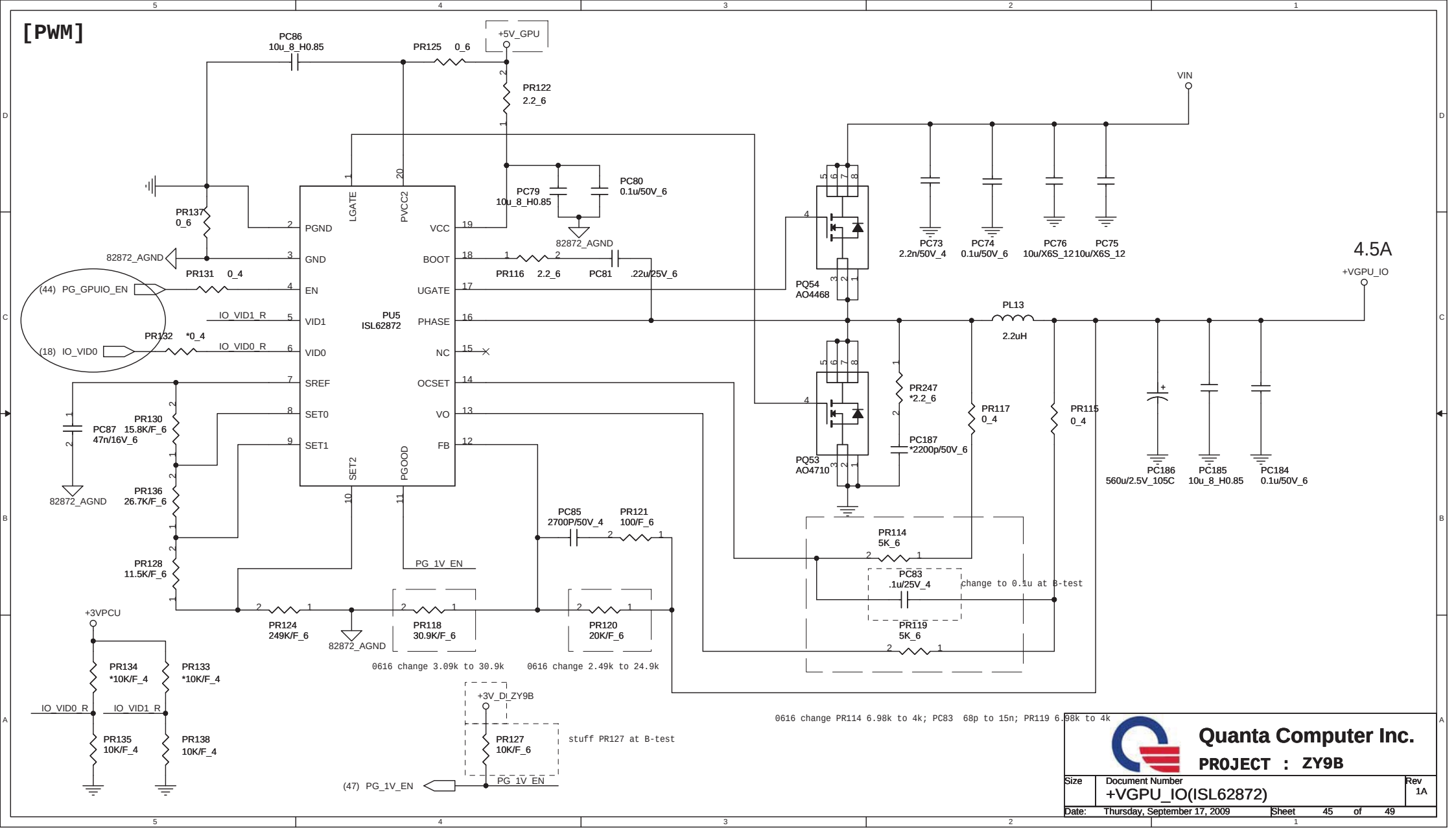




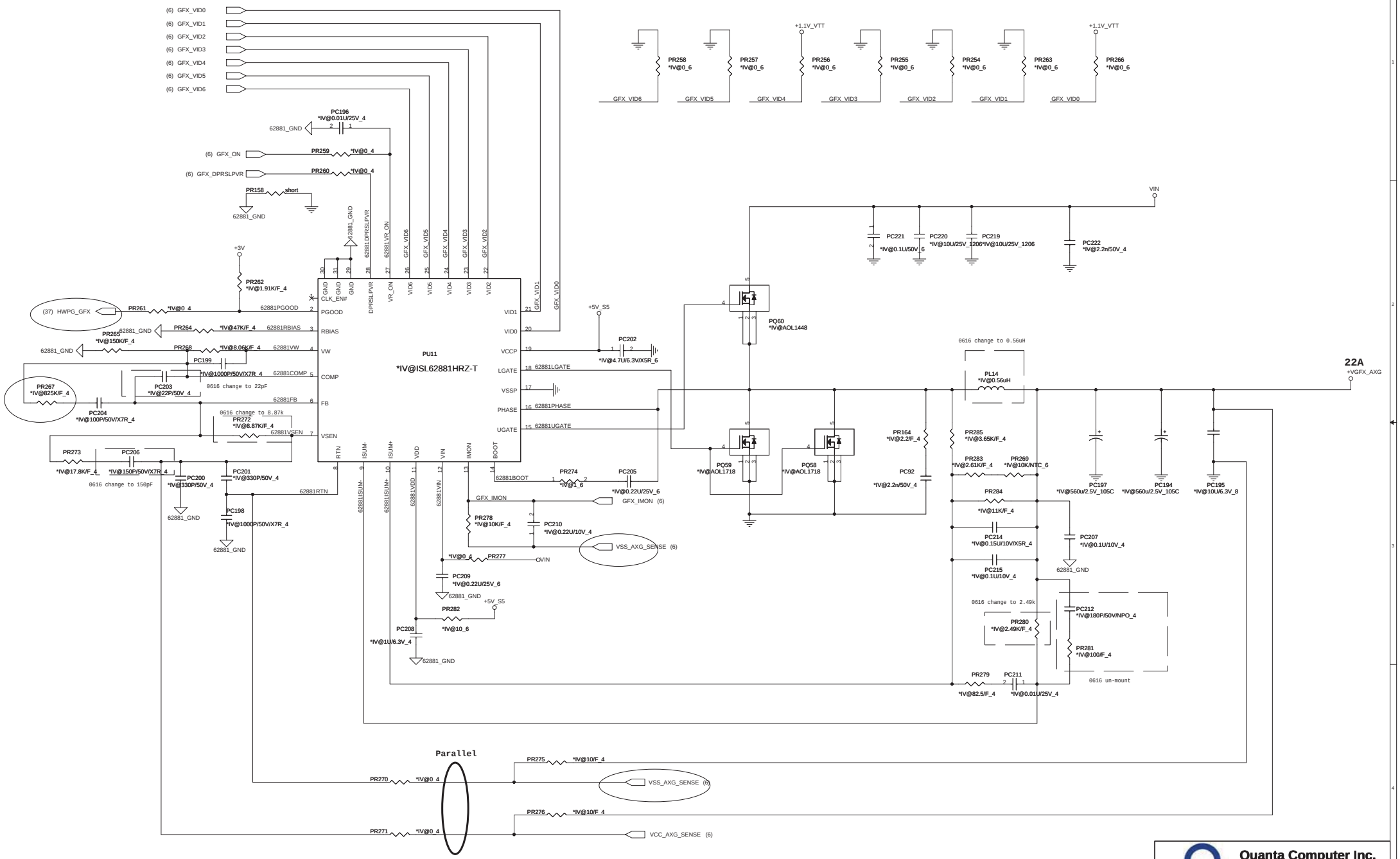
Quanta Computer Inc.
PROJECT : ZY9B

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A
Date: Thursday, September 17, 2009	Sheet 43 of 49	





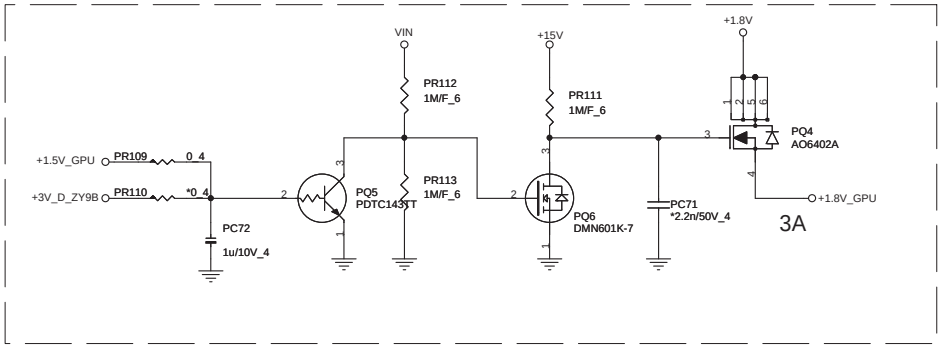
Int_VGA [PWM]

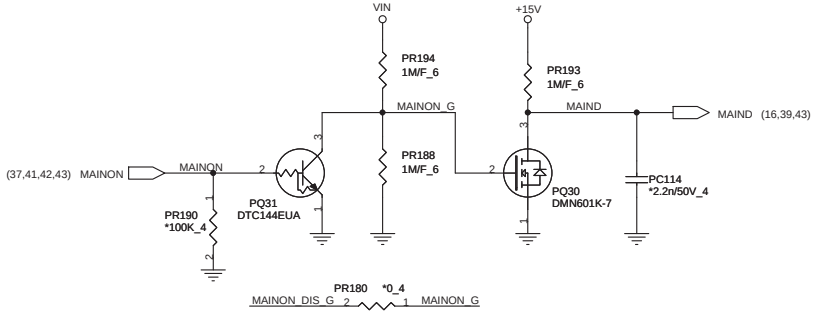


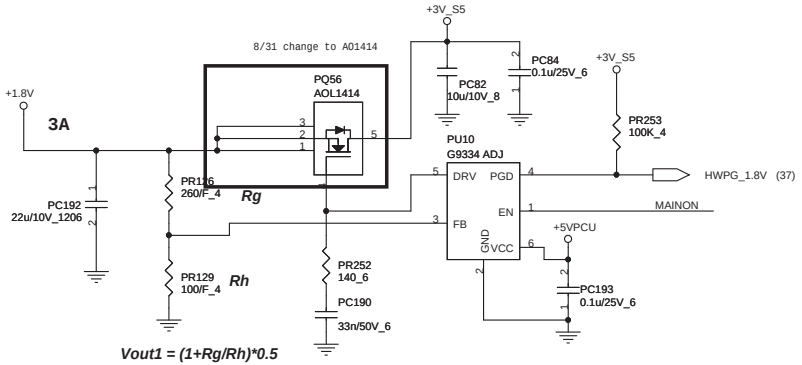
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

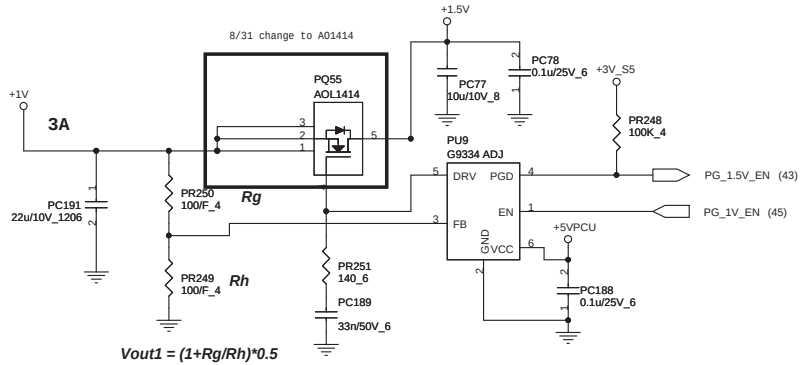
Quanta Computer Inc.		
PROJECT : ZY9B		
Size	Document Number: +VGFX_AXG (ISL62881)	Rev: 1A
Date: Tuesday, September 22, 2009	Sheet 46 of 49	

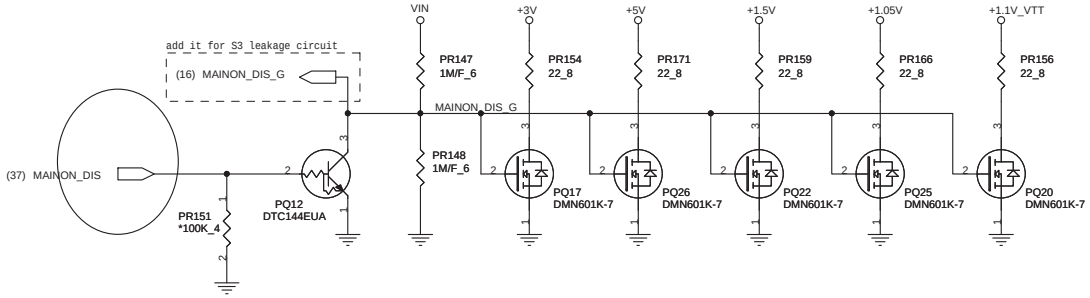
[PWM]







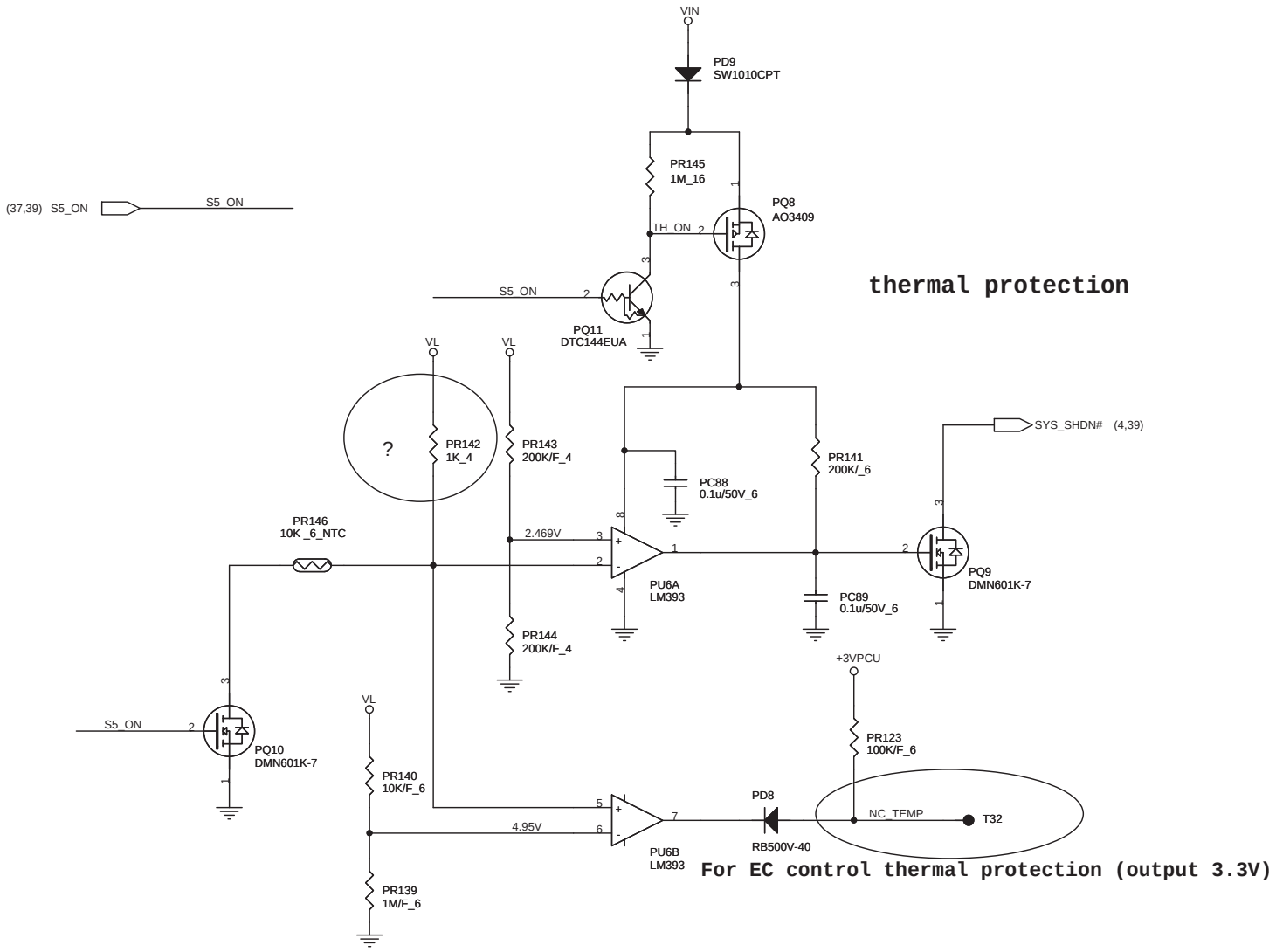




Quanta Computer Inc.
PROJECT : ZY9B

Size	Document Number	Rev
	Discharge/1V/1.8V)	1A

Date: Thursday, September 17, 2009 Sheet 47 of 49



Quanta Computer Inc.		
PROJECT : ZY9B		
Size	Document Number: Thermal Protection	Rev: 1A
Date: Thursday, September 17, 2009	Sheet 48 of 49	

Model	REV	CHANGE LIST
ZY9B MB	1A	FIRST RELEASED: E20080?-???? (PCB: DA0ZY9MB8A0)
	2A	Page4 :
	3A	
	3C	

MODEL	ZY9B	
	FROM	To
	X	1A
	X	1A
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DOC NO.	PROJECT MODEL :	ZY9B	APPROVED BY:	DATE:	2009/05/??
	PART NUMBER:		DRAWING BY:	REVISON:	1A

Quanta Computer Inc.
PROJECT : ZY9B

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	Change list	1A
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