SX7 SYSTEM DIAGRAM

AMD Smarter Choice

01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

DDRIII-SODIMM1 PAGE 6,7 — DDRIII 1066 MHz

DDRIII-SODIMM2 PAGE 6,7 — DDRIII 1066 MHz

AMD Champlain
35mm X 35mm
S1G4 Processor
638P (PGA) 25W
PAGE 3,4,5

CPU THERMAL SENSOR PAGE 5

14.318MHz

CLOCK GEN
ICS9LPRS476AKLFT-->HP
SLG8SP628VTR-->HP
RTM880N-796 -->HP
PAGE 2

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK

HT3

PCI-E

X1 New Card PAGE 29

X1 LAN Realtek PCIE-LAN RTL8151DH (10/100/1000) PAGE 28

X1 Mini PCI-E Card (Wireless LAN) PAGE 33

NORTH BRIDGE
RS880M
21mm X 21mm, 528pin BGA
PAGE 8,9,10,11

PCI-Express 16X

M93-S3/ Park-S3
64 Bit,DDR3*4
23mm X 23mm, 631pin BGA
PAGE 17,18,19,20,21,22

HDMI PAGE 24

CRT PAGE 23

LVDS PAGE 23

RJ45 PAGE 28

ALINK X4

SBSRC_CLK

USB2.0

SOUTH BRIDGE
SB820M
23mm X 23mm, 605pin BGA
PAGE 12,13.14.15.16

SATA0 150MB — SATA - HDD PAGE 31

SATA4 150MB — SATA - CD-ROM PAGE 31

SATA1 150MB — E-SATA PAGE 29

0,2,3,5 USB2.0 Ports PAGE 29

9 1 Blueflame PAGE 32

4 7 Webcam PAGE 23

FS1 8 Finger Printer PAGE 32

6 Flash Media RTS5159 PAGE 30

New Card PAGE 29

Wireless WAN PAGE 33

PCI-E WLAN Card x1 PAGE 33

Azalia

IDT 92HD80B1 PAGE 25

MDC CONN PAGE 29

LPC

SPI

Keyboard Touch Pad PAGE 32

SMSC KBC
KBC1098
PAGE 27

FAN PAGE 28

SPI ROM PAGE 35

Digital MIC PAGE 23

AUDIO CONN
Phone/ MIC
PAGE 28

SYSTEM CHARGER(bq24740) PAGE 36,37

3/5VS5 RT8206B PAGE 38

+1.1V(RT8029)/+1.1VS5/+1.8V PAGE 39

DDR3 (RT8207)/+1.0V_VGA PAGE 40

VGACORE(1.1V~0.9V)RT8028A PAGE 41

CPU_CORE ISL6265 PAGE 42

SMBUS TABLE		
SB--SCL0/SD0	Clock gen/ wirless LAN/ New card/ DDR3/ DDR3 thermal/ Accelerometer/system thermal	+3V
EC -- AB1A	Battery charge/discharge	+3VPCU
EC -- AB2A	VGA thermal	+3V

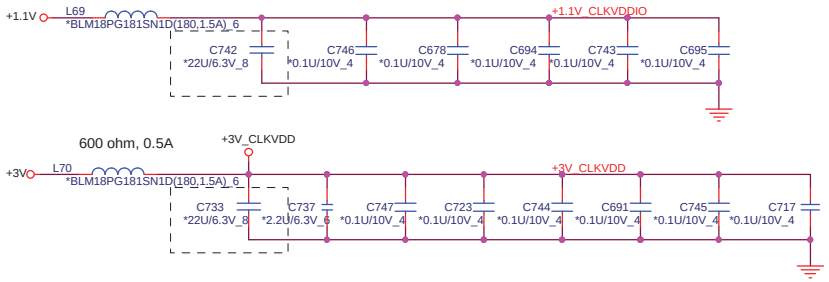
NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

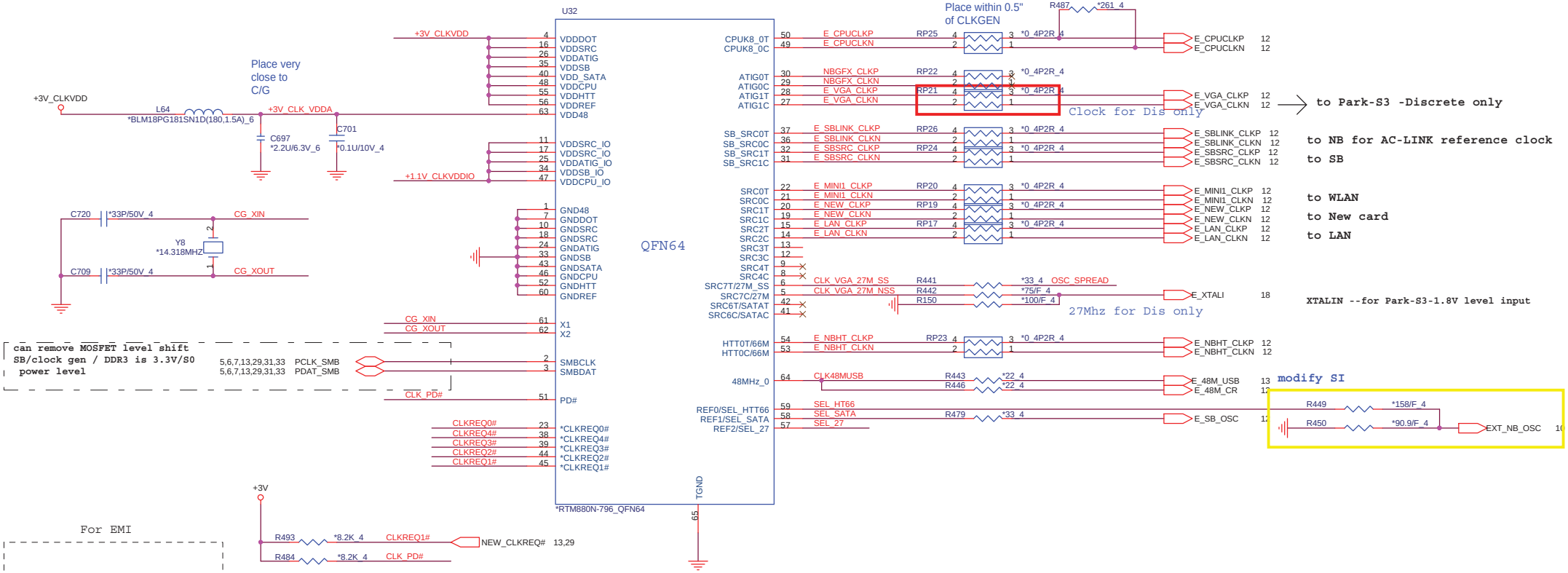
Size	Document Number	Rev
Custom	Block Diagram	3A

Date: Monday, March 15, 2010 Sheet 1 of 43

CLOCKS name	Discrete	Clock pin function
NBGFX_CLKP NBGFX_CLKN	NA	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP21 STUFF	to Park-S3 external reference clock -Discrete only
SBLINK_CLKP SBLINK_CLKN	RP26 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R441,R442 STUFF	To Park-S3 27Mhz - Discrete only



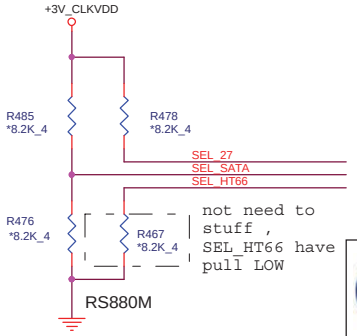
Need check the net name for the short pad



IDT ICS9LPRS480AKLFT--ALPRS480000
SLG SLG8SP628VTR--AL8SP628000
RTL RTM880N-796-- AL000880001

* default

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock



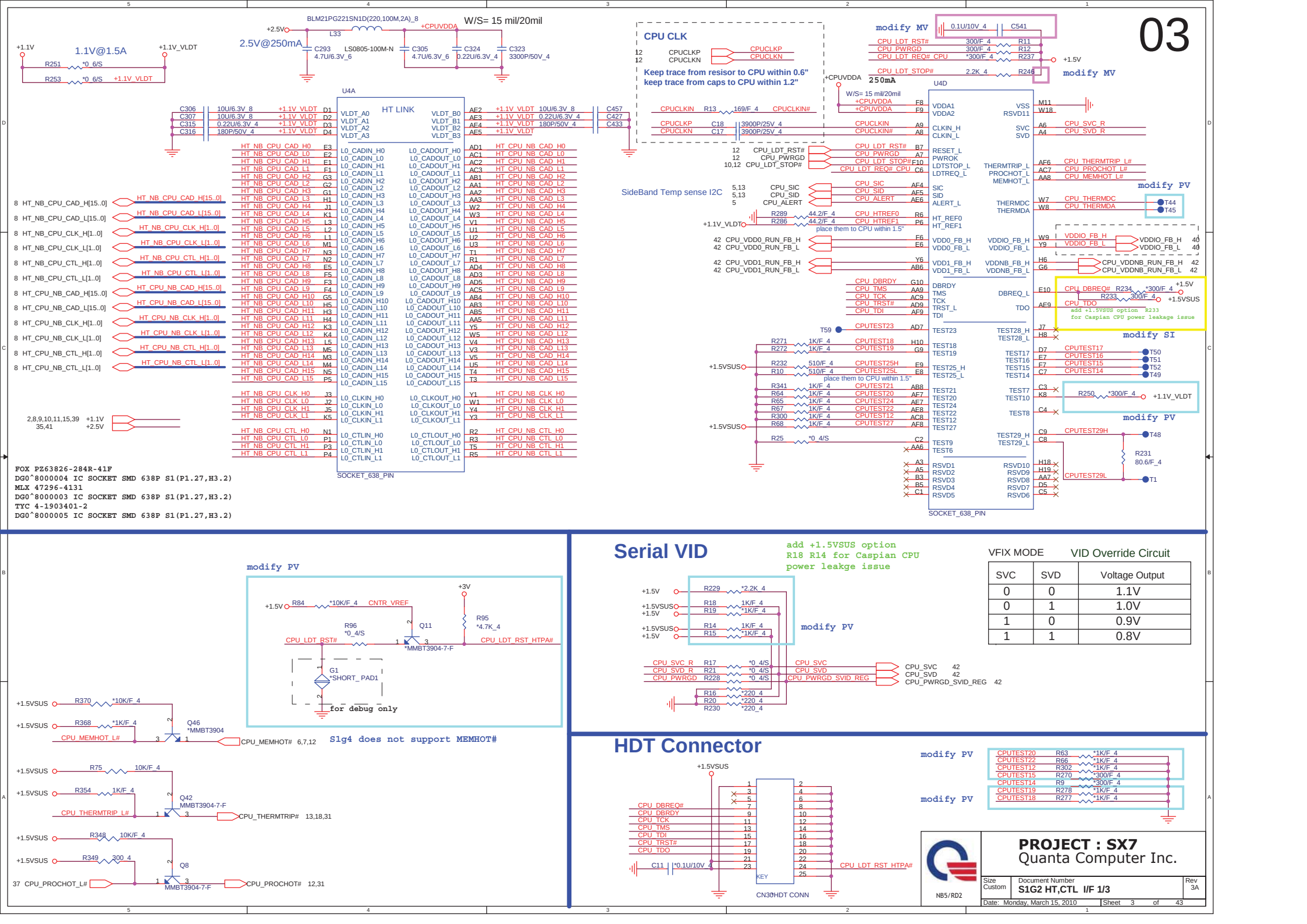
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Generator	3A

Date: Monday, March 15, 2010 Sheet 2 of 43

NB5/RD2


03
CPU CLK
Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"
modify MV
modify PV
modify SI
SideBand Temp sense I2C
HT LINK
U4A
U4D
SOCKET_638_PIN
FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)
Serial VID
add +1.5VSUS option
R18 R14 for Caspian CPU
power leakge issue
VFIX MODE
VID Override Circuit
SVC SVD Voltage Output
0 0 1.1V
0 1 1.0V
1 0 0.9V
1 1 0.8V
HDT Connector
S1g4 does not support MEMHOT#
for debug only
PROJECT : SX7
Quanta Computer Inc.
NB5/RD2
Size Custom
Document Number S1G2 HT,CTL I/F 1/3
Rev 3A
Date: Monday, March 15, 2010
Sheet 3 of 43

Processor Memory Interface

04

0.9V@1.5A

PLACE THEM CLOSE TO CPU WITHIN 1"

modify PV

U4B — MEM:CMD/CTRL/CLK — SOCKET_638_PIN

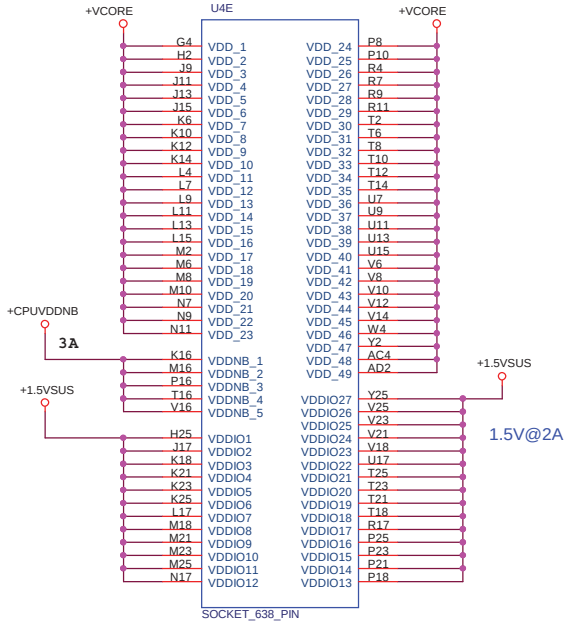
U4C — MEM:DATA — SOCKET_638_PIN

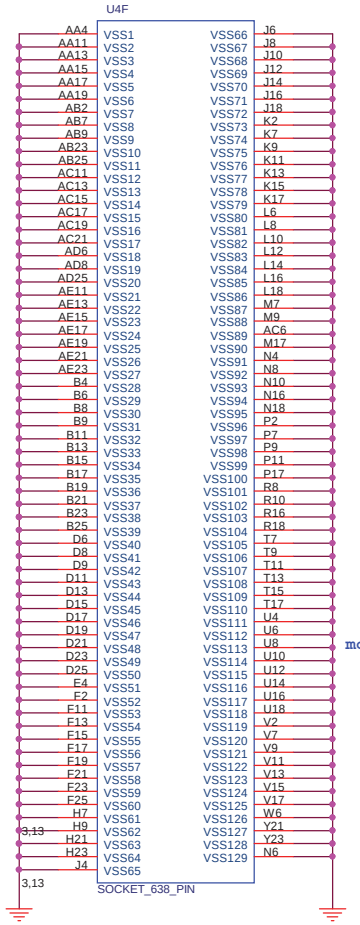
Place close to socket

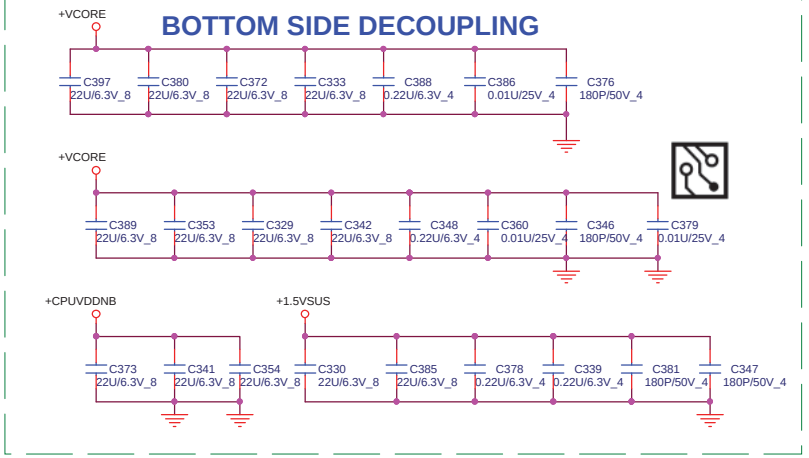
PROJECT :	SX7
	Quanta Computer Inc.
Size	Custom
Document Number	S1G2 DDRII MEMORY I/F 2/3
Rev	3A
Date:	Monday, March 15, 2010
Sheet	4 of 43

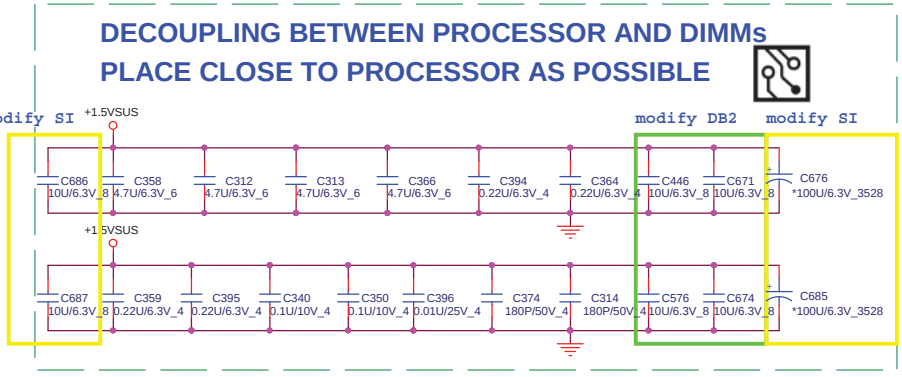
NB5/RD2

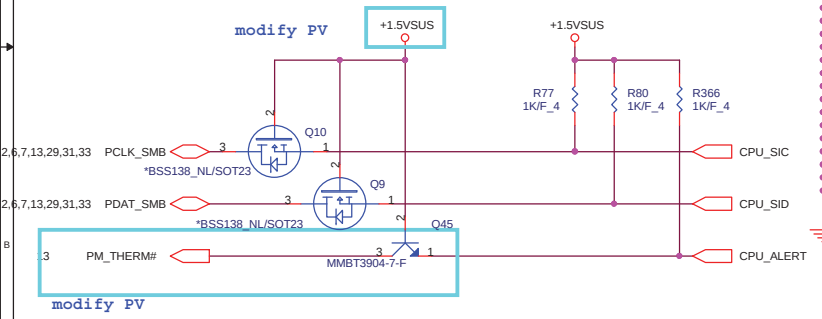
PROCESSOR POWER AND GROUND

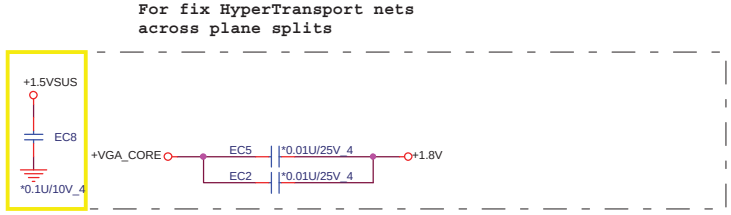


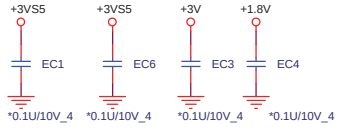










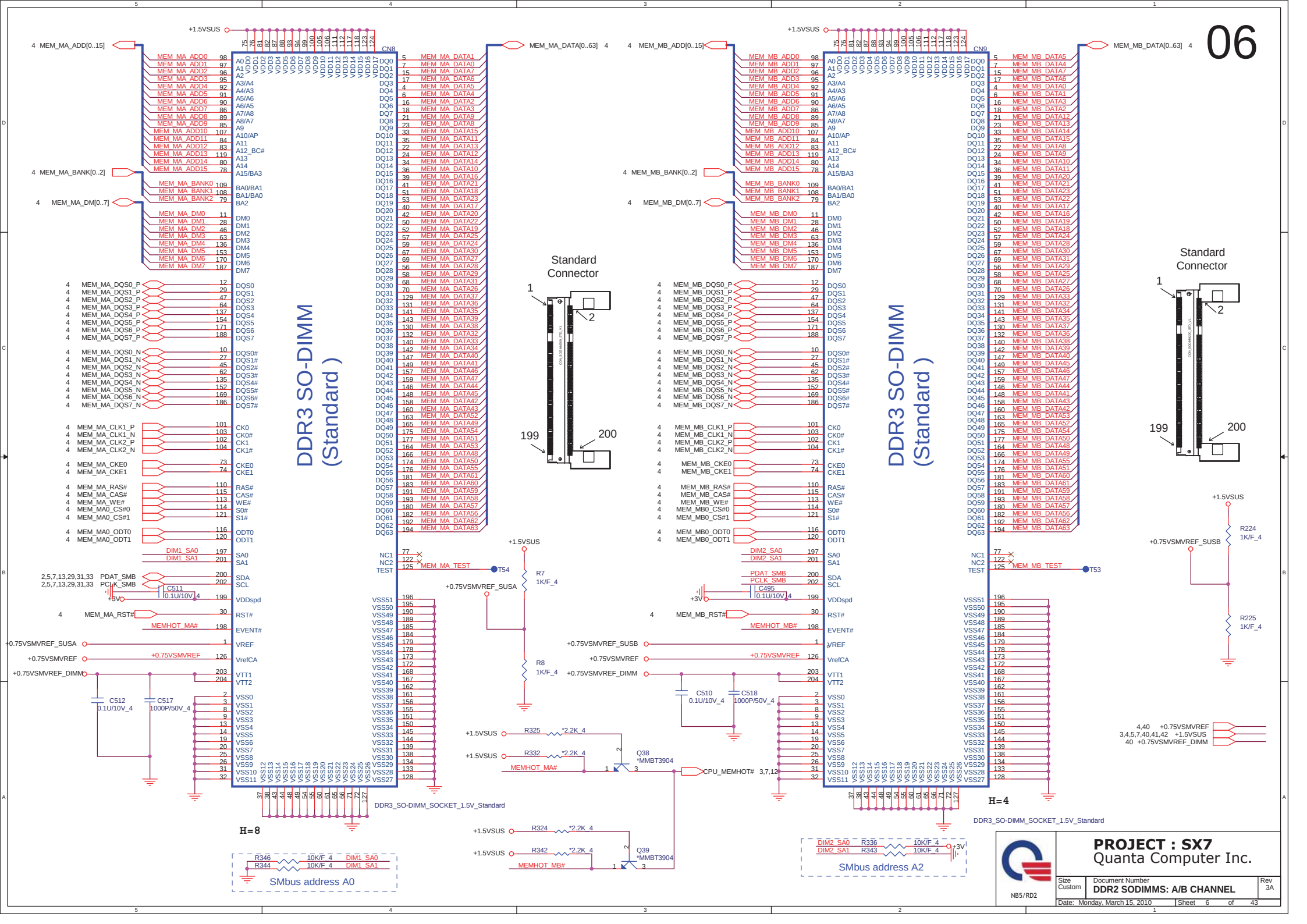


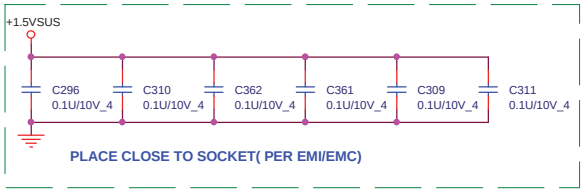
NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

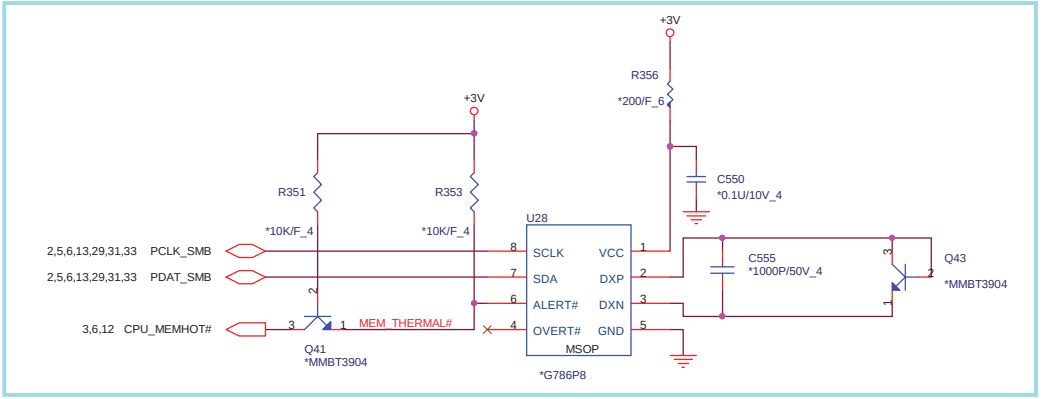
Size	Document Number	Rev
Custom	S1G2 PWR & GND 3/3	3A

Date: Monday, March 15, 2010 | Sheet 5 of 43

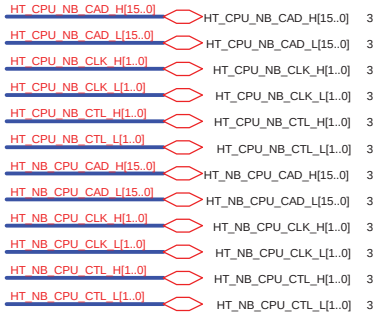

06
DDR3 SO-DIMM (Standard)
CN8
CN9
Standard Connector
H=8
H=4
DDR3_SO-DIMM_SOCKET_1.5V_Standard
SMbus address A0
SMbus address A2
PROJECT : SX7
Quanta Computer Inc.
NB5/RD2
DDR2 SODIMMS: A/B CHANNEL
Size Custom
Rev 3A
Date: Monday, March 15, 2010
Sheet 6 of 43



modify PV

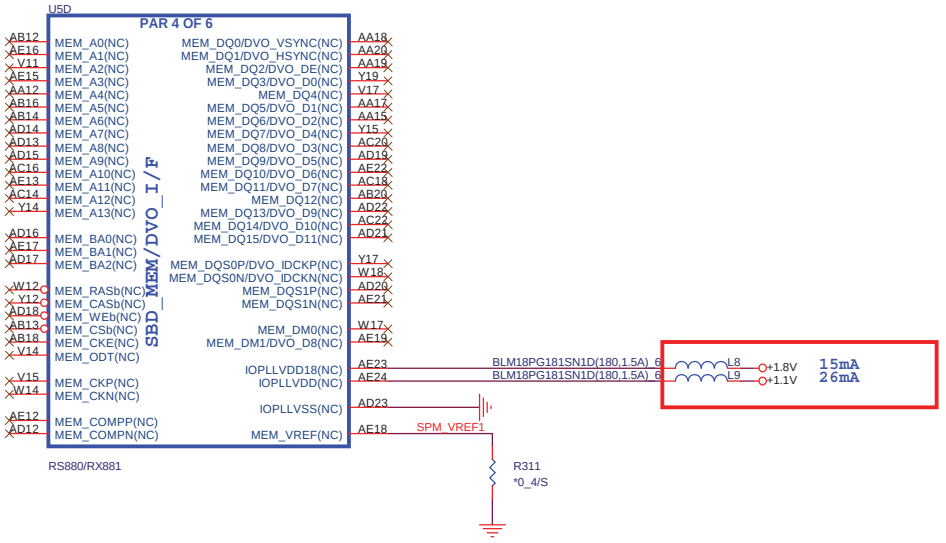


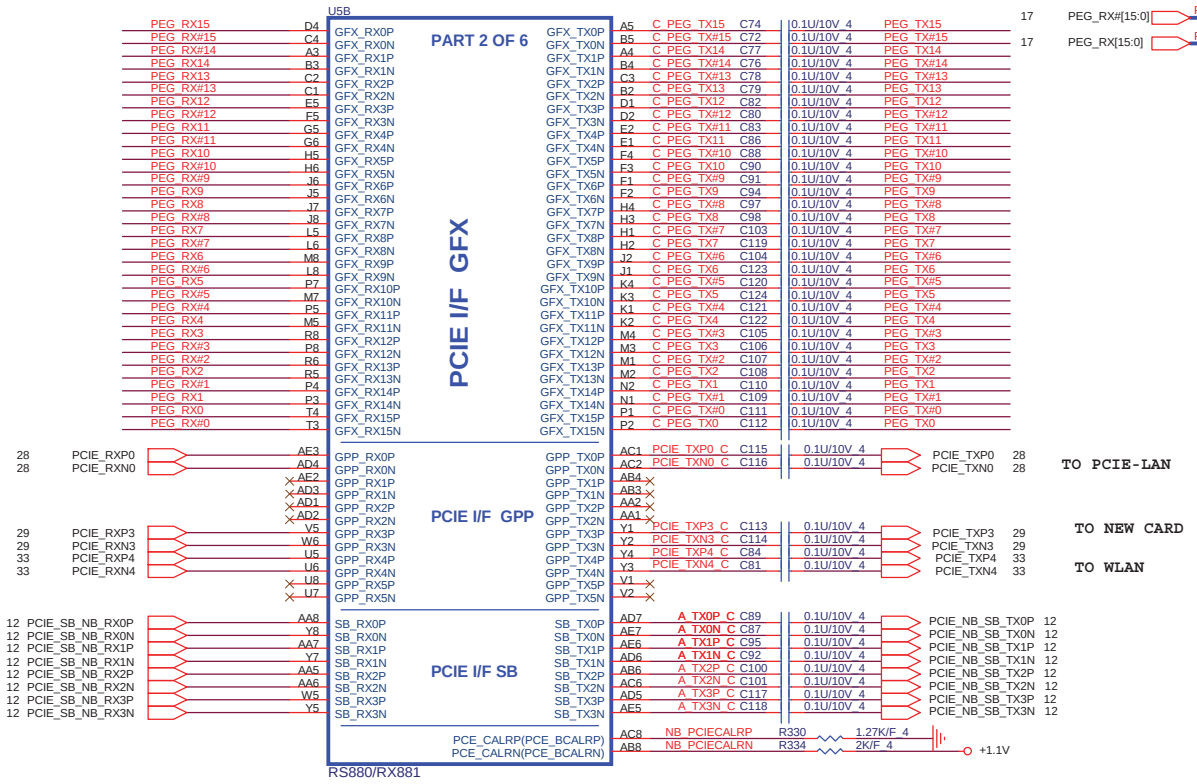
NB5/RD2	**PROJECT : SX7** Quanta Computer Inc.	
Size: Custom	Document Number: **DDR2 SODIMMS TERMINATIONS**	Rev: 3A
Date: Monday, March 15, 2010	Sheet 7 of 43	



signals	RS880M
HT_TXCALP	R430 301 ohm 1%
HT_TXCALN	
HT_RXCALP	R434 301 ohm 1%
HT_RXCALN	

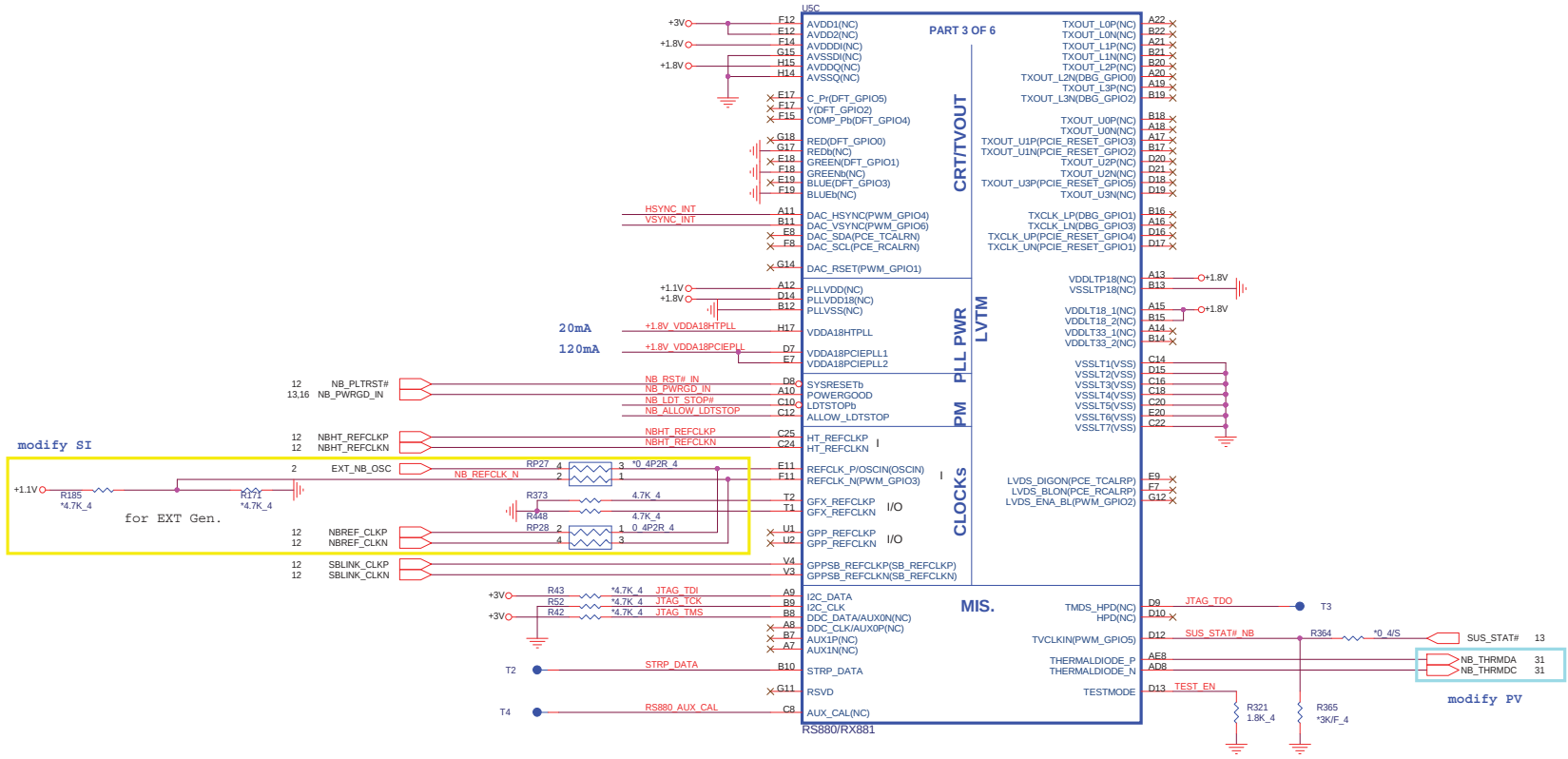
This block is for UMA only , Discrete can remove all component

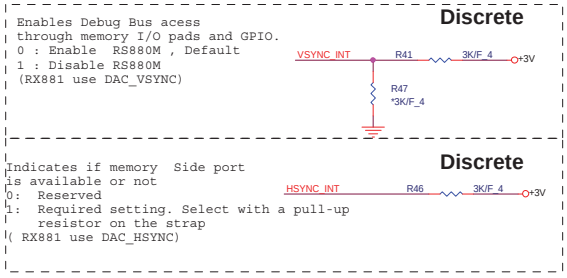


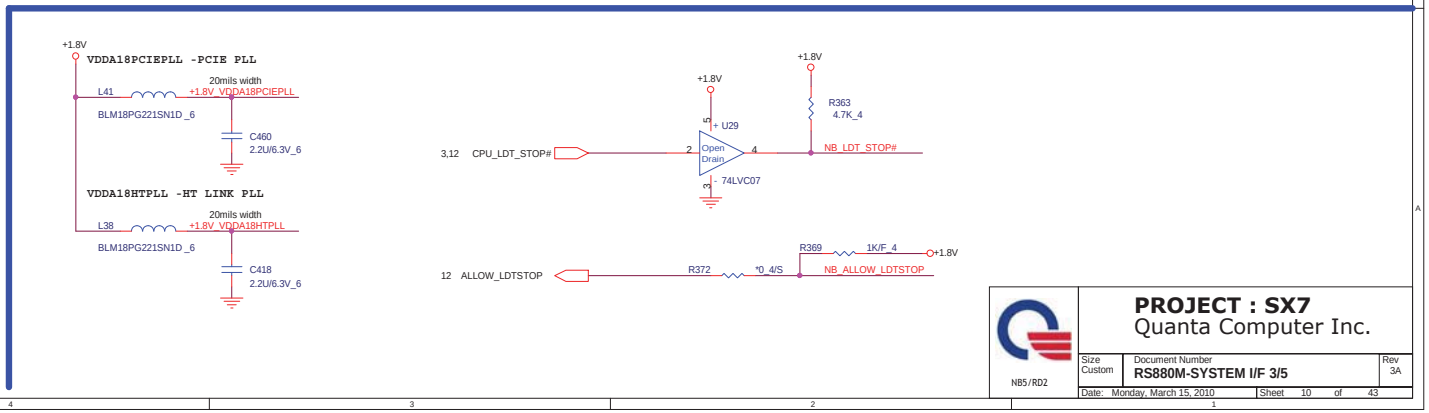


Project	Quanta Computer Inc.
Size	Custom
Document Number	RS880M-PCIE I/F 2/5
Rev	3A
Date	Monday, March 15, 2010
Sheet	9 of 43

NB5/RD2







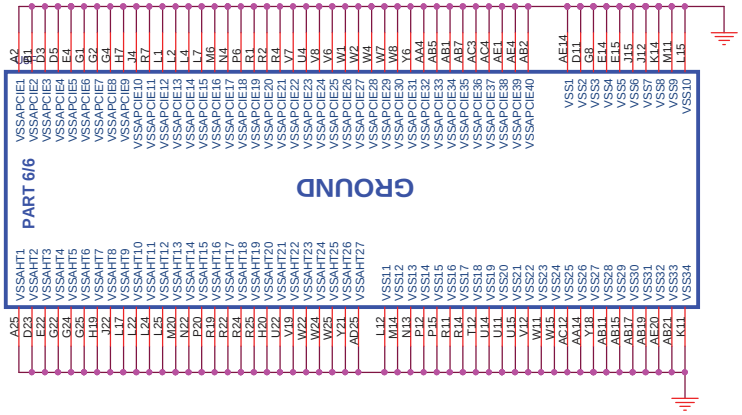
PROJECT : SX7
Quanta Computer Inc.

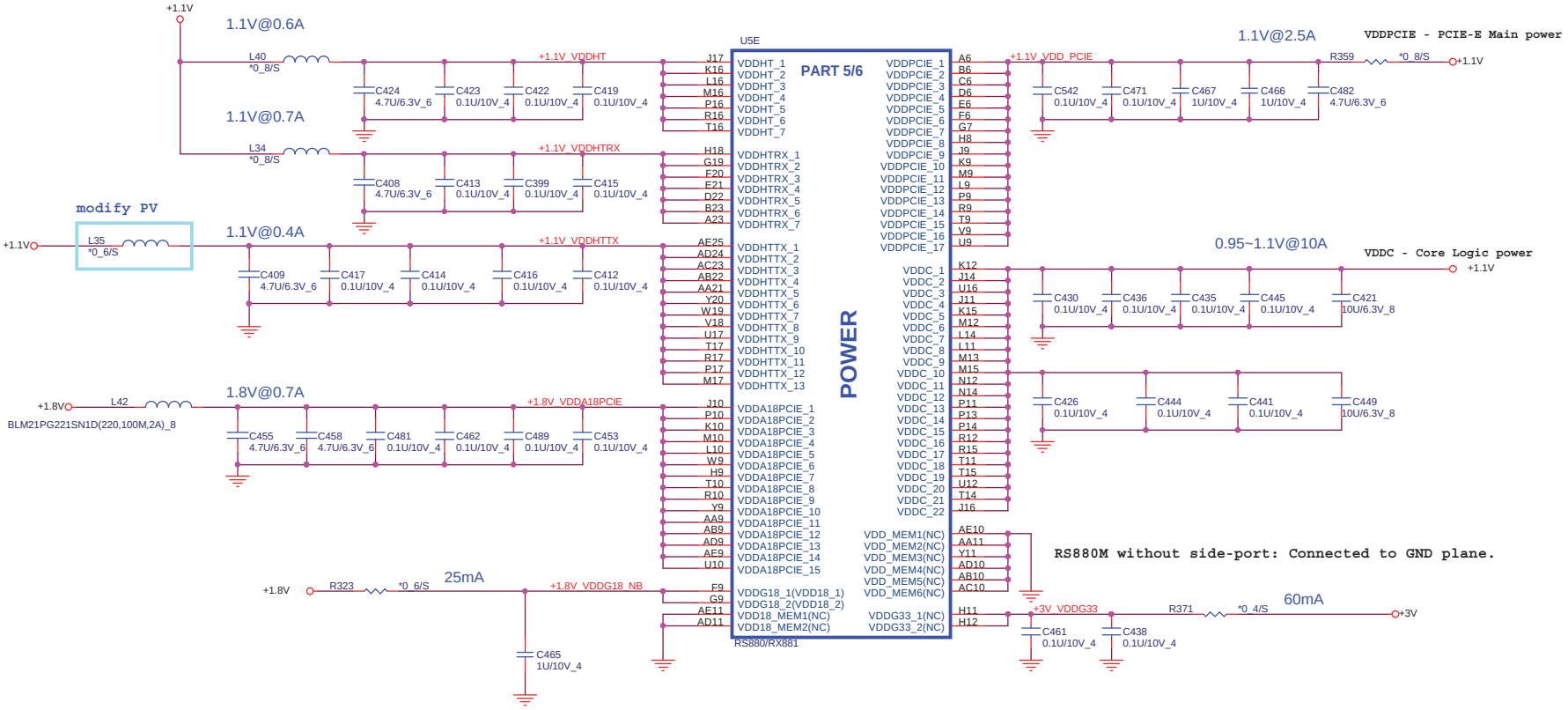
Size	Document Number	Rev
Custom	RS880M-SYSTEM I/F 3/5	3A
Date: Monday, March 15, 2010	Sheet 10 of 43	

NB5/RD2

RX881/RS880 POWER DIFFERENCE TABLE

PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVDD	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVDD18	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDDG33	+3.3V	+3.3V	VDDLT18	GND	+1.8V
IOPLLVDD18	+1.8V	+1.8V	VDDLT33	NC	NC





modify SI

modify PV

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO SB820

To RS880

U11A

SB800 Part 1 of 5

PCI CLKS

PCI EXPRESS INTERFACES

PCI INTERFACE

CLOCK GENERATOR

LPC

CPU

RTC

Change from
0ohm to 1K
for safty
issue

modify SI

modify PV

modify PV

for EMI
suggestion

modify PV

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

SB800 A11

IC CTRL(528P) SB710 A14(218-0660017)
P/N : AJ066000T01

NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-PCIE/PCI/CPU/LPC 1/4	3A

Date: Monday, March 15, 2010 | Sheet 12 of 43

NC only ,Can't be install

+3VS5 R427 *2.2K_4 SB_TEST0
R432 *2.2K_4 SB_TEST1
R423 *2.2K_4 SB_TEST2

+3V SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R377 2.2K_4 PCLK_SMB
R376 2.2K_4 PDAT_SMB
Clock gen/CPU thermal /DDR3/DDR3 thermal/Accelerometer

+3VS5 SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R428 2.2K_4 SB_SMBCLK1
R422 2.2K_4 SB_SMBDATA1

+3VS5 SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R458 2.2K_4 SB_SCLK2
R459 2.2K_4 SB_SDATA2

+3V modify PV
R418 4.7K_4 SUS_STAT#
modify MV

+3VS5
R514 *10K_4 SYS_RST#
R513 *10K_4 SB_RSMRST# 3
C857 *0.1U/10V_4

RCIN# 1
27 RCIN# 2 Q47 2N7002E

To Azalia

ACZ_SDOUT R139 33_4 ACZ_SDOUT_AUDIO 25
C166 *10P/50V_4
ACZ_SYNC R138 33_4 ACZ_SYNC_AUDIO 25
C163 *10P/50V_4
ACZ_BCLK R141 33_4 BIT_CLK_AUDIO 25
C169 22P/50V_4 EMI modify PV
ACZ_RST# R137 33_4 ACZ_RST#_AUDIO 25
ACZ_SDIN0 ACZ_SDIN0 25
Remove short pad

To Modem Board

ACZ_SDOUT R404 33_4 ACZ_SDOUT_MDC 29
C625 *10P/50V_4
ACZ_SYNC R402 33_4 ACZ_SYNC_MDC 29
C620 *10P/50V_4
ACZ_BCLK R142 33_4 BIT_CLK_MDC 29
C172 22P/50V_4 EMI modify PV
ACZ_RST# R400 33_4 ACZ_RST#_MDC 29
ACZ_SDIN1 ACZ_SDIN1 29
Remove short pad

modify DB2
T77 LID_SW# SB
27 SUSB# SUSC#
27,31 NBSWON1#
16 SB_PWRGD_IN
10 SUS_STAT#
SB_TEST0 SB_TEST1 SB_TEST2
GATEA20_SB RCIN# 1
modify DB2
27 KBC_SCI# 28 DSM#
T43 T42 CRD_REQ# SYS_RST#
modify DB2
28,29,33 PCIE_WAKE#
SB_THERMTRIP#
10,16 WD_PWRGD
27 RSMRST# R512 10K_4 SB_RSMRST#
modify MV

2,29 NEW_CLKREQ#
T70
2,28 LAN_CLKREQ#
23 WEBCAM_OFF
33 MC2_DISABLE
25 SPKR
2,5,6,7,29,31,33 PCLK_SMB
2,5,6,7,29,31,33 PDAT_SMB
SB_SMBCLK1 SB_SMBDATA1
modify DB2
2,33 WLAN_CLKREQ#
T69 CRD_CLKREQ#
28 LP_EN#
D18 RB501V-40 LID_SW# SB
23,27,31 LID_SW#
D17 RB501V-40 GATEA20_SB
27 GATEA20
modify PV
D22 RB501V-40 SB_THERMTRIP#
3,18,31 CPU_THERMTRIP#
29 NEW_CPPE#
5 PM_THERM#
R438 150K/F_4
27,36,37 ADP_PRES
SB_JTAG_TDO SB_JTAG_TCK SB_JTAG_TDI SB_JTAG_RST#

HD audio interface is +3VS5 voltage

R140 *10K/F_4
16 ACZ_SDOUT
ACZ_BCLK ACZ_SDOUT ACZ_SDIN0 ACZ_SDIN1 ACZ_SYNC ACZ_RST#

T81 ADP_PRES0

CN32 +3VS5
1 SB_JTAG_TCK
2 SB_JTAG_TDO
3 SB_JTAG_TDI
4 SB_TEST1
5
6 SB_JTAG_RST#
7
8
modify PV
C689 *10P/50V_4
SB JTAG
*S/W JTAG DEBUG

U11D
SB800 Part 4 of 5

PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#
ACPI / WAKE UP EVENTS

USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB 1.1 USB MISC

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN
GPIO

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#
USB OC

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
HD AUDIO

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR
GBE LAN

PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
EMBEDDED CTRL

USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USB 2.0

SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226
EMBEDDED CTRL

SB800 A11

E_48M_USB 2
USB_RCOMP_SB R433 11.8K/F_6
for EMI
C198 *2.2P/50V_4

USBSFDSP1+ 32
USBSFDSP1- 32 Finger Printer
USB_FDS12P T78
USB_FDS12N T76

USBP9+ 32
USBP9- 32 BLUETOOTH
USBP8+ 33
USBP8- 33 WLAN Min-Card
USBP7+ 33
USBP7- 33 WWAN
USBP6+ 30
USBP6- 30 USB card reader
USBP5+ 29
USBP5- 29 USB Connector
USBP4+ 23
USBP4- 23 Carama USB
USBP3+ 29
USBP3- 29 USB Connector
USBP2+ 29
USBP2- 29 E-SATA and USB Connector
USBP1+ 29
USBP1- 29 New Card
USBP0+ 29
USBP0- 29 USB Connector

CPU_SIC 3,5
CPU_SID 3,5
GPIO199 16
GPIO200 16

U10 TC7SH08FU +3VS5
SUSB# MAINON 20,35,36,40,41,43
U9 TC7SH08FU +3VS5
SUSC# SUSON 28,40,43

NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-ACPI/GPIO/USB 2/4	3A

Date: Monday, March 15, 2010 Sheet 13 of 43

SATA PORT 0,1,2,3
can support AHCI
mode

SATA HDD

SATA ODD

E-SATA

U11B

SB800
Part 2 of 5

SERIAL ATA

FLASH

HW MONITOR

SPI ROM

SATA_TXP0 / SATA_TXN0 → AH9 / AJ9 SATA_TX0P / SATA_TX0N
SATA_RXN0 / SATA_RXP0 → AJ8 / AH8 SATA_RX0N / SATA_RX0P
SATA_TXP1 / SATA_TXN1 → AH10 / AJ10 SATA_TX1P / SATA_TX1N
SATA_RXN1 / SATA_RXP1 → AG10 / AF10 SATA_RX1N / SATA_RX1P
SATA_TXP2 / SATA_TXN2 → AG12 / AF12 SATA_TX2P / SATA_TX2N
SATA_RXN2 / SATA_RXP2 → AJ12 / AH12 SATA_RX2N / SATA_RX2P
AH14 / AJ14 SATA_TX3P / SATA_TX3N
AG14 / AF14 SATA_RX3N / SATA_RX3P
AG17 / AF17 SATA_TX4P / SATA_TX4N
AJ17 / AH17 SATA_RX4N / SATA_RX4P
AJ18 / AH18 SATA_TX5P / SATA_TX5N
AH19 / AJ19 SATA_RX5N / SATA_RX5P

modify DB2

+1.1V_AVDD_SATA
R398 1K/F_4
R393 931/F_4
SATA_CALRP → AB14 SATA_CALRP
SATA_CALRN → AA14 SATA_CALRN

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

SB_SATA_LED# → AD11 SATA_ACT#/GPIO67
+3V R375 10K/F_4

modify DB2
C131 *22P/50V_4
Y1 *25MHZ
R108 *1M_4
C125 *22P/50V_4
SATA_X1 → AD16 SATA_X1
SATA_X2 → AC16 SATA_X2
for EXT Gen.

27 KBC_SPI_SO → J5 SPI_DI/GPIO164
27 KBC_SPI_SI → E2 SPI_DO/GPIO163
27 KBC_SPI_CLK → K4 SPI_CLK/GPIO162
27 KBC_SPI_CS0# → K9 SPI_CS1#/GPIO165
27 DEBUGRST# → G2 ROM_RST#/GPIO161

modify SI

SB800 A11

FC_CLK AH28
FC_FBCLKOUT AG28
FC_FBCLKIN AF26
FC_OE#/GPIOD145 AE28
FC_AVD#/GPIOD146 AG29
FC_WE#/GPIOD148 AG26
FC_CE1#/GPIOD149 AF27
FC_CE2#/GPIOD150 AE29
FC_INT1/GPIOD144 AF29
FC_INT2/GPIOD147 AH27
FC_ADQ0/GPIOD128 AJ27
FC_ADQ1/GPIOD129 AJ26
FC_ADQ2/GPIOD130 AH25
FC_ADQ3/GPIOD131 AH24
FC_ADQ4/GPIOD132 AG23
FC_ADQ5/GPIOD133 AH23
FC_ADQ6/GPIOD134 AJ22
FC_ADQ7/GPIOD135 AG21
FC_ADQ8/GPIOD136 AF21
FC_ADQ9/GPIOD137 AH22
FC_ADQ10/GPIOD138 AJ23
FC_ADQ11/GPIOD139 AF23
FC_ADQ12/GPIOD140 AJ24
FC_ADQ13/GPIOD141 AJ25
FC_ADQ14/GPIOD142 AG25
FC_ADQ15/GPIOD143 AH26

FANOUT0/GPIO52 W5 → WLAN_OFF# 33
FANOUT1/GPIO53 W6 → BT_OFF 32
FANOUT2/GPIO54 Y9 → WWAN_OFF# 33
FANIN0/GPIO56 W7 → WWAN_DET# 33
FANIN1/GPIO57 V9
FANIN2/GPIO58 W8 CRD_REQ1# → T75
TEMPIN0/GPIO171 B6
TEMPIN1/GPIO172 A6
TEMPIN2/GPIO173 A5 MB_THRMDA_SB → T83
TEMPIN3/TALERT#/GPIO174 B5 → T82
TEMP_COMM C7 TEMP_COMM R471 *0_4/S
VIN0/GPIO175 A3
VIN1/GPIO176 B4
ACCLED_EN 31
VIN2/GPIO177 A4 SIDE_PORT_ID0
VIN3/GPIO178 C5 SIDE_PORT_ID1
VIN4/GPIO179 A7 BOARD_ID0
VIN5/GPIO180 B7 BOARD_ID1
VIN6/GBE_STAT3/GPIO181 B8 BOARD_ID2
VIN7/GBE_LED3/GPIO182 A8 BOARD_ID3

modify PV

NC1 G27
NC2 Y2

modify MV

+3VS5 R470 *10K/F_4 SIDE_PORT_ID0
+3VS5 R465 *10K/F_4 SIDE_PORT_ID1

modify PV

+3VS5
R473 *10K/F_4 BOARD_ID0 R472 *10K/F_4
R461 *10K/F_4 BOARD_ID1 R455 *10K/F_4
R462 *10K/F_4 BOARD_ID2 R445 *10K/F_4
R167 *10K/F_4 BOARD_ID3 R166 *10K/F_4

+3V
C578 *0.1U/10V_4
U30 *TC7SH08FU
31 SATA_LED#
SB_SATA_LED#
R109 *0_4/S

ID3	ID2	ID1	ID0	
0	0	0	0	SX7 UMA
0	0	0	1	SX7 UMA
0	0	1	0	SX7 Dis
0	0	1	1	SX7 Dis
0	1	0	0	SX7 UMA DF
0	1	0	1	SX7 UMA DF
0	1	1	0	SX7 Dis DF
0	1	1	1	SX7 Dis DF

NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-ACPI/GPIO/USB 2/4	3A

Date: Monday, March 15, 2010 | Sheet 14 of 43

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

VDDQ--3.3V I/O power

VDD-- S/B CORE power

SB820 without GBE: Connected to GND plane.

modify DB2

For support USB wakeup-->3V_S5

SB800 A11

Part 3 of 5

Part 5 of 5

PROJECT : SX7
Quanta Computer Inc.

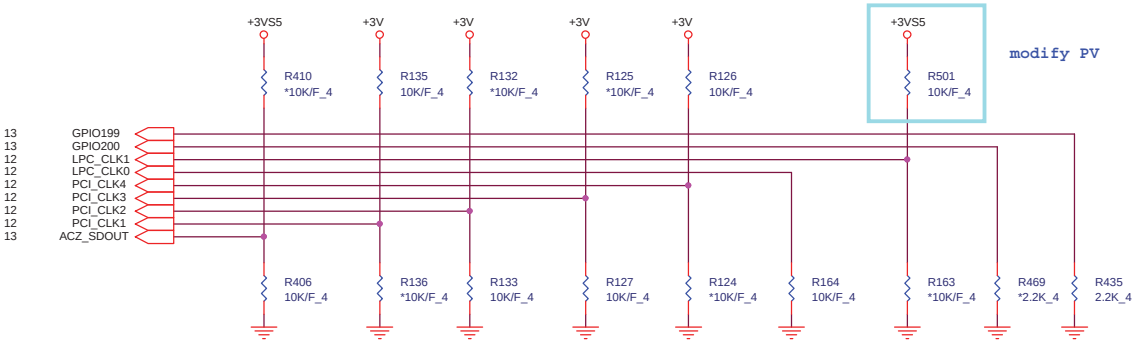
Size	Document Number	Rev
Custom	SB820-PWR/DECOUPLING 4/4	3A

Date: Monday, March 15, 2010 Sheet 15 of 43

NB5/RD2

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS



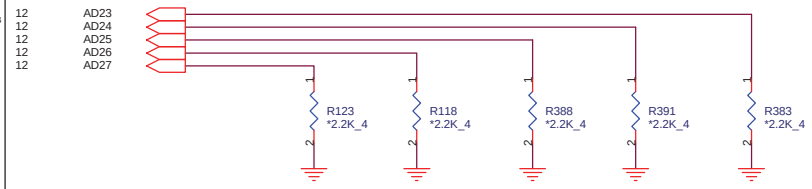
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM DEFAULT
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM L, L=FWH ROM

modify DB2

internal have pull Hi 10K

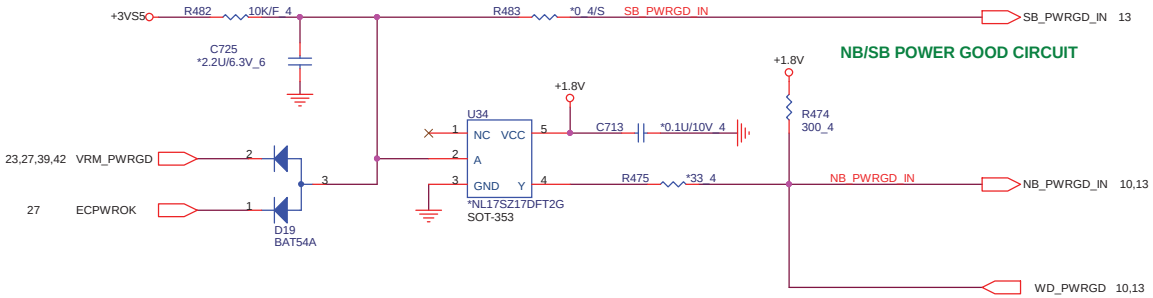
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB820-STRAPS	3A

Date: Monday, March 15, 2010 Sheet 16 of 43

POWER
for M9x-S3 DPx_VDD10=1.1V
for Park-S3 DPx_VDD10=1.0V

U6A

2.5GT/s bit rate

PCI EXPRESS INTERFACE

M9x-S2/S3 + Park-S3

100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing

M9x-S3:PWRGOOD NC
Park-S3:PWRGOOD Pull low 10K

U6G

M9x-S3:TMDS 1.1V@170mA LVDS 1.1V@100mA
Park-S3:TMDS 1.0V@110mA LVDS 1.0V@120mA

M9x-S3:1.1V@200mA Park-S3:1.0V@110mA

M9X-S2/S3 + Park-S3

VGA Core BPP
VGA Core VDDC
+1.8V PCIE_VDDR
+1.8V PCIE_PVDD
+1.8V VDDR1
3.3V_Delay VDDR3

20ms 20ms

PROJECT : SX7
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	Park_PCIE_Interface	3A

Date: Monday, March 15, 2010 Sheet 17 of 43

MEM_ID[2:0]	Vendor	Type	Vendor P/N
000	Samsung E-die	64M*16-800MHZ	K4W1G1646E-HC12
100	Hynix Orion-die	64M*16-800MHZ	H5TQ1G63BFR-12C
010	Samsung E-die	128M*16-800MHZ	
110	Hynix Orion-die	128M*16-800MHZ	

	PWRCNTL1	PWRCNTL0	V-CORE
	1	1	0.9V
	1	0	0.95V
	0	1	1.05V
	0	0	1.1V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V

No need "CLK_27M_SS" connect to GPIO_16, since M9x chip support memory SS function in VBIOS

modify PV

Memory ID

modify PV

R56 10K/F_4 GPIO22

GPIO22(ROMCS#) PD without external VBIOS ROM

+1.8V R79 *0_4 +1.8V_DPC_PVDD 1.8V(200mA DPC_PVDD)

+1.8V R86 *0_4 +1.8V_DPC_VDD18 1.8V(130mA DPC_VDD18)

+1.0V_VGA R81 *0_4 +1.1V_DPC_VDD10 1.1V(110mA DPC_VDD10)

For Park-S3 only

M93-S3/ Park-S3:Use 150R Pull down
Park-S3:NC

R357 150/F_4

modify PV

modify PV

modify PV

modify PV

modify PV

modify SI

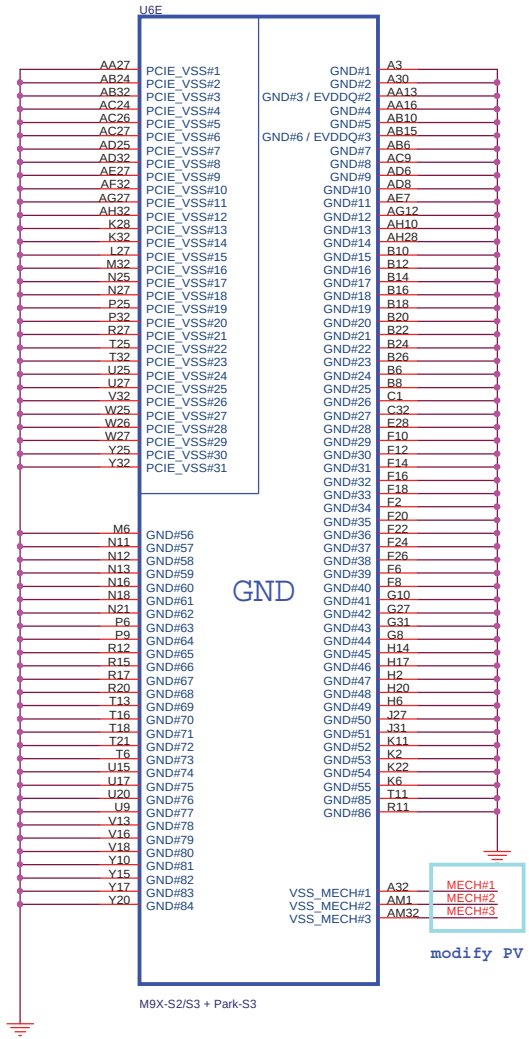
3,13,31 CPU_THERMTRIP# Q33 2N7002E R54 10K/F_4 TEMP_FAIL

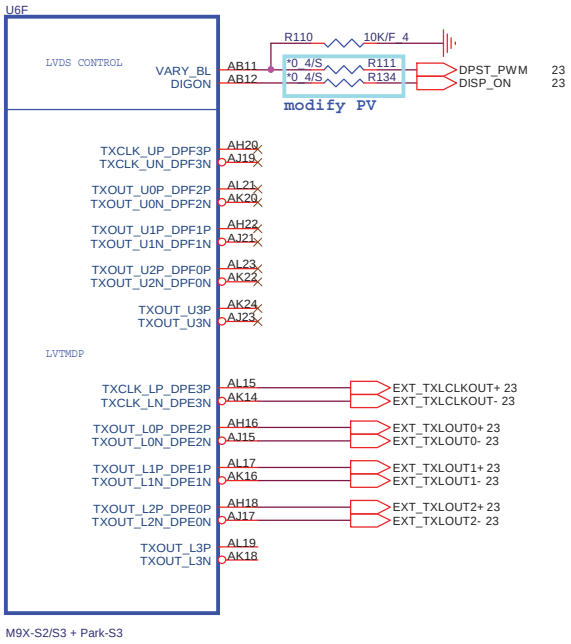
ADD VGA TEMP_ FAIL function
M93 is active Hi

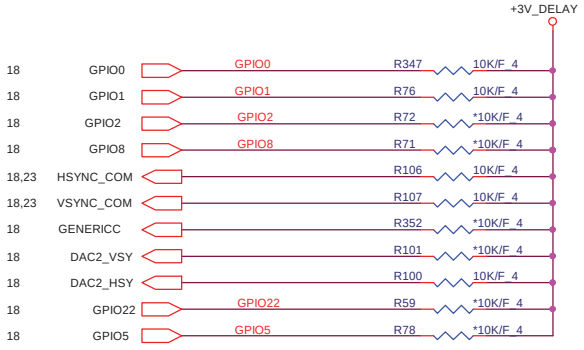
For Int Clk 27Mhz

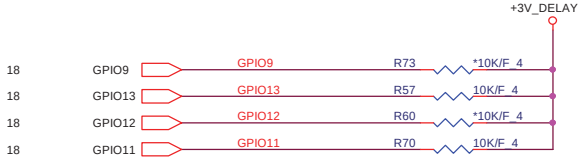
CL=20PF Y2 27MHZ C136 22P/50V_4 C135 22P/50V_4 R99 10M_6 EVGA-XTALI EVGA-XTALO

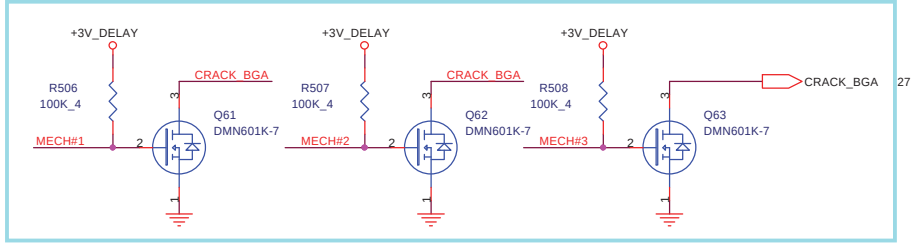
M9X-S2/S3 + Park-S3











Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	PCI Express Full TX Output Swing 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0 0 0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	1
AUD[0] AUD(1)	VSYNC HSYNC	AUD[1] AUD[0] 00 No Audio function 01 Audio for DisplayPort and HDMI if dongle is detected 10 Audio for DisplayPort only 11 Audio for both DisplayPort and HDMI	1 1
VIP_DEVICE_STRAP_ENA	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
RSVD	GENERICC		0

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Park_GND / LVDS/ Straps	3A
Date: Monday, March 15, 2010	Sheet 19 of 43	

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%

1.5V(2.A VDDR1+VDDRHA)

1.8V(110mA VDD_CT)

Gated 3.3V 60mA by VDDC

modify SI

VDD_R3 --IO power for 3.3 V pins (e.g. GPIO's). 3.3 V ± 5%

1.8V(170mA VDDR4)

1.8V(170mA VDDR5)

only for M93-S3 Used

1.8V(68mA PCIE_PVDD)

0.95V~1.1V(35mA SPV10)

1.5/1.8V 120mA

Park-S3 no support Back Bias

VDD_R4 -- Power for DVPDATA_[23:12] - external TMDS or GPIO; corresponds to DVOA_MSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%

VDD_R5 -- Power for DVP control pins (DVPCNTL_[0-2] and DVPCLK) and DVPDATA_[11:0] - external TMDS or GPIO; corresponds to DVOA_LSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V; 1.8 V ± 5% or 3.3 V ± 5%

only for Park-S3 Used

modify MV

BBP -- Connect to VBBP back bias regulator / generator. If back bias is not used, connect directly to VDDC.

Back Bias Enabled: (GPIO_21_BB_EN = 3.3 V): 1.5 V or 1.8 V

Back Bias Disabled: (GPIO_21_BB_EN = 0 V): VDDC

1.8V(500mA)

1.1V(2.0A)

PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%

VDDC+VDDCI 0.95~1.1V(15A peak)(Ripple < 87.2mV)

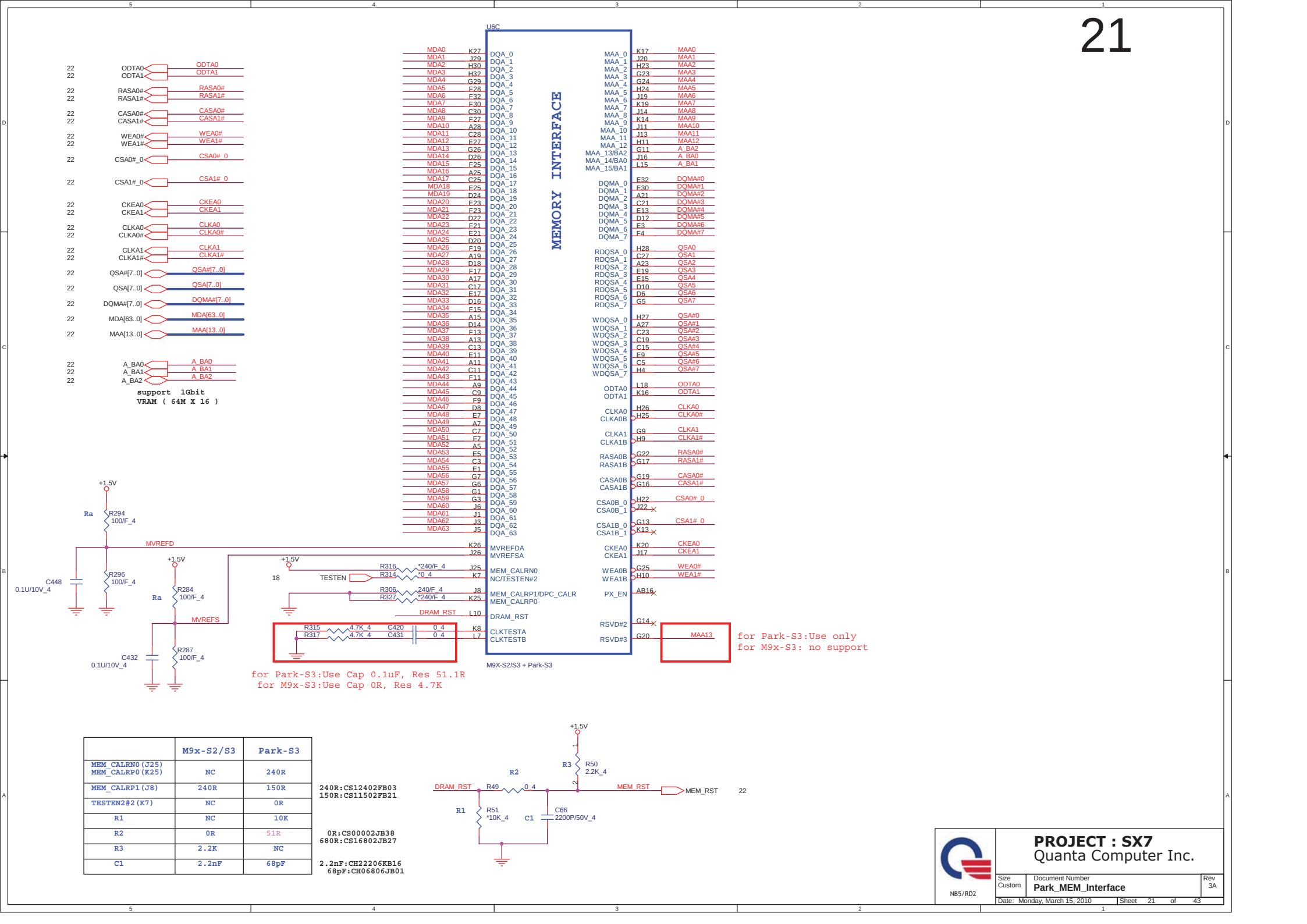
VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2V (± 5%)

0.95V~1.1V(2A VDDCI)

VDDCI--Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

M9X-S2/S3 + Park-S3

PROJECT : SX7	
Quanta Computer Inc.	
Size: Custom	Document Number: Park_Power_and_NC
Rev: 3A	
Date: Monday, March 15, 2010	Sheet 20 of 43
NB5/RD2	



	M9x-S2/S3	Park-S3
MEM_CALRN0(J25) MEM_CALRP0(K25)	NC	240R
MEM_CALRP1(J8)	240R	150R
TESTEN2#2(K7)	NC	0R
R1	NC	10K
R2	0R	51R
R3	2.2K	NC
C1	2.2nF	68pF

240R:CS12402FB03
150R:CS11502FB21

0R:CS00002JB38
680R:CS16802JB27

2.2nF:CH22206KB16
68pF:CH06806JB01

NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Park_MEM_Interface	3A

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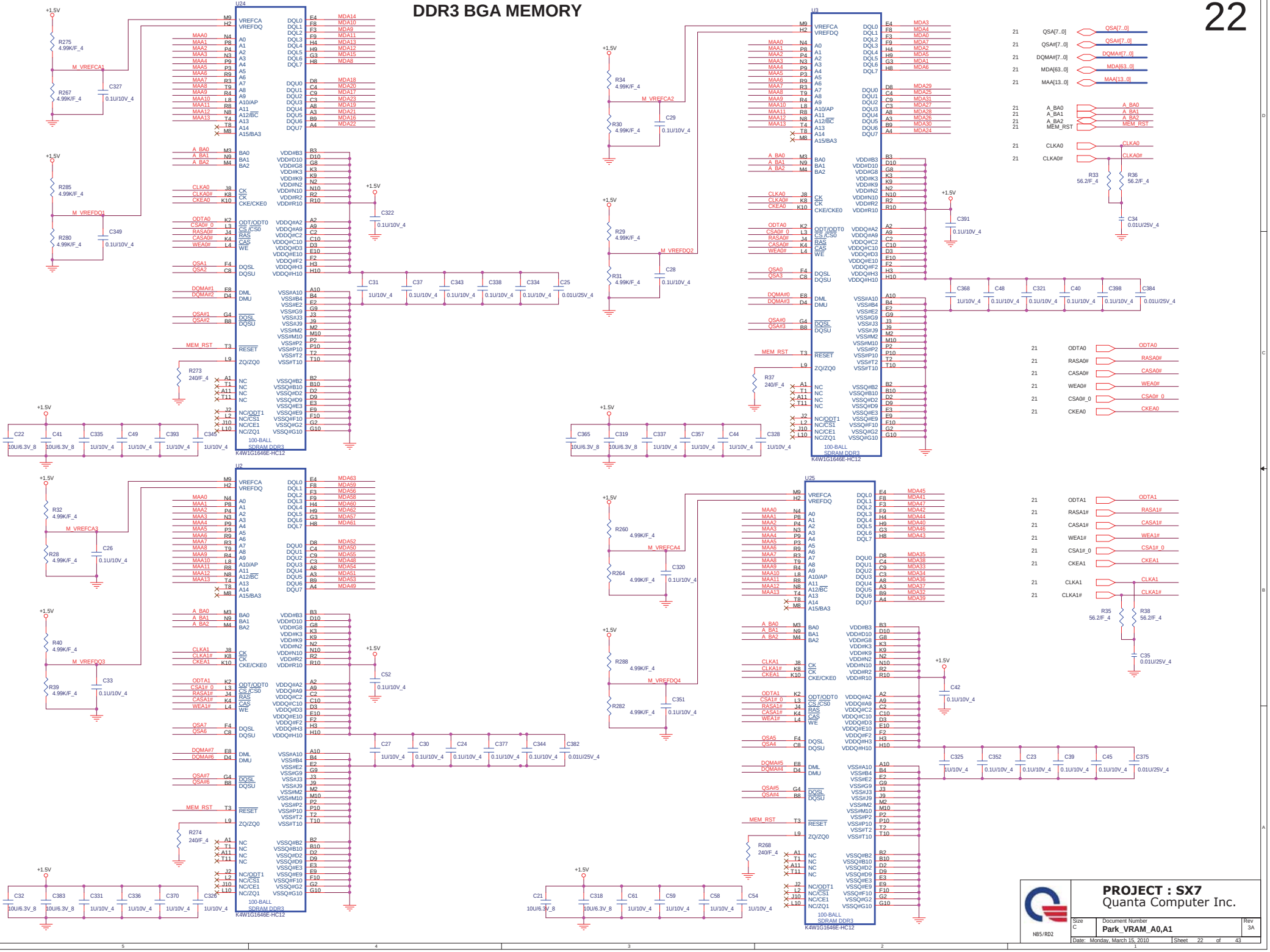
DDR3 BGA MEMORY

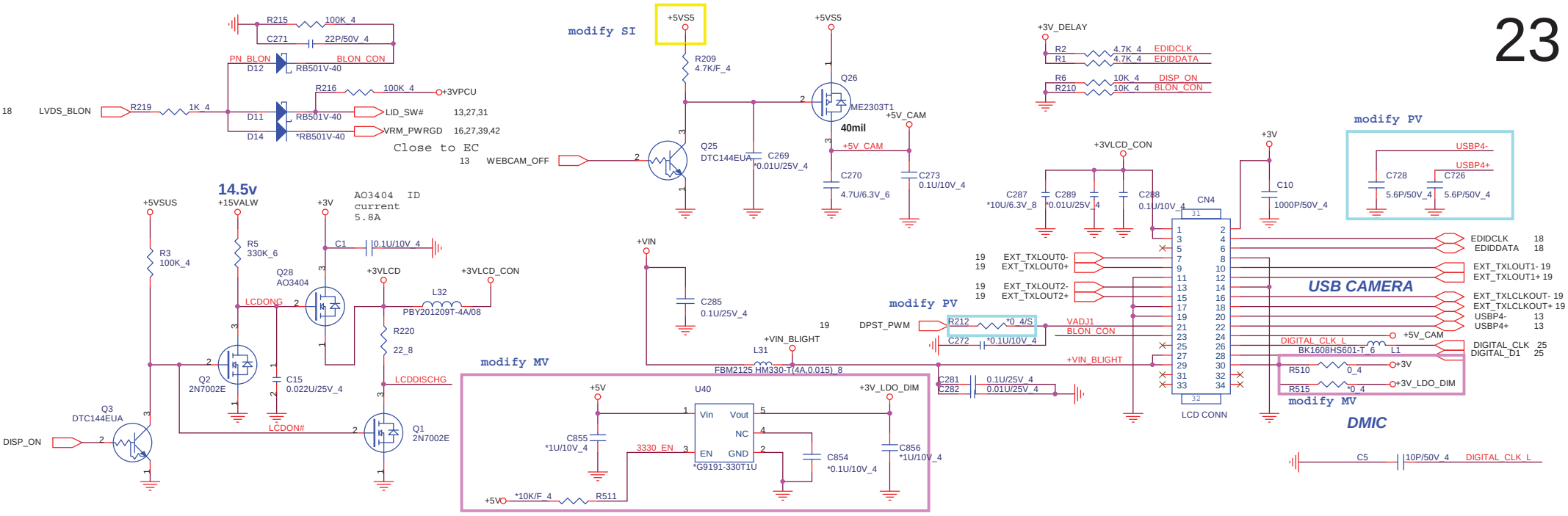


PROJECT : SX7
Quanta Computer Inc.

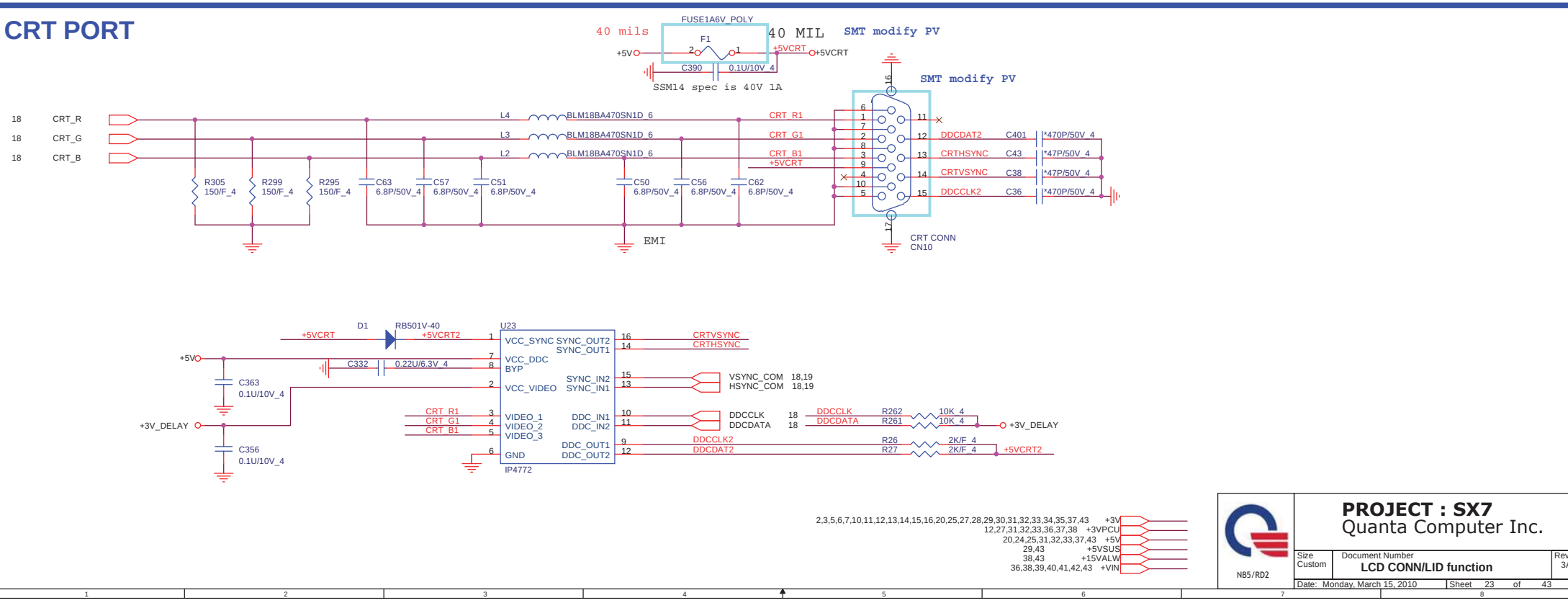
Size	Document Number	Rev
C	Park_VRAM_A0,A1	3A

NB5/RD2

Date: Monday, March 15, 2010 | Sheet 22 of 43



CRT PORT

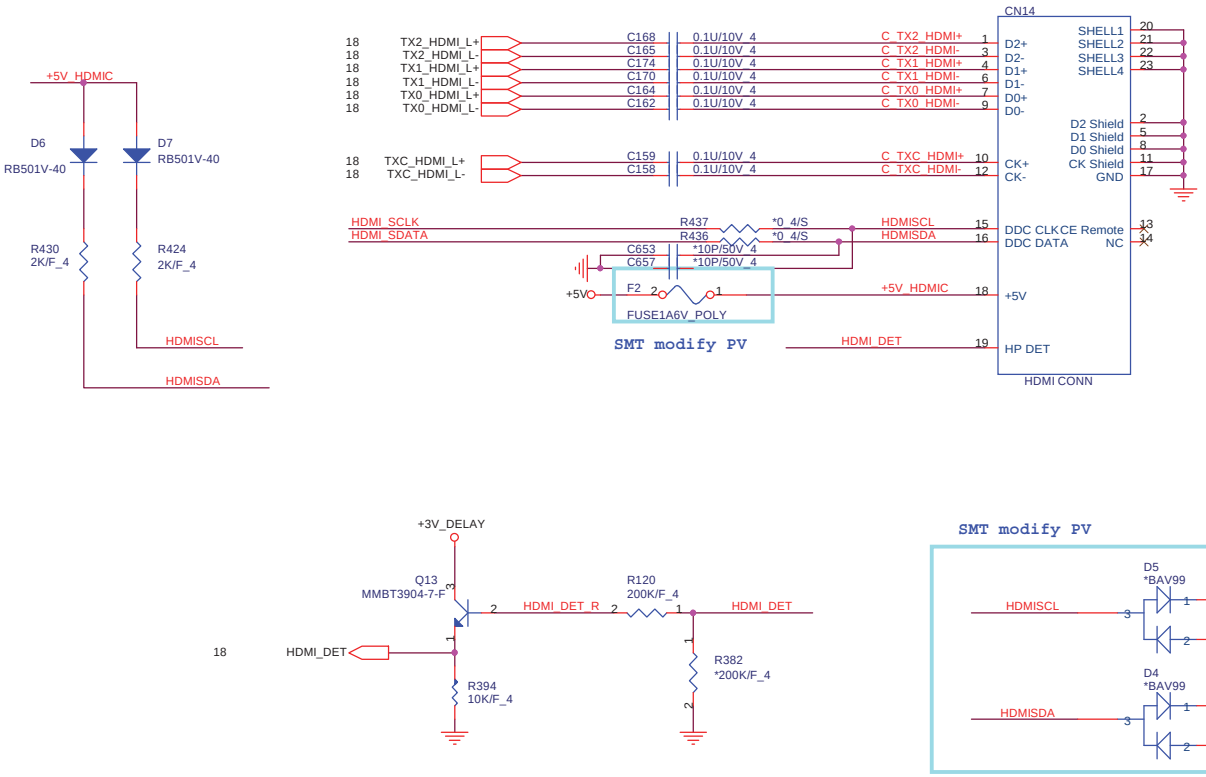


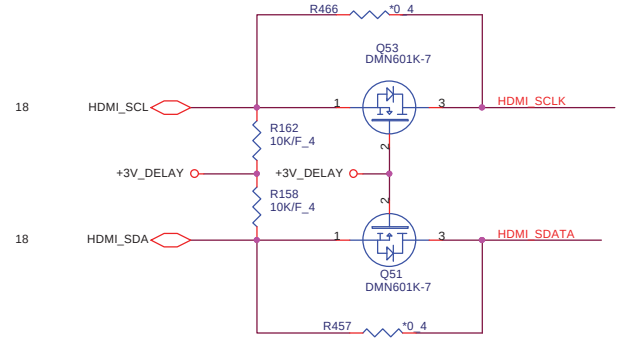
PROJECT : SX7
Quanta Computer Inc.

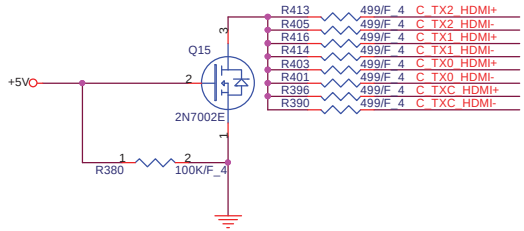
NB5/RD2

Size	Document Number	Rev
Custom	LCD CONN/LID function	3A
Date: Monday, March 15, 2010	Sheet 23 of 43	

HDMI PORT







SMT modify PV

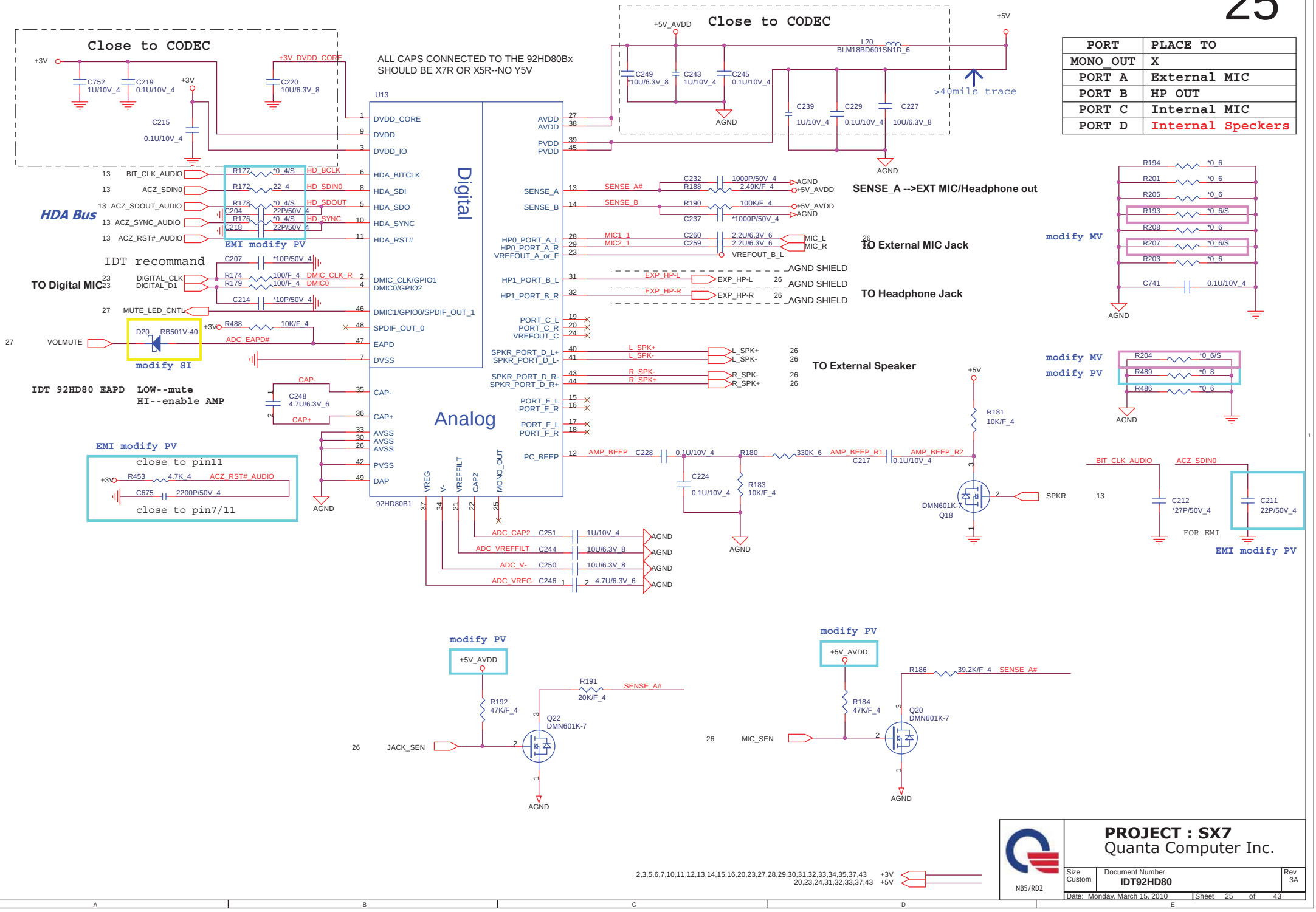
20,23,25,31,32,33,37,43 +5V

NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

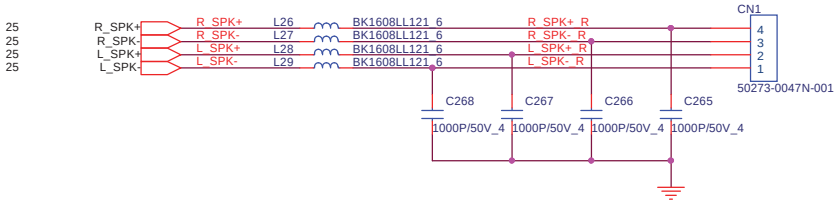
Size	Document Number	Rev
Custom	**HDMI Conn**	3A
Date: Monday, March 15, 2010	Sheet 24 of 43	

PORT	PLACE TO
MONO_OUT	X
PORT A	External MIC
PORT B	HP OUT
PORT C	Internal MIC
PORT D	Internal Speckers

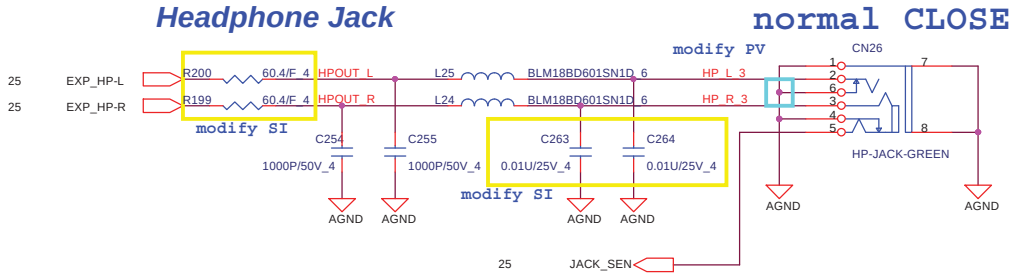


Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

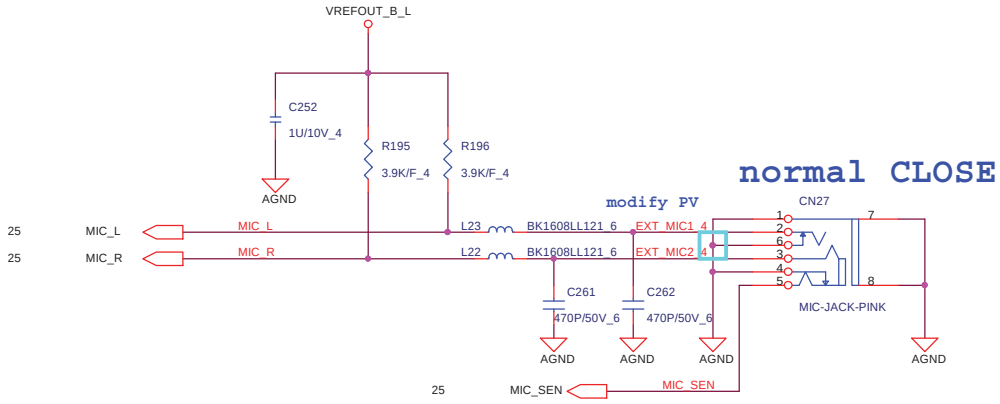
INT. SPEAKER



Headphone Jack



EXT Mic Jack



Note: MIC_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HP/MIC/SPK	3A

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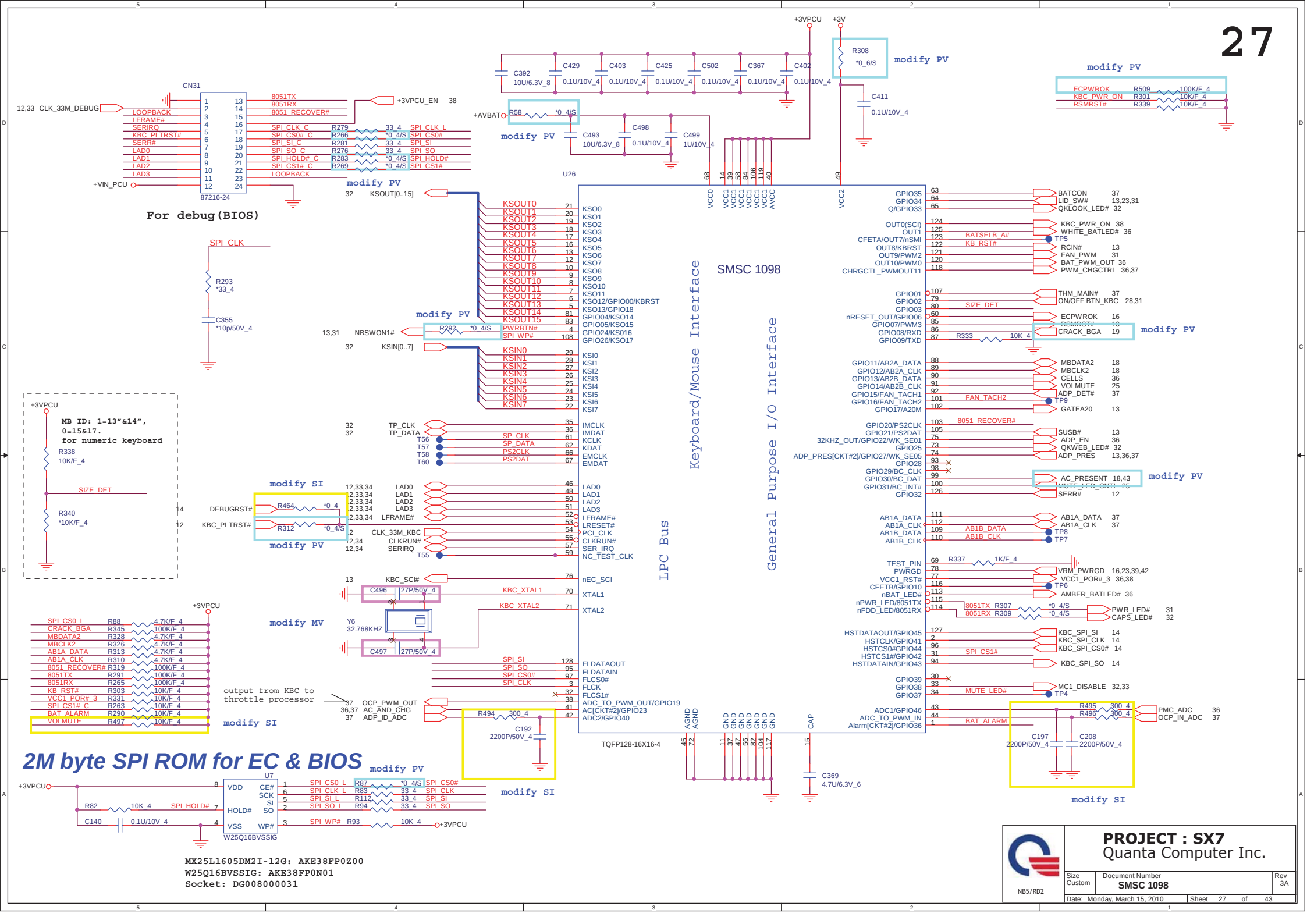
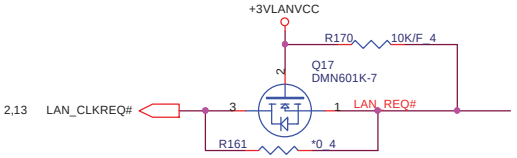
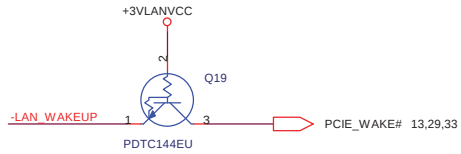
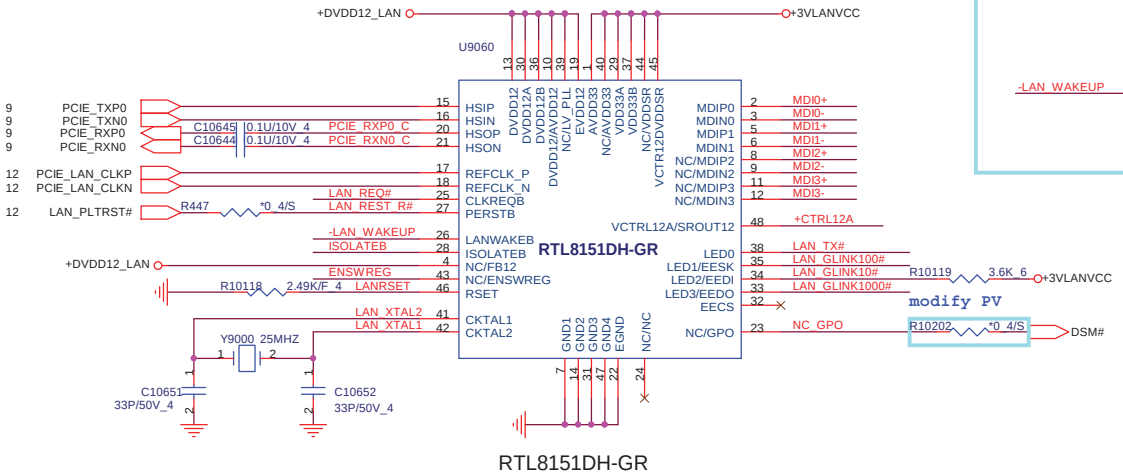

SMSC 1098
Keyboard/Mouse Interface
General Purpose I/O Interface
LPC Bus
TQFP128-16X16-4
U26
CN31
87216-24
For debug(BIOS)
modify PV
modify SI
modify MV
+3VPCU
+3V
+AVBAT
+VIN_PCU
+3VPCU_EN
SPI_CLK
MB ID: 1=13"&14", 0=15&17. for numeric keyboard
output from KBC to throttle processor
2M byte SPI ROM for EC & BIOS
W25Q16BVSSIG
MX25L1605DM2I-12G: AKE38FP0Z00
W25Q16BVSSIG: AKE38FP0N01
Socket: DG008000031
PROJECT : SX7
Quanta Computer Inc.
NB5/RD2
Size Custom
Document Number SMSC 1098
Rev 3A
Date: Monday, March 15, 2010
Sheet 27 of 43

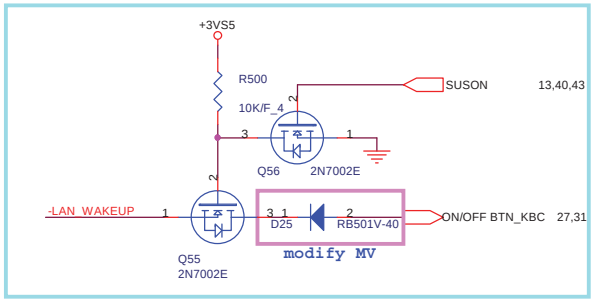
modify DB2

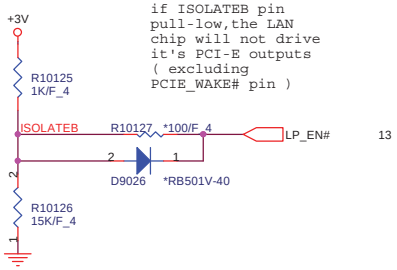




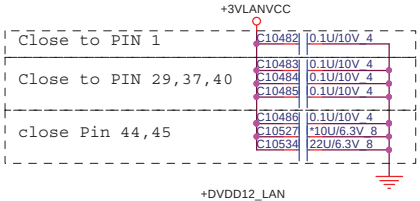


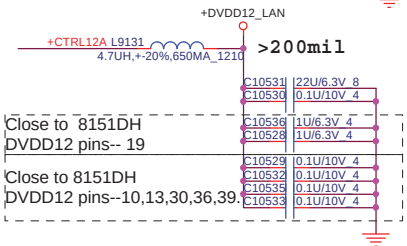
modify PV



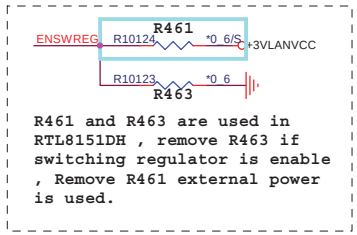


if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

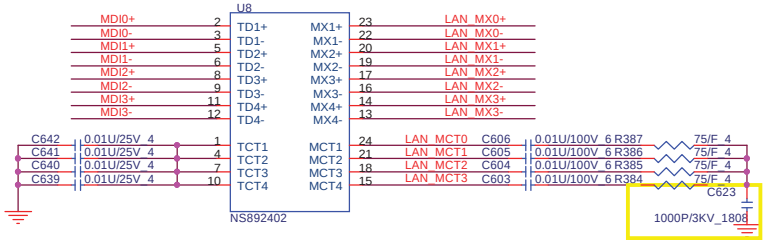




modify PV



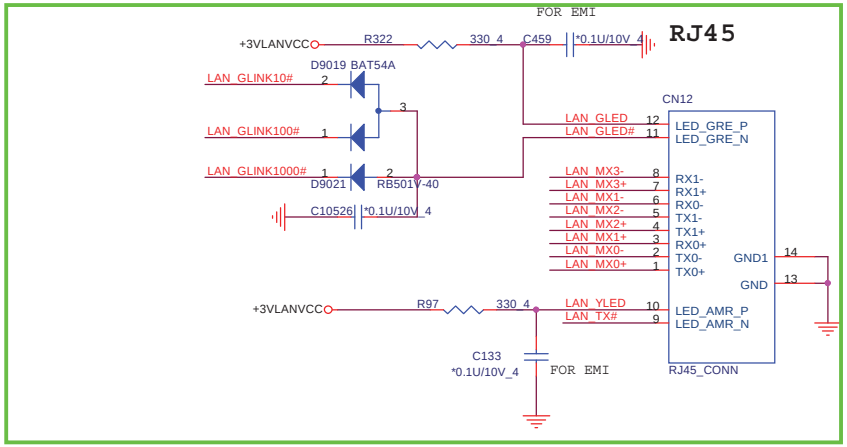
Transformer for 10/100/1000



modify SI

Lan Con.

modify DB2



43 +3VLANVCC
2,3,5,6,7,10,11,12,13,14,15,16,20,23,25,27,29,30,31,32,33,34,35,37,43 +3V

NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN RTL8151/RJ45	3A
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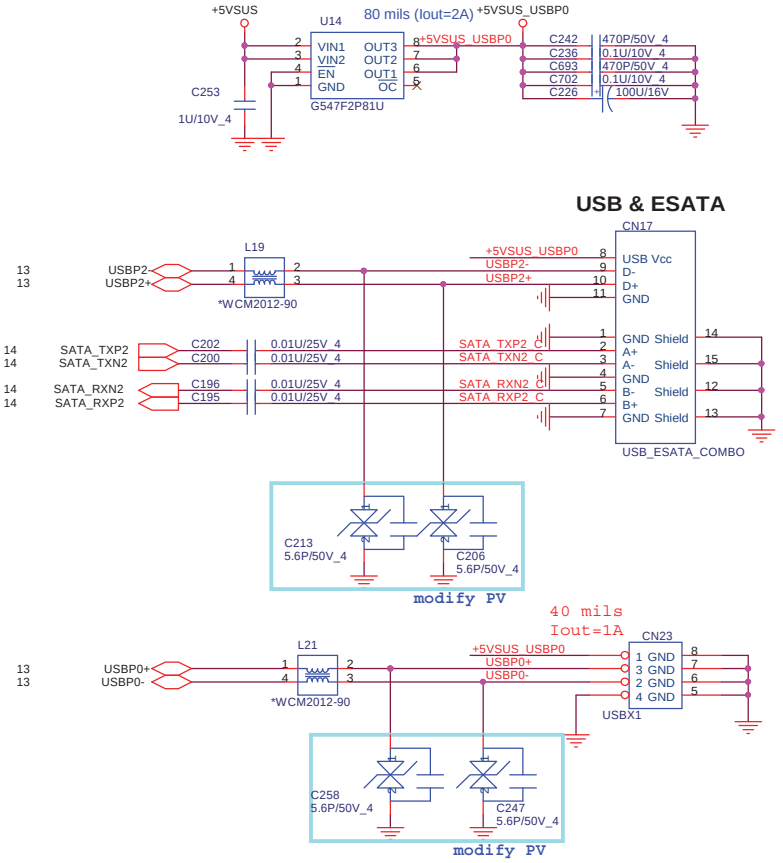
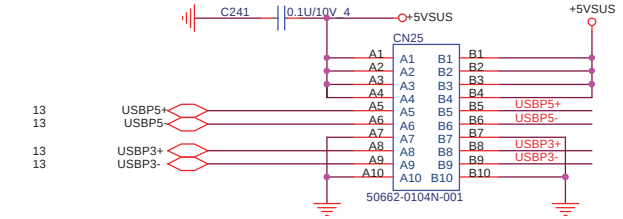
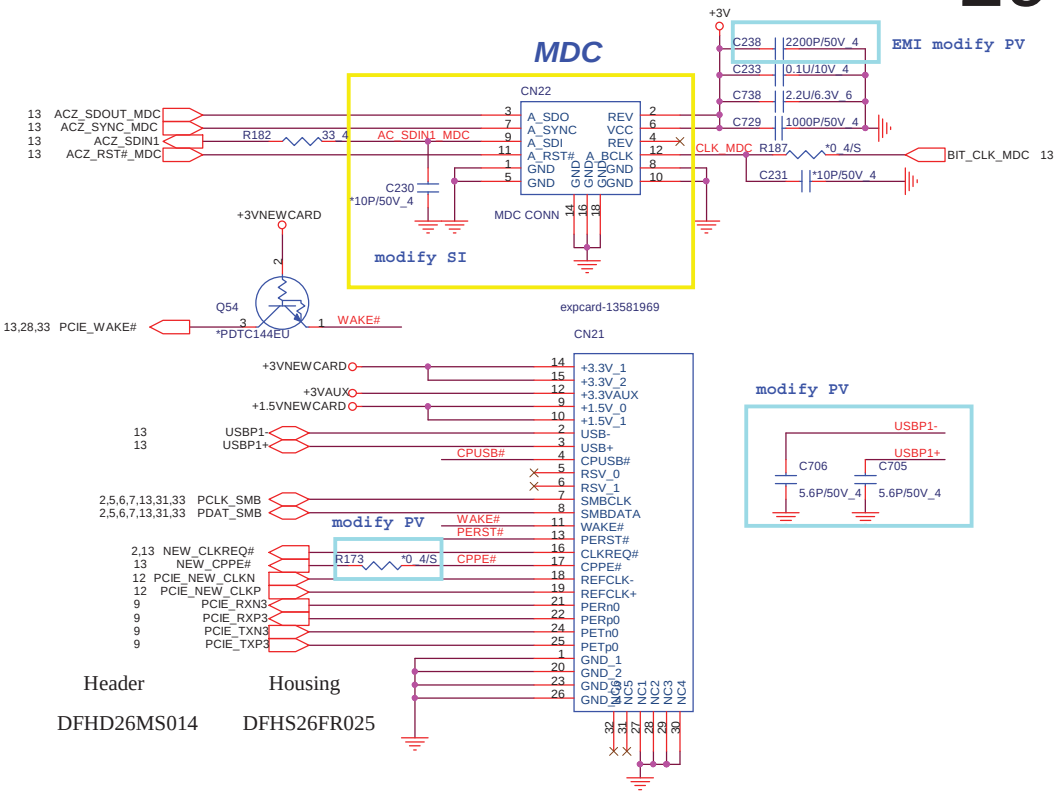
LEFT SIDE USBX1 and E-SATA/USB COMBO



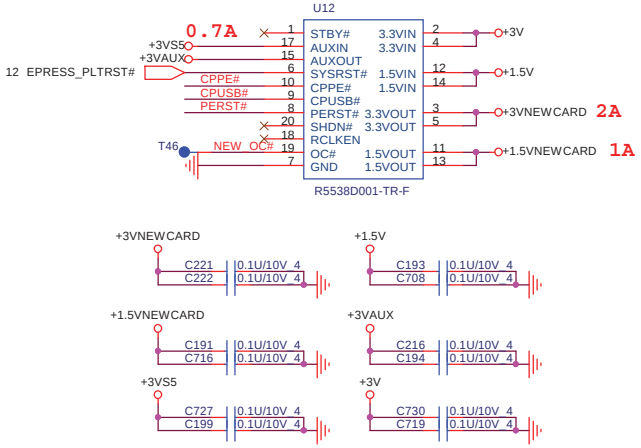
RIGHT SIDE USBX2



Modem CONN



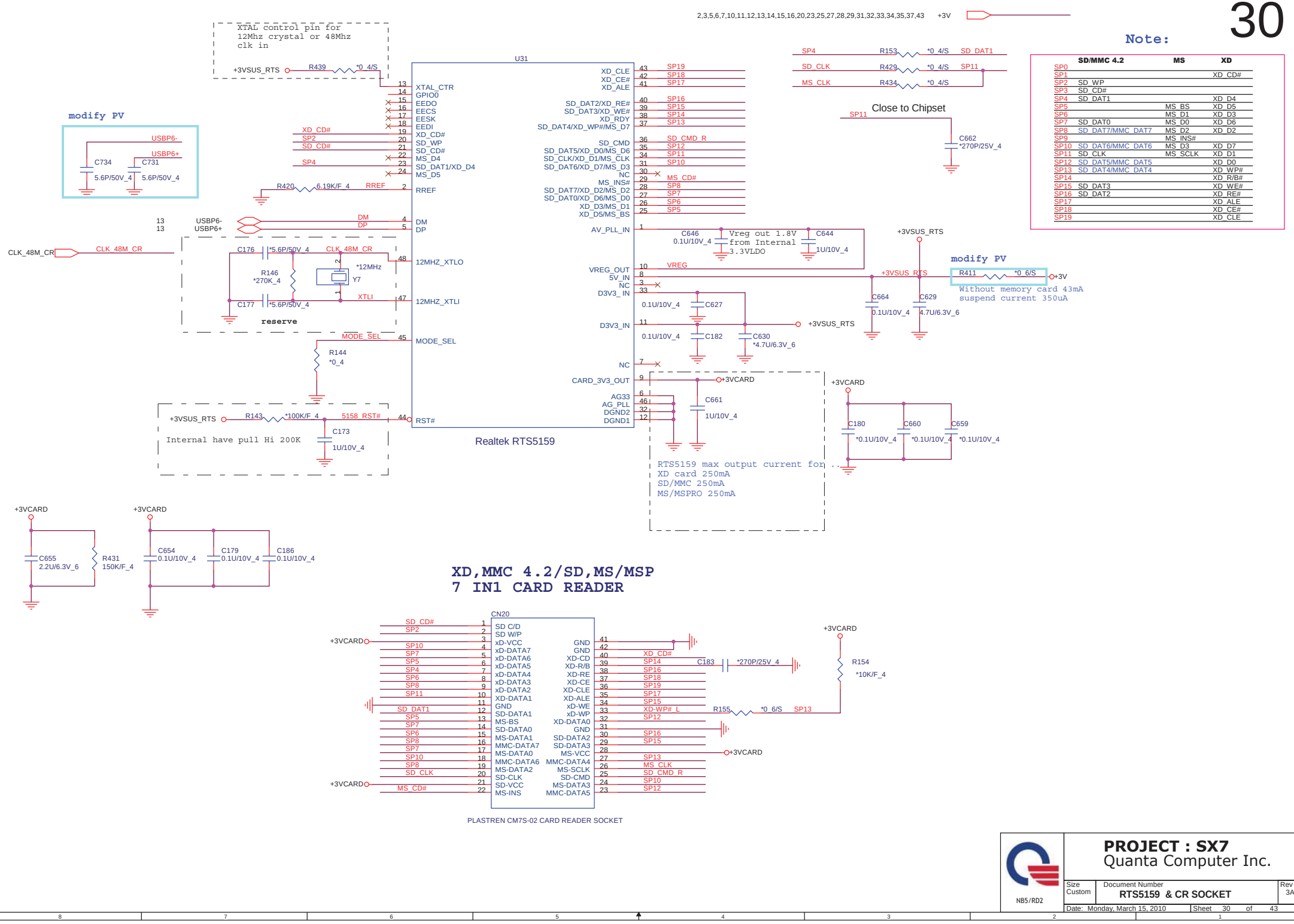
NEWCARD (PCIEXPRESS*1 + USB*1)



NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EXTERNAL USB X2	3A
Date: Monday, March 15, 2010	Sheet 29 of 43	


2,3,5,6,7,10,11,12,13,14,15,16,20,23,25,27,28,29,31,32,33,34,35,37,43 +3V
Note:
SD/MMC 4.2 MS XD
SP0
SP1 XD_CD#
SP2 SD_WP
SP3 SD_CD#
SP4 SD_DAT1 XD_D4
SP5 MS_BS XD_D5
SP6 MS_D1 XD_D3
SP7 SD_DAT0 MS_D0 XD_D6
SP8 SD_DAT7/MMC_DAT7 MS_D2 XD_D2
SP9 MS_INS#
SP10 SD_DAT6/MMC_DAT6 MS_D3 XD_D7
SP11 SD_CLK MS_SCLK XD_D1
SP12 SD_DAT5/MMC_DAT5 XD_D0
SP13 SD_DAT4/MMC_DAT4 XD_WP#
SP14 XD_R/B#
SP15 SD_DAT3 XD_WE#
SP16 SD_DAT2 XD_RE#
SP17 XD_ALE
SP18 XD_CE#
SP19 XD_CLE
XTAL control pin for 12Mhz crystal or 48Mhz clk in
+3VSUS_RTS R439 *0_4/S
U31
XTAL_CTR GPIO0 EEDO EECS EESK EEDI XD_CD# SD_WP SD_CD# MS_D4 SD_DAT1/XD_D4 MS_D5 RREF DM DP 12MHZ_XTLO 12MHZ_XTLI MODE_SEL RST#
XD_CLE XD_CE# XD_ALE SD_DAT2/XD_RE# SD_DAT3/XD_WE# XD_RDY SD_DAT4/XD_WP#/MS_D7 SD_CMD SD_DAT5/XD_D0/MS_D6 SD_CLK/XD_D1/MS_CLK SD_DAT6/XD_D7/MS_D3 NC MS_INS# SD_DAT7/XD_D2/MS_D2 SD_DAT0/XD_D6/MS_D0 XD_D3/MS_D1 XD_D5/MS_BS AV_PLL_IN VREG_OUT 5V_IN NC D3V3_IN D3V3_IN NC CARD_3V3_OUT AG33 AG_PLL DGND2 DGND1
SD_CD# SP2 SD_CD# SP4
R420 6.19K/F_4 RREF
USBP6- USBP6+ DM DP
CLK_48M_CR CLK_48M_CR
C176 *5.6P/50V_4 CLK_48M_CR
R146 *270K_4 *12MHz Y7
C177 *5.6P/50V_4 XTLI
reserve
MODE_SEL R144 *0_4
+3VSUS_RTS R143 *100K/F_4 5158_RST# C173 1U/10V_4
Internal have pull Hi 200K
Realtek RTS5159
SP4 R153 *0_4/S SD_DAT1
SD_CLK R429 *0_4/S SP11
MS_CLK R434 *0_4/S
Close to Chipset
SP11 C662 *270P/25V_4
C646 0.1U/10V_4 Vreg out 1.8V from Internal 3.3VLDO C644 1U/10V_4
C627 0.1U/10V_4
C182 0.1U/10V_4
C630 *4.7U/6.3V_6
+3VSUS_RTS
+3VSUS_RTS C664 0.1U/10V_4 C629 4.7U/6.3V_6
modify PV
R411 *0_6/S +3V
Without memory card 43mA
suspend current 350uA
+3VCARD C661 1U/10V_4
RTS5159 max output current for ..
XD card 250mA
SD/MMC 250mA
MS/MSPRO 250mA
+3VCARD C180 *0.1U/10V_4 C660 *0.1U/10V_4 C659 *0.1U/10V_4
modify PV
USBP6- USBP6+ C734 5.6P/50V_4 C731 5.6P/50V_4
+3VCARD C655 2.2U/6.3V_6 R431 150K/F_4
+3VCARD C654 0.1U/10V_4 C179 0.1U/10V_4 C186 0.1U/10V_4
XD,MMC 4.2/SD,MS/MSP
7 IN1 CARD READER
CN20
SD C/D SD W/P xD-VCC xD-DATA7 xD-DATA6 xD-DATA5 xD-DATA4 xD-DATA3 xD-DATA2 XD-DATA1 GND SD-DATA1 MS-BS SD-DATA0 MS-DATA1 MMC-DATA7 MS-DATA0 MMC-DATA6 MS-DATA2 SD-CLK SD-VCC MS-INS
GND GND XD-CD XD-R/B XD-RE XD-CE XD-CLE XD-ALE xD-WE xD-WP XD-DATA0 GND SD-DATA2 SD-DATA3 MS-VCC MMC-DATA4 MS-SCLK SD-CMD MS-DATA3 MMC-DATA5
SD_CD# SP2 +3VCARD SP10 SP7 SP5 SP4 SP6 SP8 SP11 SD_DAT1 SP5 SP7 SP6 SP8 SP7 SP10 SP8 SD_CLK +3VCARD MS_CD#
XD_CD# SP14 SP16 SP18 SP19 SP17 SP15 XD-WP# L SP12 SP16 SP15 +3VCARD SP13 MS_CLK SD_CMD_R SP10 SP12
C183 *270P/25V_4
R155 *0_6/S SP13
+3VCARD R154 *10K/F_4
PLASTREN CM7S-02 CARD READER SOCKET
NB5/RD2
PROJECT : SX7
Quanta Computer Inc.
Size Custom
Document Number RTS5159 & CR SOCKET
Rev 3A
Date: Monday, March 15, 2010
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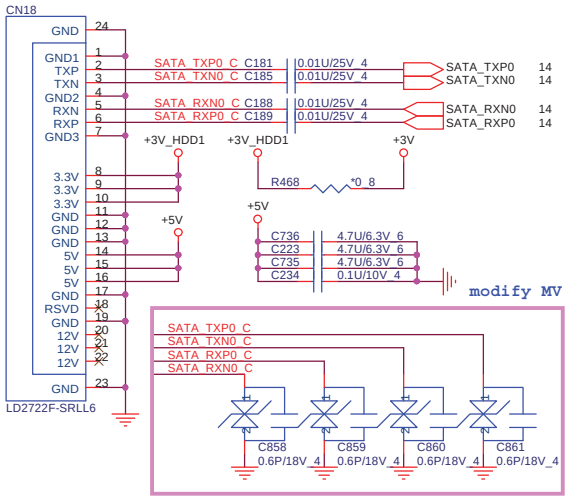
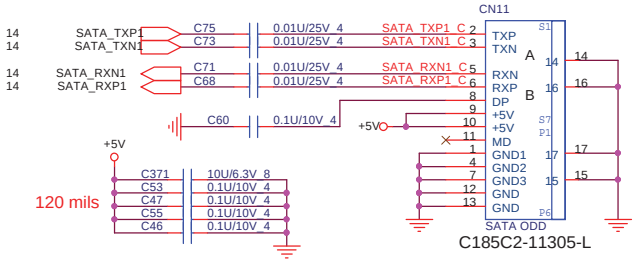
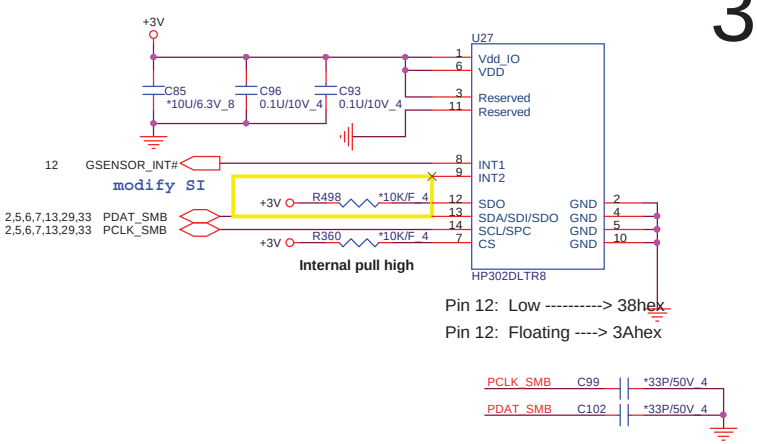
SATA HDD CONNECTOR



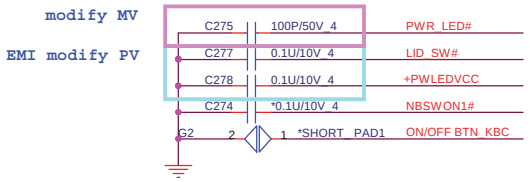
SATA CD-ROM



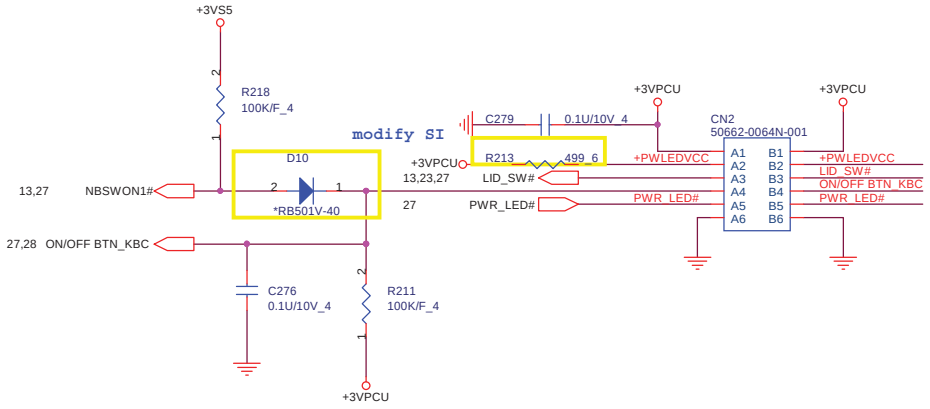
Accelerometer Sensor



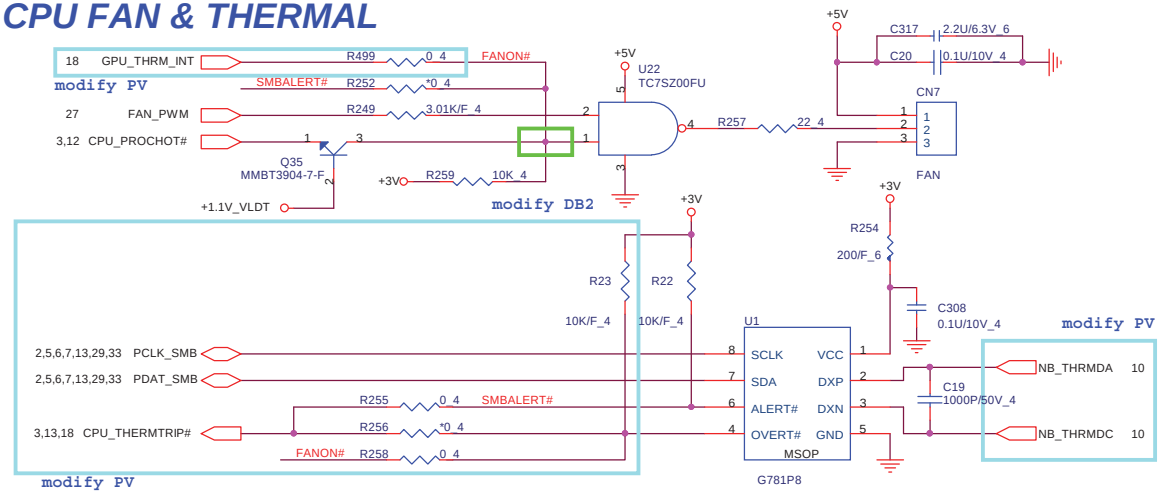
POWER BOTTON CONNECT



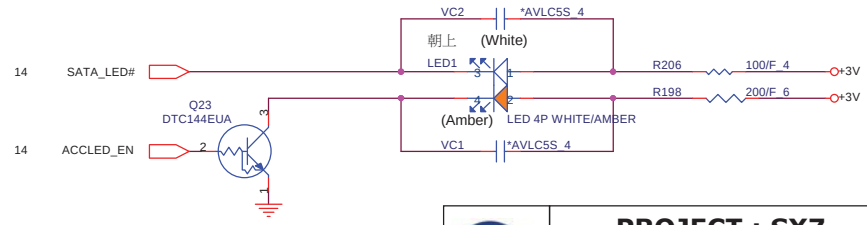
1. +3VPCU(LIDSWITCH PWR)
2. +PWLEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND



CPU FAN & THERMAL



LED



NB5/RD2

PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ESATA/HDD/ODD/LED/FAN	3A
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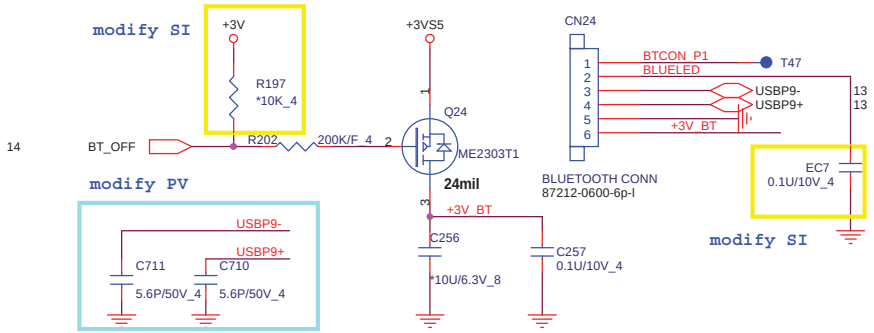
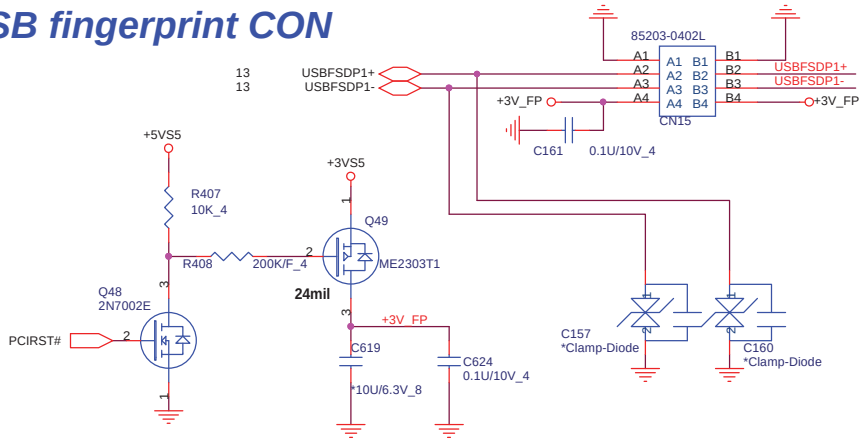
BLUETOOTH

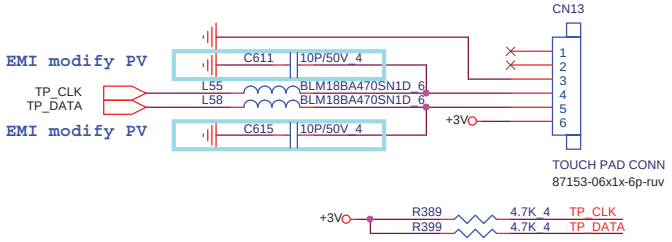


USB fingerprint CON

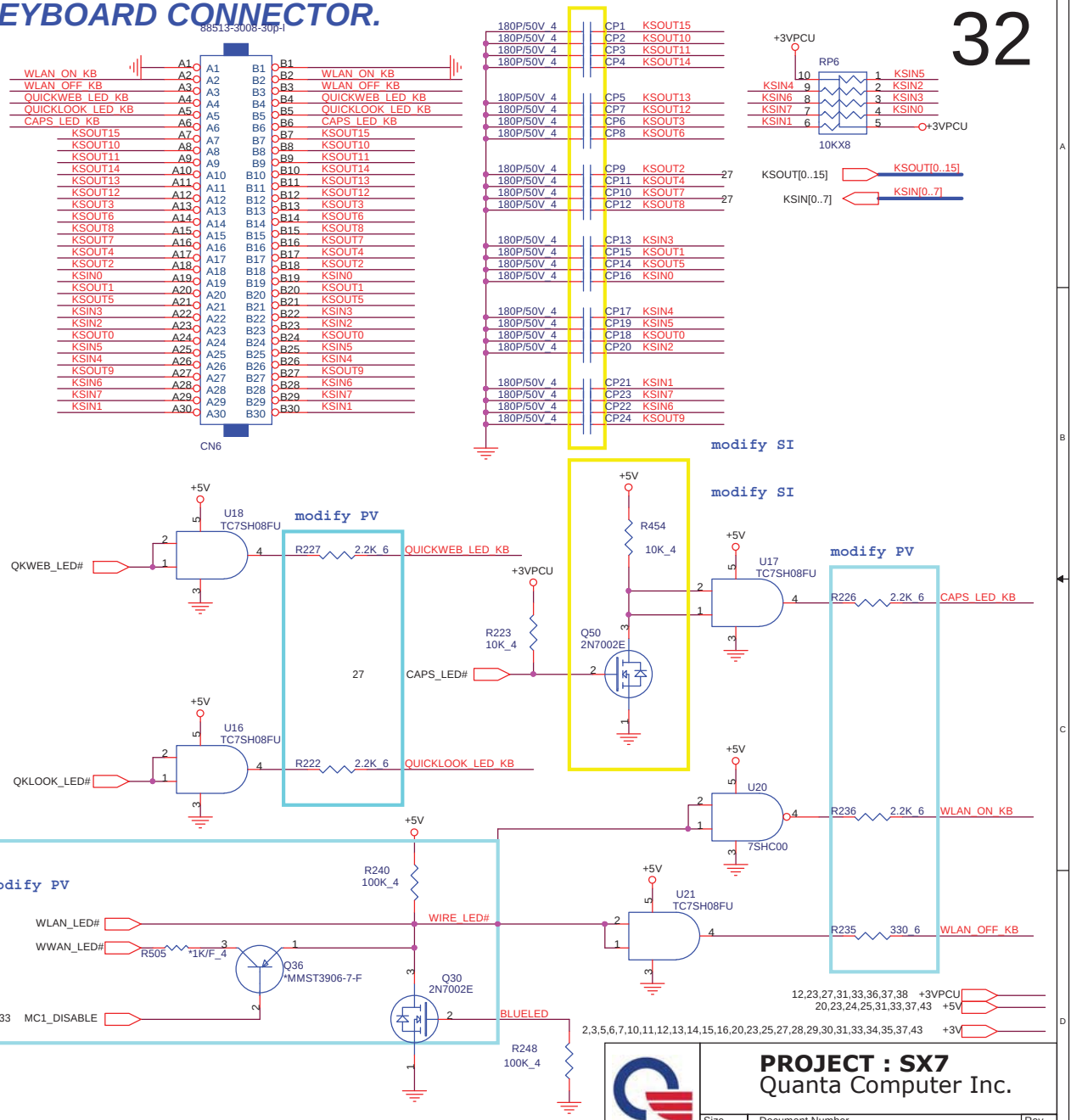


TOUCH PAD CONNECTOR

Pin1	VDD
Pin2	DATA
Pin3	CLK
Pin4	GND
Pin5	X
Pin6	X



KEYBOARD CONNECTOR.



PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/WC/FT/ESATA/USB/LED	3A

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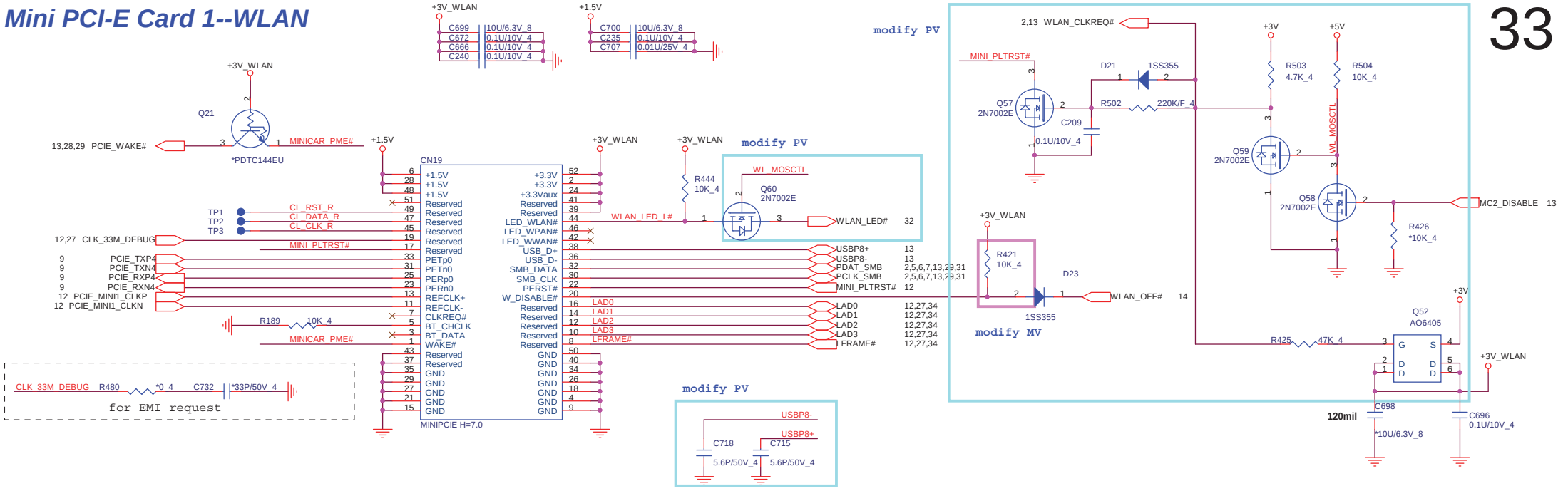
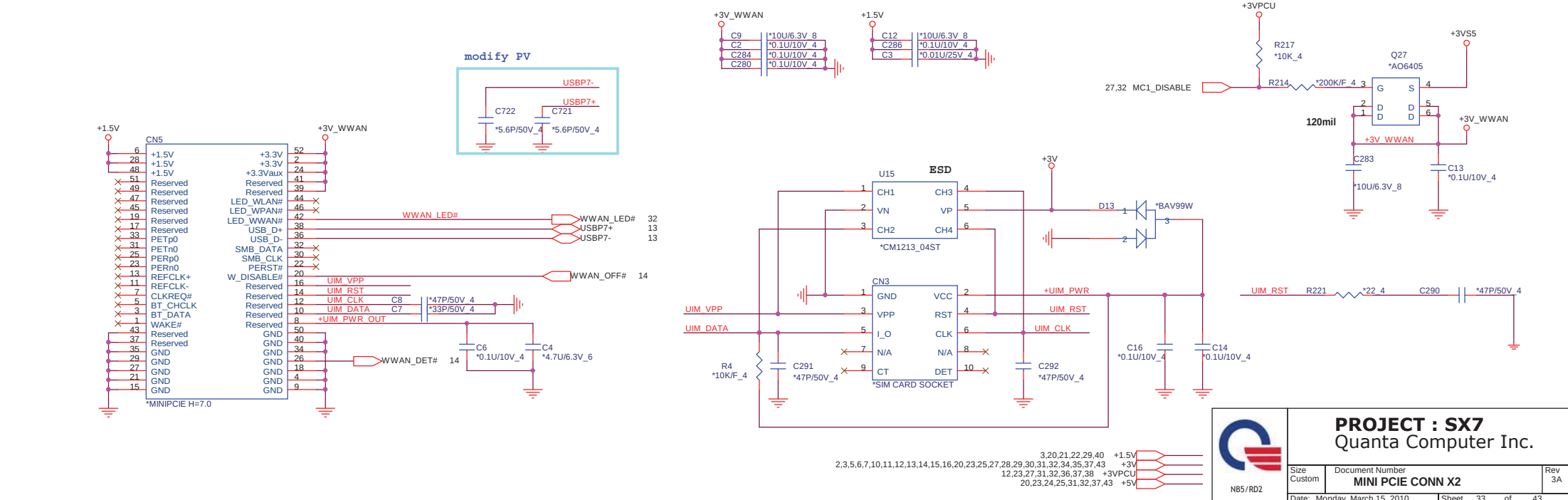
NB5/RD2

Mini PCI-E Card 1--WLAN



Mini PCI-E Card 2 --WWAN



PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN X2	3A
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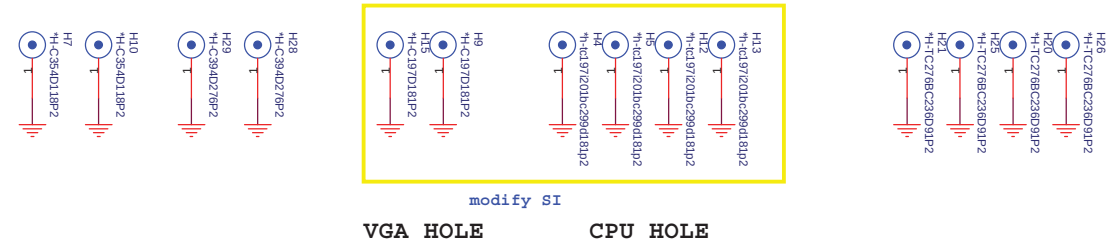
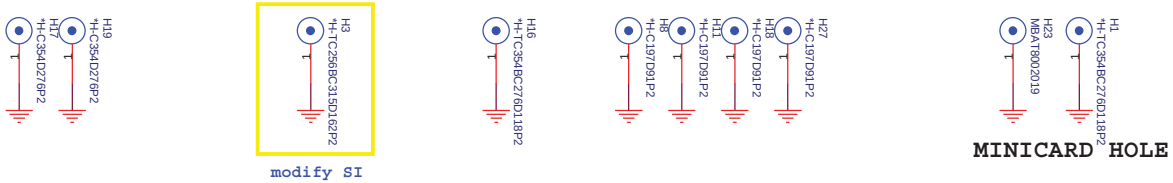
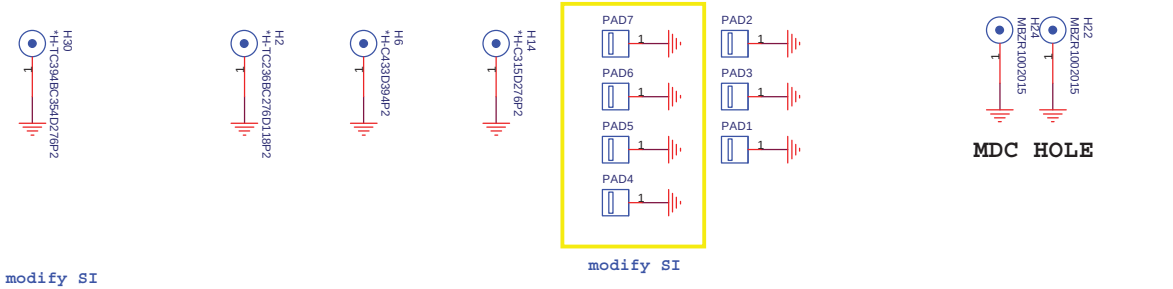
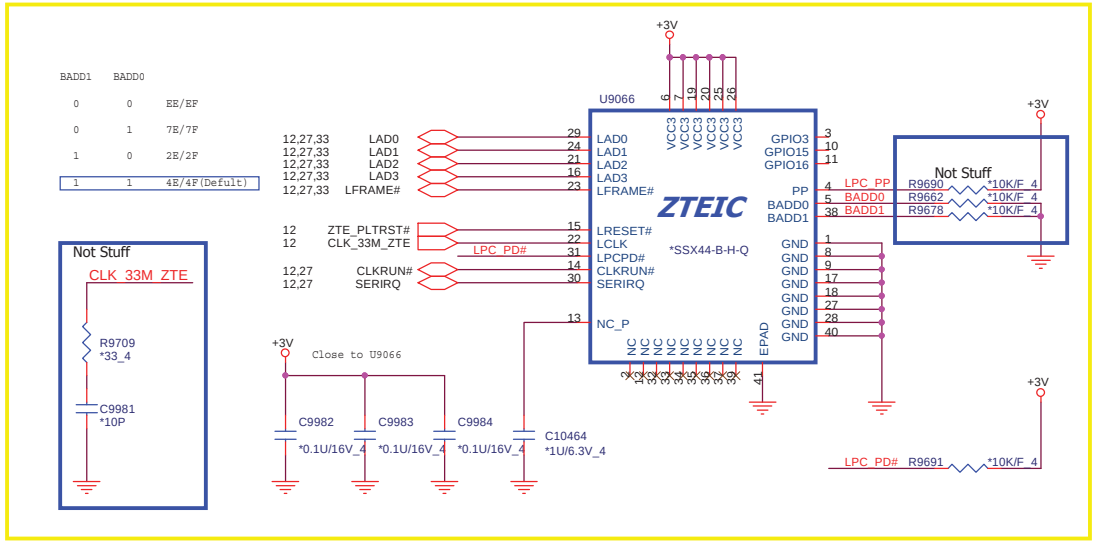
NB5/RD2









PROJECT : SX7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hole, Nuts	3A
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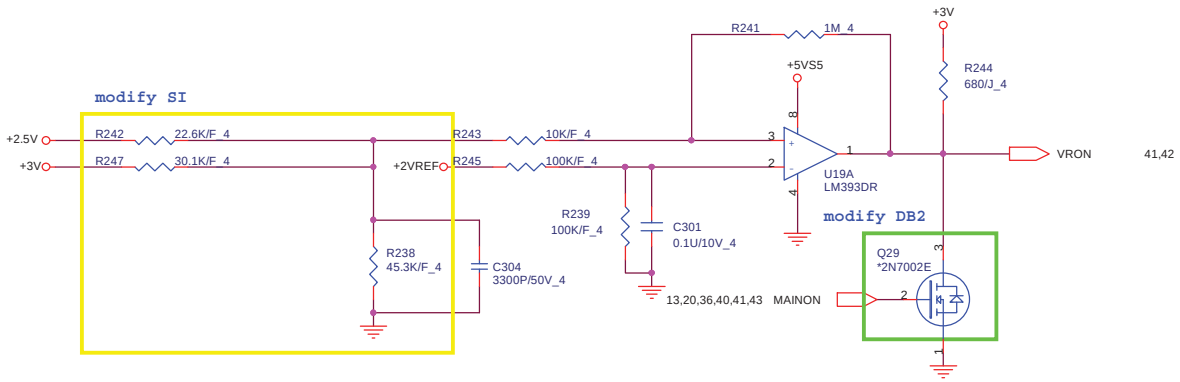
NB5/RD2



NB5/RD2	**PROJECT : SX7** Quanta Computer Inc.	
Size: Custom	Document Number: **POWER Sequance**	Rev: 3A
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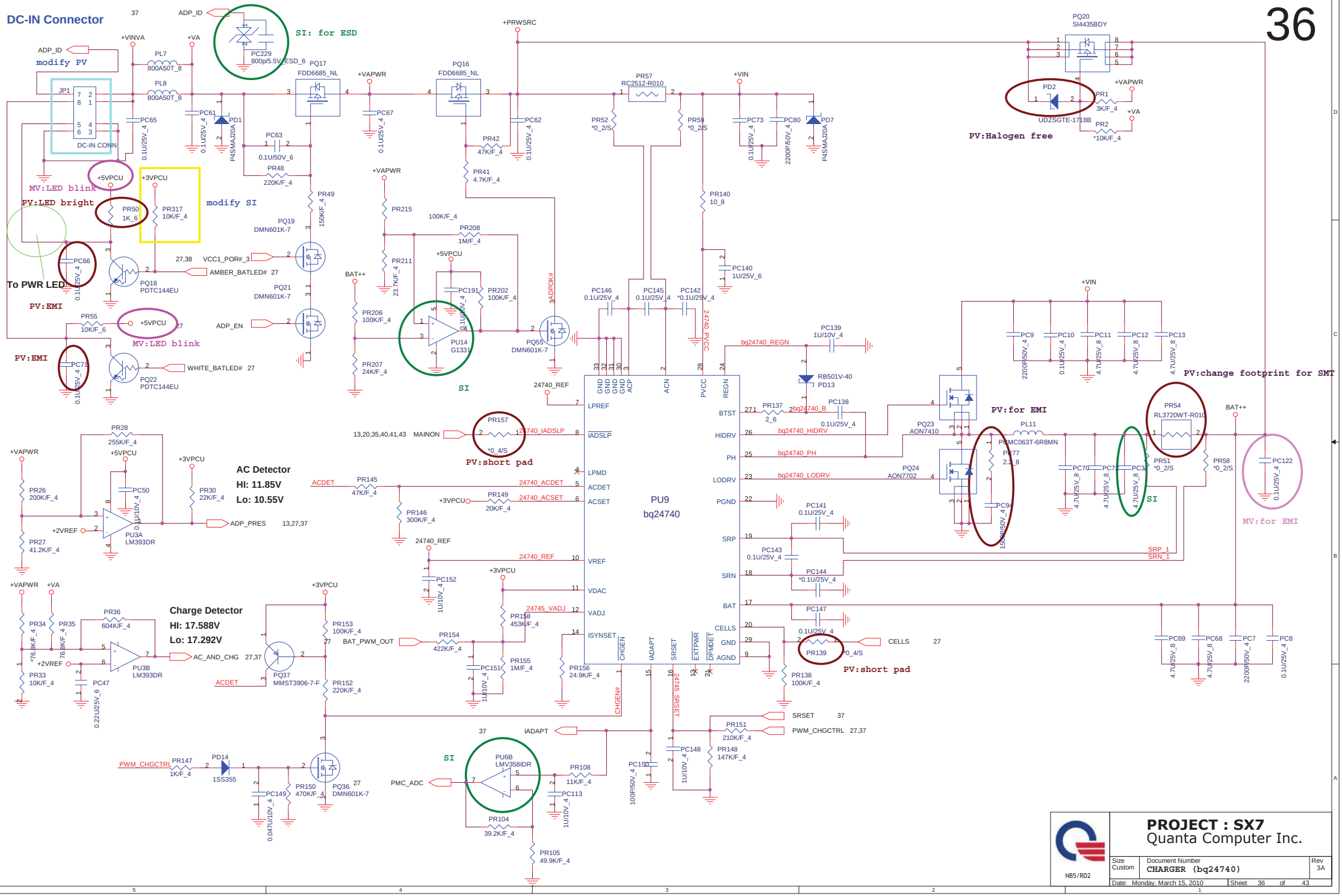
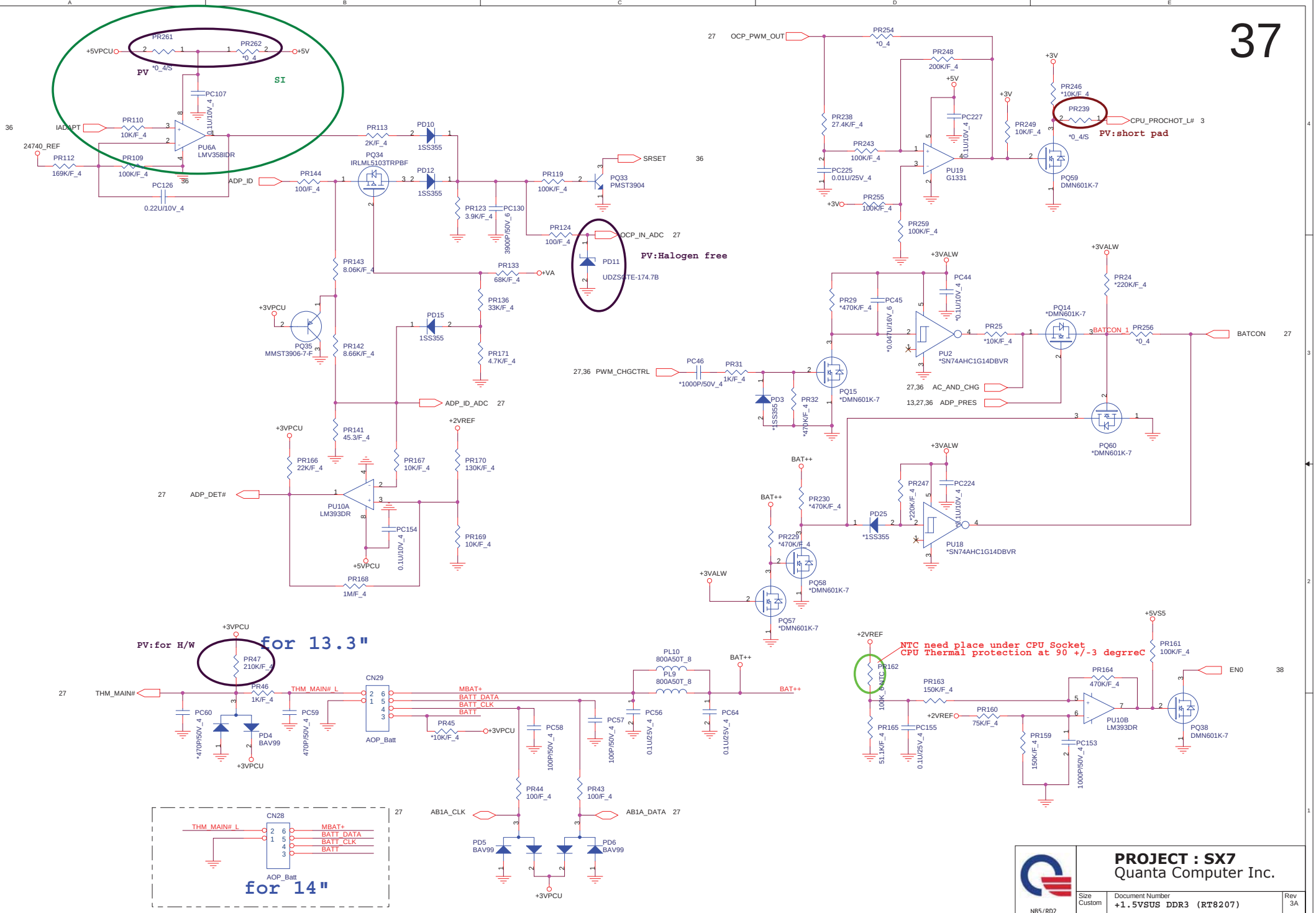

DC-IN Connector
SI: for ESD
modify PV
MV:LED blink
PV:LED bright
modify SI
To PWR LED
PV:EMI
PV:short pad
AC Detector
HI: 11.85V
Lo: 10.55V
Charge Detector
HI: 17.588V
Lo: 17.292V
PU9
bq24740
SI
PV:Halogen free
PV:for EMI
PV:change footprint for SMT
MV:for EMI
PROJECT : SX7
Quanta Computer Inc.
CHARGER (bq24740)
NB5/RD2
Monday, March 15, 2010



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Custom	+1.5VSUS DDR3 (RT8207)	3A
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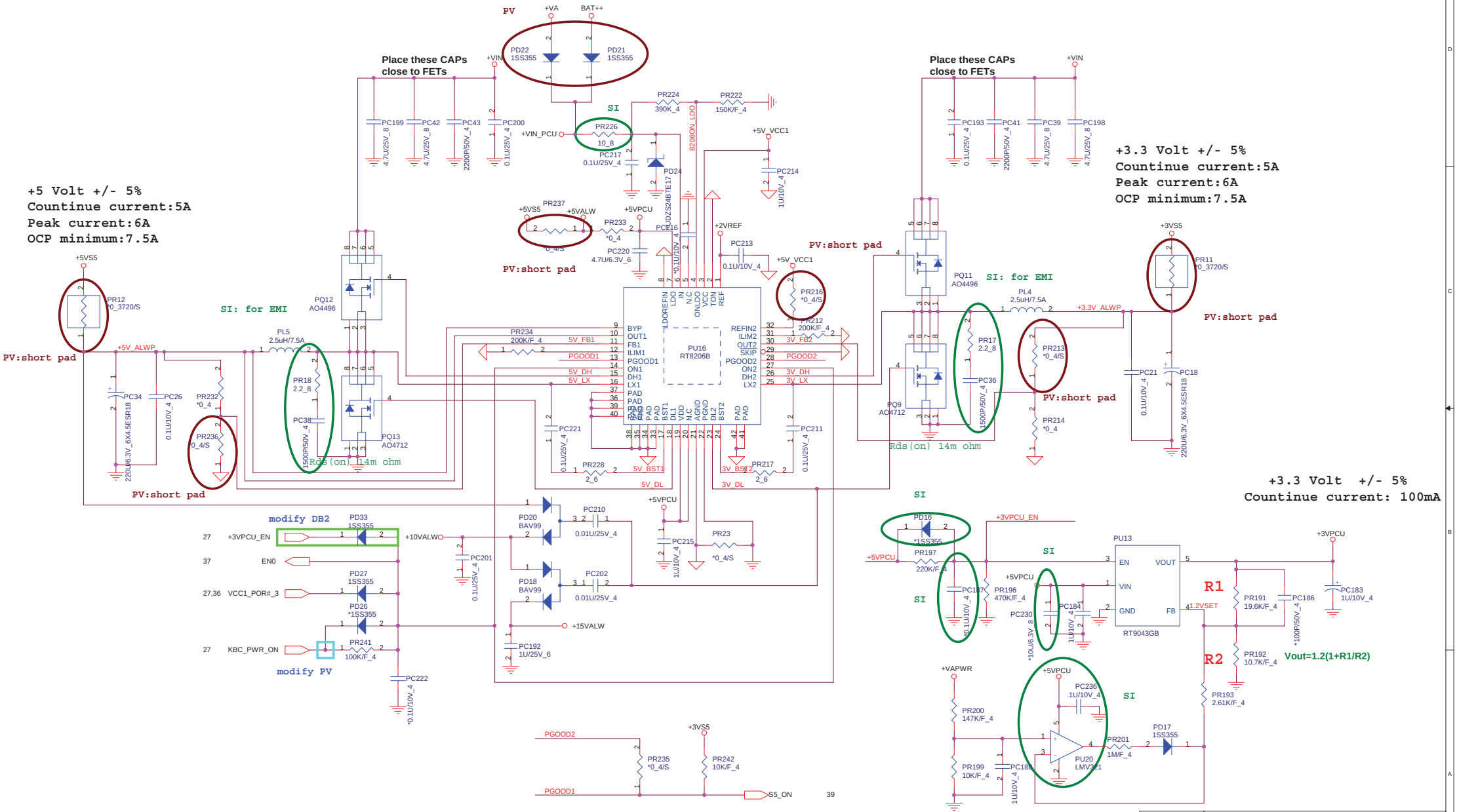
NB5/RD2

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

+5 Volt +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current: 100mA



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Size	Document Number	Rev
Custom	+5V/+3V (RT8206B)	3A
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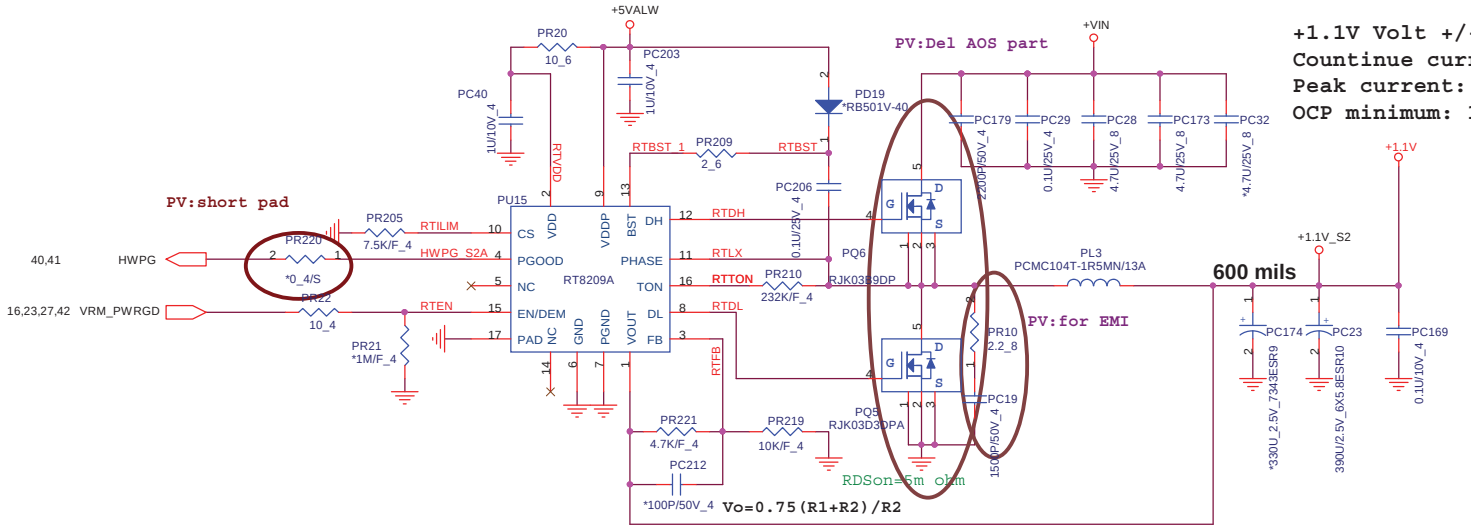
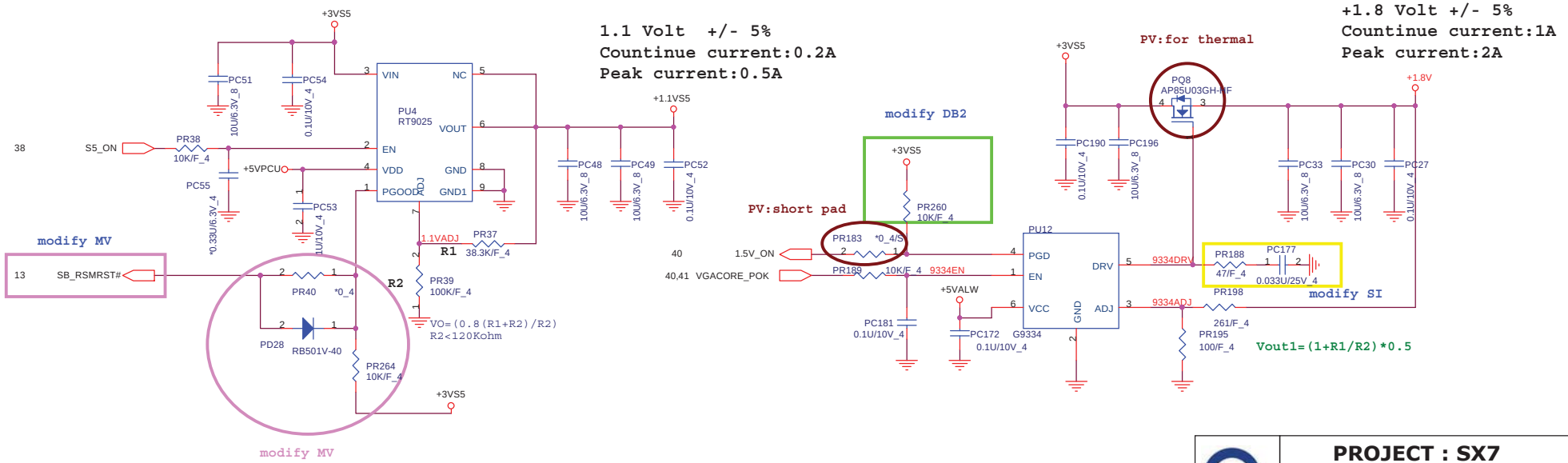
NB5/RD2





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NB5/RD2

Size	Document Number	Rev
Custom	VGA Core/+1.8VGFX/1.0VGFX	3A

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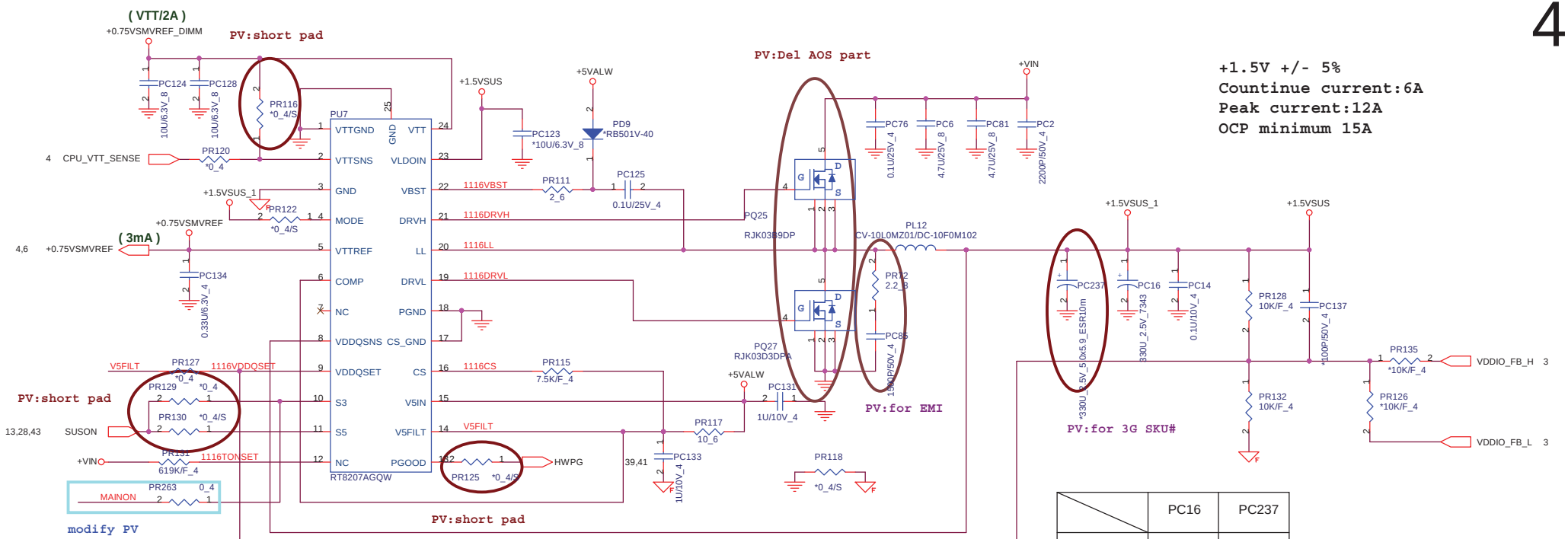
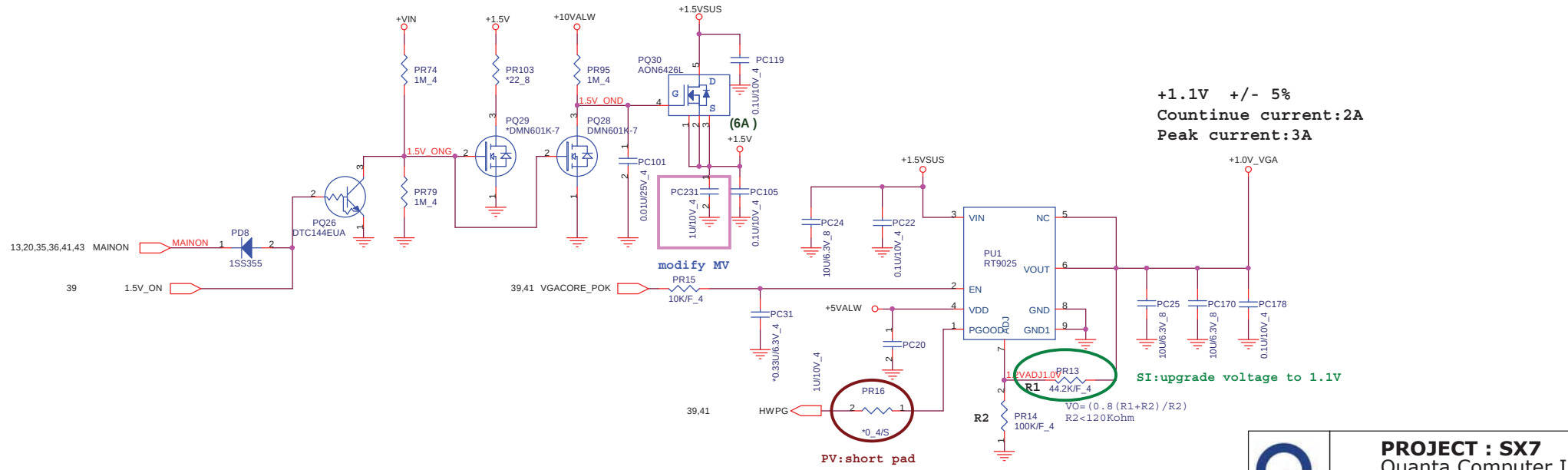


	PC16	PC237
For 3G sku	**Stuff**	NC
non 3G sku	NC	**Stuff**



NB5/RD2	**PROJECT : SX7** Quanta Computer Inc.		
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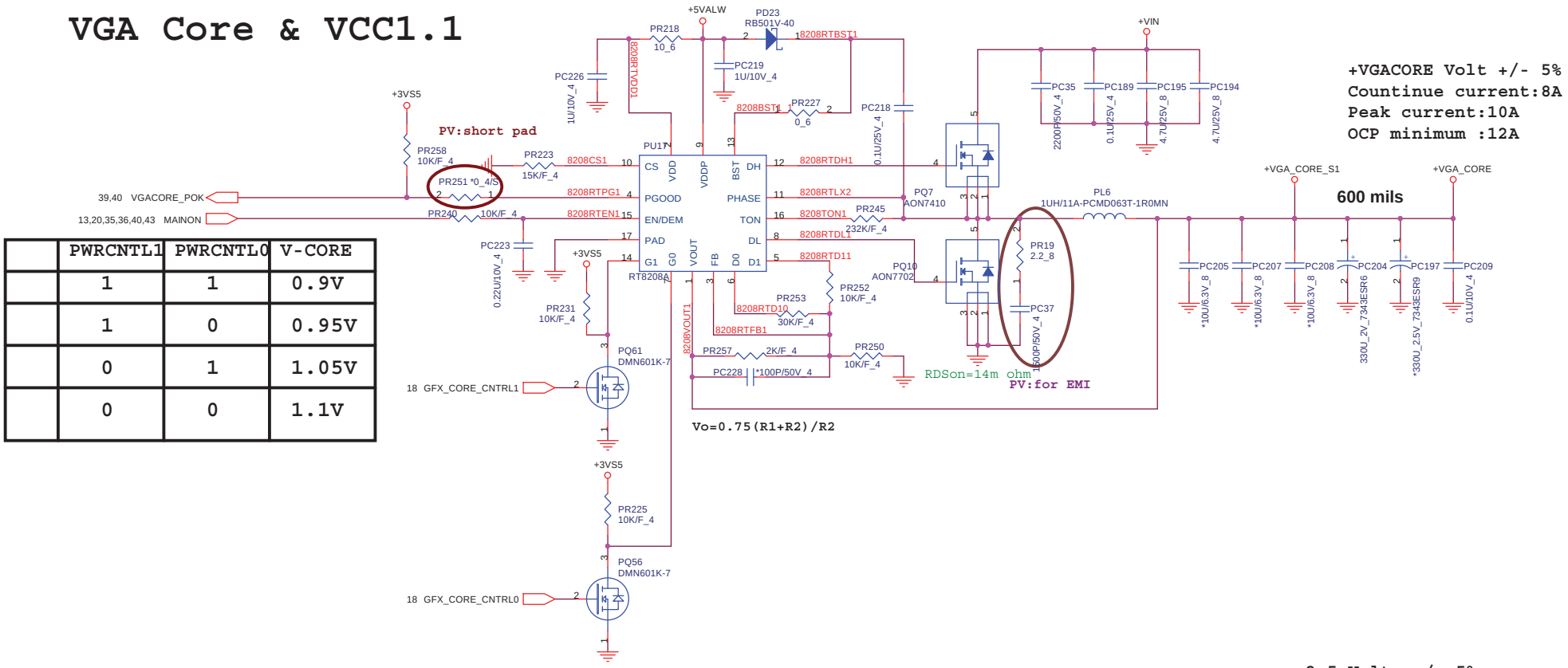
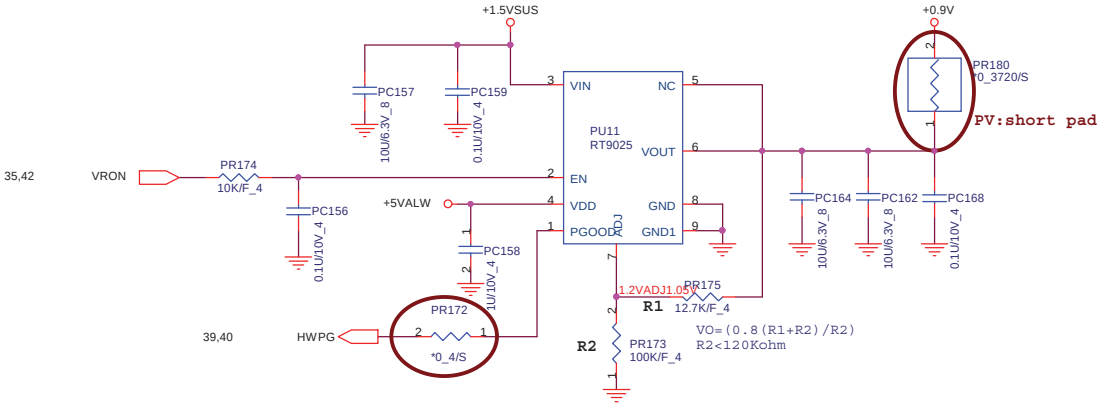
VGA Core & VCC1.1

	PWRCNTL1	PWRCNTL0	V-CORE
	1	1	0.9V
	1	0	0.95V
	0	1	1.05V
	0	0	1.1V

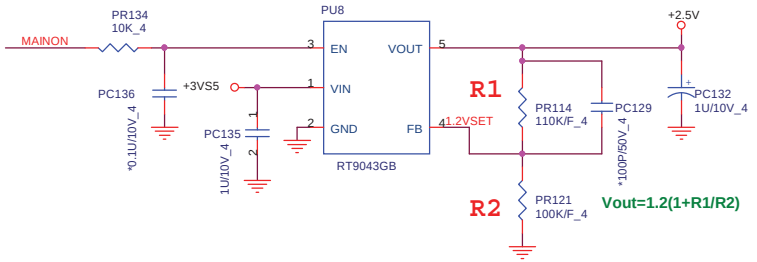


+VGACORE Volt +/- 5%
Countinue current:8A
Peak current:10A
OCP minimum :12A

+0.9V +/- 5%
Countinue current:1.5A
Peak current:2A



+2.5 Volt +/- 5%
Countinue current: 200mA
Peak current: 600mA



NB5/RD2

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Size	Document Number	Rev
Custom	VGA Core/+1.8VGFX/1.0VGFX	3A

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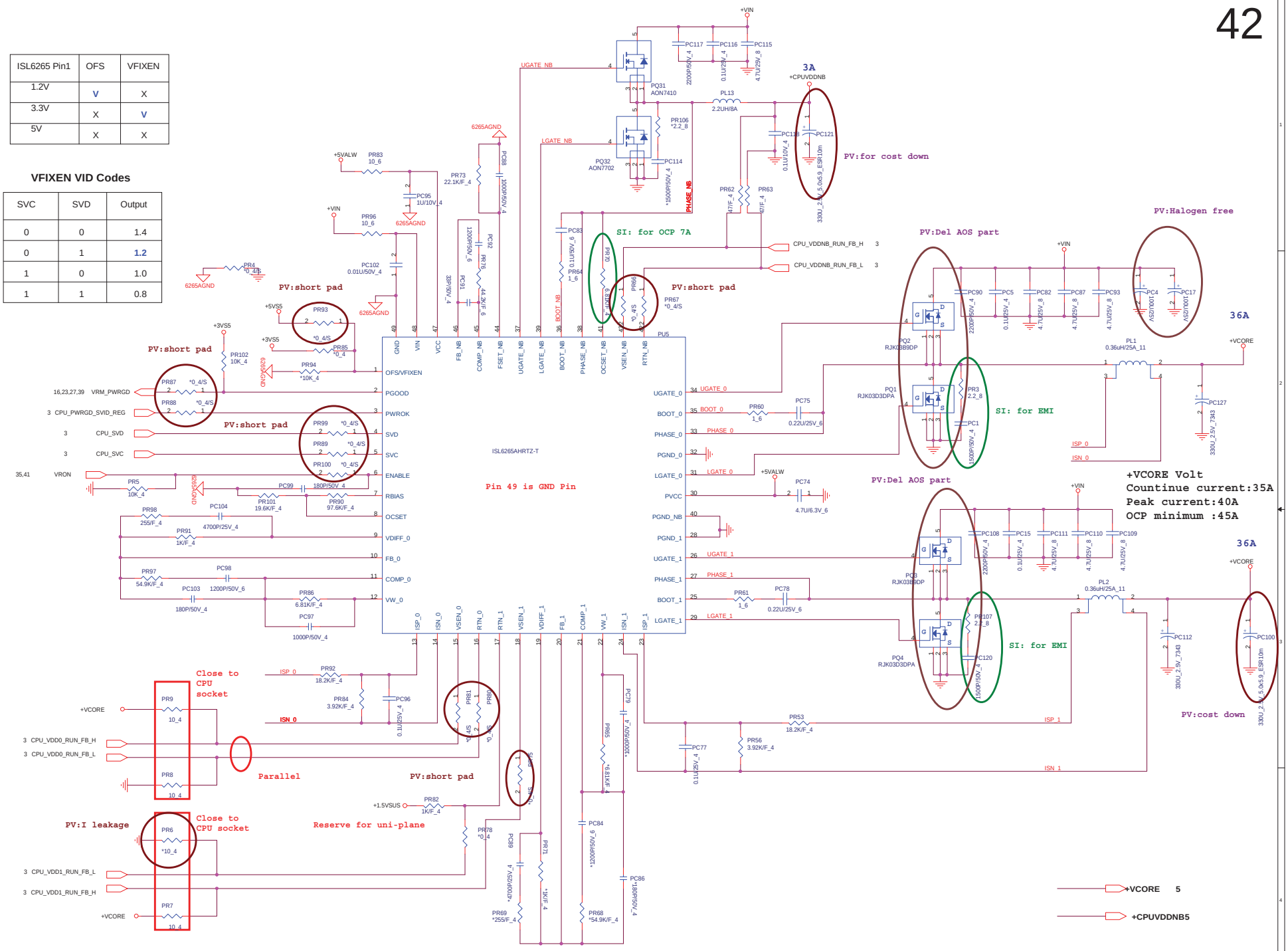
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



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NB5/RD2	Size: C	Document Number: CPU_CORE(ISL6265)	Rev: 3A
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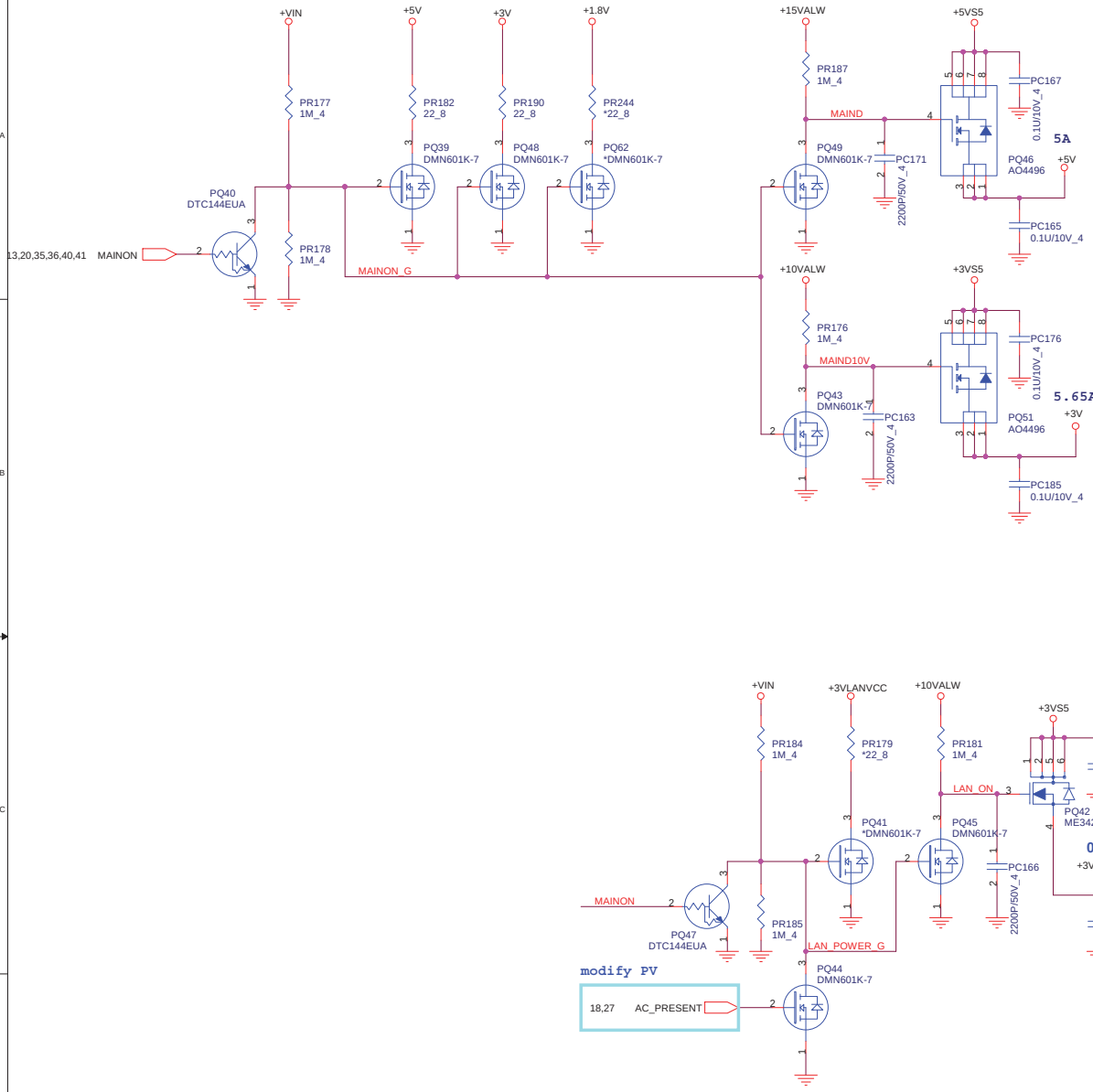

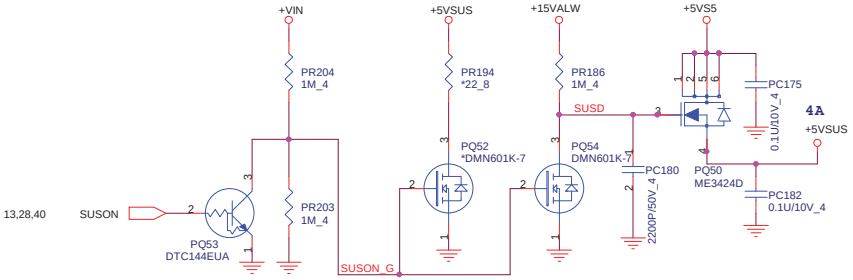

NB5/RD2	**PROJECT : SX7** Quanta Computer Inc.	
	Size: Custom Document Number: **DISCHARGE/3VS5/5VS5/LAN**	Rev: 3A
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