

KN3 BLOCK DIAGRAM

01

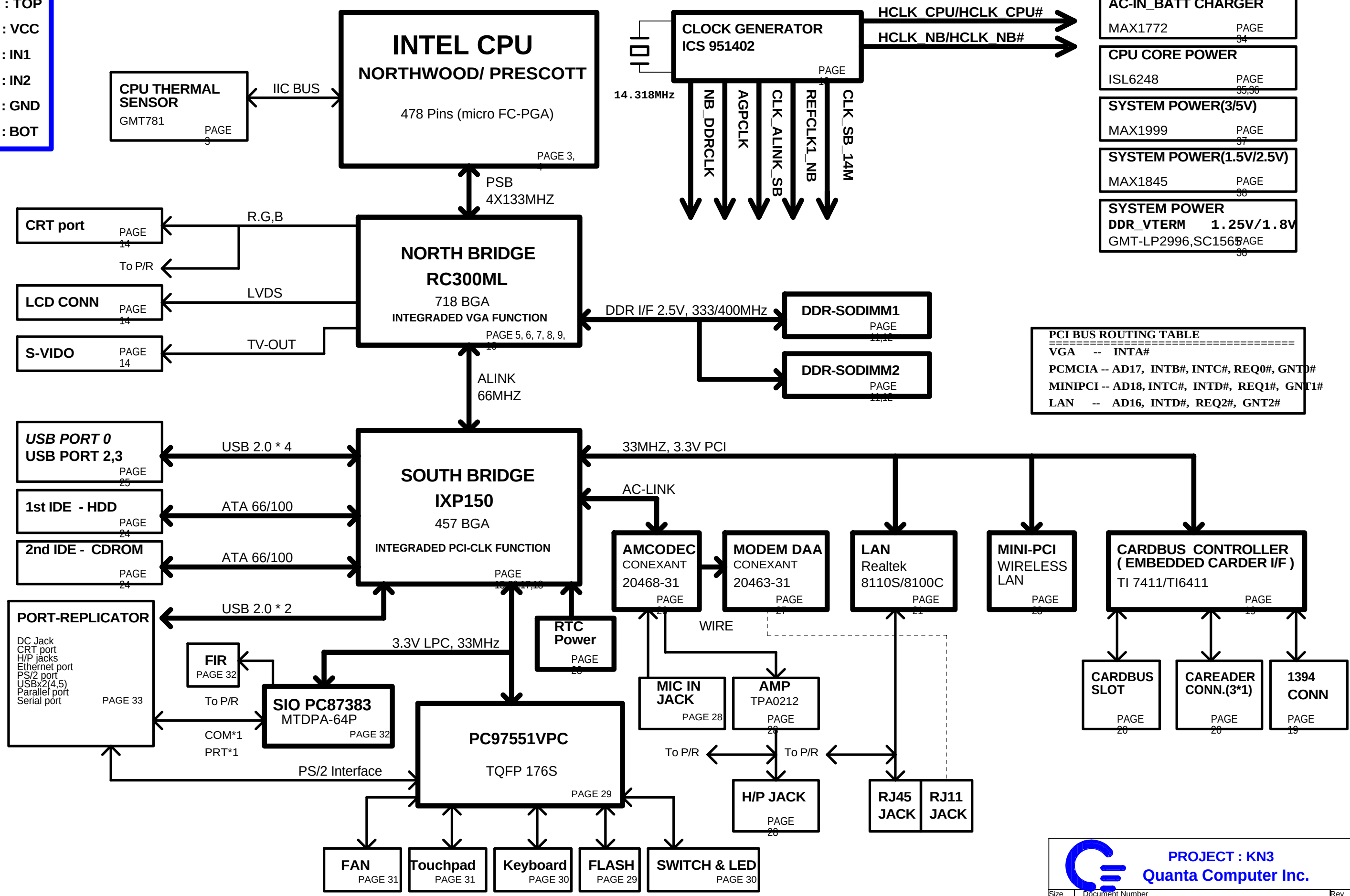
NORTHWOOD-PRESCOTT/RC300ML/IXP150

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : VCC
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : GND
- LAYER 6 : BOT

POWER-SOURCE CONTROL

- AC-IN_BATT CHARGER
MAX1772 PAGE 34
- CPU CORE POWER
ISL6248 PAGE 35,36
- SYSTEM POWER(3/5V)
MAX1999 PAGE 37
- SYSTEM POWER(1.5V/2.5V)
MAX1845 PAGE 38
- SYSTEM POWER
DDR_VTERM 1.25V/1.8V
GMT-LP2996,SC1565 PAGE 38



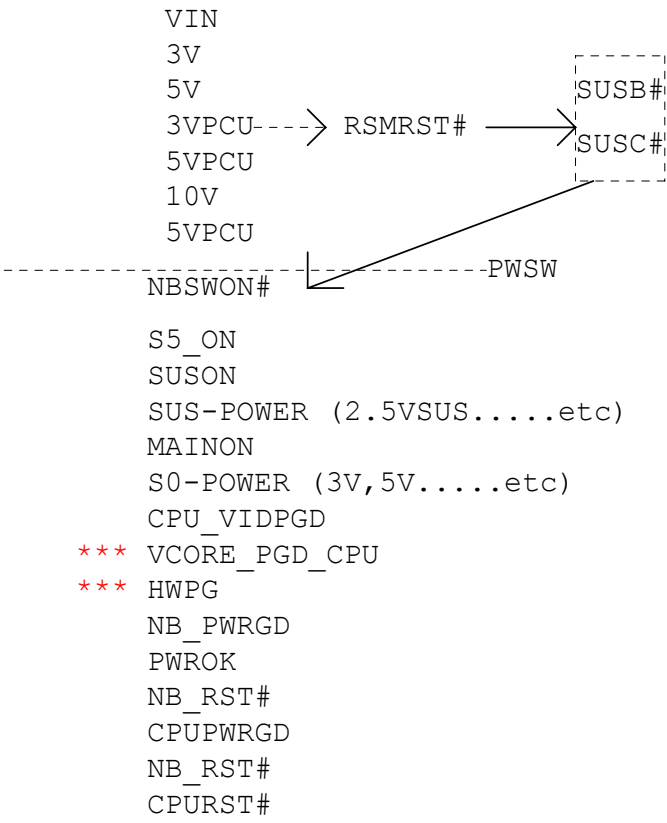
PCI BUS ROUTING TABLE

VGA	--	INTA#
PCMCIA	--	AD17, INTB#, INTC#, REQ0#, GNT0#
MINIPCI	--	AD18, INTC#, INTD#, REQ1#, GNT1#
LAN	--	AD16, INTD#, REQ2#, GNT2#

Voltage Rails	Core voltage for Processor	ON S0-S1	ON S3	ON S4	ON S5	Control signal
VCC CORE	Core voltage for Processor	X				VR_ON
SMDDR_VREF	1.25V for DDR Reference voltage	X	X			SUSON
SMDDR_VTERM	1.25V for DDR Termination voltage	X				MAINON
1.5V		X				MAINON
1.8V		X				MAINON
2.5VSUS		X	X			SUSON
2.5V		X				MAINON
2.5VPCU		X	X	X	X	VL
3VPCU		X	X	X	X	VL
3VSUS		X	X			SUSON
3V		X				MAINON
5VPCU		X	X	X	X	VL
5VSUS		X	X			SUSON
5V		X				MAINON

PCI DEVICE	IDSEL#	REQ/GNT#	Interrupts
LAN(10/100)	AD16	3/3	INTD#
CARDBUS	AD17	1/1	INTB#, INTC#
MINI-PCI	AD18		INTC#, INTD#

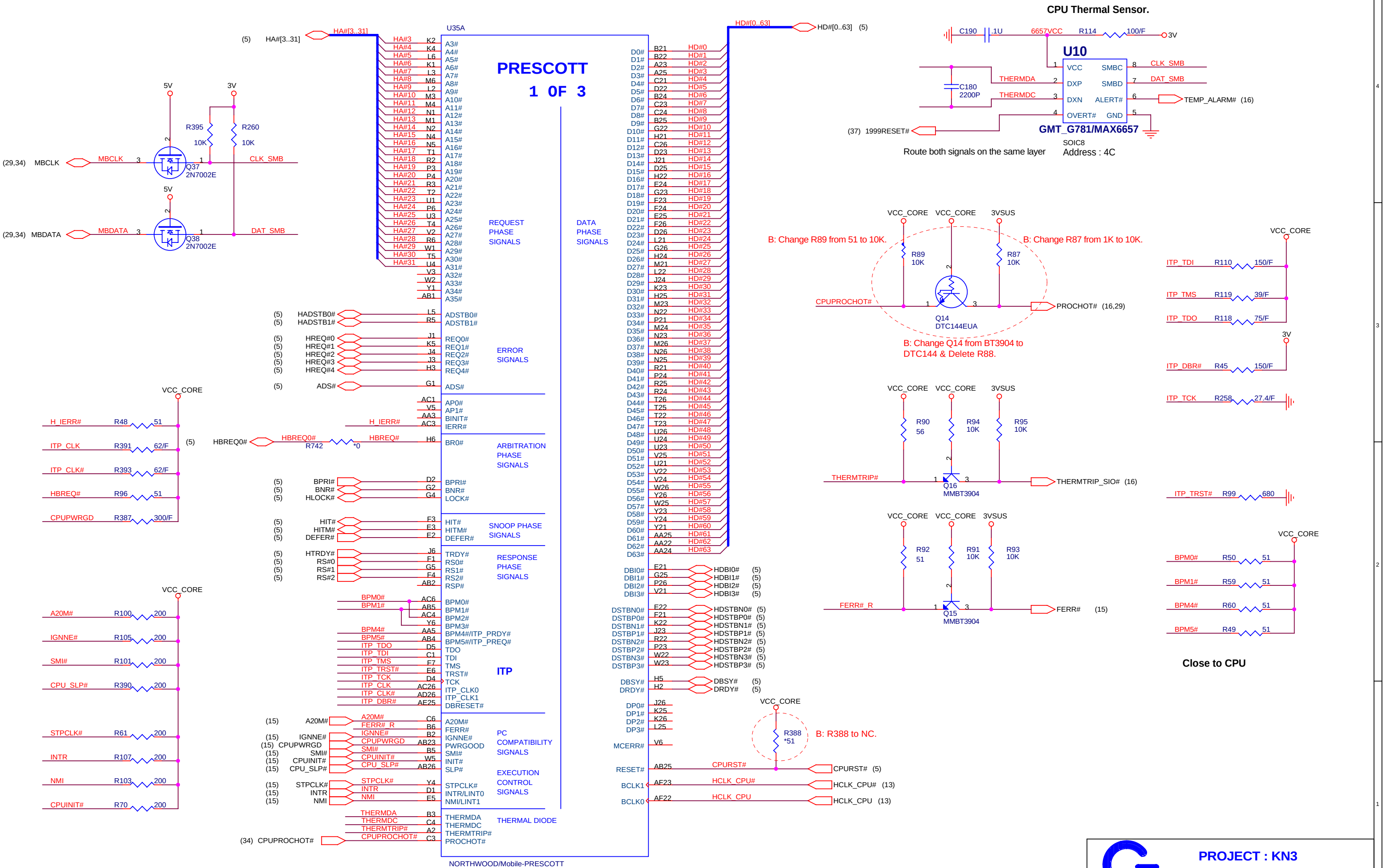
POWER SEQUENCE



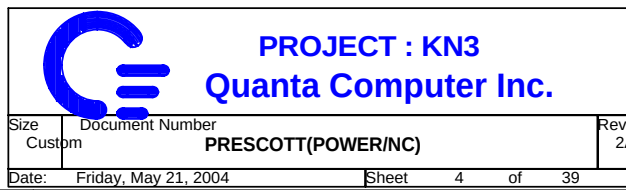
PROJECT : KN3
Quanta Computer Inc.

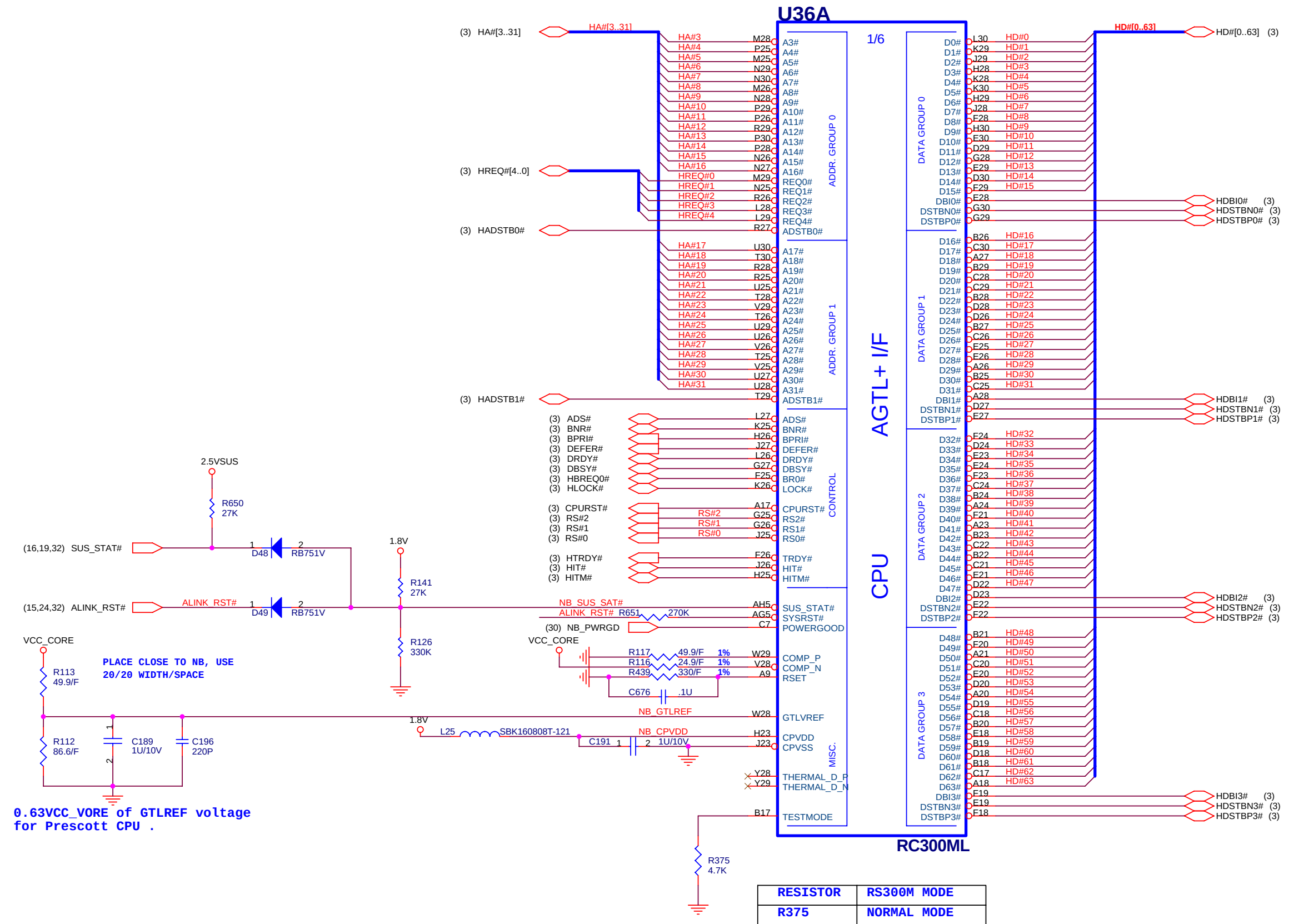
NORTHWOOD/Mobile-PRESCOTT CPU - HOST BUS

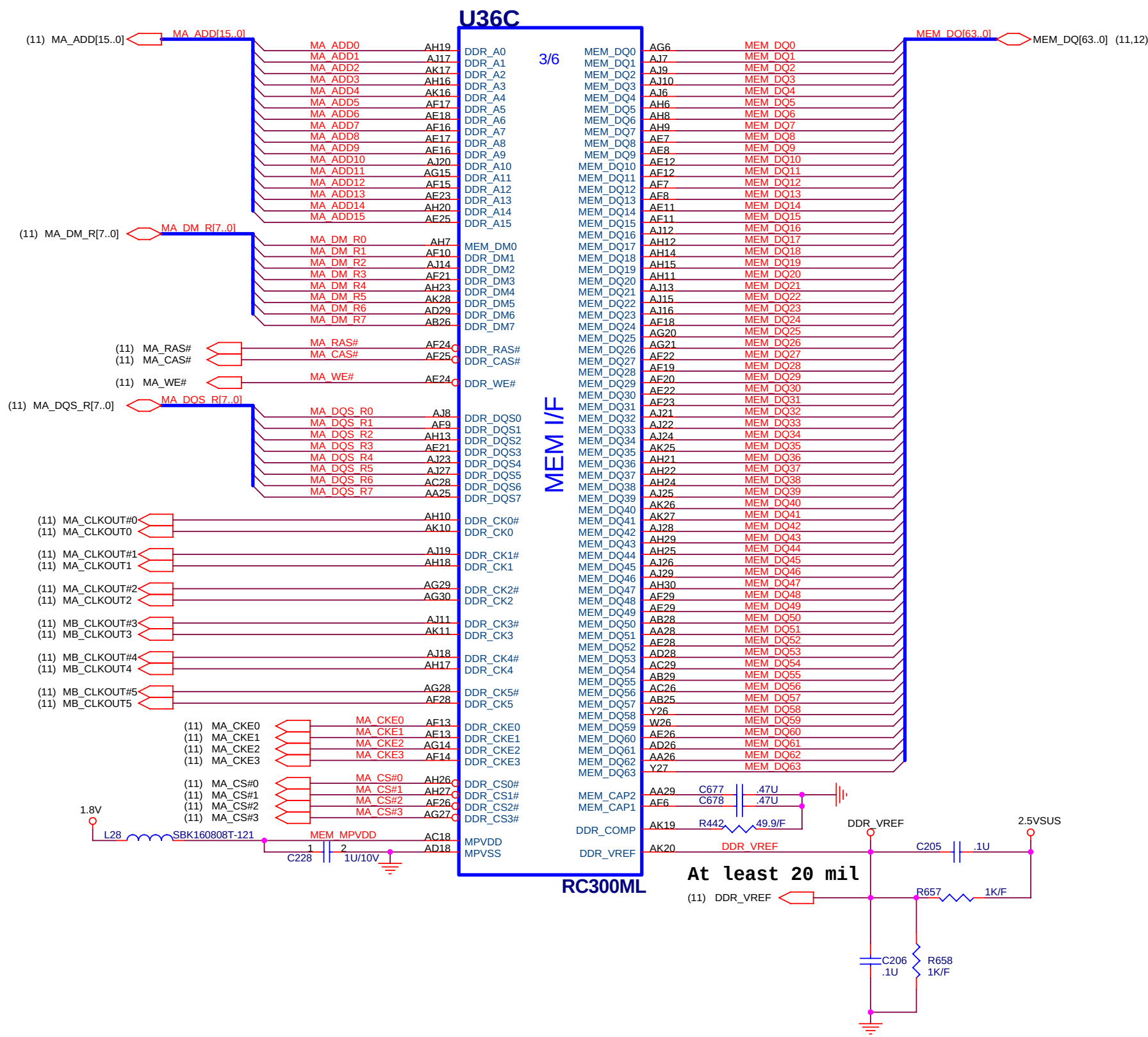
03

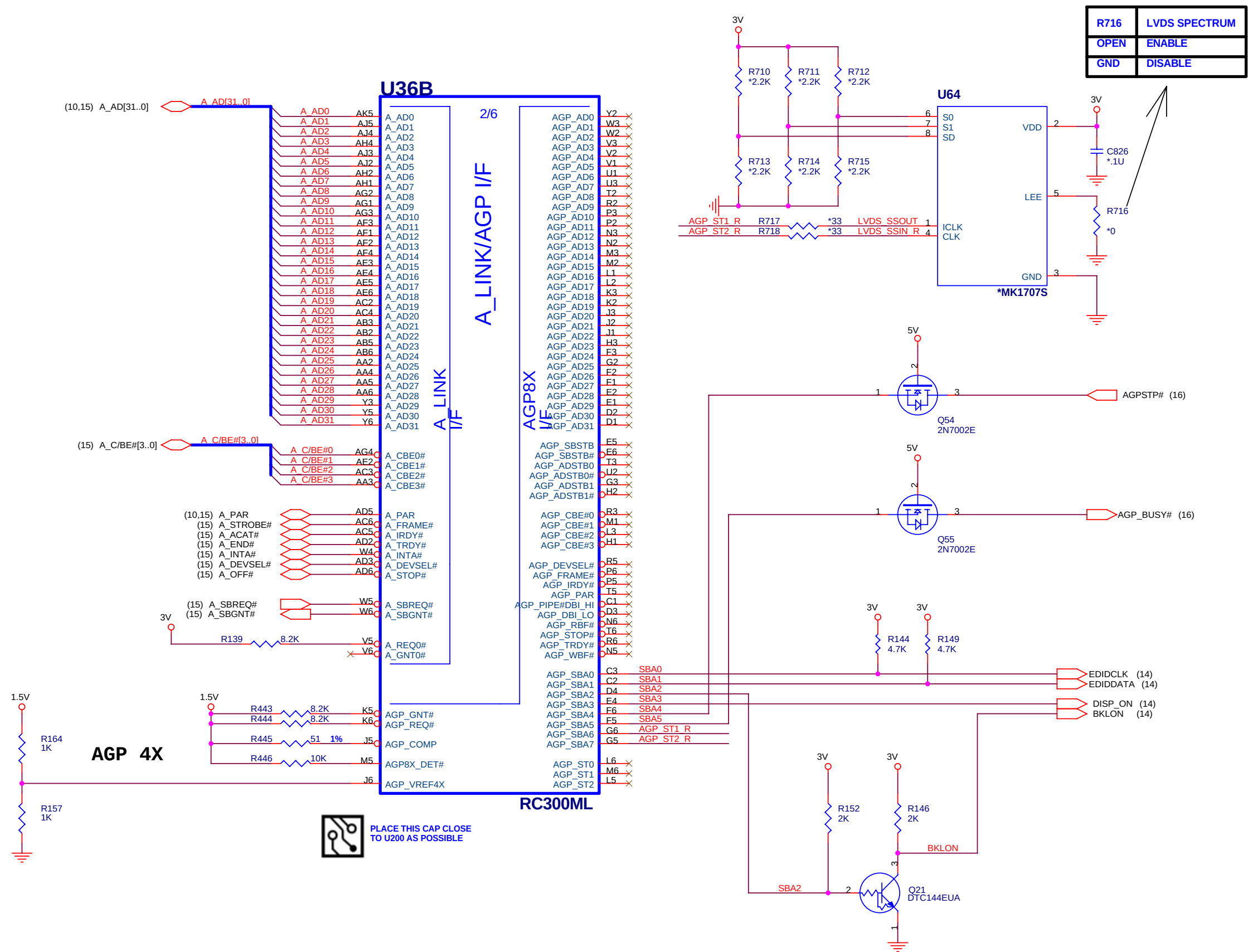


04









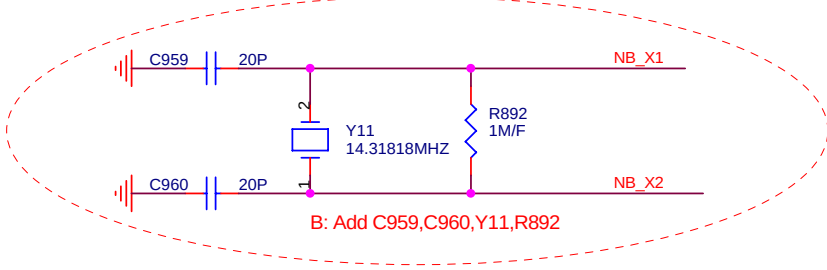
NorthBridge-ATI RC300ML-VIDEO I/F & CLKGEN

AVDD	DAC VDD (2.5V)
AVDDDI	DIGITAL VDD (1.8V)
AVDDQ	DAC2 BANDGAP REF (1.8V)
PLLVD	PLL VDD (1.8V)

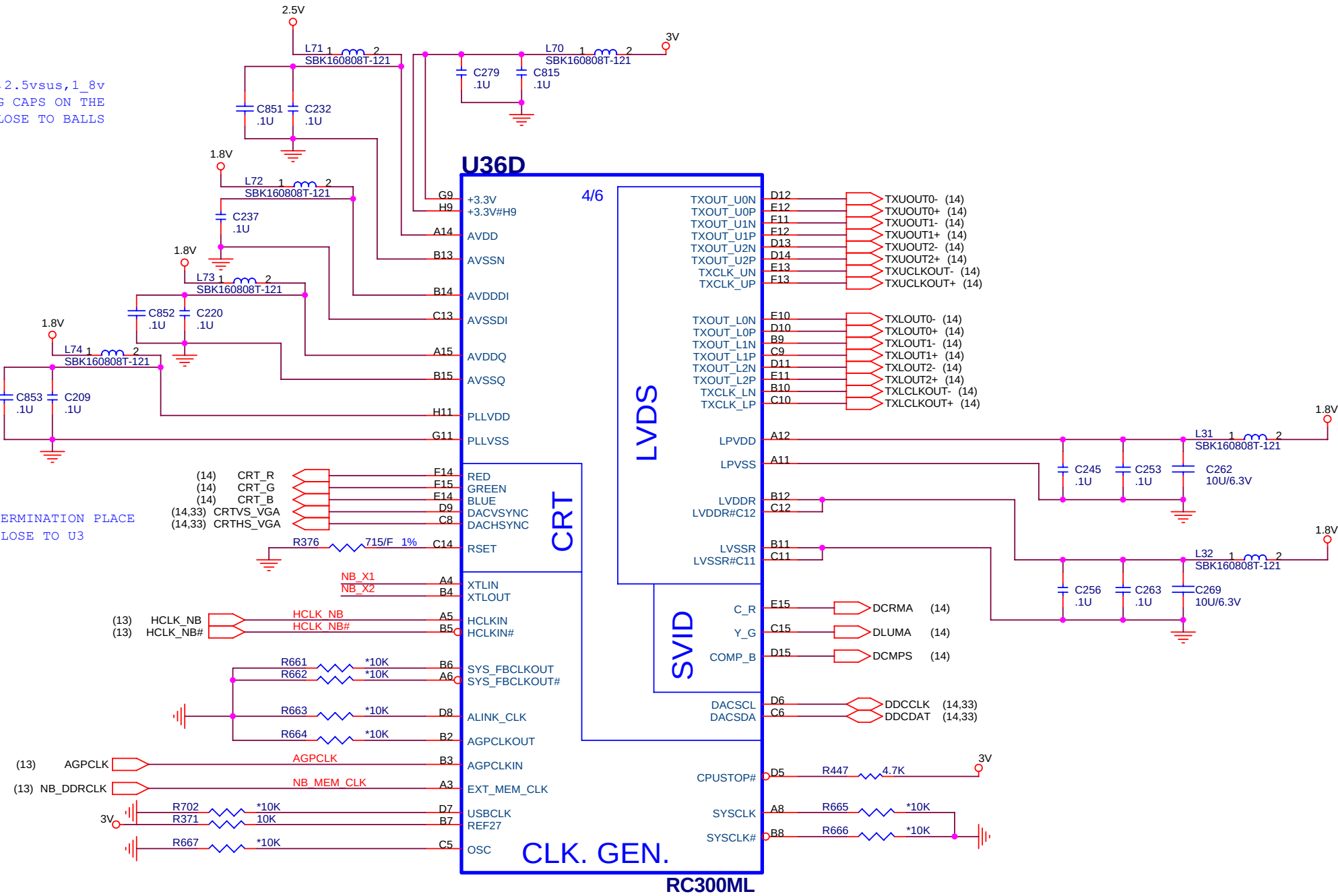
PUT 3vsus,2.5vsus,1.8v
DECOUPLING CAPS ON THE
BOTTOM, CLOSE TO BALLS

TERMINATION PLACE
CLOSE TO U3

B: Delete R659,R660

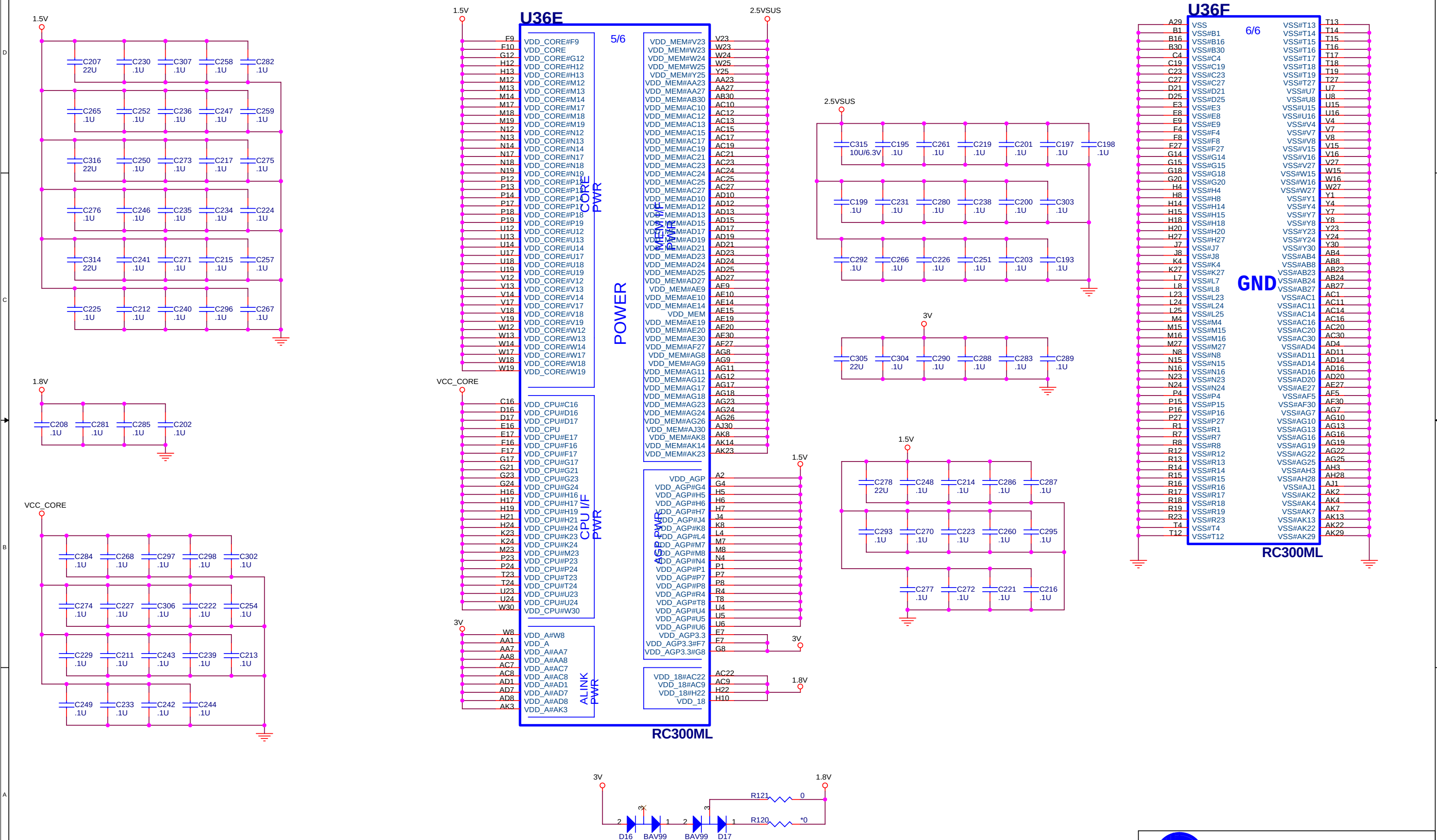


Y11 P/N ?

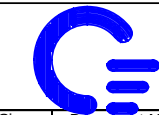
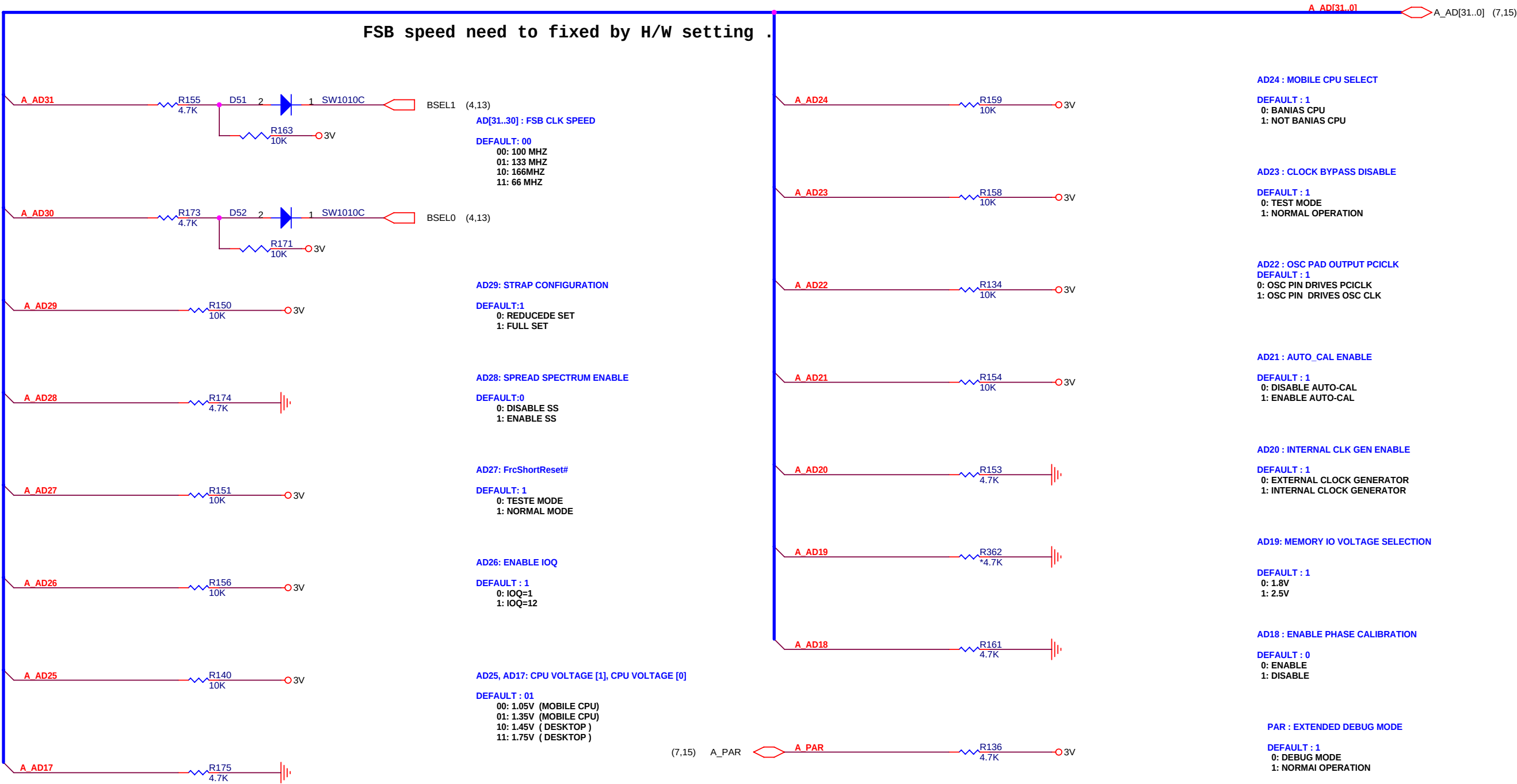


NorthBridge-ATI RC300ML - POWER

09



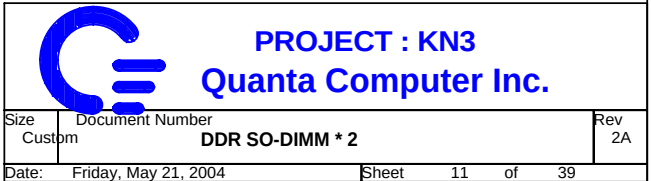
1.8V (NB) should ramp up with 3V, < 2.1V

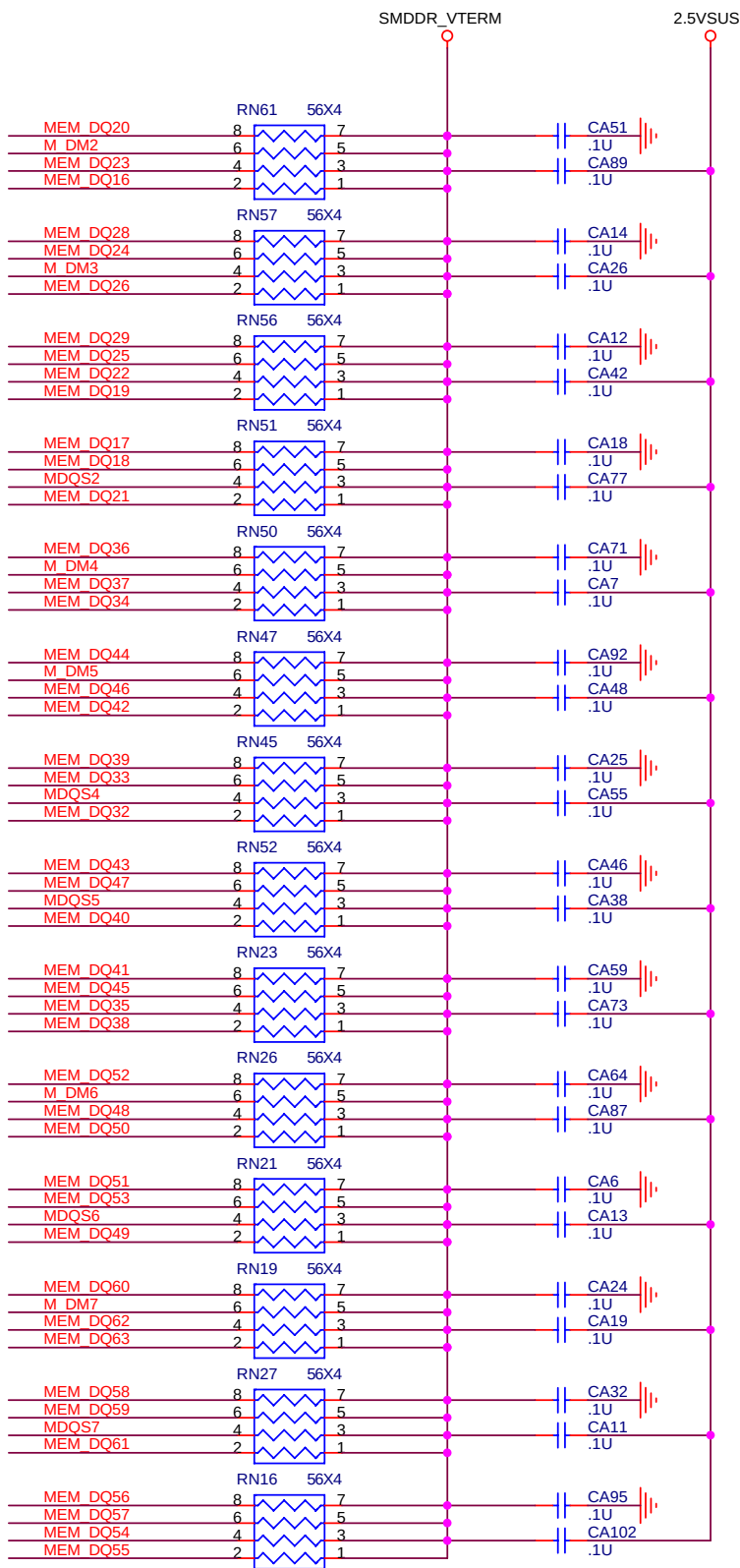
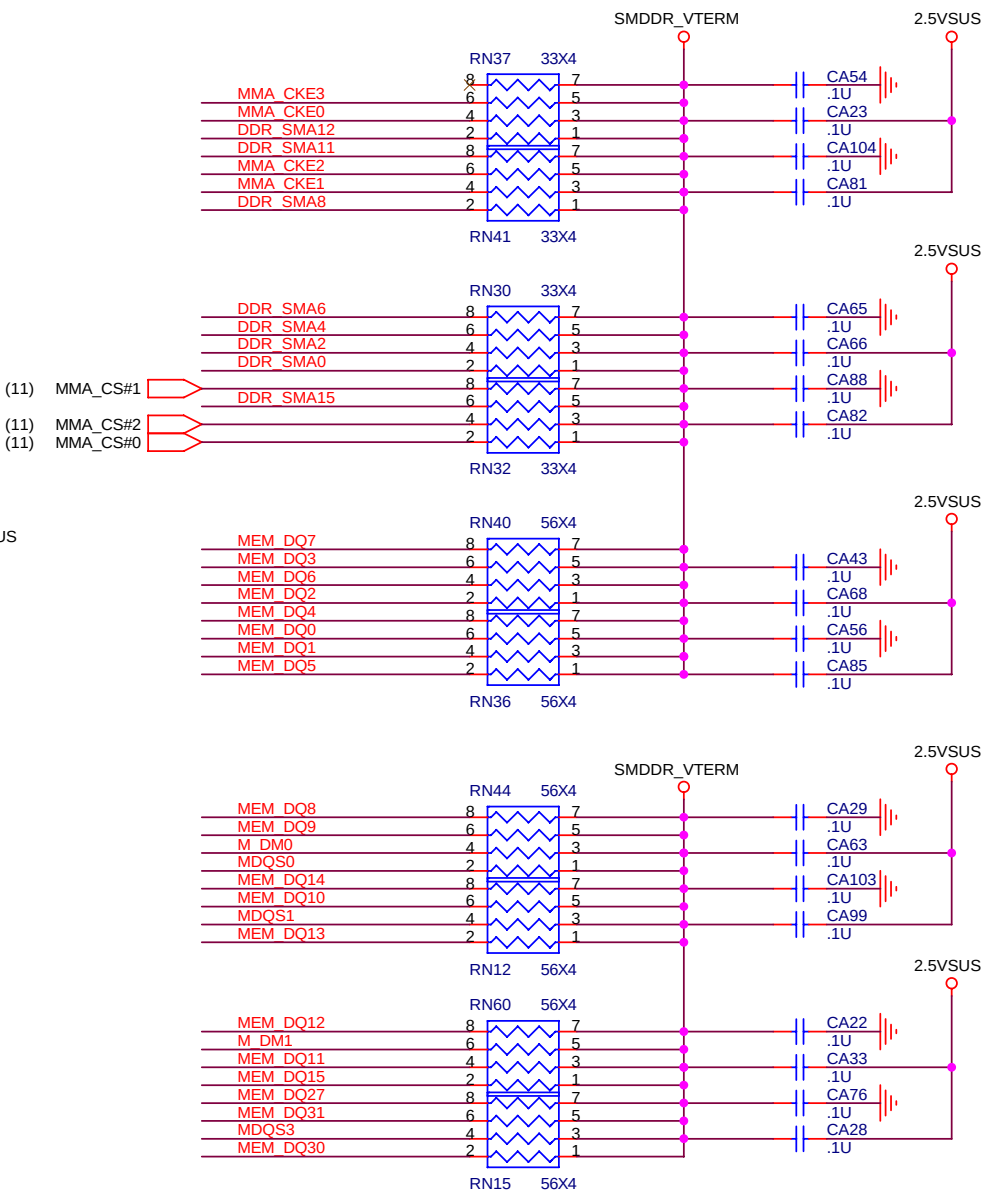
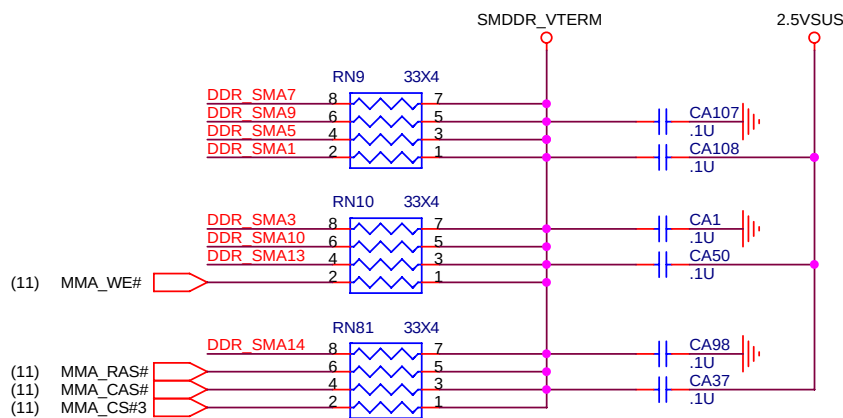
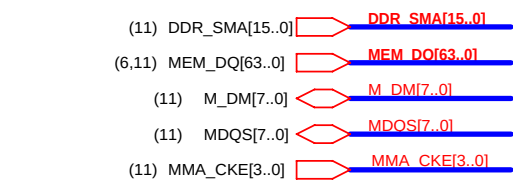


PROJECT : KN3
Quanta Computer Inc.

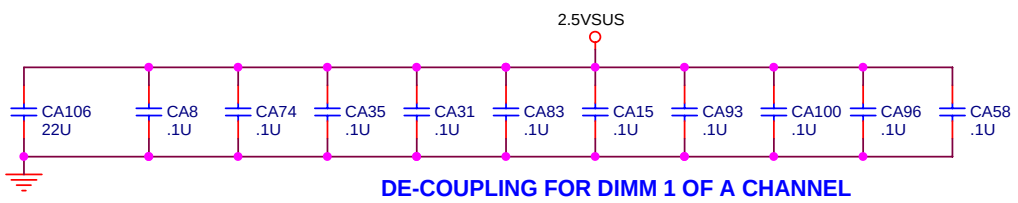
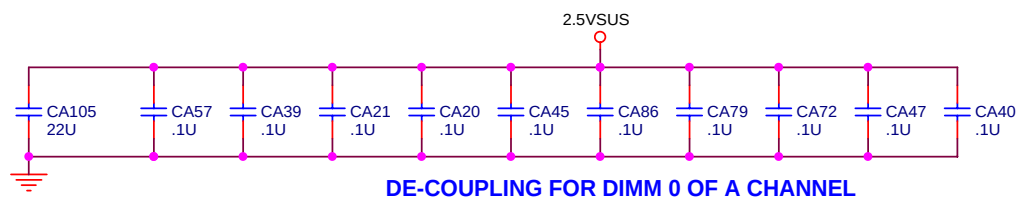
Size Custom	Document Number RC300ML-STRAPS	Rev 2A
Date: Friday, May 21, 2004	Sheet 10 of 39	

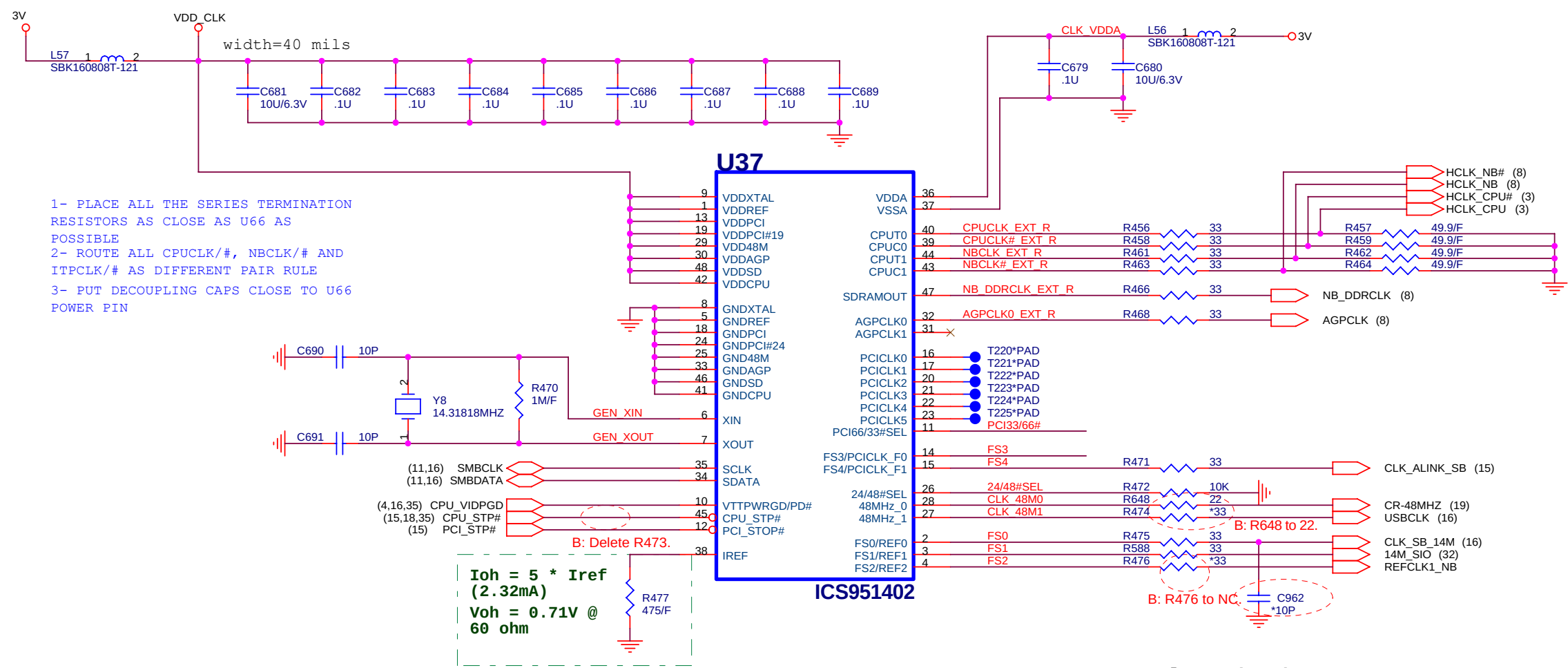
11





- 1) 2 DE-COUPLING CAPS PER RPAK
- 2) PLACE RPACKS&RESISTORS AFTER THE LAST DIMM



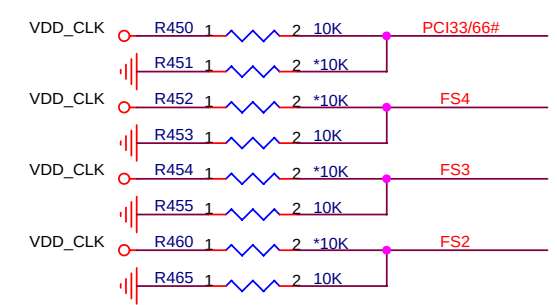


- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U66 AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBCLK/# AND ITPCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U66 POWER PIN

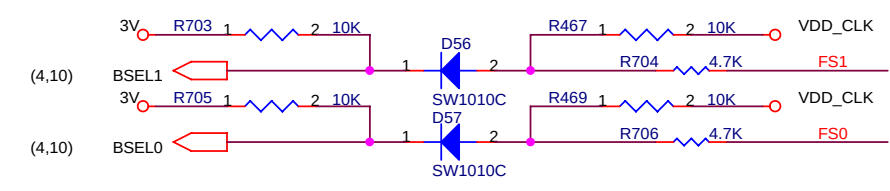
EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS4	FS3	FS2	FS1	FS0	CPU	MEM	AGP	PCI	FS4	FS3	FS2	FS1	FS0	CPU	MEM	AGP	PCI
0	0	0	0	0	100.01	100.01	66.66	66.66	1	0	0	0	0	99.51	99.51	66.66	66.66
0	0	0	0	1	133.33	133.33	66.66	66.66	1	0	0	0	1	132.69	132.69	66.66	66.66
0	0	0	1	0	200.01	200.01	66.66	66.66	1	0	0	1	0	199.02	199.02	66.66	66.66
0	0	0	1	1	166.64	166.64	66.66	66.66	1	0	0	1	1	165.85	165.85	66.66	66.66
0	0	1	0	0	100.01	133.34	66.66	66.66	1	0	1	0	0	99.51	99.51	66.66	66.66
0	0	1	0	1	133.34	100.01	66.66	66.66	1	0	1	0	1	132.68	132.68	66.66	66.66
0	0	1	1	0	133.16	166.45	66.66	66.66	1	0	1	1	0	132.59	132.59	66.66	66.66
0	0	1	1	1	166.45	133.16	66.66	66.66	1	0	1	1	1	165.73	165.73	66.66	66.66
0	1	0	0	0	105.00	105.00	66.66	66.66	1	1	0	0	0	99.38	99.38	66.66	66.66
0	1	0	0	1	140.00	140.00	66.66	66.66	1	1	0	0	1	132.52	132.52	66.66	66.66
0	1	0	1	0	66.67	66.67	66.66	66.66	1	1	0	1	0	198.77	198.77	66.66	66.66
0	1	0	1	1	175.00	175.00	66.66	66.66	1	1	0	1	1	165.64	165.64	66.66	66.66
0	1	1	0	0	109.99	109.99	66.66	66.66	1	1	1	0	0	99.38	132.51	66.66	66.66
0	1	1	0	1	146.66	146.66	66.66	66.66	1	1	1	0	1	132.51	99.38	66.66	66.66
0	1	1	1	0	210.00	210.00	66.66	66.66	1	1	1	1	0	132.36	165.45	66.66	66.66
0	1	1	1	1	183.27	183.27	66.66	66.66	1	1	1	1	1	165.45	132.36	66.66	66.66

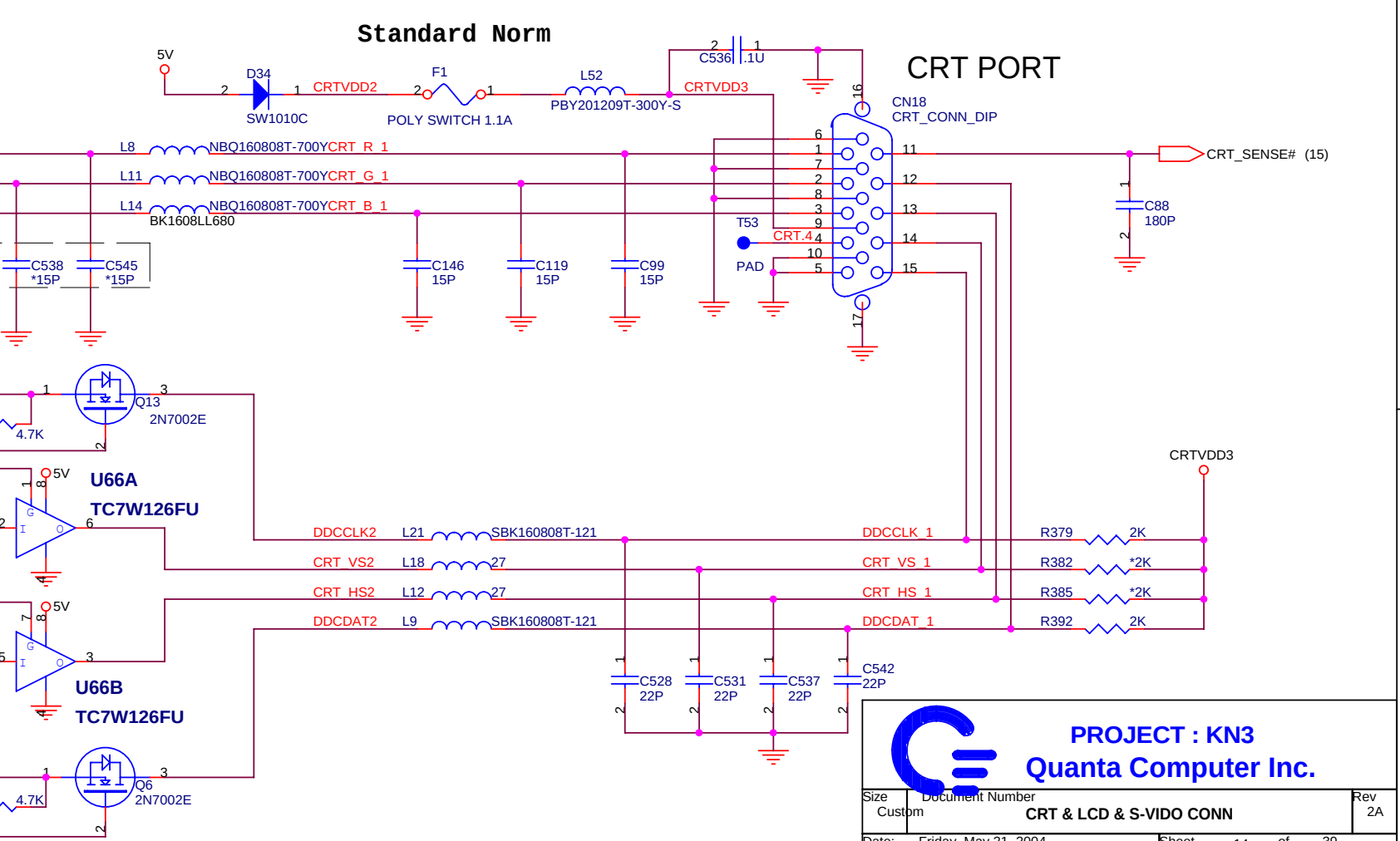
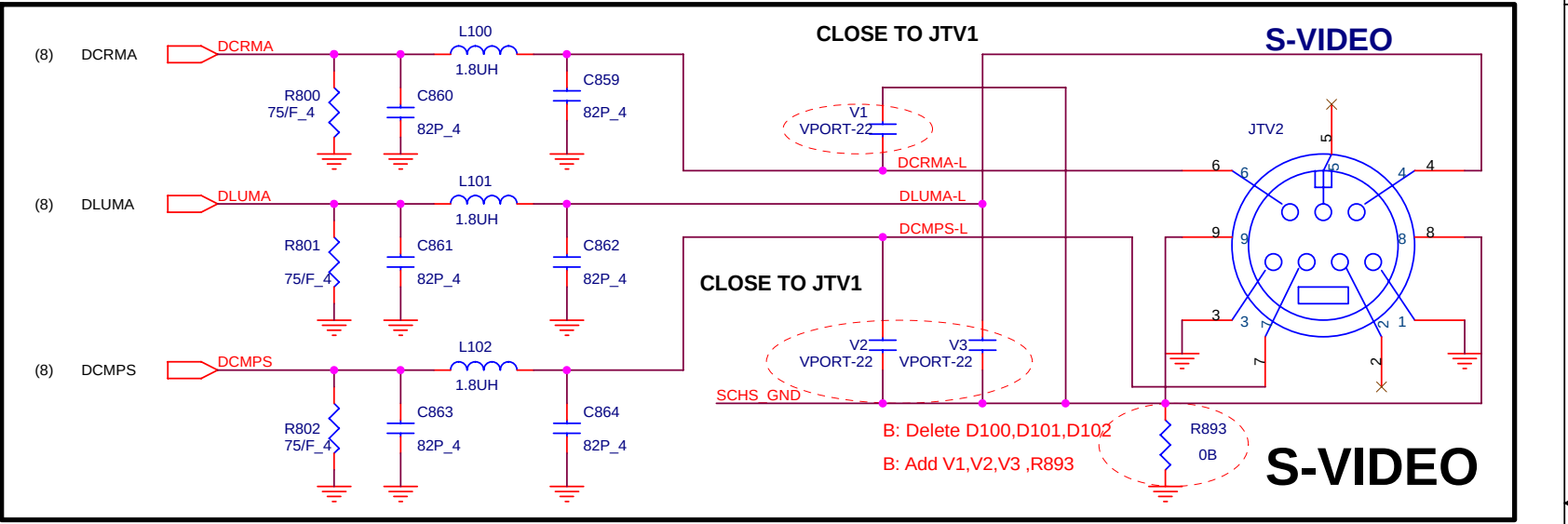
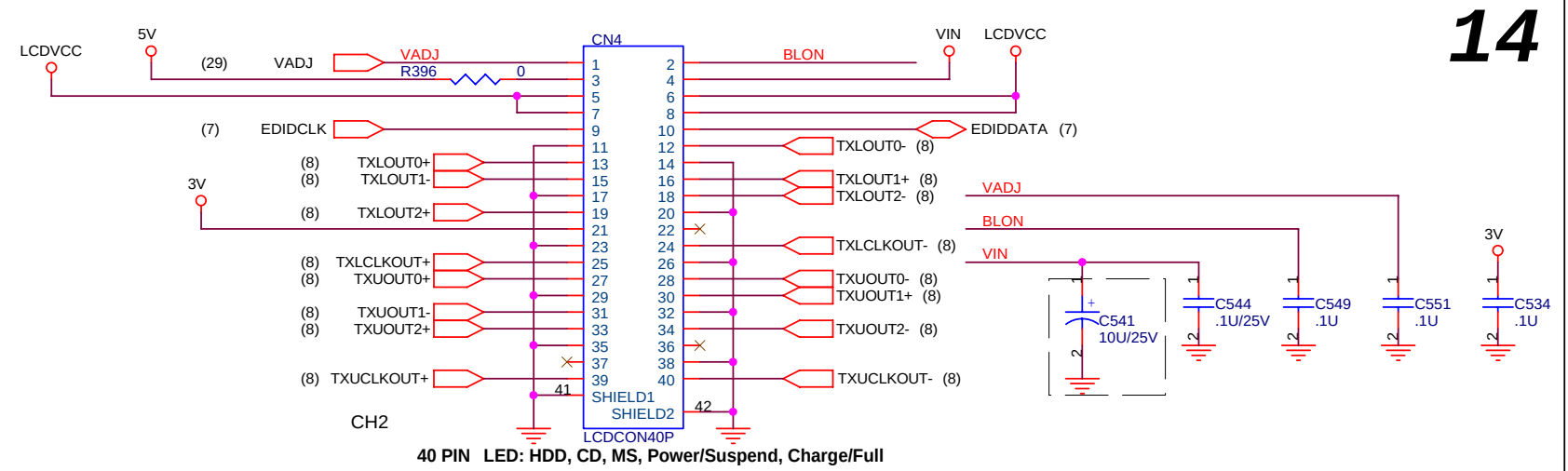
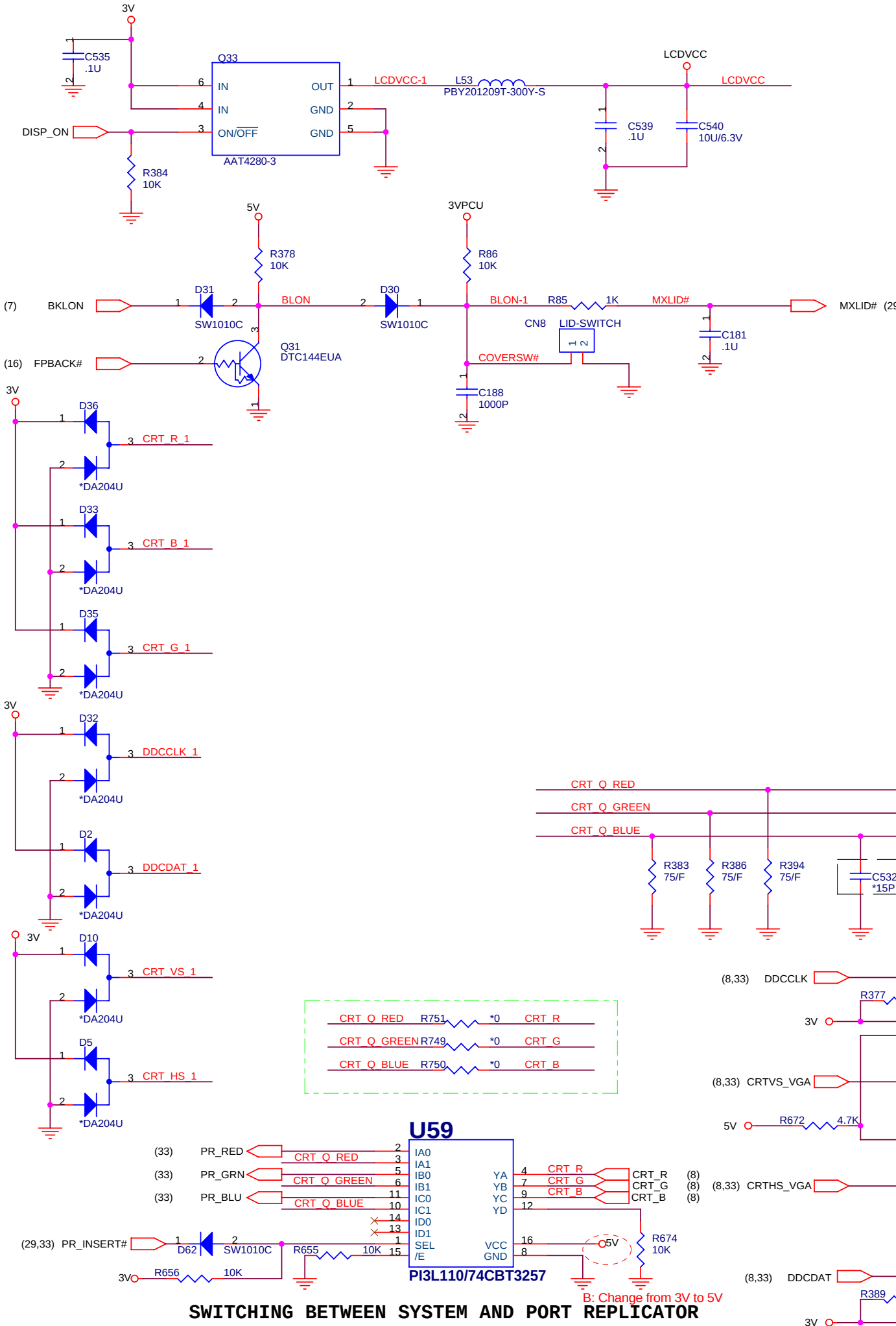
Frequency Select Circuit



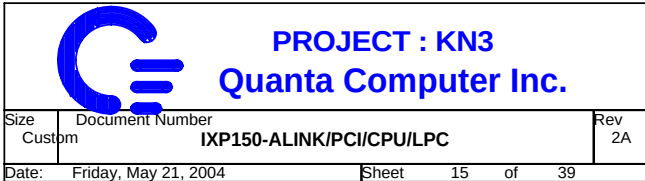
INTERNAL PULL DOWN



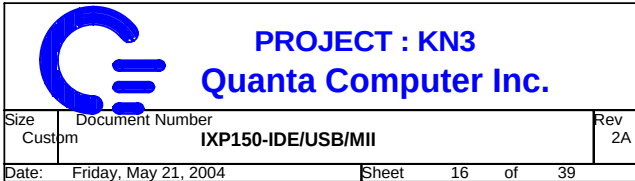
CRT & LCD CONN



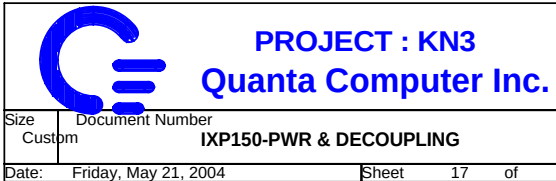
15



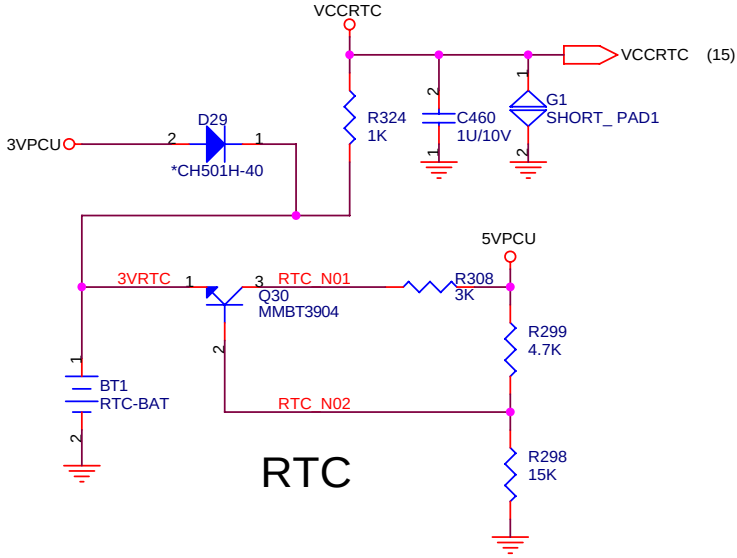
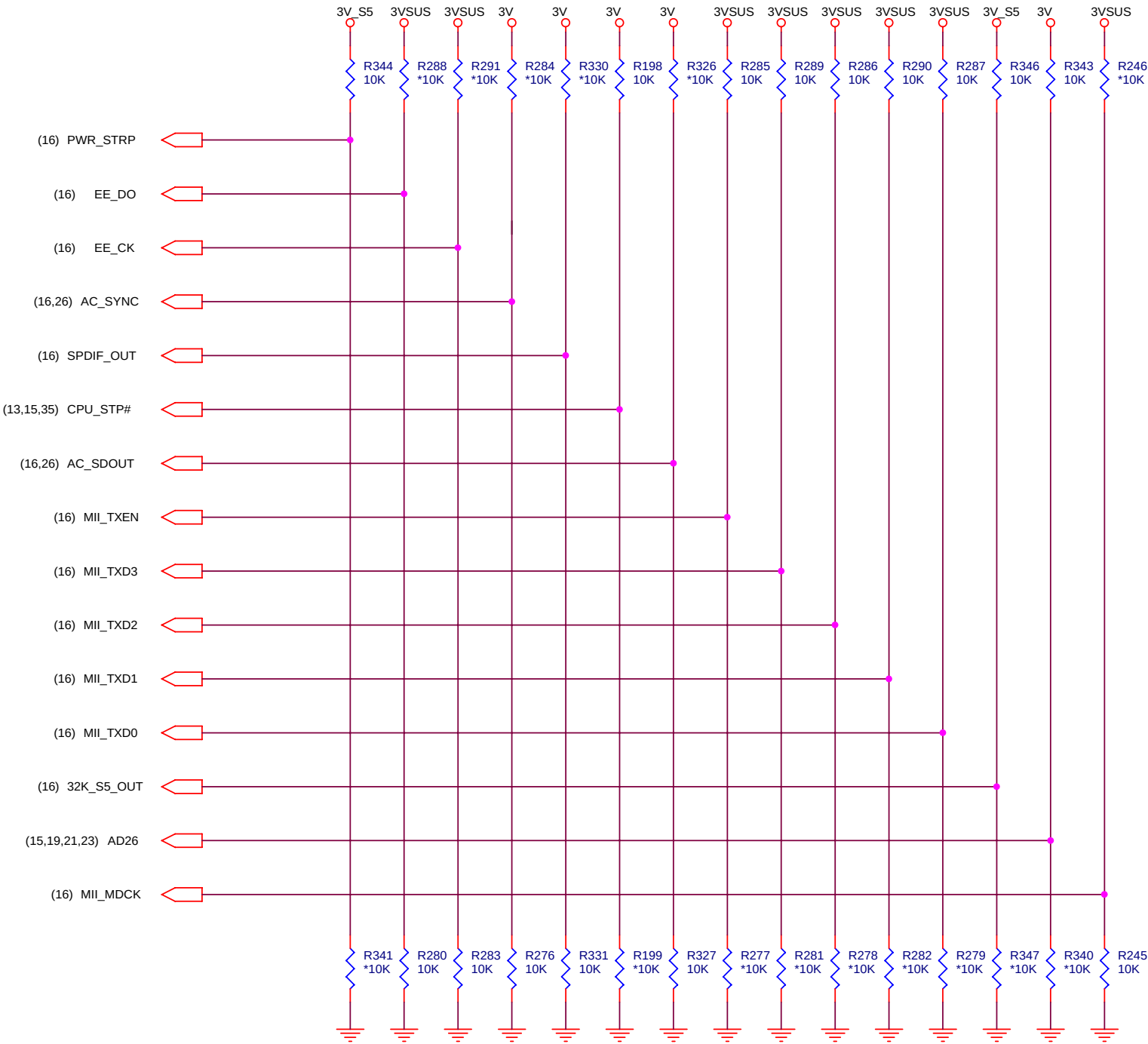
16



17



There is no such strap for A41 SB200

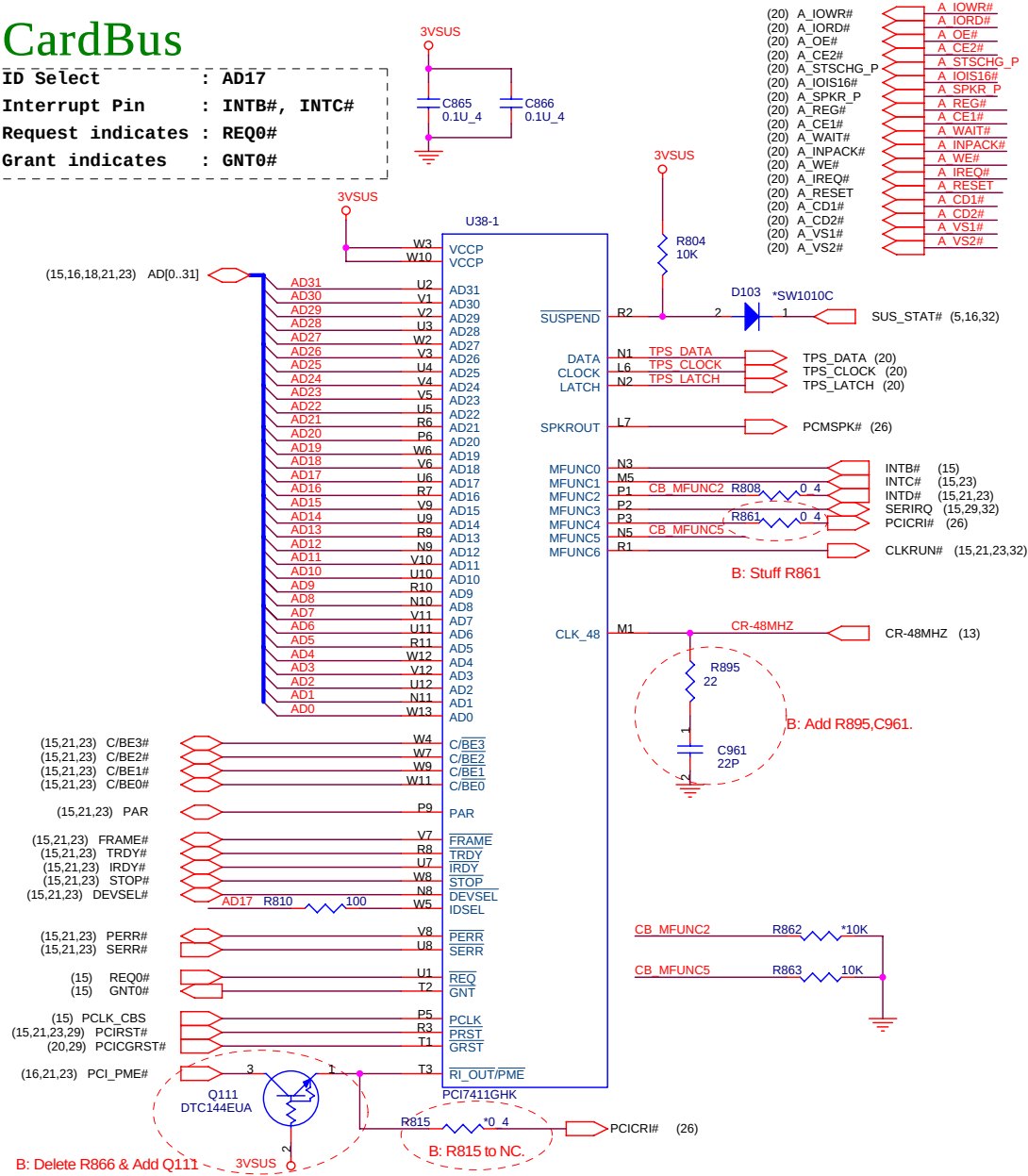


 OVERLAP COMMON PADS
FOR DUAL-OP
RESISTORS
REQUIRED SYSTEM STRAPS

STRAP HIGH	PWR_STRP	EEDO	EECK	AC_SYNC	AC_SDOUT	SPDIF_OUT	CPU_STP#	TX_EN	ETHERNET TXD[3:0]	32KHZ_S5	PCI_AD26
	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS DEFAULT	ROM ON PCI BUS	INIT ACTIVE HIGH(AMD)	33MHz NB BUS	SIO 24MHz	ENABLE SPEED STEP DEFAULT	DISABLE CPU FREQ SETTING DEFAULT		32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT	BIOS use LPC cycle DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (P4) DEFAULT	HI SPEED A-LINK DEFAULT	SIO 48MHz DEFAULT	DISABLE SPEED STEP	ENABLE CPU FREQSETTING	PROCESSOR FREQ MULTIPLIER	32KHZ INPUT TO SB200 (EXT RTC)	BIOS uSE FWH Cycle

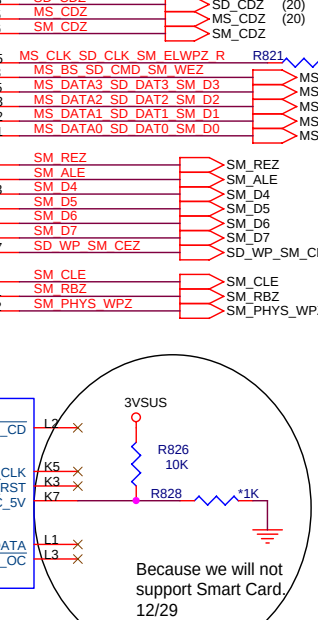
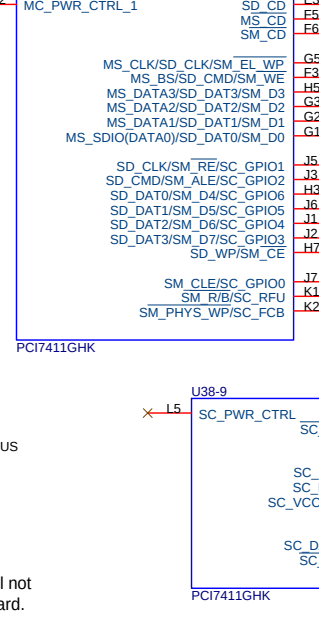
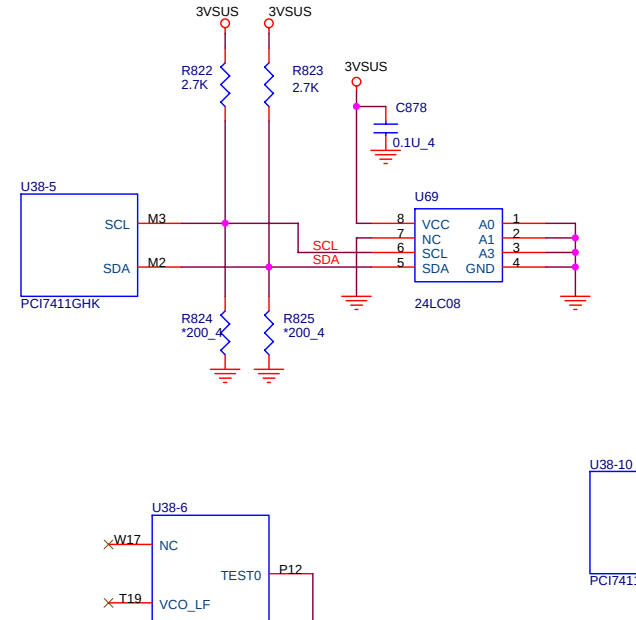
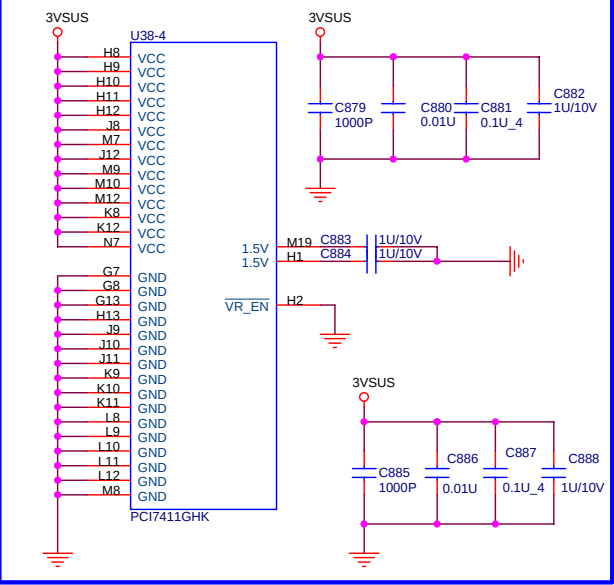
CardBus

ID Select : AD17
Interrupt Pin : INTB#, INTC#
Request indicates : REQ0#
Grant indicates : GNT0#

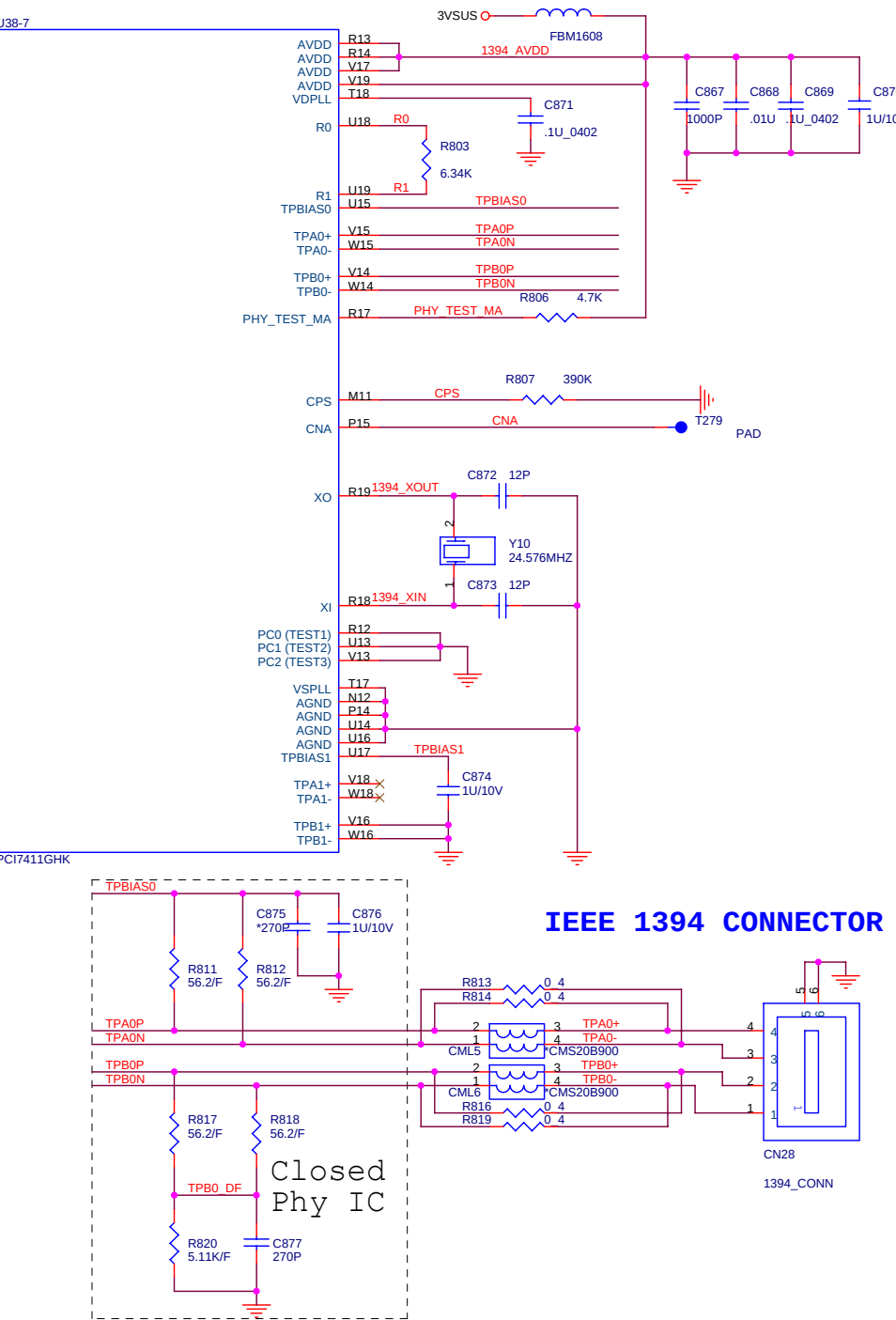


	PCI6411	PCI7411
POP	R862, R824, R825,	R808, R822, R823, C878, U69, L103, C867, C868, C869, C870, C871, C872, C873, C874, C876, C877, R803, R806, R807, R811, R812, R813, R814, R816, R817, R818, R819, R820, Y10, CN28
De-Pop	R808, R822, R823, C878, U69, L103, C867, C868, C869, C870, C871, C872, C873, C874, C876, C877, R803, R806, R807, R811, R812, R813, R814, R816, R817, R818, R819, R820, Y10, CN28	R862, R824, R825

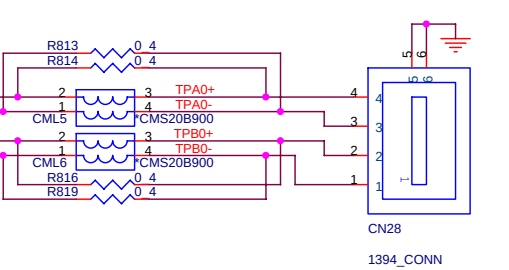
PCIXX21 Power Terminals



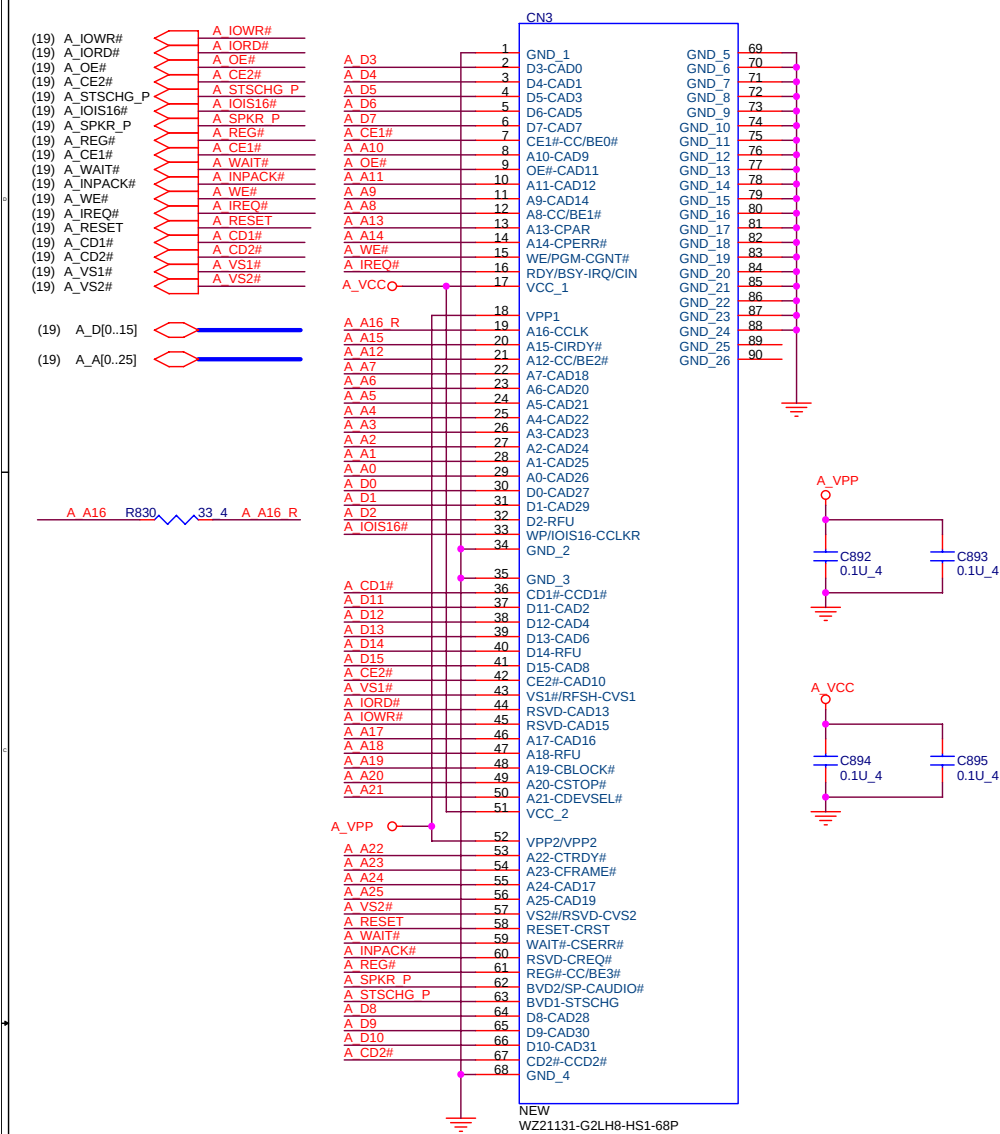
IEEE 1394a



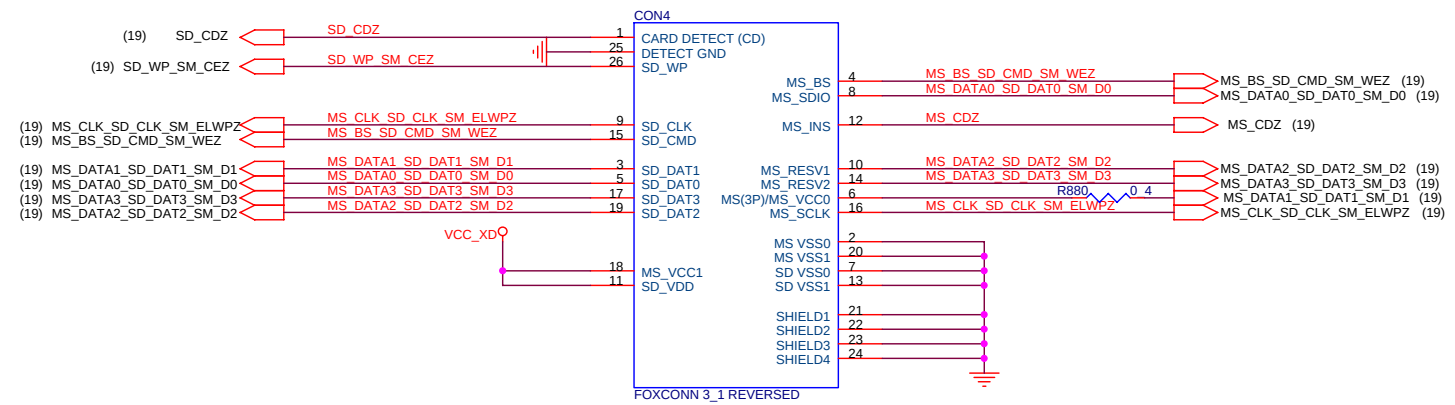
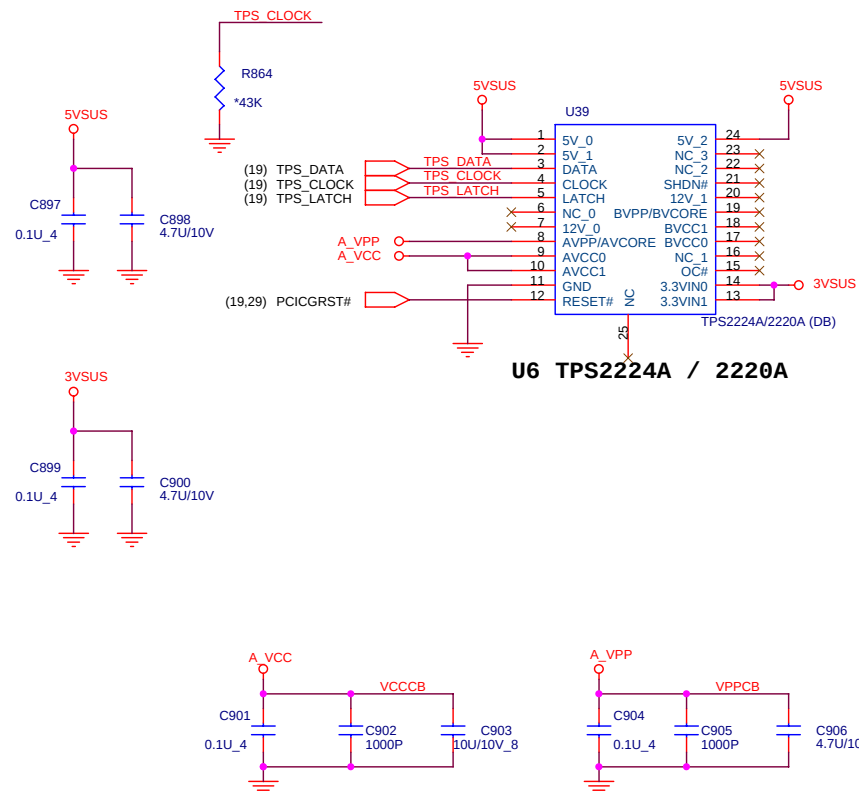
IEEE 1394 CONNECTOR



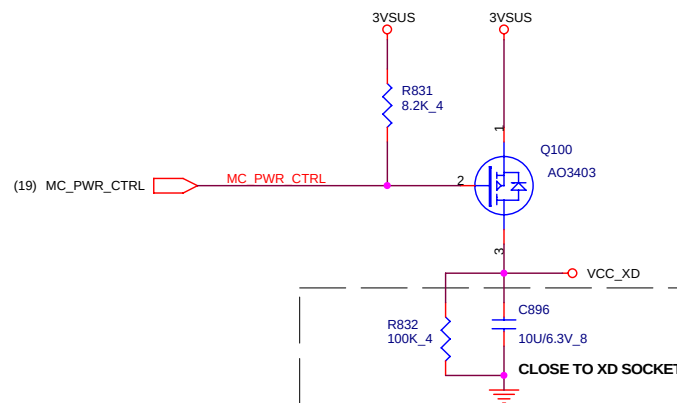
CardBus Connector

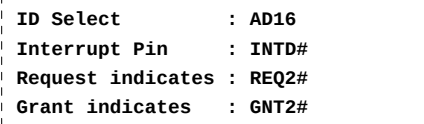


PCMCIA SOCKET

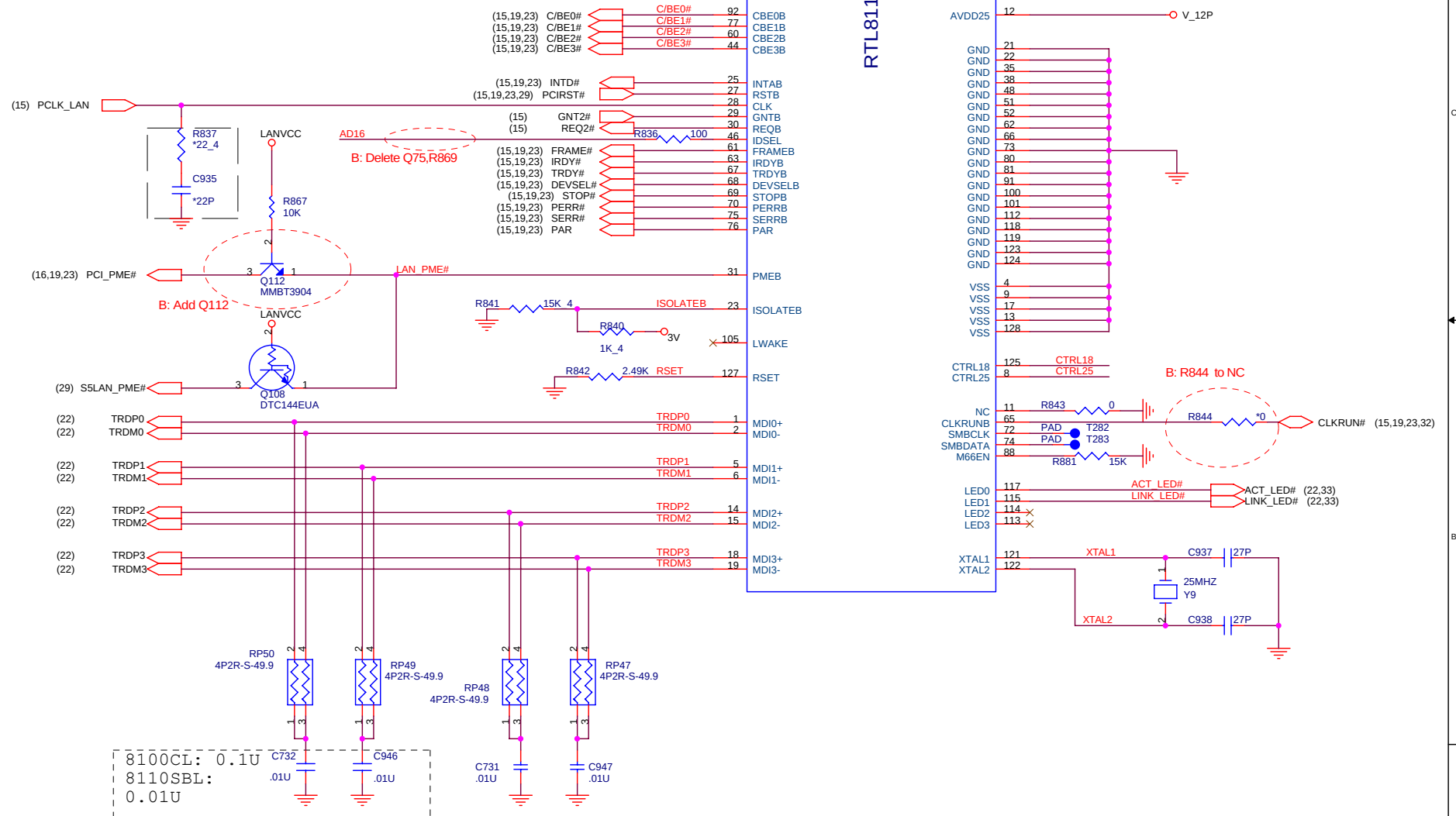


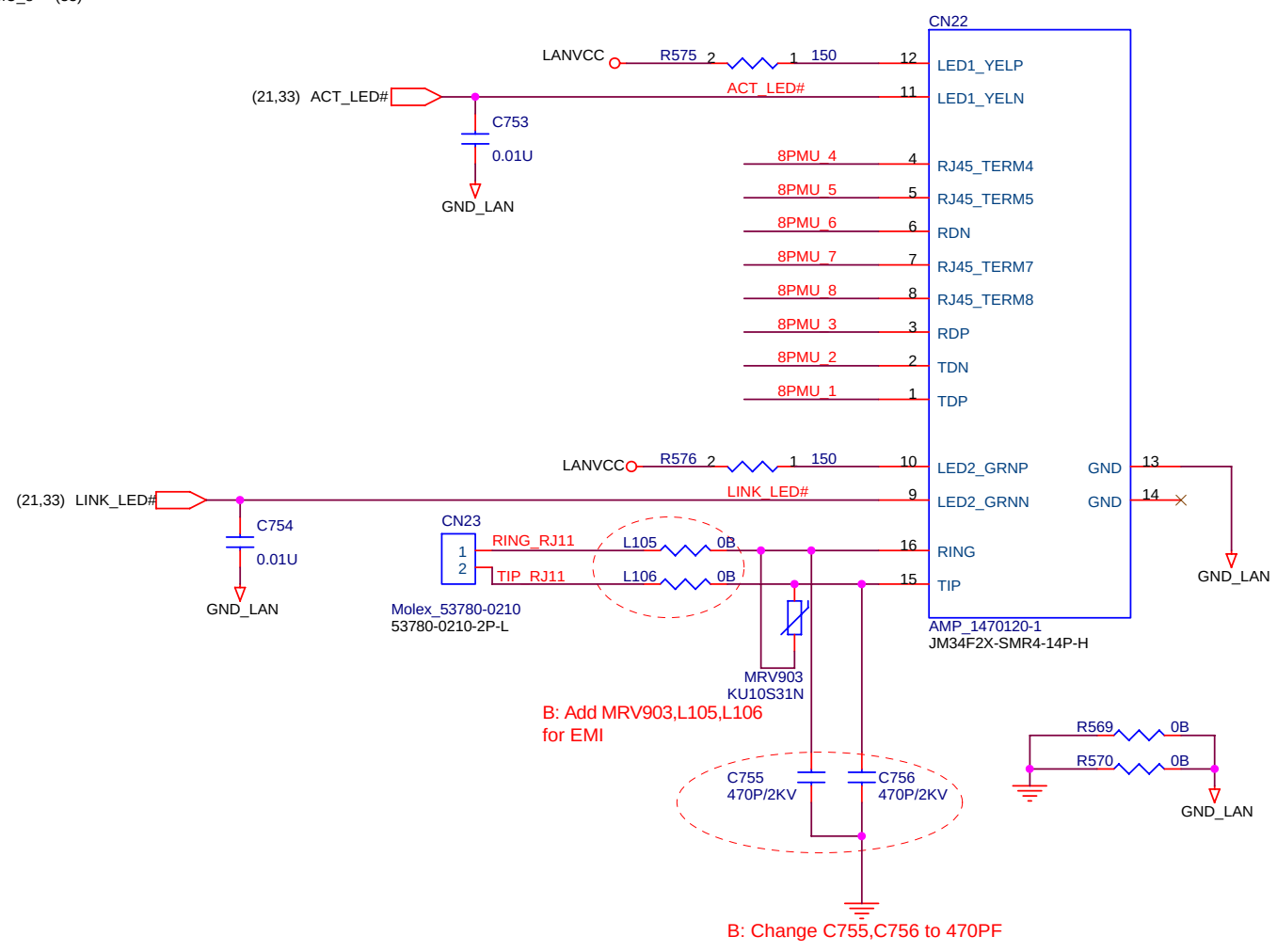
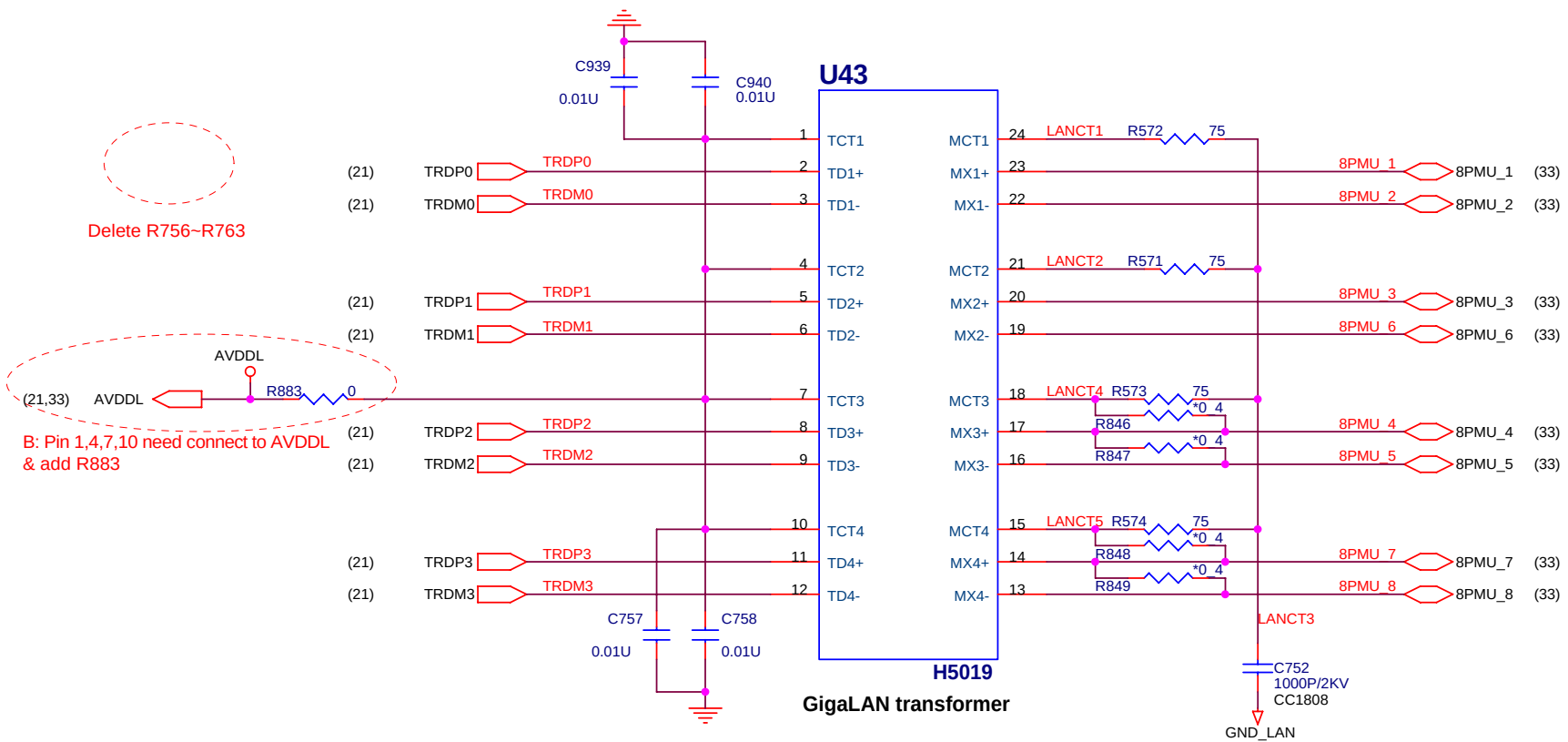
Place 0.1u bypass capacitor to each VCC Pin.



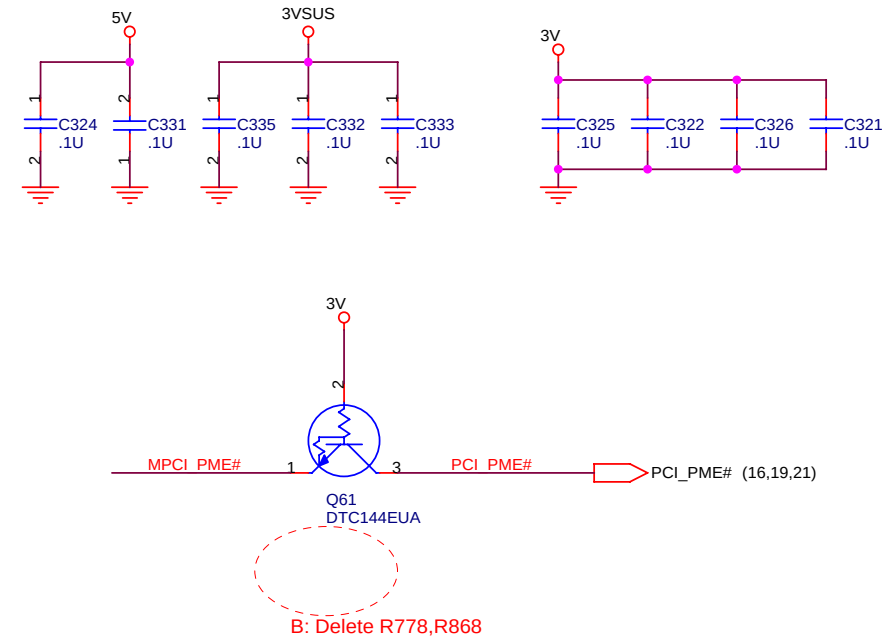
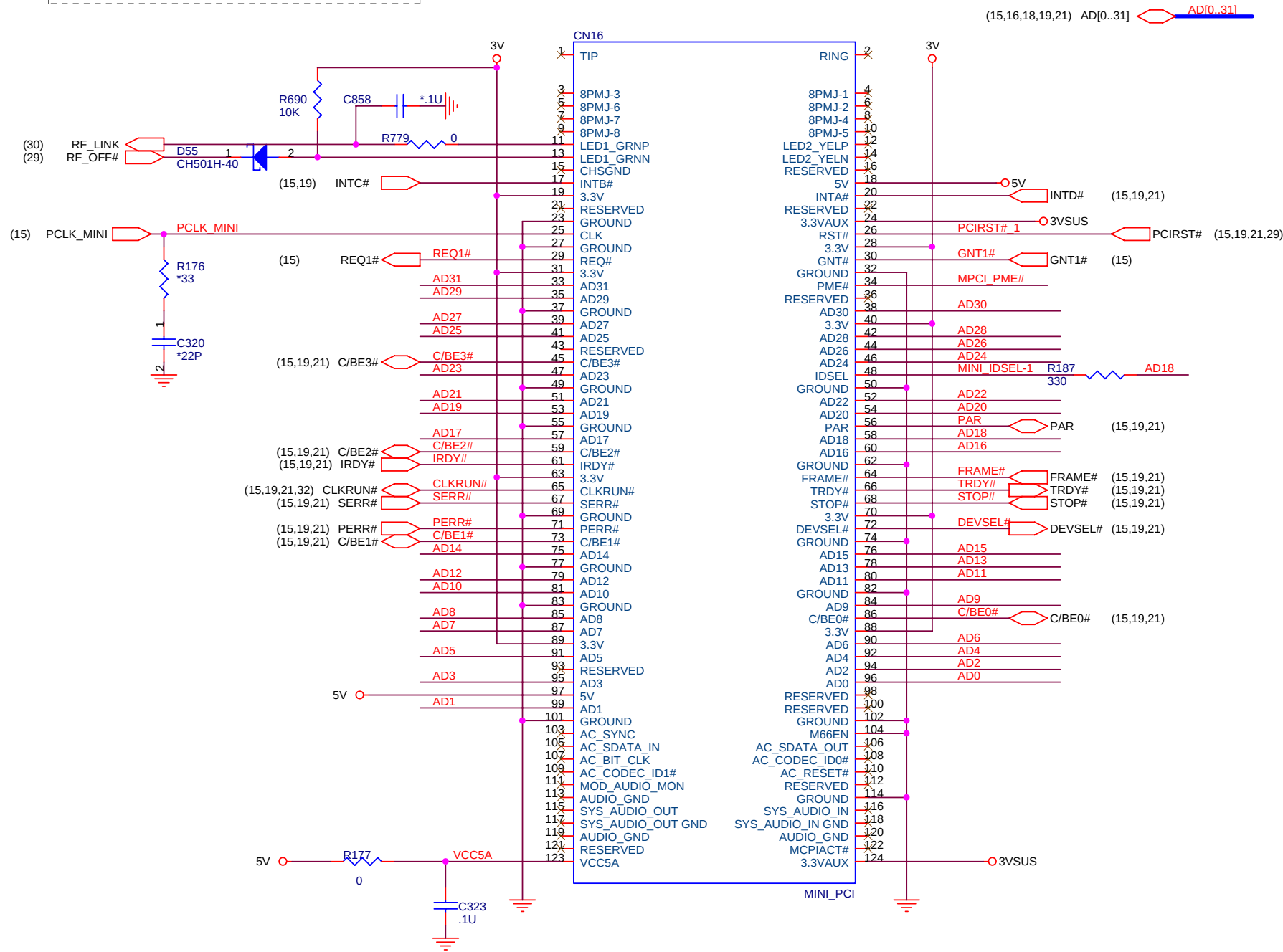


	8100CL(10/100M)	8110SB(1G)
DVDD33	3.3VD 26,41,56,71,84,94,107	3.3VD 26,41,56,71,84,94,107
AVDDL	3.3VA 3,7,20	2.5VA 3,7,20,16
DVDD	2.5VD 32,54,78,99	1.8VD 32,54,78,99,24,45,64,110,116,126
AVDD25	2.5VA 12	NC
AVDDH	NC	3.3VA 10,120
Pin 127	5.6k (1%) pull-low	2.49k (1%) pull-low
Pin 88	NC	15K pull-low
Pin 11	NC	0Ω pull-low



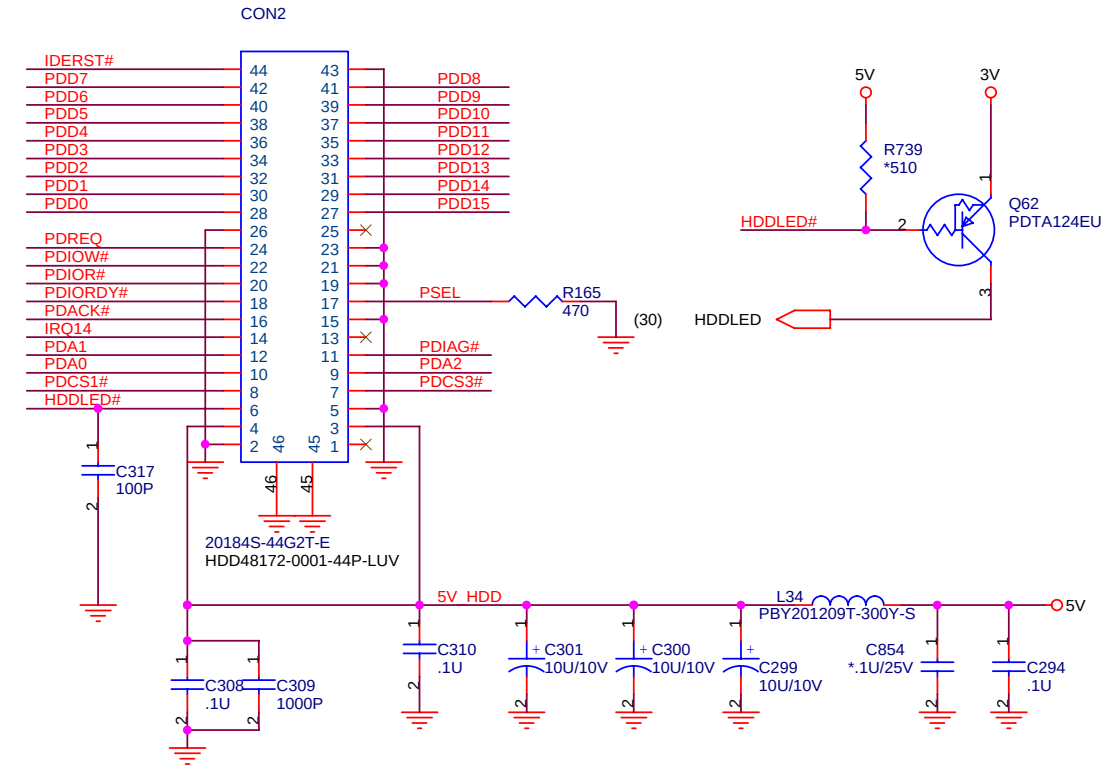


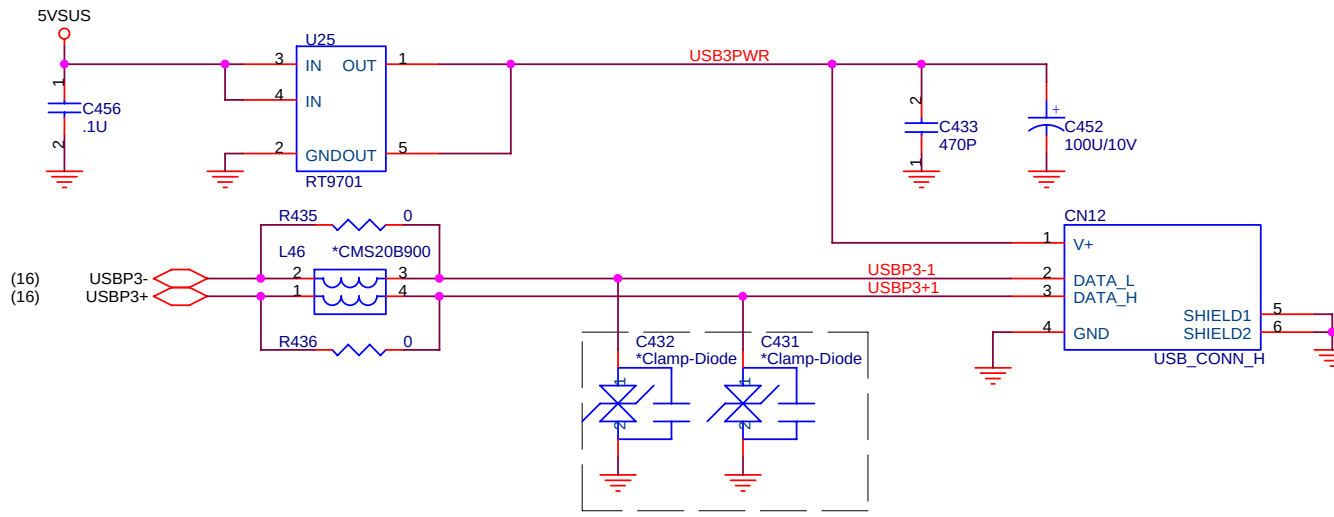
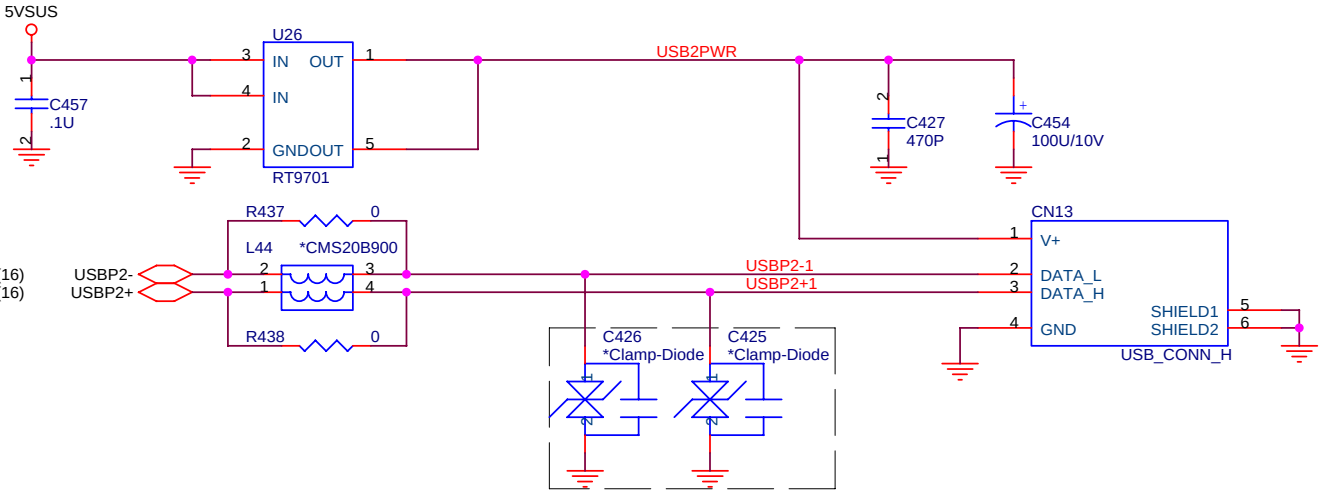
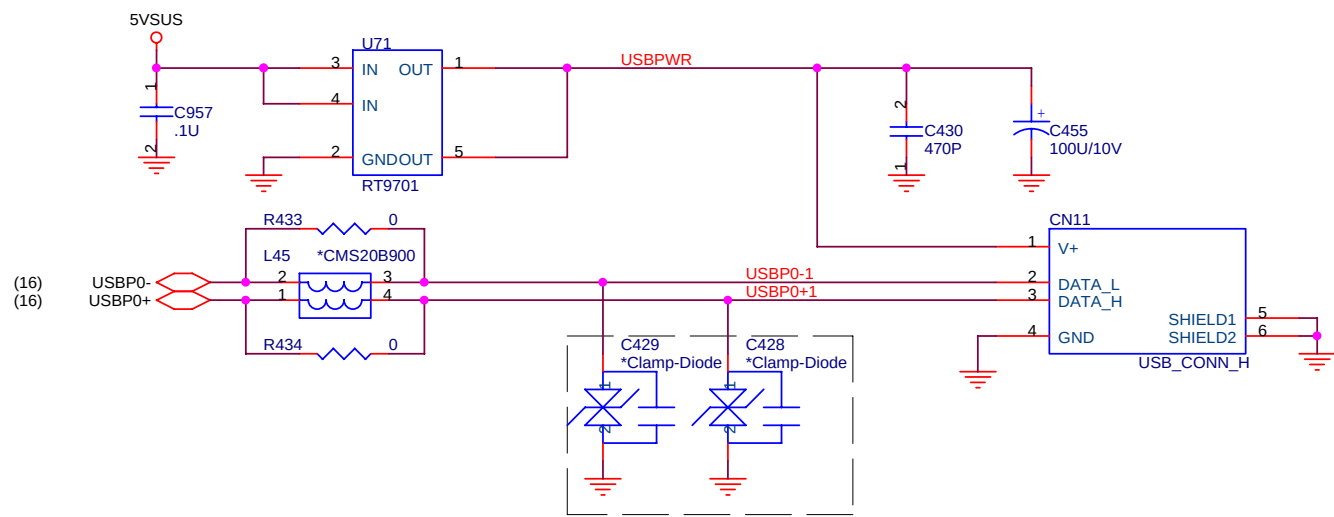
ID Select : AD18
Interrupt Pin : INTC# , INTD#
Request indicates : REQ1#
Grant indicates : GNT1#



24

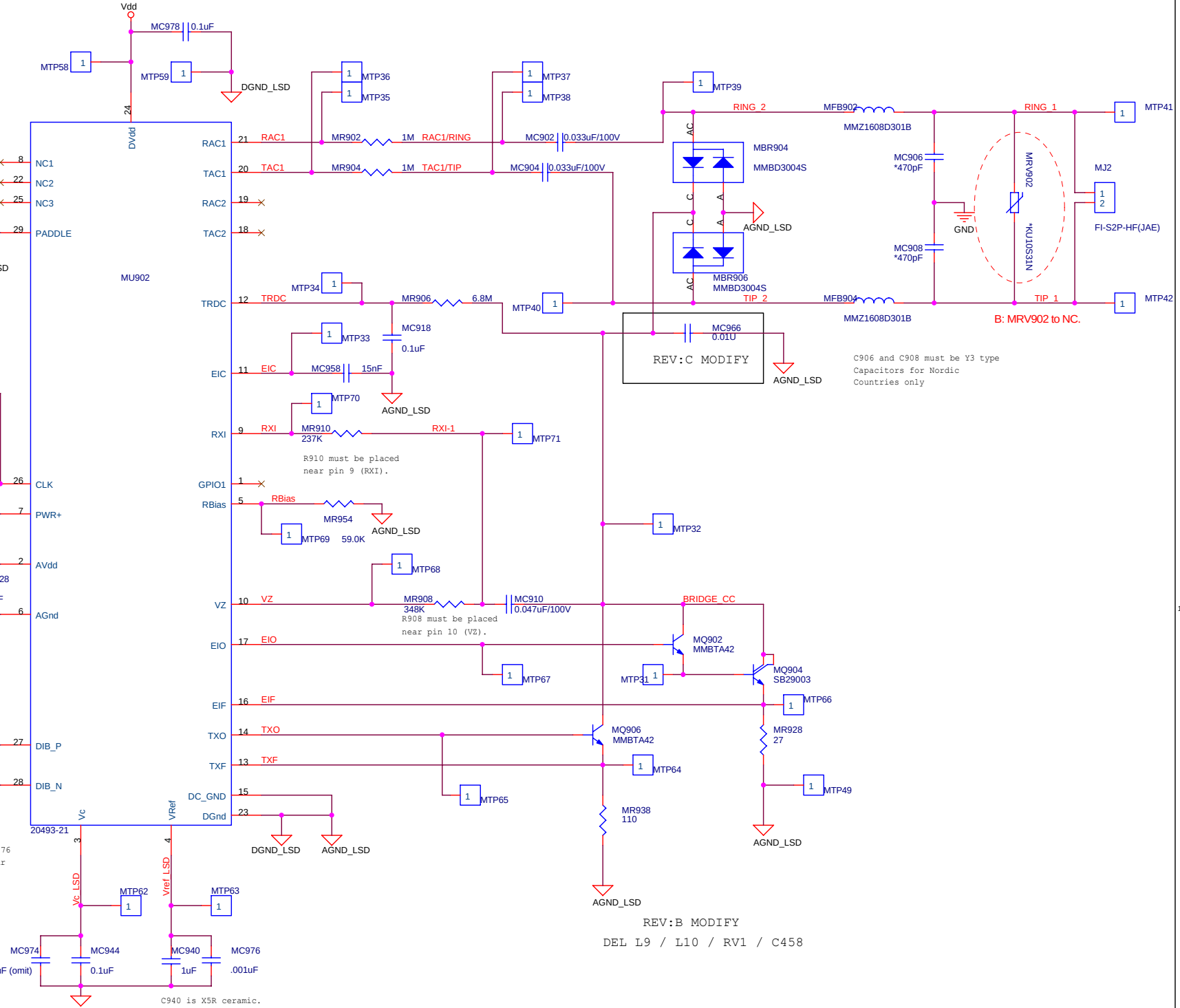
A

[illegible]



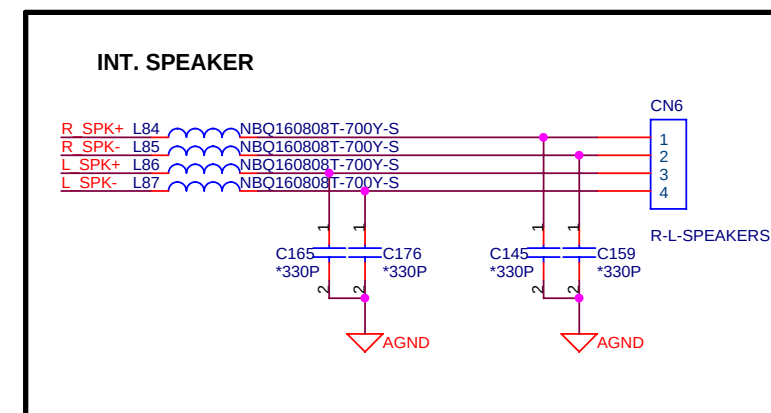
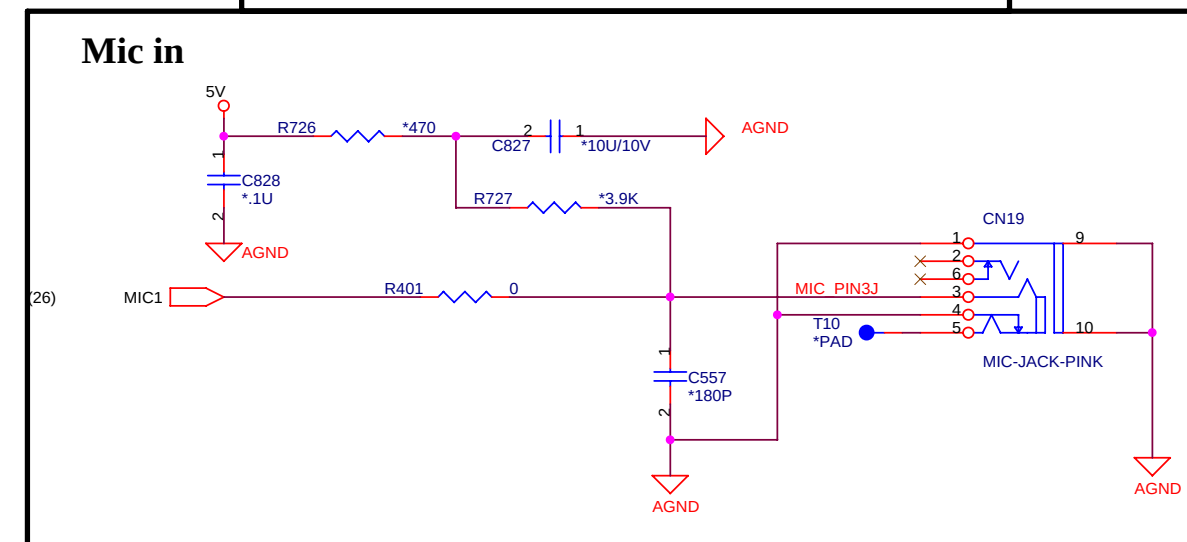
Size	Document Number SMARTAMC-CONEXANT_20468-31	Rev 2A
Date:	Friday, May 21, 2004	Sheet 26 of 39

REV:B MODIFY FOR USE
NEW MODEM MODULE

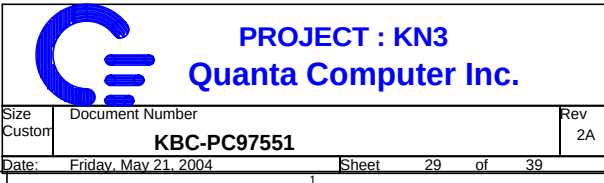


28

Gain0	Gain1	Av
0	0	2 times
0	1	4 times
1	0	12 times
1	1	24 times

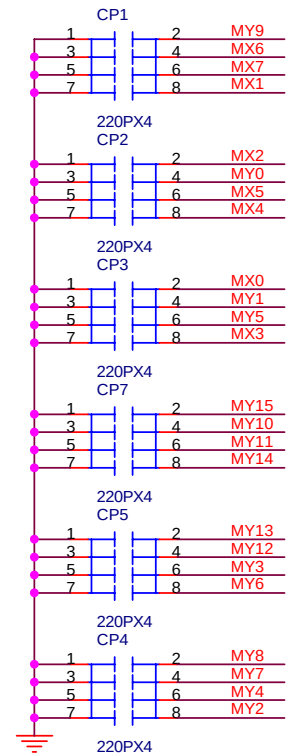
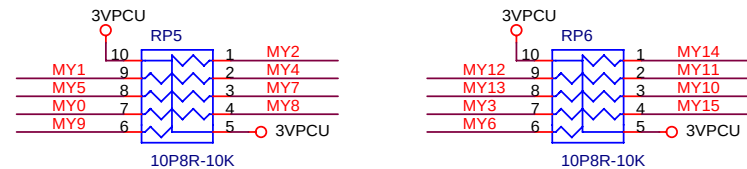
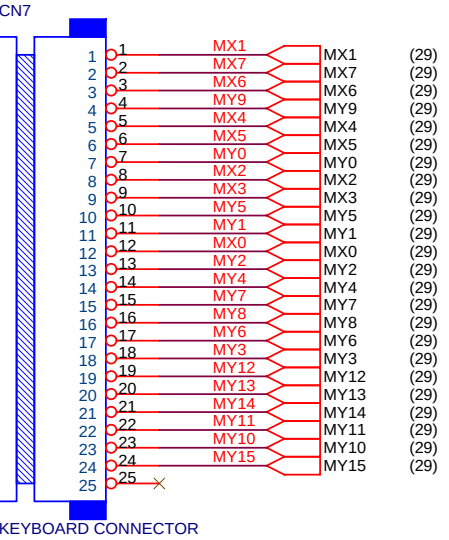


29

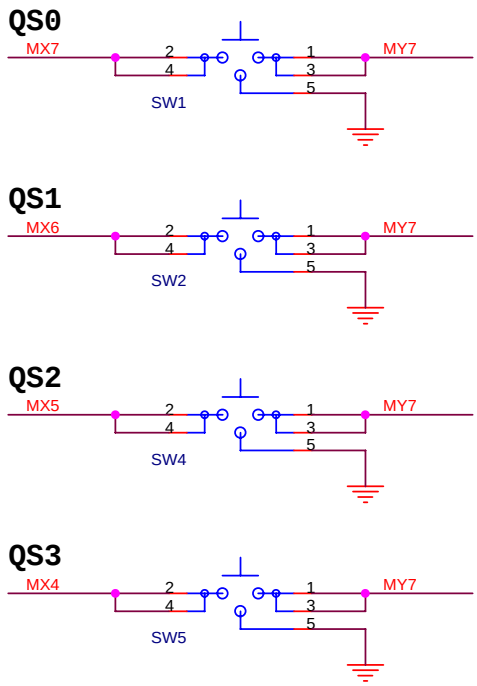


KEYBOARD CONN & INDICATOR

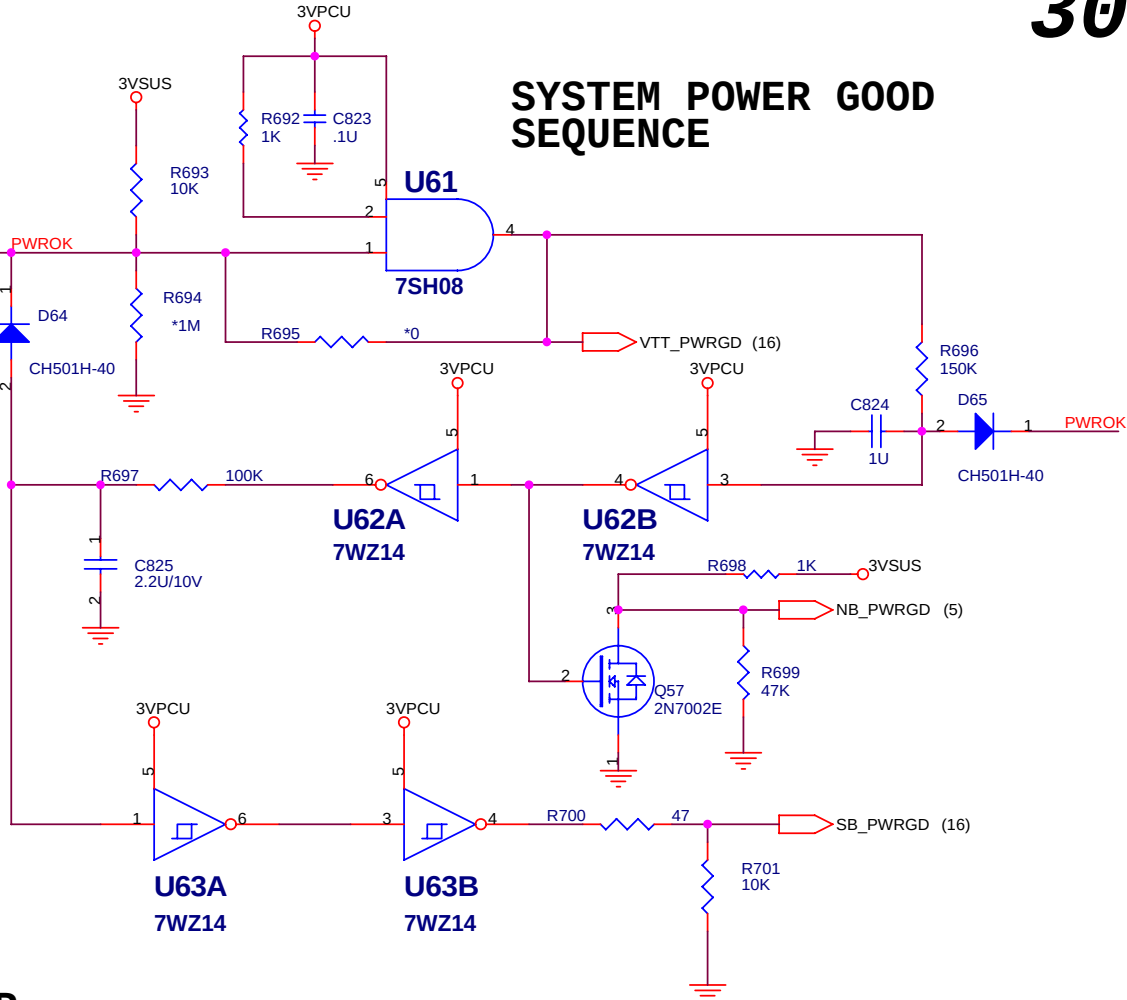
KEYBOARD CONNECTOR



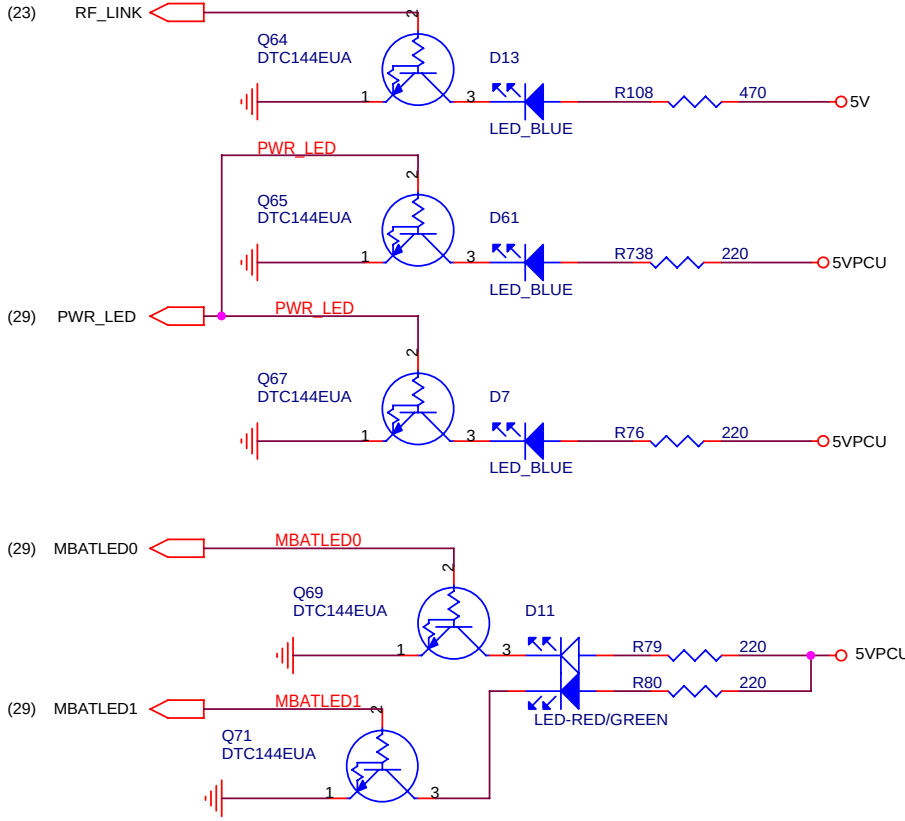
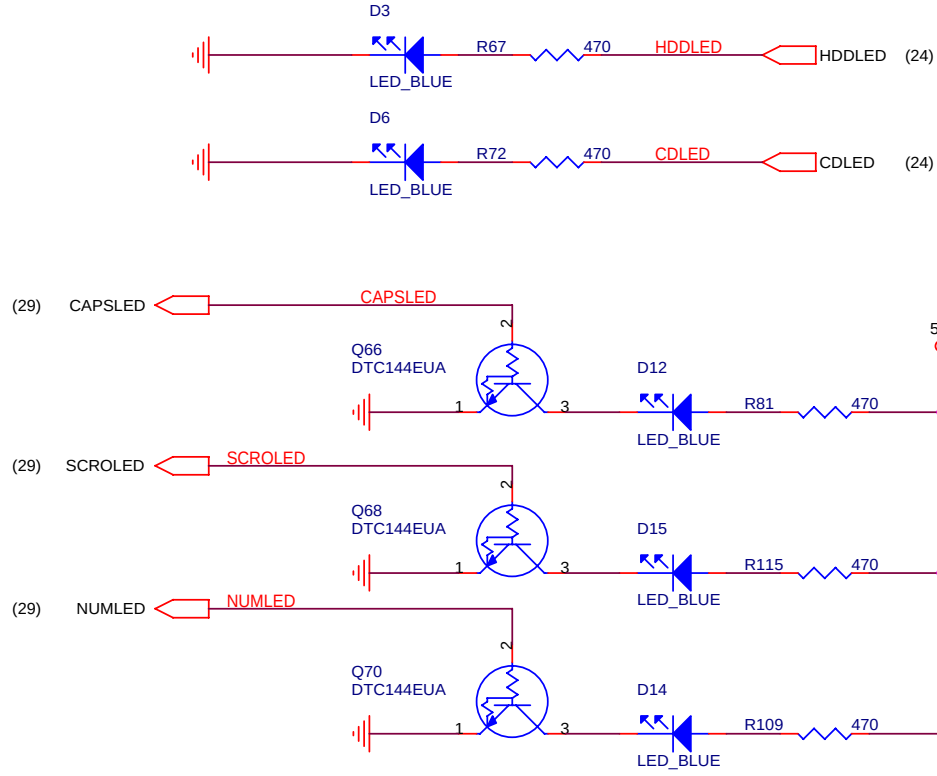
QUICK SWITCH



SYSTEM POWER GOOD SEQUENCE

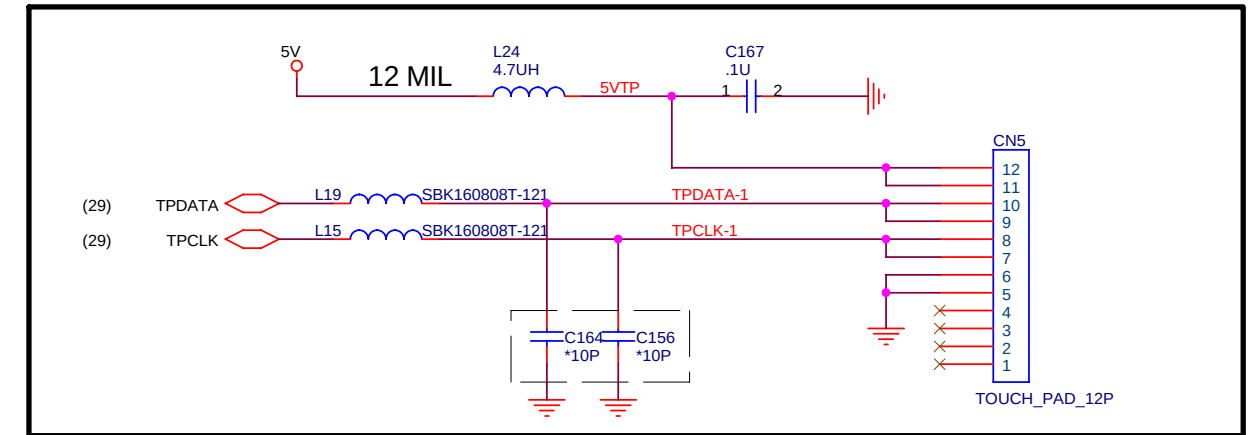


SYSTEM INDICATOR



31

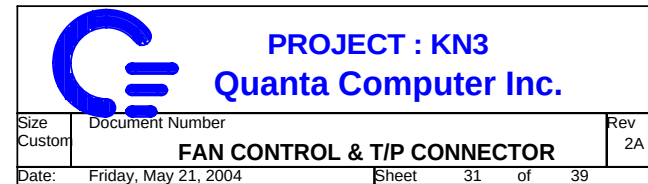
TOUCH PAD CONN.



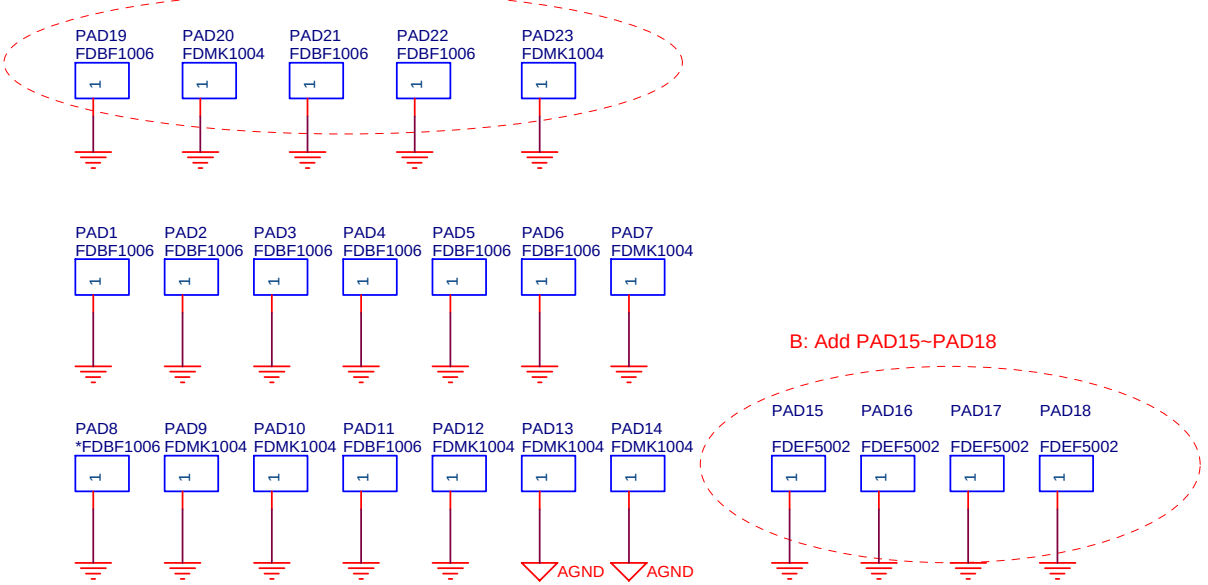
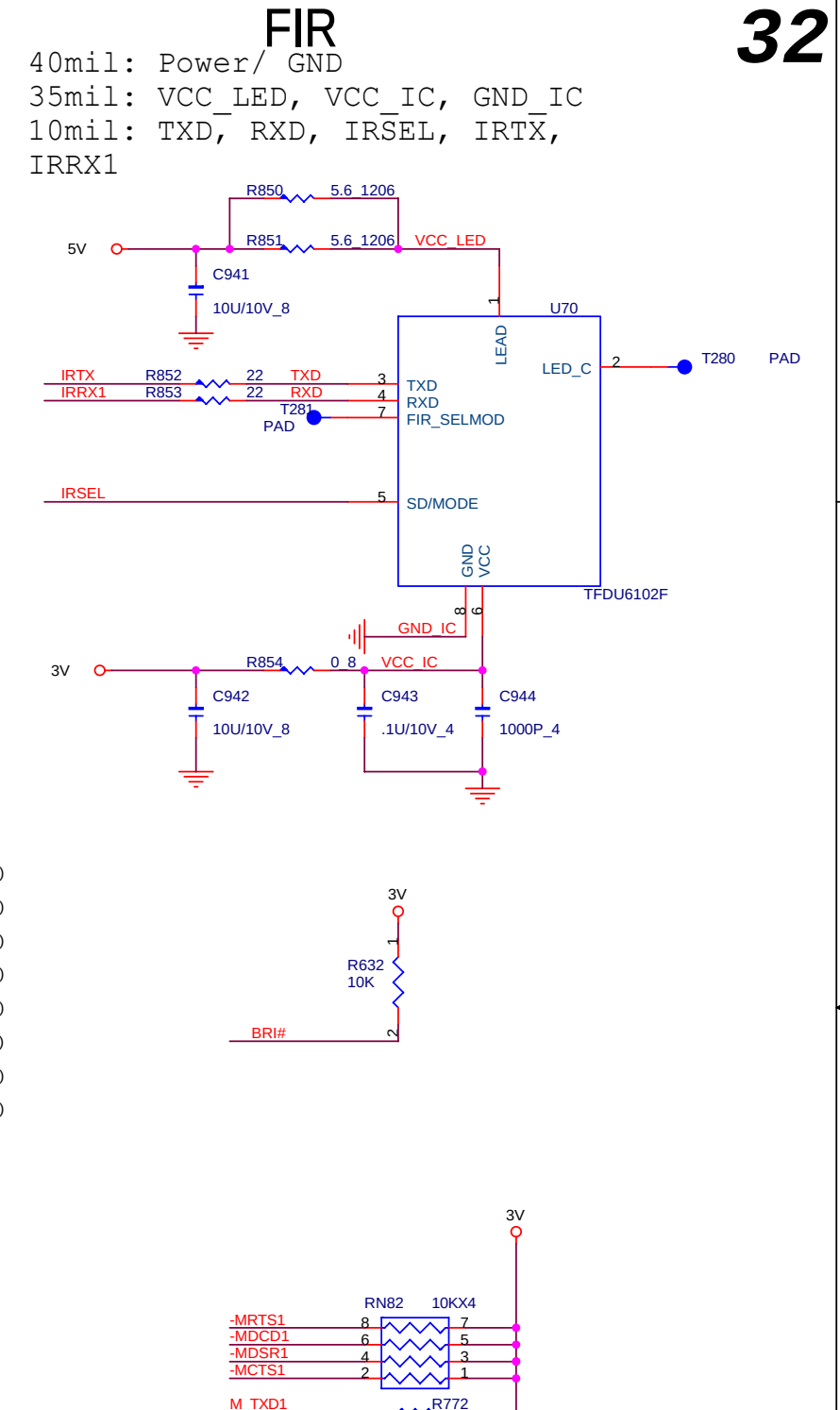
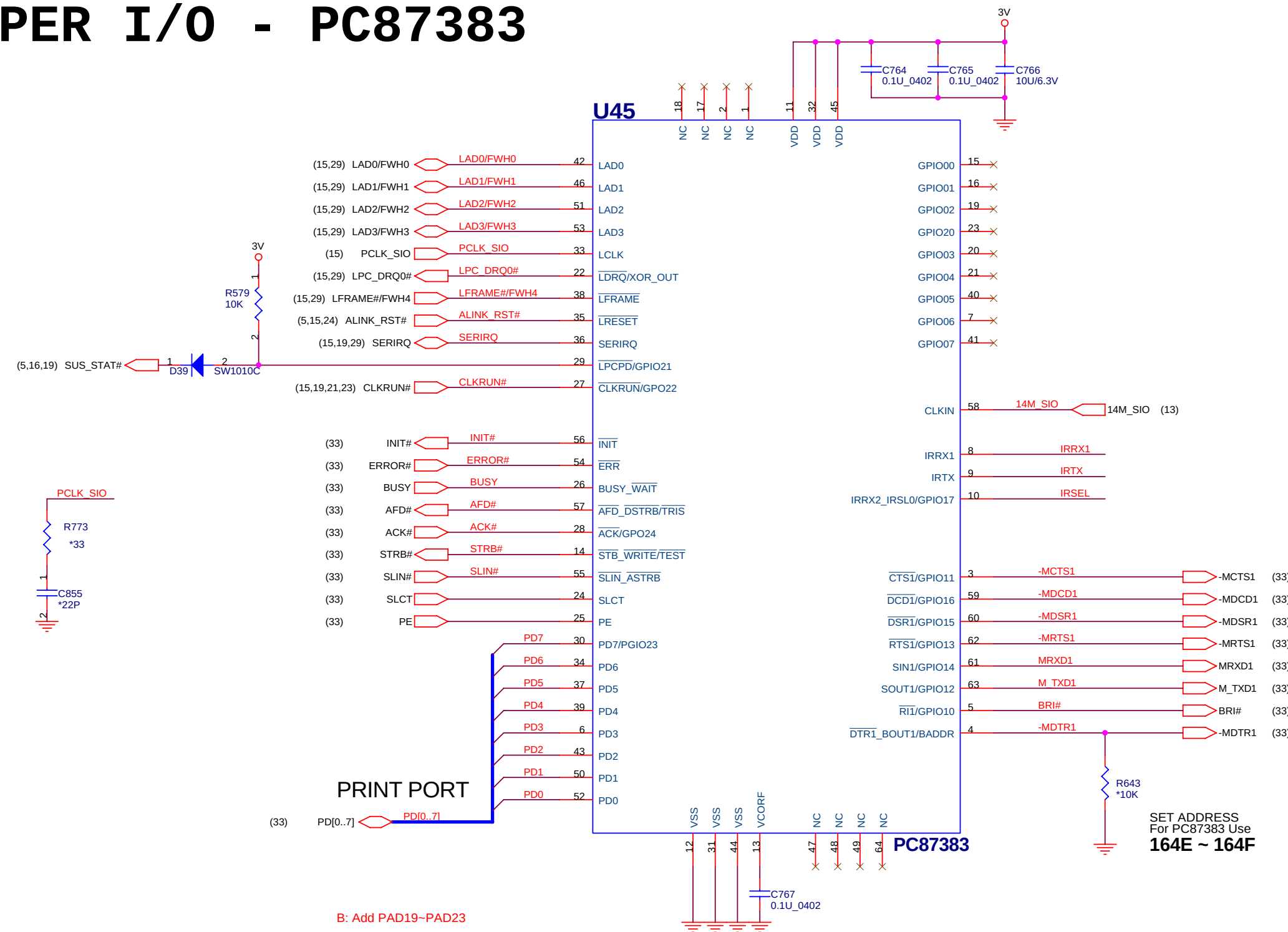
VFAN = 0-5V DC or PWM (R5 330K)

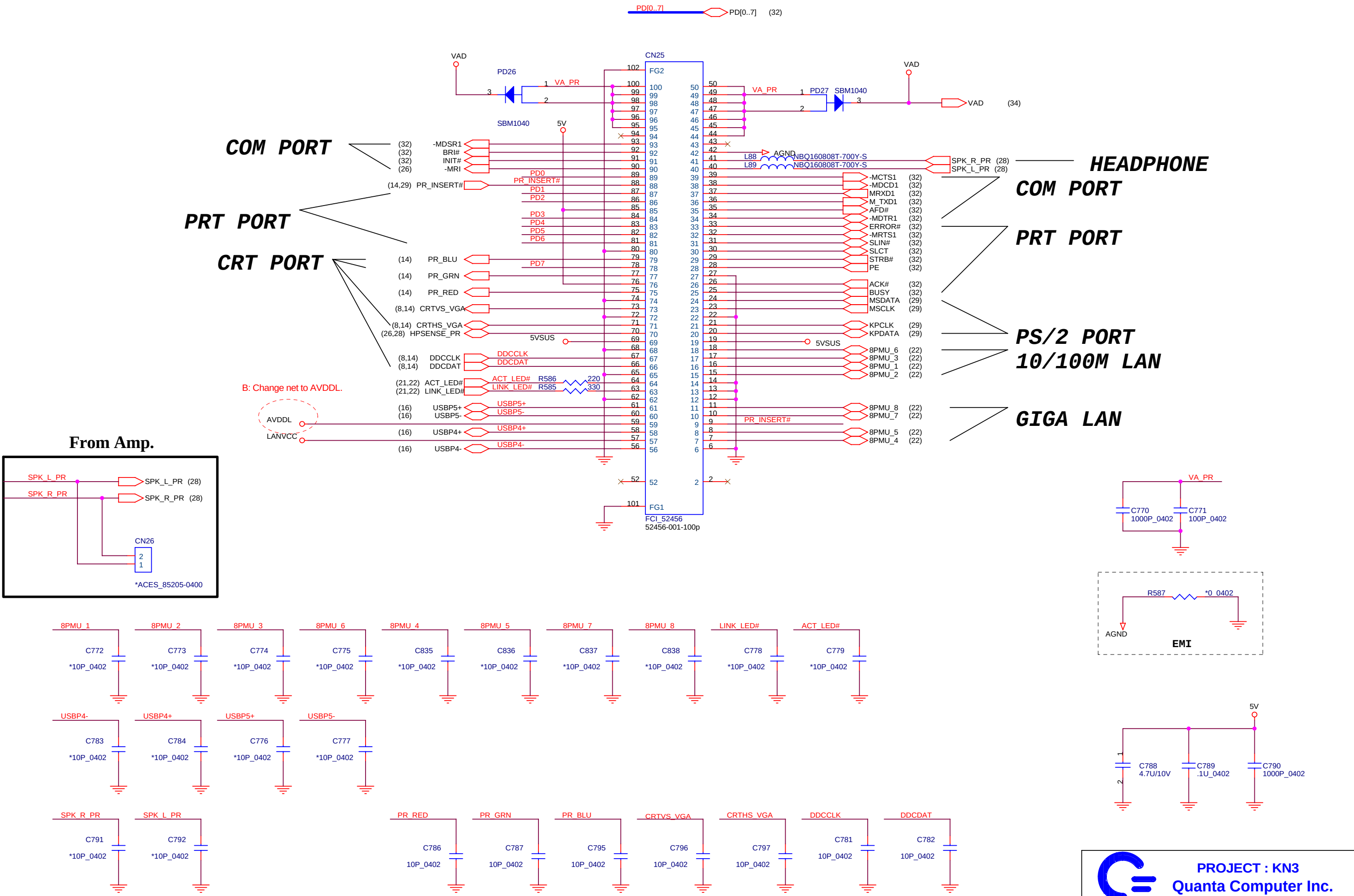
H3 H-C354D110P2 H-C354D110P2	H4 H-C295D110P2 H-C295D110P2	H20 H-C295D110P2 H-C295D110I160P2	H21 H-C295D110P2 H-C295D110P2	
H15 H-C354D110P2 H-C354D110P2	H14 H-C295D110P2 H-C295D110P2	H22 H-C295D110P2 H-C295D110P2	H25 H-C295D157P2 H-C295D157P2	H26 H-C295D110P2 H-C295D110P2
H8 H-C315D157P2 H-C315D157P2	H9 H-C315D157P2 H-C315D157P2	H6 H-C315D157I187P2 H-C315D157I187P2	H7 H-C315D157I187P2 H-C315D157I187P2	H10 H-C315D157I187P2 H-C315D157I187P2
H1 H-C220D150P2 H-C220D150P2	H2 H-C335D110P2 H-C335D110P2	H5 H-C315D315N H-C315D315N	H19 H-C295D110I160P2 H-C295D110I160P2	H23 H-C295D110I160P2 H-C295D110I160P2

B: Delete Q106,Q107,R860 for H/W throttling.

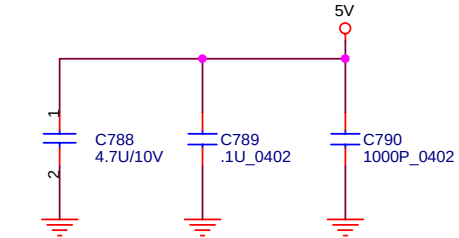
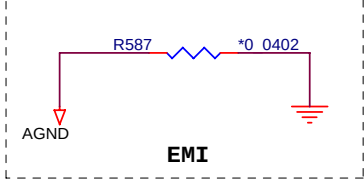
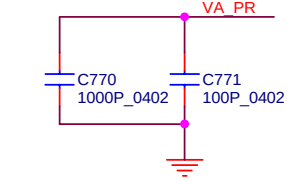
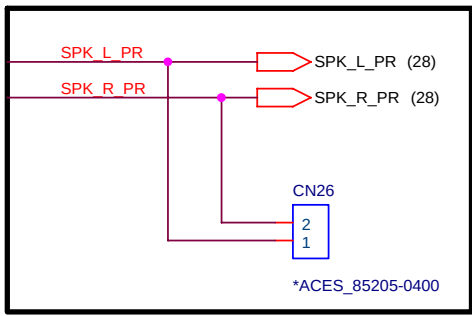


SUPER I/O - PC87383





From Amp.



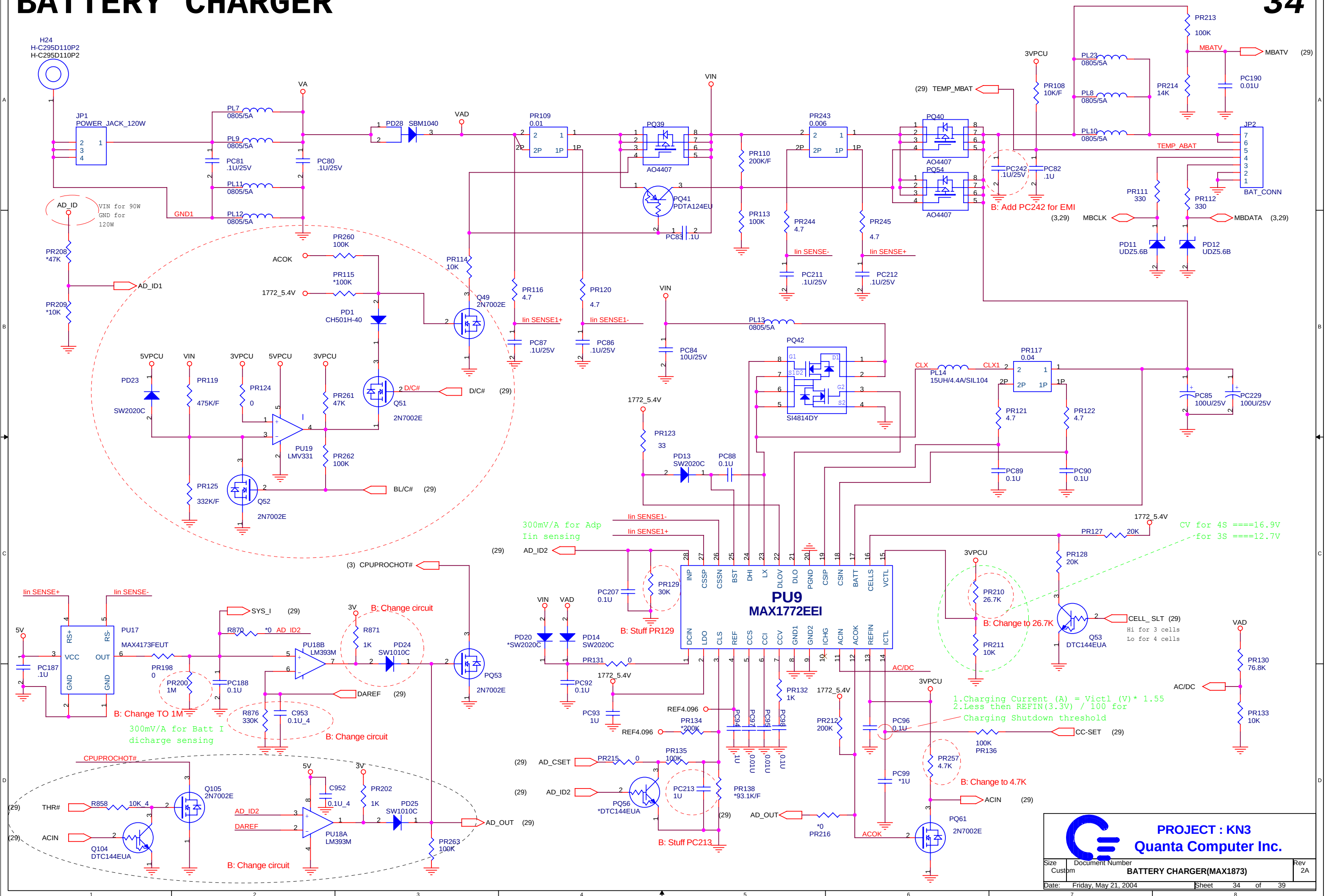


PROJECT : KN3

Quanta Computer Inc.

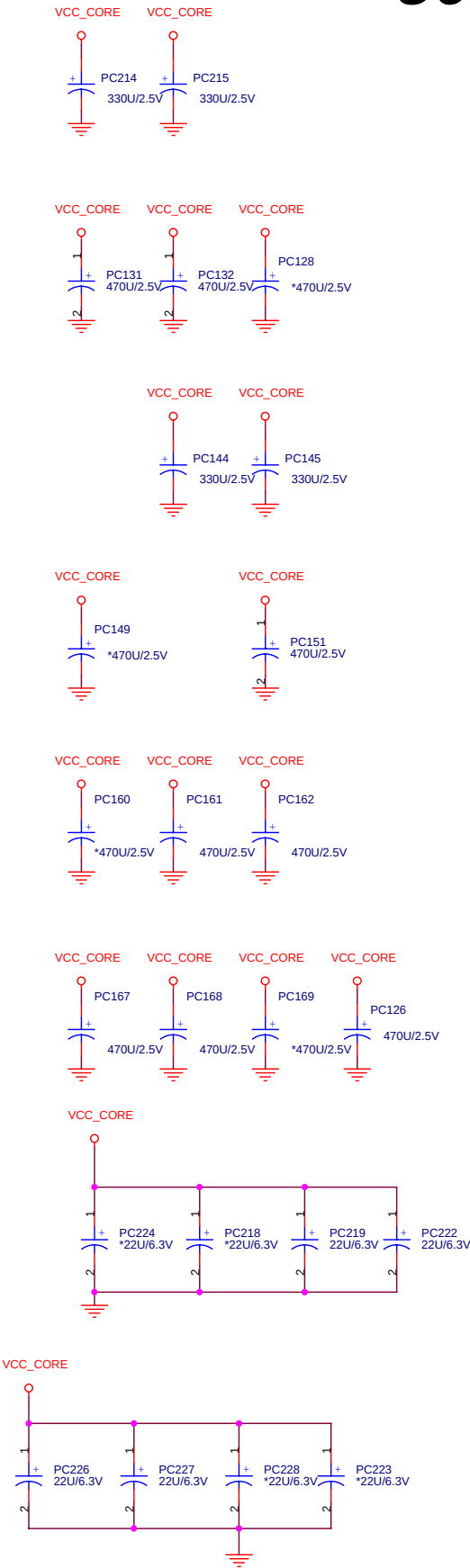
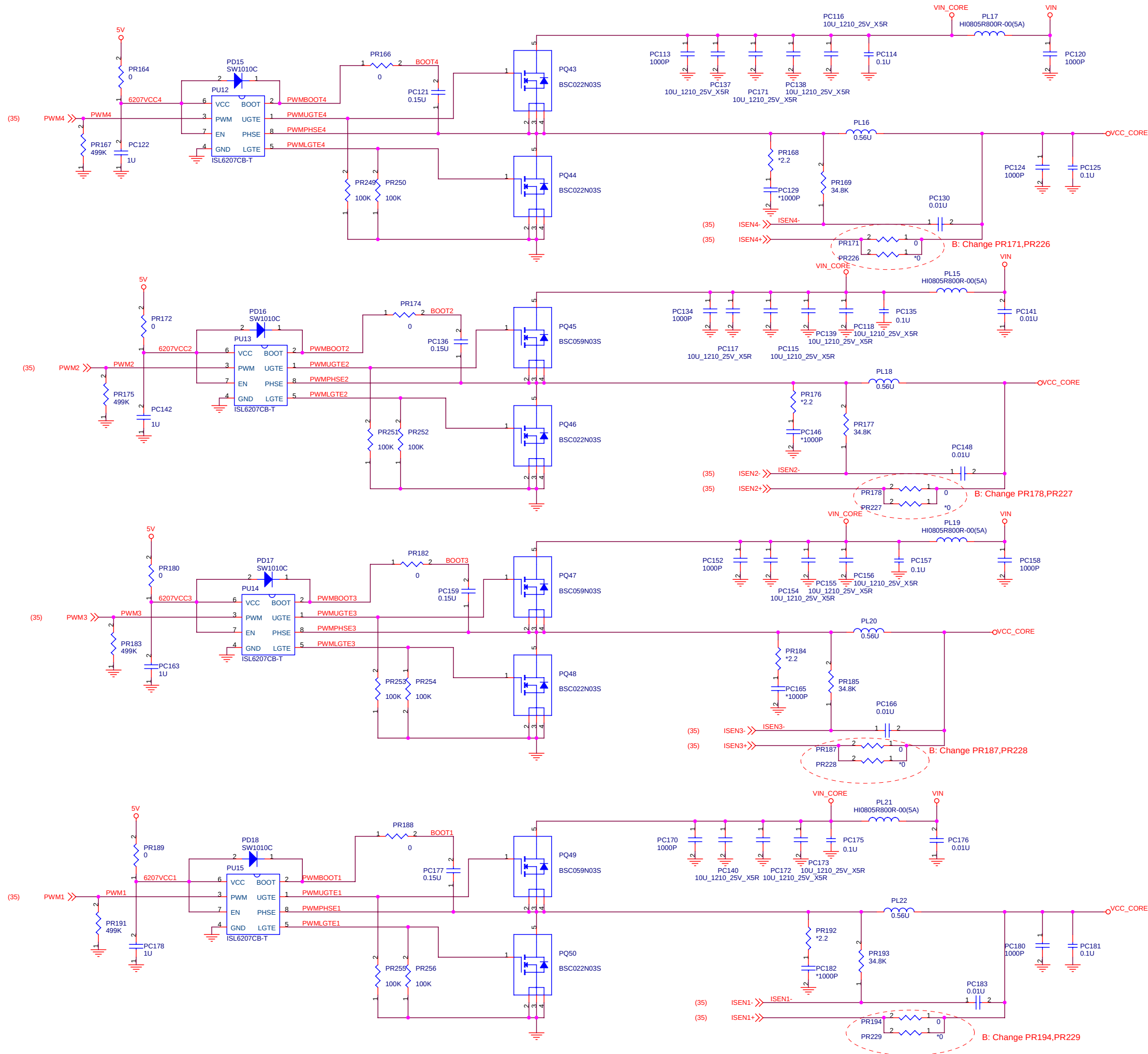
Size	Document Number	Rev
Custom	PORT REPLICATOR	2A
Date:	Friday, May 21, 2004	Sheet 33 of 39

34

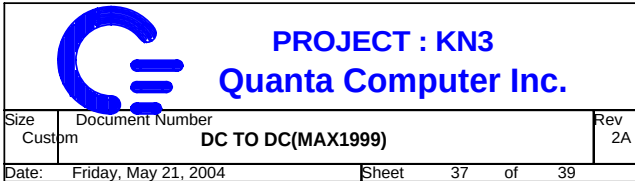


VCORE-2(Power train)

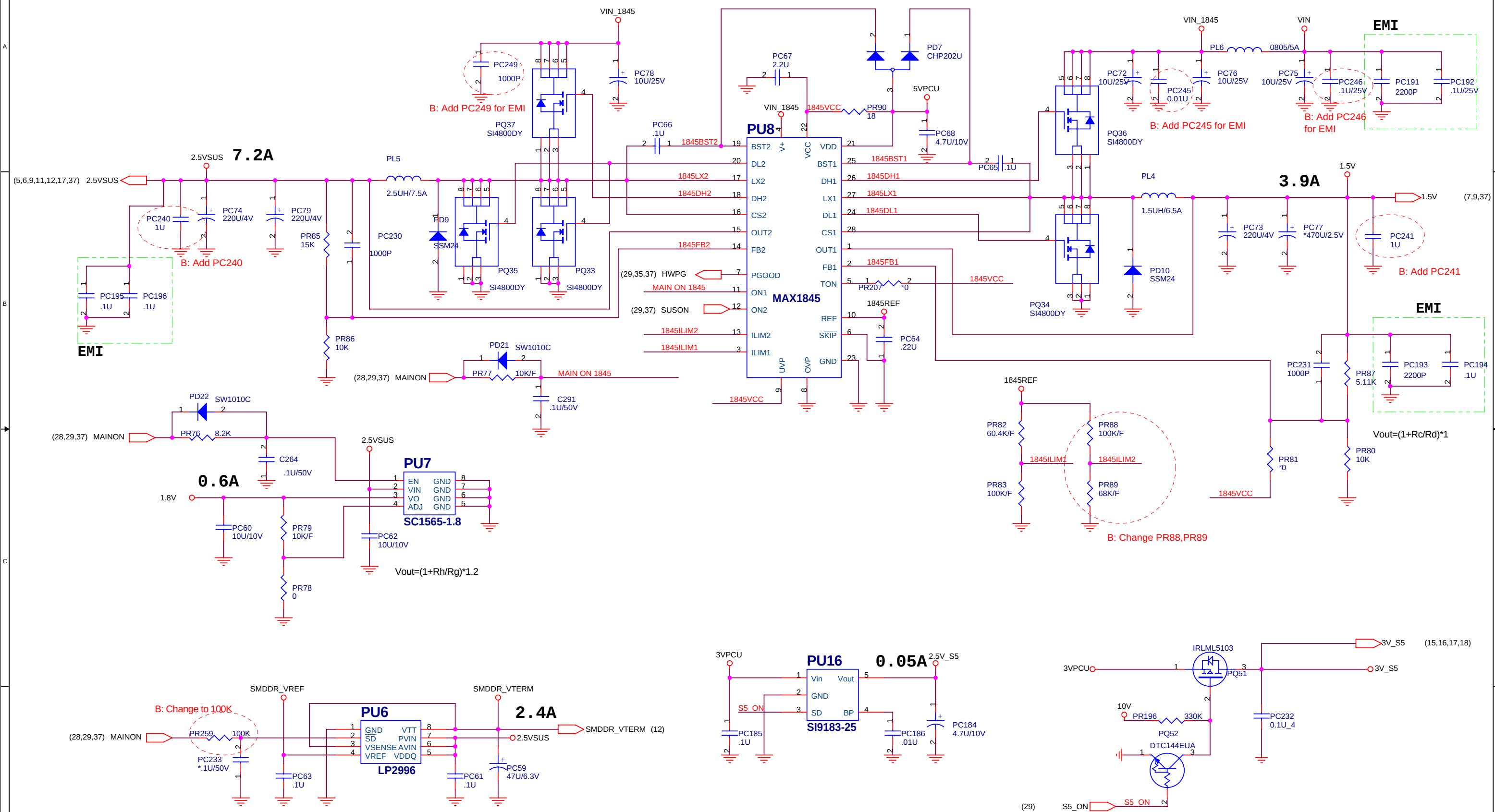
36



37



DC/DC MAX1845(2.5V&1.5V), 1.8V&1.25V

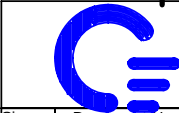


MODEL	REV	CHANGE LIST	MODEL		
			PAGE	KN3	
				FROM	TO
KN3 Main Board	1A	First Release	01	1A	
			02	1A	
			03	1A	
			04	1A	
			05	1A	
			06	1A	
			07	1A	
			08	1A	
			09	1A	
			10	1A	
			11	1A	
			12	1A	
			13	1A	
			14	1A	
			15	1A	
			16	1A	
			17	1A	
			18	1A	
			19	1A	
			20	1A	
			21	1A	
			22	1A	
			23	1A	
			24	1A	
			25	1A	
			26	1A	
			27	1A	
			28	1A	
			29	1A	
			30	1A	
			31	1A	
			32	1A	
			33	1A	
			34	1A	
			35	1A	
			36	1A	
			37	1A	
			38	1A	
			39	1A	



PROJECT : KN3
Quanta Computer Inc.

Size Custom	Document Number RELEASE NOTE	Rev 2A
Date: Friday, May 21, 2004		Sheet 39 of 39



PROJECT : KN3
Quanta Computer Inc.