

BY2D Block Diagram

PCB 8 layer Stackups

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

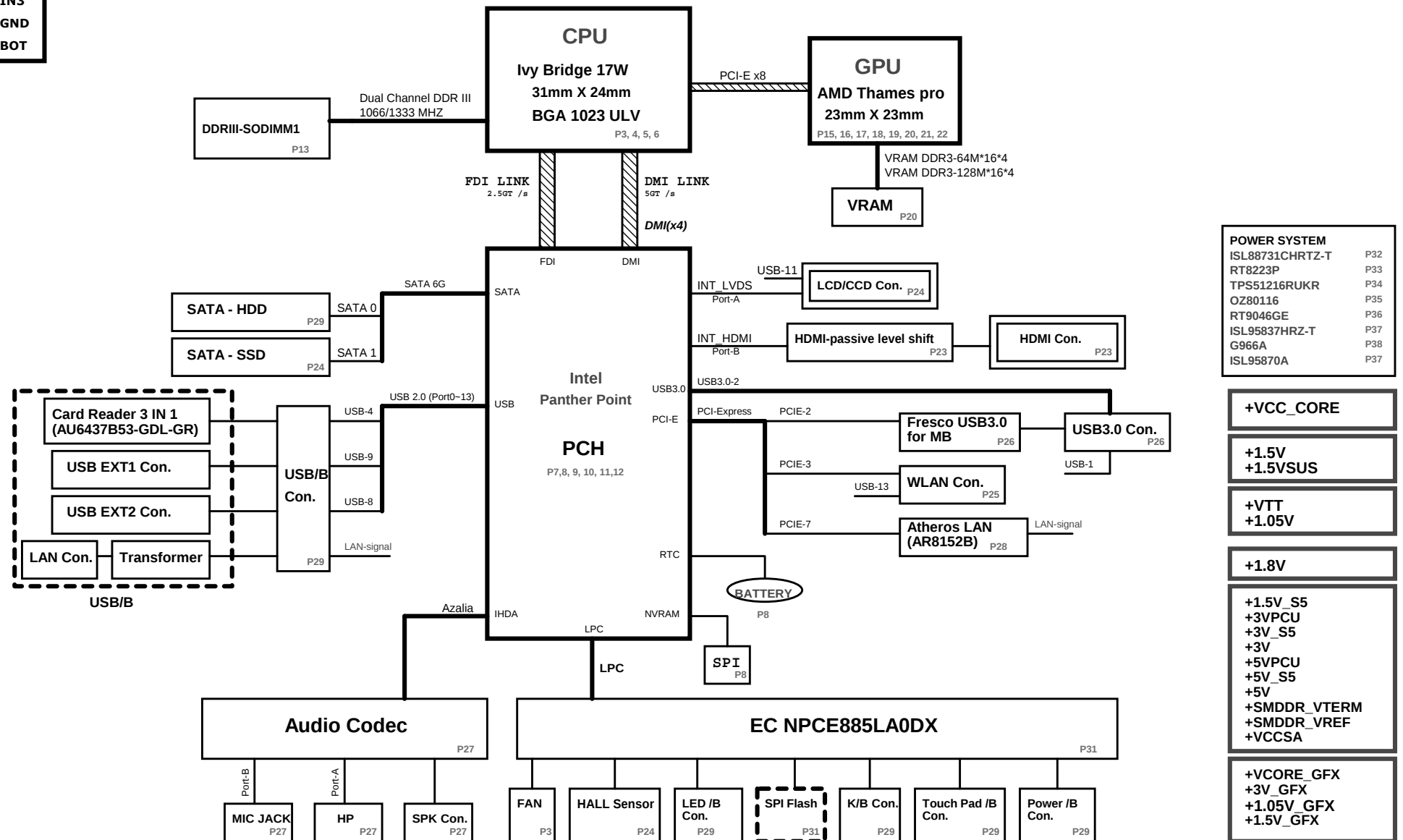


Table of Contents

PAGE	DESCRIPTION	BOI-FUNCTIONS
1	Schematic Block Diagram	
2	Front Page	
3-6	Processor	CPU
7-12	PCH	CLG
8	RTC	RTC
13	DDRIII SO-DIMM	DDR
15-22	VGA	VGA
14	S3 Power reduction	S3P
21	VGA Thermal sensor	THV
22	AMD BACO	SWA
23	HDMI comm part	HDM
24	LCD Panel	LDS
	CCD	CCD
	HALL SENSOR&BACK LIGHT SWITCH	HSR
	mSATA	H1D
25	MINI Card (Wi-Fi & WIMAX)	MNW
26	USB Connector	U3B/USB
	USB w S&C	SLC
27	Audio Codec(CX20671-21Z)	ADO
28	Atheros LAN (AR8152B)	LAN
29	INT KeyBoard & K/B LED Power	KBC
	LED Board	LED
	TP&FP board	TPD,FPD
	Power SW	PSW
	USB Connector	U2B
	SATA HDD Connector	H2D
	Card reader	MMC
30	HOLE	FMM
31	EC NPCE795LA0DX	KBC
32	Charger (ISL88731C)	CHR
33	System 5V/3V (RT8223)	PWM
34	DDR(TPS51216RUKR)	PWM
35	+VTT/+1.05V (OZ80116)	PWM
36	+VCCAS(RT9046GE)	PWM
37	+VCC_CORE(ISL95837CRZ)	PWM
38	+1.8V (G966A)/Discharge	PWM
39	AMD_GPU(ISL95870A)-1	PWM
40	AMD_GPU-2	PWM
41	POWER TREE	
42	EE Change List	

Power plant table

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States
			ACTIVE IN
VIN	6V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P for EC	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT/+1.05V	+1.05V	MAIN_ON	S0
+VCCSA	+0.75V~+0.9V	HWPG_VCCIO	S0
+VAXG		GFXVR_EN	S0
+3V_GPU	+3.3V	DGPU_PWR_EN#	S0
+1.8V_GPU	+1.8V	DGPU_PWR_EN	S0
+1.5V_GPU	+1.5V	DGPU_PWROK	S0
+1V_GPU	+1V	DGPU_PWR_EN	S0
+BIF_VDDC	+0.875V~+1V	DGPU_PWROK	S0
+VGPU_CORE	+0.875V~+1V	PX_PWRGOOD	S0

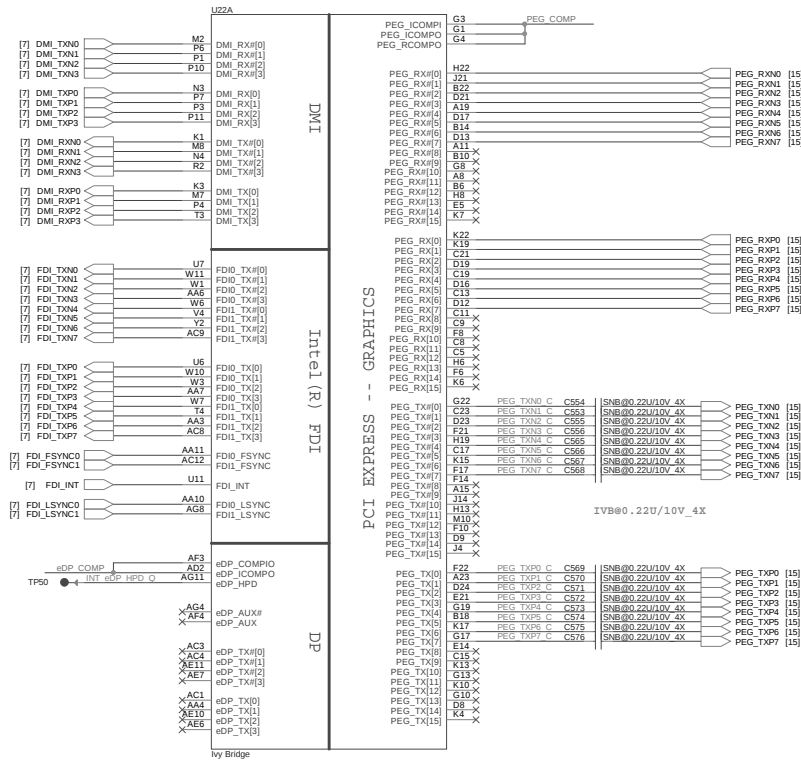


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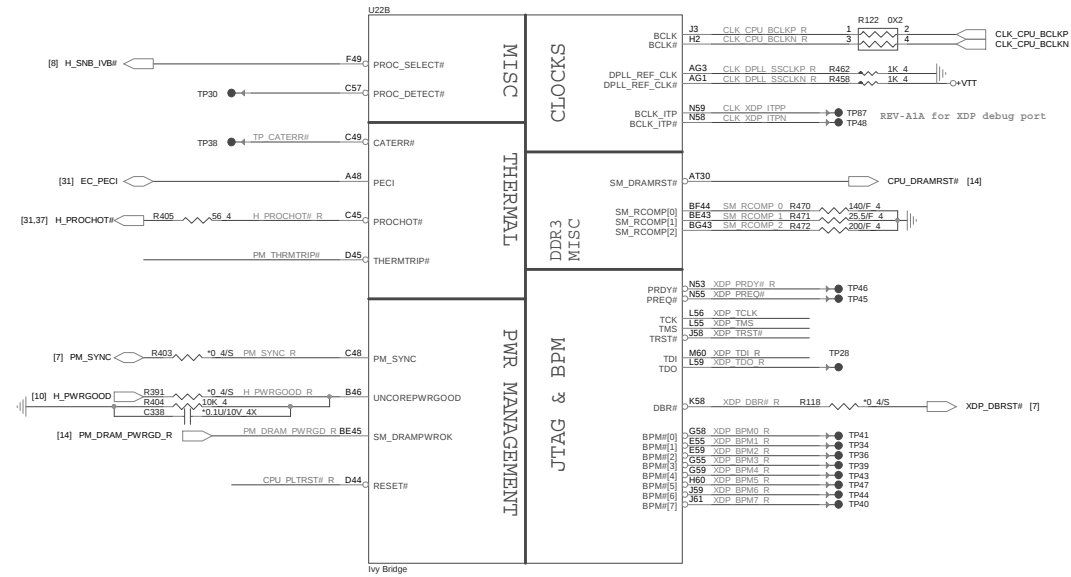
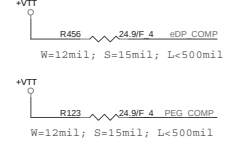
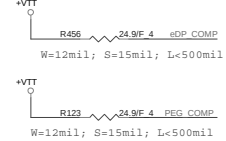
PROJECT : BY2D

Size	Document Number	Rev
	POWER STAGE AND BOI-FUNCTION	3B
Date:	Monday, March 26, 2012	Sheet 2 of 42

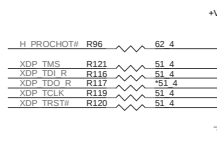
Ivy/Sandy Bridge Processor (DMI,PEG,FDI)



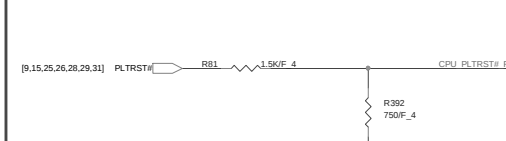
Ivy/Sandy Bridge Processor (CLK,MISC,JTAG)

FDI Disabling (Discrete Only)
<CPU>DP & PEG Compensation
<CPU>

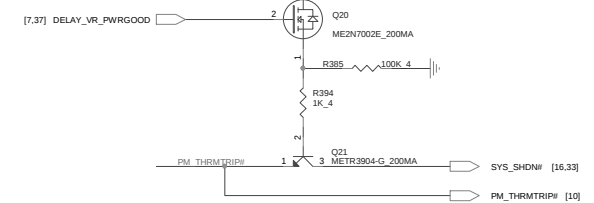
Processor pull-up <CPU>



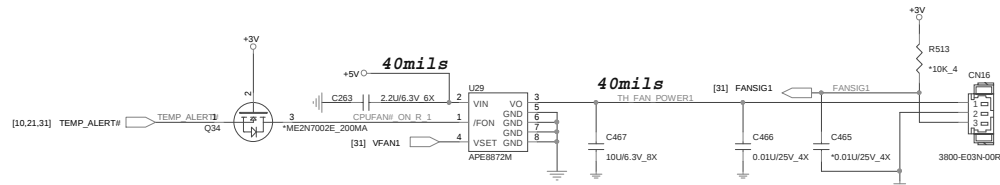
Level Shift <CPU>



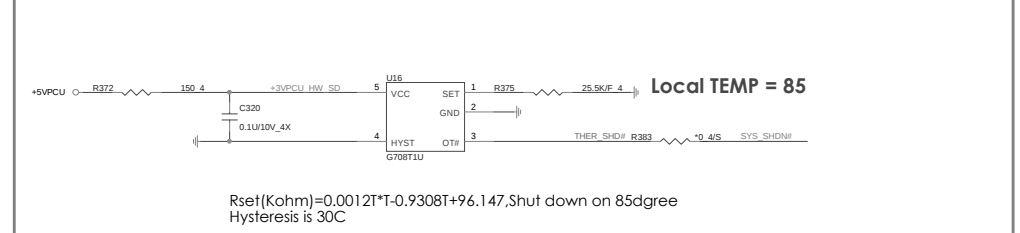
Thermal Trip<CPU>



FAN Control-->For one FAN solution <THC>

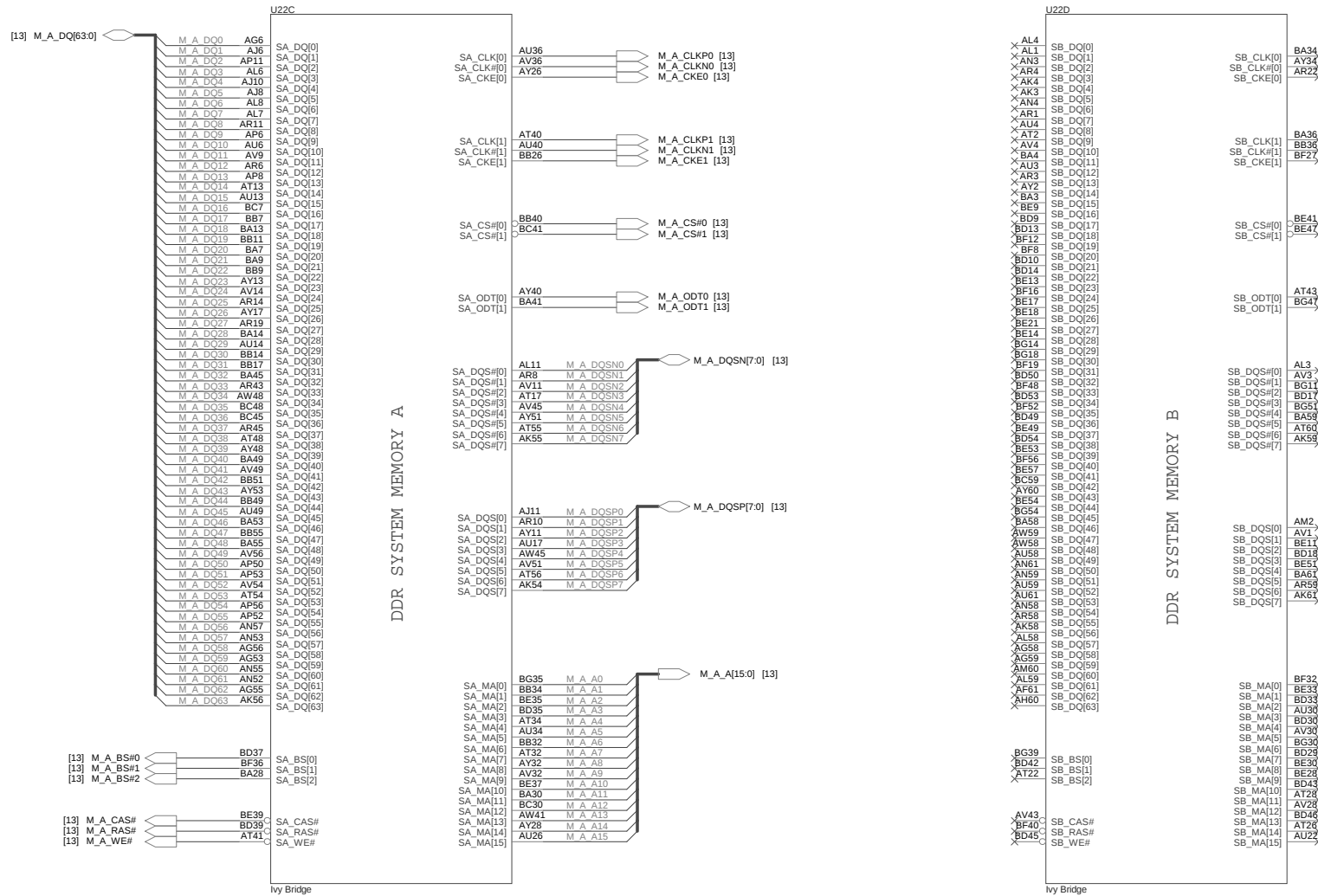


CPU Thermal sensor / MB Local TEMP <THC>

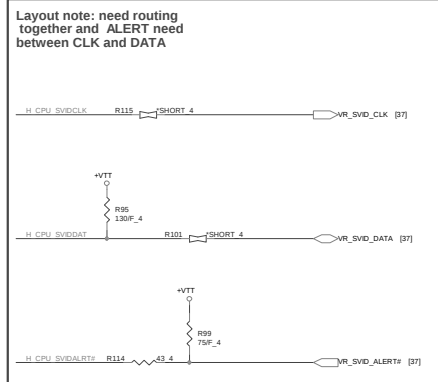


Ivy/Sandy Bridge Processor (DDR3)

04

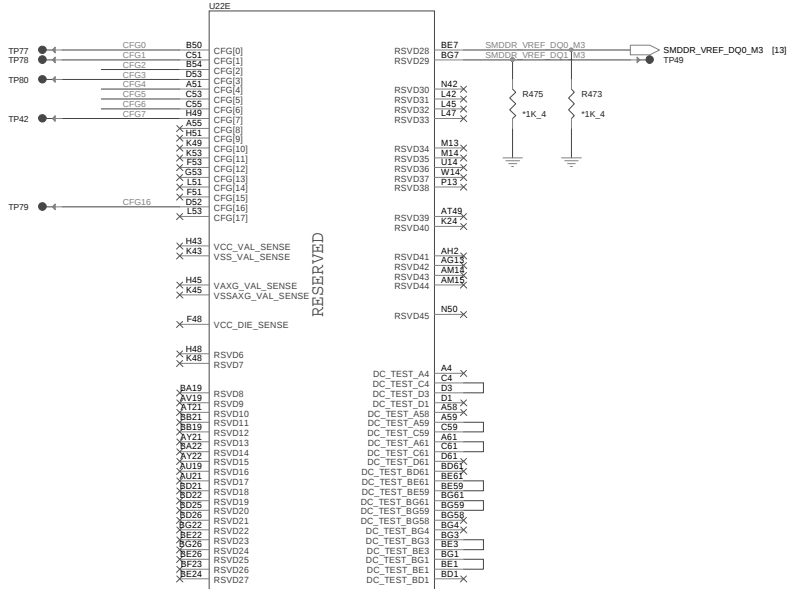
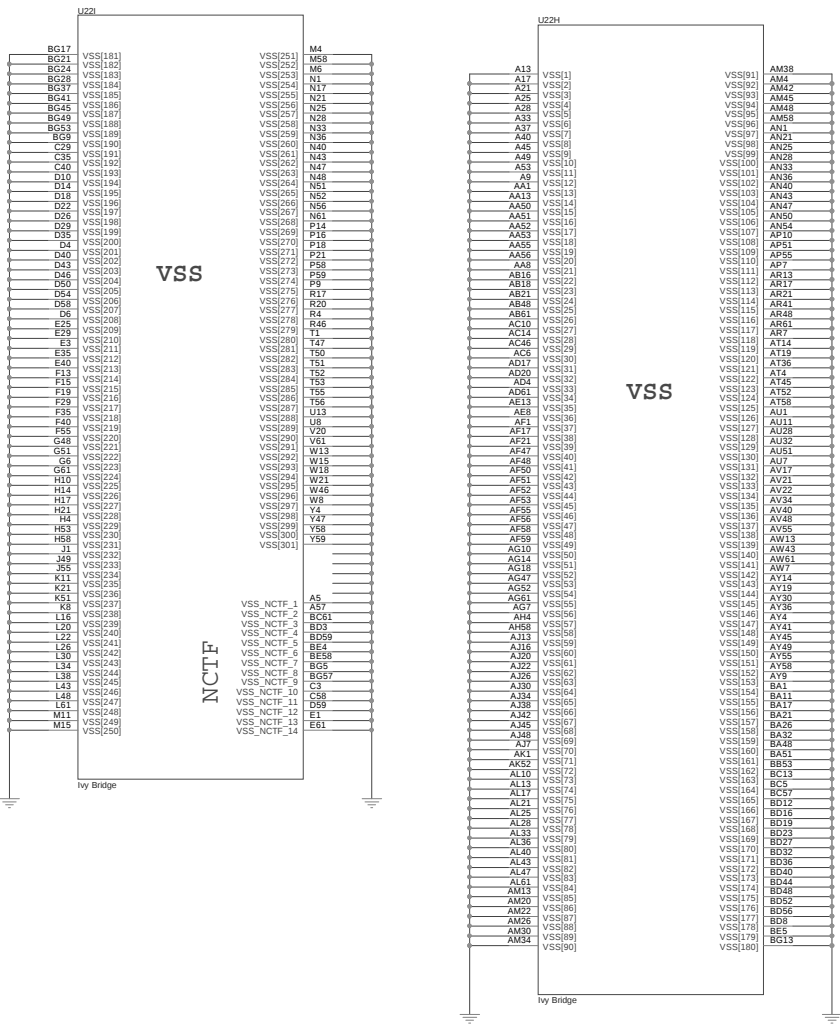


Ivy/Sandy Bridge Processor (GRAPHIC POWER)



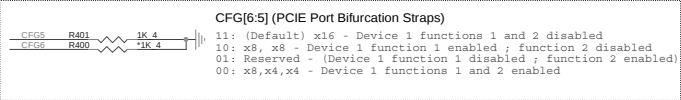
Ivy/Sandy Bridge Processor (GND)

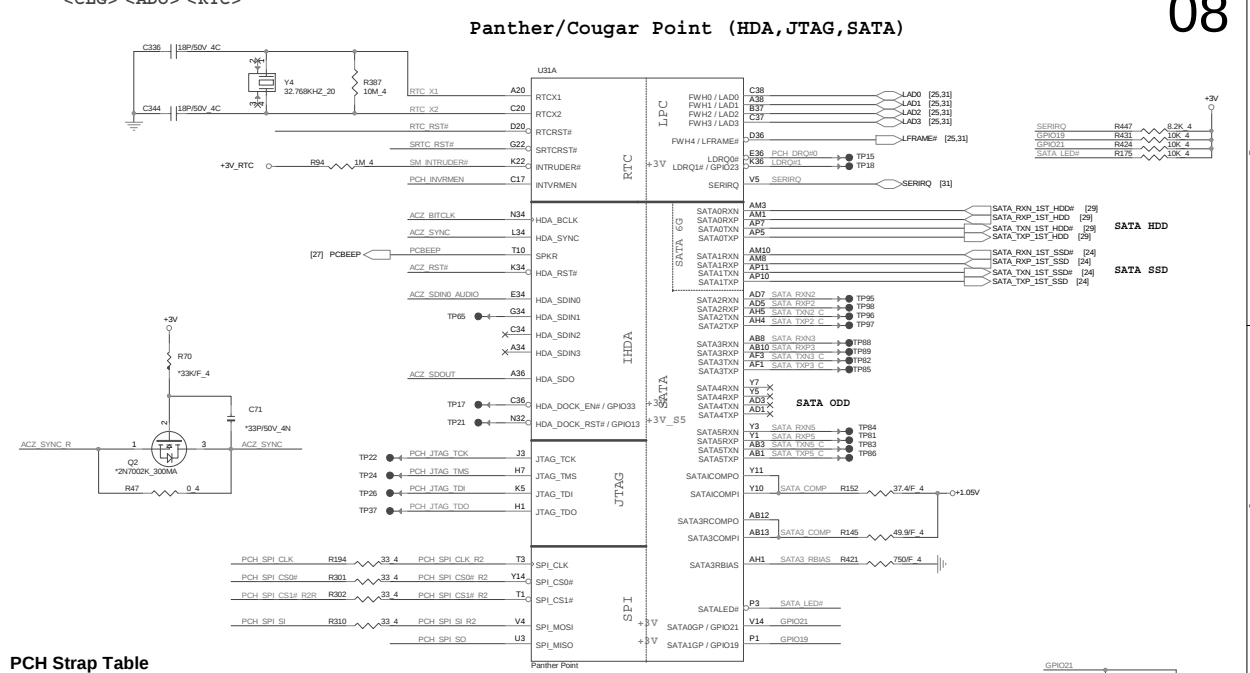
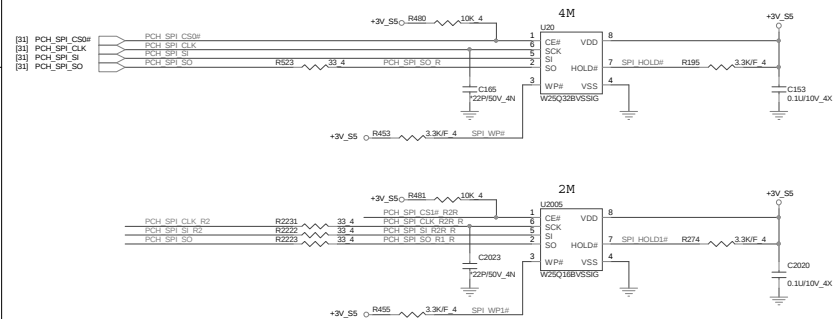
Ivy/Sandy Bridge Processor (RESERVED, CFG)



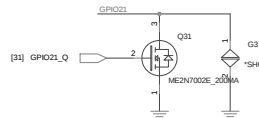
Processor Strapping

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP



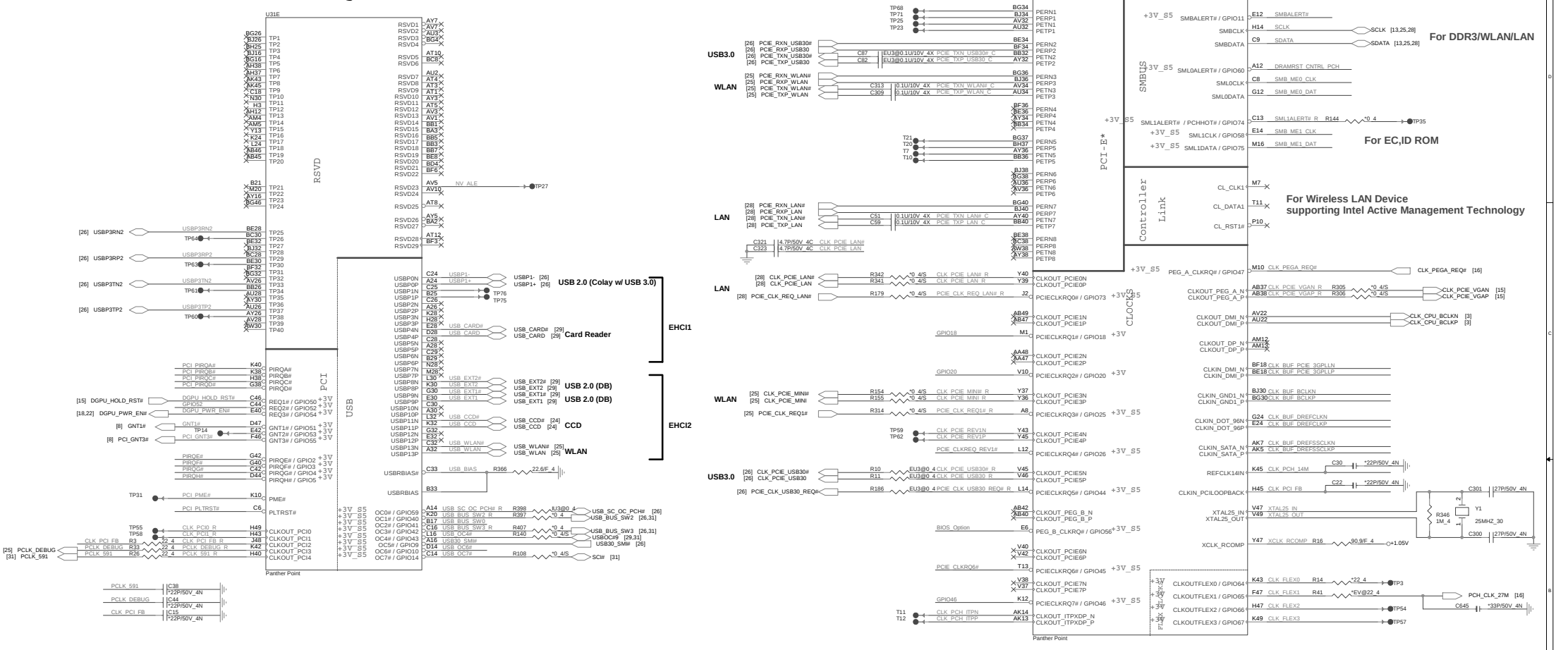


Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT3#</th><th>GPIO19</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	GNT3#	GPIO19	Boot Location	1	1	SPI *	0	0	LPC	
GNT3#	GPIO19	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)										
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)										
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
GPIO15	TLS Confidentiality	RSMRST	0 = Default, TLS No Confidentiality 1 = TLS Confidentiality										
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable										
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	Should not pull low, leave as No Connect									
GNT2# / GPIO53	ESI Strap (Server Only)	PWROK	1 = Default, Should not be pulled low for desktop and mobile	Should not pull low for desktop and mobile									
L_DDC_DATA	LVDS Detected	PWROK	0 = Default, Not Detected 1 = Detected	1= PU to 3V									
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default, Not Detected 1 = Detected	1= PU to 3V									
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default, Not Detected 1 = Detected	0=NC									
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default, Not Detected 1 = Detected	0=NC									
SATA3GPI / GPIO37	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									
SATA2GPI / GPIO36	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									

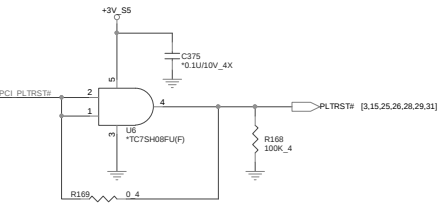


Panther/Cougar Point-M (PCI-E, SMBUS, CLK)

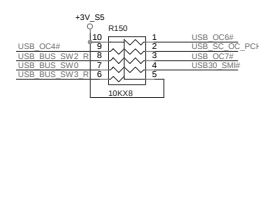
Panther/Cougar Point-M (PCI, USB, NVRAM)



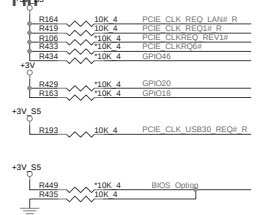
PLTRST# <CLG>



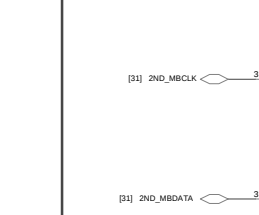
PCI/USBOC# Pull-up <CLG>



CLK_REQ/Strap <CLG>



SMBus/Pull-up <CLG>

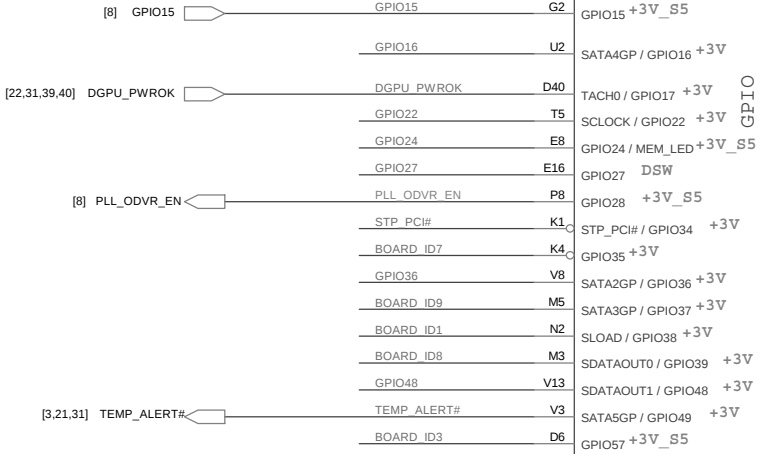


	33MHz	27MHz	18/24MHz	14.318MHz	25MHz
CLK_FLEX0					
CLK_FLEX1					
CLK_FLEX2					
CLK_FLEX3					

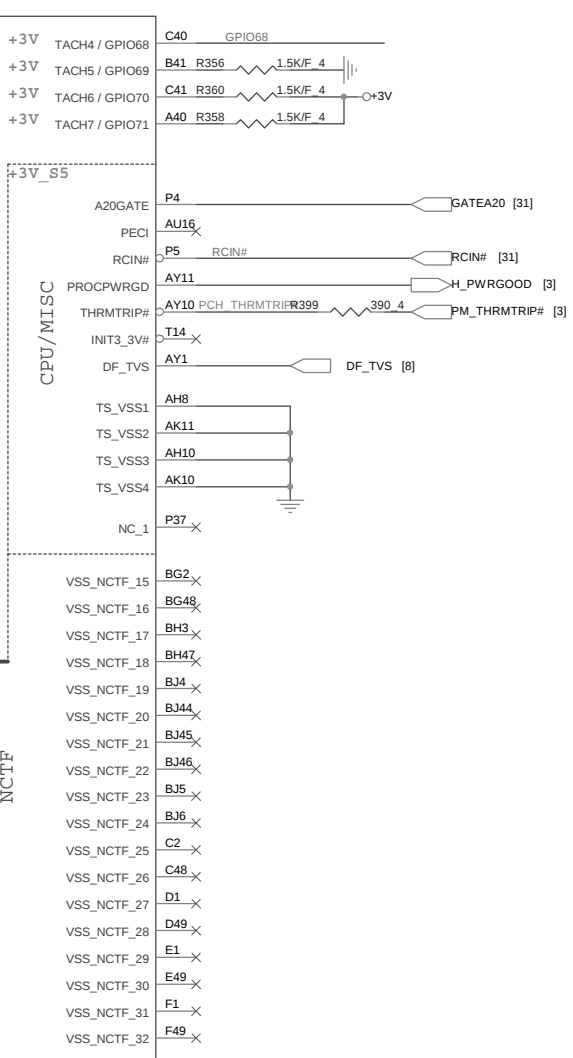
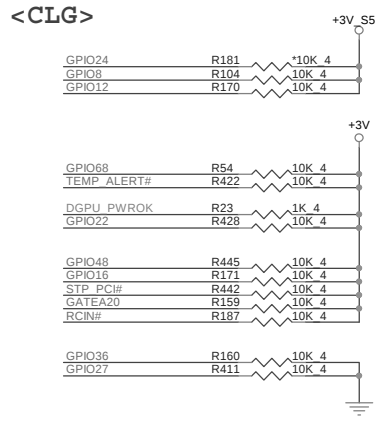
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Panther/Cougar Point 3/6
Date: Monday, March 26, 2012 Sheet 9 of 42

Panther/Cougar Point (GPIO,NCTF,RSVD)

OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO50
DGPU_PWR_EN	GPIO54

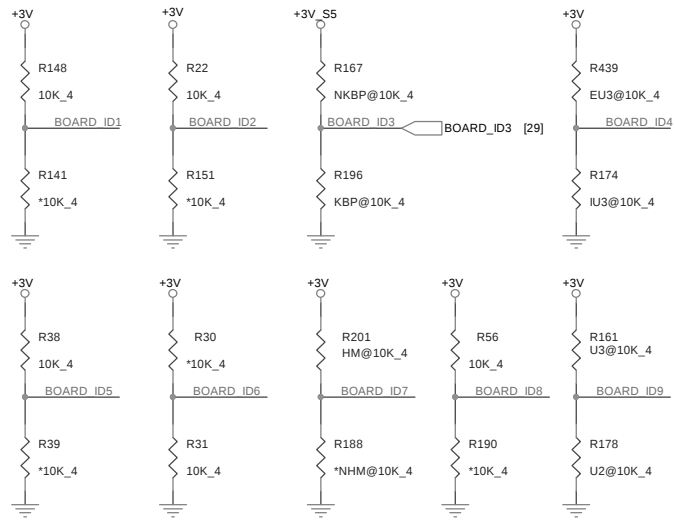


GPIO Pull-up/Pull-down



BOARD ID SETTING <CLG>

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
BU6 SKU KZ1 SKU	H L								
BY2D BY2		H L							
W/O LED KB W/ LED KB			H L						
Ext USB3.0 Int USB3.0				H L					
Reserve					H L				
W/O CCD W/ CCD						H L			
W/ HDMI W/O HDMI							H L		
BY1 BU6 or KZ1								H L	
W/ USB3.0 W/O USB3.0									H L

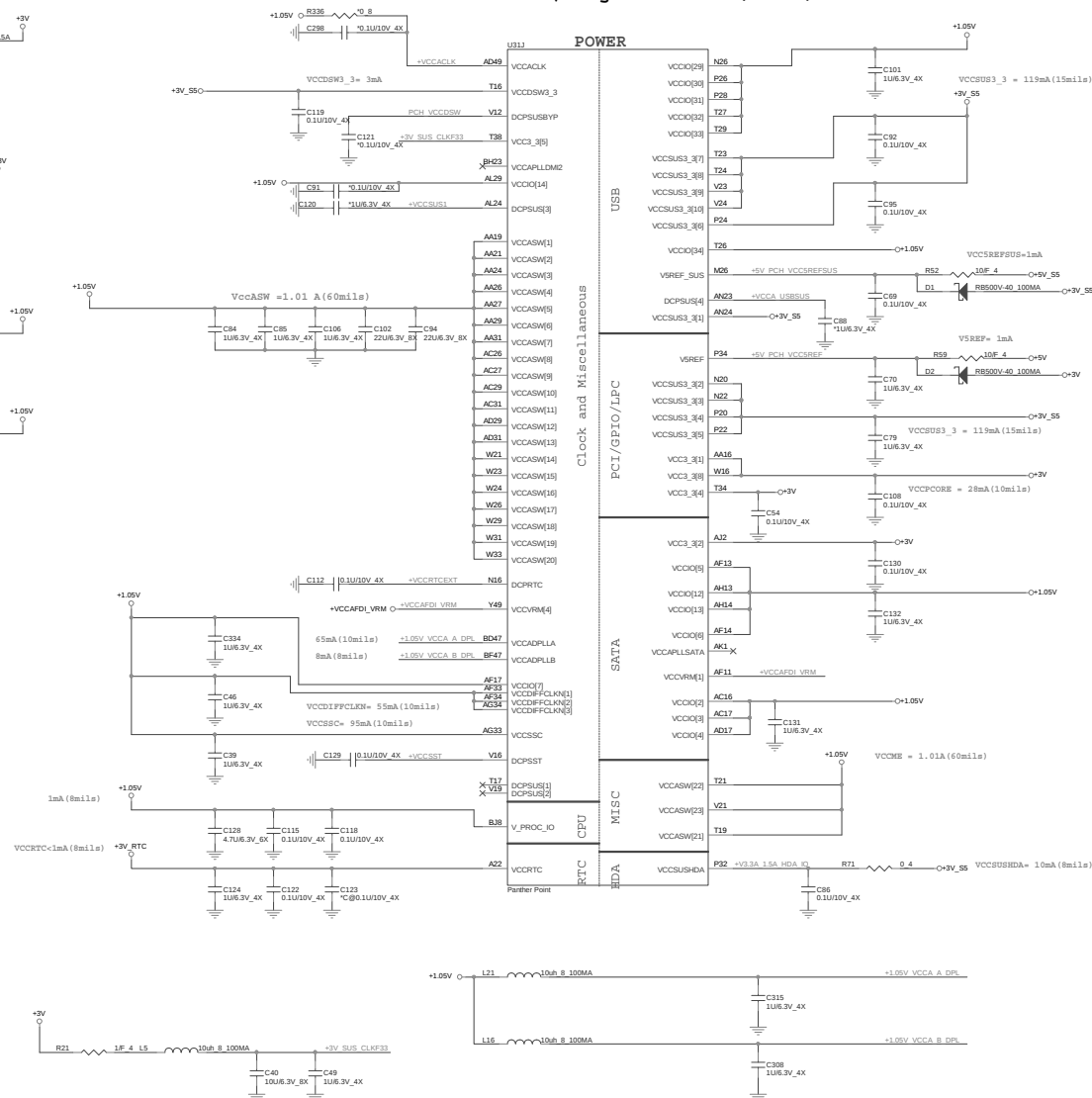


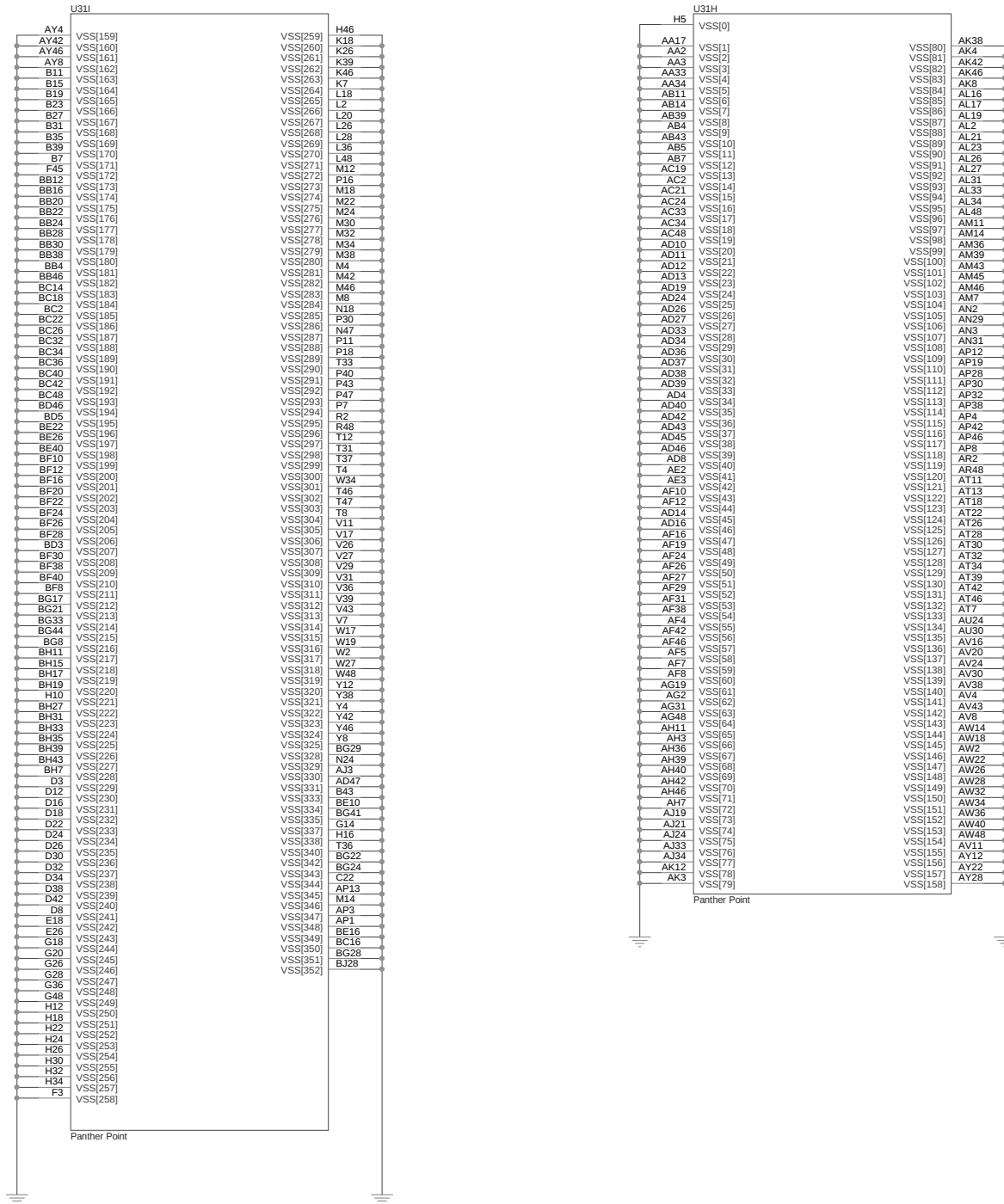


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Size	Document Number	Rev
	Panther/Cougar Point 4/6	3B
Date:	Monday, March 26, 2012	Sheet 10 of 42

Panther/Cougar Point-M (POWER)





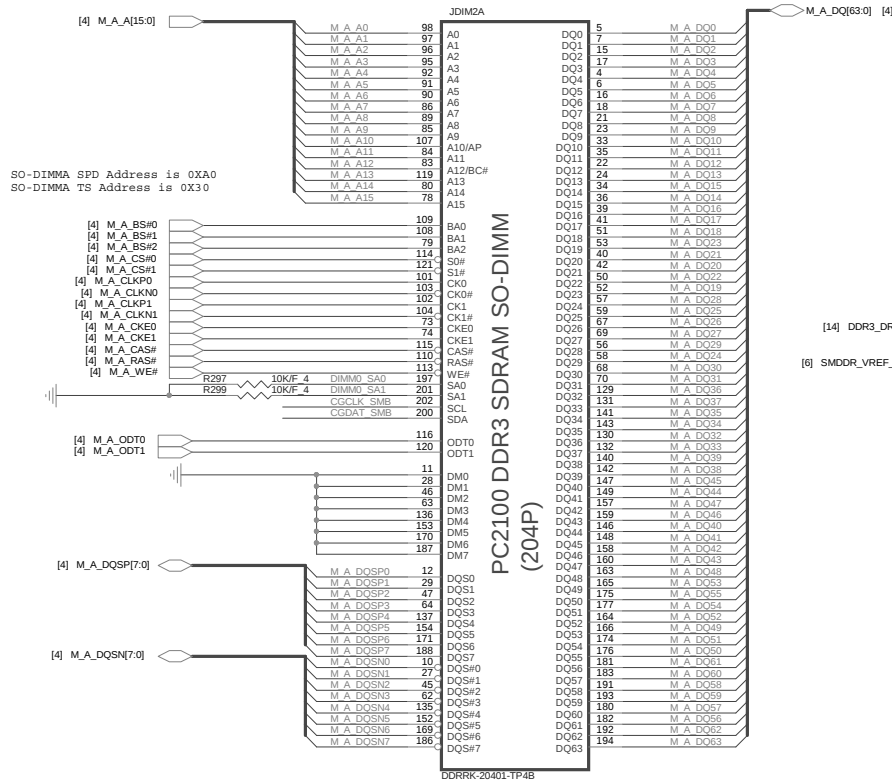
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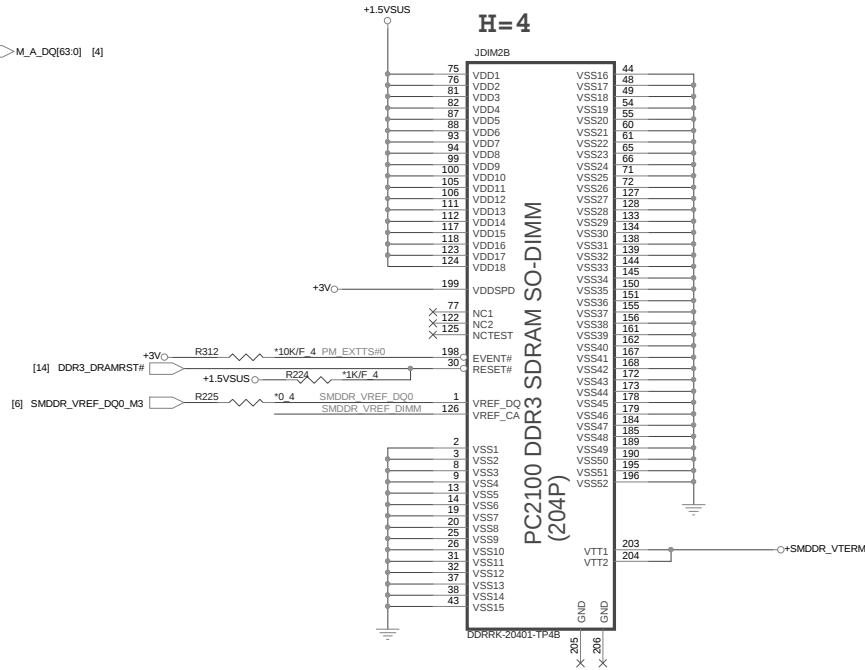
Size	Document Number	Rev
	Panther/Cougar Point 6/6	3B
Date:	Monday, March 26, 2012	Sheet 12 of 42

<DDR>

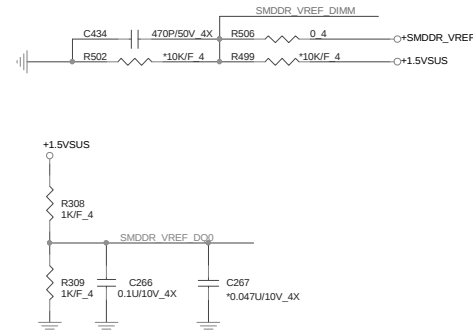
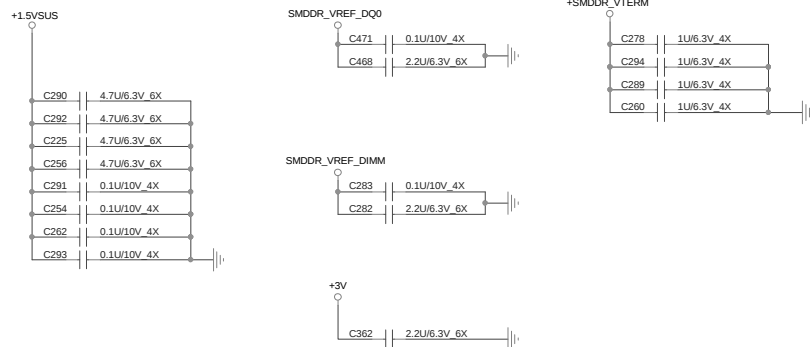
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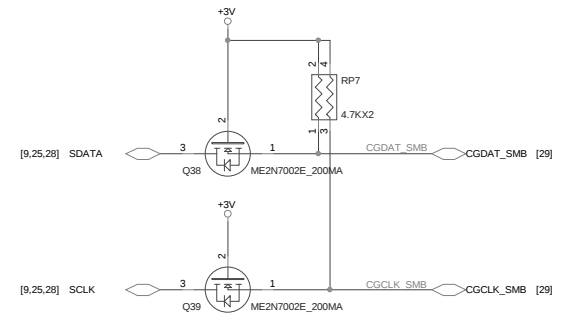
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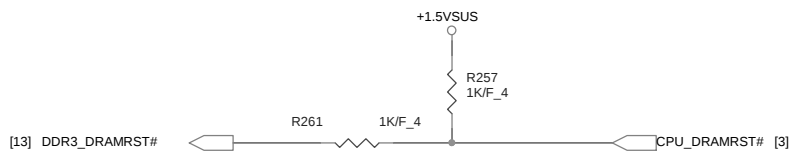
Place these Caps near Memory Down-1



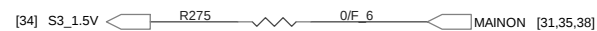
SMBus(DDR3/WLAN/LAN)



S3 power Reduction (SM_DRAMRST#) <S3P> <4>

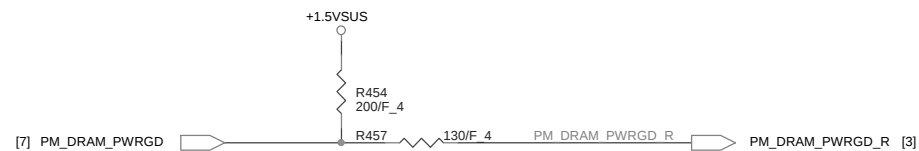


For S3 power Reduction Sequence <S3P> <3>

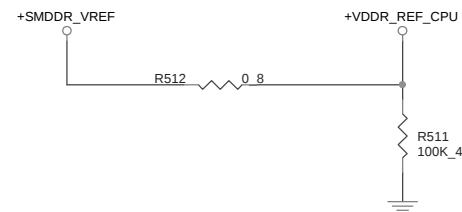


For S3 power Reduction VTT discharge <S3P> <13>

S3 power Reduction (SM_DRAMPWROK) <S3P> <3> 14

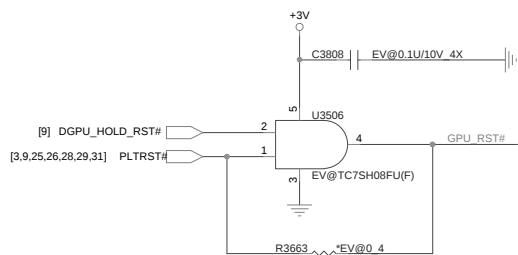
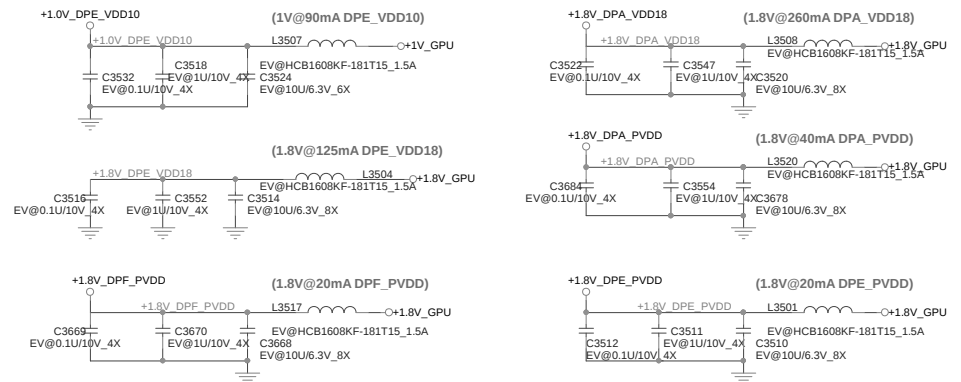
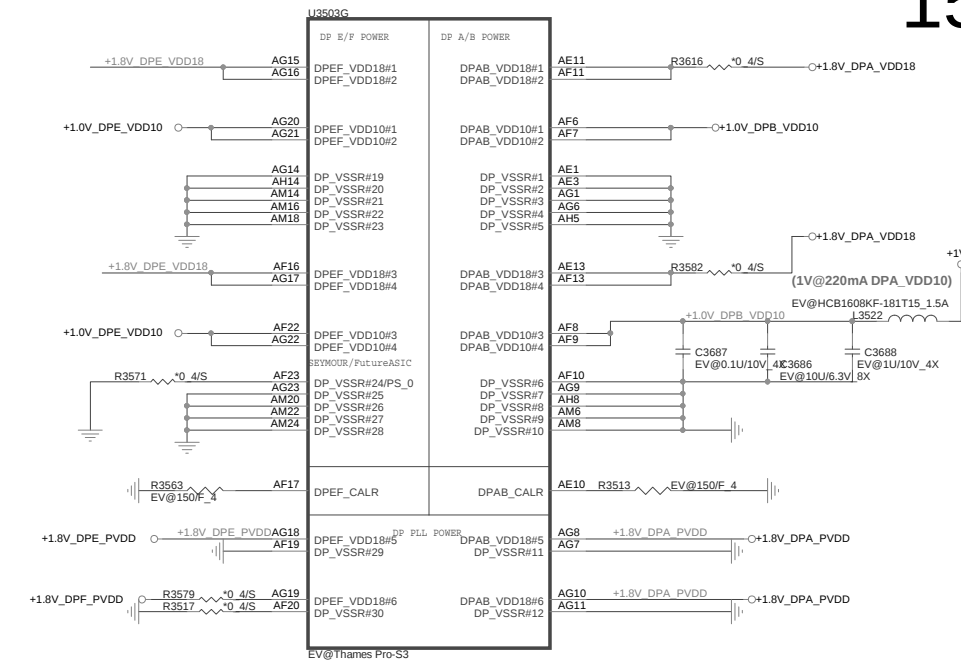
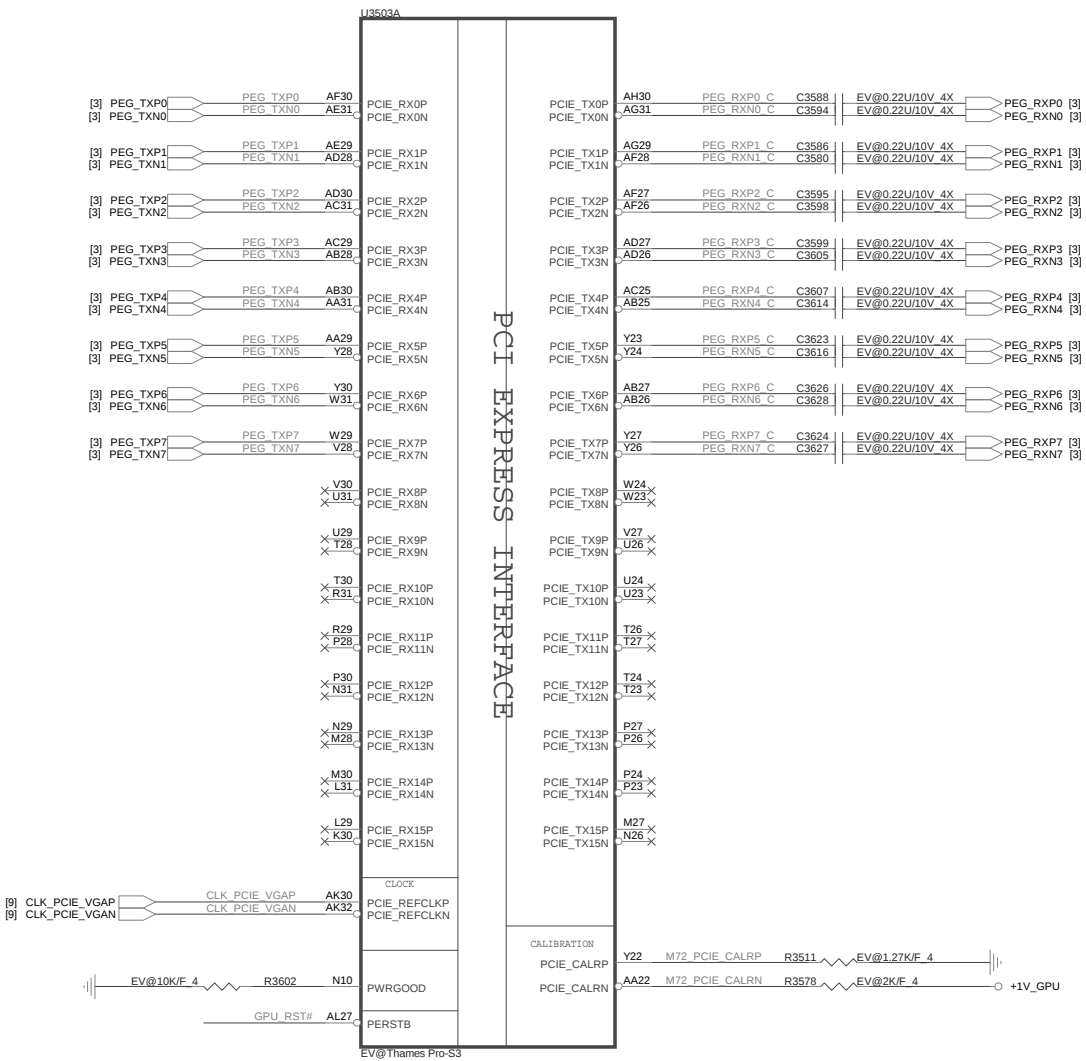


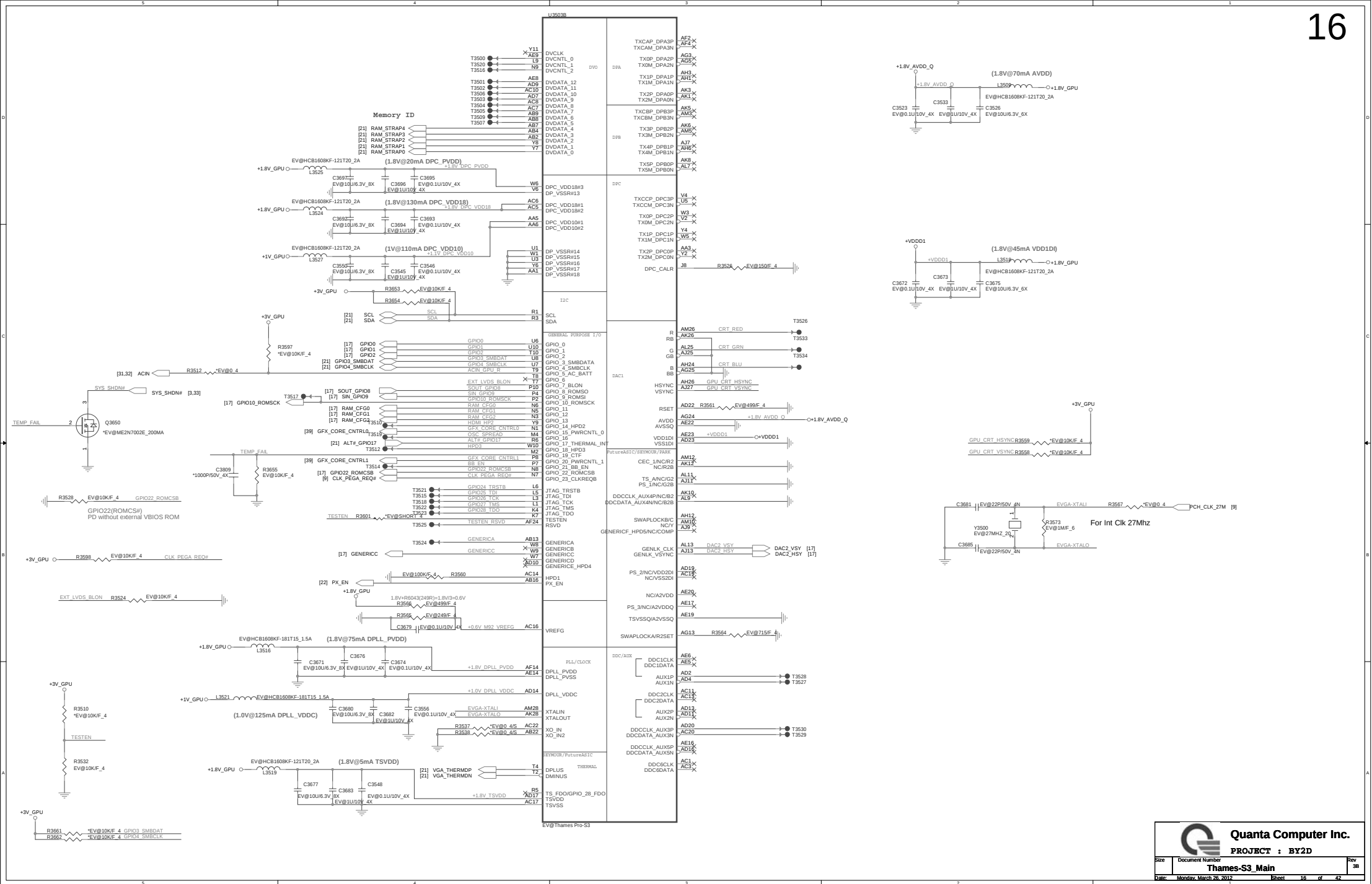
S3 power Reduction (CPU Power) <S3P> <5>

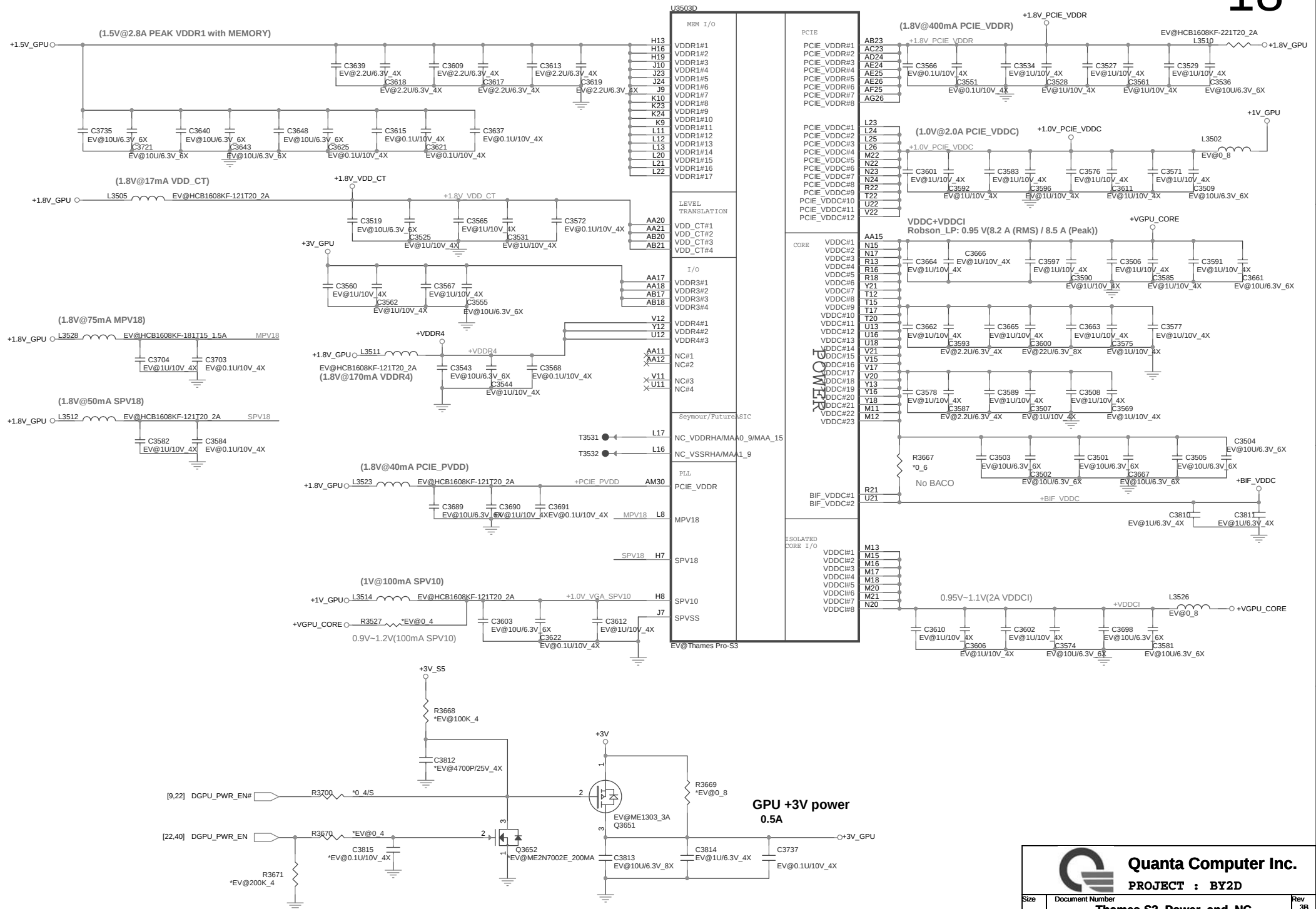


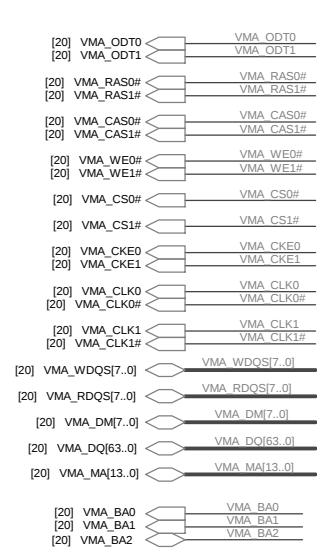
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Size	Document Number	Rev
	S3 power Reduction	3B
Date:	Monday, March 26, 2012	Sheet 14 of 42



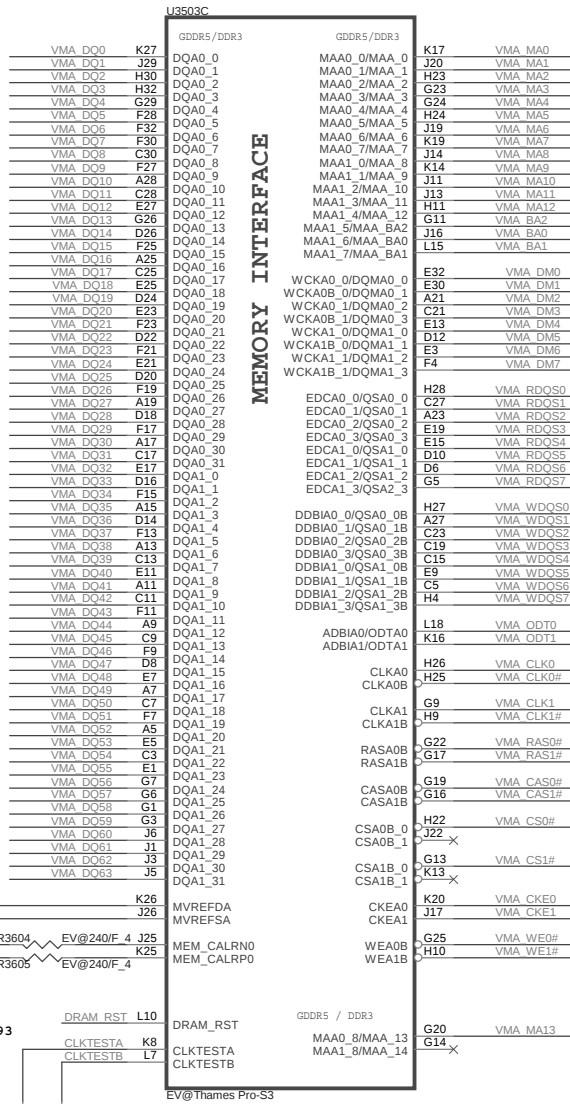
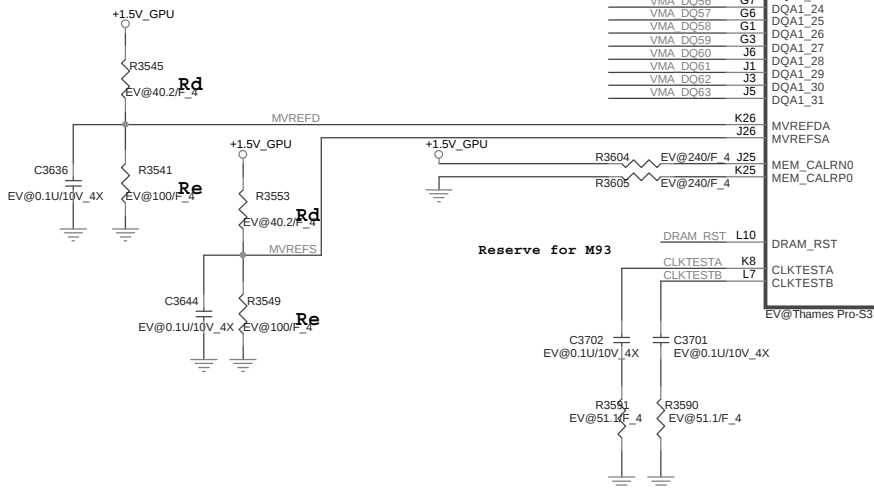






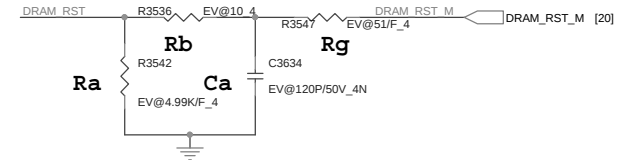
support 1Gbit
VRAM (64M X 16)

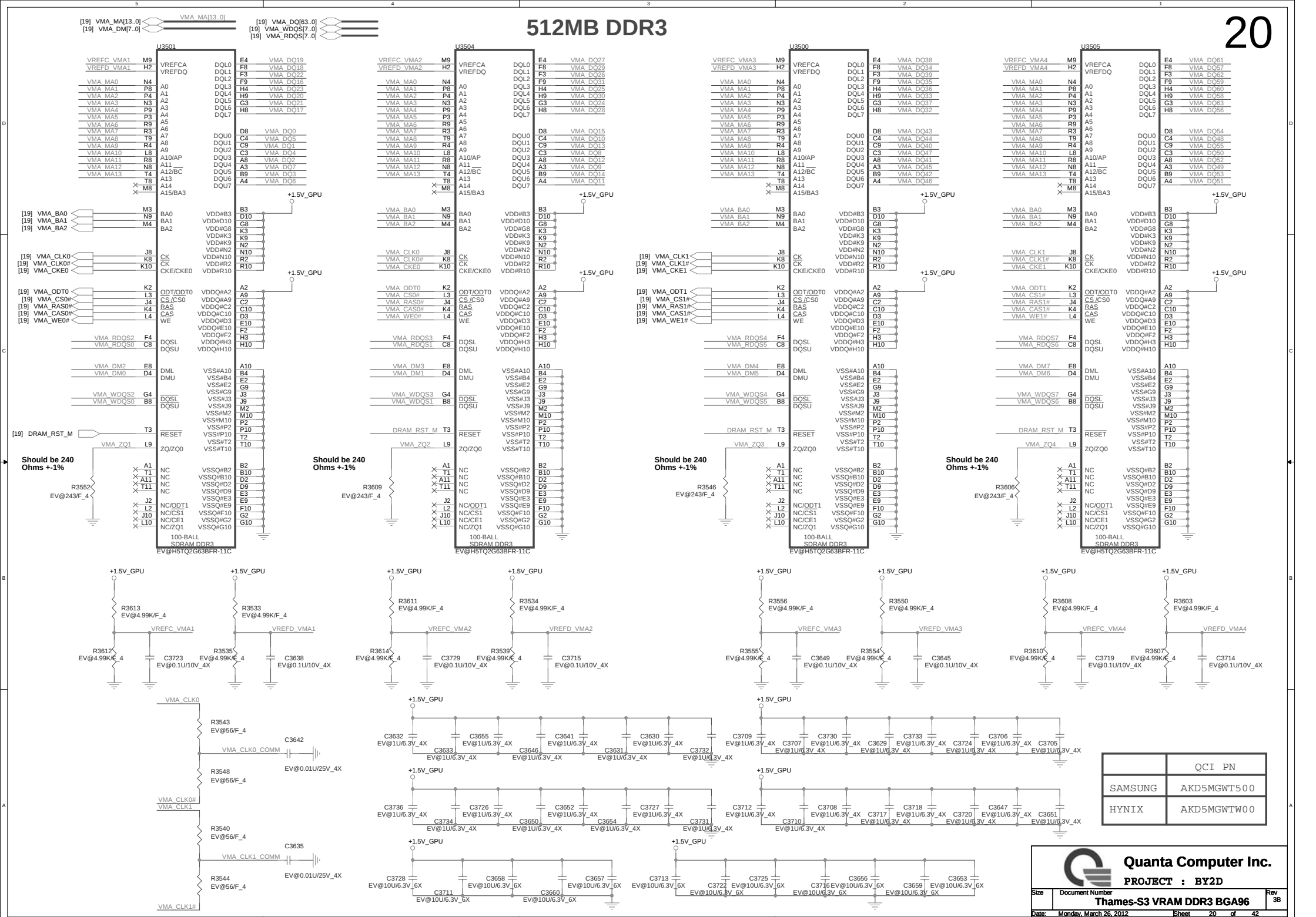
DIVIDER RESISTORS	M93	PARK
MVREF TO 1.8V (Rd)	100R	40.2R
MVREF TO GND (Re)	100R	100R



EV@Thames Pro-S3

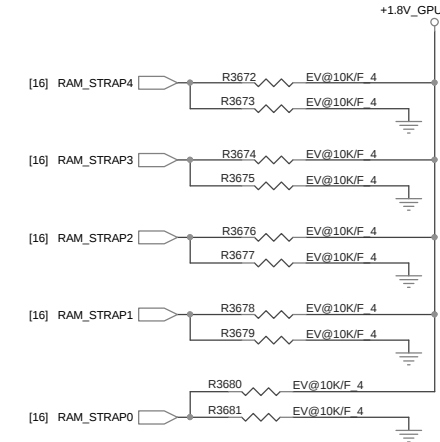
Designator	Robson
Ra	5K
Rb	10R
Ca	120pF
Rg	51R



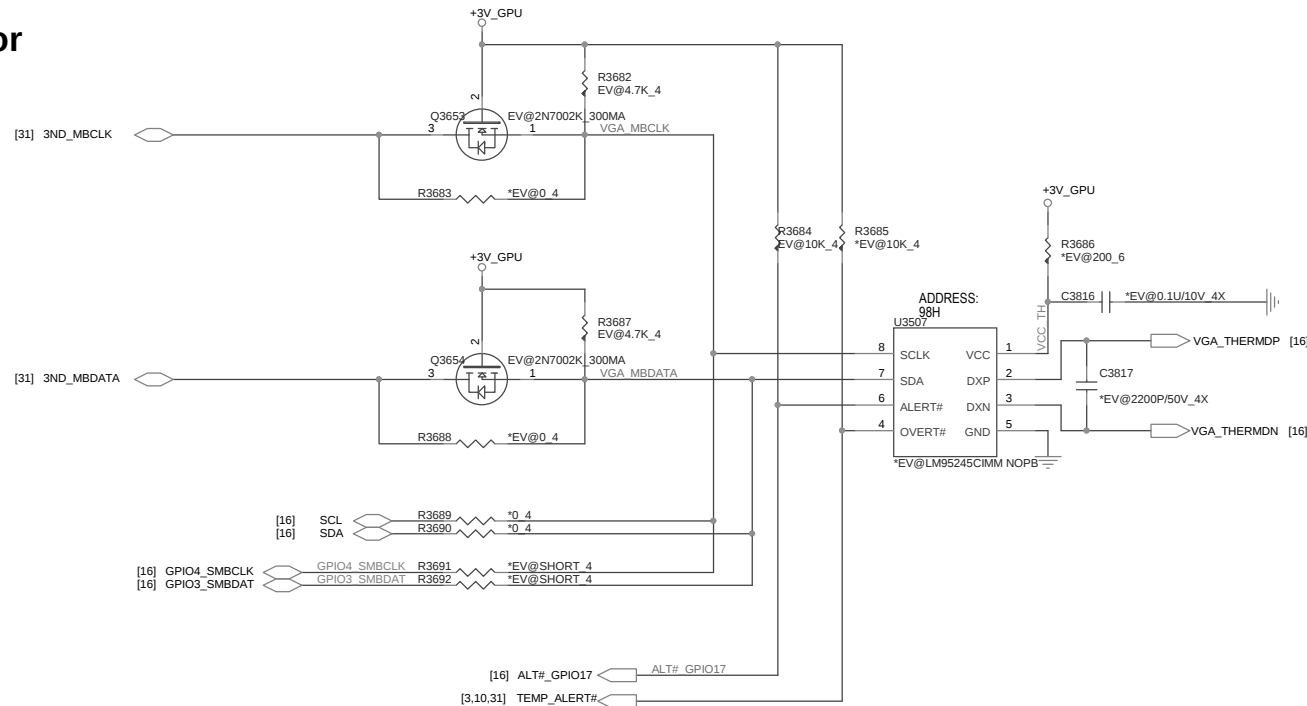


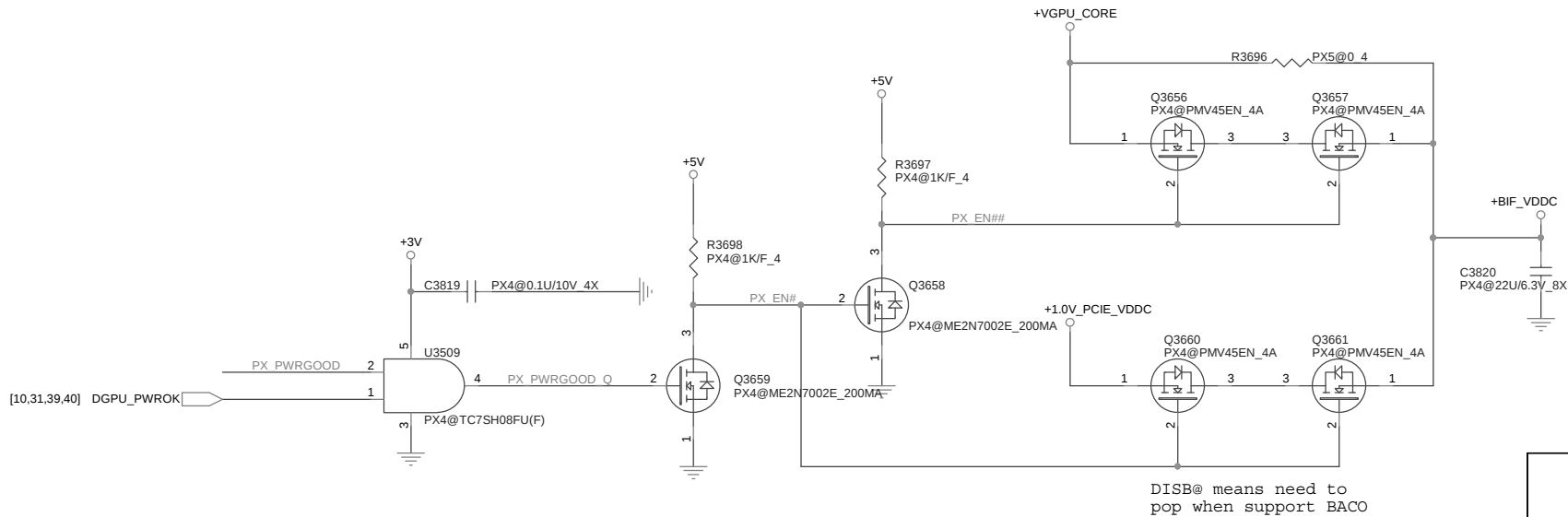
VRAM Memory TYPE

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP4 DVPDATA_4	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
AMD	23EY2387MC11	AKD5EZWT700 *4 (64M*16-1Gb)	512MB	0	0	0	1	0
	23EY4187MA11	AKD5DZWT700 *4 (128M*16-2Gb)	1GB	0	1	0	1	0
Samsung	K4W1G1646G-BC11	AKD5EGGT500 *4 (64M*16-1Gb)	512MB	0	0	0	0	1
	K4W2G1646C-HC11	AKD5MGWT500 *4 (128M*16-2Gb)	1GB	0	1	0	0	1
Hynix	H5TQ1G63DFR-11C	AKD5LZWTW02 *4 (64M*16-1Gb)	512MB	0	0	0	0	0
	H5TQ2G63BFR-11C	AKD5MGWTW00*4 (128M*16-2Gb)	1GB	0	1	0	0	0

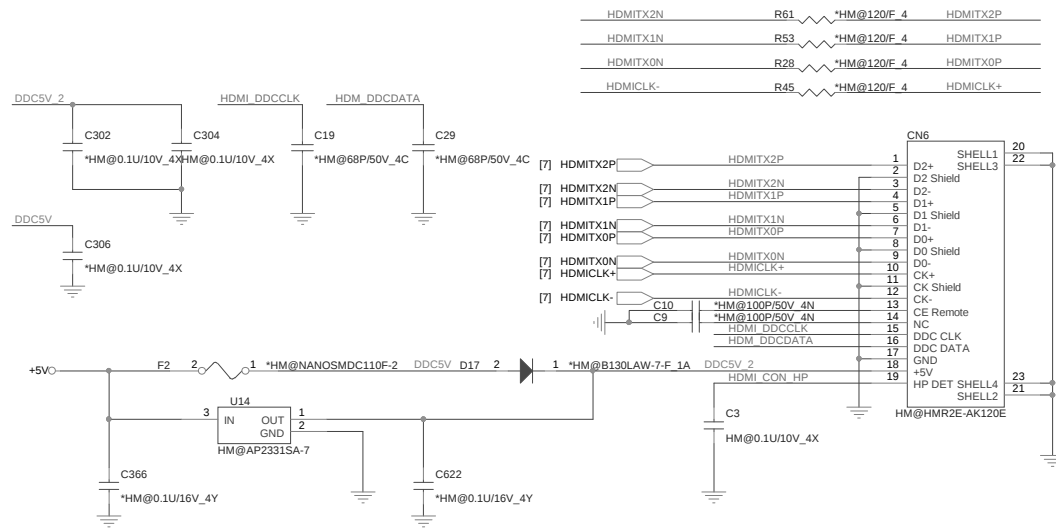


Thermal Sensor

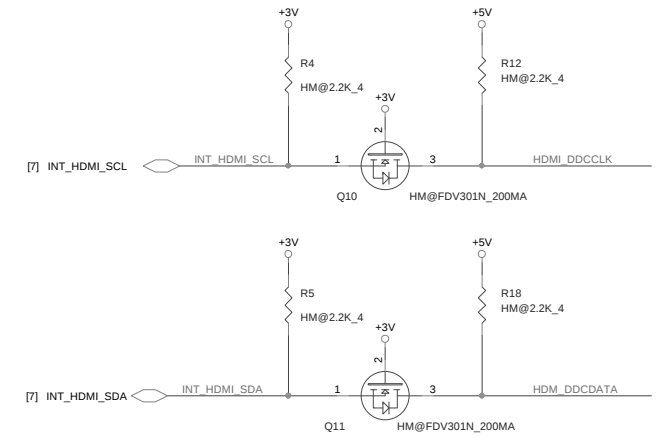




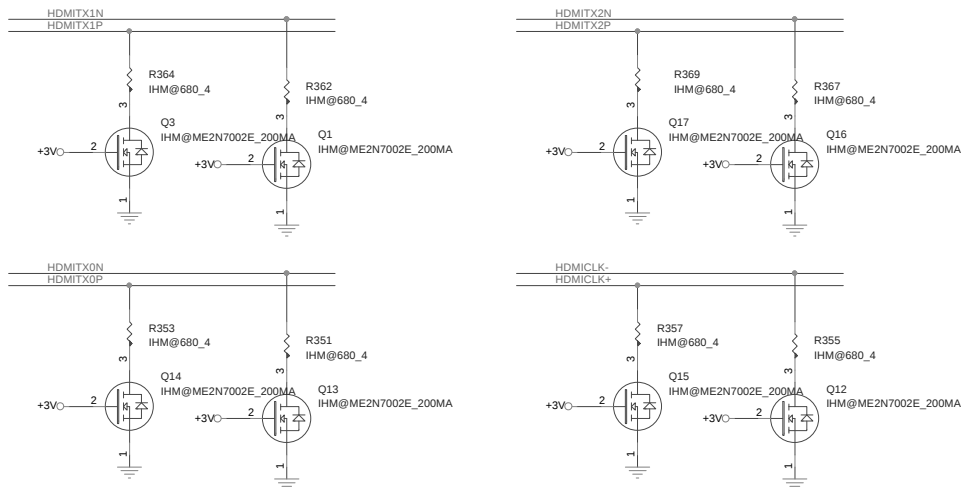
HDMI Conn <HDM>



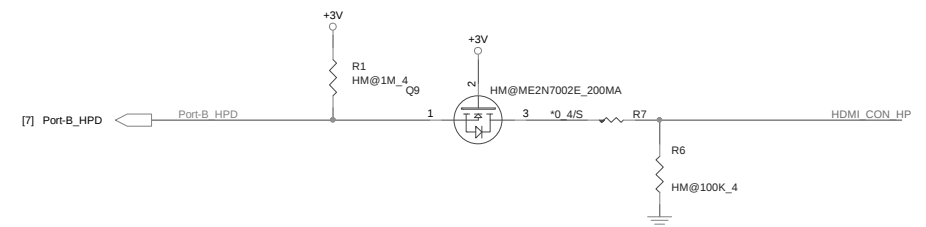
HDMI-SMBus <HDM>

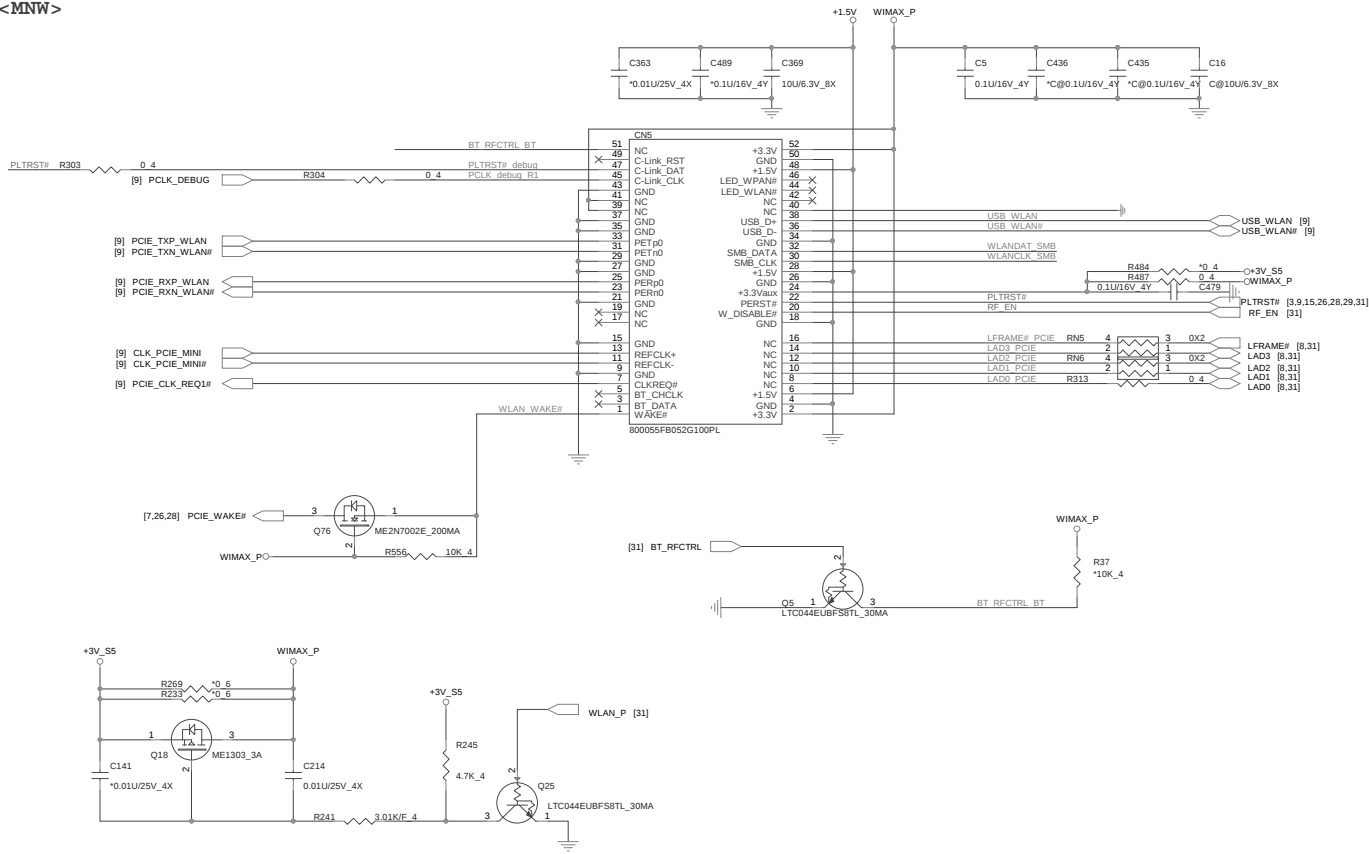


HDMI-passive level shift <HDM>

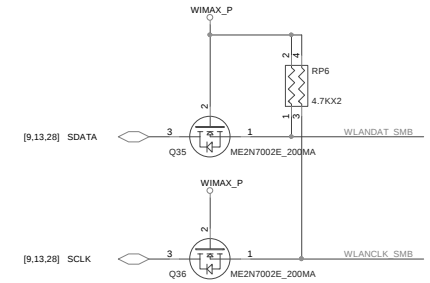


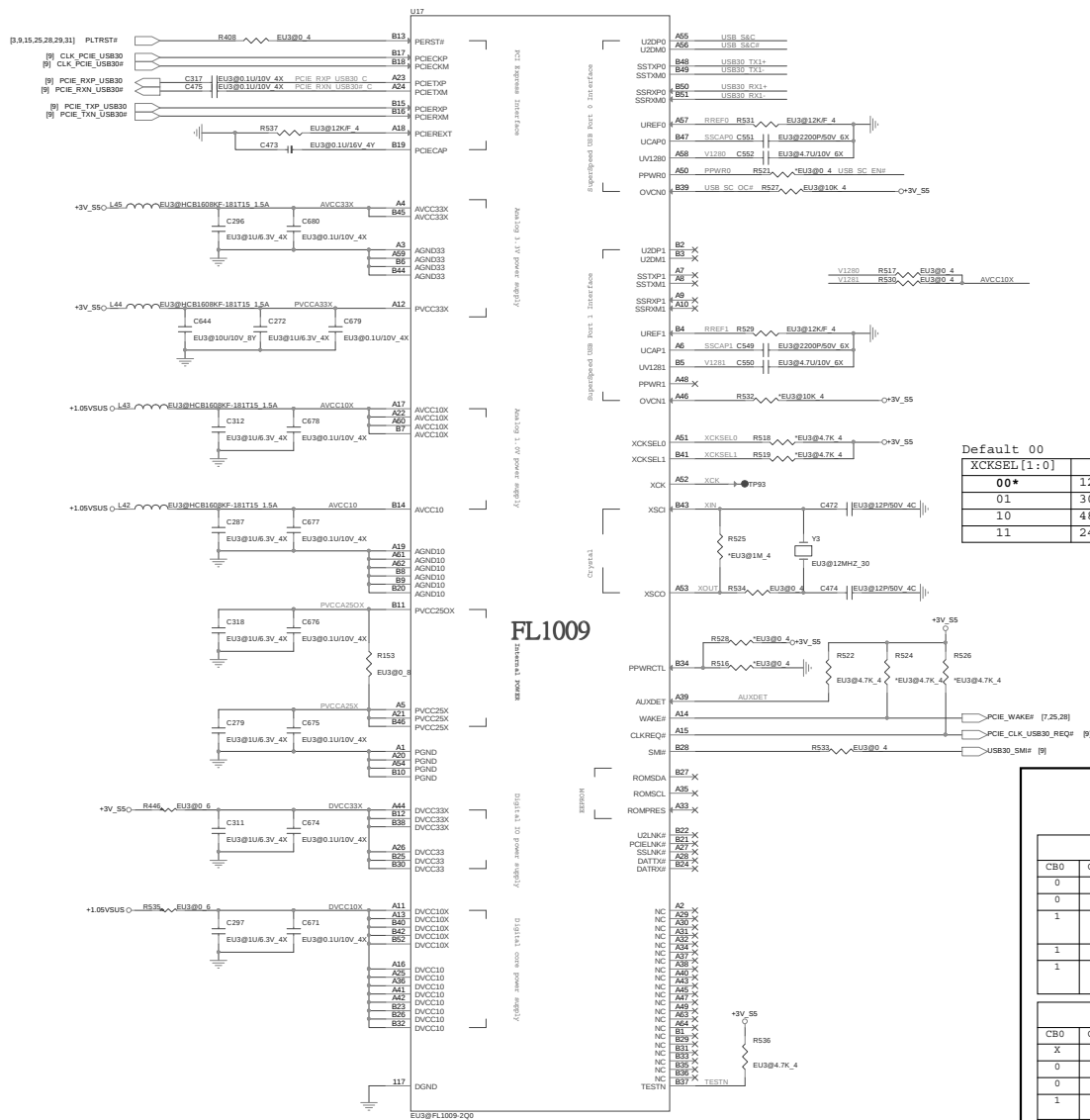
HDMI-HPD <HDM>



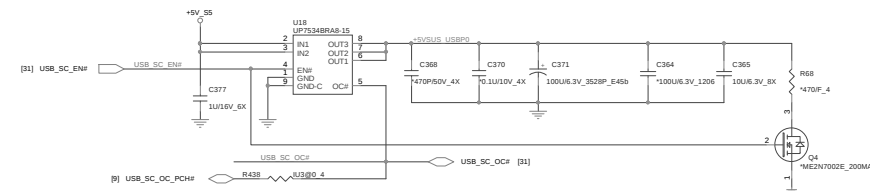


SMBus(DDR3/WLAN/3G)

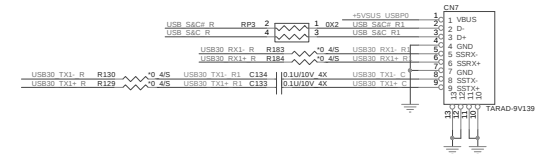




USB 3.0 Power switch <U2B> <USB> <U3B>

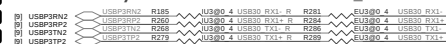


<EMI> <U3B> <USB>

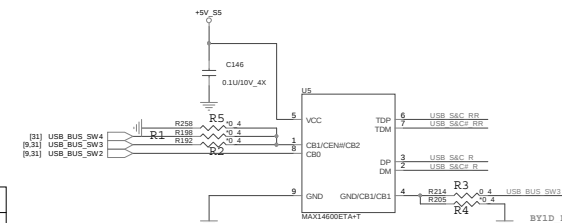


USB 3.0 CONN

USB 3.0 Colay for Chief River and Huron_River

USB 2.0 Colay <U3B>
<U2B>

USB w S&C MAXIM solution <SLC>

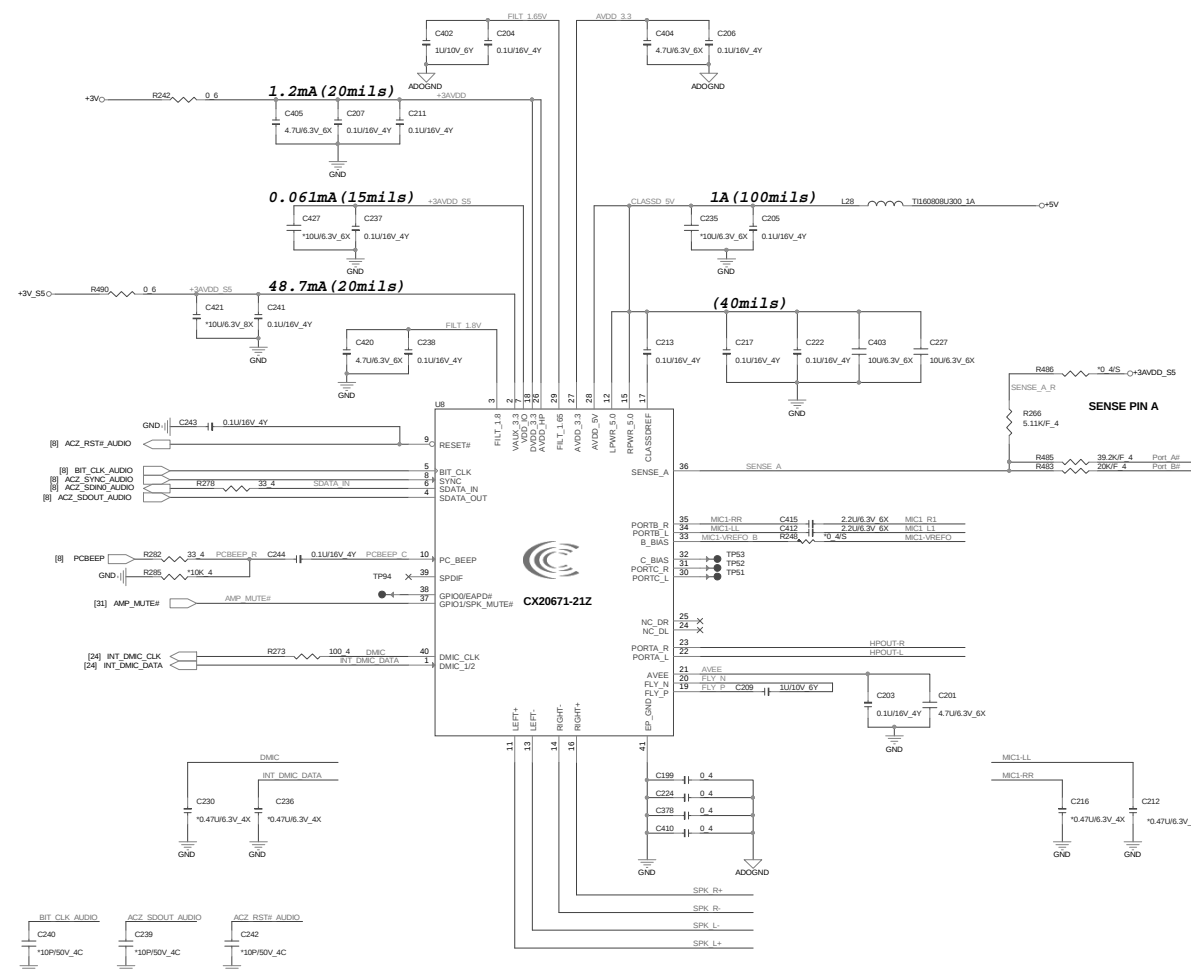


14566/14600/14617

	R1	R2	R3	R4	R5
14566		V		V	
14600			V		
14617(with CB2)	V		V		
14617(no CB2)			V		V

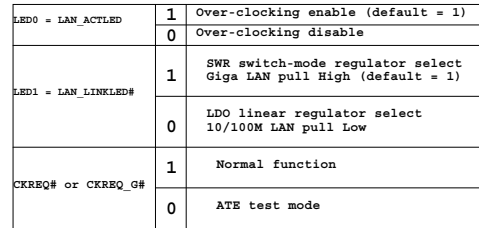
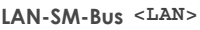
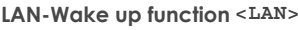
14566/14600		
CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-through(USB) mode: Connect DP/DW to TDP/TDM for 14566
1	0	Pass-through(USB) mode for 14600
1	1	pass-through(USB) with CDP Emulation for 14600

14617			
CB0	CB1	CB2	Status
X	X	1	Force Apple 2A Charger Mode
0	0	0	Autodetection charger mode
0	1	0	Force-Dedicated Charger Mode
1	0	0	USB Pass-Through Mode (USB) Connect DP/DM to TDP/TDM
1	1	0	USB Pass-Through Mode with CDP Emulation.Auto connect DP/DM to TDP/TDM depending on CDP status

[illegible][illegible]

The schematic diagram illustrates the power supply and signal connections for the P8000. The top section shows a power supply circuit with a 5V regulator (R298) and decoupling capacitors (C250, C253, C252, C249) connected to the INSPKR-N, INSPKR-L, INSPKR-R, and INSPKR-L pins of the CN11 connector. The bottom section shows four signal channels (D12, D13, D14, D11) connected to the INSPKR-N pin of the CN11 connector, each with a 0603 220K-V05 resistor.

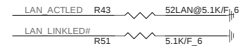
AR8151/AR8152

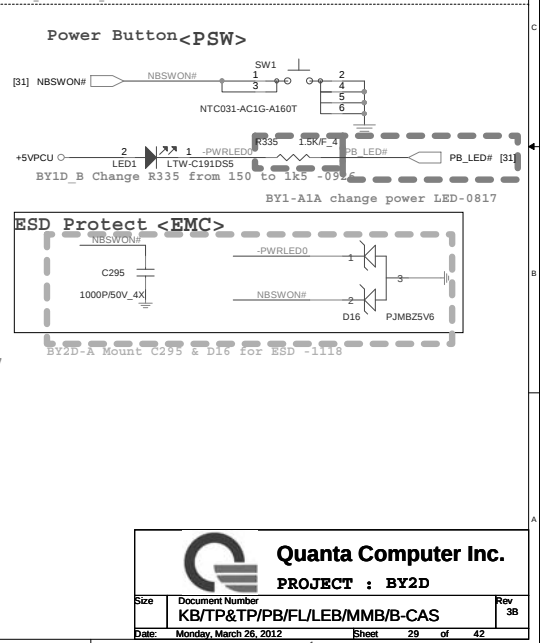
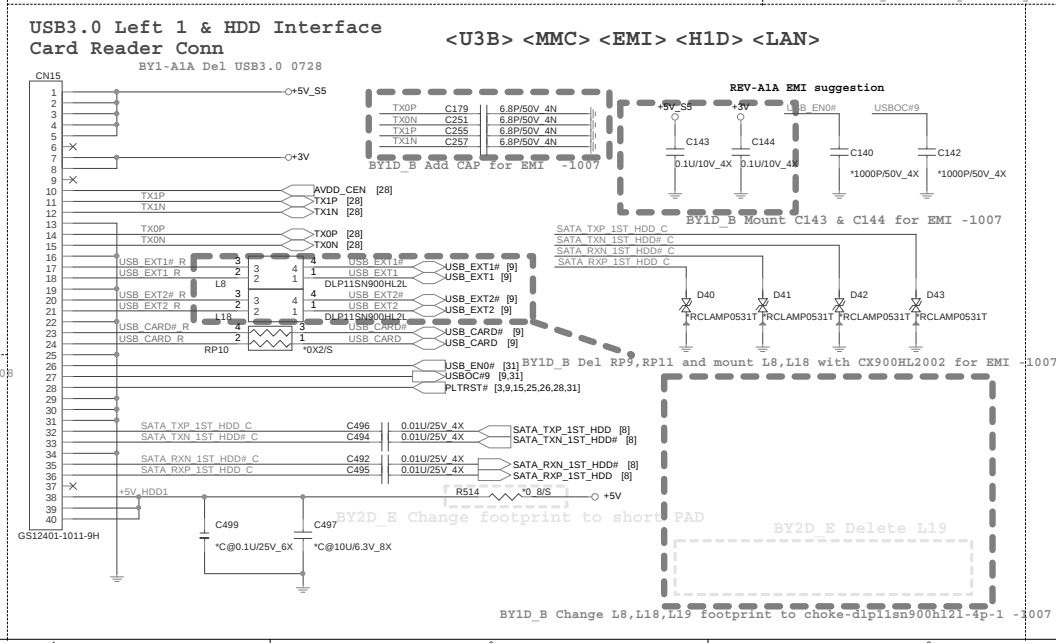
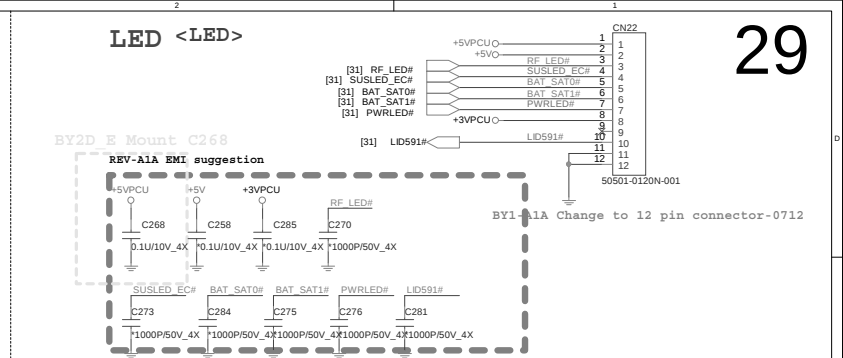
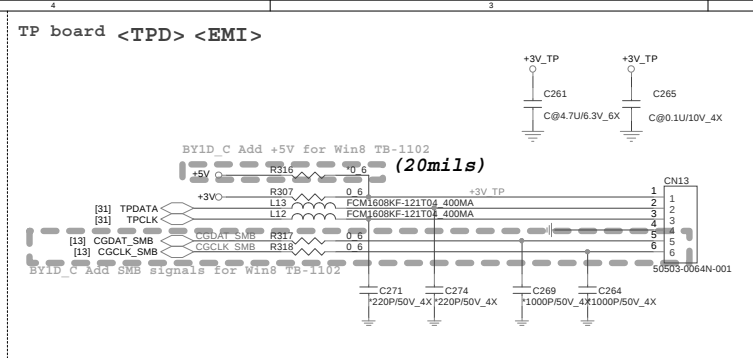
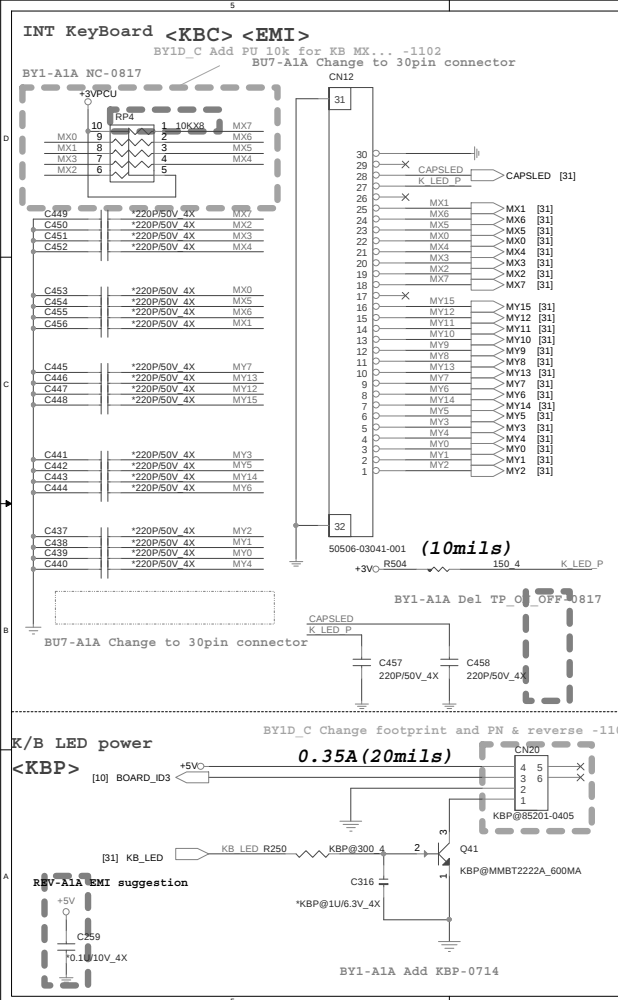


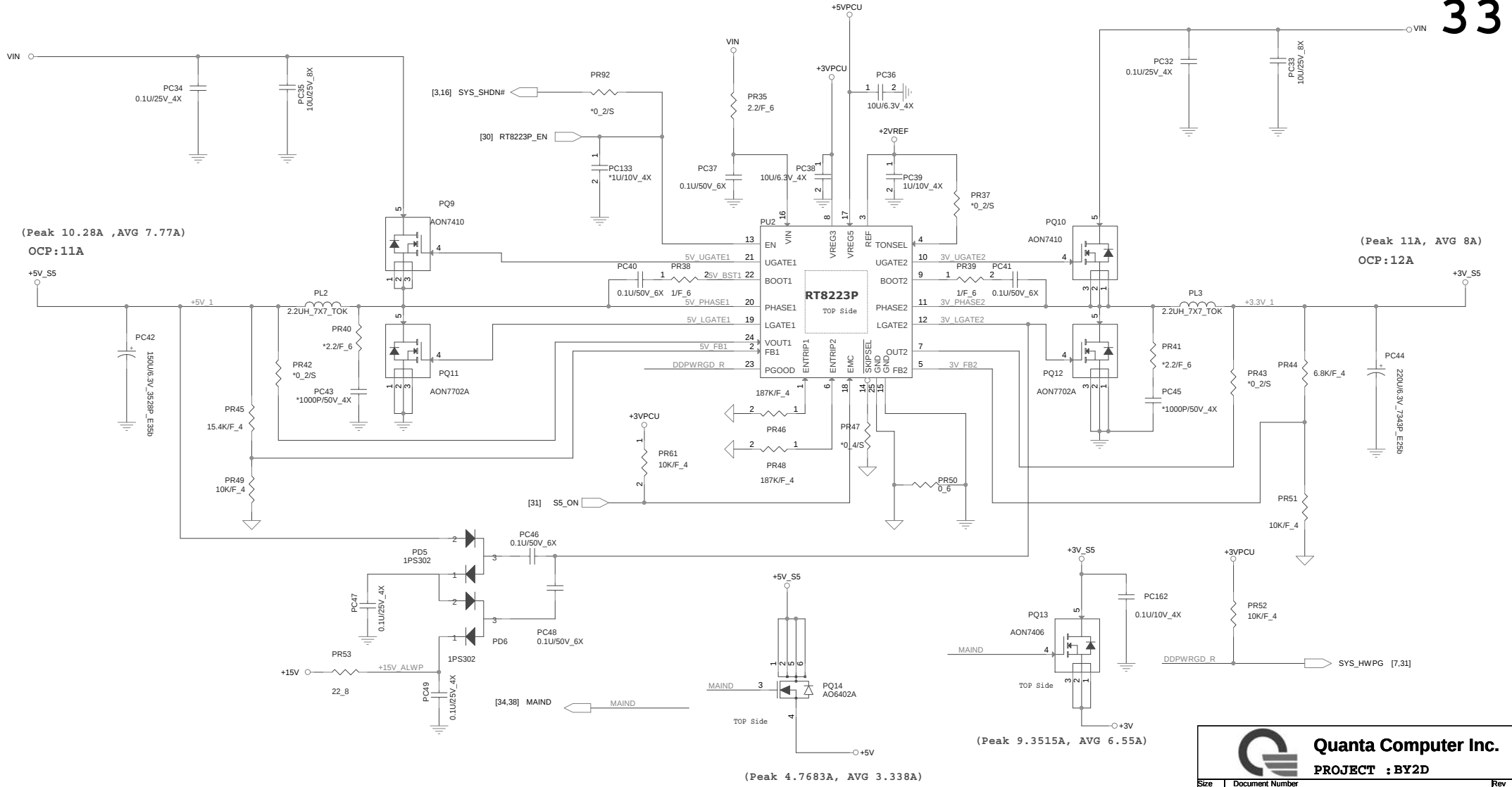
<LAN>



RJ45<LAN>





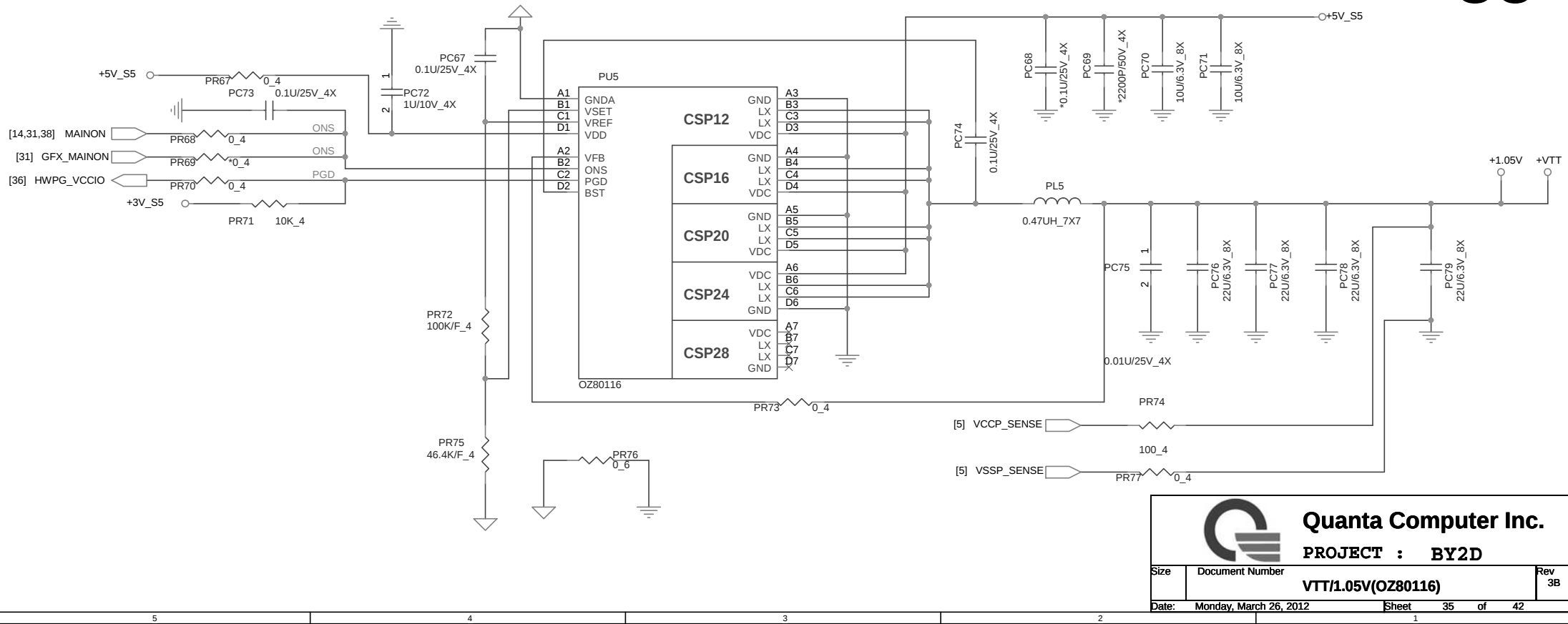


PROJECT : BY2D

DDR 1.5V(TPS51216)/1.05VSUS

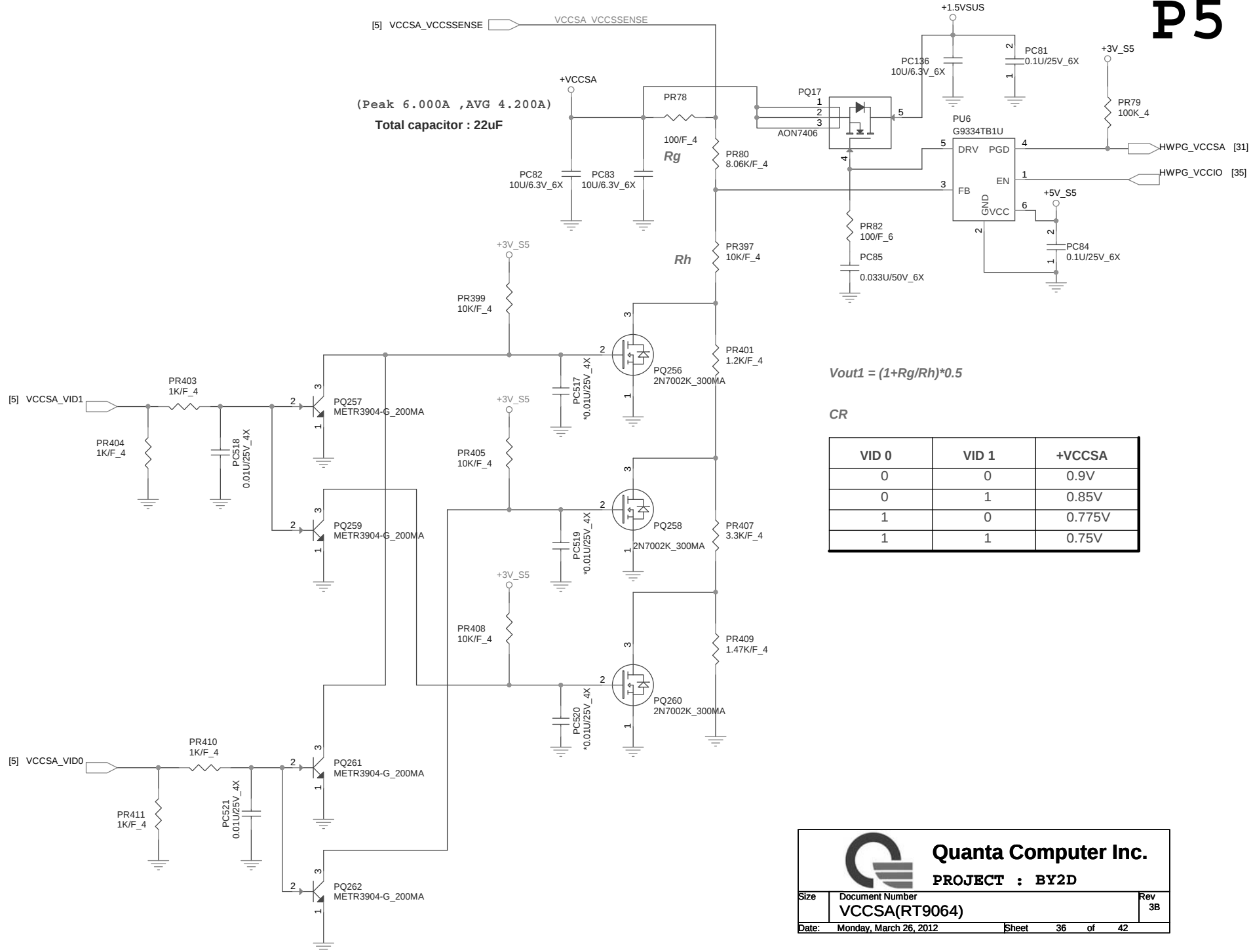
Rev
3B

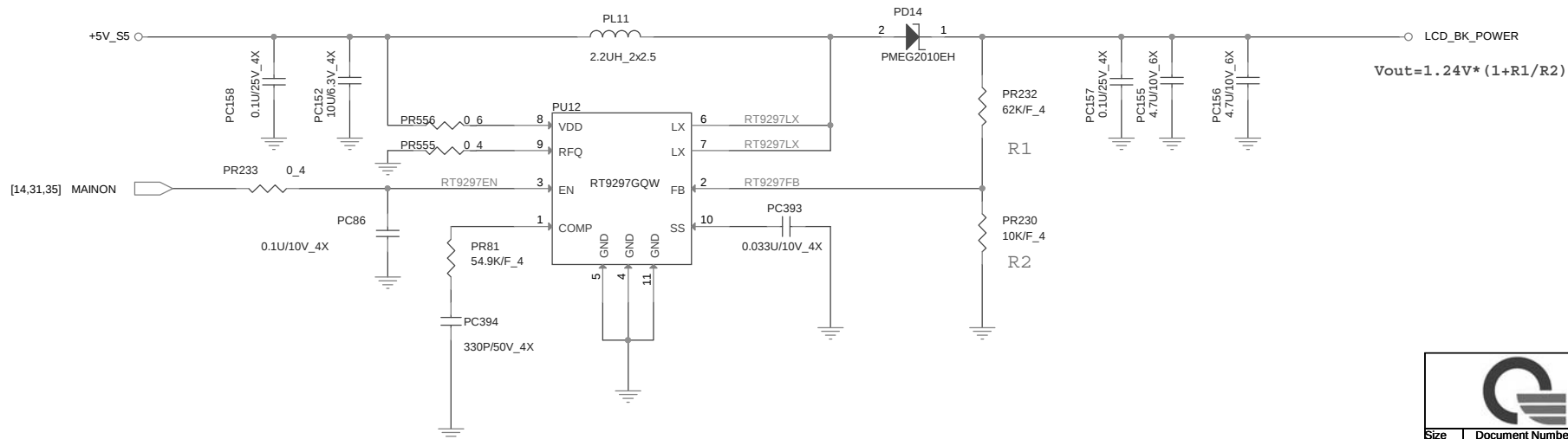
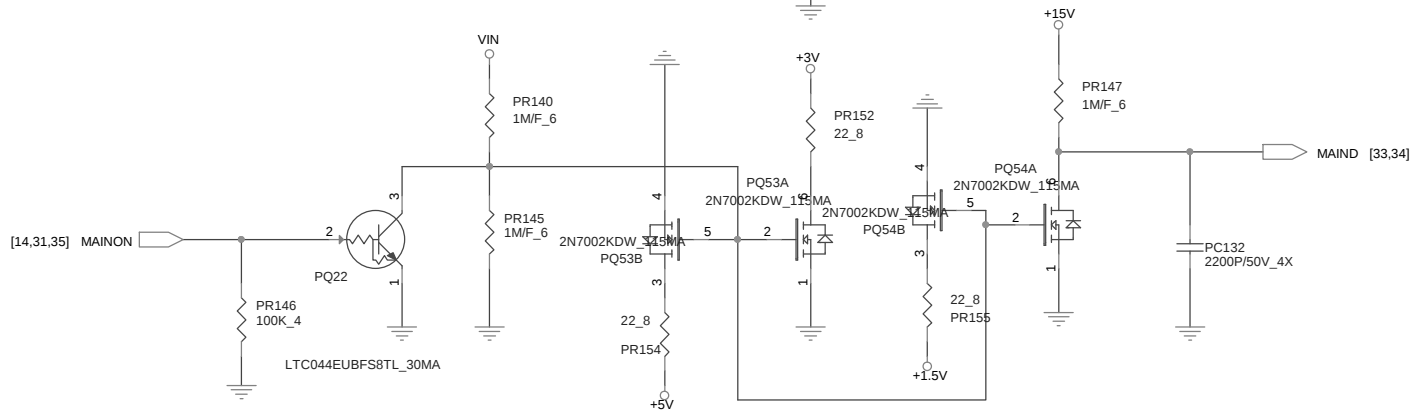
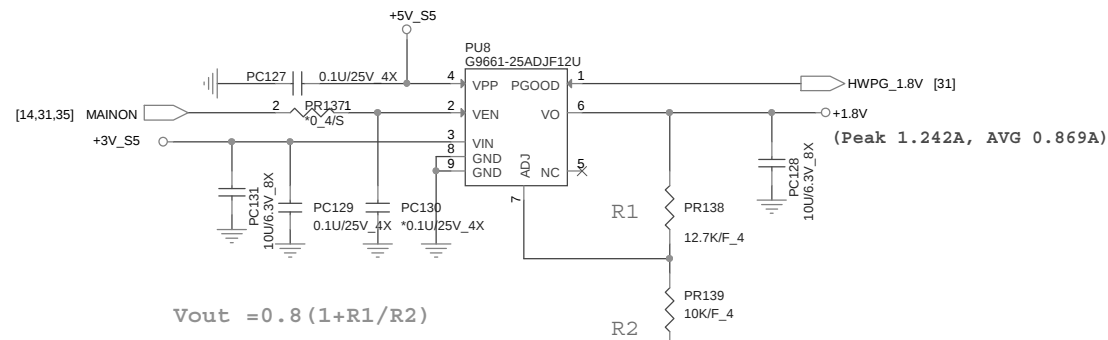
Size	Document Number	Rev
	DDR 1.5V(TPS51216))/1.05VSUS	3B
Date:	Monday, March 26, 2012	Sheet 34 of 42

**Quanta Computer Inc.****PROJECT : BY2D**

Size	Document Number	Rev
	VTT/1.05V(OZ80116)	3B
Date:	Monday, March 26, 2012	Sheet 35 of 42

P5

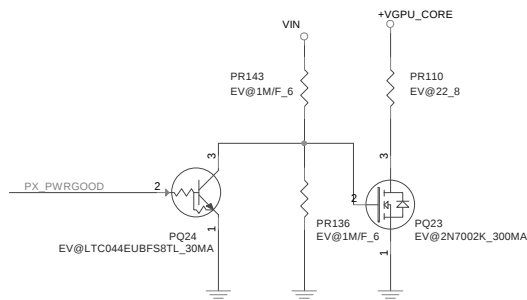
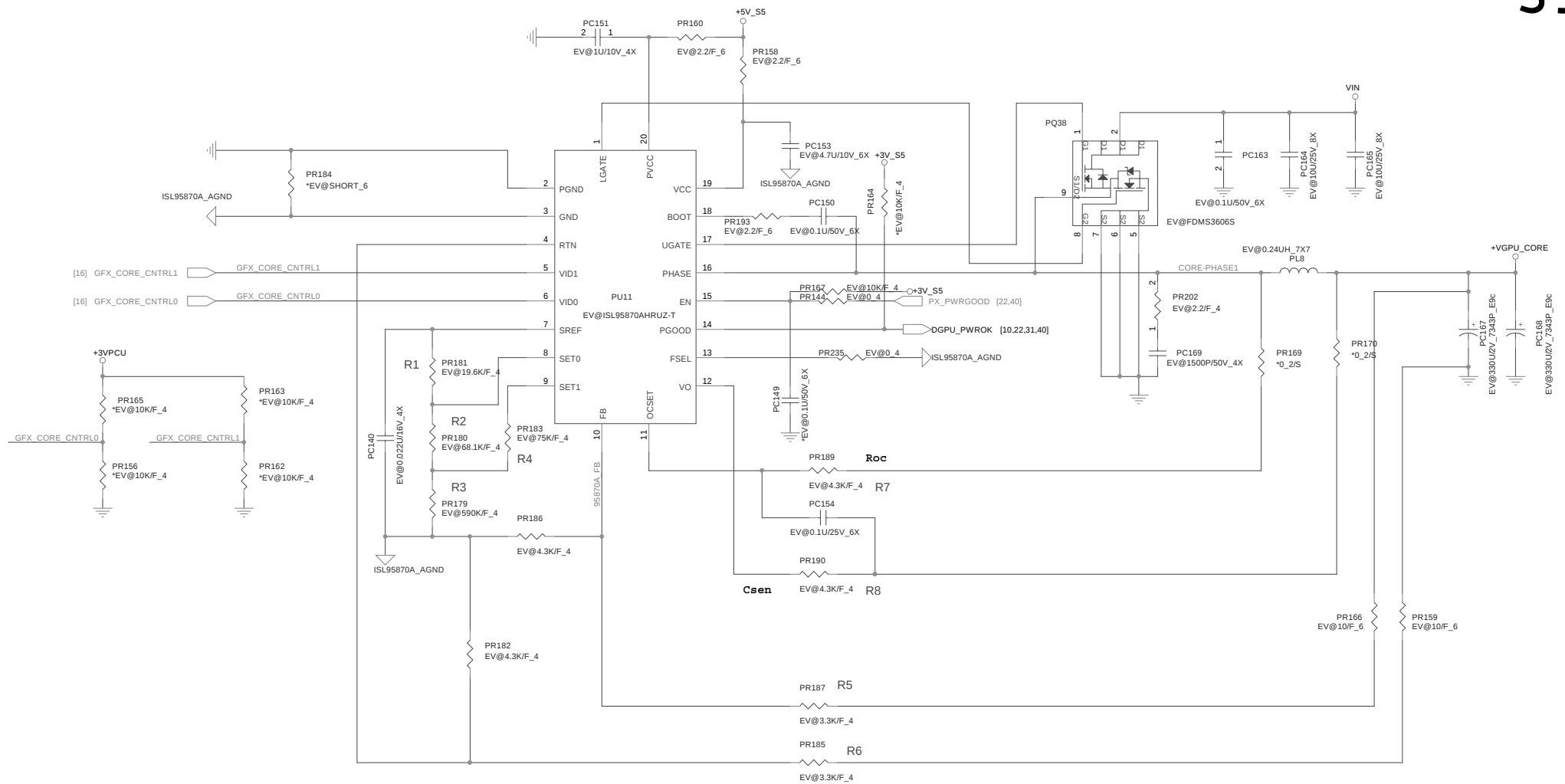




Quanta Computer Inc.

PROJECT : BY2D

Size	Document Number	Rev
	Discharge	3B
Date:	Monday, March 26, 2012	Sheet 38 of 42



R1	19.6K/F_4
R2	68.1K/F_4
R3	590K/F_4
R4	75K/F_4
R5/R6	3.3K/F_4
R7/R8	4.3K/F_4

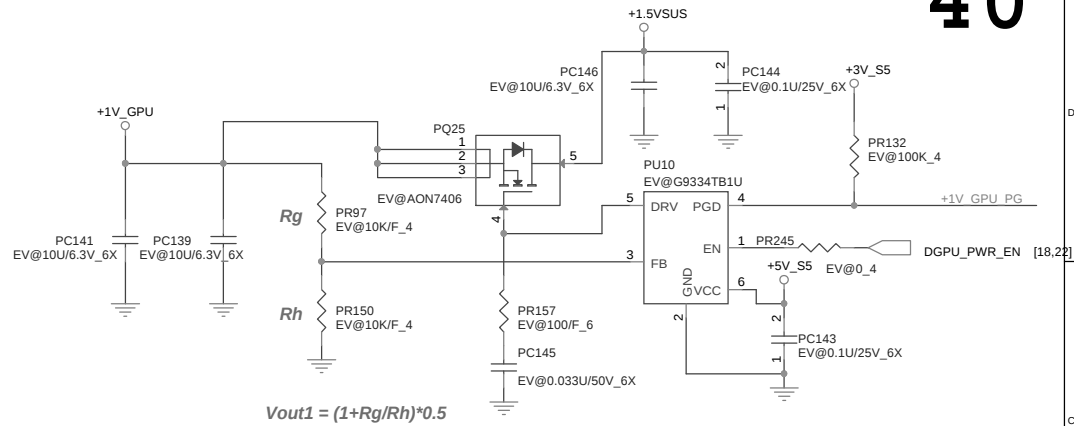
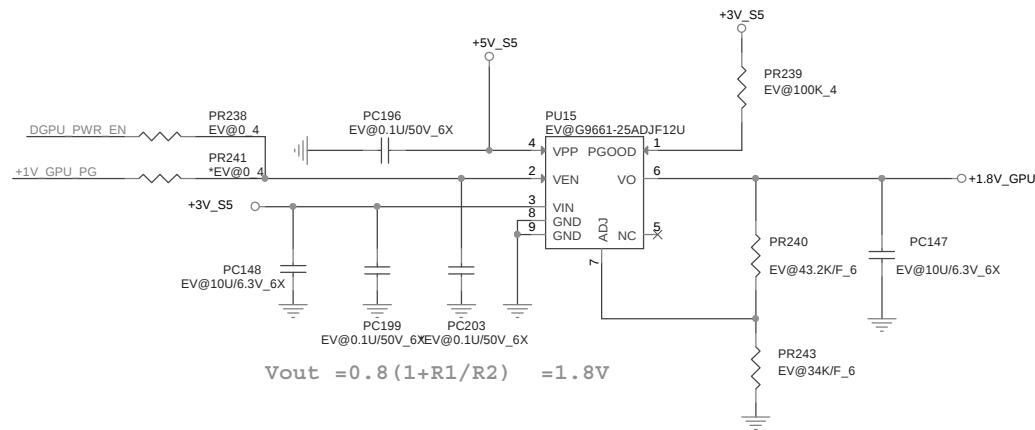
Thames Pro S3

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.875V
1	0	0.9V
0	1	1V
0	0	1V

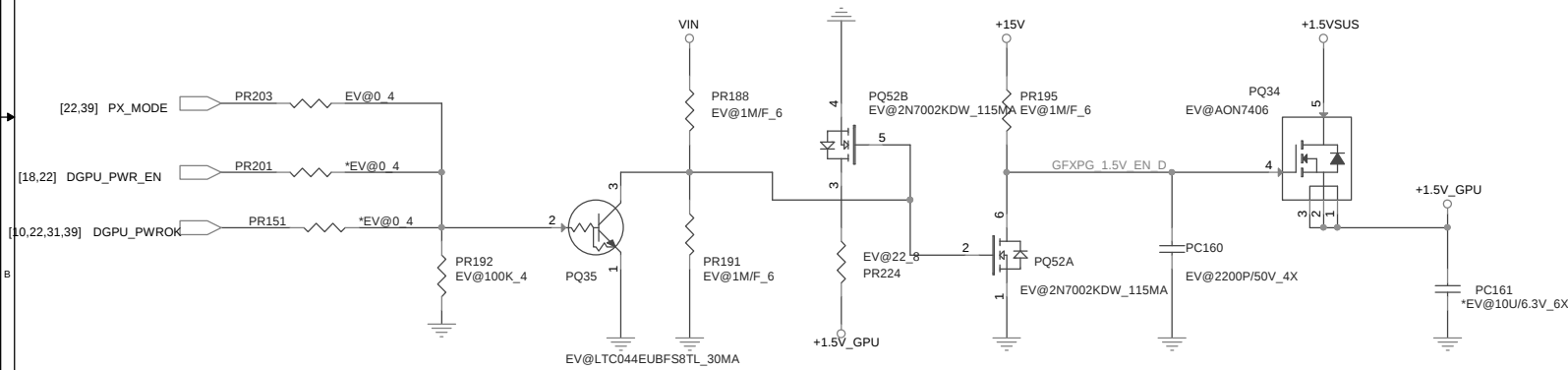


Quanta Computer Inc.
PROJECT : BY2D

Size	Document Number	Rev
	GPU Core (ISL62881C)	38
Date	Monday, March 26, 2012	Sheet 39 of 42



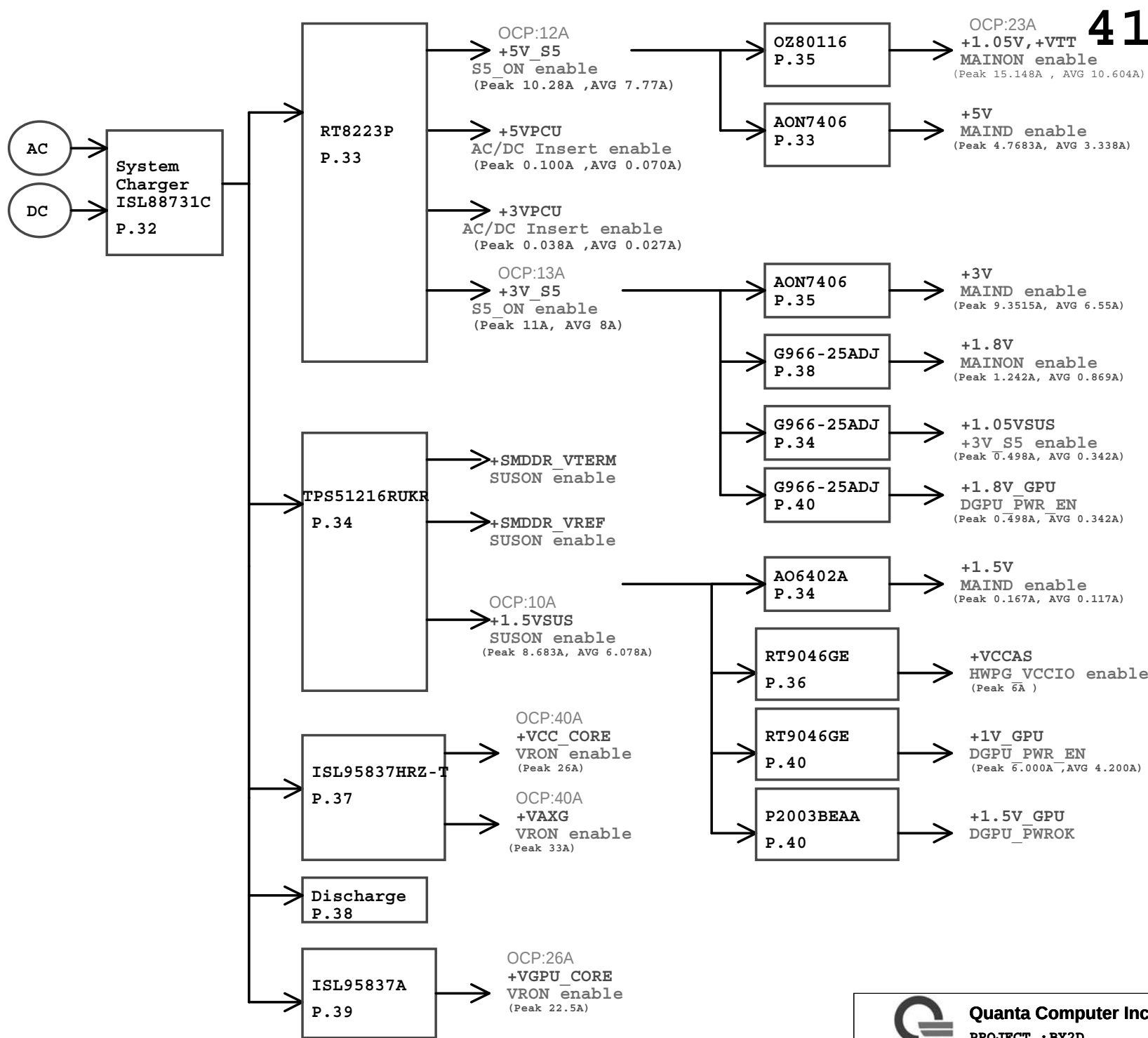
(Peak 6.000A ,AVG 4.200A)
Total capacitor : 22uF



Power On Sequence

1. +3V_GPU connect +3V
2. PX_PWRGOOD Enable +VGPU_CORE
3. DGPU_PWROK Enable(Delay) +1.8V_GFX
4. DGPU_PWR_EN Enable(Delay) +1.5V_GFX
5. DGPU_PWR_EN Enable(Delay) +1V_GFX

 Quanta Computer Inc. PROJECT : BY2D		Size	Document Number	Rev
			+VGACORE	3B
Date:	Monday, March 26, 2012	Sheet	40	of 42



41

BY2D MB

MODEL	PAGE	FROM	To
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	40		

PAGE 10: BY2D, B Add BOARD_ID4 to set Hi=Int or Low=Ext USB3.0
PAGE 10: BY2D, B Correct BOARD_ID2 Hi=BY2D Low=BY2
PAGE 22: BY2D, B Change R5147 from 10k to 1k for VGA loss issue
PAGE 24: BY2D, B Del R345 but add R338
PAGE 25: BY2D, B Mount C16 for WiMAX power issue
PAGE 26: BY2D, B Mount C371 for USB3.0 power issue
PAGE 31: BY2D, B Add RE_LED# PU 10k to +5VPCU
PAGE 34: BY2D, B Remove +1.05VUS power rail circuit
PAGE 38: BY2D, B Remove LCD_BK_POWER power rail circuit PU12,PL11,PD14,PC152,PC158,PR555,PR556,PR233,PC86,PR81,PC394,PC393,PR230,PR232,PC155,PC156,PC157
PAGE 08: BY2D, C Add D15 and remove D19 & D18
PAGE 09: BY2D, C Change usb3.0 port from port2 to port1
PAGE 09: BY2D, C Change usb2.0(Colay w/ USB 3.0) port from port1 to port0
PAGE 24: BY2D, C Del R338 but add R345
PAGE 33: BY2D, C Remove PC133
PAGE 37: BY2D, C Change PR124 from 2.37k to 3.24k, PR95 from 3.83K to 5.76K
PAGE 38: BY2D, C Add LCD_BK_POWER power rail circuit PU12,PL11,PD14,PC152,PC158,PR555,PR556,PR233,PC86,PR81,PC394,PC393,PR230,PR232,PC155,PC156,PC157
PAGE 38: BY2D, C Change PR232 from 97.6K to 52K
The BY2D, D schematic is the same as BY2D, C
PAGE 3: BY2D, E R118,R383 Change footprint to short PAD
PAGE 3: BY2D, E Add ESD parts D46,D47,D48
PAGE 5: BY2D, E R112,R113,R208,R209,R218,R220 Change footprint to short PAD
PAGE 8: BY2D, E Add U2005,R2222,R2223,R2231,R481,R455,R274,C2020,R302 second BIOS into BOM
PAGE 9: BY2D, E R108,R140,R154,R155,R179,R305,R306,R314,R341,R342 Change footprint to short PAD
PAGE 11: BY2D, E R69 Change footprint to short PAD
PAGE 15: BY2D, E R3517,R3571,R3579,R3582,R3616 Change footprint to short PAD
PAGE 18: BY2D, E R3700 Change footprint to short PAD
PAGE 18: BY2D, E Change C3600 footprint from 0603 to 0805
PAGE 23: BY2D, E R7 Change footprint to short PAD
PAGE 24: BY2D, E R13,R231 Change footprint to short PAD
PAGE 24: BY2D, E Add C6 for LCD noise.
PAGE 26: BY2D, E R129,R130,R183,R184 Change footprint to short PAD
PAGE 26: BY2D, E Change C364 footprint from 0805 to 1206
PAGE 26: BY2D, E Delete L9
PAGE 27: BY2D, E R248,R486 Change footprint to short PAD
PAGE 29: BY2D, E Delete L19
PAGE 29: BY2D, E R514 Change footprint to short PAD
PAGE 29: BY2D, E Mount C268
PAGE 30: BY2D, E Hole17 disconnect to GND
PAGE 31: BY2D, E Remove R226
PAGE 31: BY2D, E Add ESD parts D49,D50
PAGE 32: BY2D, E Remove R226
PAGE 34: BY2D, E Change PR54,PR58 footprint from RC0402 to SHORT0402
PAGE 35: BY2D, E Change PC76,PC77,PC78,PC79 footprint from 0603 to 0805
PAGE 37: BY2D, E Change PQ20,PQ21 from FDMS3660S to MS3606S
PAGE 37: BY2D, E Change PR107,PR134 from 1.02kOhm to 1.2kOhm
PAGE 37: BY2D, E Change PC114 from 68pF to 100pF
PAGE 37: BY2D, E Add PC166,PC170 330U12.5V 3528P E9b
PAGE 37: BY2D, E Change PC89 from 47pF to 68pF
PAGE 37: BY2D, E Change PC92 from 270pF to 330pF
PAGE 37: BY2D, E Change PR93 from 255kOhm to 169kOhm
PAGE 38: BY2D, E PU12.9 connect to GND
PAGE 39: BY2D, E Change PQ38 from FDMS3660S to FDMS3606S