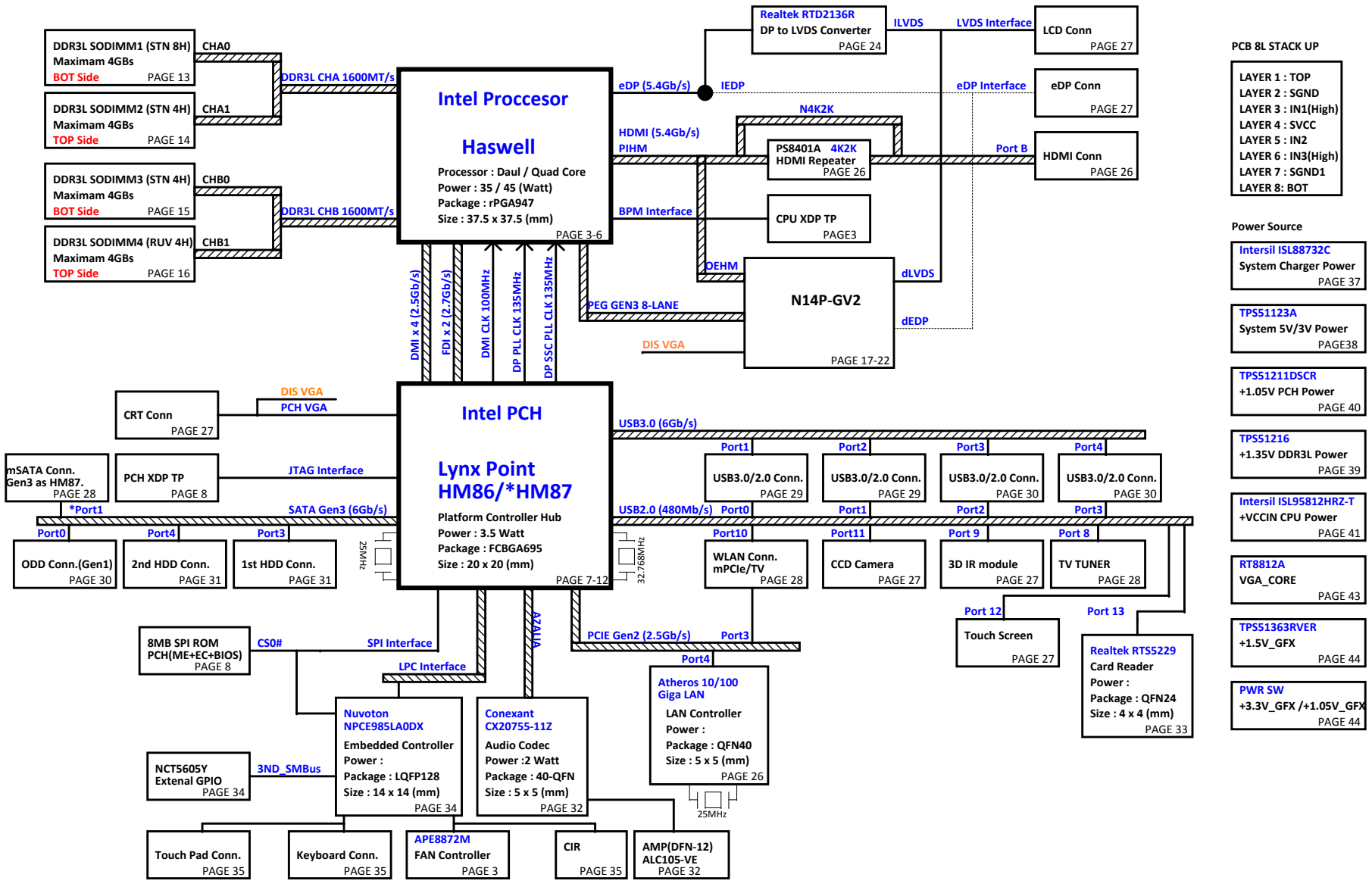
(17.3") Intel Shark Bay Platform Block Diagram

01



PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : SVCC
LAYER 5 : IN2
LAYER 6 : IN3(High)
LAYER 7 : SGND1
LAYER 8: BOT

Power Source

Intersil ISL88732C
System Charger Power
PAGE 37

TPS51123A
System 5V/3V Power
PAGE38

TPS51211DSCR
+1.05V PCH Power
PAGE 40

TPS51216
+1.35V DDR3L Power
PAGE 39

Intersil ISL95812HRZ-T
+VCCIN CPU Power
PAGE 41

RT8812A
VGA_CORE
PAGE 43

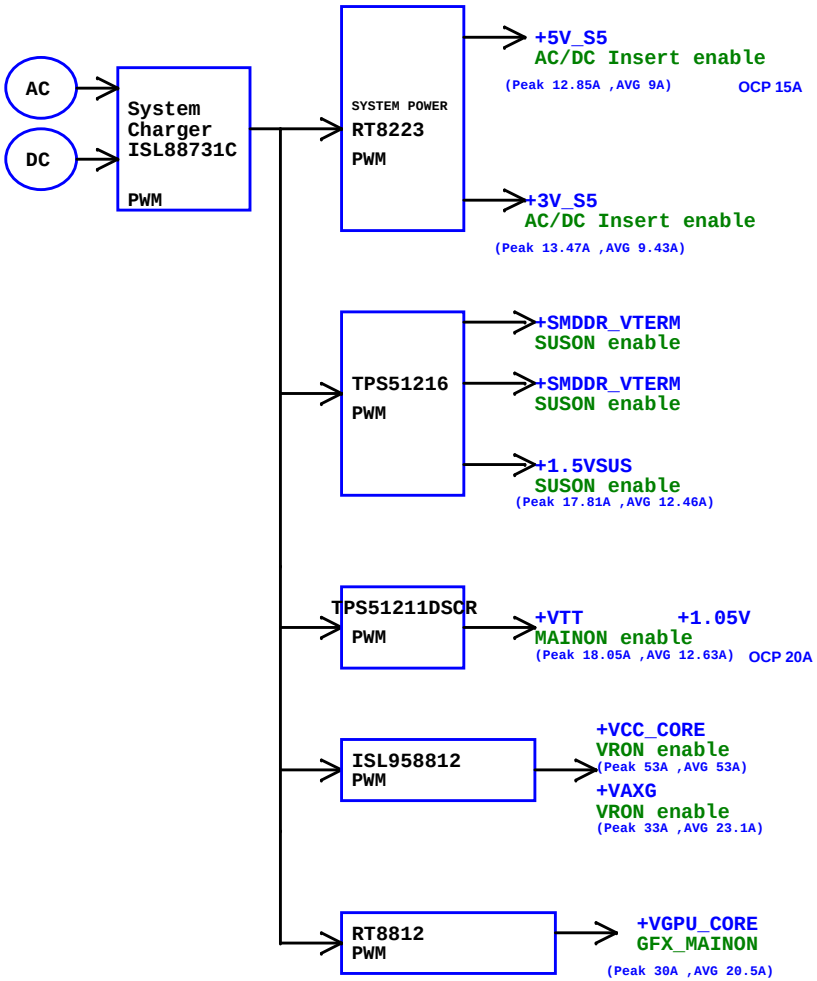
TPS51363RVER
+1.5V_GFX
PAGE 44

PWR SW
+3.3V_GFX /+1.05V_GFX
PAGE 44

Quanta Computer Inc.
PROJECT : BDBD

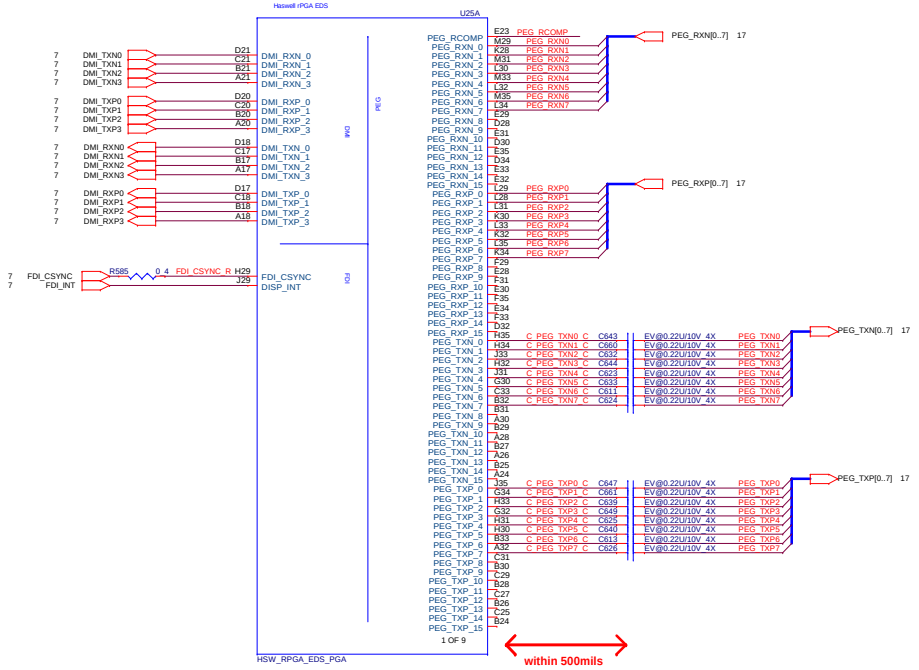
Size	Document Number	Rev
	Block Diagram	2A

Date: Monday, December 17, 2012 Sheet 1 of 45

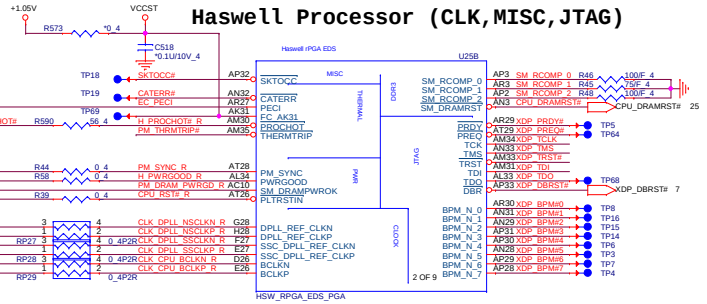


POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
+VCCRTC	+3.0V~+3.3V		S0~S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0~S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0~S5
+5VPCU	+5V	AC/DC Insert enable	S0~S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0~S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0

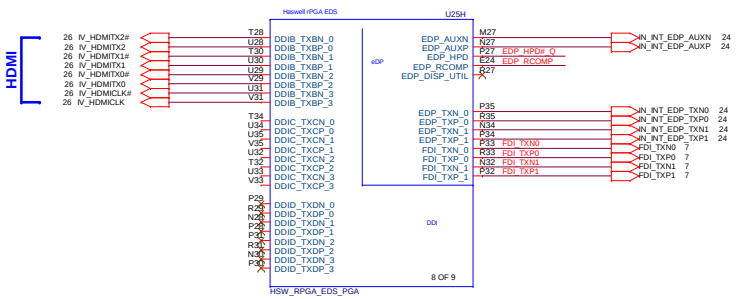
Haswell Processor (DMI,PEG,FDI)



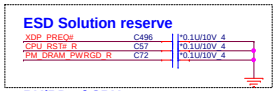
Haswell Processor (CLK,MISC,JTAG)



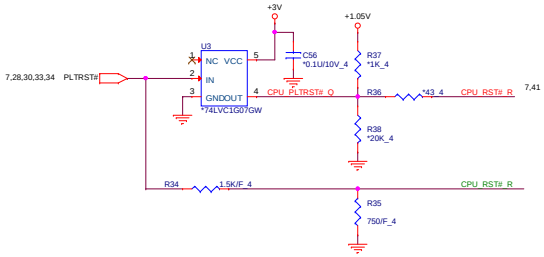
Haswell Processor (DDI,eDP,FDI)



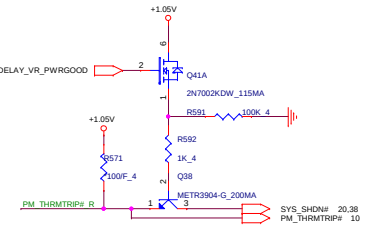
ESD Solution reserve



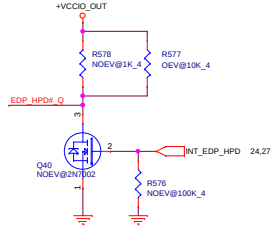
CPU



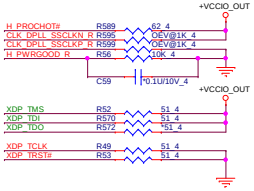
Thermal Trip & Process HOT CPU



eDP Hot Plug Detect CPU

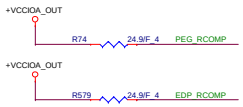


PU/PD of CPU

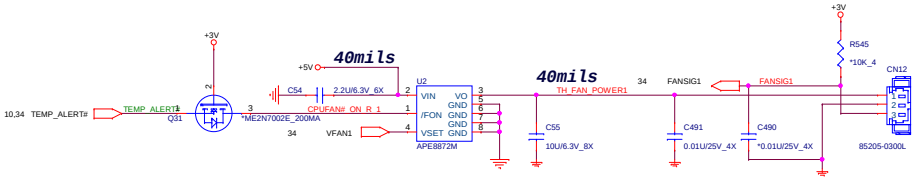


FDI Disabling (Discrete Only) <CPU>

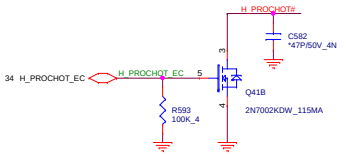
DP & PEG Compensation <CPU>



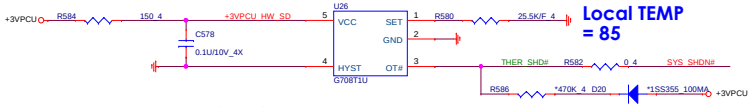
FAN Control-->For one FAN solution <THC>



Intel Turbo mode only CPU



CPU Thermal sensor / MB Local TEMP <THC>



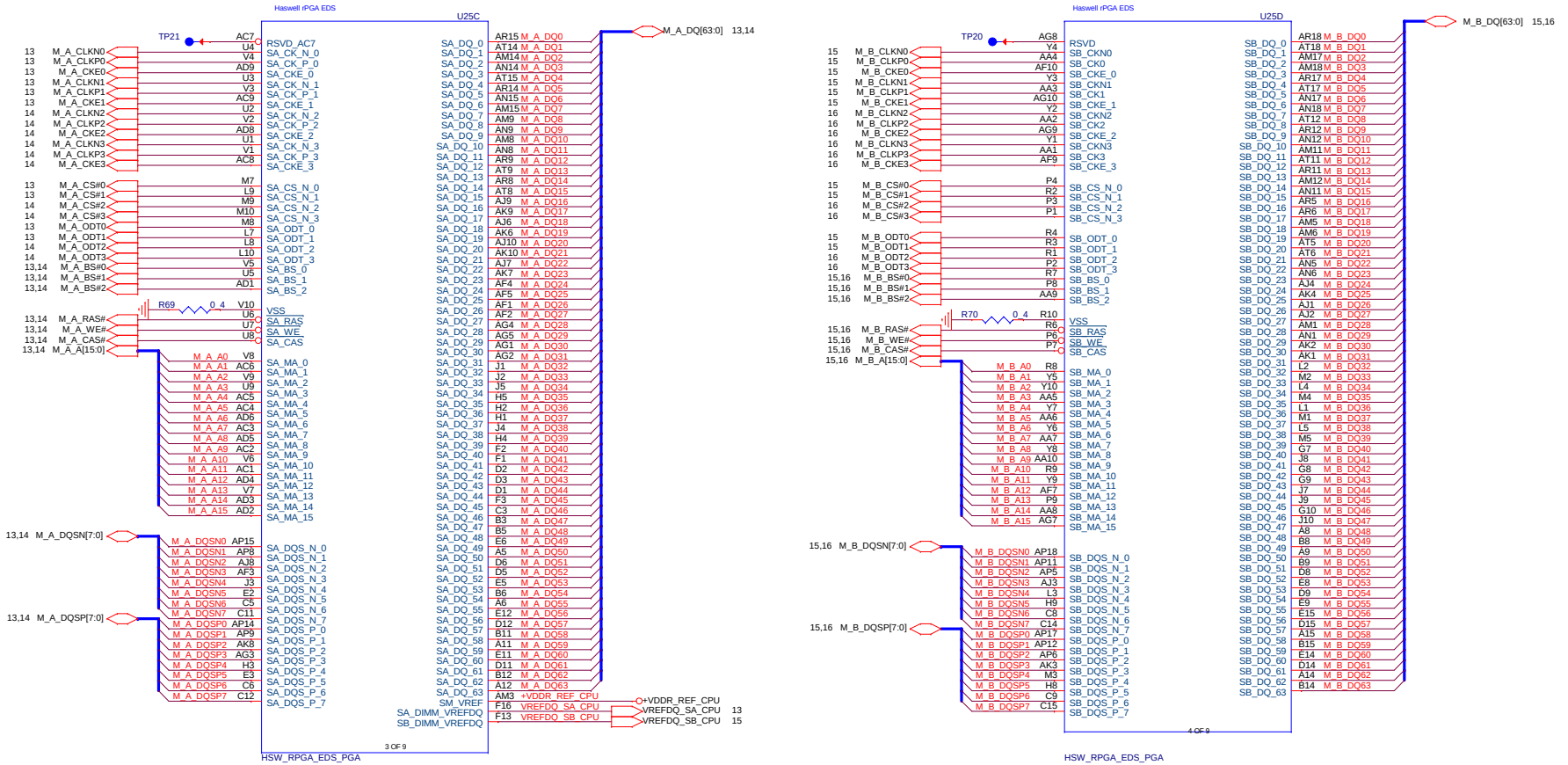
Local TEMP = 85

Rset(Kohm)=0.0012T*T-0.9308T+96.147,Shut down on 85dgree
Hysteresis is 30C

Quanta Computer Inc.
PROJECT : BDBD

Size	Document Number	Rev
	Haswell 1/5 (PEG/DMI/FDI)	2A
Date: Monday, December 17, 2012	Sheet 3 of 45	

Haswell Processor (DDR3)



Quanta Computer Inc.			
PROJECT : BDBD			
Size	Document Number		Rev
	Haswell 2/5 (DDR3 I/F)		2A
Date: Monday, December 17, 2012	Sheet 4 of 45		

Haswell Processor (POWER)

05

+1.35V_CPU 4.2A

+VCCIN 95A

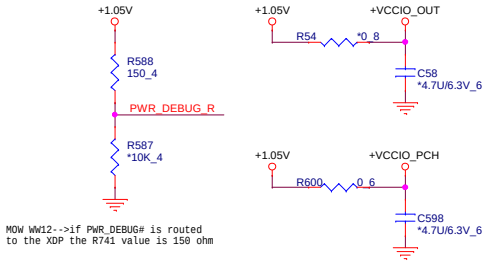
Haswell rPGA EDS

U25E

5 OF 9

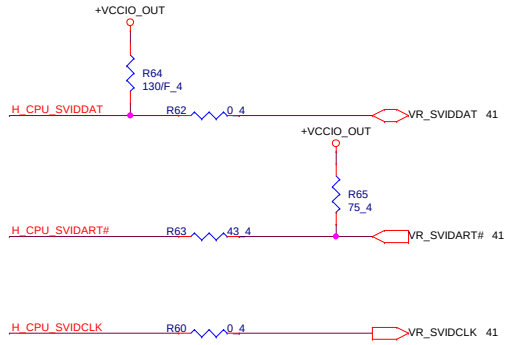
HSW_RPGA_EDS_PGA

Power Test Propose



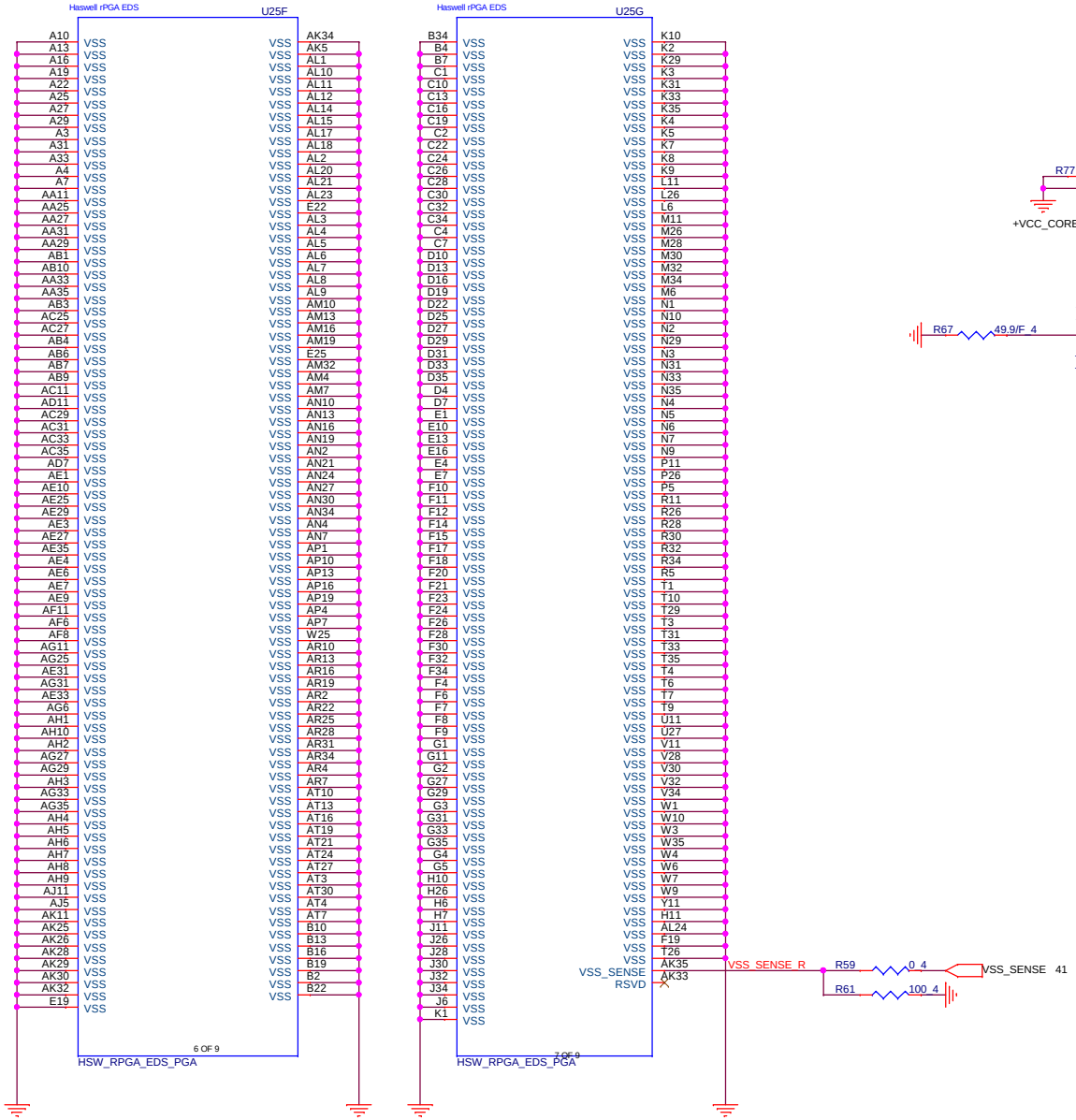
MOW WW12-->if PWR_DEBUG# is routed to the XDP the R741 value is 150 ohm

SVID

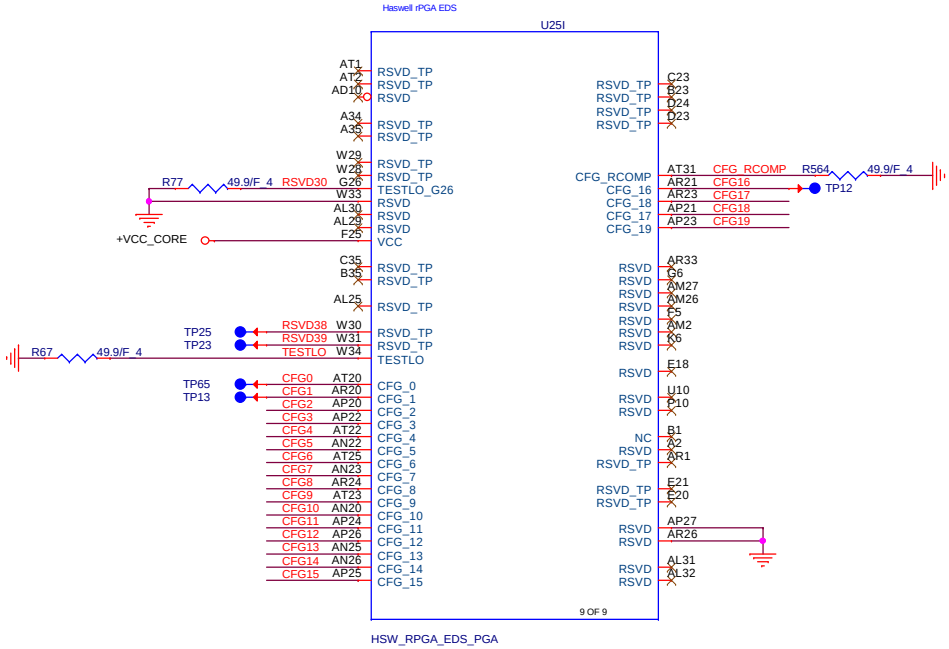


Quanta Computer Inc.		
PROJECT : BDBD		
Size	Document Number: Haswell 4/5 (POWER)	Rev: 2A
Date: Monday, December 17, 2012	Sheet 5 of 45	

Haswell Processor (GND)



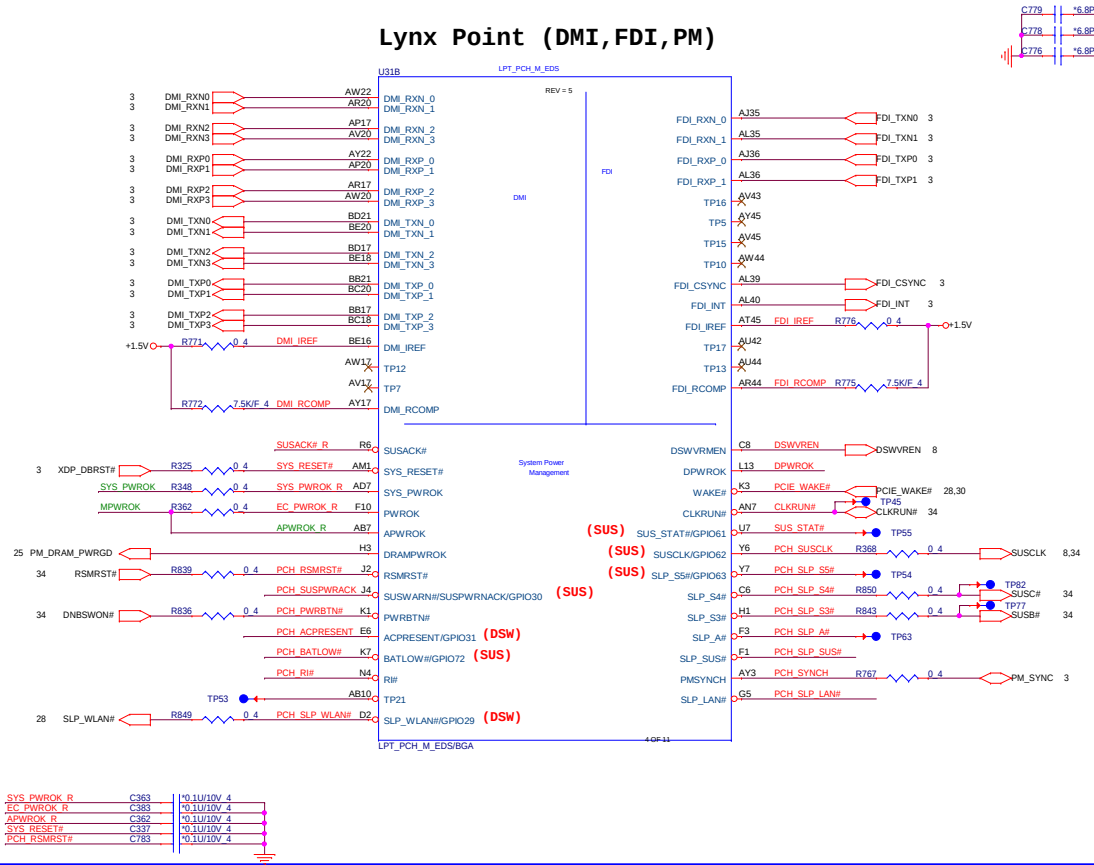
Haswell Processor (CFG,RSVD)



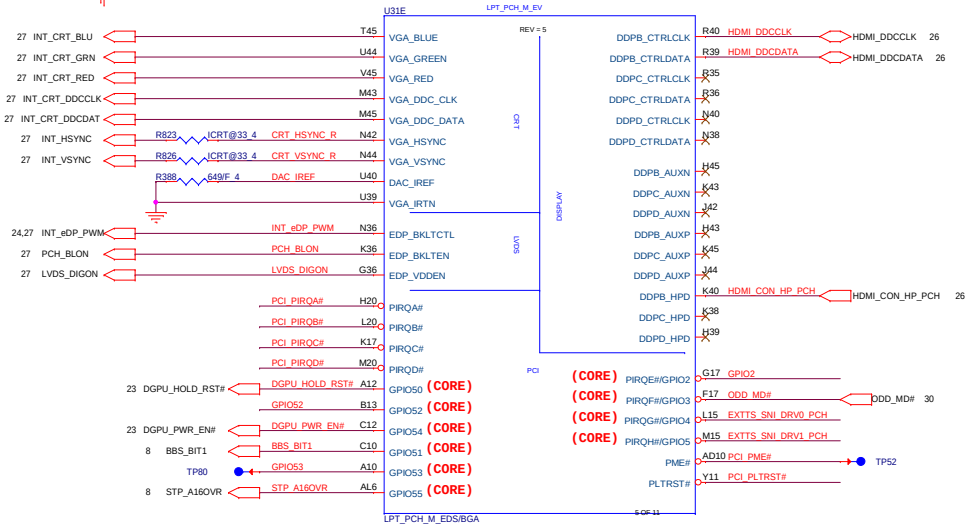
06

Quanta Computer Inc.		
PROJECT : BDBD		
Size	Document Number: Haswell 5/5 (CFG/GND)	Rev 2A
Date: Monday, December 17, 2012	Sheet 6 of 45	

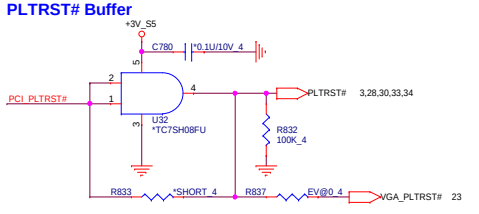
Lynx Point (DMI,FDI,PM)



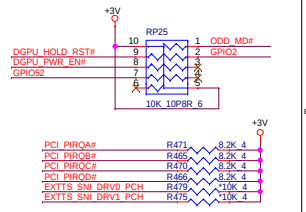
Lynx Point (CRT,PCI,DDI CNTL)



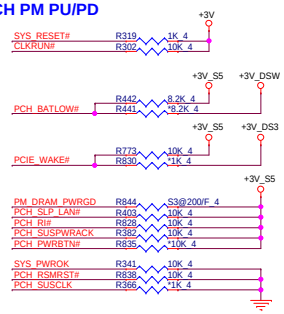
PLTRST# Buffer



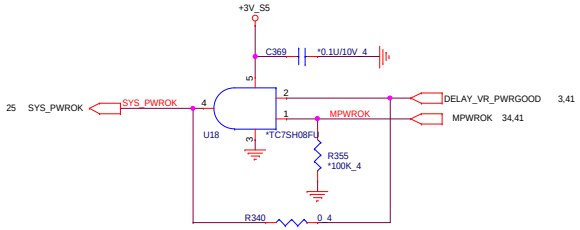
PCI PU



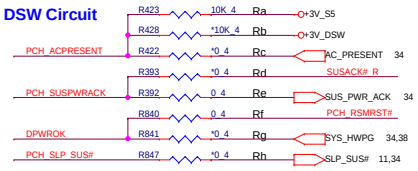
PCH PM PU/PD

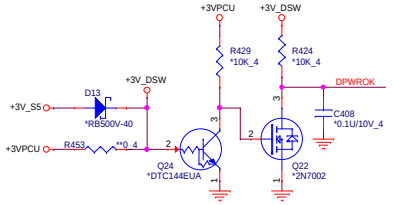


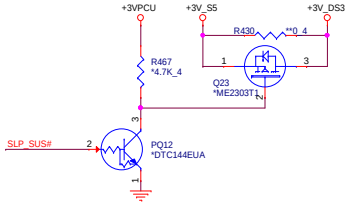
SYSPWOK



DSW Circuit







Quanta Computer Inc.
PROJECT : BDBD

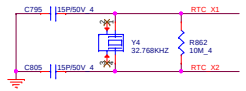
Size	Document Number	Rev
	LPT 1/6 (DMI/FDI/VGA)	2A
Date: Monday, December 17, 2012	Sheet 7 of 45	

Lynx Point (RTC,IHDA,SATA,JTAG)

Lynx Point (LPC,SPI,SMBUS,C-LINK,THERMAL)

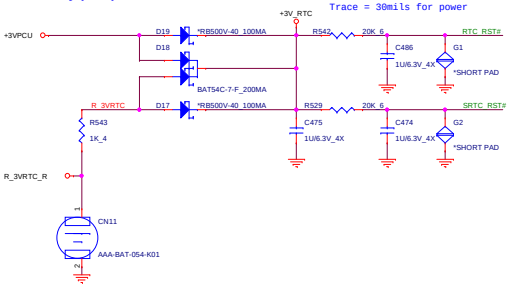
08

RTC Clock 32.768KHz (RTC)

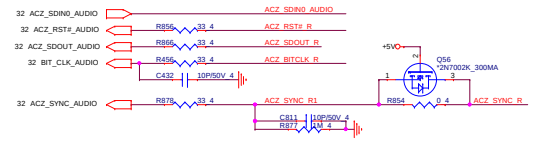


RTC Circuitry (RTC)

Trace = 30mils for power

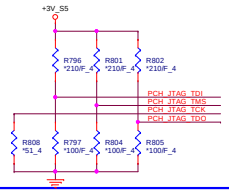


HDA

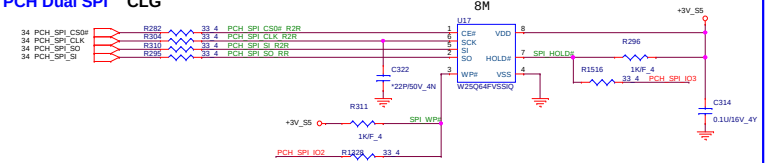


PCH JTAG

JTAG_TCK,JTAG_TMS
Trace Length < 9000mils



PCH Dual SPI CLG



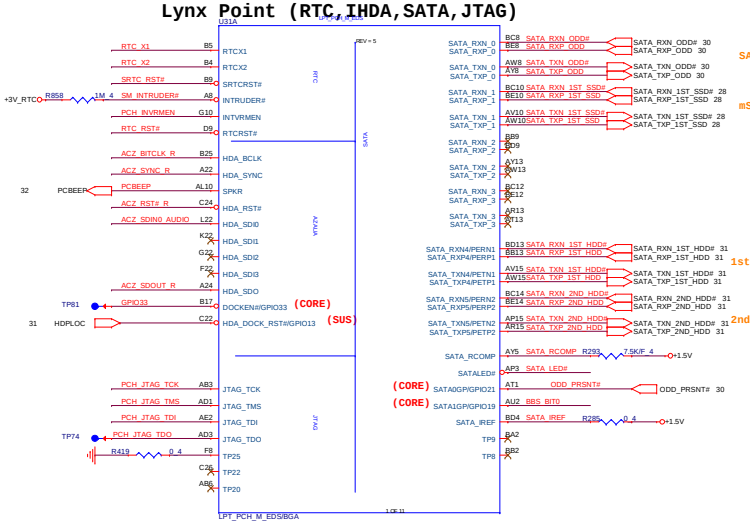
EC (EC+BIOS):SPI_CS0#

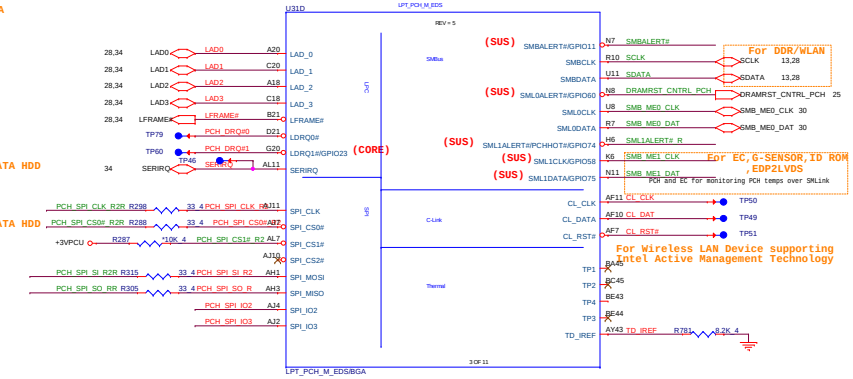
SATA ODD

mSATA

1st SATA HDD

2nd SATA HDD





For DDR/WLAN

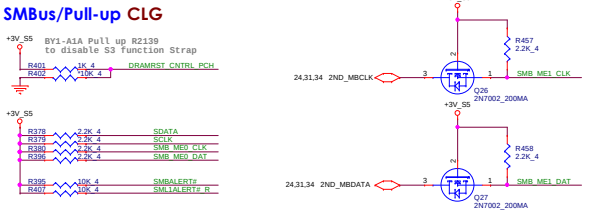
For EC,G-SENSOR,ID ROM ,EDP2LVDS

PCH and EC for monitoring PCH temps over SMLink

For Wireless LAN Device supporting Intel Active Management Technology

CLG

SMBus/Pull-up CLG



PCH STRAPING

Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	PCBEEP R438 *1K_4 +3V
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	7,34 SUSCLK R367 *1K_4
GPIO55	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	7 STP_A16OVR R335 *1K_4
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	PCH_INVRMEN R431 330K_4 +3V_RTC
GPIO51	Boot BIOS Strap bit 1	PWROK	Bit1 Bit0 1 0 Resvered 1 1 SPI 0 0 LPC	7 BBS_BIT1 R432 *1K_4
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK		BBS_BIT0 R783 *1K_4
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	34 ACZ_SDOUT R851 *1K_4 VCC_HDA_IO
GPIO36	RSVD	PWROK	Internal PD	10 GPIO36 R786 *1K_4 +3V
SATA3GP/GPIO37	TLS Confidentiality	PWROK	0 = TLS no confidentiality (Int PD) 1 = TLS with confidentiality	10 FDI_OVRVLTG R795 *1K_4 +3V
GPIO8	RSVD	RSMRST#	Internal PU	10 GPIO8 R815 10K_4
GPIO28	PLL on die VR enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	10 PLL_ODVR_EN R358 *1K_4
DSWVREN	On Die DSW VR Enable	Always	0 = Disable 1 = Enable Must be PU to VCCRTC	7 DSWVREN R857 330K_4 R862 330K_4 +3V_RTC

Quanta Computer Inc.

PROJECT : BDBD

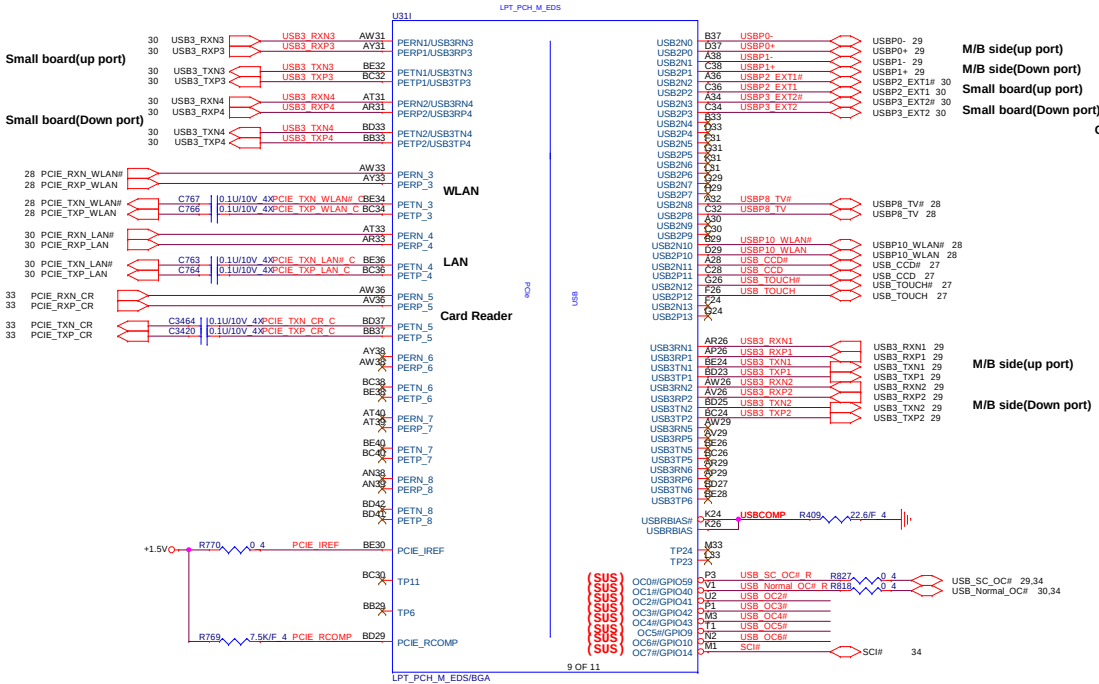
Size	Document Number	Rev
	LPT 2/6 (SATA/HDA/SPI)	2A

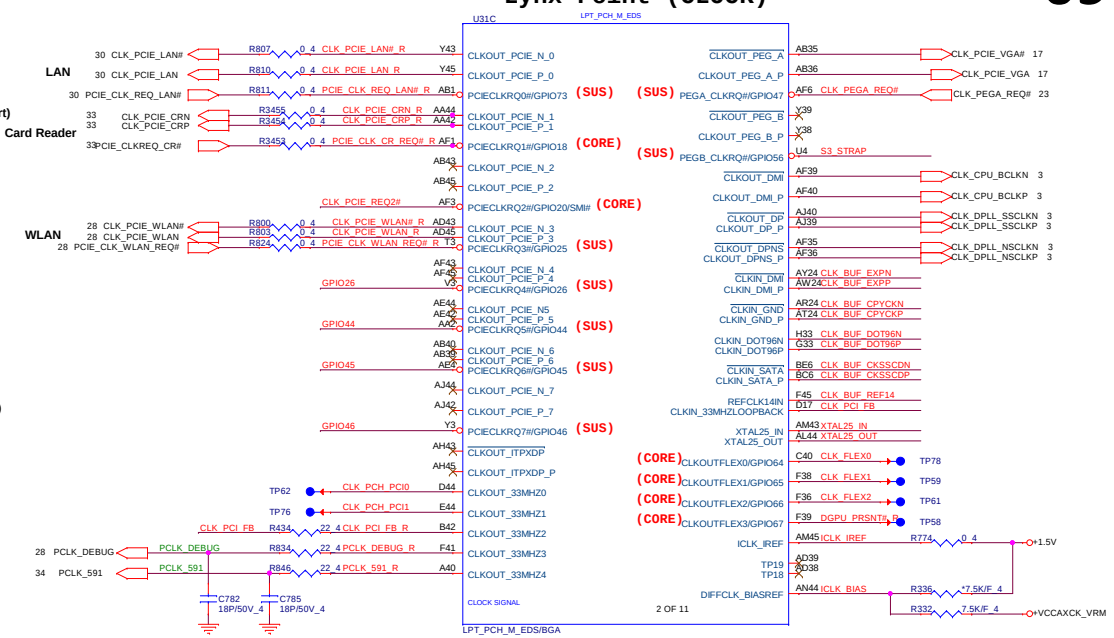
Date: Monday, December 17, 2012 Sheet 8 of 45

Lynx Point (PCIE,USB3.0,USB2.0)

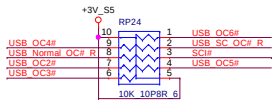
Lynx Point (CLOCK)

09

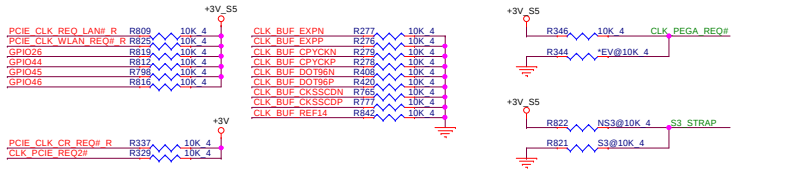




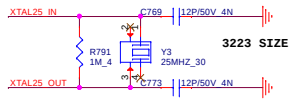
USB Overcurrent



PCH Intenal Clock



25MHz Crystal for PCH



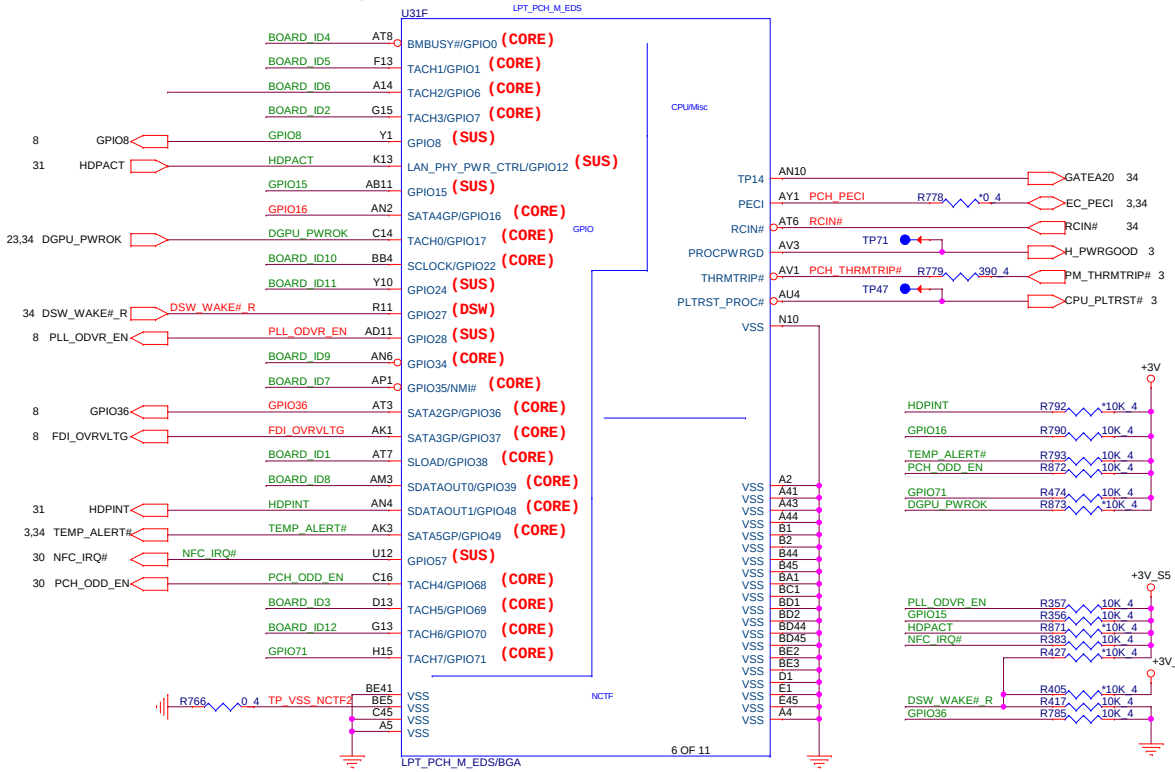
Quanta Computer Inc.

PROJECT : BDBD

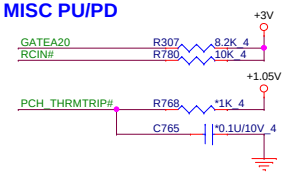
Size	Document Number	Rev
	LPT 3/6 (PCIE/USB/CLK)	2A

Date: Monday, December 17, 2012 Sheet 9 of 45

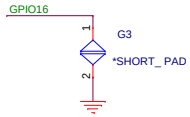
Lynx Point (GPIO,CPU/MISC,NCTF)



PCH MISC PU/PD

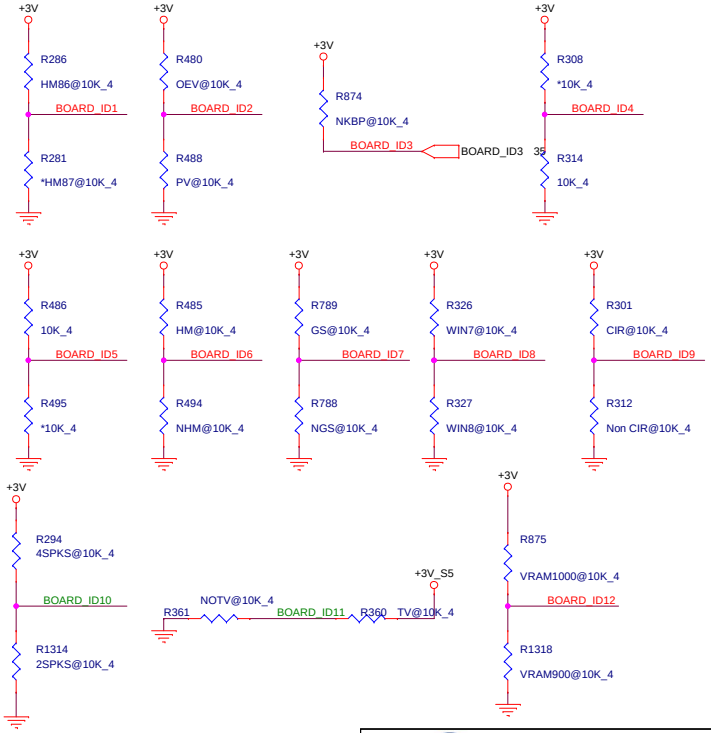


PU & Password Clear



BOARD ID SETTING CLG/PX/OEV/UGA/CLG-Strap

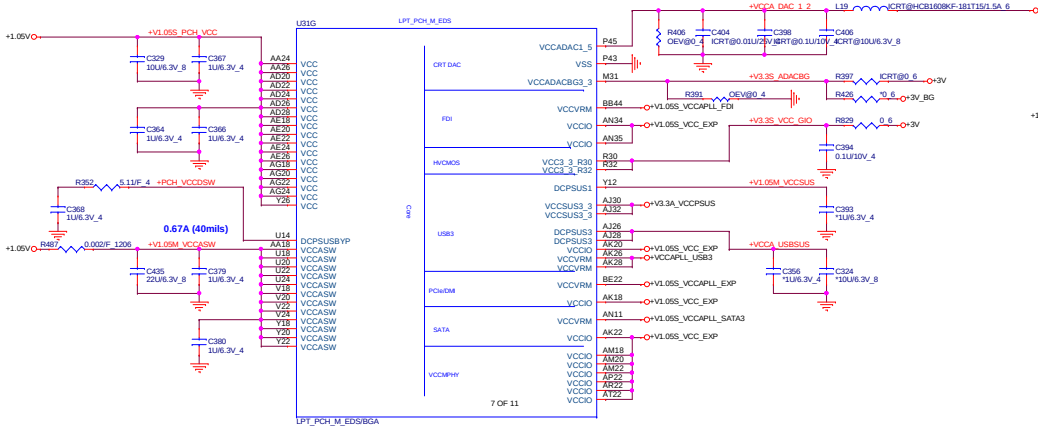
Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9	ID10	ID11	ID12
HM86 HM87	H L											
Only VGA OPTIMUS		H L										
W/O LED KB W/ LED KB			H L									
UMA Discrete				H L								
17" Premium 17" Gaming					H L							
W/ HDMI W/O HDMI						H L						
W/ G-sensor W/O G-sensor							H L					
WIN7 WIN8								H L				
ECO Mode 3D Mode									H L			
4 SPKS 2 SPKS										H L		
TV SKU SSD SKU											H L	
VRAM 1000 VRAM 900												H L

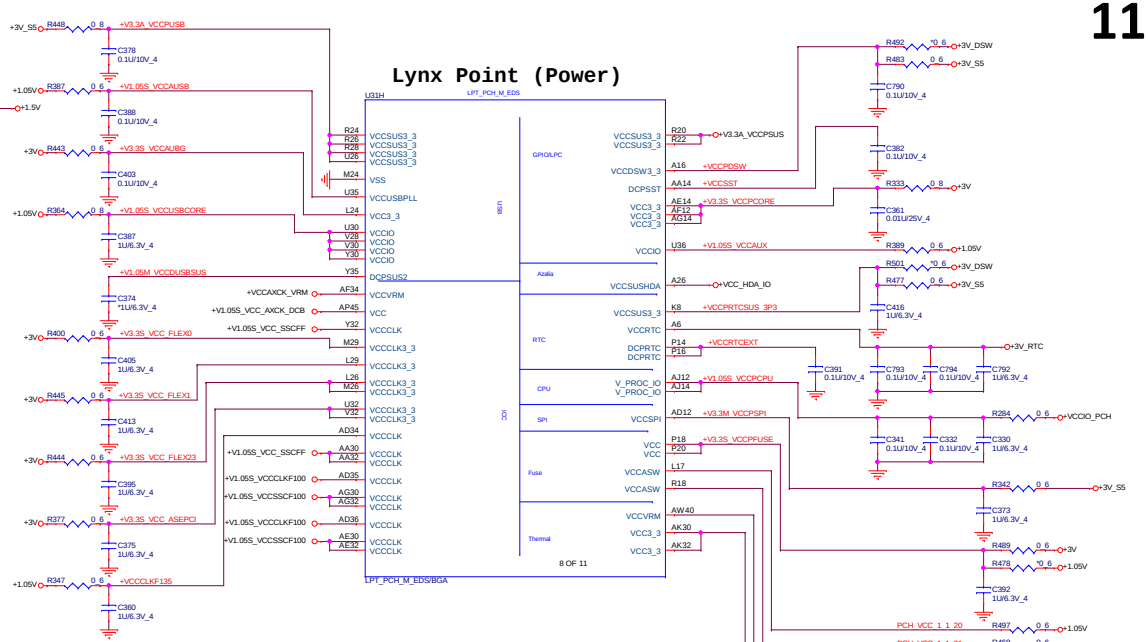


Quanta Computer Inc.
PROJECT : BDBD

Size	Document Number	Rev
	LPT 4/6 (GPIO/MISC)	2A
Date: Monday, December 17, 2012	Sheet 10 of 45	

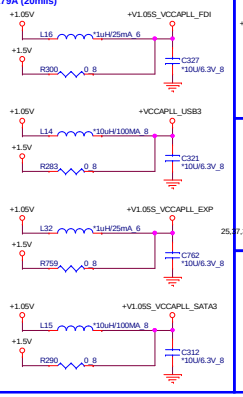
Lynx Point (Power)



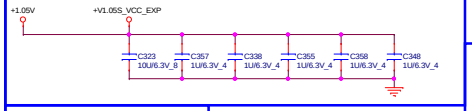


PCH VRM Power

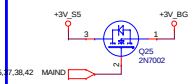
0.179A (20mils)



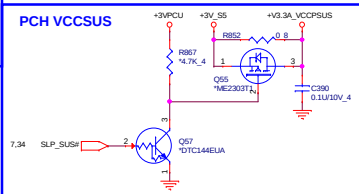
PCH VCCIO Power



PCH band gap Power

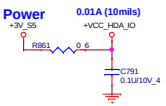


PCH VCCSUS



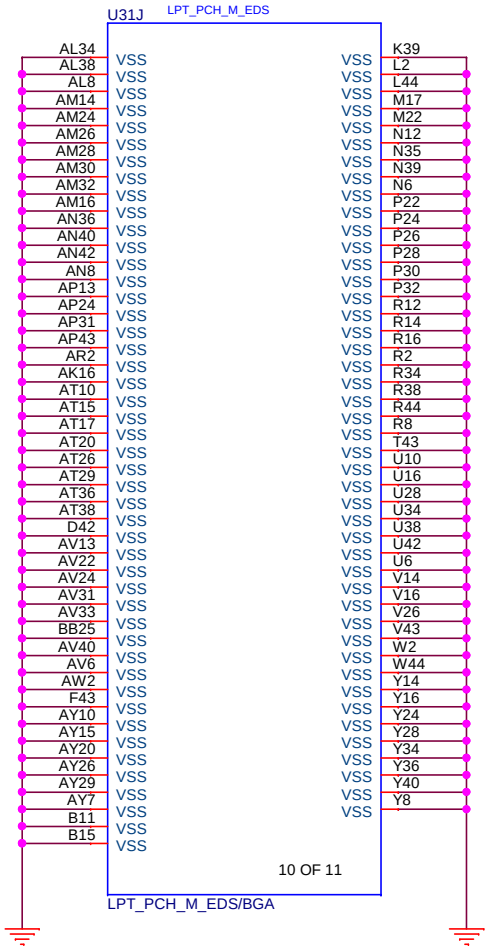
PCH HDA Power

0.01A (10mils)

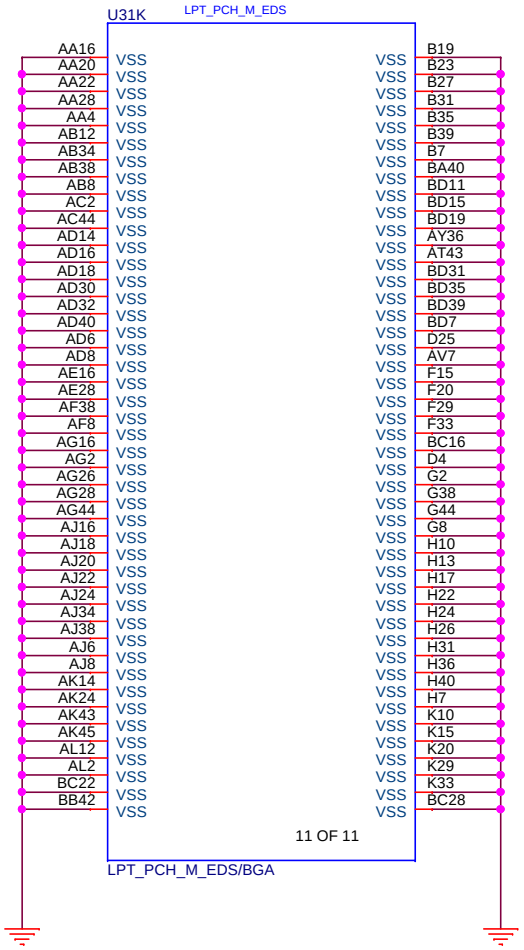


Quanta Computer Inc.			
PROJECT : BDBD			
Size	Document Number		Rev
	LPT 5/6 (POWER)		2A
Date: Monday, December 17, 2012	Sheet 11 of 45		

Lynx Point (GND)



Lynx Point (GND)



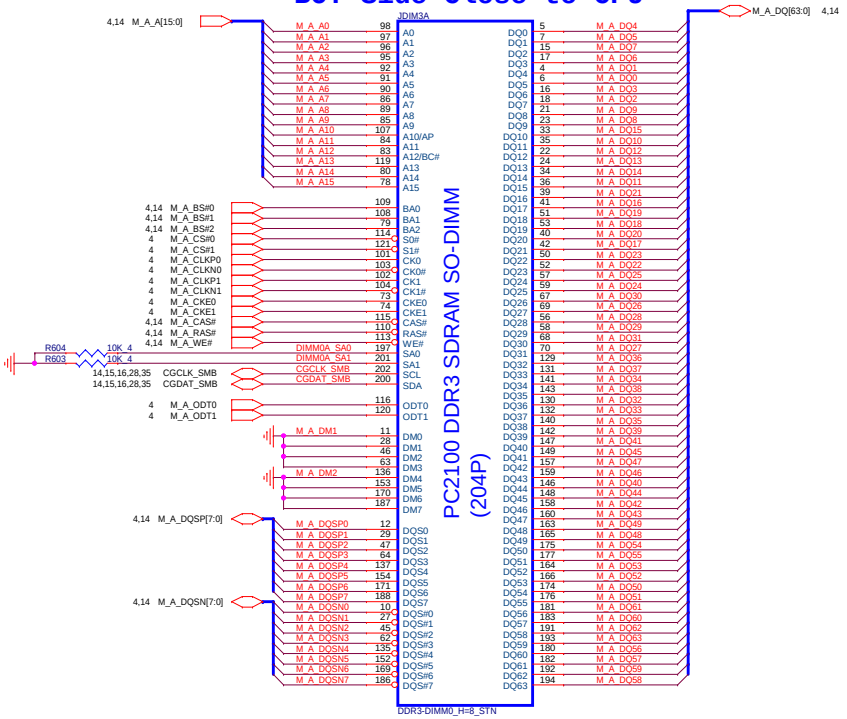
Quanta Computer Inc.

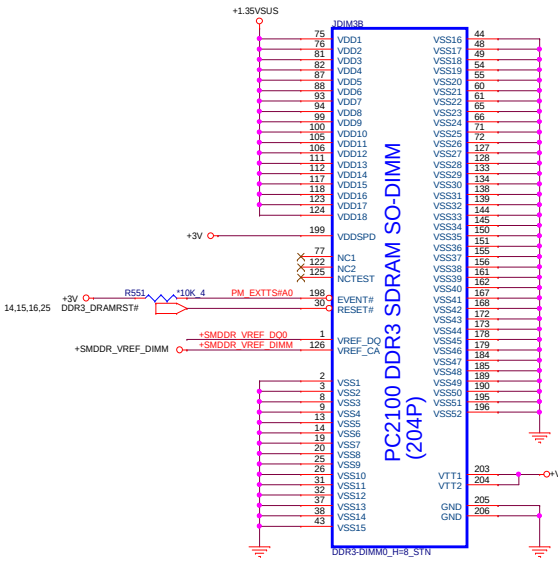
PROJECT : BDBD

Size	Document Number	Rev
	LPT 6/6 (GND)	2A

Date: Monday, December 17, 2012 Sheet 12 of 45

BOT Side Close to CPU

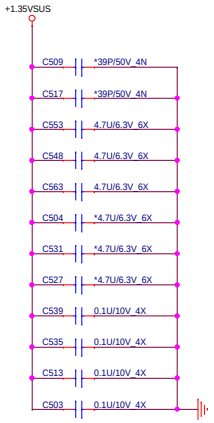


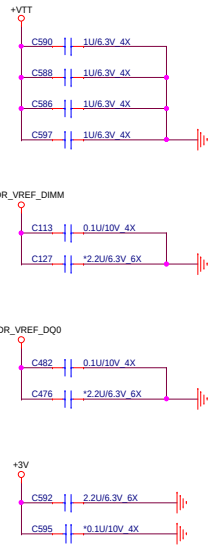


3,7,8,9,10,11,14,15,16,23,24,26,27,28,30,31,33,34,35,36,38,42 +3V

14,15,16,25,39 +VTT

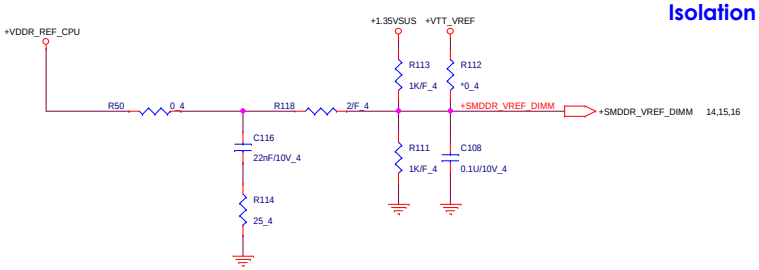
14,15,16 +SMDDR_VREF_DIMM





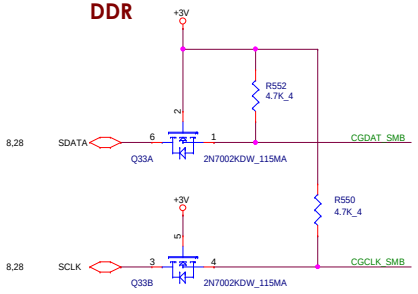
DDR3 VREF CA

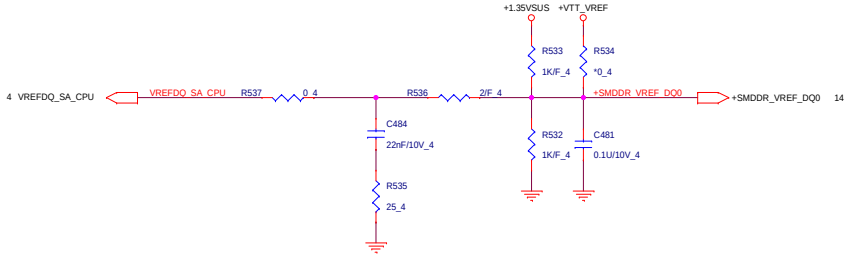
DDR



SMBus Isolation

DDR





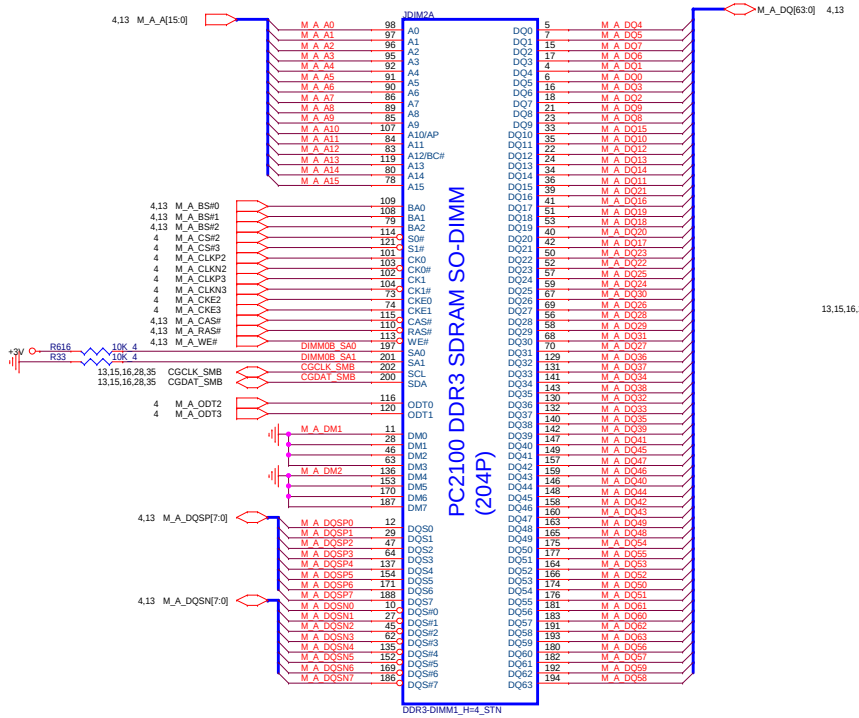
Quanta Computer Inc.

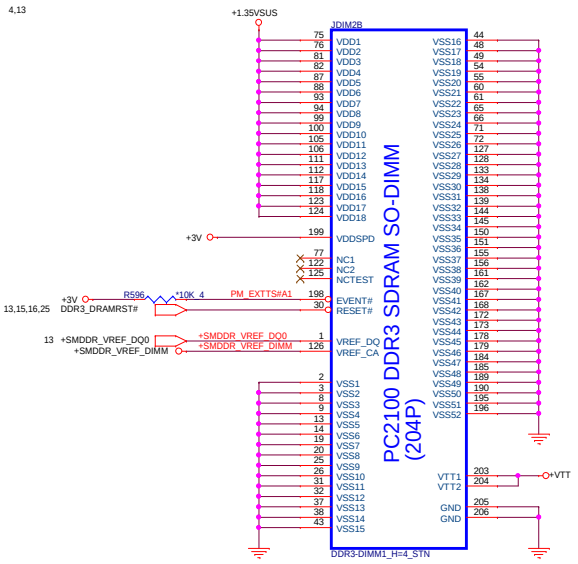
PROJECT : BDBD

Size	Document Number	Rev
	System Memory 1/4	2A

Date: Monday, December 17, 2012 Sheet 13 of 45

TOP Side Close to CPU

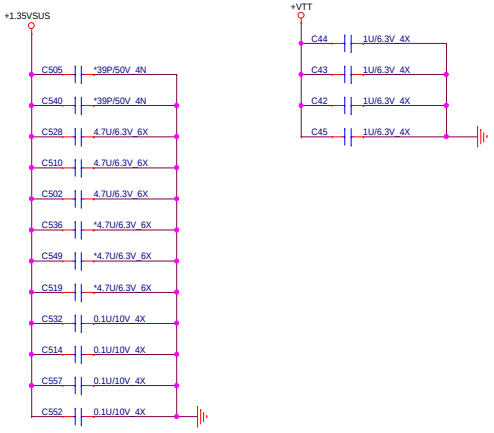


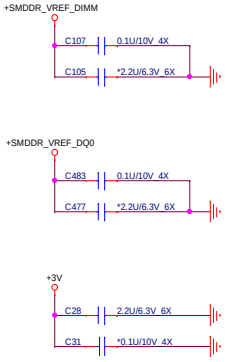


3,7,8,9,10,11,13,15,16,23,24,26,27,28,30,31,33,34,35,36,38,42 +3V

13,15,16,25,39 +VTT

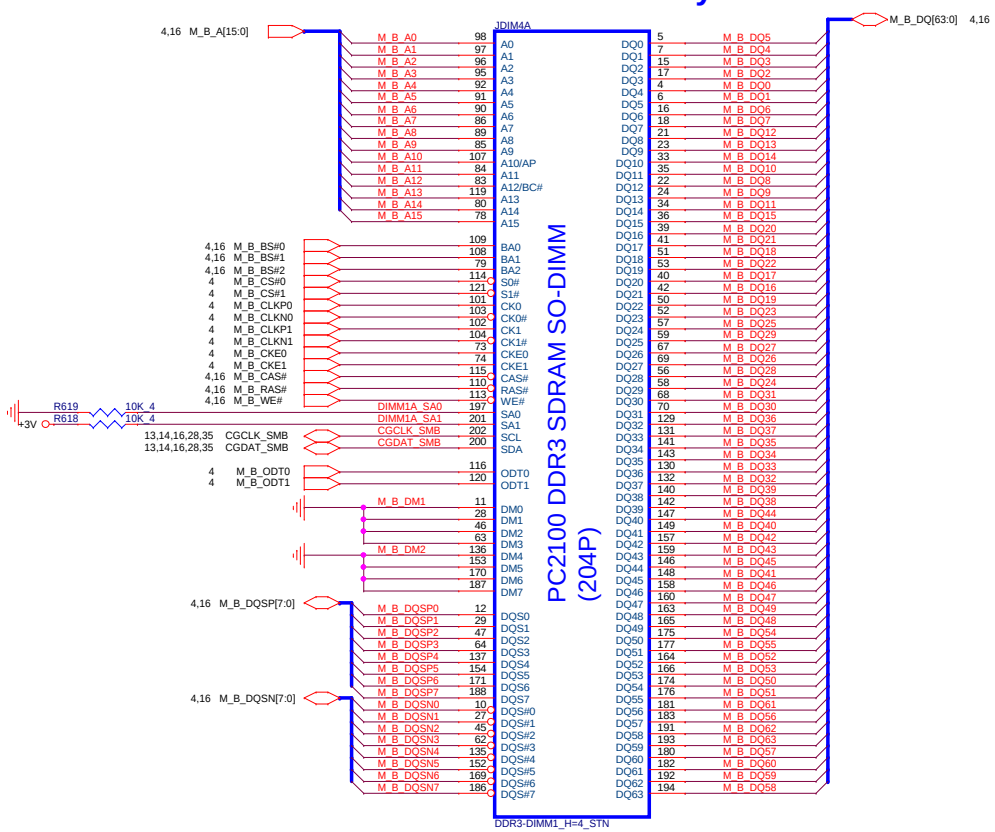
13,15,16 +SMDDR_VREF_DIMM

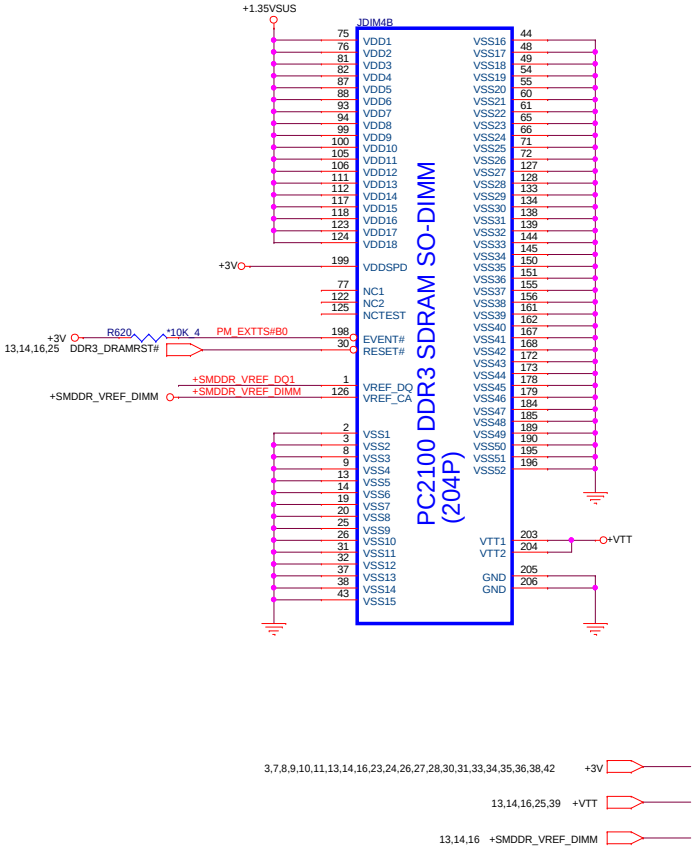


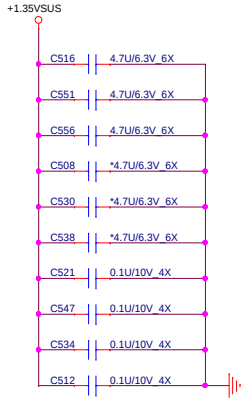


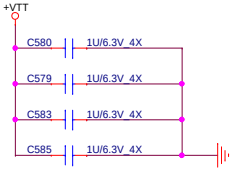
Quanta Computer Inc. PROJECT : BDBD			
Size	Document Number: System Memory 2/4		Rev 2A
Date: Monday, December 17, 2012		Sheet 14 of 45	

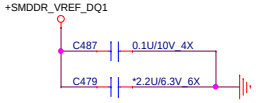
BOT Side Far away CPU

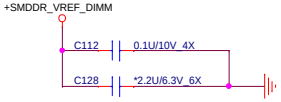


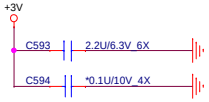


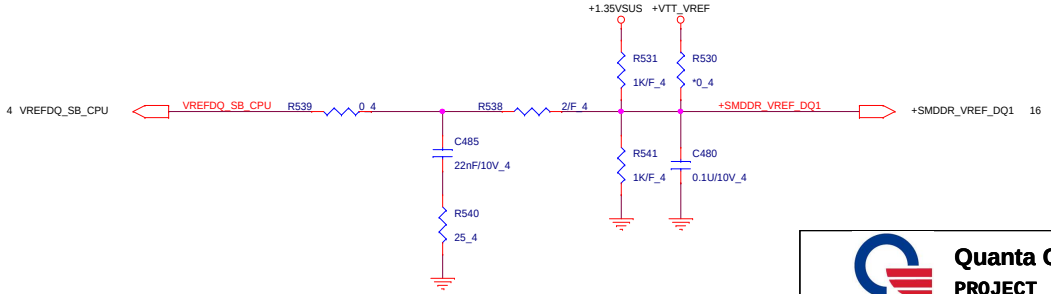












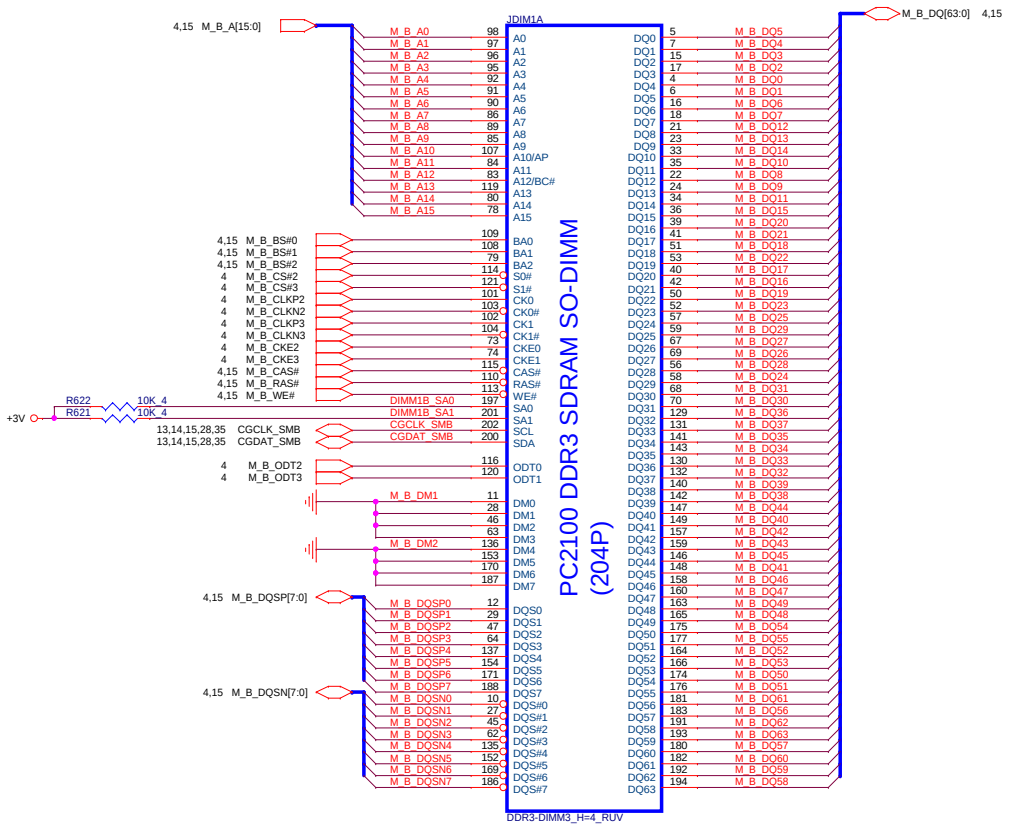
Quanta Computer Inc.

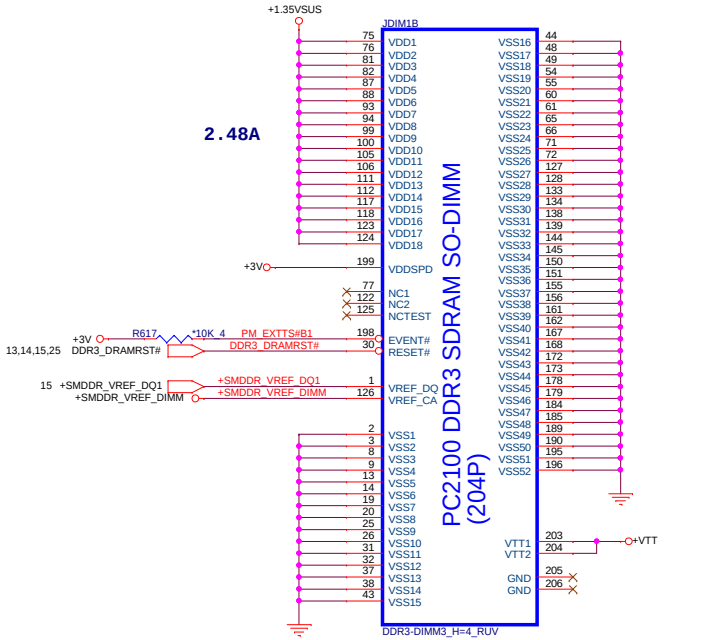
PROJECT : BDBD

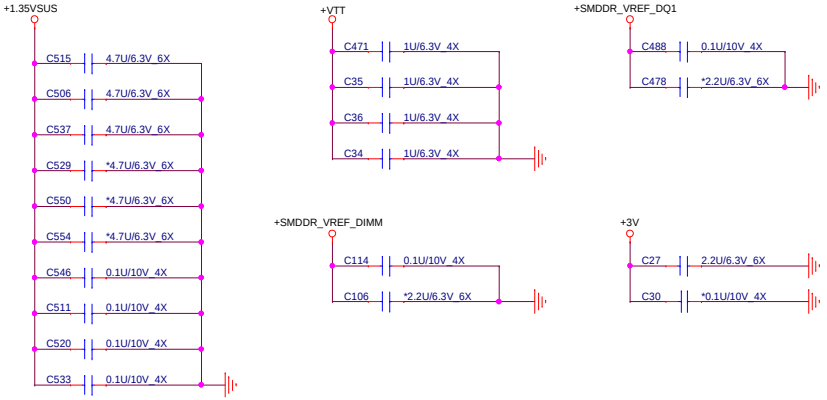
Size	Document Number	Rev
	System Memory 3/4	2A

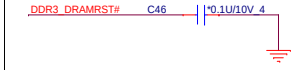
Date: Monday, December 17, 2012 Sheet 15 of 45

TOP Side Far away CPU







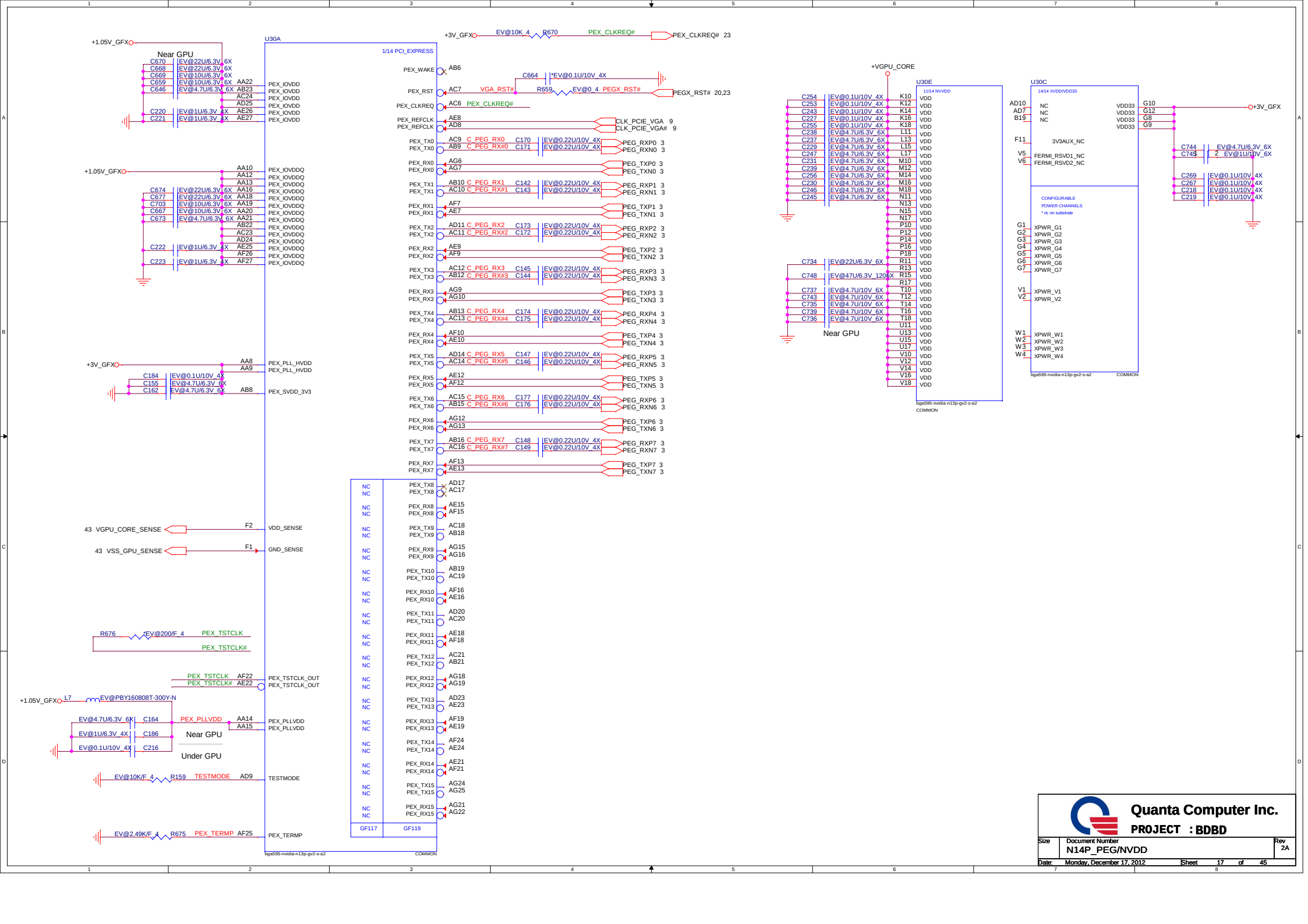


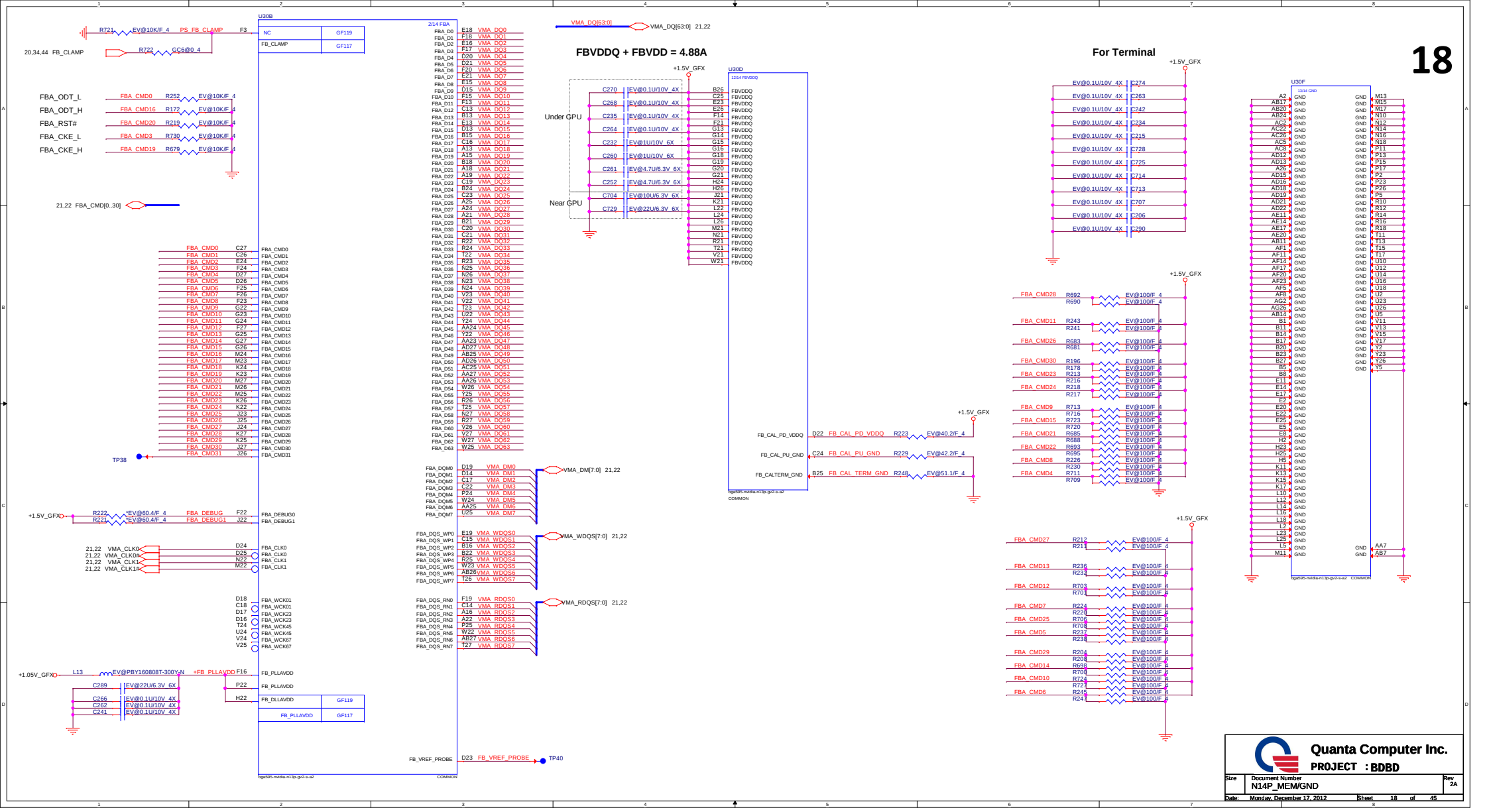
Quanta Computer Inc.

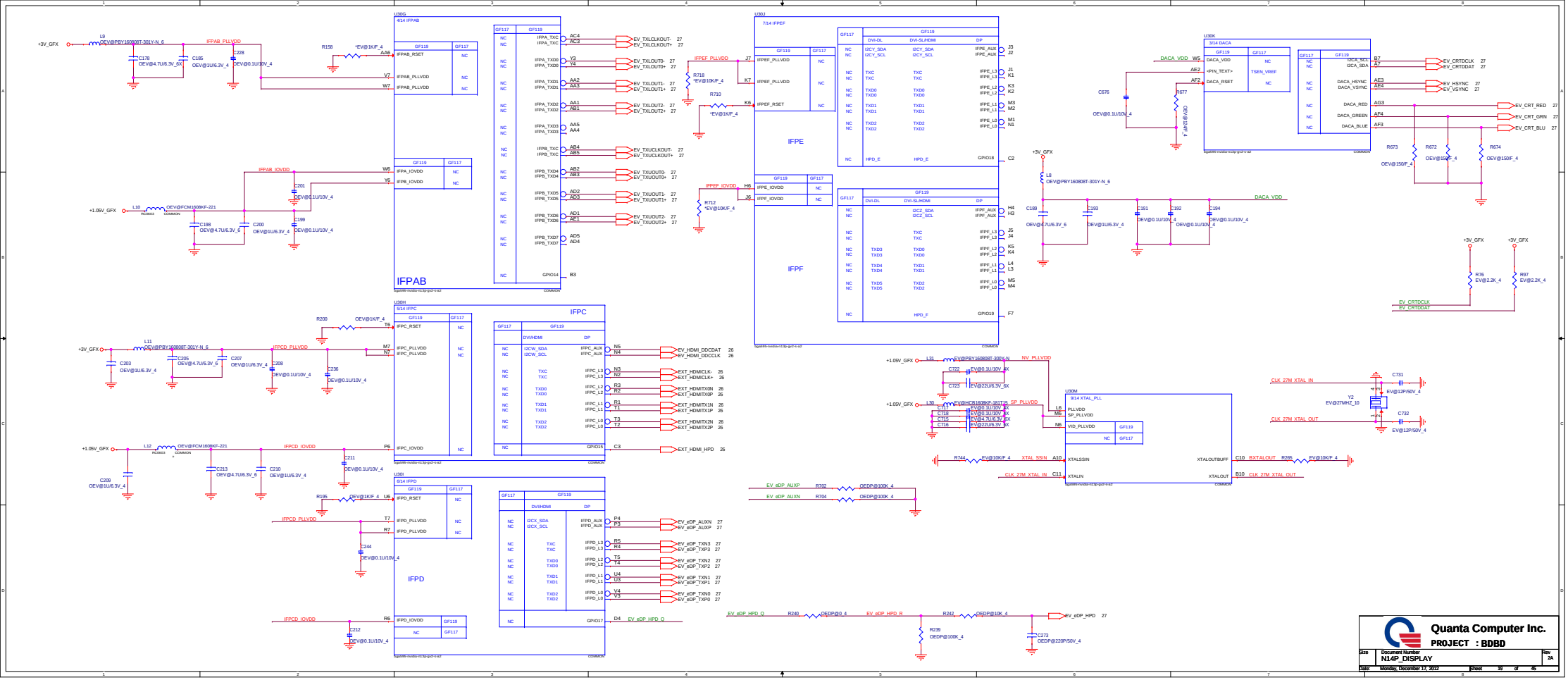
PROJECT : BDBD

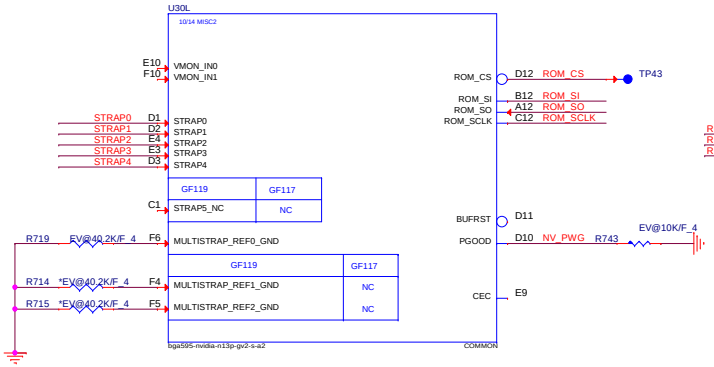
Size	Document Number	Rev
	System Mermory 4/4)	2A

Date: Monday, December 17, 2012 Sheet 16 of 45

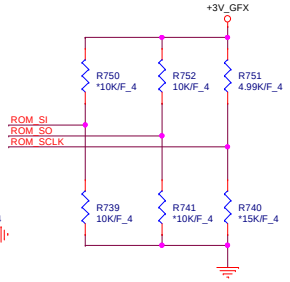

U30A
1/14 PCI_EXPRESS
Near GPU
Under GPU
+1.05V_GFX
+3V_GFX
+VGPU_CORE
U30E
11/14 NVVDD
U30C
14/14 XVDD/VDD33
3V3AUX_NC
CONFIGURABLE
POWER CHANNELS
* nc on substrate
bga595-nvidia-n13p-gv2-s-a2
COMMON
PEX_CLKREQ#
PEX_RST
PEX_CLKREQ
PEX_REFCLK
PEX_REFCLK#
PEX_TSTCLK
PEX_TSTCLK#
PEX_PLLVDD
TESTMODE
PEX_TERMP
VGA_RST#
VGPU_CORE_SENSE
VSS_GPU_SENSE
VDD_SENSE
GND_SENSE
PEX_SVDD_3V3
PEX_PLL_HVDD
PEX_IOVDD
PEX_IOVDDQ
PEX_TSTCLK_OUT
Quanta Computer Inc.
PROJECT : BDBD
Size
Document Number
N14P_PEG/NVDD
Rev
2A
Date: Monday, December 17, 2012
Sheet 17 of 45

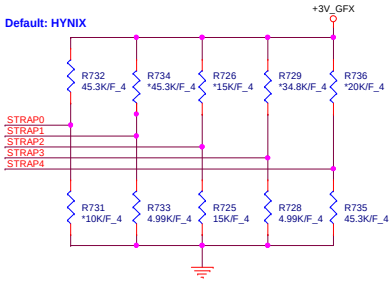

U30B
R721 EV@10K/F_4 PS_FB_CLAMP F3
20,34,44 FB_CLAMP
R722 GC6@0_4
NC GF119
FB_CLAMP GF117
FBA_ODT_L FBA_CMD0 R252 EV@10K/F_4
FBA_ODT_H FBA_CMD16 R172 EV@10K/F_4
FBA_RST# FBA_CMD20 R219 EV@10K/F_4
FBA_CKE_L FBA_CMD3 R730 EV@10K/F_4
FBA_CKE_H FBA_CMD19 R679 EV@10K/F_4
21,22 FBA_CMD[0..30]
TP38
+1.5V_GFX R222 EV@60.4/F_4 FBA_DEBUG F22
R221 EV@60.4/F_4 FBA_DEBUG1 J22
21,22 VMA_CLK0 21,22 VMA_CLK0# 21,22 VMA_CLK1 21,22 VMA_CLK1#
+1.05V_GFX L13 EV@PBY160808T-300Y-N +FB_PLLAVDD F16
C289 EV@22U/6.3V_6X
C266 EV@0.1U/10V_4X
C262 EV@0.1U/10V_4X
C241 EV@0.1U/10V_4X
FB_PLLAVDD P22
FB_DLLAVDD H22
FB_DLLAVDD GF119
FB_PLLAVDD GF117
FB_VREF_PROBE D23 FB_VREF_PROBE TP40
bga595-nvidia-n13p-gv2-s-a2 COMMON
2/14 FBA
VMA_DQ[63:0]
VMA_DQ[63:0] 21,22
FBVDDQ + FBVDD = 4.88A
+1.5V_GFX
Under GPU
Near GPU
C270 EV@0.1U/10V_4X
C268 EV@0.1U/10V_4X
C235 EV@0.1U/10V_4X
C264 EV@0.1U/10V_4X
C232 EV@1U/10V_6X
C260 EV@1U/10V_6X
C261 EV@4.7U/6.3V_6X
C252 EV@4.7U/6.3V_6X
C704 EV@10U/6.3V_6X
C729 EV@22U/6.3V_6X
U30D
12/14 FBVDDQ
FBVDDQ
FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ R223 EV@40.2/F_4
FB_CAL_PU_GND C24 FB_CAL_PU_GND R229 EV@42.2/F_4
FB_CALTERM_GND B25 FB_CAL_TERM_GND R248 EV@51.1/F_4
VMA_DM[7:0] 21,22
VMA_WDQS[7:0] 21,22
VMA_RDQS[7:0] 21,22
For Terminal
+1.5V_GFX
EV@0.1U/10V_4X C274
EV@0.1U/10V_4X C263
EV@0.1U/10V_4X C242
EV@0.1U/10V_4X C234
EV@0.1U/10V_4X C215
EV@0.1U/10V_4X C728
EV@0.1U/10V_4X C725
EV@0.1U/10V_4X C714
EV@0.1U/10V_4X C713
EV@0.1U/10V_4X C707
EV@0.1U/10V_4X C206
EV@0.1U/10V_4X C290
U30F
13/14 GND
GND
bga595-nvidia-n13p-gv2-s-a2 COMMON
FBA_CMD28 R692 R690 EV@100/F_4
FBA_CMD11 R243 R241 EV@100/F_4
FBA_CMD26 R683 R681 EV@100/F_4
FBA_CMD30 R196 R178 EV@100/F_4
FBA_CMD23 R213 R216 EV@100/F_4
FBA_CMD24 R218 R217 EV@100/F_4
FBA_CMD9 R713 R716 EV@100/F_4
FBA_CMD15 R723 R720 EV@100/F_4
FBA_CMD21 R685 R688 EV@100/F_4
FBA_CMD22 R693 R695 EV@100/F_4
FBA_CMD8 R226 R230 EV@100/F_4
FBA_CMD4 R711 R709 EV@100/F_4
FBA_CMD27 R212 R211 EV@100/F_4
FBA_CMD13 R236 R233 EV@100/F_4
FBA_CMD12 R703 R701 EV@100/F_4
FBA_CMD7 R224 R220 EV@100/F_4
FBA_CMD25 R706 R708 EV@100/F_4
FBA_CMD5 R232 R234 EV@100/F_4
FBA_CMD29 R204 R208 EV@100/F_4
FBA_CMD14 R698 R700 EV@100/F_4
FBA_CMD10 R724 R722 EV@100/F_4
FBA_CMD6 R245 R247 EV@100/F_4
Quanta Computer Inc.
PROJECT : BDBD
Size
Document Number
N14P_MEM/GND
Rev 2A
Date: Monday, December 17, 2012
Sheet 18 of 45

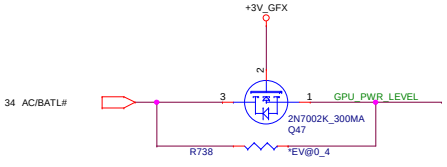

IFPAB
IFPE
IFPF
IFPC
IFPD
Quanta Computer Inc.
PROJECT : BDBD
Size
Document Number
N14P_DISPLAY
Rev
2A
Date: Monday, December 17, 2012
Sheet 19 of 45

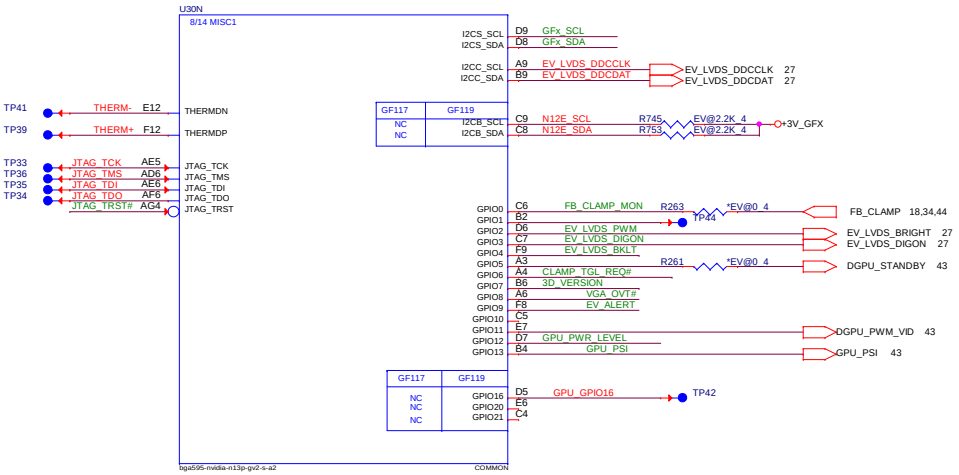


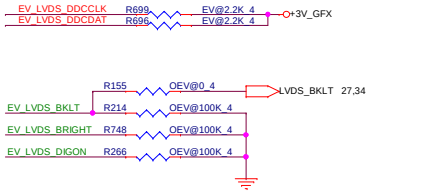
TP43



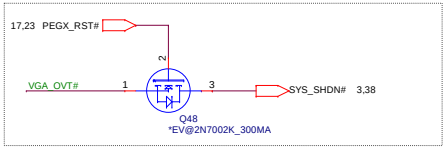


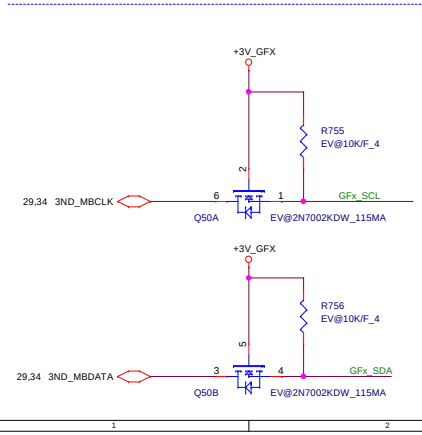


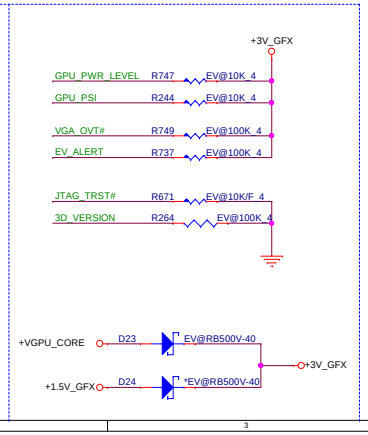


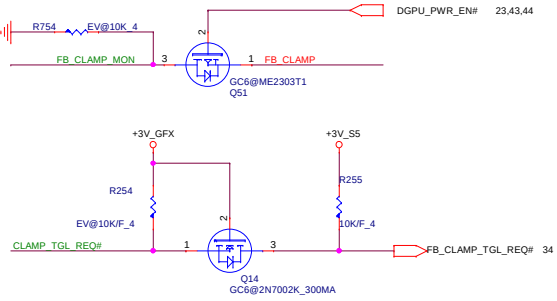


External LVDS control









Quanta Computer Inc.
PROJECT : BDBD

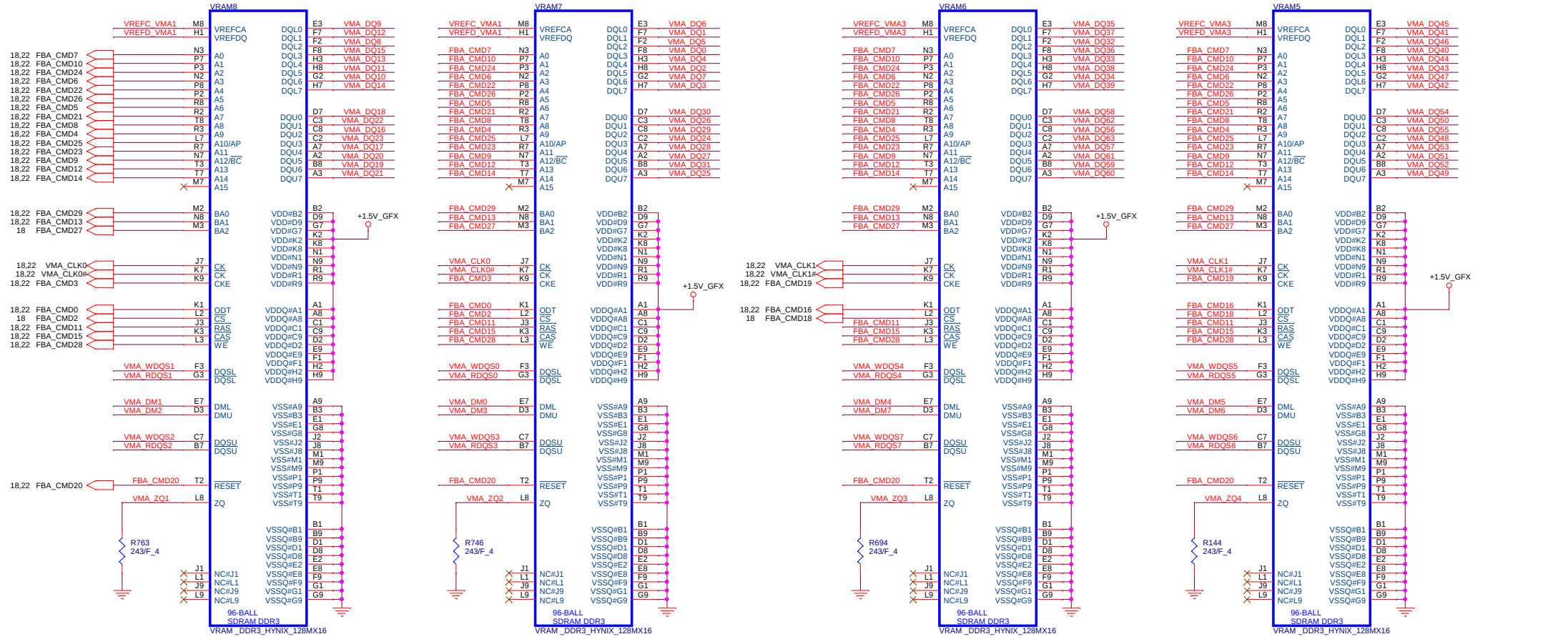
Size	Document Number	Rev
	N14P_GPIO	2A

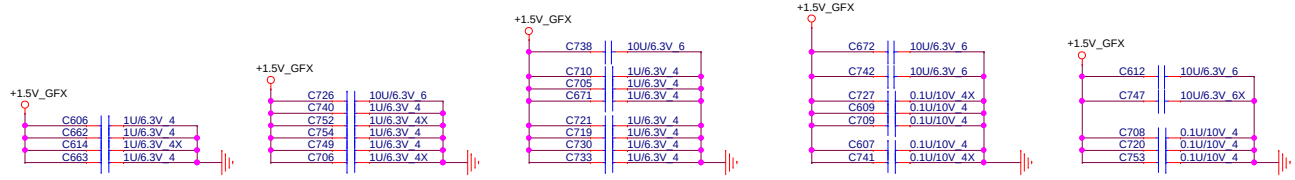
Date: Monday, December 17, 2012 Sheet 20 of 45

RANK 0

900MHz VRAM size:
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 128Mx16, P/N = AKD5MGWTW16

18,22 FBA_CMD[0..30]
18,22 VMA_DQ[63..0]
18,22 VMA_DM[7..0]
18,22 VMA_WDQS[7..0]
18,22 VMA_RDQS[7..0]





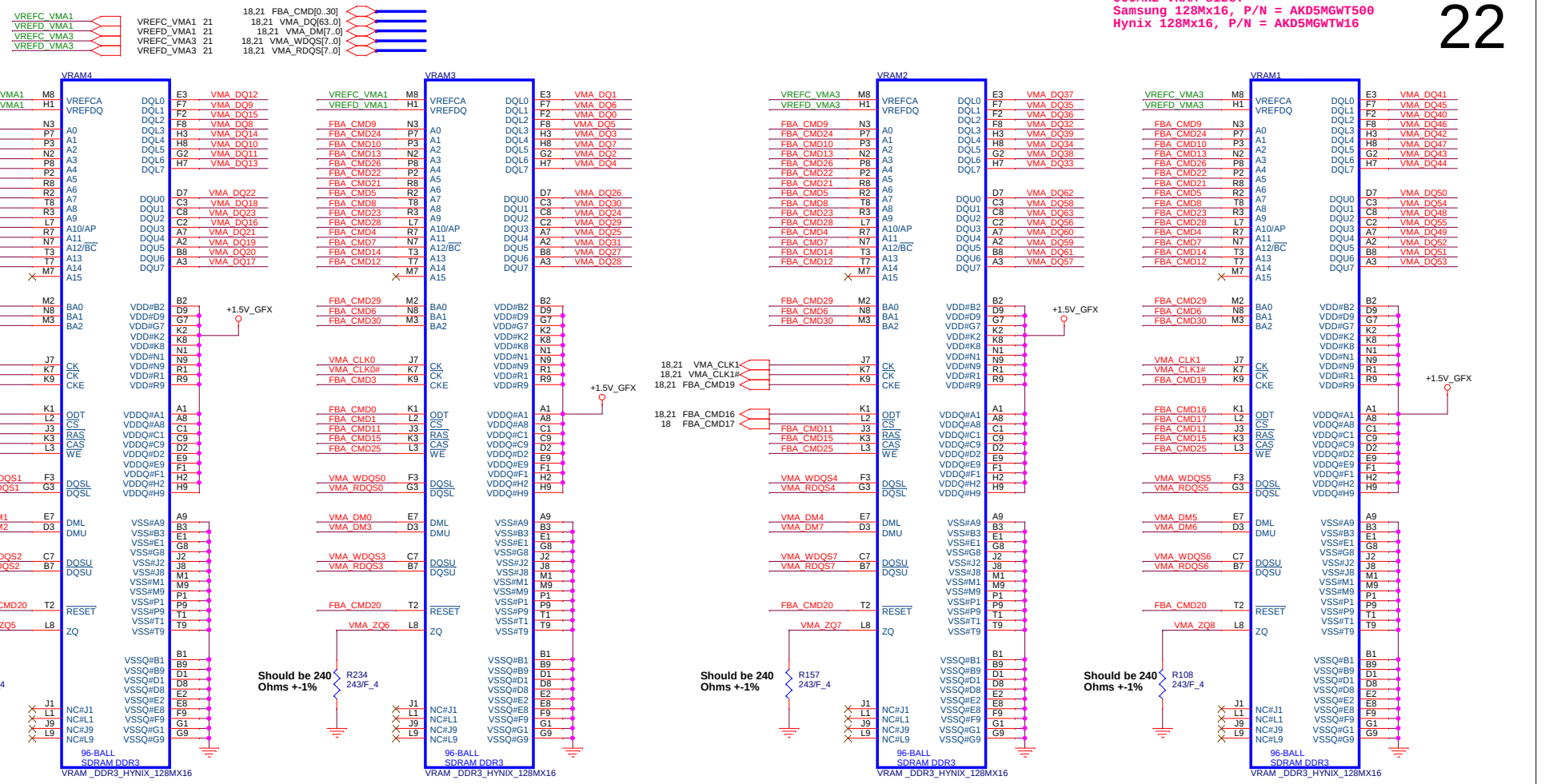
Quanta Computer Inc.
PROJECT : BDBD

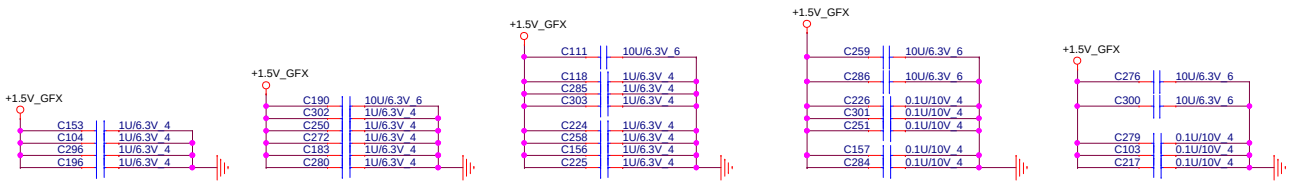
Size	Document Number	Rev
	N14P_VRAM RANK0	2A

Date: Monday, December 17, 2012 Sheet 21 of 45

RANK 1

900MHz VRAM size:
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 128Mx16, P/N = AKD5MGWTW16

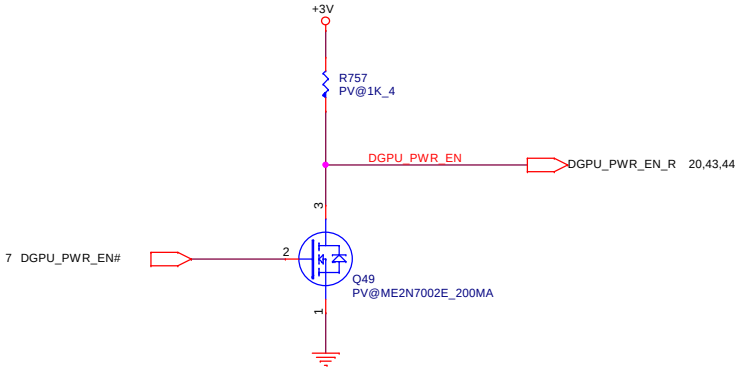


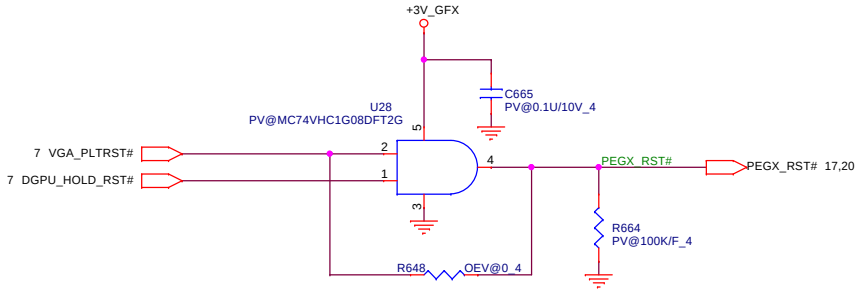


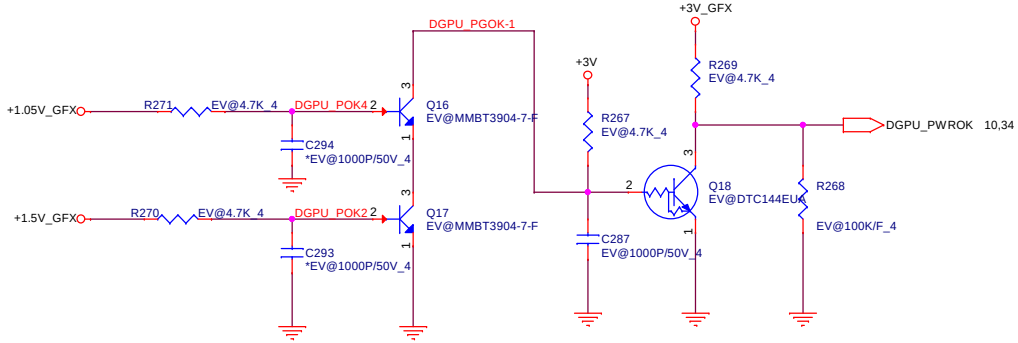
Quanta Computer Inc.
PROJECT : BDBD

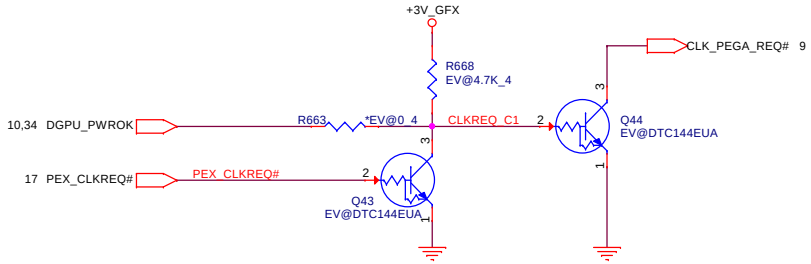
Size	Document Number	Rev
	N14P_VRAM RANK1	2A

Date: Monday, December 17, 2012 Sheet 22 of 45







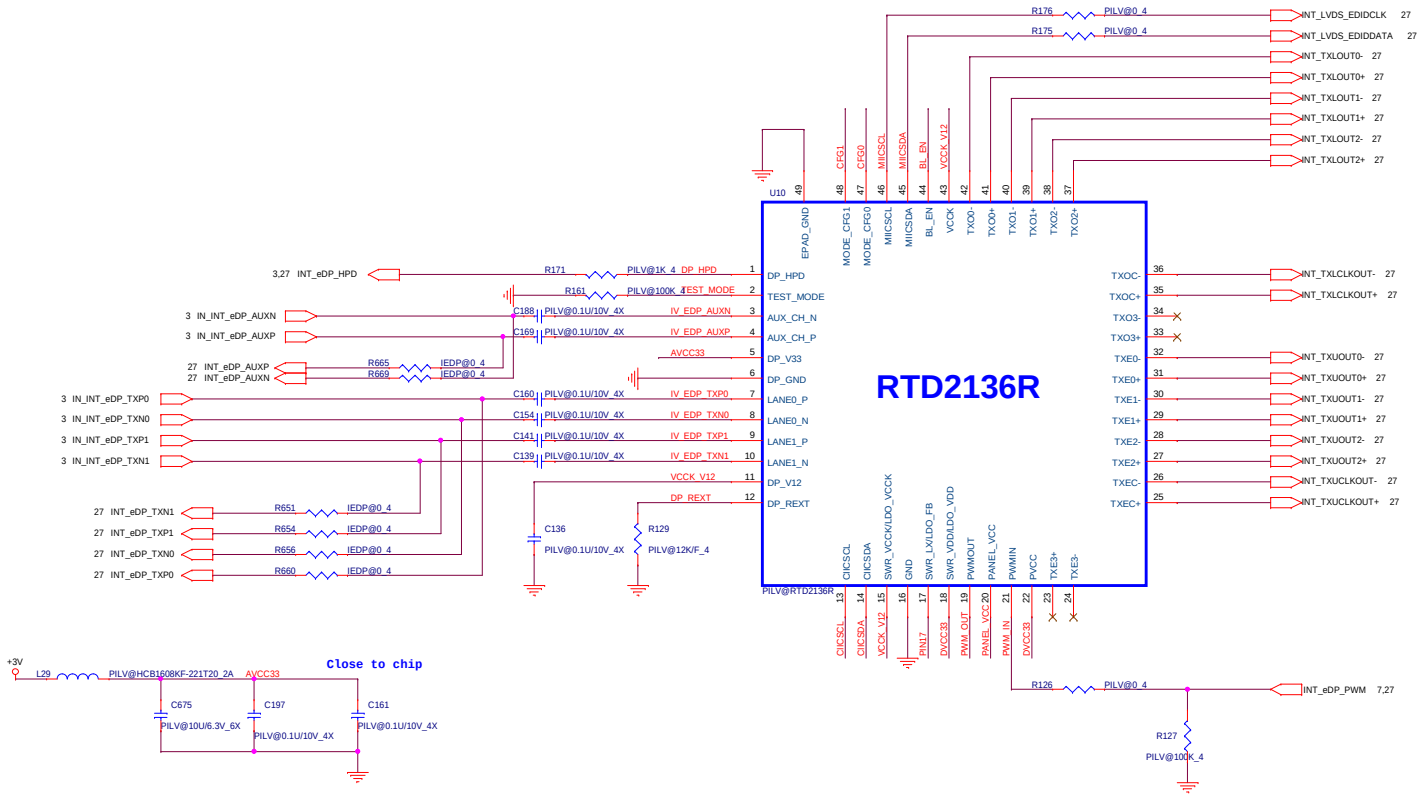


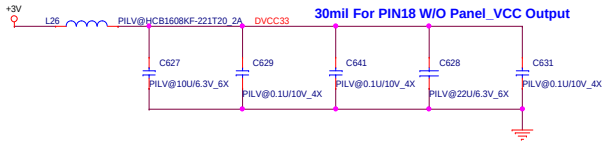
Quanta Computer Inc.

PROJECT : BDBD

Size	Document Number	Rev
	Blank	2A

Date: Monday, December 17, 2012 Sheet 23 of 45

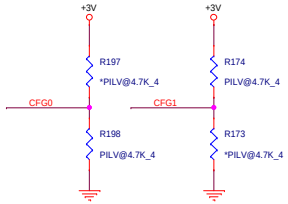




Mode Configure Table(Power On Latch)

		CFG0	
		0	1
CFG1	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

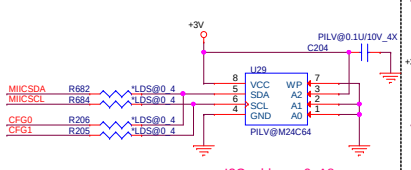
ROM ONLY Mode : CFG0 4.7K pull low, CFG1 4.7K pull high
EP Mode : CFG0 4.7K pull high, CFG1 4.7K pull low
EEPROM Mode : CFG0 4.7K pull high, CFG1 4.7K pull high



EEPROM Mode

In EEPROM mode, an additional EEPROM is needed.
EEPROM should configure with following condition.

1- EEPROM with a size 8K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8

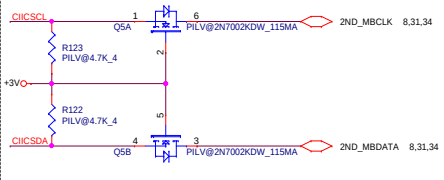


I2C address=0xA8

EP Mode

External device connect to DP2LVDS by
Pin13/Pin14, I2C protocol is used

Address=0x94&0x6A

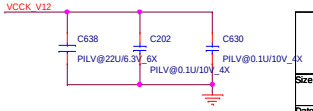


Dual Mode Regulator Configuration

	2.2-uH(L6)	0 Olm(R31)
SWR	Connect	NC
LDO	NC	Connect

SWR MODE

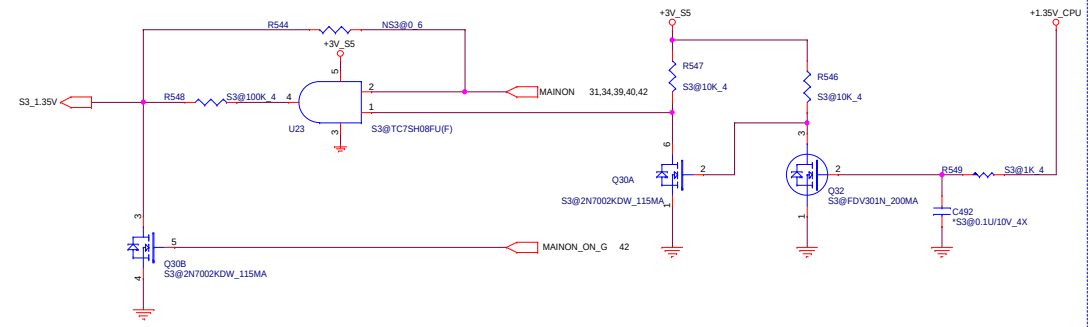
LDO MODE



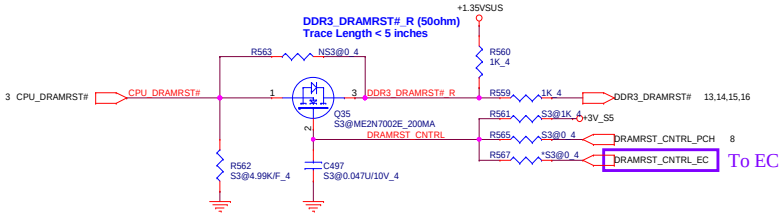
Quanta Computer Inc.
PROJECT : BDBD

Size	Document Number	Rev
	Thames_M2/ Baco	2A
Date: Monday, December 17, 2012	Sheet 24 of 45	

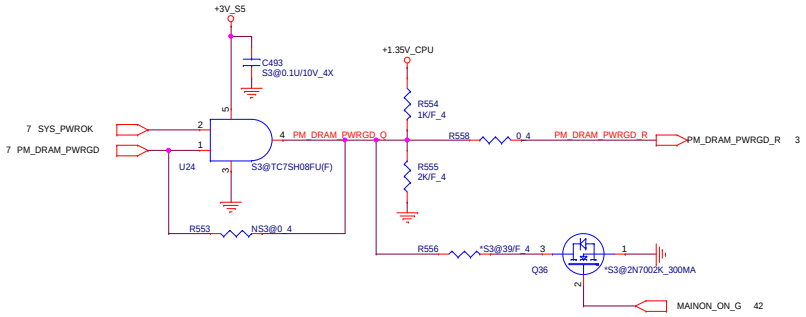
For S3 power Reduction Sequence S3P/NS3P/CPU



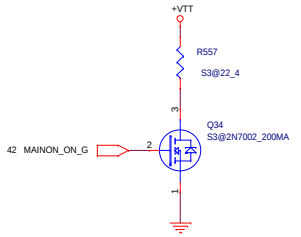
SM_DRAMRST# Topology S3P/NS3P/CPU



S3 power Reduction (SM_DRAMPWROK) S3P/NS3P/CPU

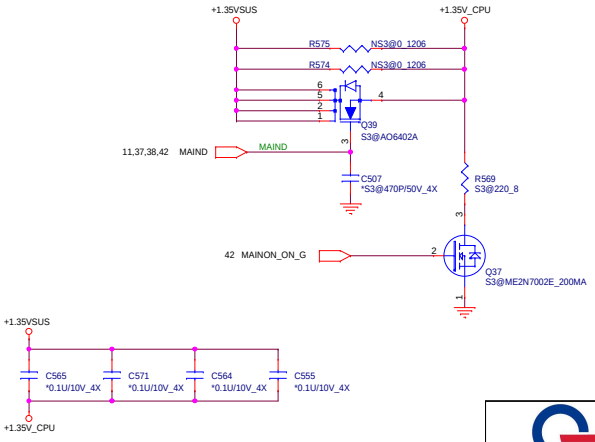


For S3 power Reduction VTT discharge S3P/NS3P/CPU



CPU SM_VREF S3P/NS3P/CPU

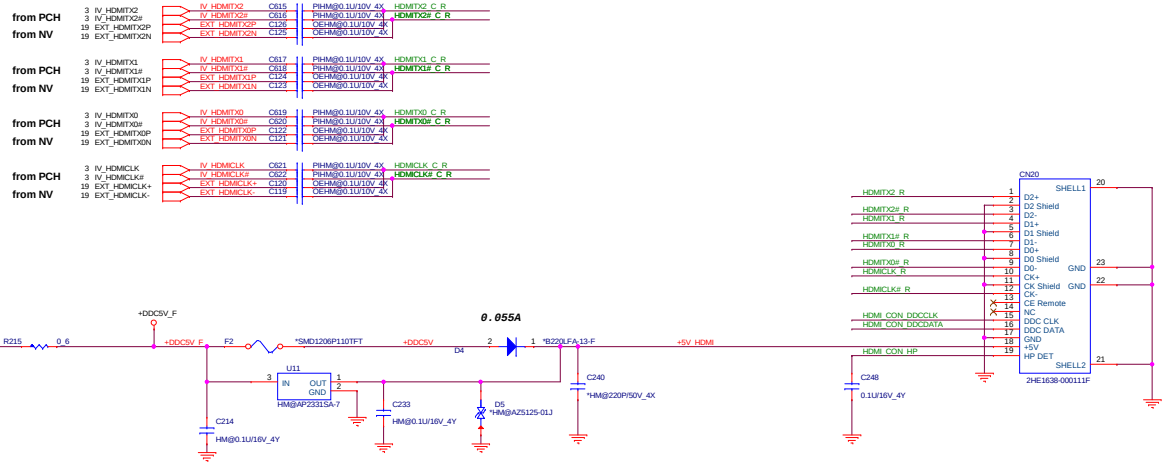
S3 power Reduction (CPU Power) S3P/NS3P/CPU



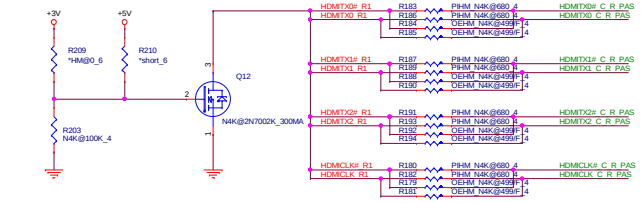
Quanta Computer Inc.
PROJECT : BDBD

Size	Document Number	Rev
	Haswell 3/5 (DDI/eDP)	2A
Date: Monday, December 17, 2012	Sheet 25 of 45	

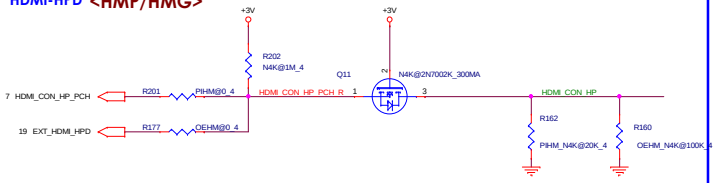
HDMI Conn <HDM>



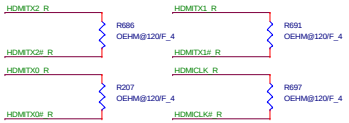
HDMI-passive level shift <HMP/HMG>



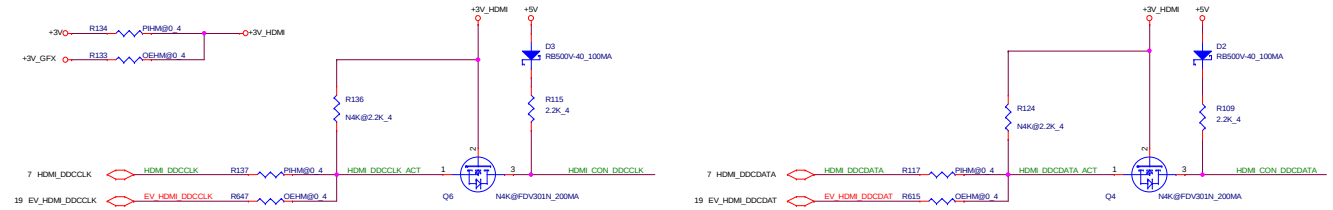
HDMI-HPD <HMP/HMG>

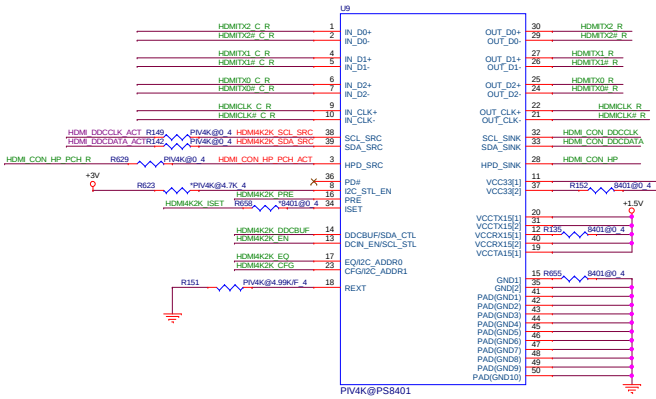


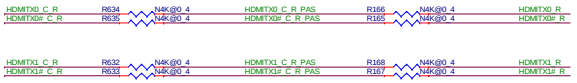
FOR EMI <EMC>

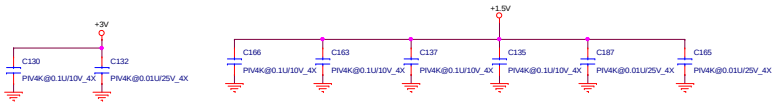


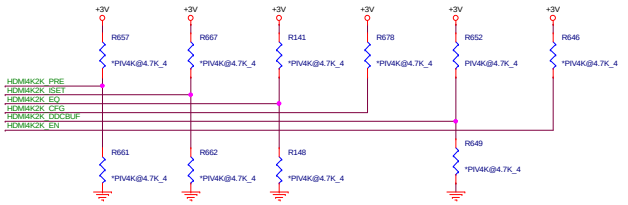
HDMI-SMBus <HDM>











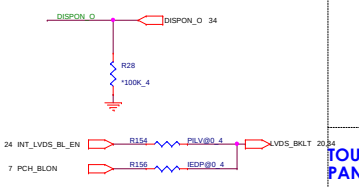
	Pre	ISET	EQ	CFG	DDCBUF	DCIN_EN
NC(Low)	0 dB	default	12.4 dB	HDMI ID disable	default	default,AC coupling input
1(High)	1.6 dB	+13%	4.3 dB	HDMI ID enable	active DDC buffer with default threshold	DC coupling input
M	2.5 dB	-13%	8.6 dB	N/A	active DDC buffer without internal pull up resistor	N/A

Pre	Output pre-emphasis setting
ISET	TMDS output swing adjustment
EQ	Receiver equalization setting
CFG	Configuration pin
DDCBUF	enable active DDC buffer
DCIN_EN	DC coupling enable

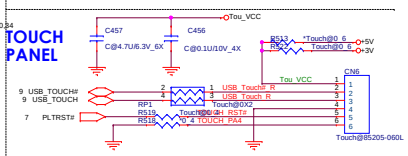
Pin	PS8401A	PS8201A
12	VDDRX	NC
15	GND	NC
34	ISET	NC
37	VDD33	NC

Quanta Computer Inc.
PROJECT : BDBD
Size | Document Number: HDMI CONN/CEC | Rev: 2A
Date: Monday, December 17, 2012 | Sheet 26 of 45

Panel backlight control LDS



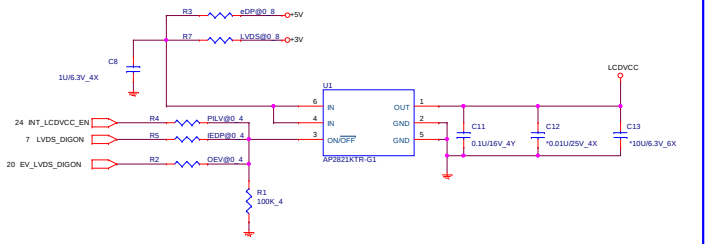
TOUCH PANEL



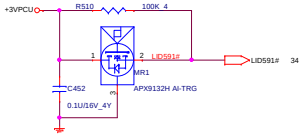
LCD POWER SWITCH

INT_LVDS PWR

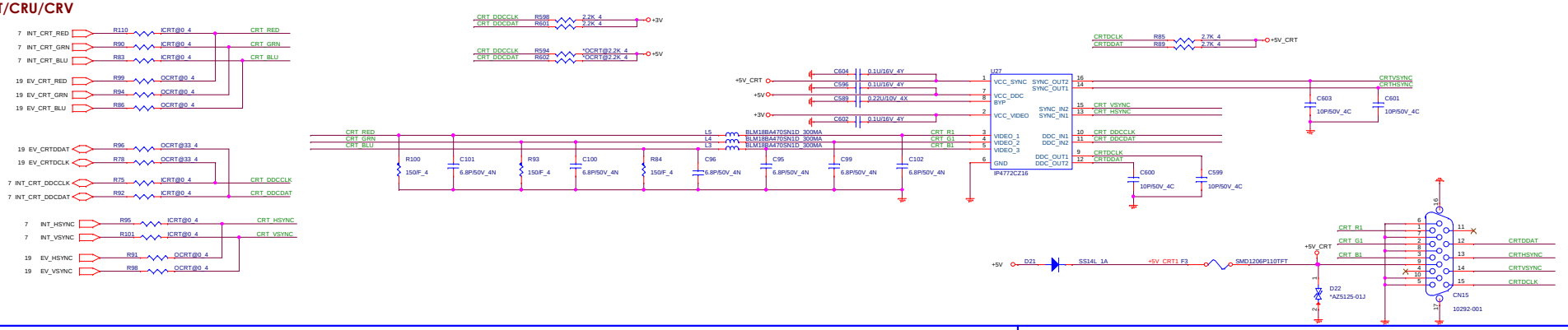
80 mil



HALL Sensor HSR

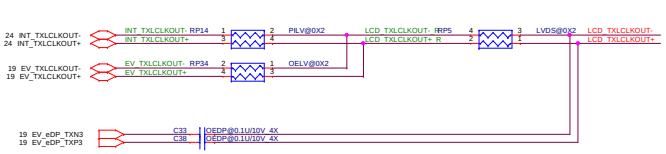


CRT CRT/CRU/CRV

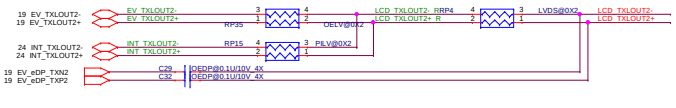


LCD Panel Module <LDS>

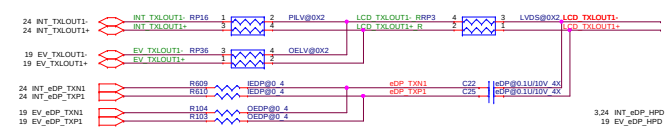
Lane 3



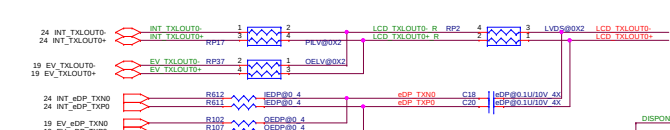
Lane 2



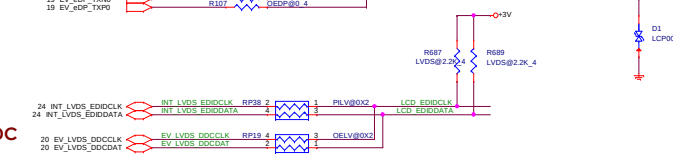
Lane 1

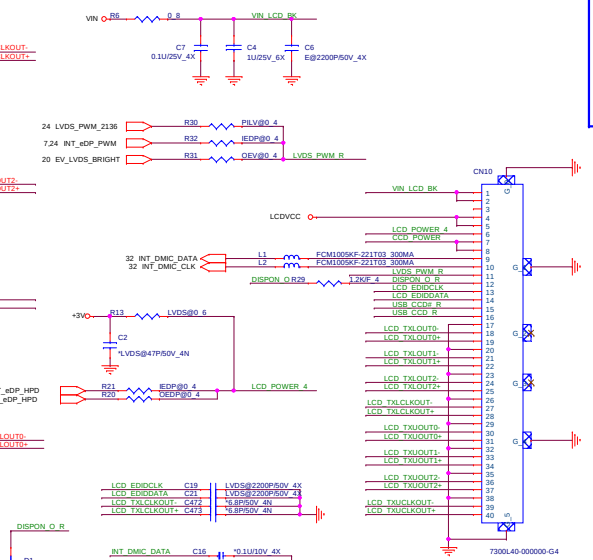


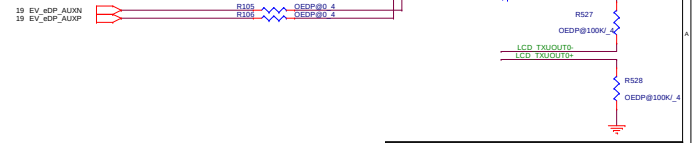
Lane 0



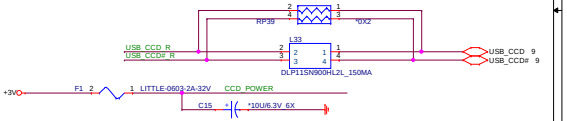
EDID DDC







CCD

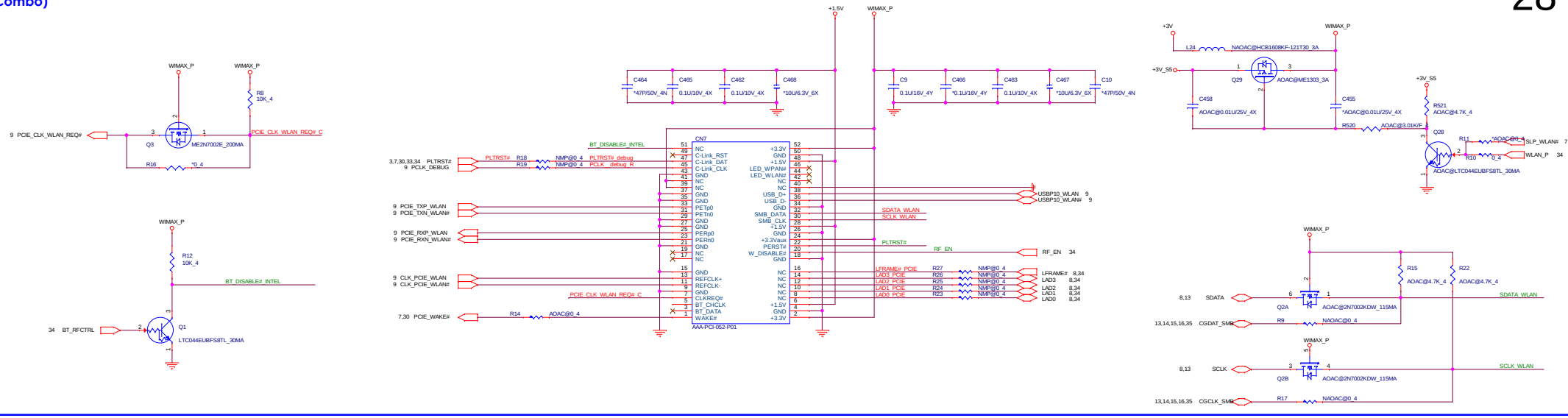


Quanta Computer Inc.
PROJECT : BDBD

Size	Document Number	Rev
	LCD/LED Panel/CCD	2A
Date: Monday, December 17, 2012	Sheet 27 of 45	

MINI Card Slot#1(WiFi / Wimax / Combo)

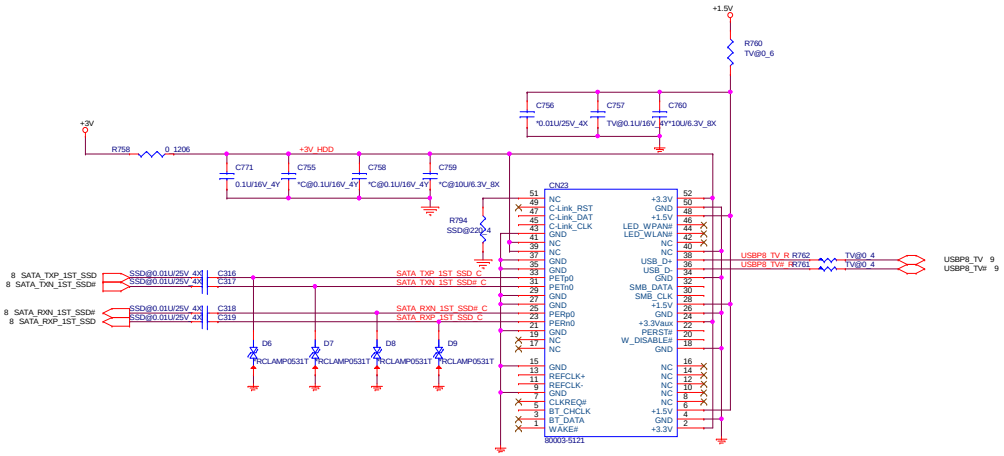
MNW/DEG



TV Tuner / MSATA

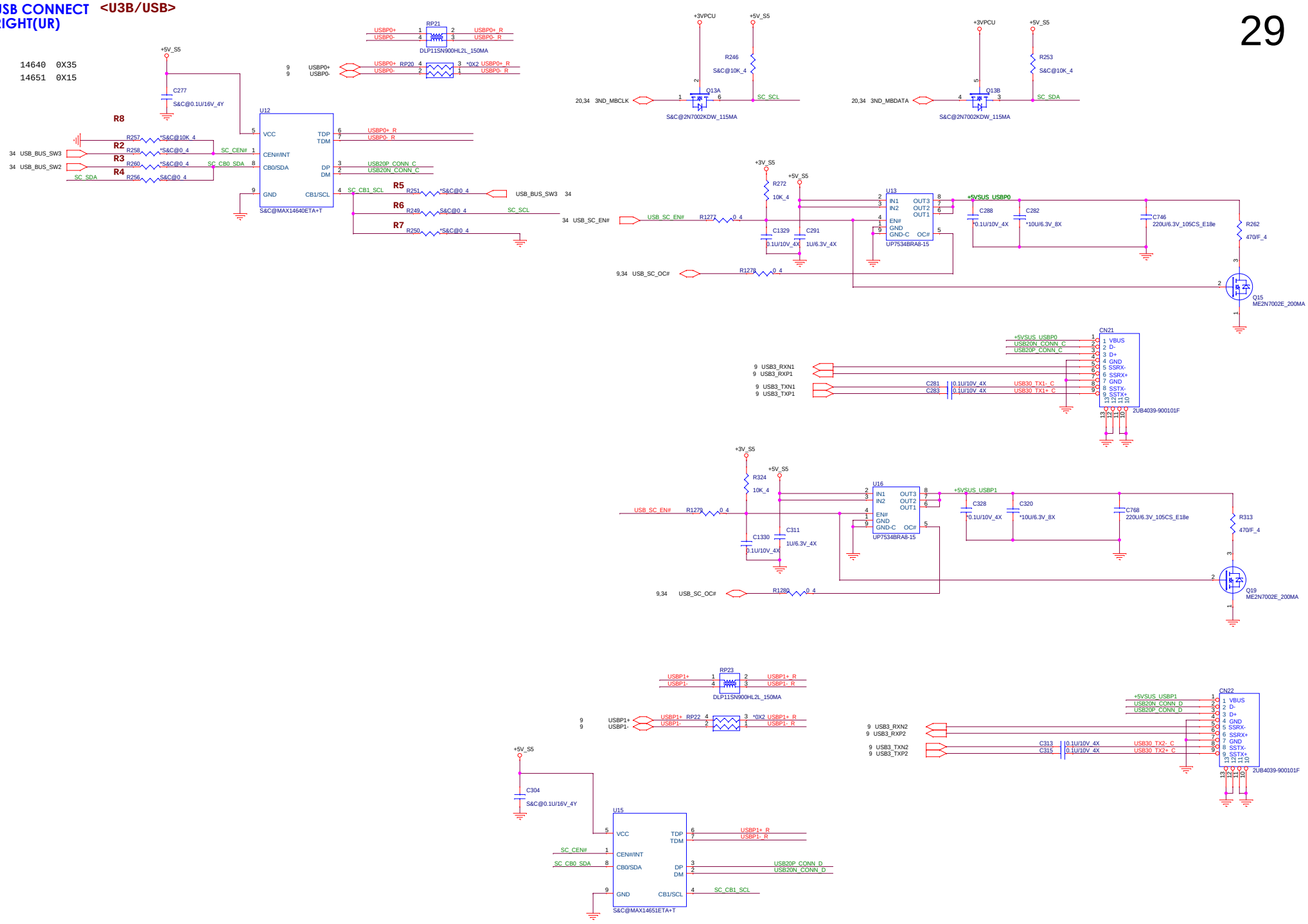
<SSD>

TV Tuner: 1.5V@240mA 3.3V@470mA



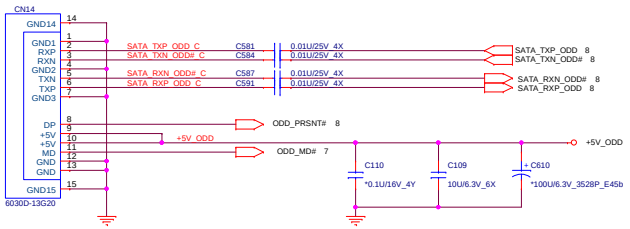
USB CONNECT RIGHT(UR) <U3B/USB>

14640 0X35
14651 0X15

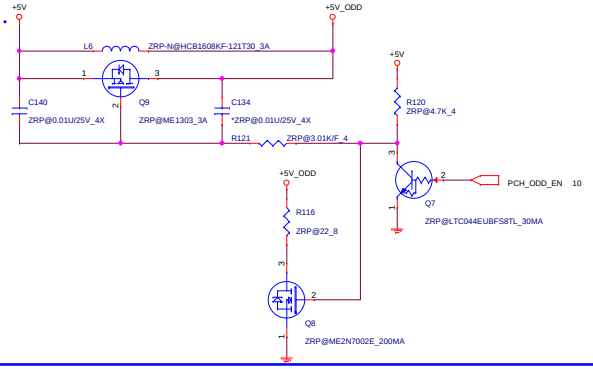


Quanta Computer Inc.		
PROJECT : BDBD		
Size	Document Number	Rev 2A
	USB3 Redriver/S&C(Right side)	
Date: Monday, December 17, 2012	Sheet 29 of 45	

SATA ODD

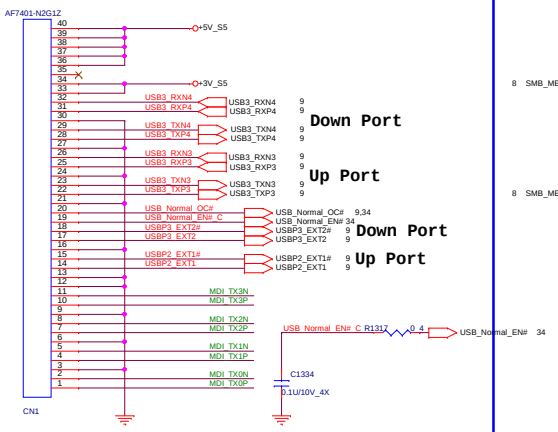


ODD Zero power . (Only for Intel)

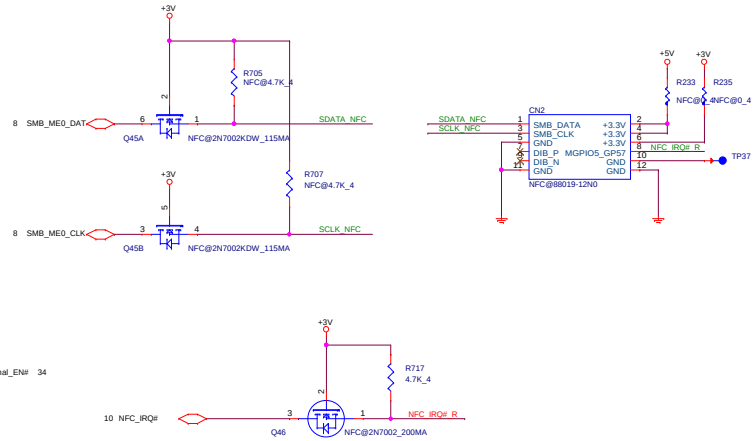


Atheros Lan/USB3 CONN

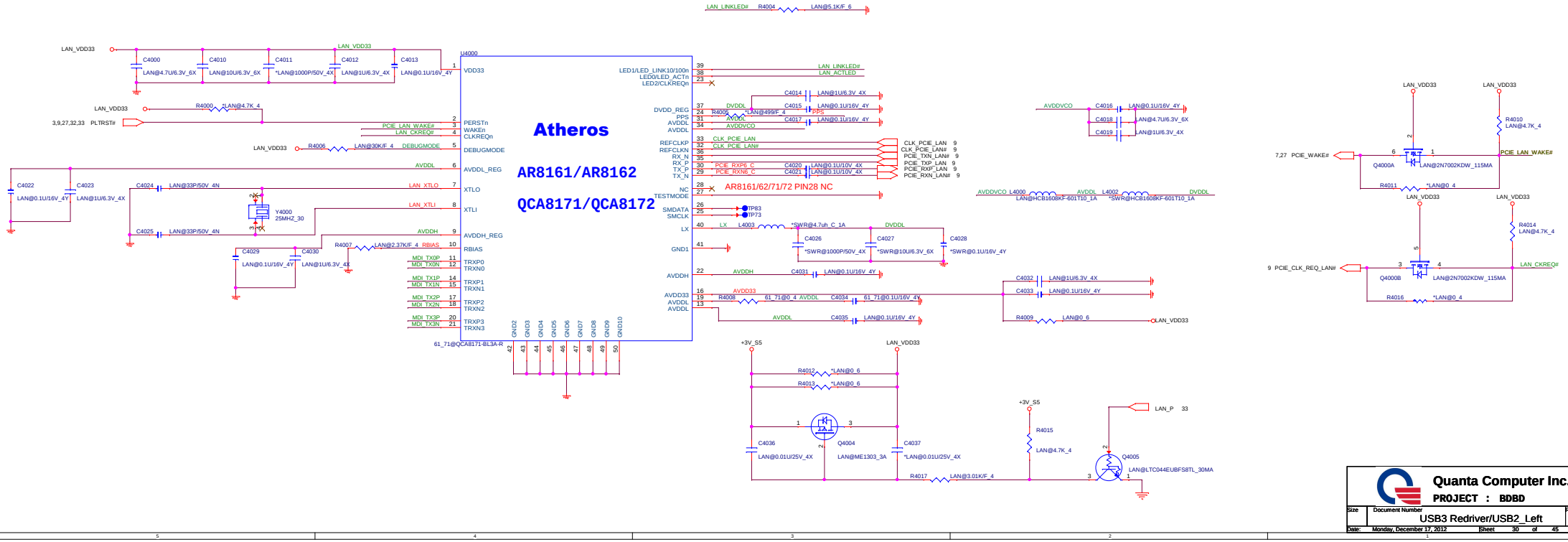
<LAN/LN1.LNG>



NFC Connector



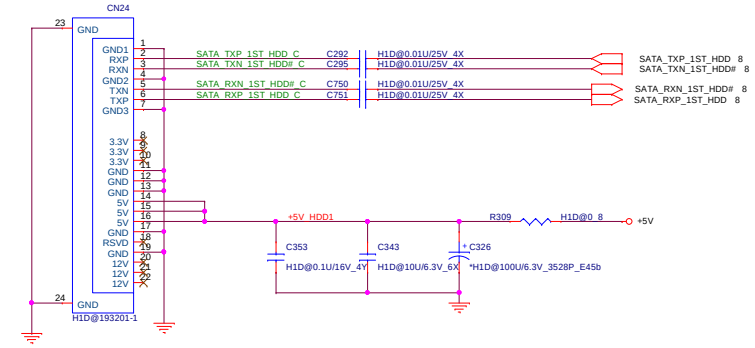
Atheros AR8161/AR8162 QCA8171/QCA8172



Quanta Computer Inc.
PROJECT : BDBD

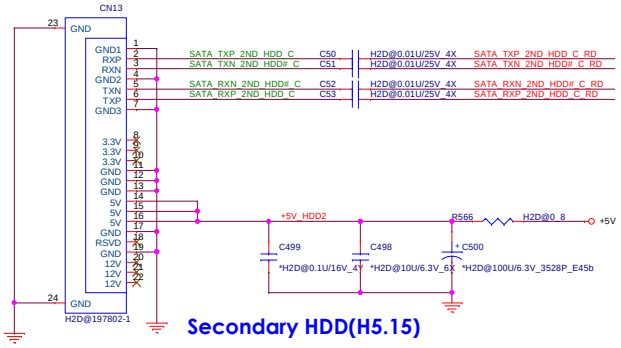
Size	Document Number	Rev
	USB3 Redriver/USB2_Left	2A
Date: Monday, December 17, 2012	Sheet 30 of 45	

SATA HDD1



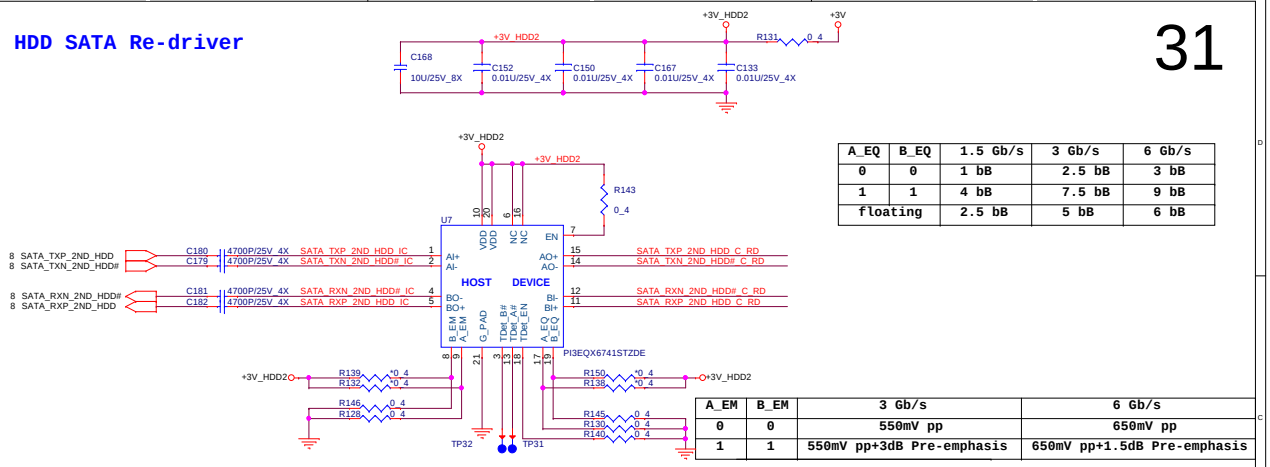
Primary HDD(H2.75)

SATA HDD2



Secondary HDD(H5.15)

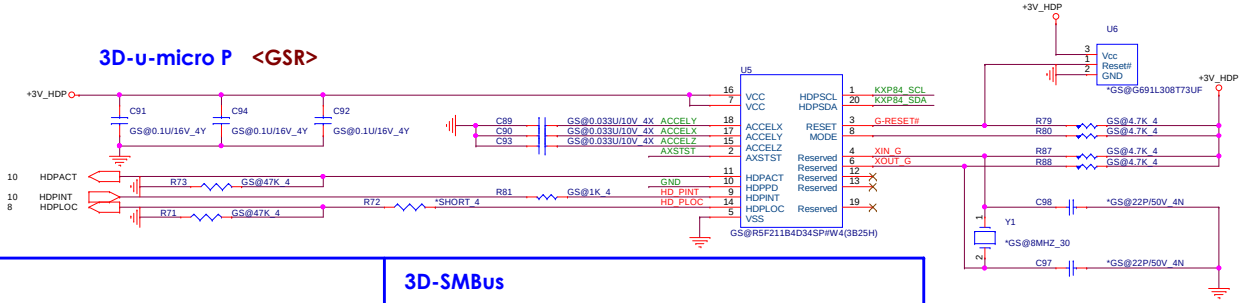
2nd HDD SATA Re-driver



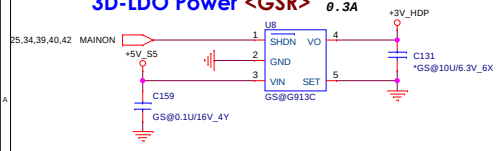
A_EQ	B_EQ	1.5 Gb/s	3 Gb/s	6 Gb/s
0	0	1 bB	2.5 bB	3 bB
1	1	4 bB	7.5 bB	9 bB
floating		2.5 bB	5 bB	6 bB

A_EM	B_EM	3 Gb/s	6 Gb/s
0	0	550mV pp	650mV pp
1	1	550mV pp+3dB Pre-emphasis	650mV pp+1.5dB Pre-emphasis

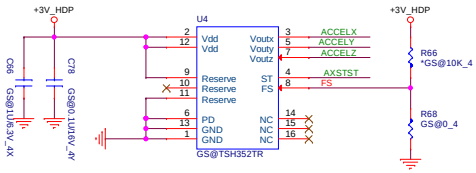
3D-u-micro P <GSR>



3D-LDO Power <GSR> 0.3A



3D-Sensor IC <GSR>



FS (Full Scale) selection

FS	0	1
	2g Full-Scale	6g Full-Scale

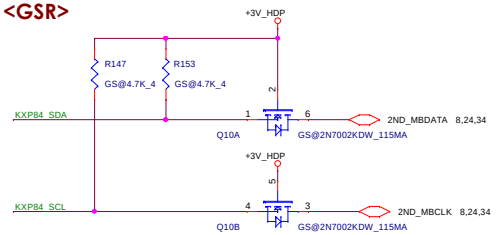
PD (Power Down) selection

PD	0	1
	Normal Mode	Power-down mode

HDPPD selection

HDPPD	0	1
	Normal Mode	Power-down mode

3D-SMBus <GSR>



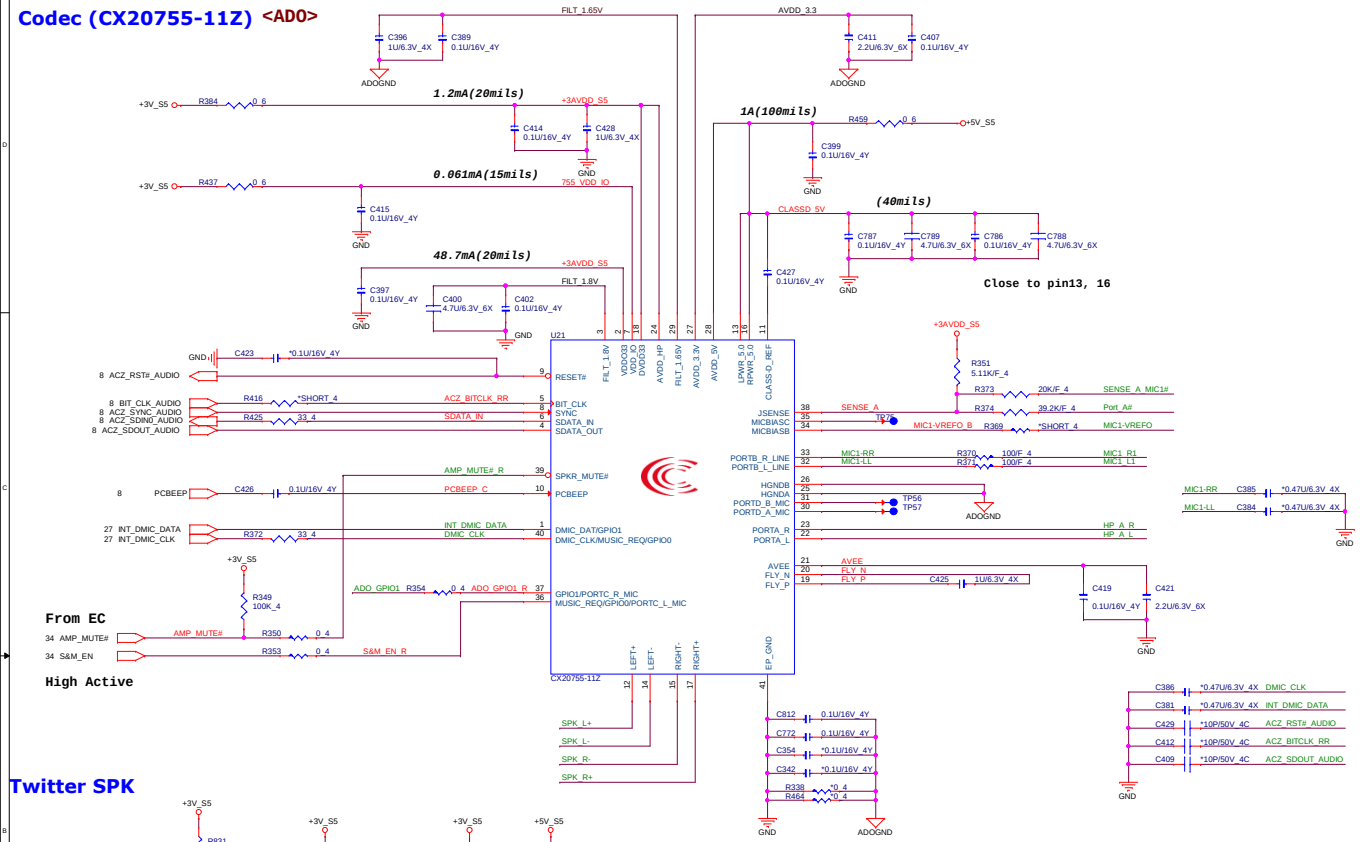
Quanta Computer Inc.

PROJECT : BDBD

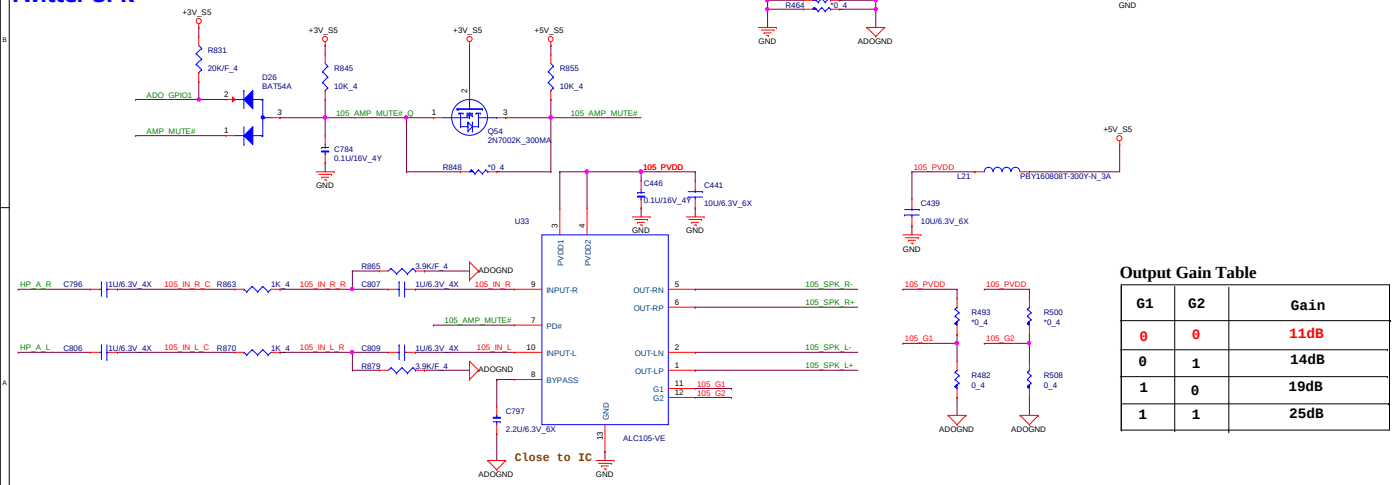
Size	Document Number	Rev
	HDD/ODD	2A

Date: Monday, December 17, 2012 Sheet 31 of 45

Codec (CX20755-11Z) <ADO>



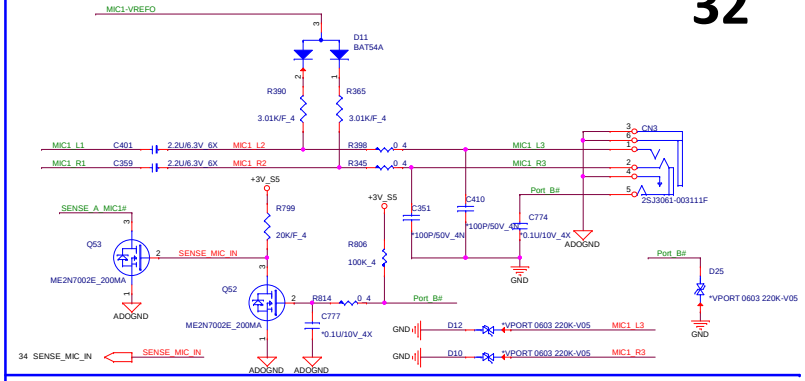
Twitter SPK



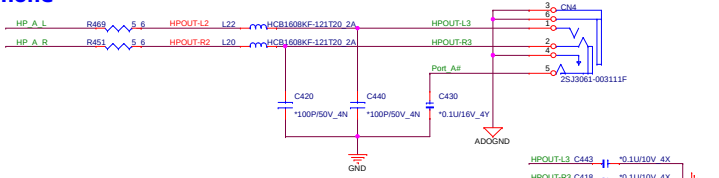
Output Gain Table

G1	G2	Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

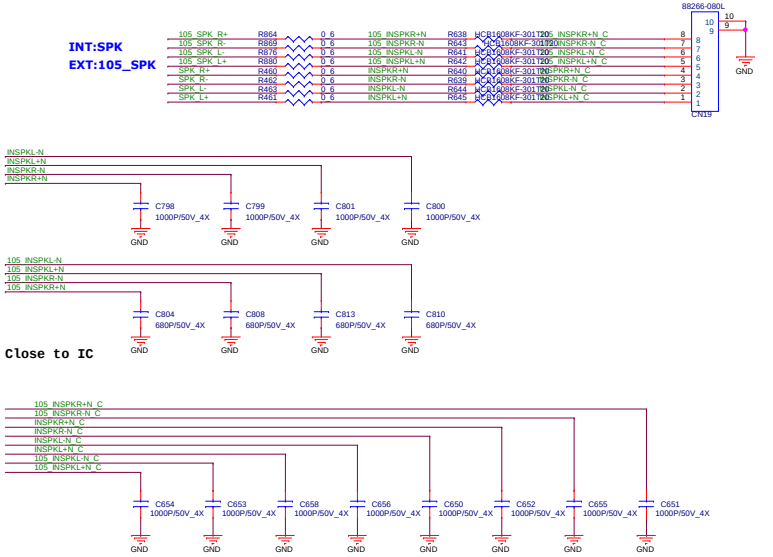
External MIC



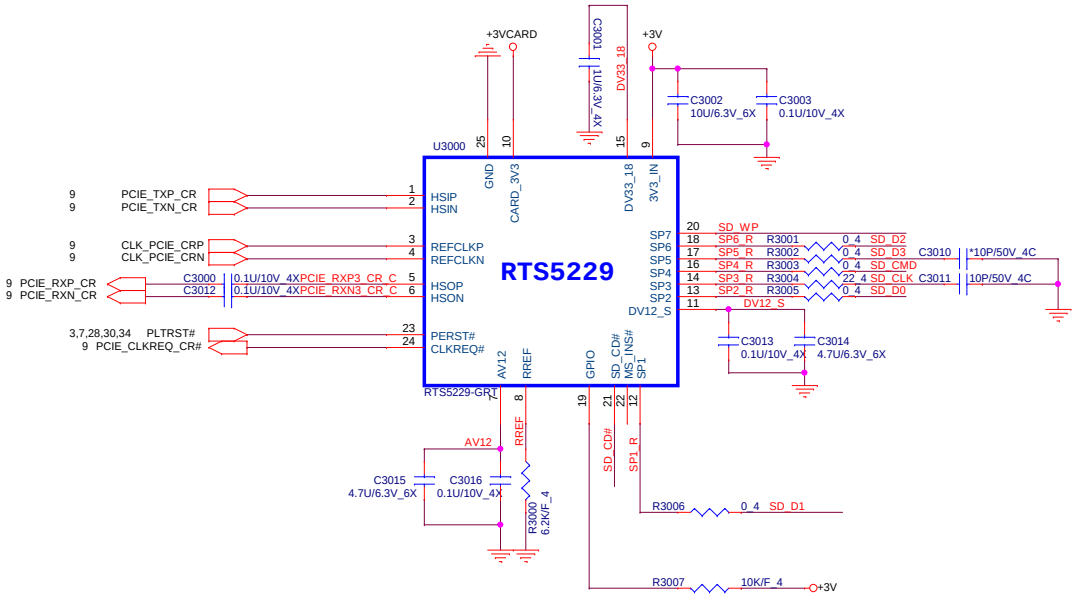
Headphone <ADO>

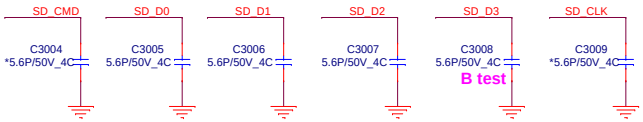


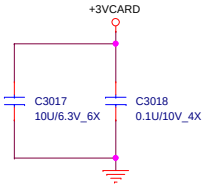
4 Speakers <ADO>



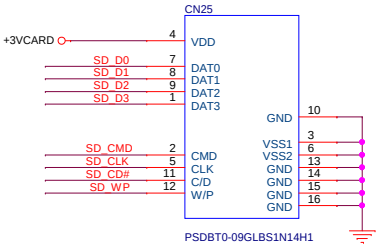
Quanta Computer Inc.
PROJECT : BDBD
Size | Document Number: Audio Codec (CX20755) | Rev 2A
Date: Monday, December 17, 2012 | Sheet 32 of 45







SD / MMC CARD READER



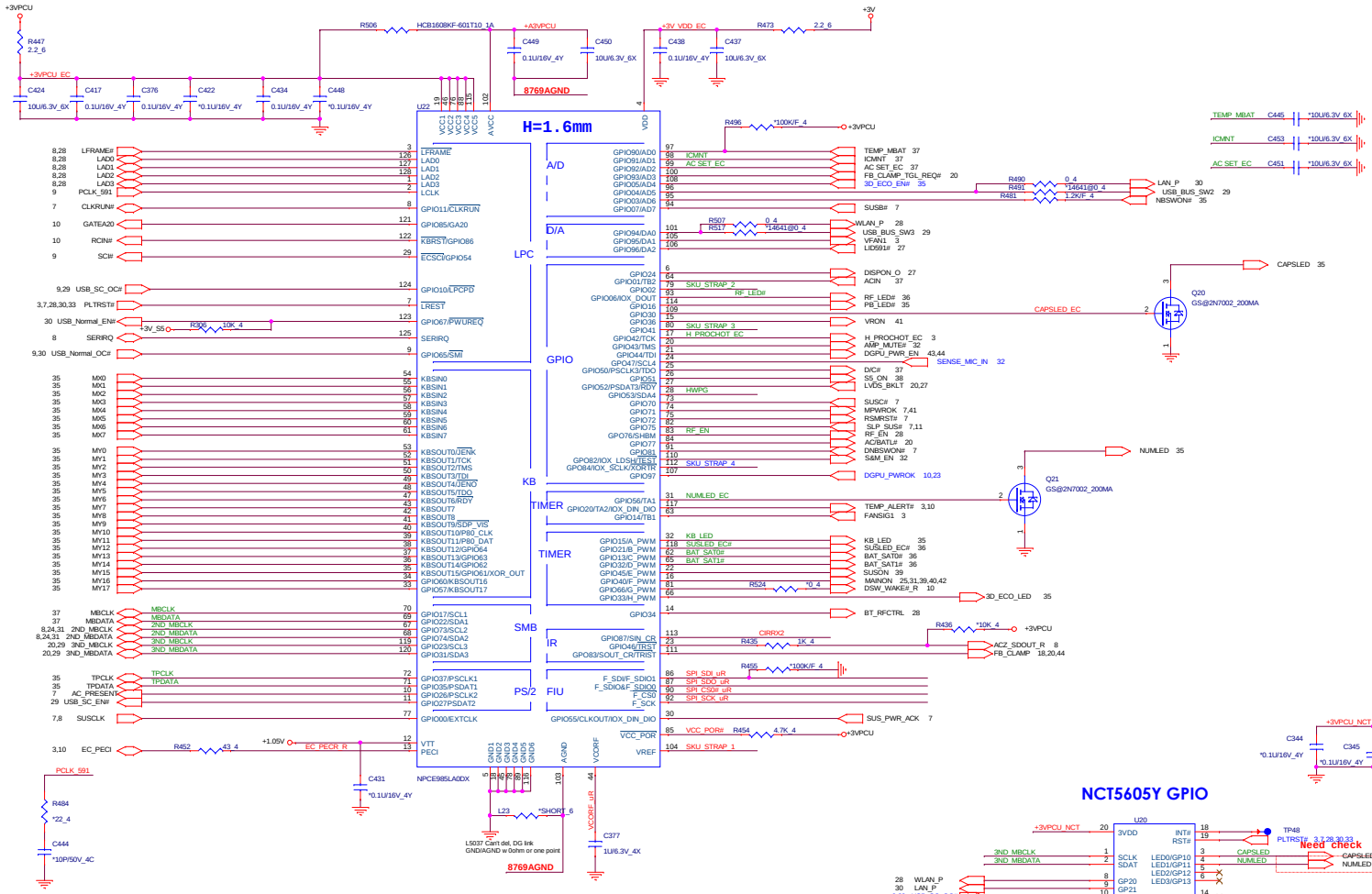
Quanta Computer Inc.

PROJECT : BDBD

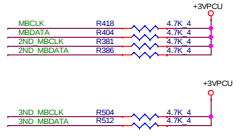
Size	Document Number	Rev
	Card Reader(AU6437)	2A

Date: Monday, December 17, 2012 Sheet 33 of 45

EC<KBC>

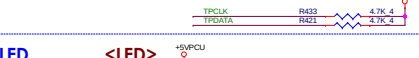


SM BUS PU/Address <KBC>

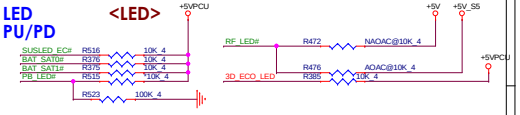


SMBUS	Devices	Address
1	Battery(A)	
2	PCH(S5)	
	G-sensor(S0)	
	IDROM(A)	
	EDP2LVDS IC	94H or 6AH
3	VGA Thermal(A or S0)	98H
	Extend GPIO	
	S&C IC 14640 Up Port S&C IC 14651 Down Port	35H 15H

TP <KBC>

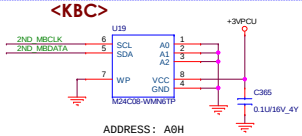


LED PU/PD <LED>



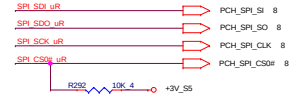
INTERNAL KEYBOARD STRIP SET <KBC>

ID EEPROM <KBC>

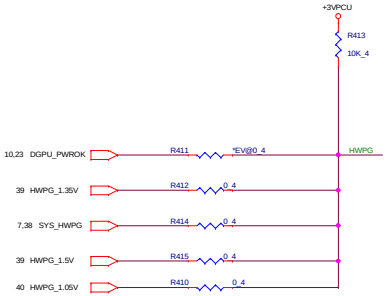


ADDRESS: A0H

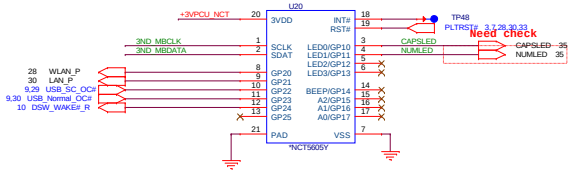
SPI FLASH <KBC>



HWPG circuit <KBC>

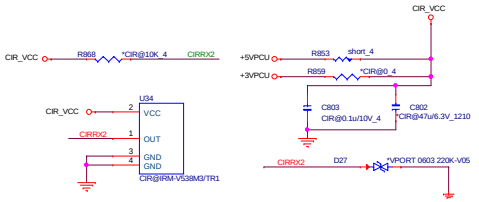


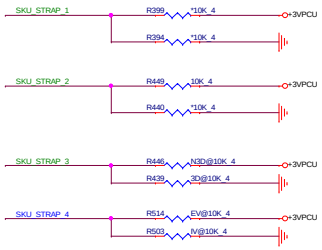
NCT5605Y GPIO



Power Button <KBC>

CIR



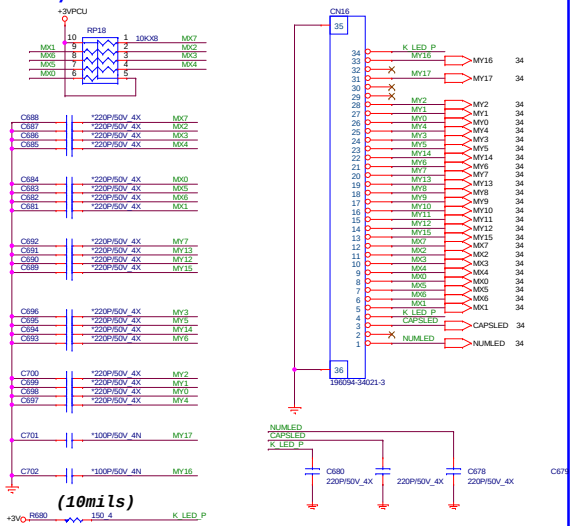


MS Strap	SKU_STRAP_1	SKU_STRAP_2	SKU_STRAP_3	SKU_STRAP_4
17"P	0			
17"G	1			
Chief River		0		
Shark Bay		1		
W/ 3D			0	
W/O 3D			1	
UMA				0
Discrete(Optmius)				1

Quanta Computer Inc.
PROJECT : BDBD

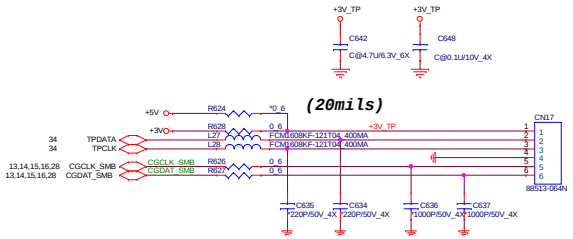
Size	Document Number	Rev
	EC-NPCE885L	2A
Date: Monday, December 17, 2012	Sheet 34 of 45	

INT KeyBoard <KBC>



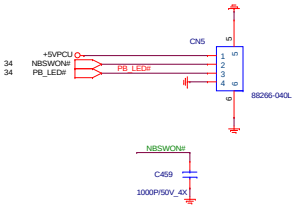
TP board <TPD>

Touch Pad Connector <TPD> <EMI>



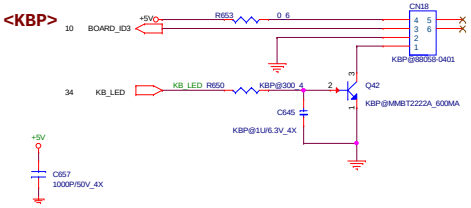
Power board w LED <PSW>

Power Botton Connector <PSW>

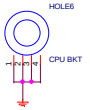


K/B LED power

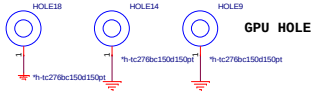
<KBP>



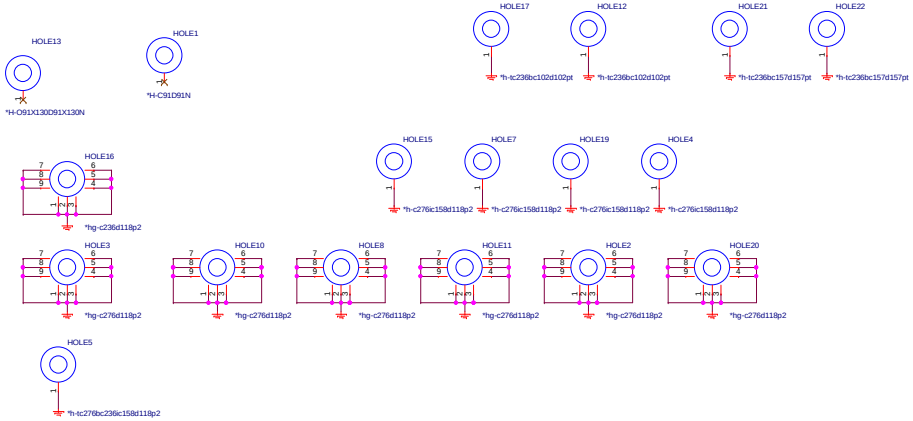
CPU BKT INTEL-CPU-BKT2



GPU



HOLE



Quanta Computer Inc.

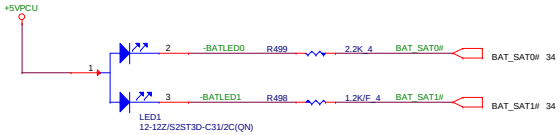
PROJECT : BDBD

Size	Document Number	Rev
	KB/TP&TP/PB/FL/LEB/MMB/B-CAS	2A

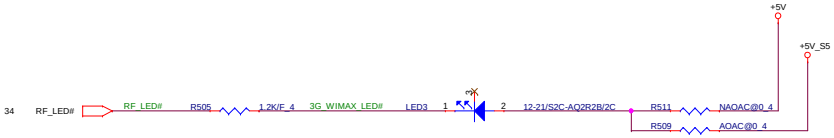
Date: Monday, December 17, 2012 Sheet 35 of 45

LED

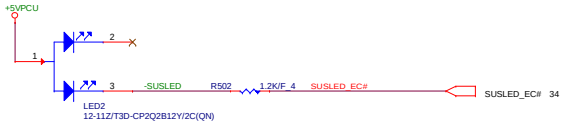
BATERRY



RF LED LED

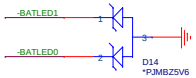


POWER LED

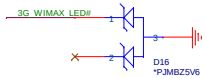


ESD Protect LED

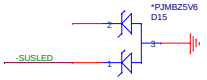
FOR BATTERY LED



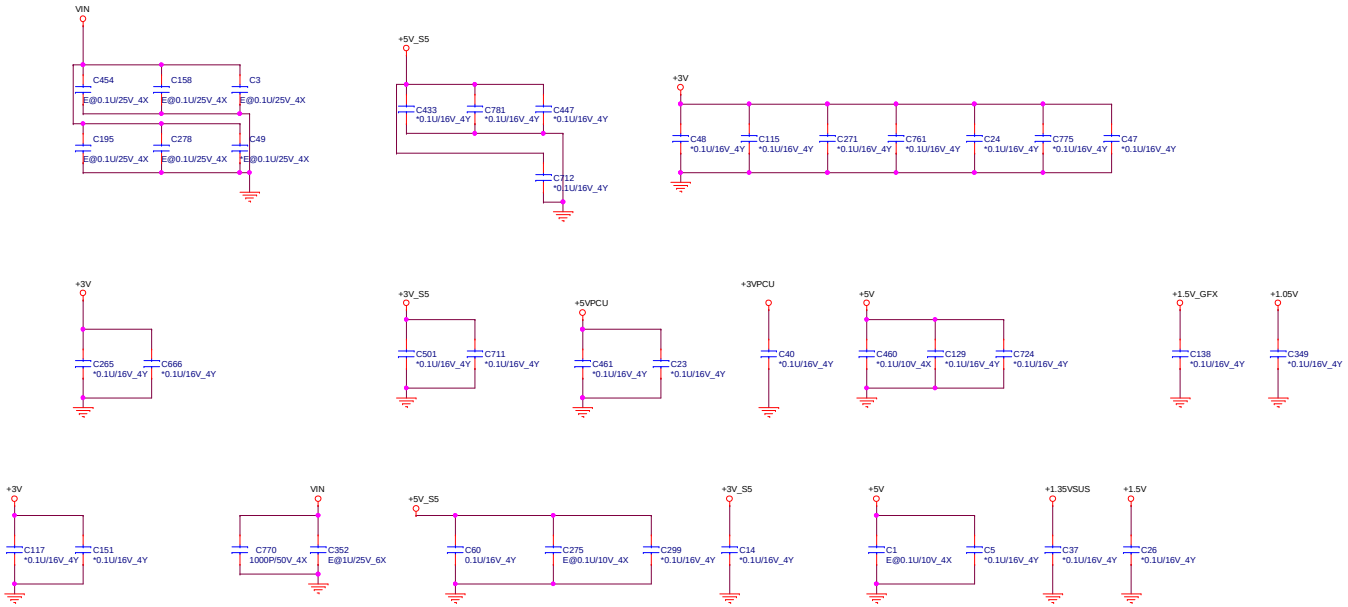
FOR W-LAN LED



FOR Power LED



EMI

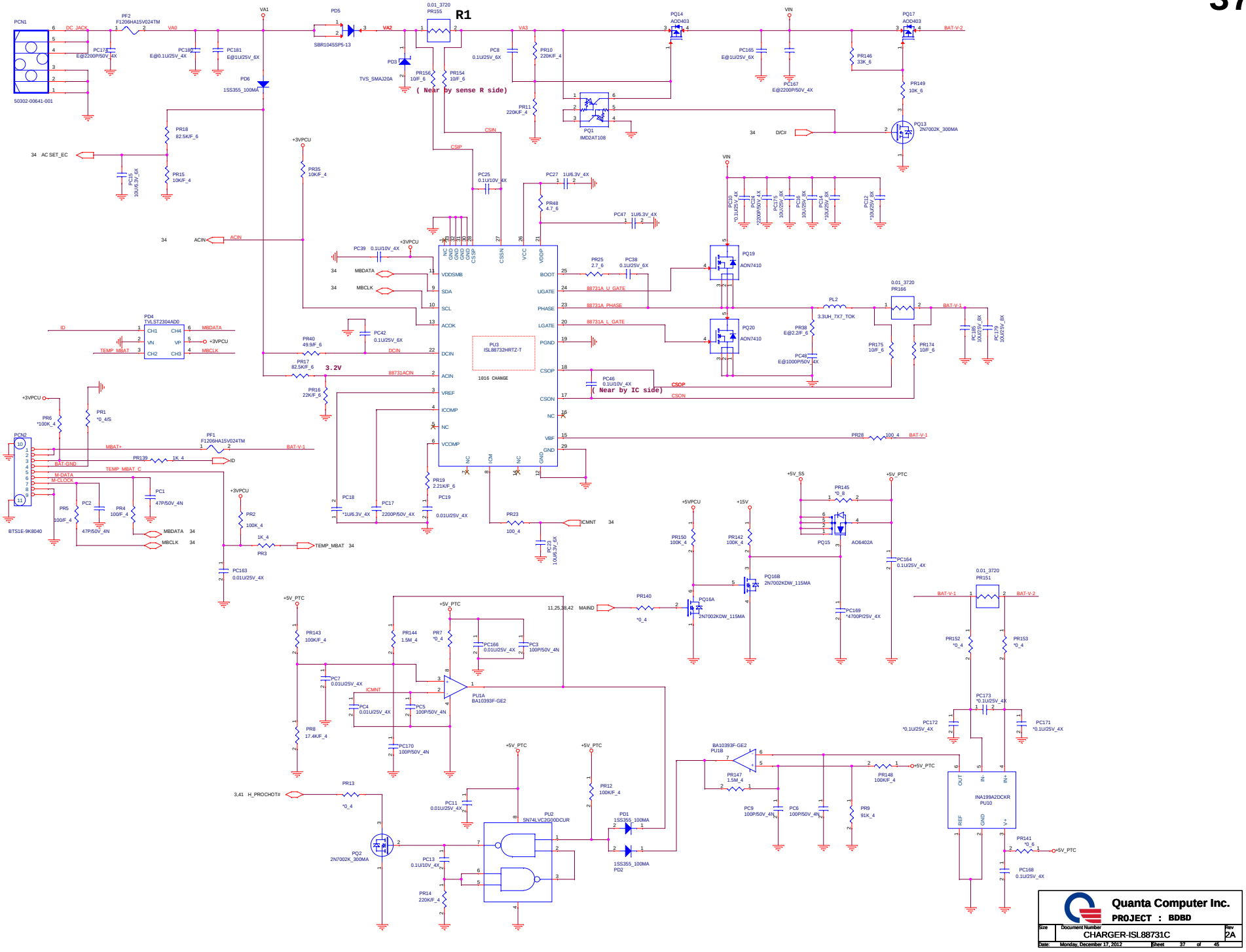


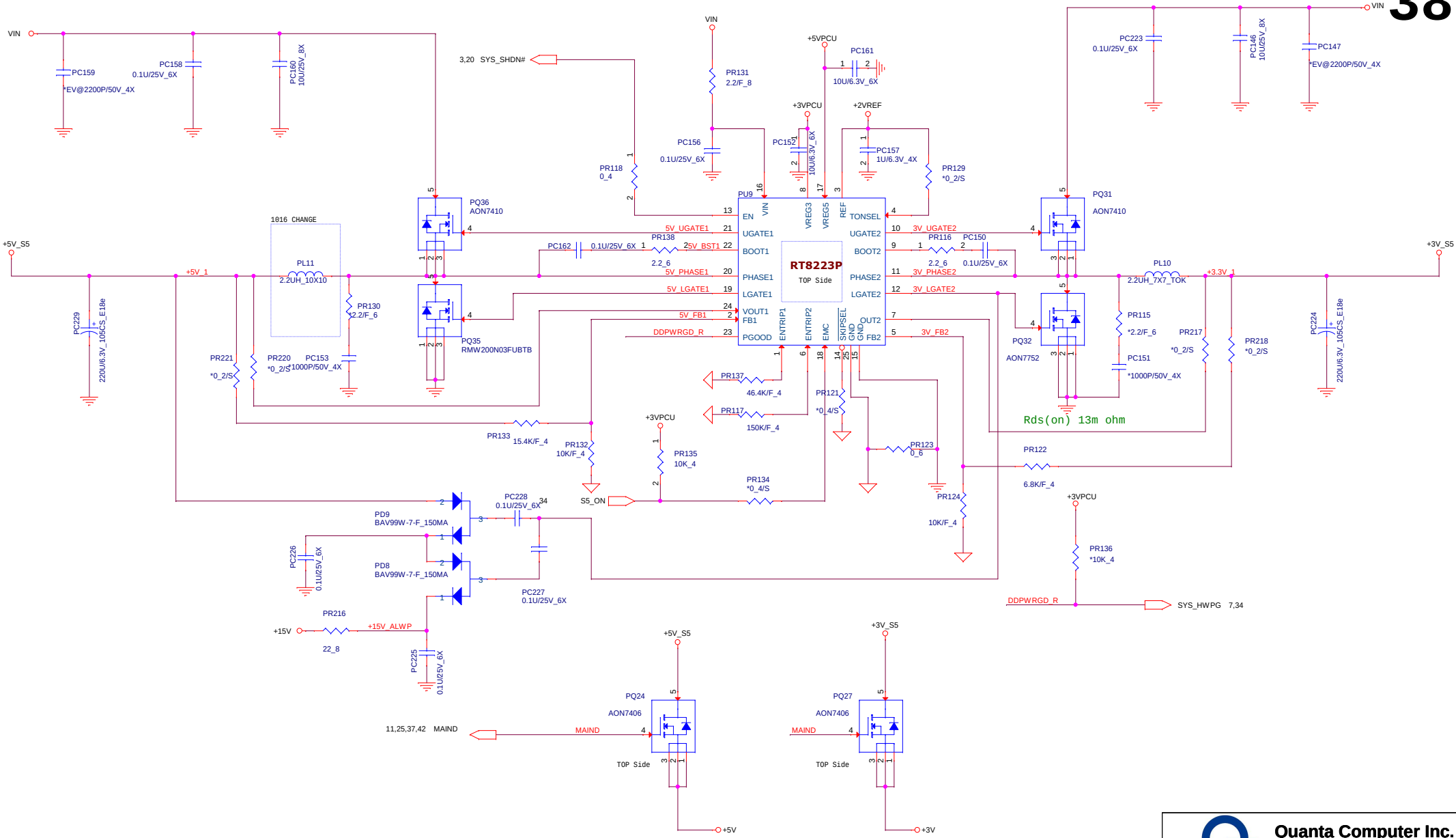
Quanta Computer Inc.

PROJECT : BDBD

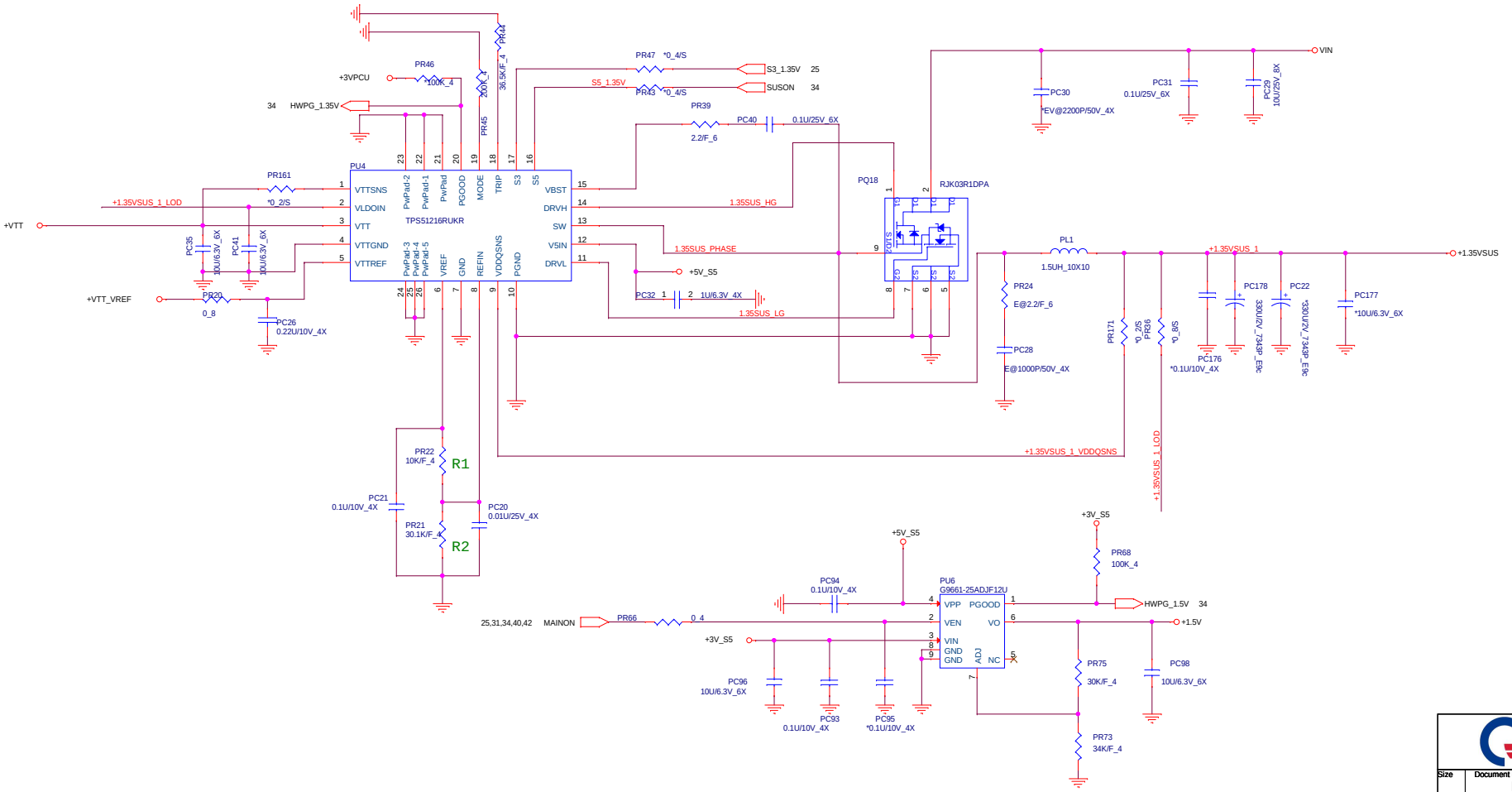
Size	Document Number	Rev
	LED/EMI/Green CLK	2A

Date: Monday, December 17, 2012 Sheet 36 of 45

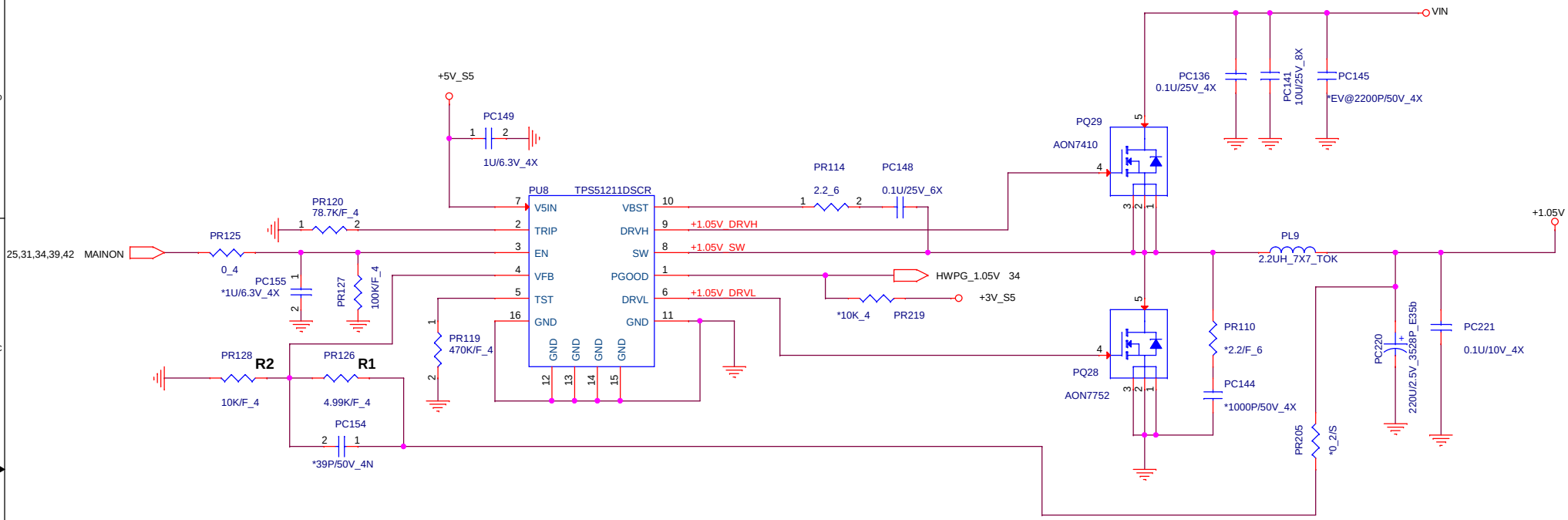

R1
(Near by sense R side)
(Near by IC side)
3.2V
1016 CHANGE
PU3 ISL88732HRTZ-T
PCN1
DC_JACK
50302-00641-001
PF2 F1206HA15V024TM
SBR1045SP5-13
TVS_SMAJ20A
1SS355_100MA
IMD2AT108
2N7002K_300MA
AON7410
AO6402A
2N7002KDW_115MA
3.3UH_7X7_TOK
PCN2
BTS1E-9K8040
PF1 F1206HA15V024TM
TVL-ST2304AD0
SN74LVC2G00DCUR
BA10393F-GE2
INA199A2DCKR
Quanta Computer Inc.
PROJECT : BDBD
CHARGER-ISL88731C
Monday, December 17, 2012



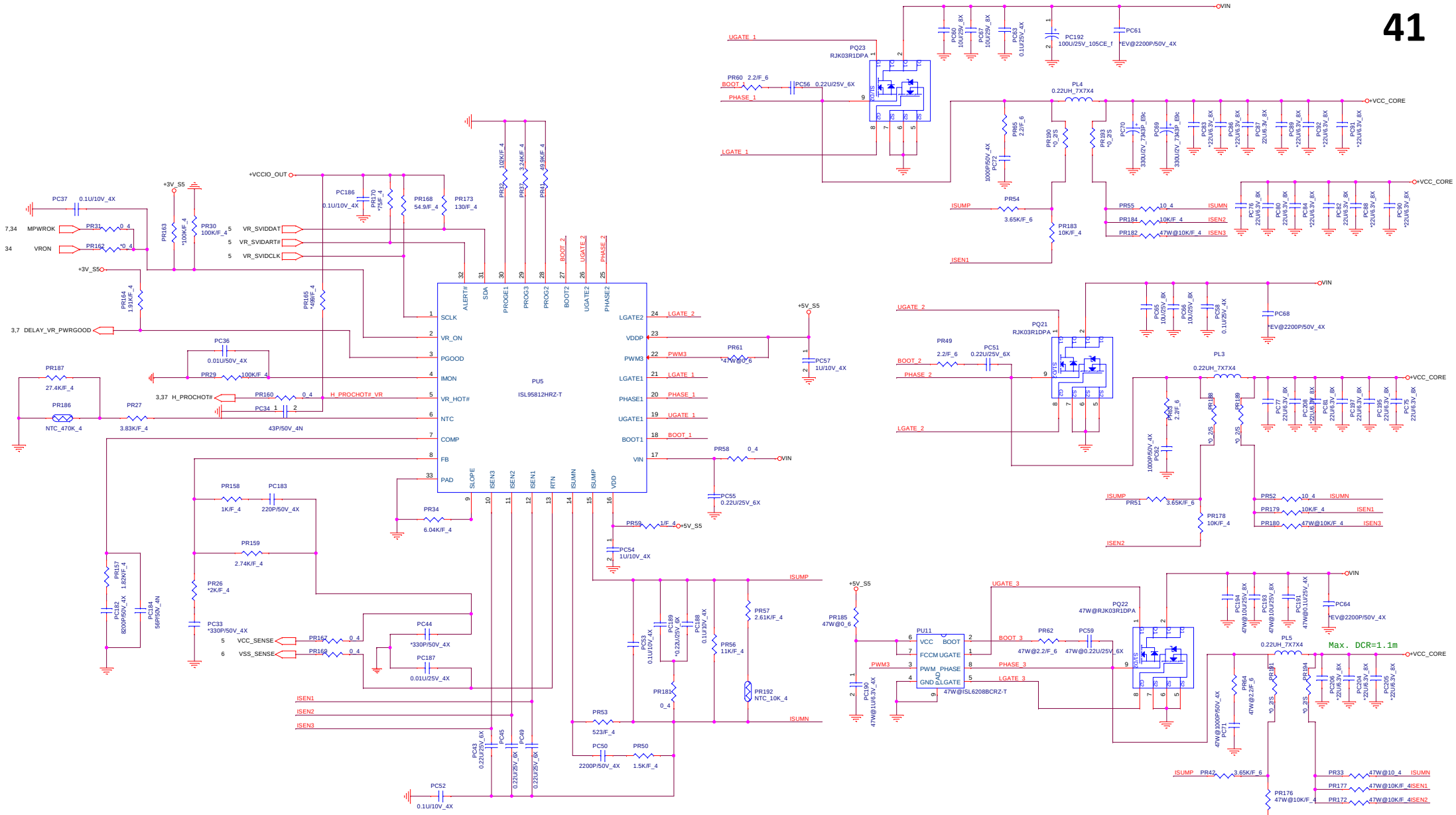
Quanta Computer Inc.		
PROJECT : BDBD		
Size	Document Number: System 3V/5V(TPS51123A)	Rev: 2A
Date: Monday, December 17, 2012	Sheet 38 of 45	



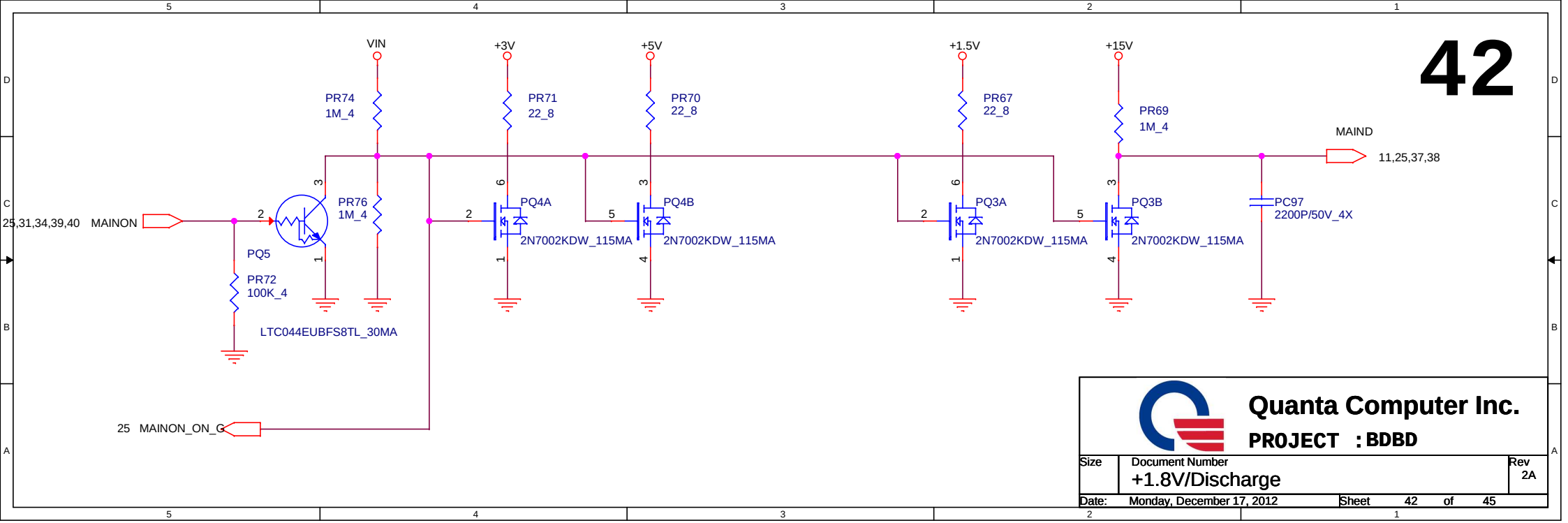
Quanta Computer Inc.		
PROJECT : BDBD		
Size	Document Number: DDR1.5V	Rev: 2A
Date: Monday, December 17, 2012	Sheet 39 of 45	

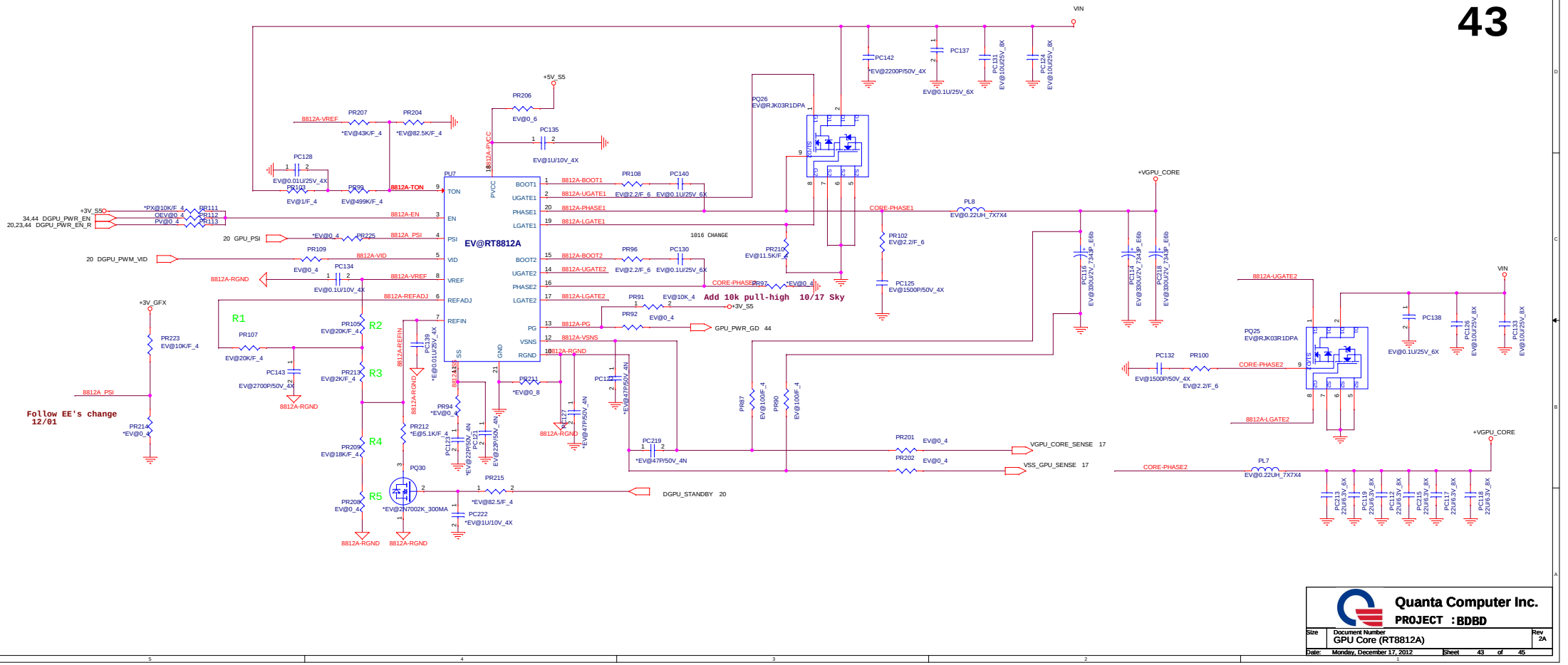


Quanta Computer Inc.		
PROJECT : BDBD		
Size	Document Number: +1.05V_A(TPS51211DSCR)	Rev: 2A
Date: Monday, December 17, 2012	Sheet 40 of 45	



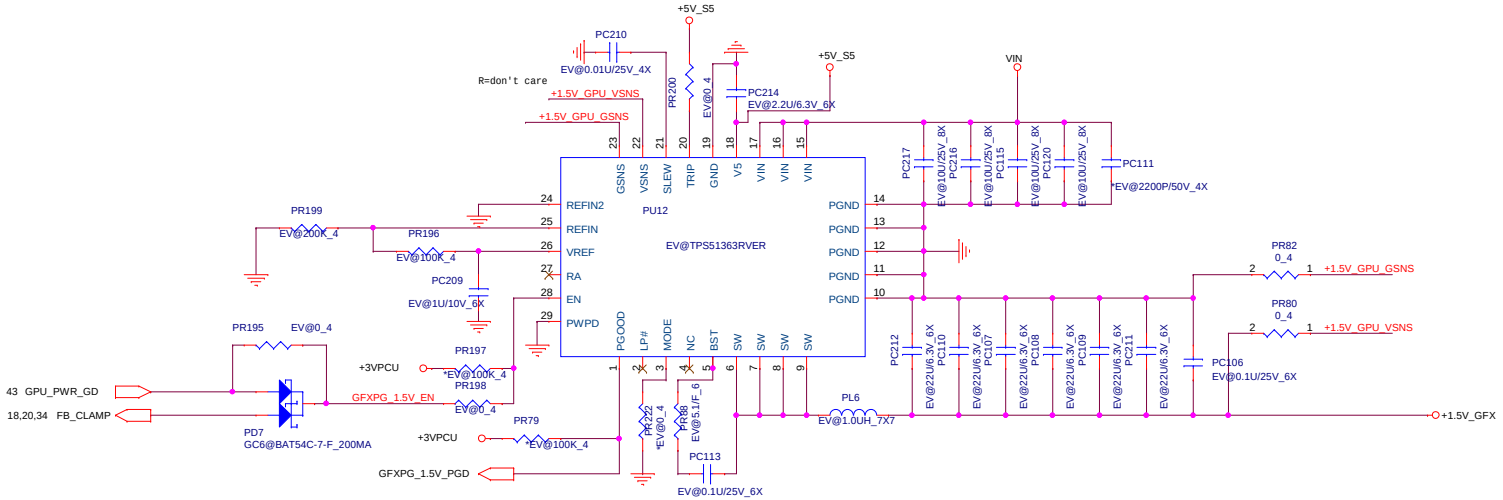
Quanta Computer Inc.			
PROJECT : BDBD			
Size	Document Number		Rev
	+VCCIN (ISL95812) 47/57W		2A
Date: Monday, December 17, 2012	Sheet 41 of 45		

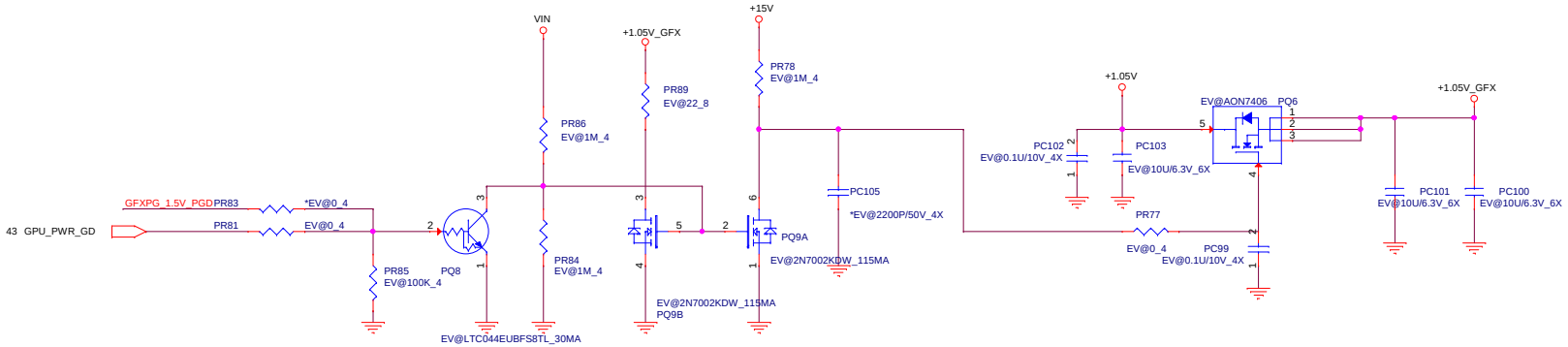

42
VIN
+3V
+5V
+1.5V
+15V
PR74
1M_4
PR71
22_8
PR70
22_8
PR67
22_8
PR69
1M_4
MAIND
11,25,37,38
25,31,34,39,40 MAINON
PR76
1M_4
PQ5
PR72
100K_4
LTC044EUBFS8TL_30MA
PQ4A
2N7002KDW_115MA
PQ4B
2N7002KDW_115MA
PQ3A
2N7002KDW_115MA
PQ3B
2N7002KDW_115MA
PC97
2200P/50V_4X
25 MAINON_ON_G
Quanta Computer Inc.
PROJECT : BDBD
Size
Document Number
+1.8V/Discharge
Rev
2A
Date: Monday, December 17, 2012
Sheet 42 of 45

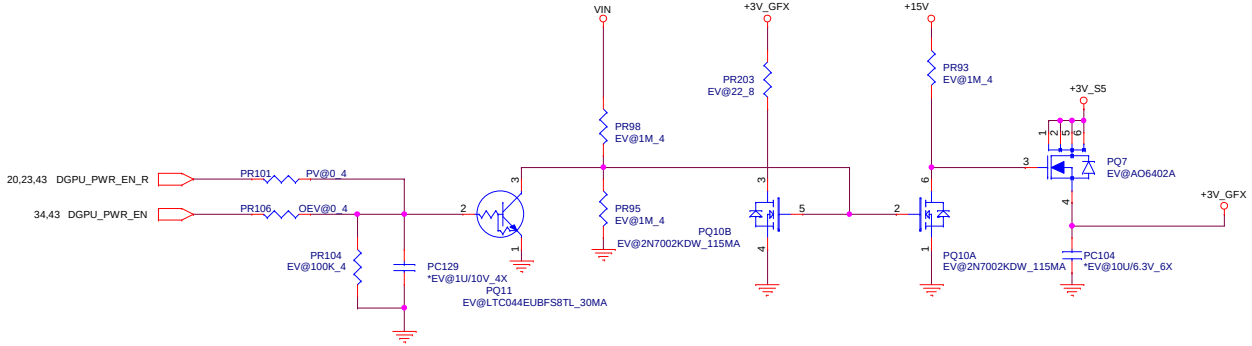


Quanta Computer Inc.		
PROJECT : BDBD		
Size	Document Number: GPU Core (RT8812A)	Rev 2A
Date: Monday, December 17, 2012	Sheet 43 of 45	

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.







Quanta Computer Inc.

PROJECT : BDBD

Size	Document Number	Rev
	+VGACORE	2A

Date: Monday, December 17, 2012 Sheet 44 of 45

Model	REV	CHANGE LIST
BDBD	B2A	PAGE 8: C795,C805 Change to 15pf
		PAGE 8: CN11 Change socket type
		PAGE 8:Add R1328 and R1516 for QUAD IO
		PAGE 9: Change C769,C763 to 12pf
		PAGE 10: Add board ID for SPK,CIR,TV
		PAGE 19: Change C731,C732 to 12pf
		PAGE 30: Add LAN IC
		PAGE 32: Change R638,R639,R640,R641,R642,R643,R644,R645 to bead
		PAGE 33: Change Card read to RTS5229
		PAGE 34: Add R523 for PB_LED change to high active
		PAGE 34:Remove R411 for optimu
		PAGE 35: Change R499,R498,R505,R502 for LED brightness SPEC

MODEL BY3E

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	

DOC NO. 20121217	PROJECT MODEL :	BDBD	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISON:	

Quanta Computer Inc.
PROJECT : BDBD
Size | Document Number: Change list | Rev 2A
Date: Monday, December 17, 2012 Sheet 49 of 49