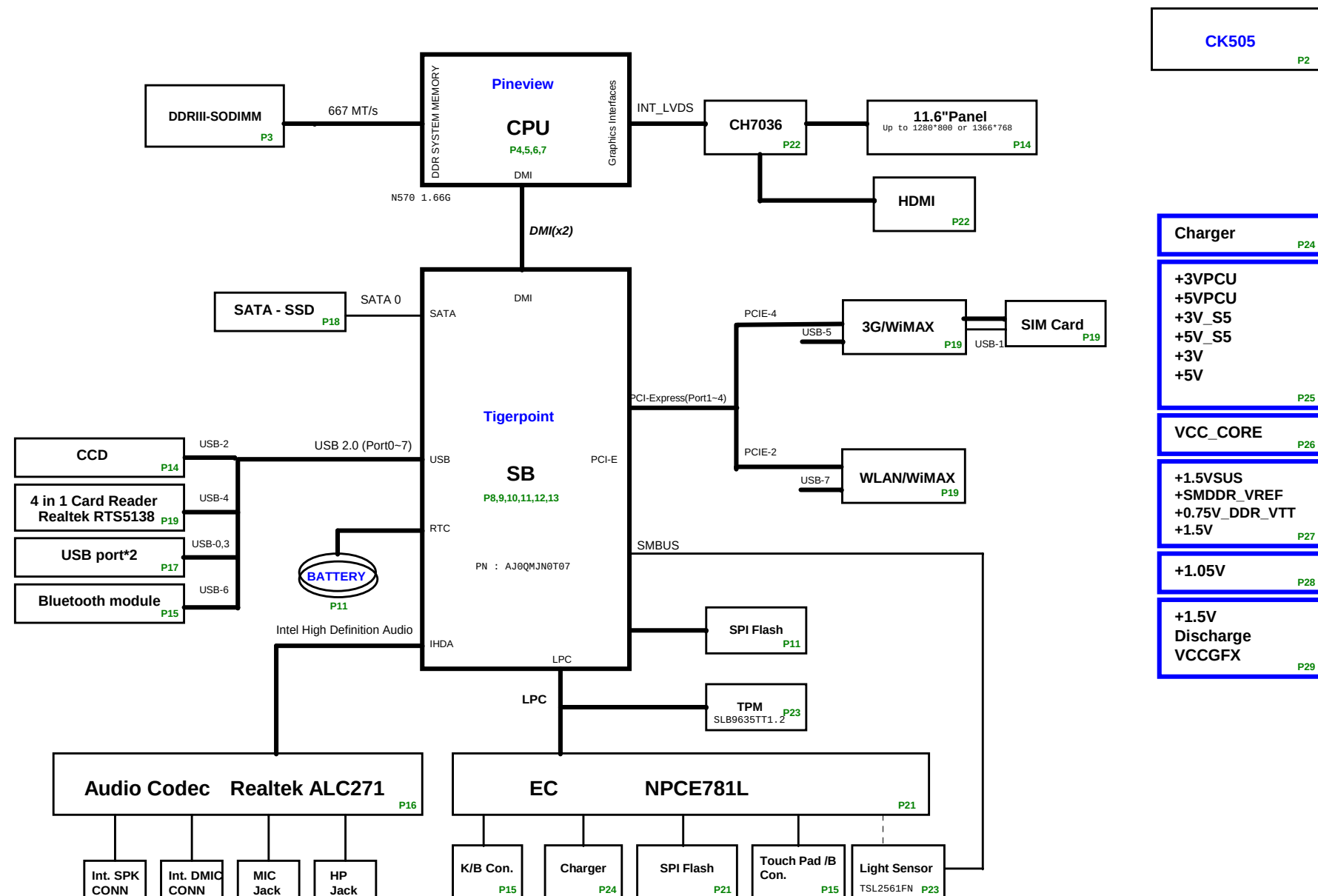
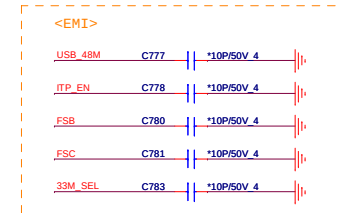
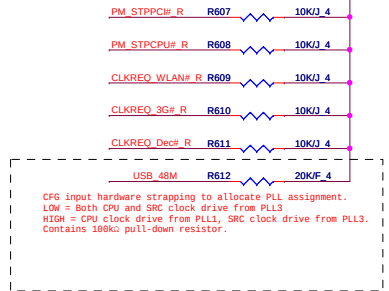
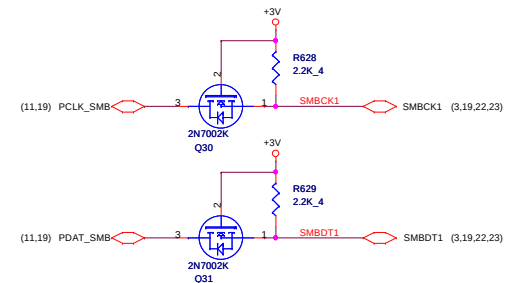


ZGB Block Diagram

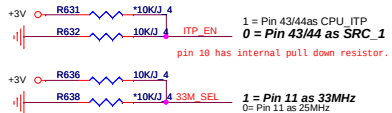
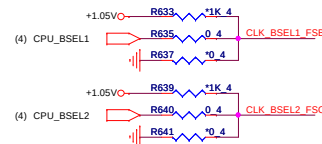




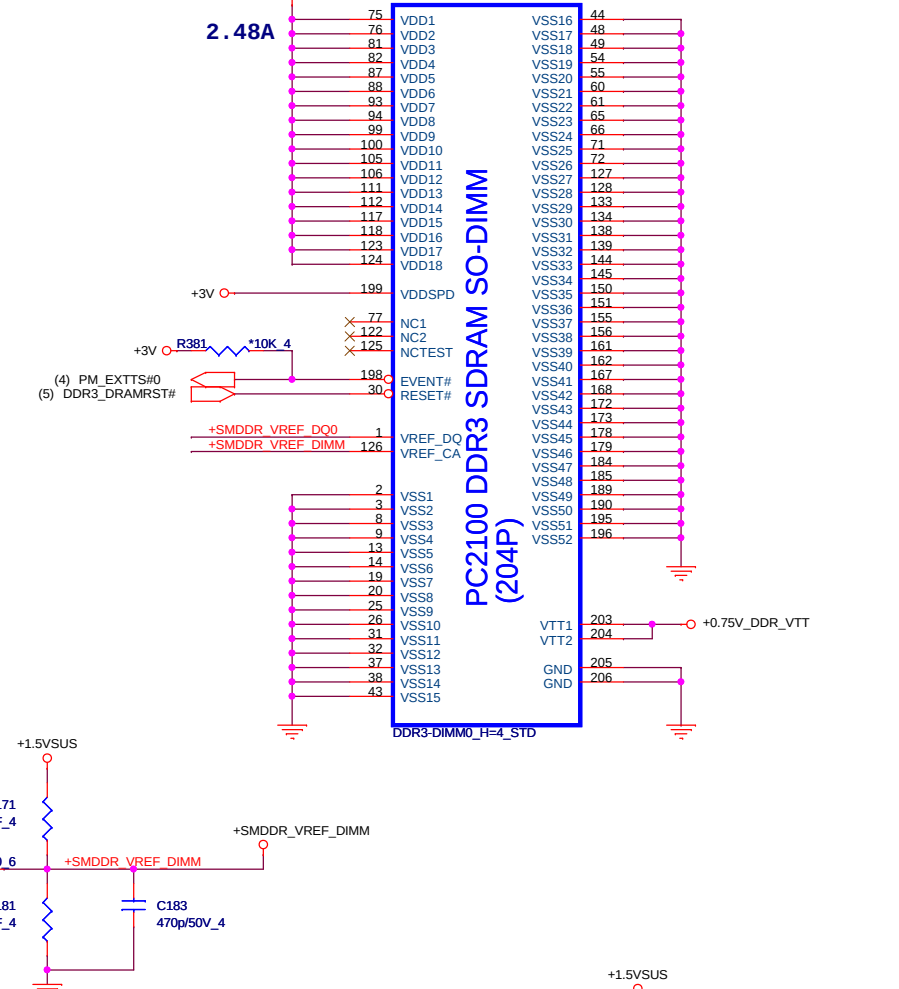
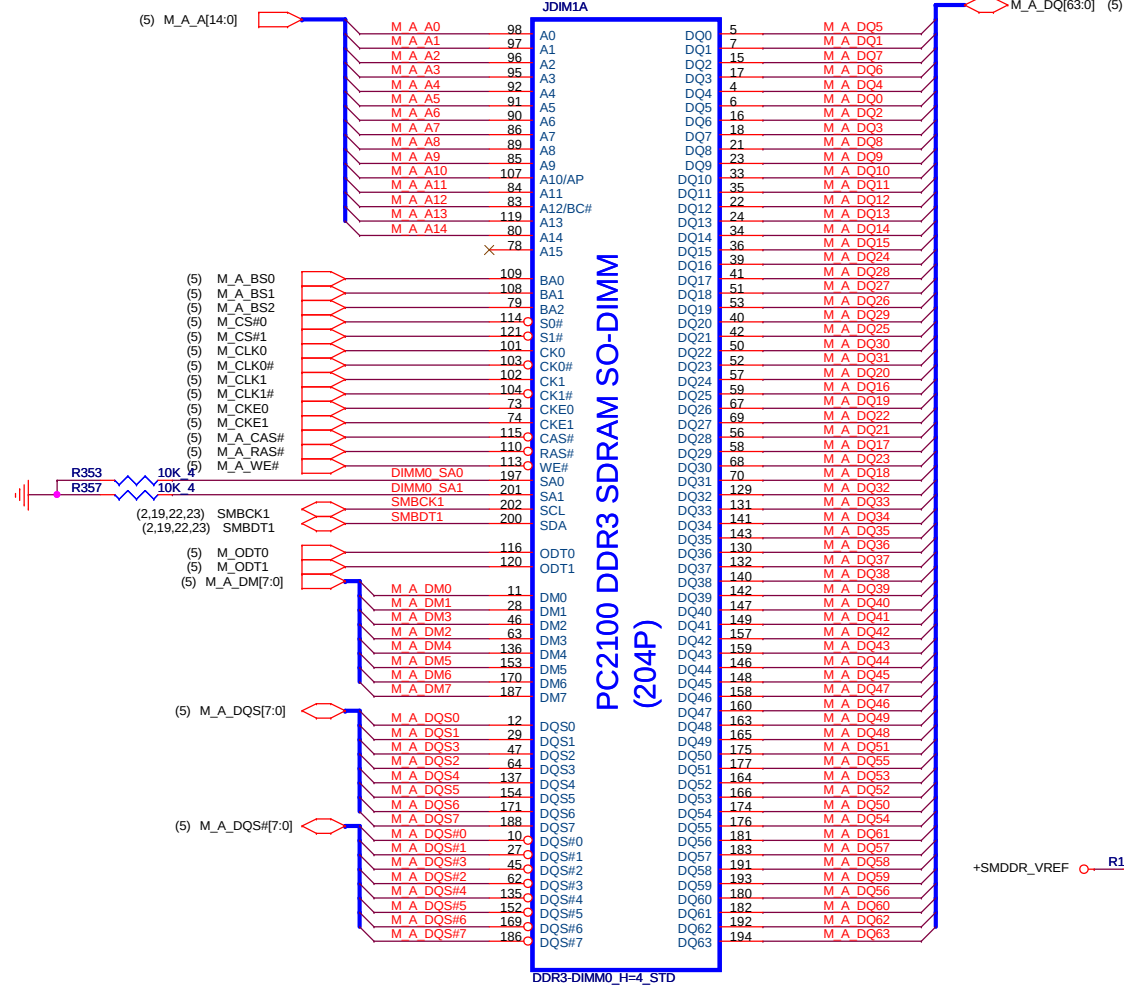
VR PWRGD



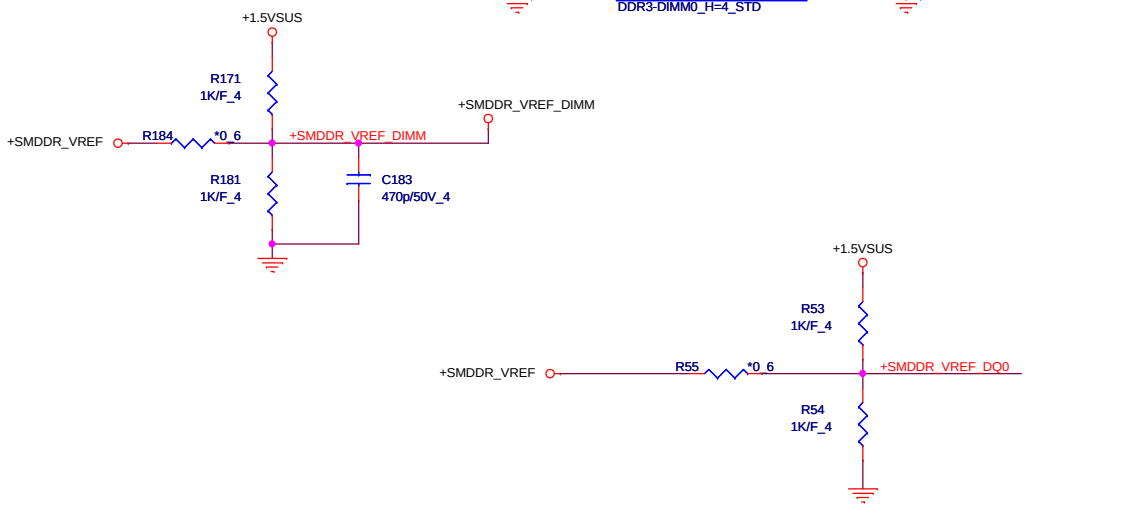
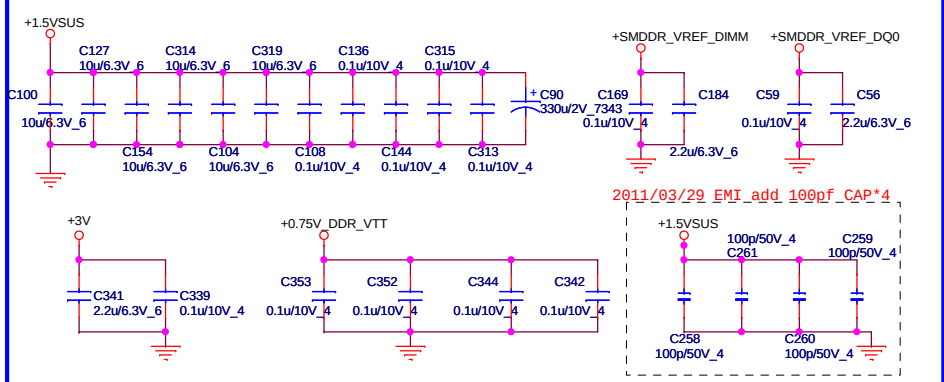
no connect FSA to CPU, due to there is no FSA PIN for CPU.
need to check check how to handle it in CPU CLK_BESEL0

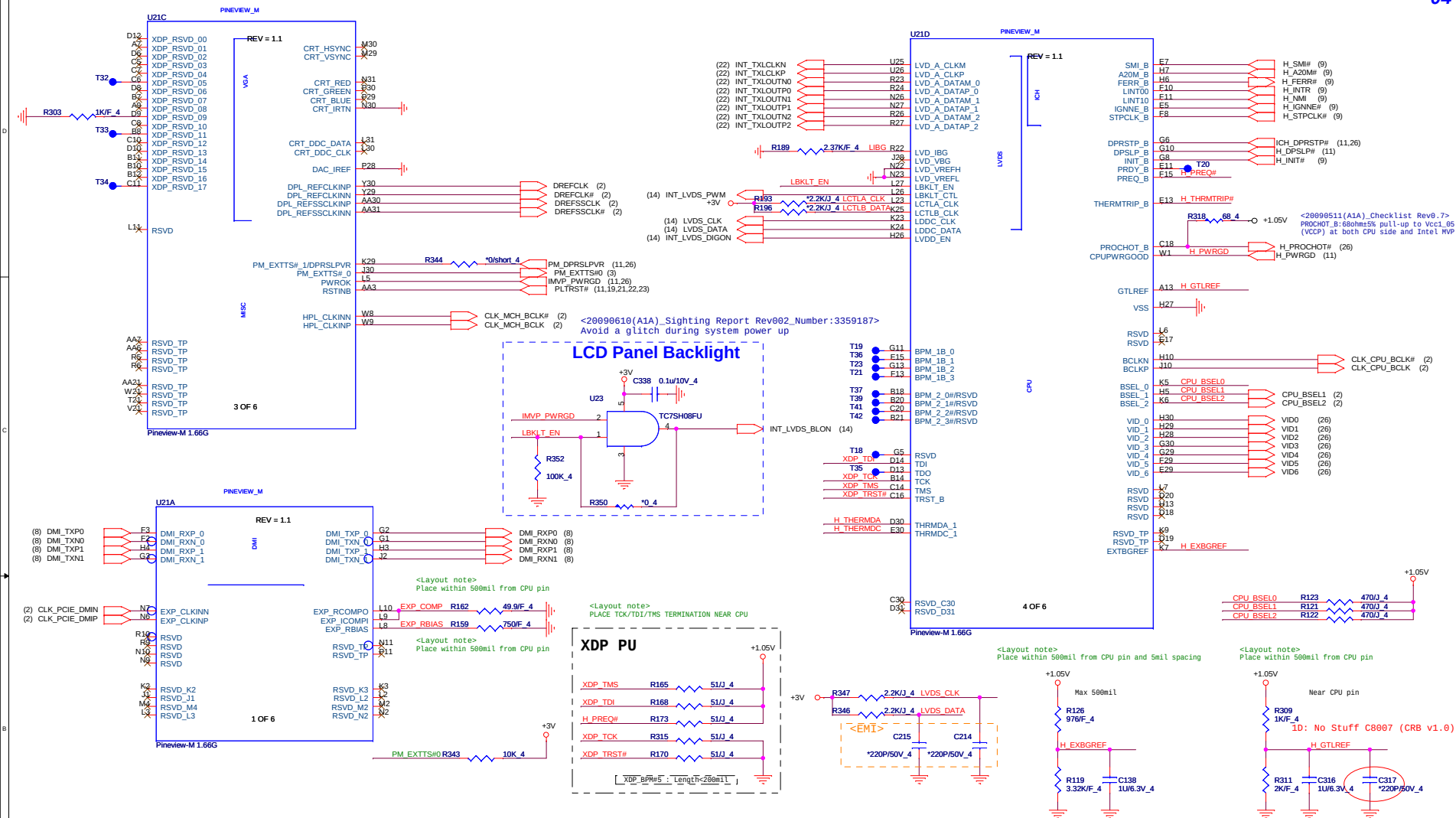


DDR_STD(DDR)



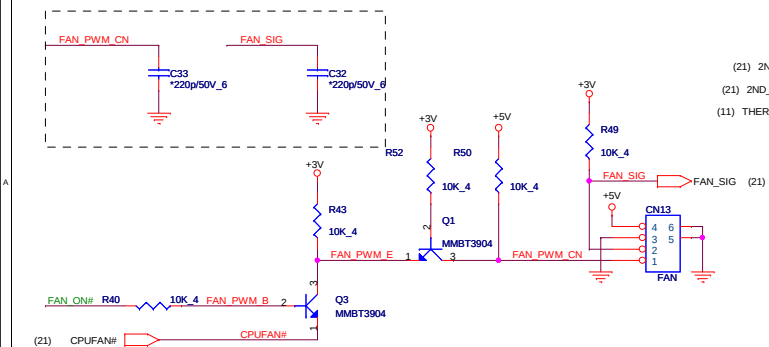
Place these Caps near So-Dimm0.



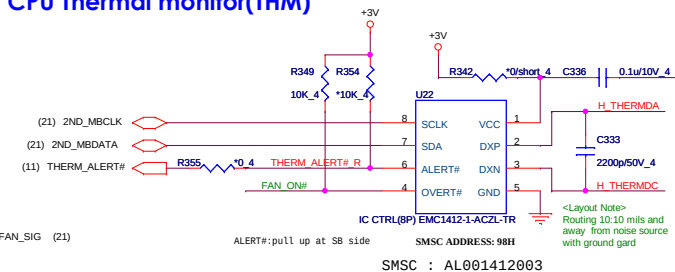


CPU FAN CTRL(THM)

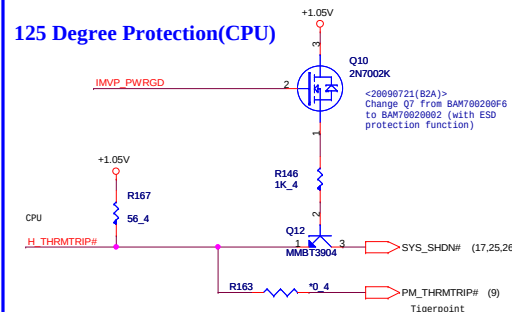
8/11 B-test : for EMI

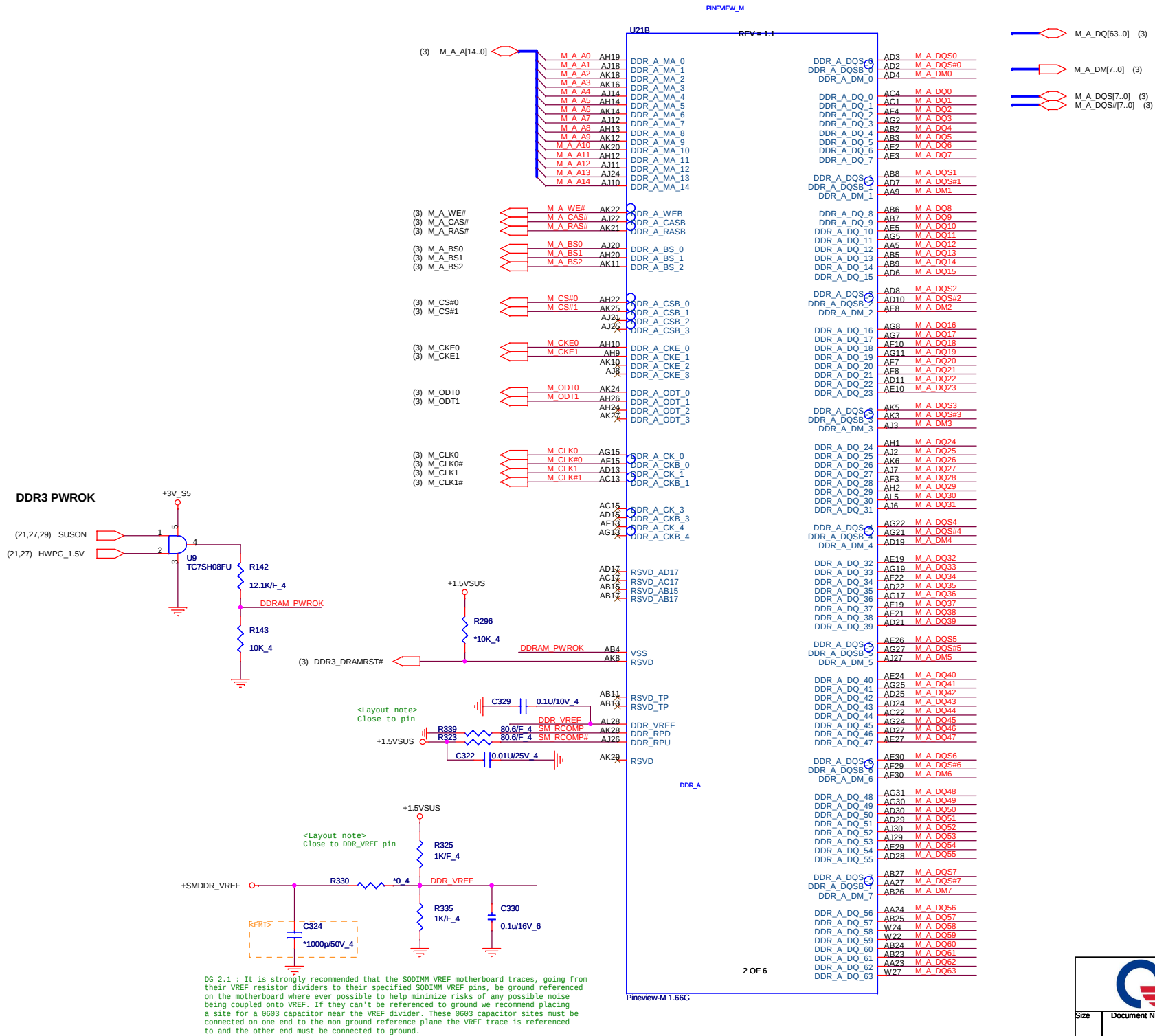


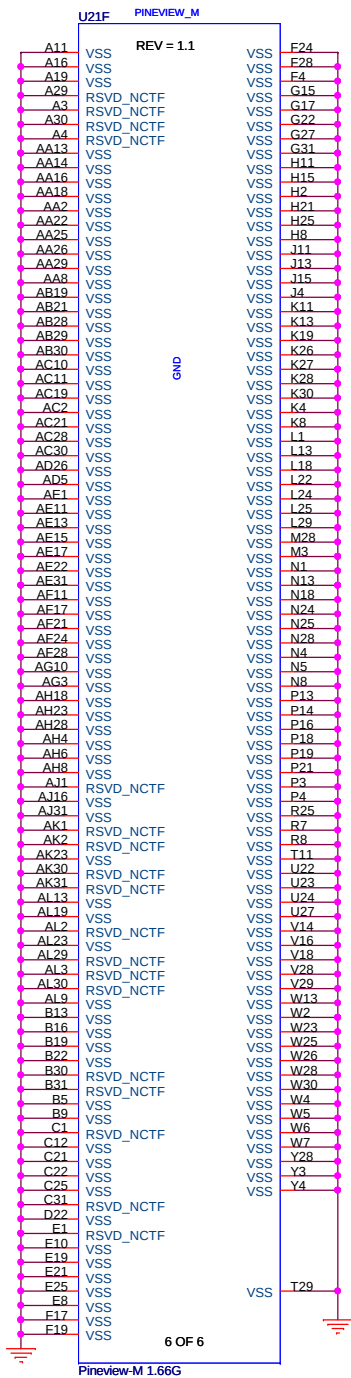
CPU Thermal monitor(THM)

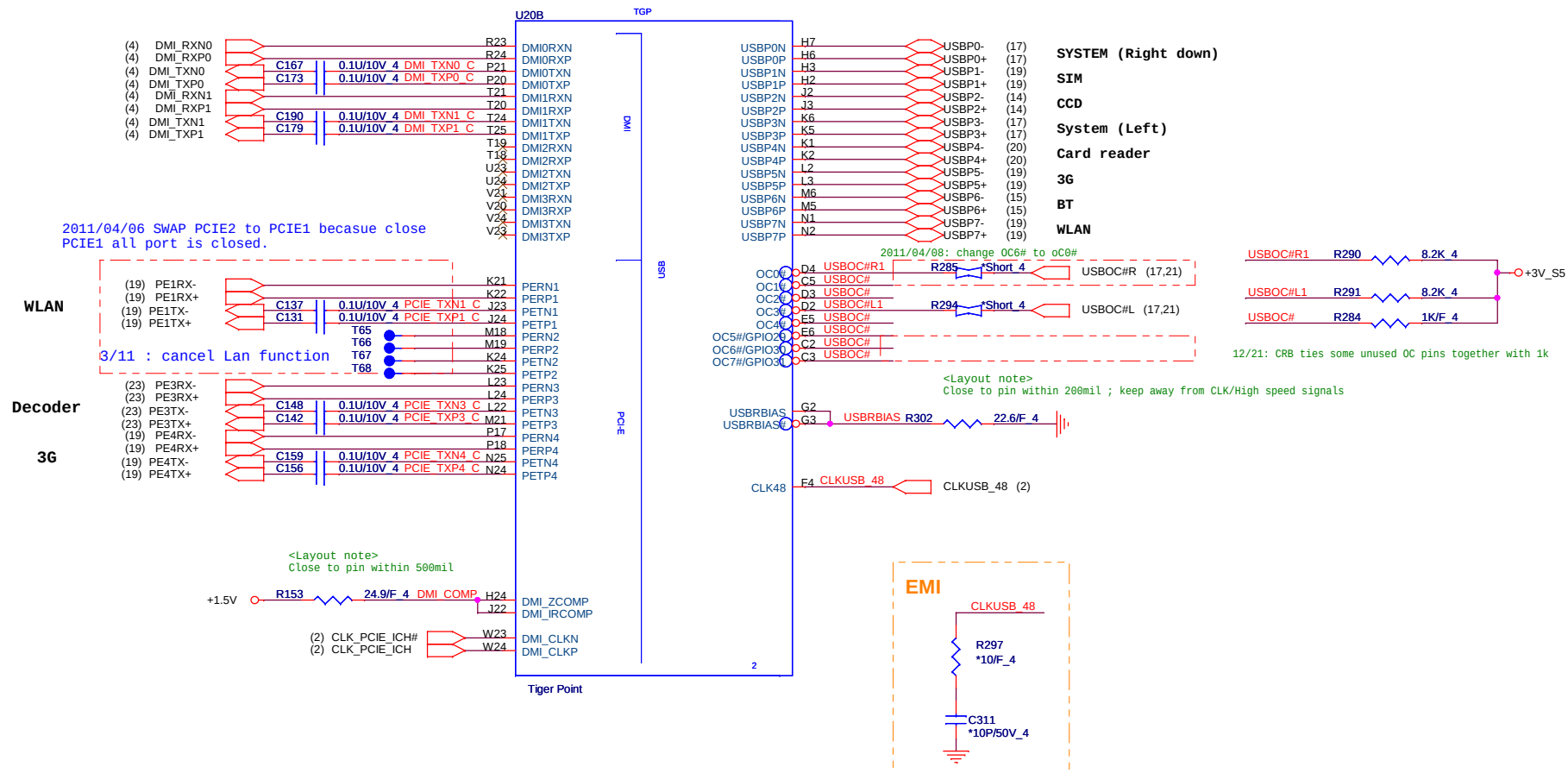


125 Degree Protection(CPU)



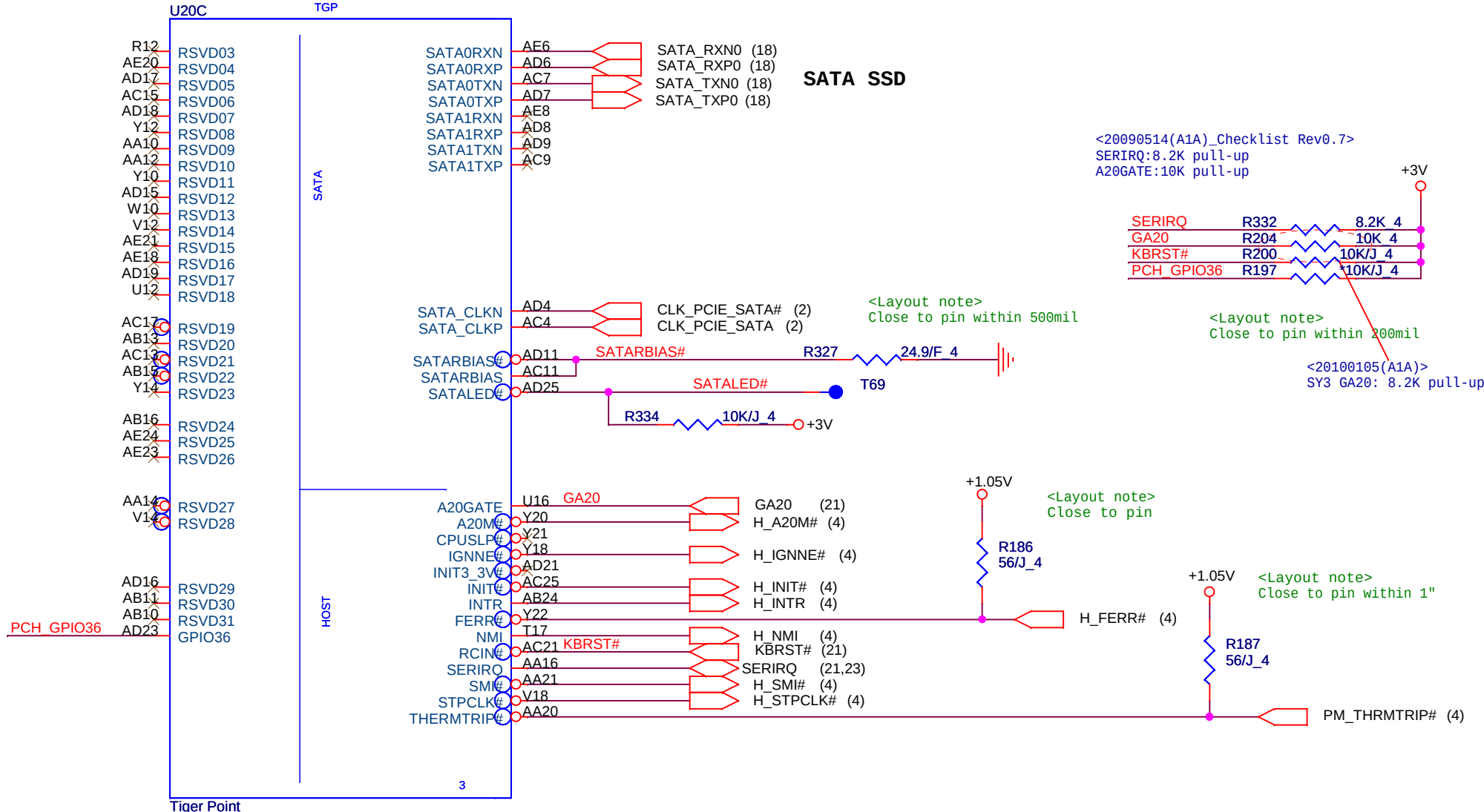






Quanta Computer Inc.
PROJECT : Z6B

Size	Document Number	Rev
	Tiger Point DMI/PCIE/USB	2A
Date:	Friday, April 08, 2011	Sheet 8 of 34



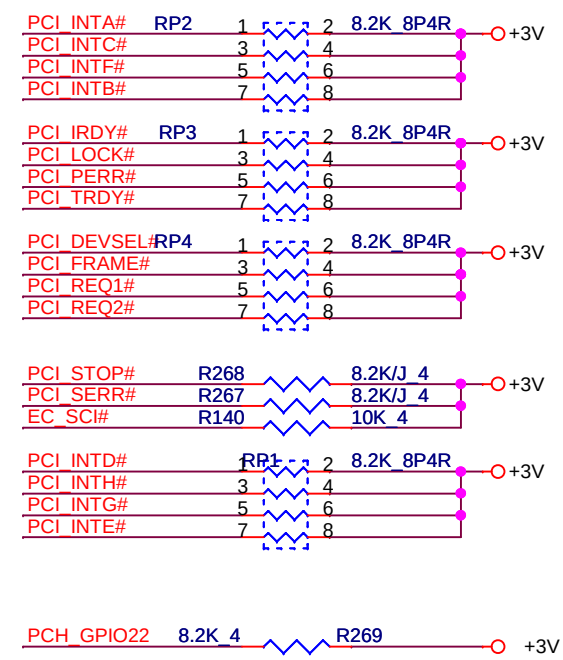
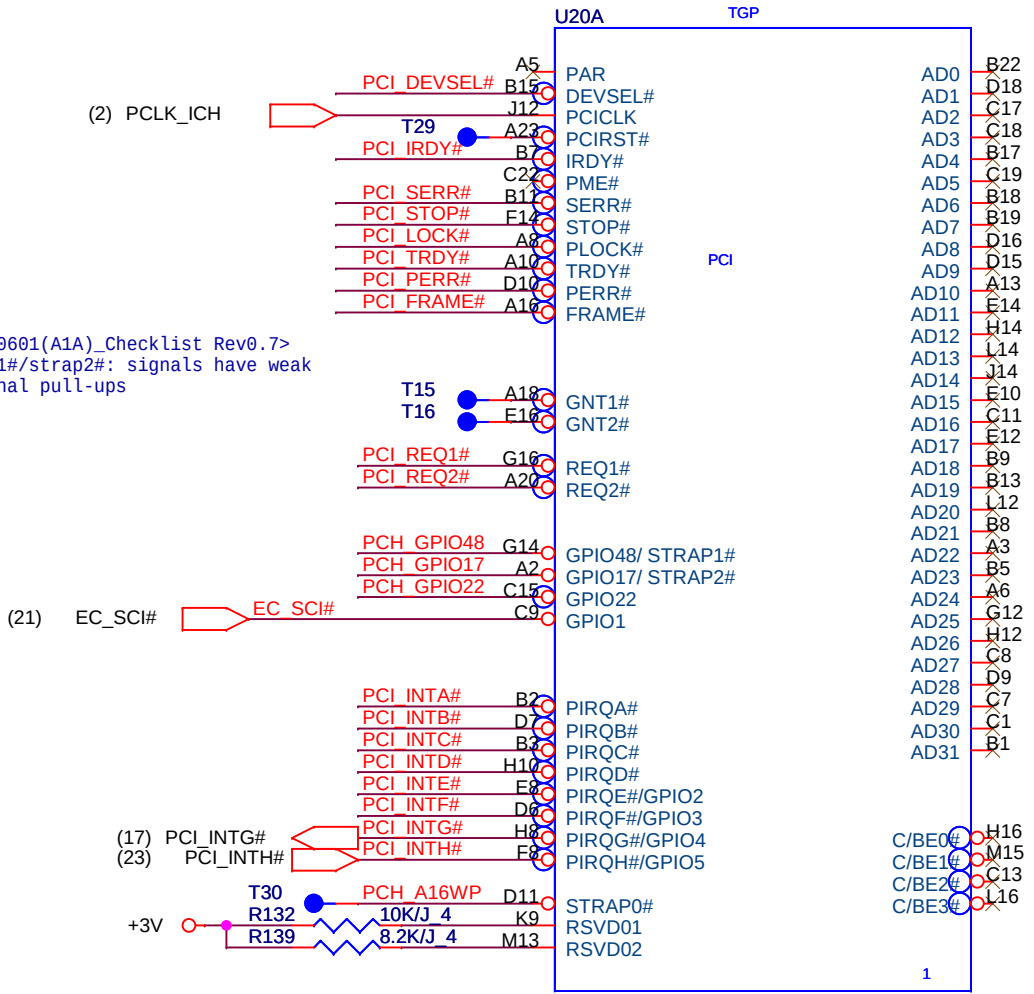
NOTE :
 1. CPUSLP# is supported only on nettop platforms.

Quanta Computer Inc.

PROJECT : ZGB

Size	Document Number	Rev
	Tiger Point Sata/Host	2A
Date:	Friday, April 08, 2011	Sheet 9 of 34

<20090601(A1A)_Checklist Rev0.7>
Strap1#/strap2#: signals have weak
internal pull-ups



IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UH Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2

PCI_GNT#2	Internal PU Should not be PD
-----------	---------------------------------

ICH Boot BIOS select

PCH_GPIO17 (INT PU)	PCH_GPIO48 (INT PU)	Boot BIOS Location
0	1	SPI (Default)
1	0	PCI
1	1	LPC



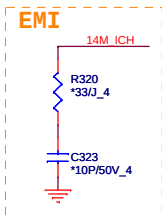
A16 SWAP Override strap

PCH_A16W (INT PU)	Low = A16 swap override enabled High = Default
----------------------	---

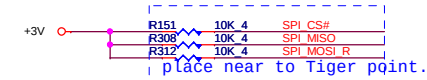
Quanta Computer Inc.

PROJECT : ZGB

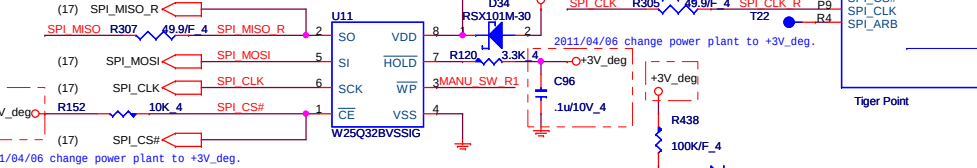
Size	Document Number	Rev 2A
TigerPoint PCI(3/6)		
Date:	Friday, April 08, 2011	Sheet 10 of 34



debug port for google require

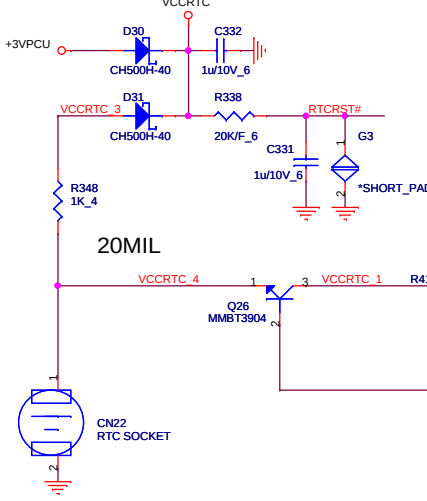


SPI FLASH(CLG)

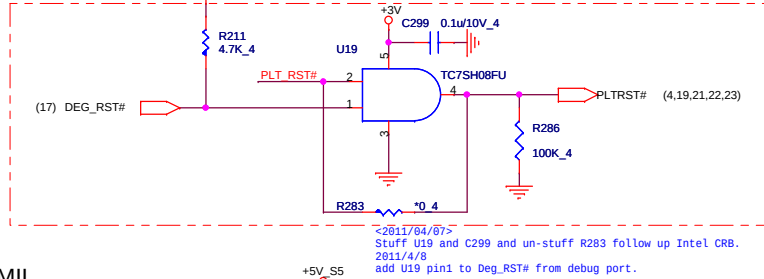


1/13 Confirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

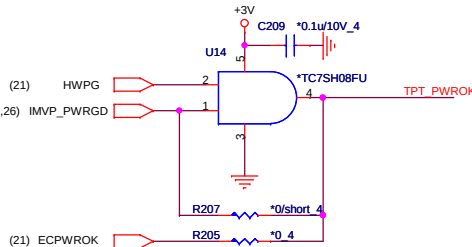
RTC(RTC)



Platform Reset



TPT Power OK



ACZ_SDOUT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0	* 4 x 1s
1	0	Reserved
0	1	Reserved
1	1	1 x 4s (1 port/4 lanes)

INTVRMEN	
1	Enable internal VccSus1_5 VRM (default)
0	Disable

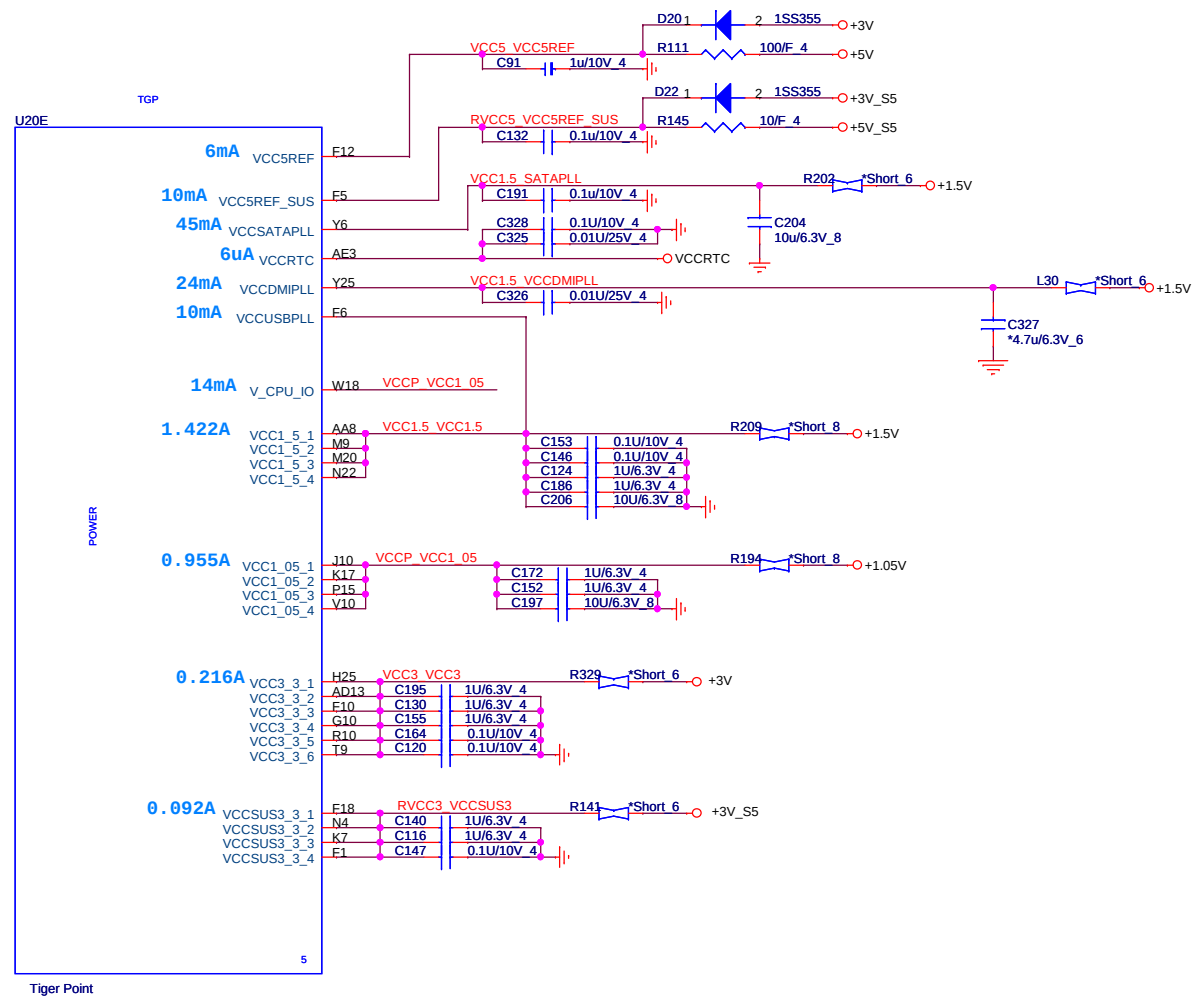
Quanta Computer Inc.
PROJECT : ZGB

Size: Document Number: Rev 2A

Date: Friday, April 08, 2011 Sheet 11 of 34

1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

<Layout note>
Place 0402 caps close to ball
Place 0603/0805 caps close to ICH

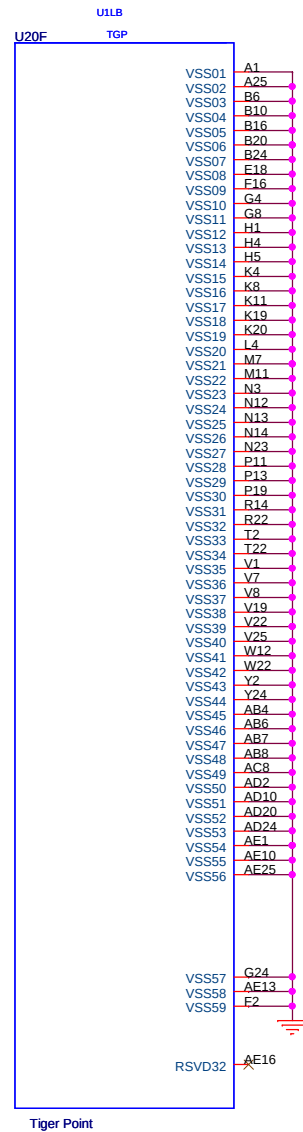


- 1.Level 1 Environment-related Substances should NEVER be Used.
- 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



Quanta Computer Inc.
PROJECT : ZGB

Size	Document Number	Rev
		2A
TigerPoint Power		
Date:	Friday, April 08, 2011	Sheet 12 of 34

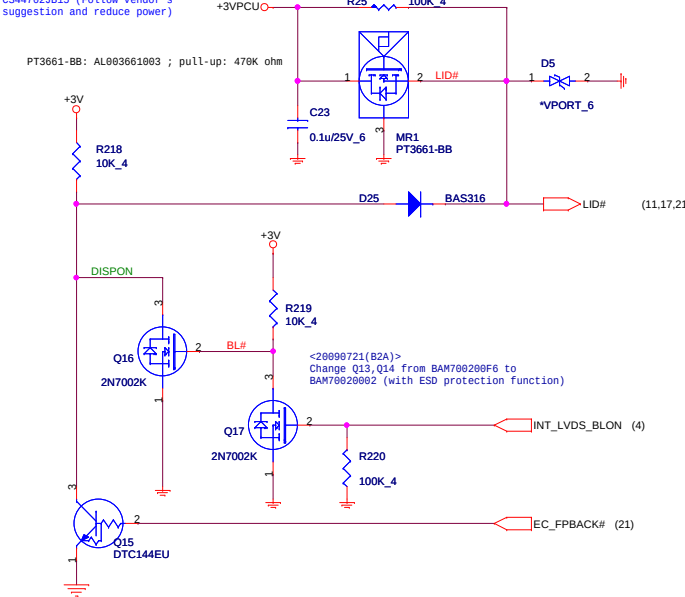


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

		Quanta Computer Inc.	
		PROJECT : ZGB	
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TigerPoint GND			
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<20090724(B2A)>
Change R5 from CS41002J820 to
CS44702J815 (Follow vendor's
suggestion and reduce power)

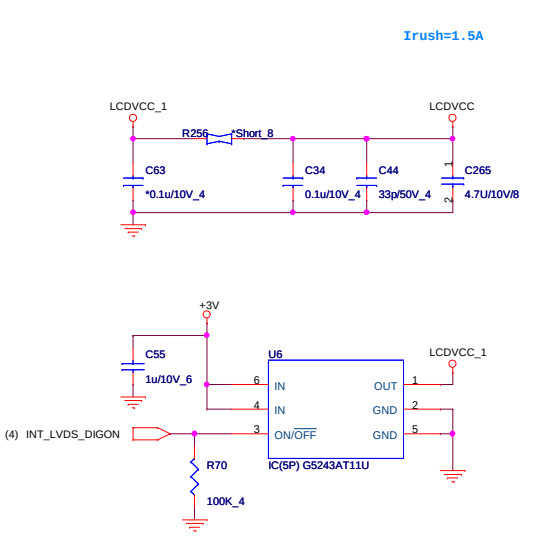
HALL SENSOR(HSR)



CRT(CRT)

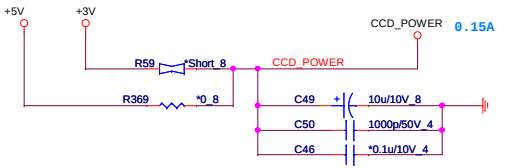
3/11 : cancel CRT function

LED Panel POWER SWITCH(LDS)

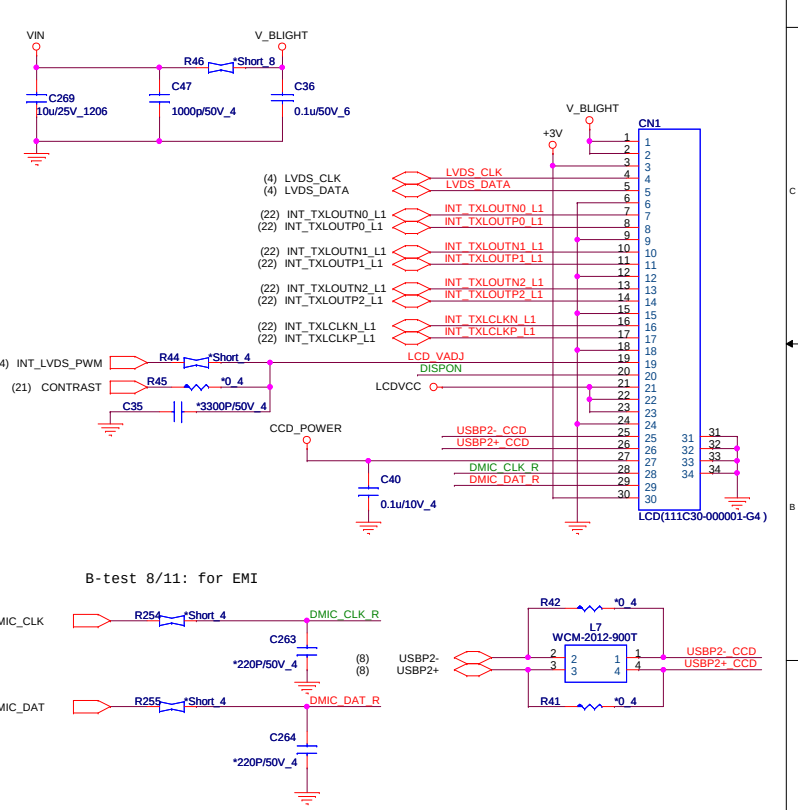


CAMERA POWER(CCD)

14



LED Panel(LDS)



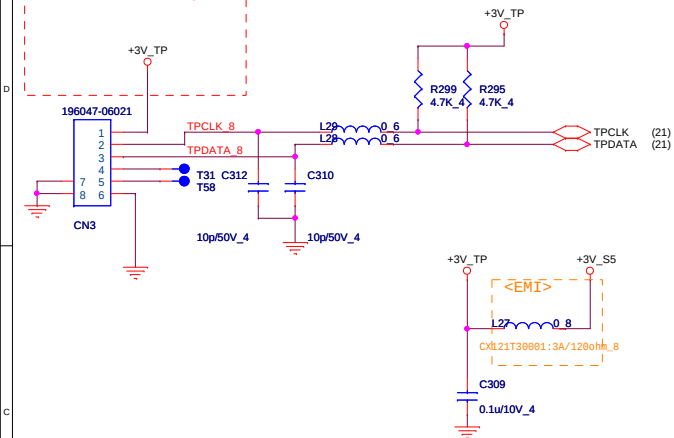


Quanta Computer Inc.
PROJECT : ZGB

Size	Document Number	Rev
	CRT/LVDS	2A
Date:	Friday, April 08, 2011	Sheet 14 of 34

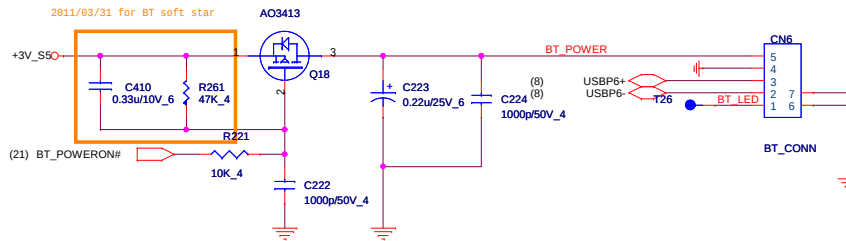
TOUCH PAD(TPD)

2011/3/28 Remove 4pin connector

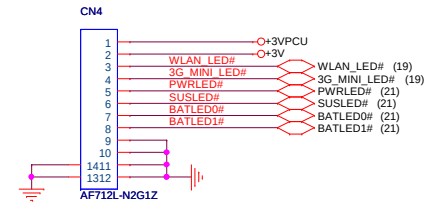


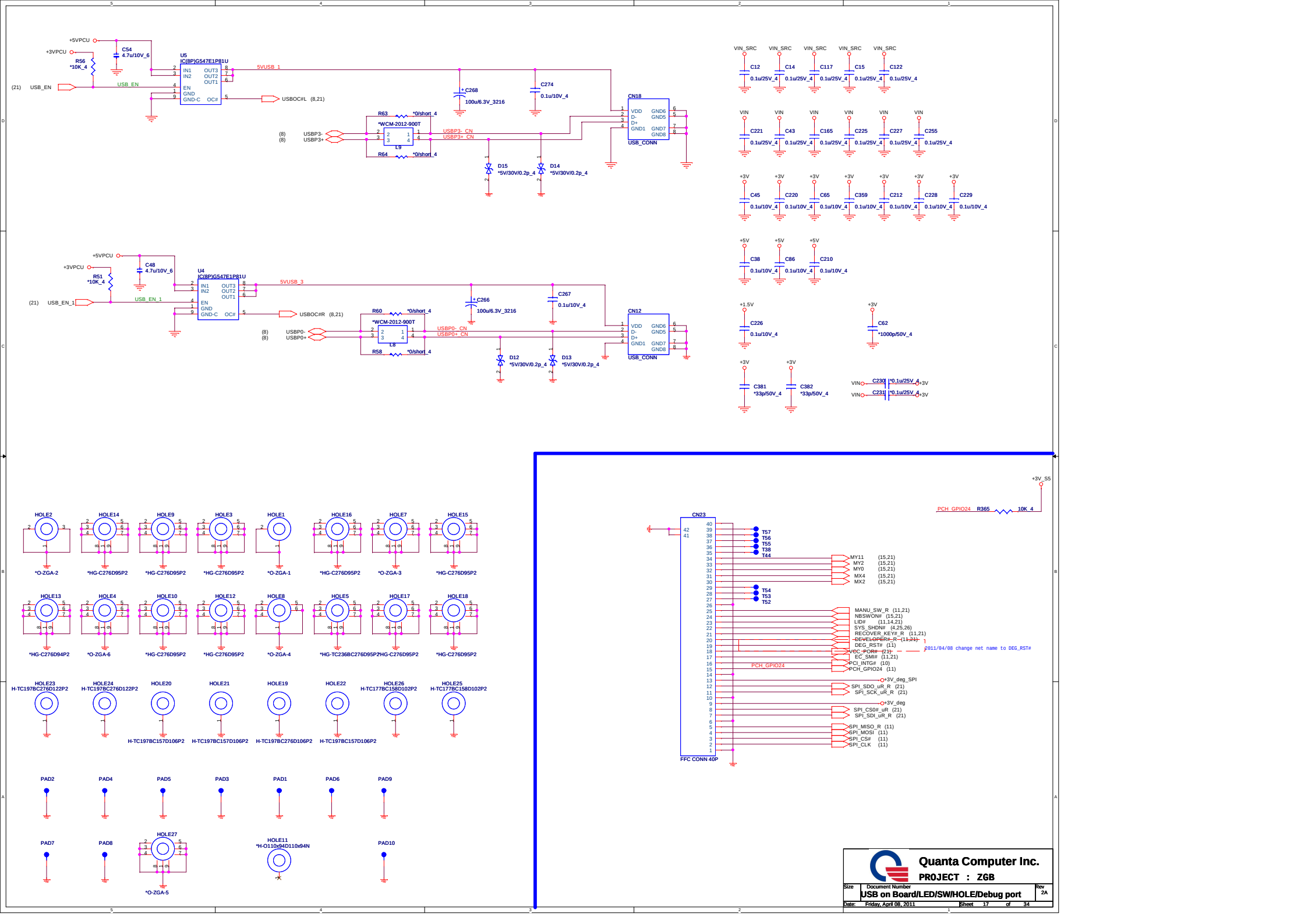
BLUETOOTH(BTM)

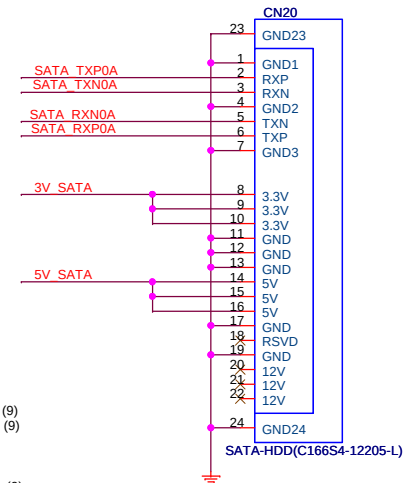
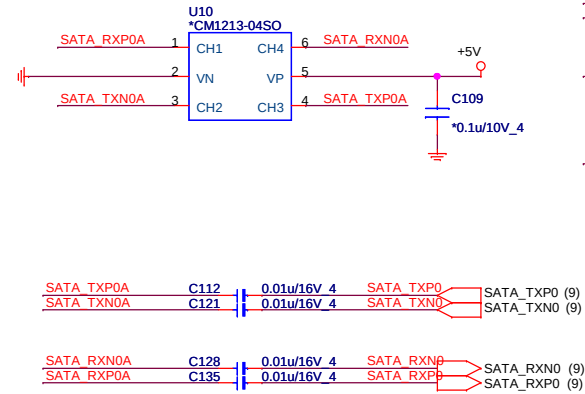
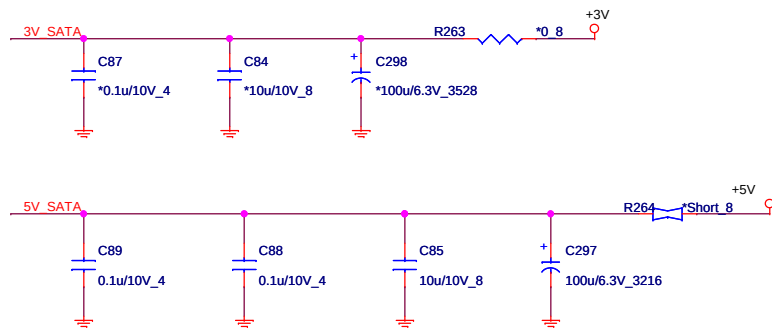
2011/03/31 for BT soft star

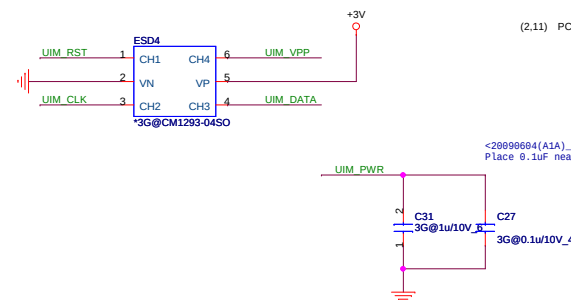


Connector (UIF)



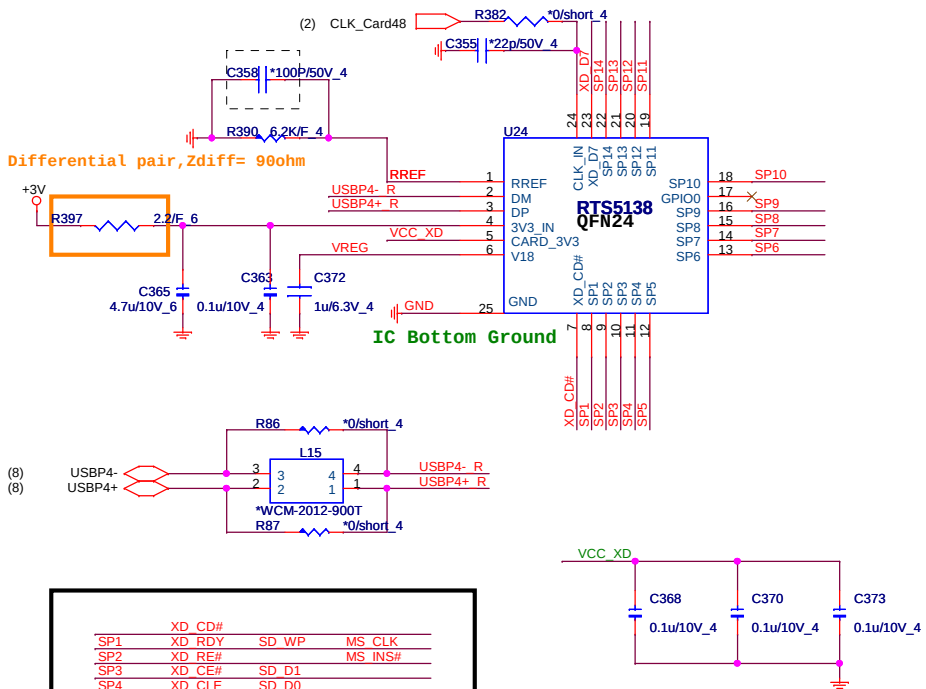






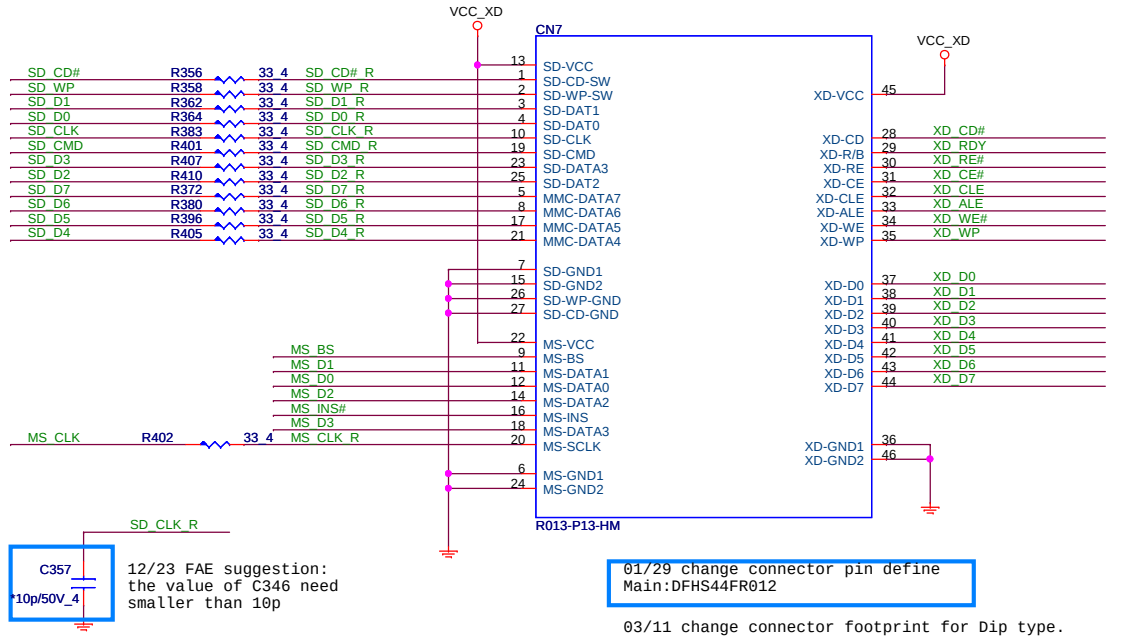
 Quanta Computer Inc. PROJECT : ZGB		Rev
Size	Document Number	2/
Mini-Card/WL/3G/SIM		
Date:	Friday, April 08, 2011	Sheet 19 of 34

RTS5138

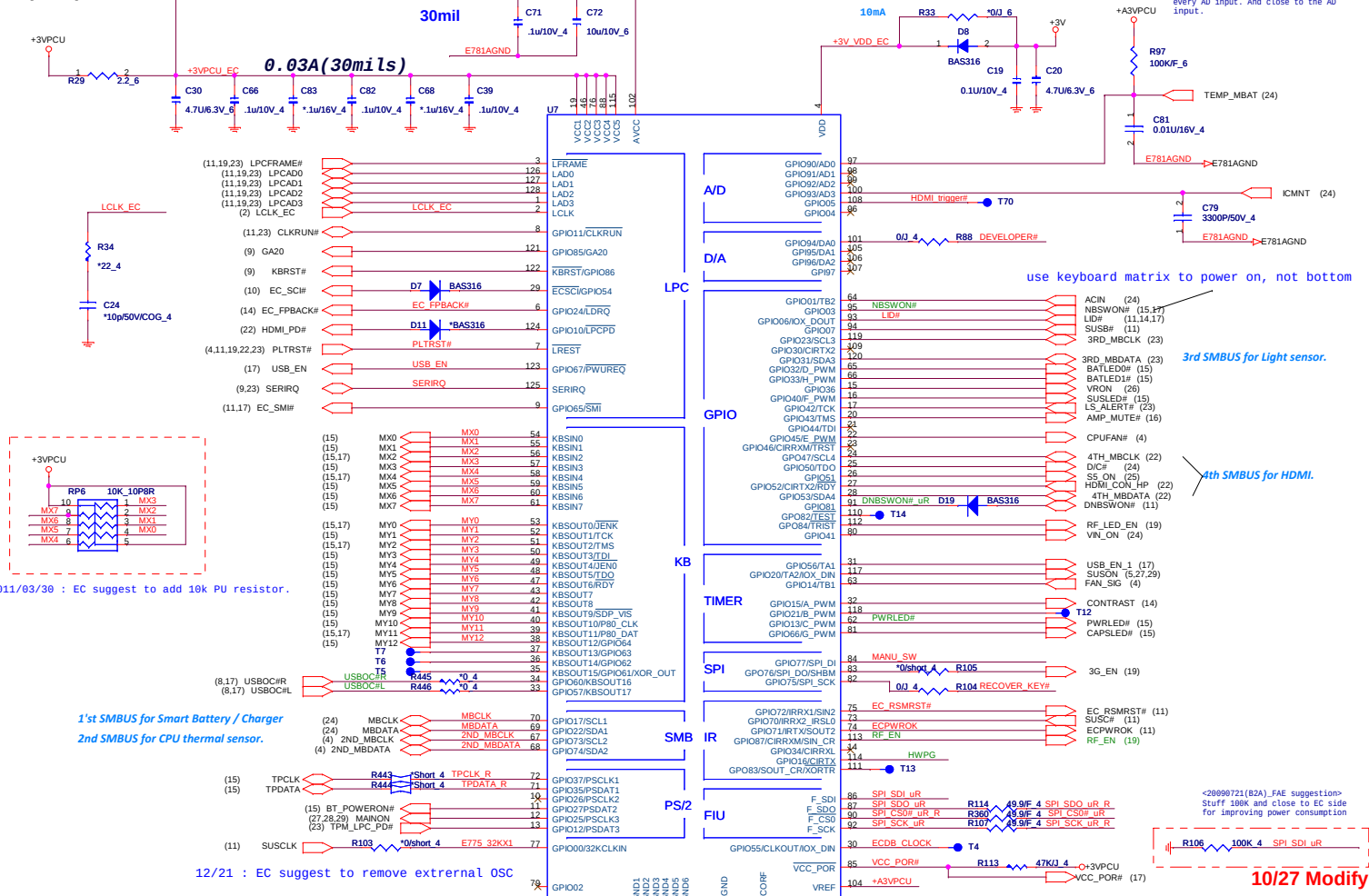


SP1	XD	CD#		
SP2	XD	RDY	SD	WP
SP3	XD	RE#		MS
SP4	XD	CE#	SD	D1
SP5	XD	CLE	SD	D0
SP6	XD	WE#	SD	D7
SP7	XD	WP	SD	D6
SP8	XD	D0	SD	CLK
SP9	XD	D1	SD	D5
SP10	XD	D2	SD	CMD
SP11	XD	D3	SD	D4
SP12	XD	D4	SD	D3
SP13	XD	D5	SD	D2
SP14	XD	D6		MS
	XD	D7		BS

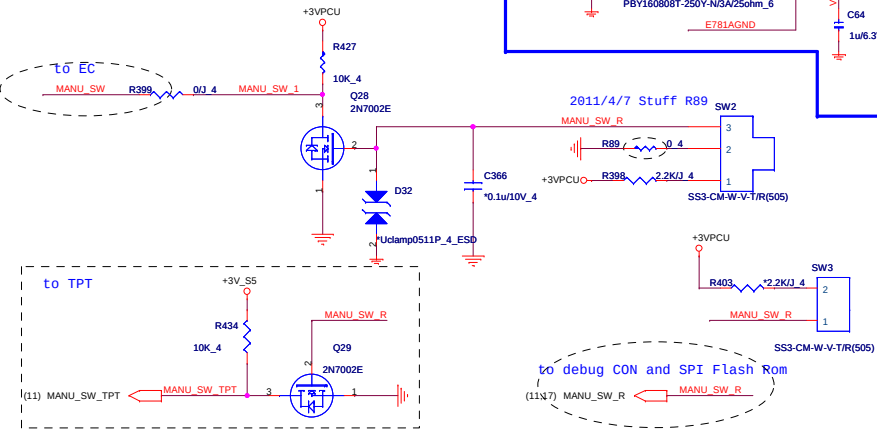
Share Pin



EC(KBC)

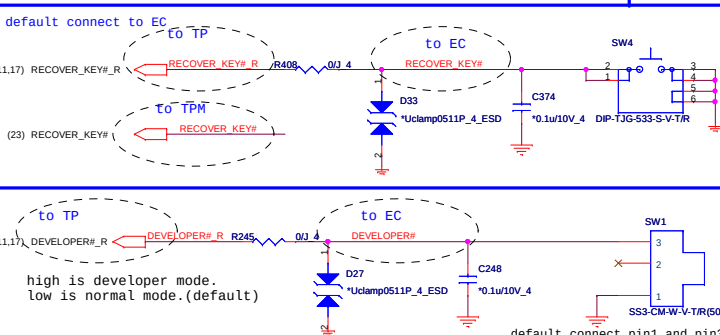


SW2 : connect pin2 and pin3, MANU_SW_R is low.
connect pin1 and pin3, MANU_SW_R is high.(default)

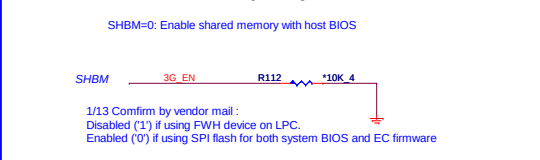


SM BUS ARRANGEMENT TABLE

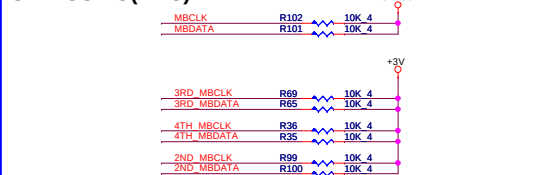
SM Bus 1	Battery
SM Bus 2	CPU thermal sensor
SM Bus 3	Light sensor



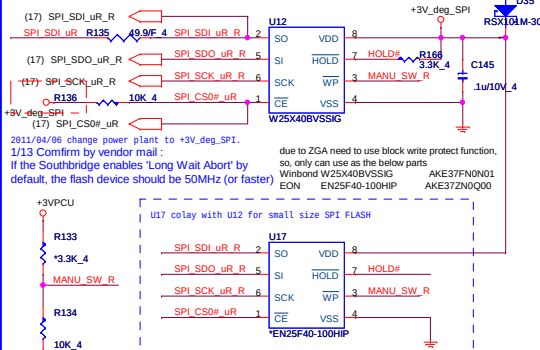
I/O ADDRESS SETTING(KBC)



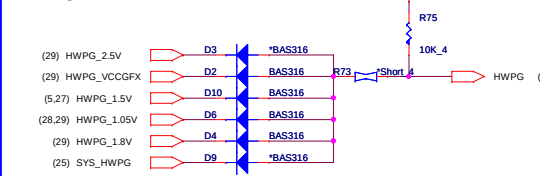
SM BUS PU(KBC)



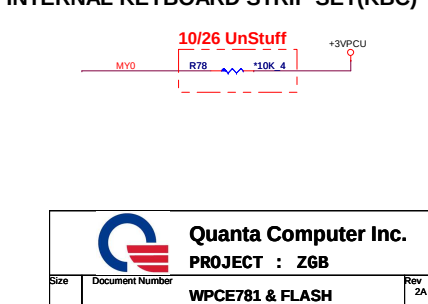
SPI FLASH(KBC)



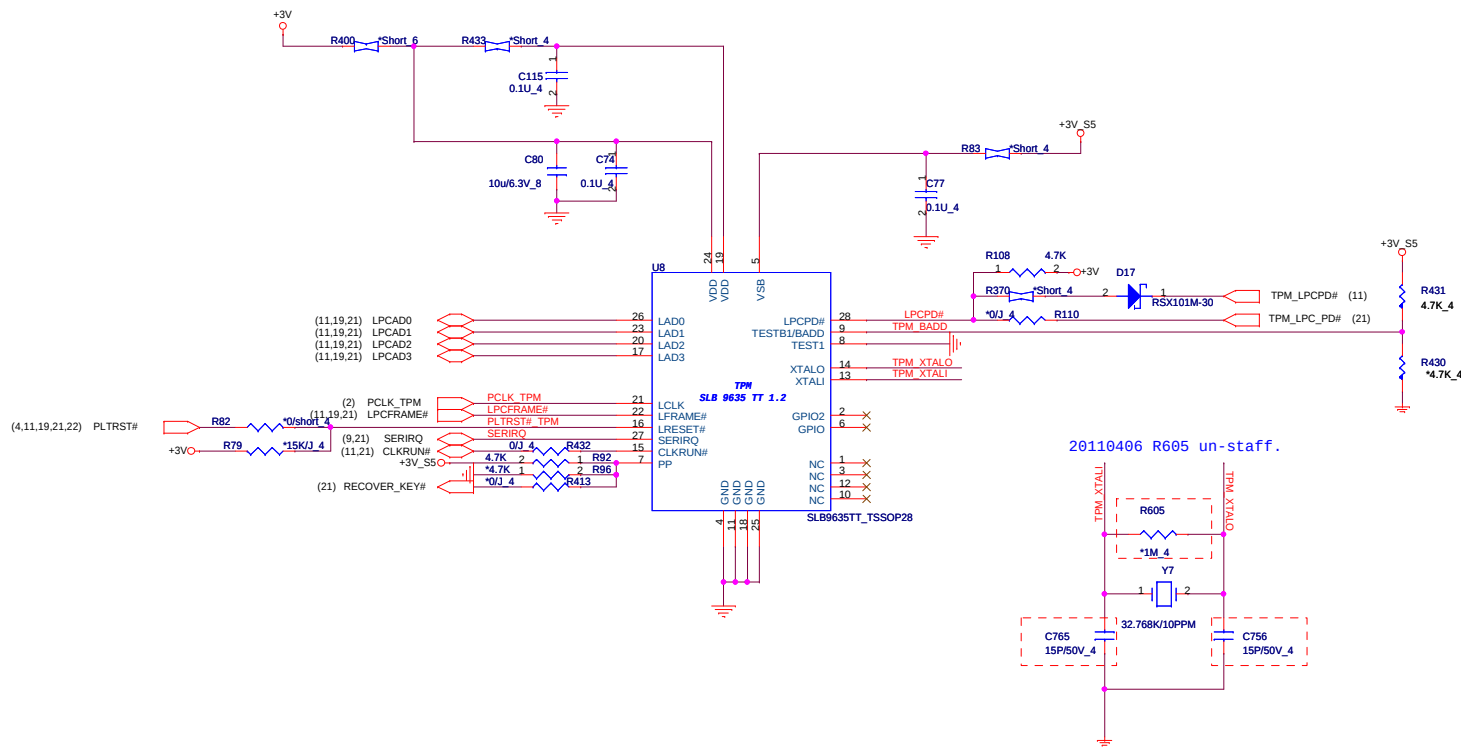
HWPG



INTERNAL KEYBOARD STRIP SET(KBC)



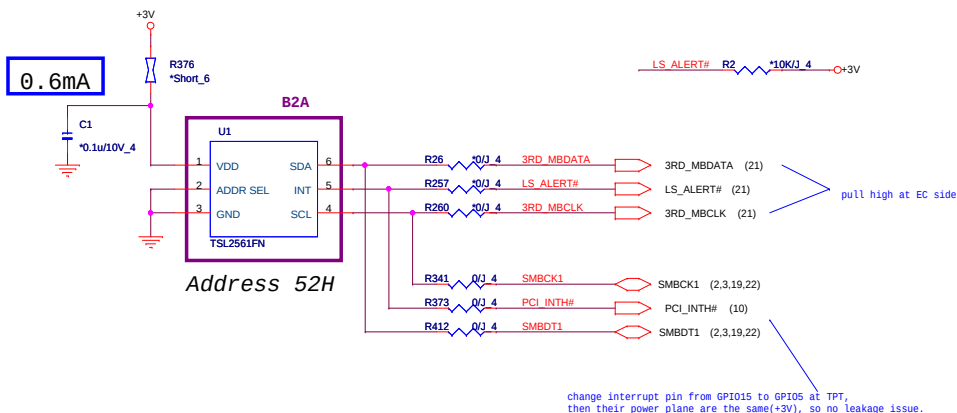
TPM



	Resiger Base Address
BADD=0	2E / 2F
BADD=1 (default)	4E / 4F

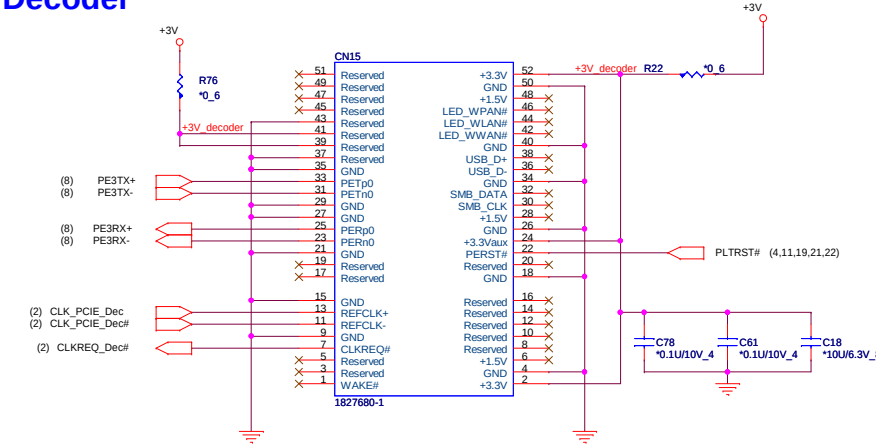
Light Sensor(LSR)

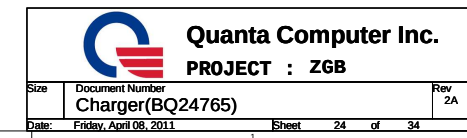
connector to EC, just stuff R2,R26,R257,R260
connector to TPT, just stuff R341,R373,R412

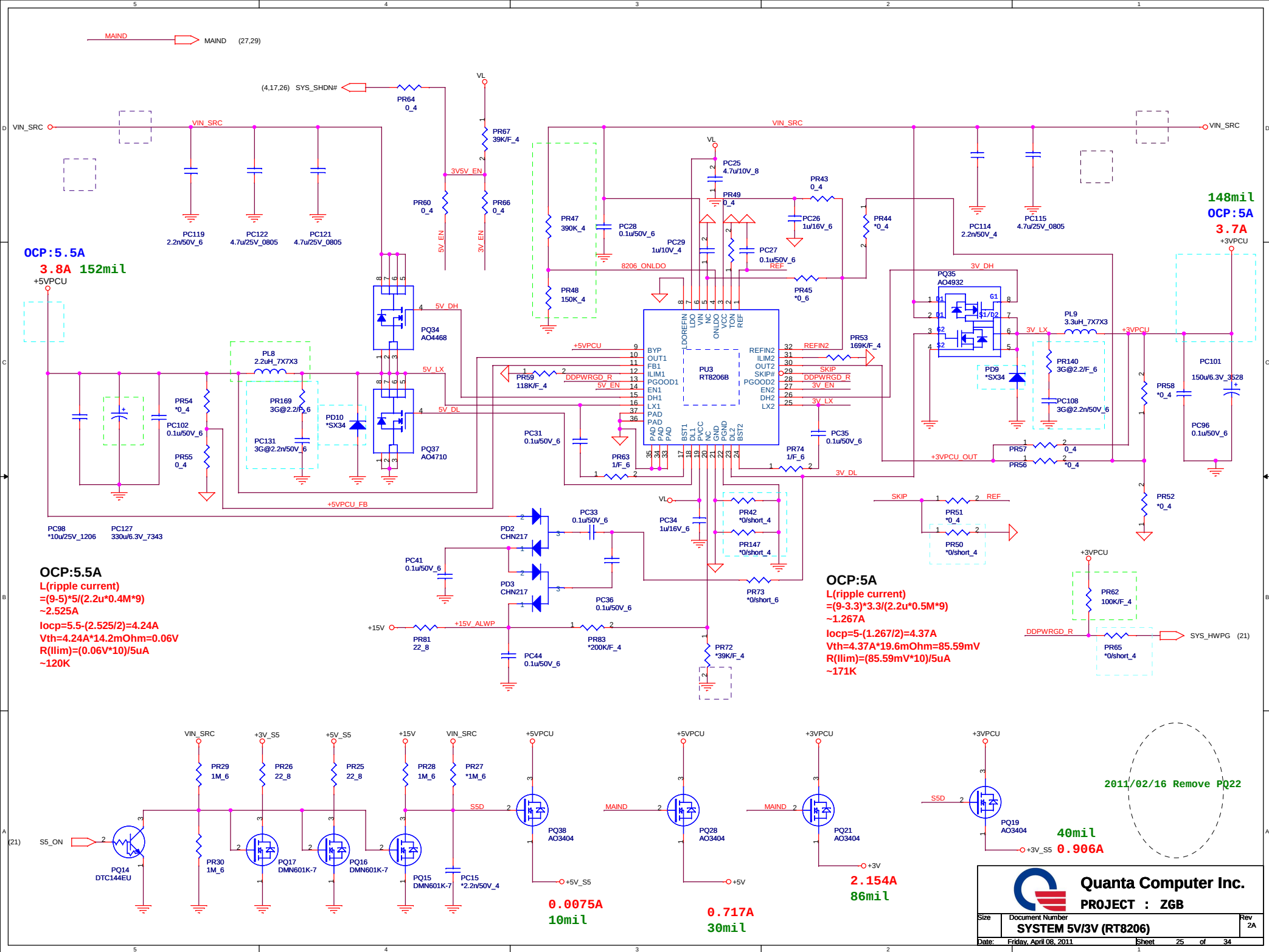


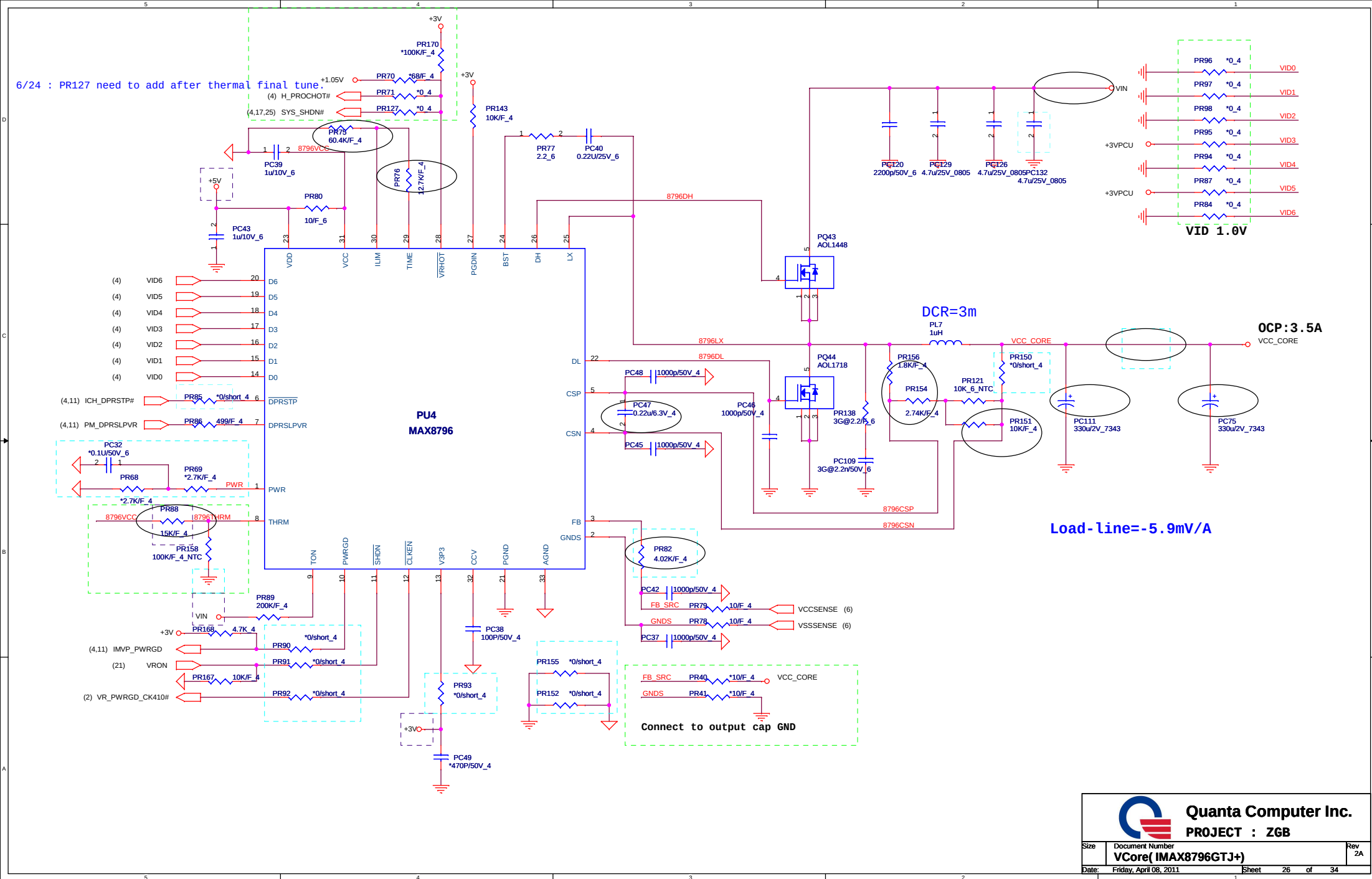
Video Decoder

dont need to stuff first, use innr document to add it.

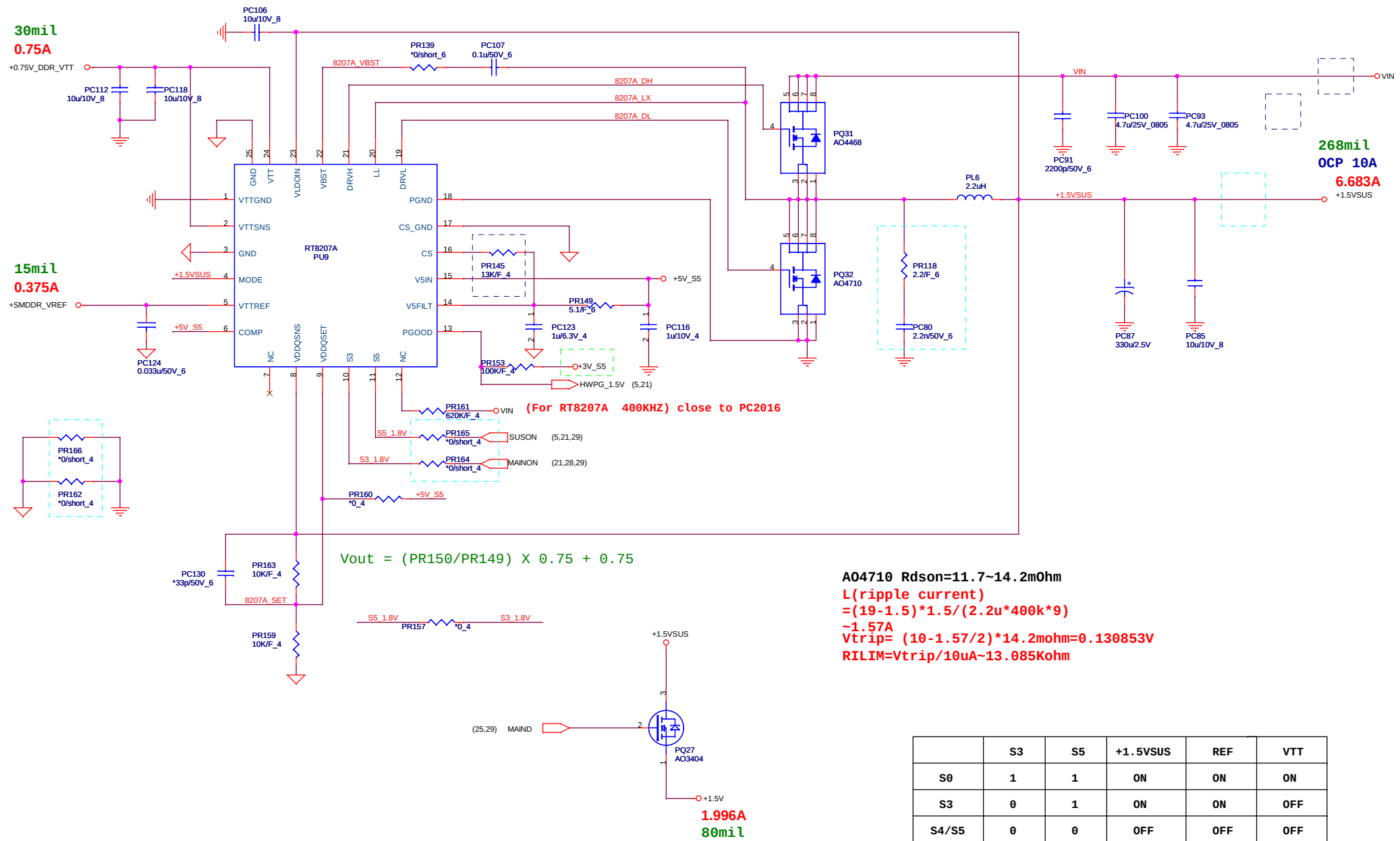






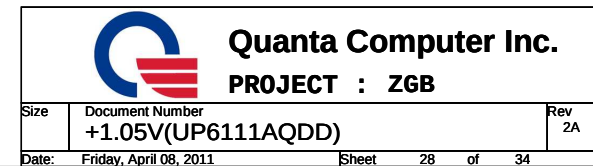


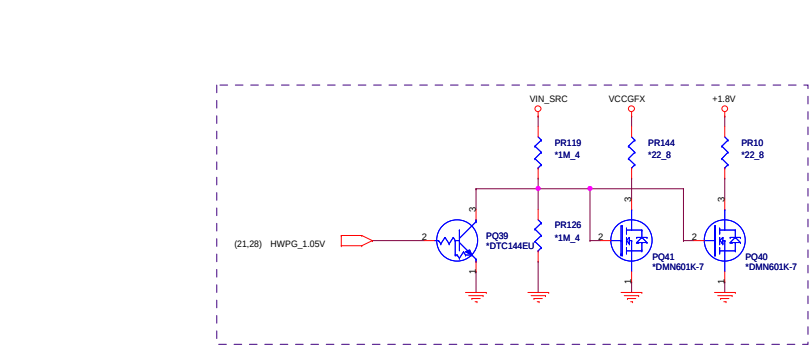
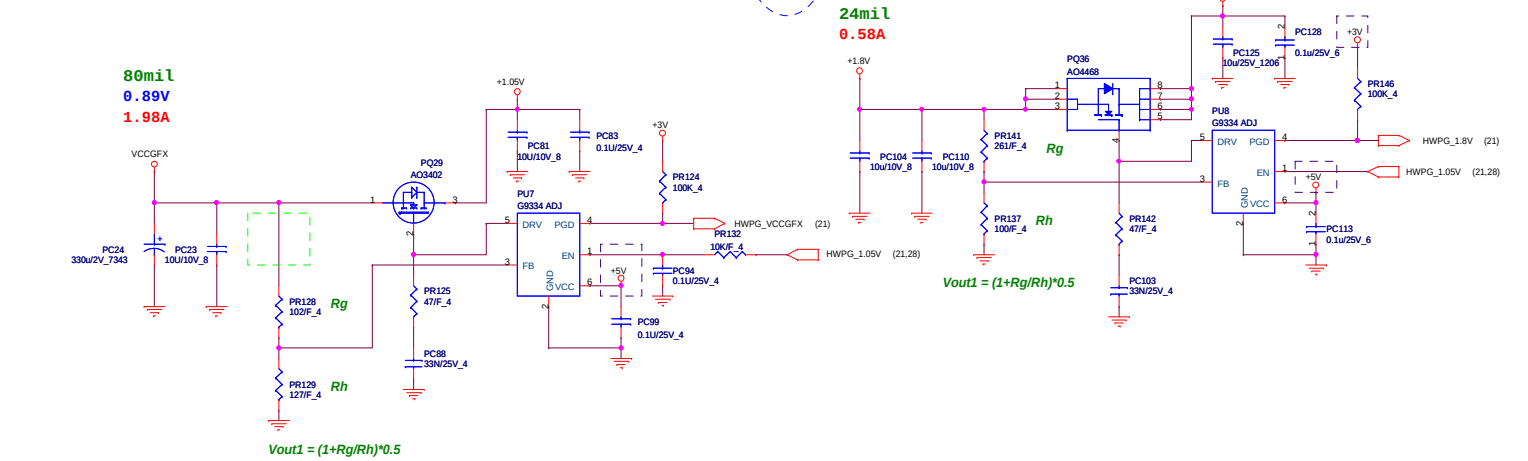
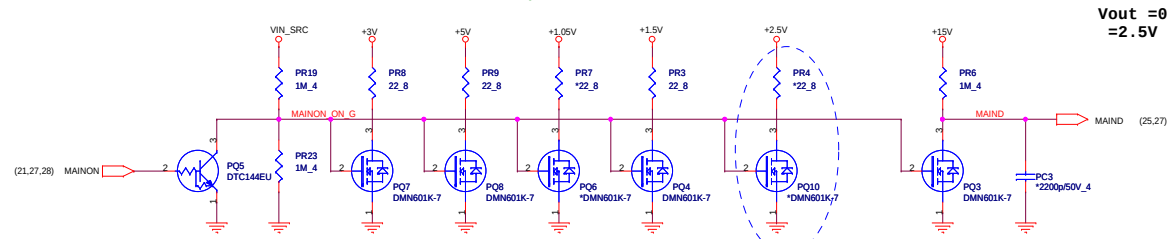
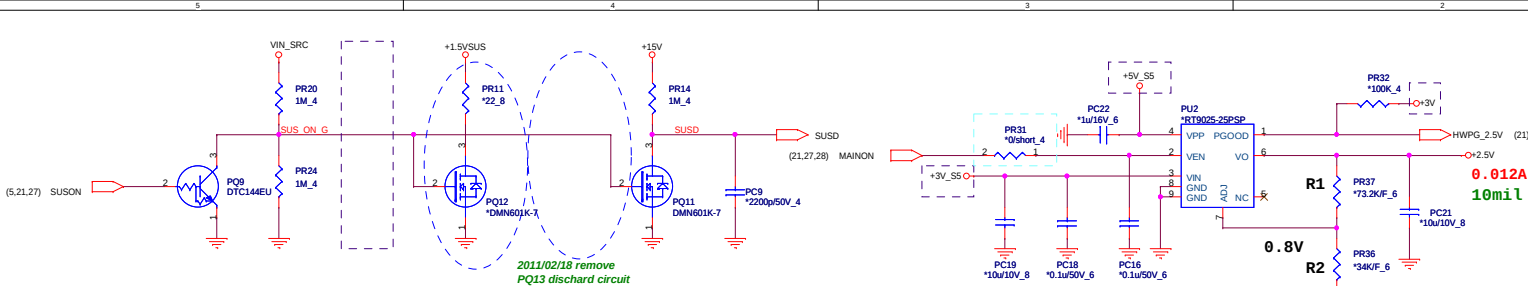
[PWM]

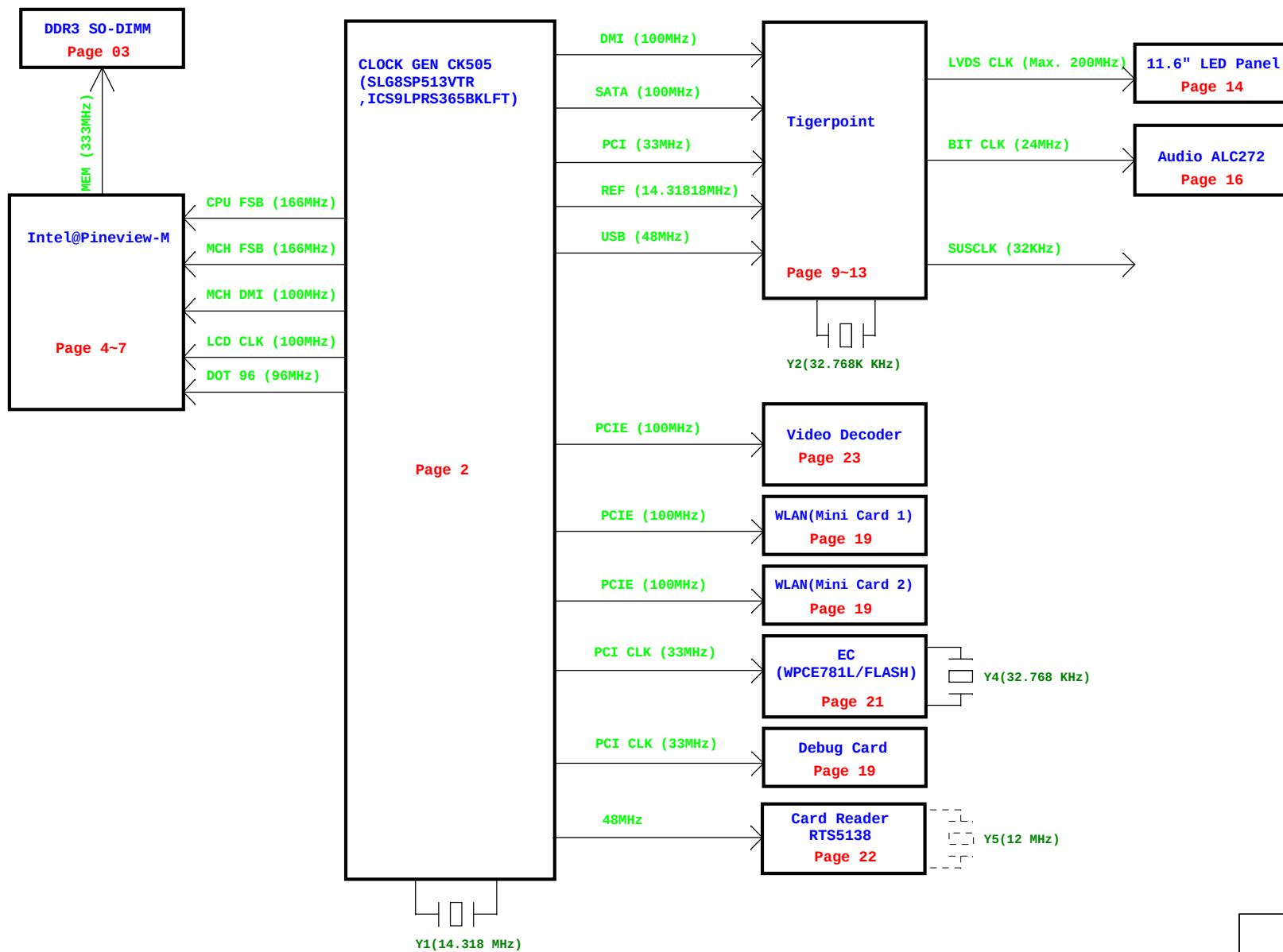


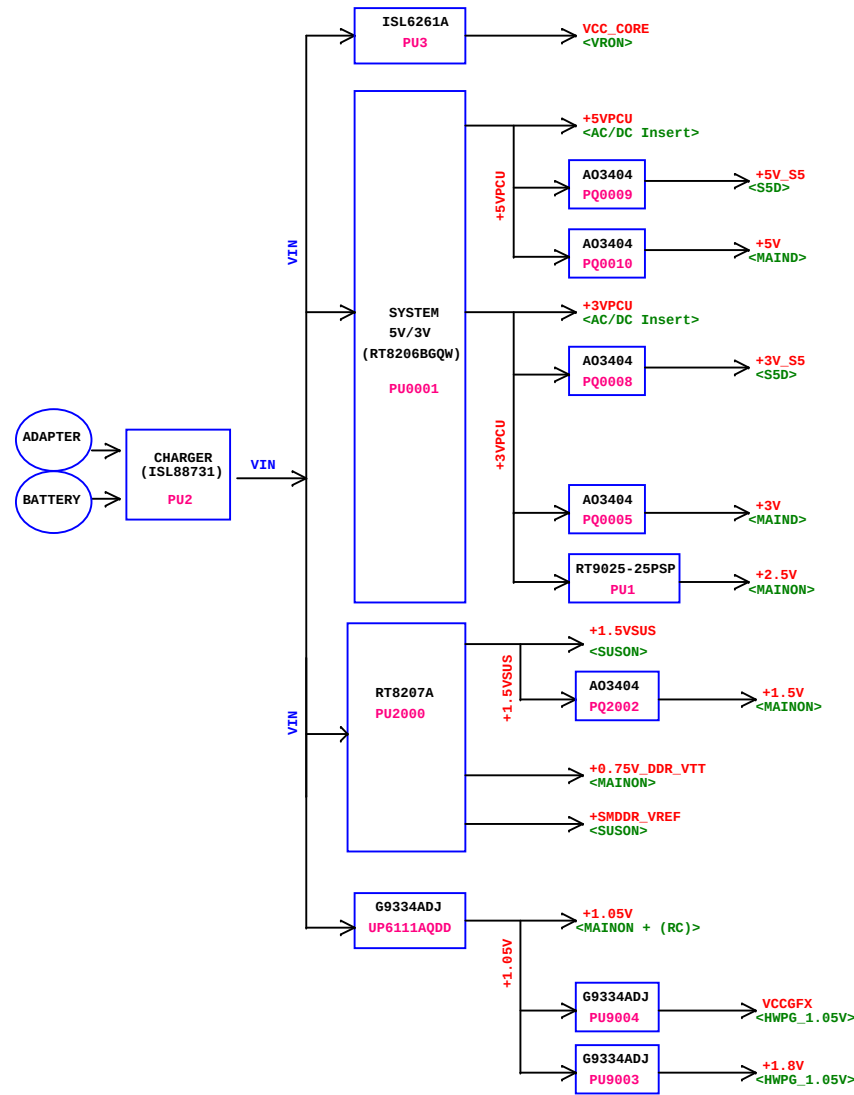
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

L,29) HWPG_1.05V









POWER	Distribution
VIN	LCD Backlight
VCC_CORE	CPU
+5VPCU	USB Connector
+5V_S5	RTC, TPT
+5V	TPT , CRT , TouchPad , Codec , SATA , FAN , HDMI
+3VPCU	RTC, Hall Sensor, Light Sensor, EC, BIOS
+3V_S5	TPT , LAN , LAN EEPROM , RJ45 LED ,3G
+3V	CLK_GEN, CPU, TPT , LCD , CCD, DMIC, BT, Codec, WLAN/Wimax, Card reader, EC, DDR, HDMI
+1.5VSUS	DDR
+1.8V	CPU, HDMI
+1.5V	CPU, TPT
+0.75V_DDR_VTT	DDR
+SMDDR_VREF	CPU, DDR
+1.05V	CLK_GEN , CPU, TPT
VCCGFX	CPU
+2.5V	HDMI

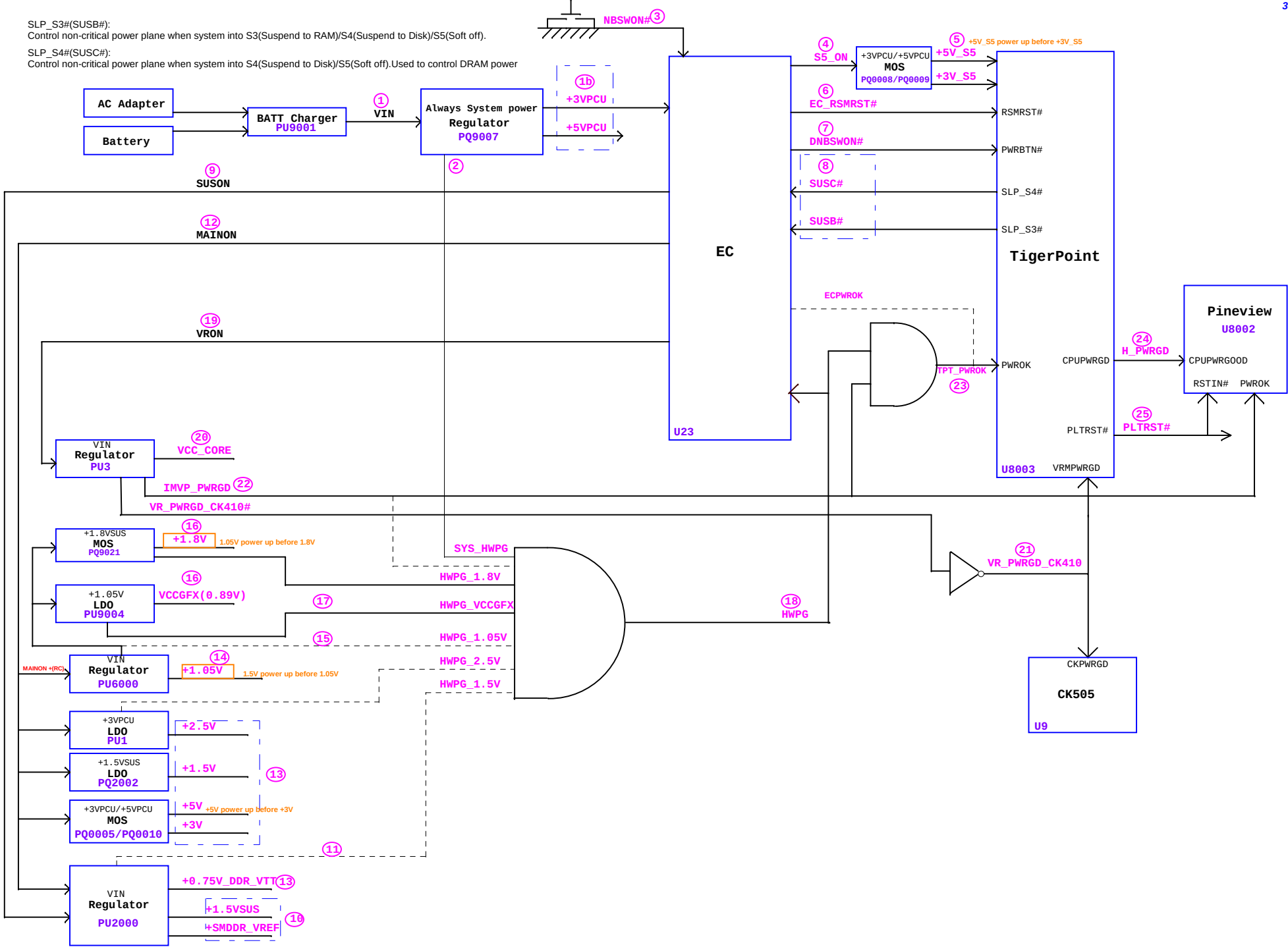


EC SMBUS Table

	Battery	CPU thermal Sensor	Light Sensor
EC781 SDA1 / SCL1 (+3VPCU)	V		
EC781 SDA2 / SCL2 (+3V)		V	
EC781 SDA3 / SCL3 (+3VPCU)			V
Power Plane	+3VPCU	+3V	+3VPCU
MOS CKT (Level shift)	X	X	X

 Quanta Computer Inc. PROJECT : ZGB		Rev 2A
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SYSTEM INFORMATION		
Date:	Friday, April 08, 2011	Sheet 22 of 34

SLP_S3#(SUSB#):
Control non-critical power plane when system into S3(Suspend to RAM)/S4(Suspend to Disk)/S5(Soft off).
SLP_S4#(SUSC#):
Control non-critical power plane when system into S4(Suspend to Disk)/S5(Soft off).Used to control DRAM power



Model	REV	CHANGE LIST	MODEL	ZGB	
ZGB MB				FROM	To
				X	2A
A1 (V1.0)		page 29 :Change PQ33 to PQ43,PQ44 for CPU change to dual core.			
		page 29 : change PC75 from 220uf to 330uf. because dual core CPU need adjustment.			
		page 29 : change PC111 from 330uf to 220uf because dual core CPU need adjustment.			
		page 29 : change PR151 from 1.8k to 10k because dual core CPU need adjustment.			
		page 29 : change PR156 from 1.6k to 1.8k because dual core CPU need adjustment.			
		page 29 : change PR154 from 1.1k to 2.7k because dual core CPU need adjustment.			
		page 29 : change PC47 from 0.1uf to 0.22uf because dual core CPU need adjustment.			
		page 29 : change PR82 from 1.2k to 4.02k because dual core CPU need adjustment.			
		page 29 : change PR88 from 15k to 13k because dual core CPU need adjustment.			
		page 29 : change PR76 from 18k to 12.7k because dual core CPU need adjustment.			
A1 (V1.1)		page 29 : change PR57 from 53.6k to 60.4k because dual core CPU need adjustment.			
		page 2 : change CLK GEN from SLG85P513VTR to SLG8LV631VTR for power saving.			
		page 11: change RTC from connector to socket for SMT request.			
		page 23: TPM change to Infineon replacement R428,R38,R433,C77,R83,R82,R96,R431,C756,C765,Y7,R432			
		page 29 : change net name VCC_CORE to VCC_CORE_1 for net name adjustment.			
		page 17 : Add debug port 40pin for customer request.(2011/02/27)			
		page 09 : Delete 10pin debug port and add test point on PCH debug pin.(2011/01/31)			
		page 15 : Base on customer request Reserve BT circuit.(2011/02/01)			
		page 17: CN23 add test point Pin7,8,11,12,13,21,27,28,29,35,36,37,38,39 for NC pin.(2011/02/01)			
		page 21: Add 0ohm on SMB clk and SMB Data for test use.(2011/02/01)			
A1 (V1.2)		page 15: Add PCH SMB CLK and data to TP SMB clk and data and additional MOS to prevent electric leakage for reserve test use.(2011/02/01)			
		page 14: Add +5V CCD power for OV9726 CCD and reserve +3V CCD power.(2011/02/01)			
		page 14: Change to +3V CCD power and reserve +5V CCD power.(2011/02/01)			
		page 23 : 1.remove break net U8.10 to U8.24. 2.R96->NI, change R92 to pull to +3V_S5 (leave NI)3.populate Y7C756/C765/R605. R606->1M, C756/C765->12pF4.populate R428, populate R431. Change R431 pull to +3V_S5.5.add populated 0R jumper U8.28 to U20.G22, change R108 pullup to +3V_S5			
		page 17: R359-361, R363, R366 are not required remove CN23 Pin7,8,11,12,13 connector to KBC EC ROM. CN23 Pin22 connector to SYS_SHDN#(2011/02/10)			
		page 14 : add resistor between Rom and Tigerpoint of U20 pin M8(2011/02/10)			
		page 21 : add resistor between SPI Rom and KBC of U7pin 90.Remove 0ohm on U7 pin71.72. because separate I2C circuit.2011/02/10)			
		page 15 : Add a connector and circuit for TPD I2C circuit, but SPEC acer not yet confirm.(2011/02/10)			
		page 15 : Follow up synaptic pin define modify TPD I2C circuit.(2011/02/11)			
		Pin 6 => CLK/Pin 5 => GND/Pin 4 => DAT/Pin 3 => VDD/Pin 2 => NC/Pin 1 => INT(interrupt)			
A1 (V1.3)		page 17: Change CN23 Pin15 PCH_GPIO24. 0 net name to PCH_GPIO24(2011/02/11)			
		page 23: Add one 0R ahead U1 pin1.R76 and R22 change from 0402 to 0603 for power consumption measure.(2011/02/11)			
		page 23: LPCPD R108 change +3V_S5 to +3V well.Add diode between U20.G22 and U8.28 to ensure well isolation.(2011/02/14)			
		page 15 : 1.Remove R439,L37 because not use +5VSUS option.2.Change CN3 from 4pin to 6pin 3.Add CN8 for PS2 TPD option.(2011/02/15)			
		page 02 : C768, C774 and C772 change from 100u/10V_8 to 100u/6.3V_6. (2011/02/15)			
		page 17 : C268, C266 and C297 change from 100u/6.3V_3528 to 100u/6.3V_3216.(2011/02/15)			
		page 11 : D34 change to 30V 1A diode.(2011/02/15)			
		page 17 : D35 change to 30V 1A diode and Delet D36 only use one diode.D4/6/10 remove NI.(2011/02/15)			
		page 15 : Follow up pin define modify TPD I2C circuit.(2011/02/15)			
		Pin 6 => VDD/Pin 5 => SCL/Pin 4 => SDA/Pin 3 => HINT/Pin 2 => SINT/Pin 1 => GND			
A1 (V1.4)		page 25 : Remove PQ42 because not +5VSUS supply(2011/02/18)			
		page 12 : change R209 and R194 from 0603 to 0805 for current limitation.(2011/02/18)			
		page 11 : Change U20 A24 net name from MBID2 to SNIT_TP.U20 D19 net name change PCH_GPIO26 to HINT_TP, for TP I2C interrup. CN3 pin3 change net to HINT_TP and pull up +3V_S5,PCH_GPIO39 leave test point.			
		page 08 : R294 and R285 to remove NI for PCH control.			
		page 21 : R112 leave NI.R97 pull up change to +A3PCU power wall,remove U7 pin96 net name because dulpicate, add NI 0 ohm on U7 PIN34/33 for EC option.			
		page 11 : R277,R276 from 8.2k change to 10k ,R195/R188 10k to 8.2k pull up following intel spec.			
		page 17 : Update CN23 P/N and footprint for pich0.5.			
		page 21 : R102/R101/R69/R65/R36/R35/R99/R100 change to 4.7k 0402 for supplier NVO suggestion.			
		page 23 : D17 change diode to 30V 1A.			
		page 15 : Swap CN3 pin define			
A1 (V1.6)		Pin 1 => VDD/Pin 2 => SCL/Pin 3 => SDA/Pin 4 => HINT/Pin 5 => SINT/Pin 6 => GND			
		page 23 : U8_PP pull down to GND.(2011/02/18)			
		page 11 : Change TPD power well to +3V_S5.(2011/02/18)			
		page 25 : Remove PQ22 +3VSUS power well.(2011/02/18)			
		page 29 : Remove PQ13 and PR12 discharge circuit.(2011/02/18)			
		page 21 : R102/R101/R69/R65/R36/R35/R99/R100 change to 10k 0402 for supplier NVO suggestion.			
		Change All +3V/SU to +3V_S5 power plant			
		page 22 : Remove LVDS bypass resistor (cancel LVDS stub trace)			
		page 16 : Change C163 from 10u to 2.2uf (follow Codec FAE suggestion.)			
		page 03 : Add EMI CAP C258,C261,C260,C259 100pf.(EMI request.)			
B1 (V2.0)		page 11/15 : Remove I2C criort SNIT/HNIT and Change RTC charge limitation resistor to prevent charge current to large,R415 and R422. unstuff U14 and add R207 0ohm.(Follow Google commend to use 6pin P/S2 touch pad.)			
		page 15 : Remove CN8 TP 4pin.(Following Google suggestion use 6pin connector.)			
		CN6 from DFHD05MRD98 to DFWF05MRD42 and BT power plant from +3VPUC to +3V_S5.(Follow acer AVAP to use new BT ,so we have to use new connector. Correct wrong BT power supply.)			
		page 16 : R16/R17 add 0ohm for EMI.(EMI request)			
		page 26 : Remove vcore jump (those R for power consumption measurement, we won't use they after A stage.)			
		R615,R176,R148,R351,R280,R279,R281,R298,R207,R202,L30,R194,R329,R141,R256,R46,R56,R44,R254,R255, R125,R124,R131,R17,R16,R258,R324, R98,R256,R210,R337,R287,R196,R292,R293,R198,R199,R217,R216,26 4,R382,R73,R443,R444,R74,R78,R400,R433,R83,R370,R376, (Change 0ohm to short pad.(those R for power)consumption measurement, we won't use they after A stage.)			
		page 15 : add R261 and C410 for BT soft star.			
		page 11 : change R152/210 power plant from +3V to +3V_deg.(for google suggestion.)			
		page 21 : Add RP6 PU 10K. (for keyboard lose key issue.)			
		page 21 : R136 change power plant from +3VPUC to +3V_deg_SPI.(for google suggestion.)			
A1 (V1.7)		page 22 : Add C271/272/273/262/270 0.1uf.(for EMI suggestion)			
		page 22 : Remove RN2/34/5 and L3/4/5/6 (avoid HDMI stub trace)			
		page 23 : R605 un-staff.(for supplier suggestion because internal Rd 1Mohm.)			
		page 08 : PE2RX+/- and PE2TX+/- swap to PE1RX+/- and PE1TX+/-.(WLAN change from PCIE2 to PCIE1. So BIOS can turn off PCIE2 alone and save power consumption)			
		page 19 : PE2CLK+/- net name change to PE1CLK+/-.(PE2 already swap to PE1 so change net name.)			
		page 11 : C96 change power plant to +3V_deg.(for google suggestion.)			
		page 11 : Change R283 from short-pad to 0ohm and unstuff U19 (AND gate) to increase fan-out (There are many devices use PLTRST#, TPT may not drive them so use AND gate to fan out)			
		page 21 : Add R89 0ohm on SW2.2.(for google suggestion.reserve 0ohm.)			
		page 8 : Change USB0CN1 from OC# to C#0 base on usb port.(Wrong assign for USB OC change to correct)			
		page 11 : Change U19 Pin1 to Deg_RST# pull 4.7k to +3V.(for google suggestion control PLTRST#)			
B1 (V2.1)		page 17 : Change CN23 Pin19 net name from PLTRST# to DEG_RST#.			
B1 (V2.2)					
B1 (V2.3)					