KL2A Intel Huron River Platform with Discrete GFX

01

FAN / THERMAL
EMC2103-2

DDRIII-SODIMM1
PG 14

DDRIII-SODIMM2
PG 15

Dual Channel DDR3
800/1067 1.5V

DDR SYSTEM MEMORY

<MCH Process>
SandyBridge 0.61

rPGA 988

PCI-E

Graphics Interfaces

PG 4,5,6,7

FDI DMI

PCI-Express

AMD (40nm)

Capilano 969p

27MHz

PG 16,17,18,19,20,21,22

DMIX4

FDI DMI

SATA - HDD
PG 29

SATA - CD-ROM
PG 29

USB+eSATA
PG 29

SATA1 150MB

SATA3 150MB

SATA4 150MB

CougarPoint 0.7

PCH

PG 8,9,10,11,12,13

INT_HDMI

INT_CRT

INT_LVDS

HDMI CON
PG 23

CRT
PG 25

LCD CONN
PG 24

USB2.0

Port 5,6,7
USB2.0 Ports X3
PG 30

Port 1
BlueTooth
PG 30

Port 3,4
Mini PCI-E Card X 2
PG 32

Speaker
PG 27

Audio Jack
(External MIC)
PG 27

Head-Phone Jack
+ SPDIF
PG 27

AUDIO CODEC
ALC272
PG 28

IHDA

Camera + D-MIC
PG 26

USB2.0

PCI-E

X2
Mini PCI-E Card
(WLAN/ WWAN)
PAGE 30

X1
LAN
Broadcom
(10/100/1G LAN)
BCM57790/57780
PAGE 27

25MHz

X1
Card Reader
JMB385/387
PAGE 31

7-IN-1 Card
Reader CONN
PG 31

32.768KHz

LPC

EC
IT8518
PAGE 36

Ambient
LIGHT SENSOR
PG 35

REGULATOR (DDR3)
1.5VSUS, 0.75VSMDDR_VTERM,1.5V
1.5V_GPU,1.5V_CPU

REGULATOR
+1.05V_VTT,+1.8V

DC/DC
3VPCU, 5VPCU, +15V
PG 42

CPU Core
PG 43

VGA Core Discrete
PG 44

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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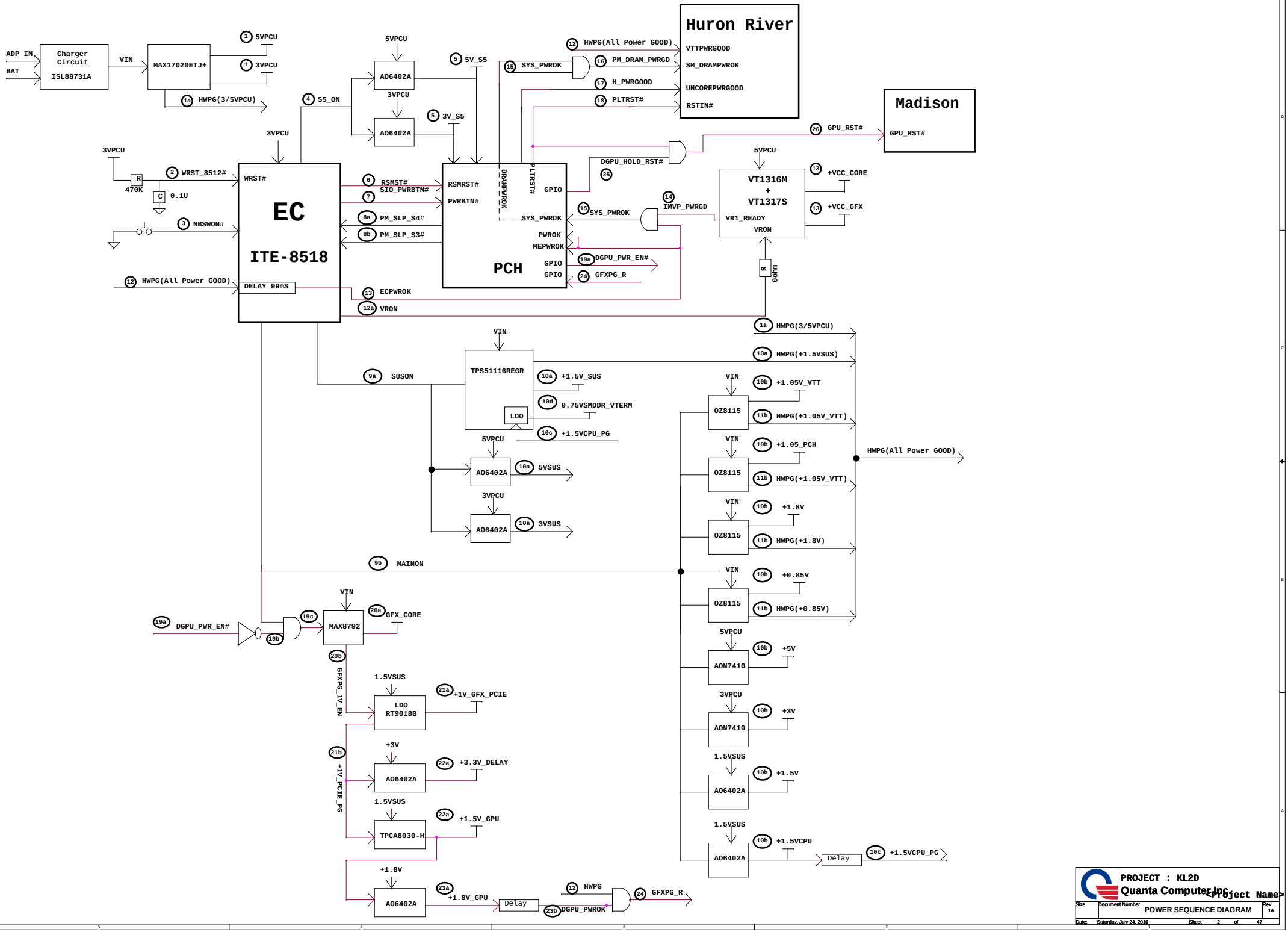

PROJECT : KL2D
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<Project Name>

Size	Document Number	Rev
	POWER SEQUENCE DIAGRAM	1A

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CLK Gen(CLK)

03

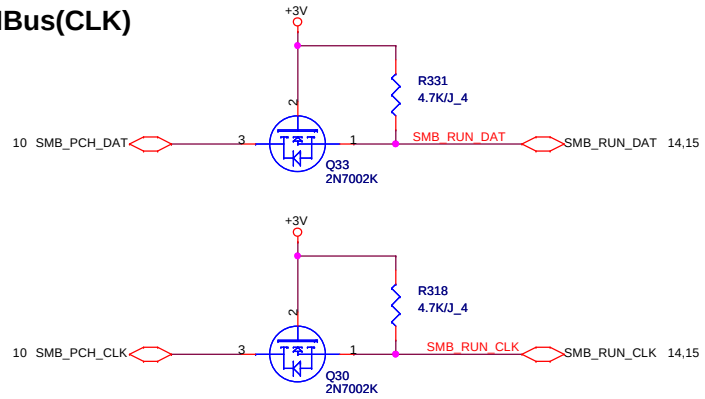
02/20 DEL for Pre-ES1

CPU_CLK select(CLK)

02/20 DEL for Pre-ES1

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus(CLK)



PROJECT : KL2D
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Size	Document Number	Rev
	Clock Generator	1A

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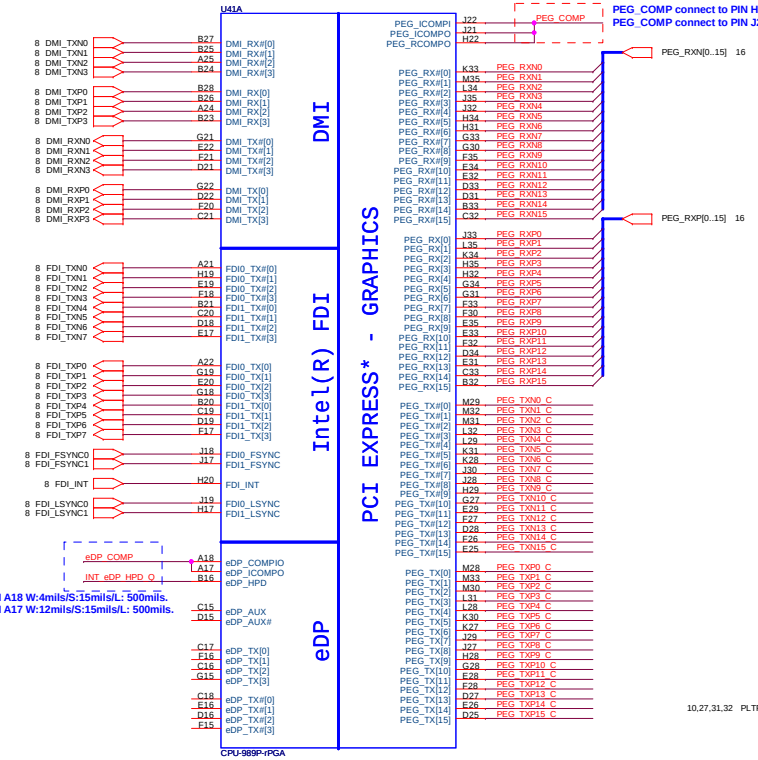
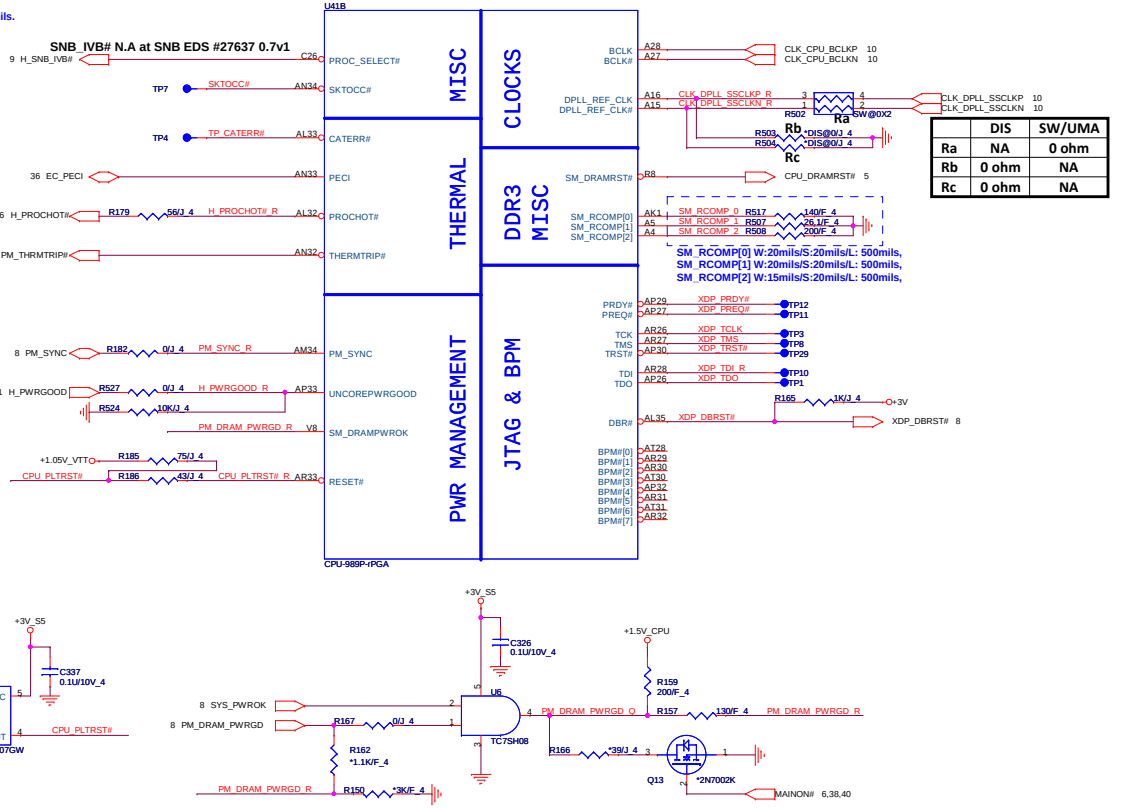
Sandy Bridge Processor (DMI,PEG,FDI)



PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

Sandy Bridge Processor (CLK,MISC,JTAG)

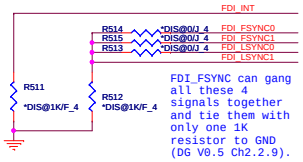


SNB_IVB# N.A at SNB EDS #27637 0.7v1

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

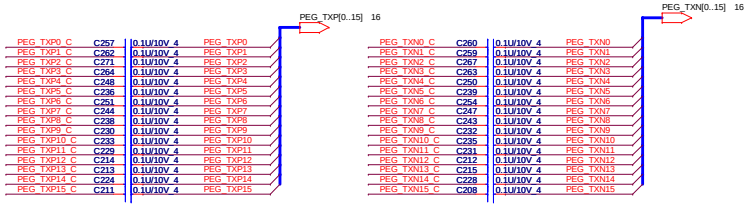
	DIS	SW/UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

FDI Disable



FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 (UMA Non-stuff)

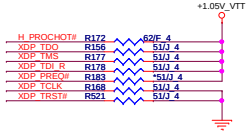


DP & PEG Compensation

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils
typical impedance = 14.5 mohms

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Processor pull-up(CPU)



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	Sandy Bridge 1/4	1A

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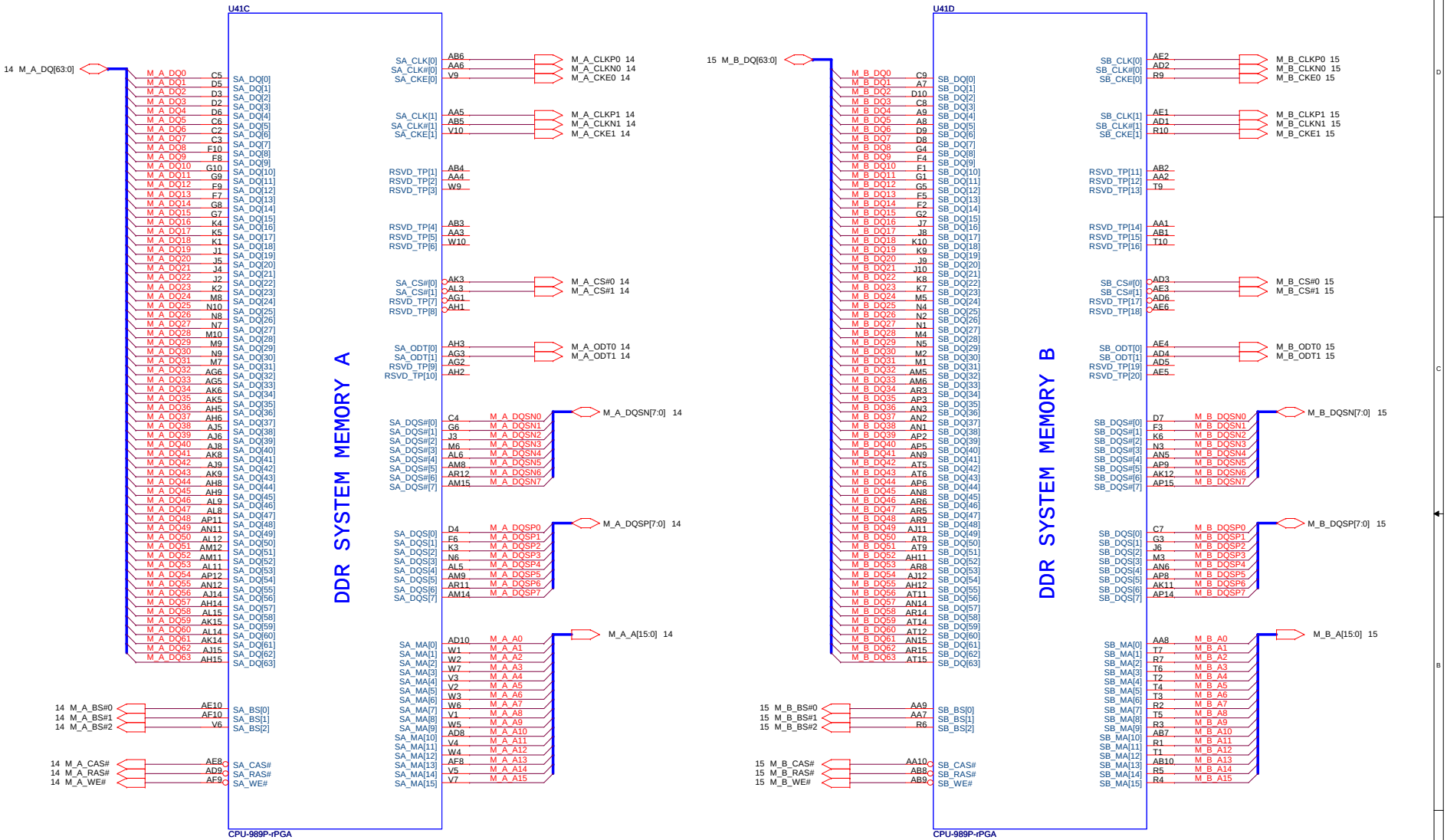
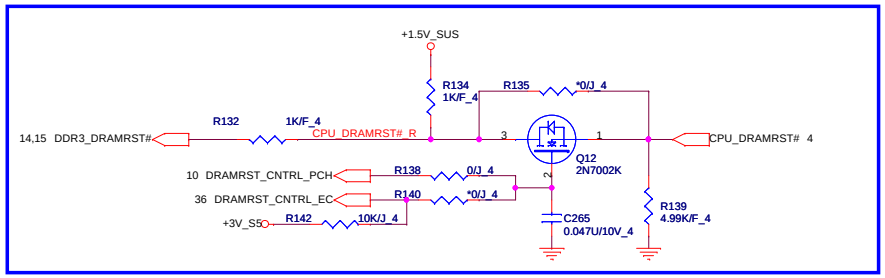
04

Sandy Bridge Processor (DDR3)





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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

CPU Core Power
SNB 45W:55A
22uF x 32
22uF x 3 (Non-stuff)

CPU VTT
SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-stuff)

CPU VGT
SNB 45W:22A
22uF x 12
22uF x 4 (Reserved)

CPU VCCPL
SNB 45W:3A
330uF/7mohm x 1
10uF x 1
1uF x 2

CPU MCH
SNB 45W: 5A
330uF/6mohm x 1
10uF x 6

CPU SA
SNB 45W: 6A
330uF/7mohm x 1
10uF x 3

POWER
CORE SUPPLY
PEG AND DDR
SVID
SENSE LINES
GRAPHICS
DDR3 -1.5V RAILS
VREF
SENSE LINES
SA RAIL
1.8V RAIL
MISC

U41F
U41G
CPU-989P-rPGA

Reserved

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

22uF (Reserved)

Ra	DIS	SW
Ra	0 ohm	NA

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
Close to VR
Place PU resistor close to CPU
SVID DATA
Close to VR
Place PU resistor close to CPU
SVID ALERT

4.5A
3/26 DB add for Intel. Placement close to CPU.

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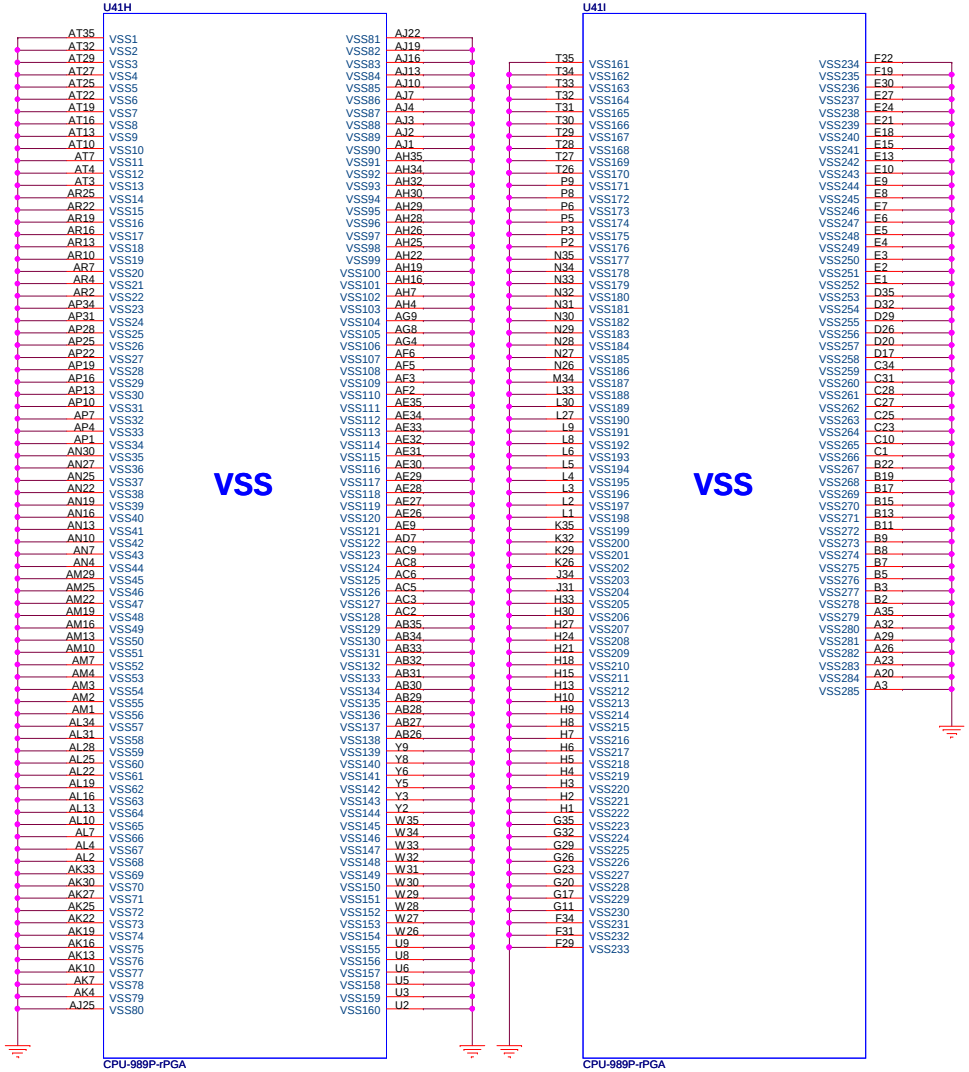
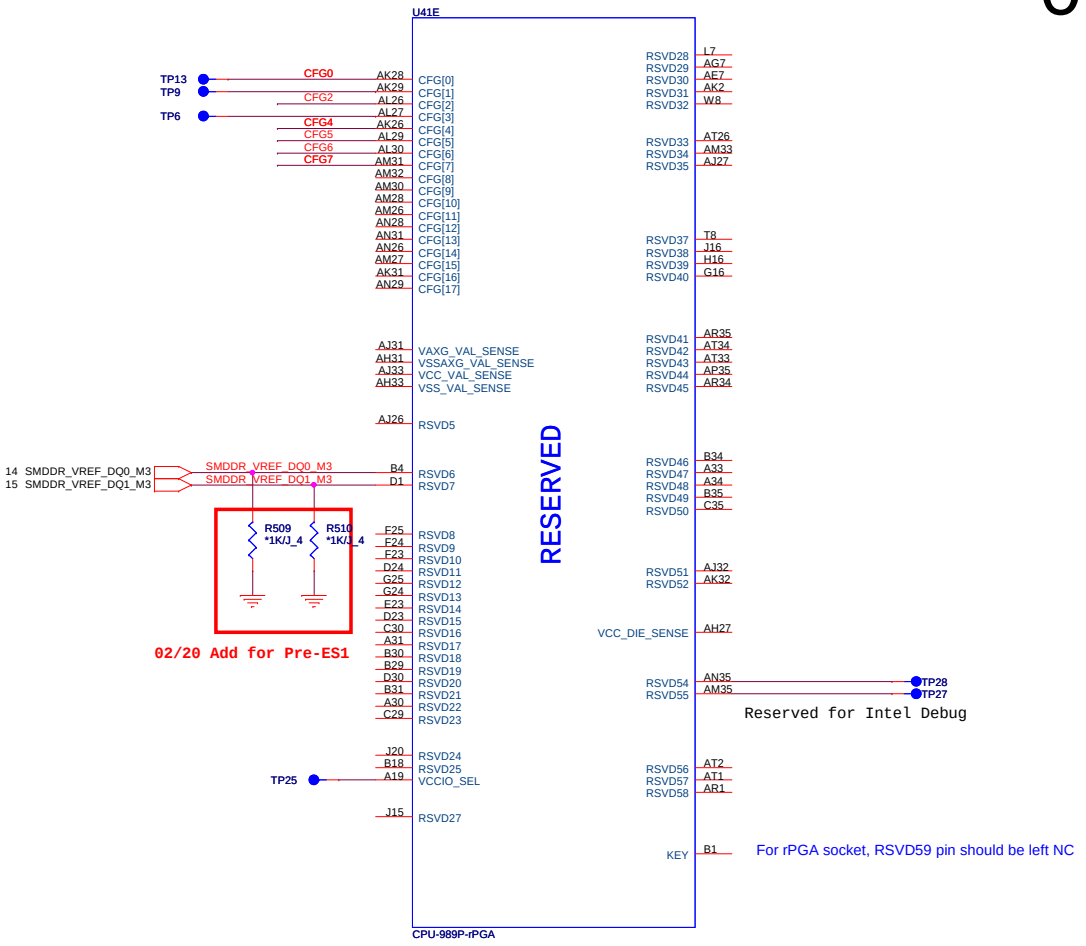
Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)

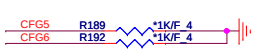
07



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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	Sandy Bridge 4/4	1A

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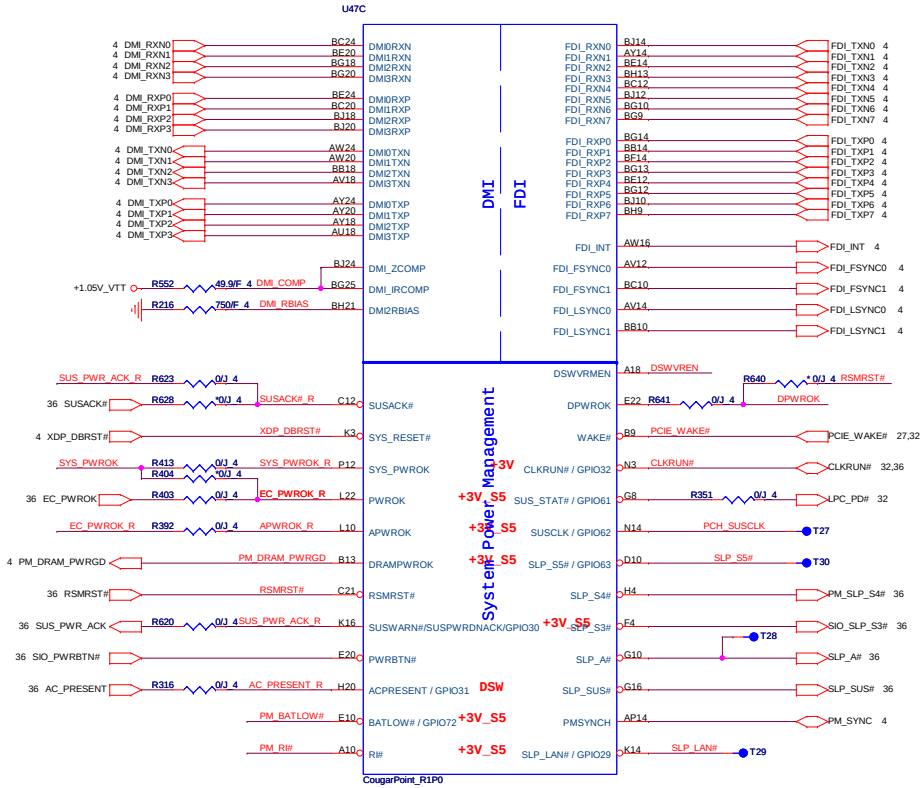
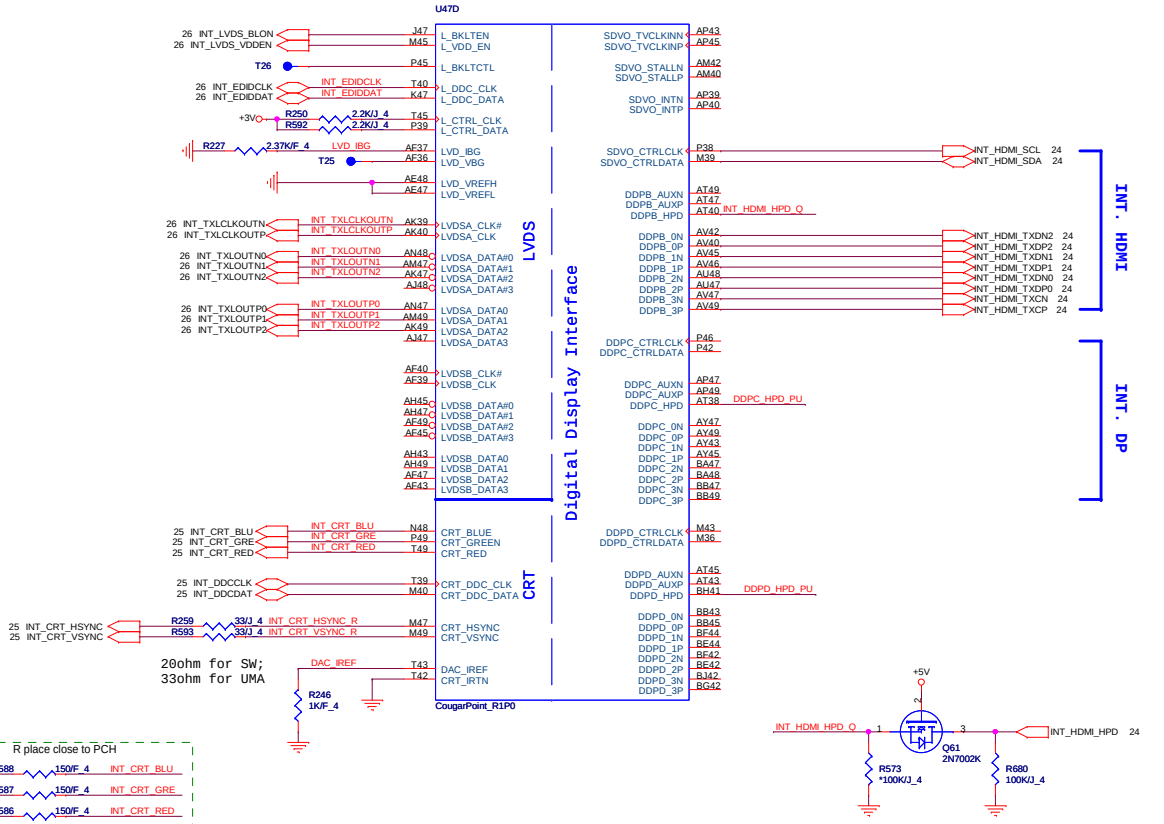
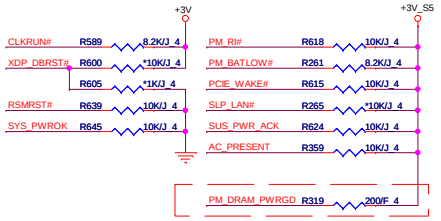
Cougar Point (DMI,FDI,PM)



Cougar Point (LVDS,DDI)

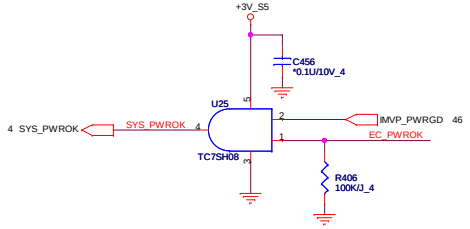


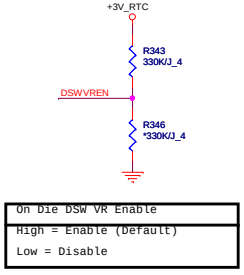
PCH Pull-high/low(CLG)



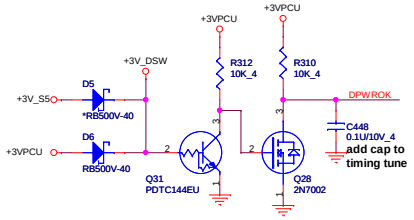
3/16 Change topology; 200ohm PU to +3V_S5

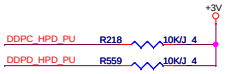
System PWR_OK(CLG)





DPWROK FOR DSW





Follow PDG eDP disable guide

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	Cougar Point 1/6	1A
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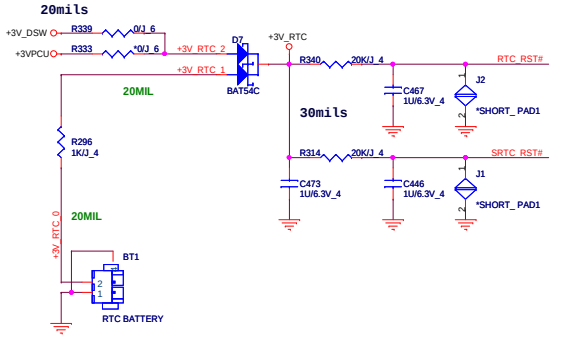
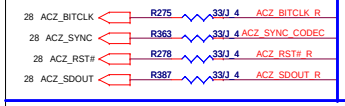
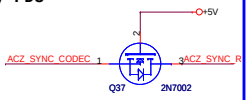
RTC Circuitry(RTC)



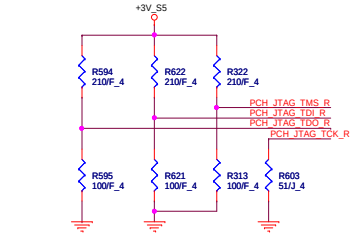
HDA Bus(CLG)



To Separate Codec Sync by PD3

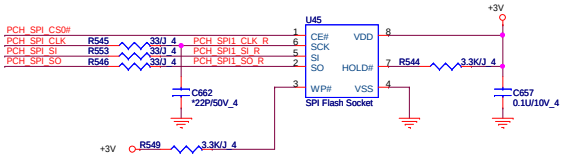


PCH JTAG Debug (CLG)



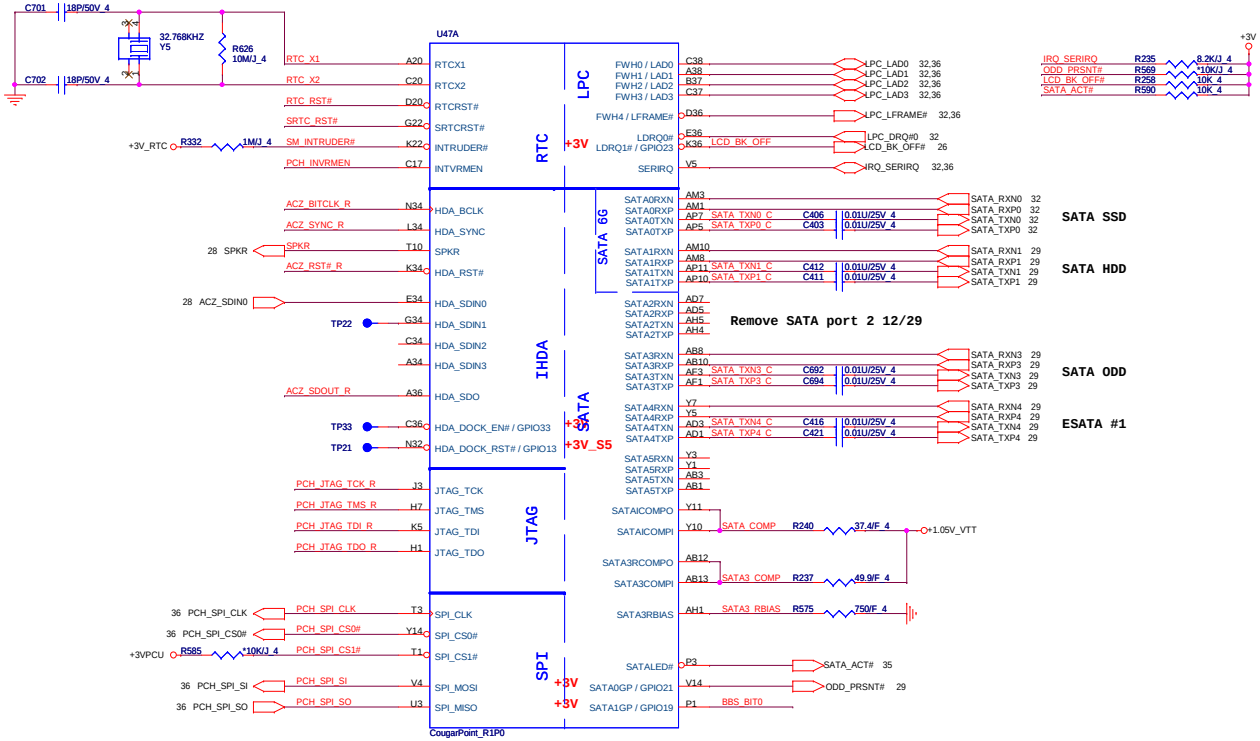
PCH Dual SPI (CLG)

MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00
Socket: DG008000031



PCH2(CLG)

Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R584 *1K/J_4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R608 *1K/J_4 PCI_GNT3# 10
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R311 330K/J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R606 *1K/J_4 BBS_BIT1 10 R591 *1K/J_4 BBS_BIT0
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5 R390 *1K/J_4 ACZ_SDOUT_R
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R566 2.2K/J_4 +1.8V R570 4.7K/J_4 DF_TVS 11 H_SNB_IVB# 4
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R394 *1K/J_4 PLL_ODVR_EN 11,36
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R355 1K/J_4 ACZ_SYNC_R
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R555 *1K/J_4 PCH_SPI_SI
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)	

PROJECT : KL2D
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	Cougar Point 2/6	1A

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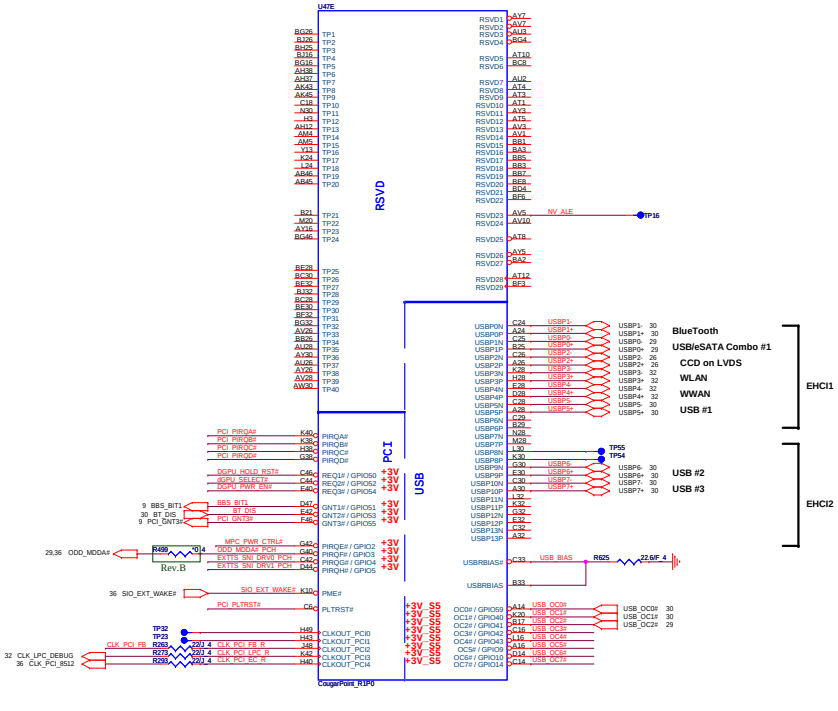
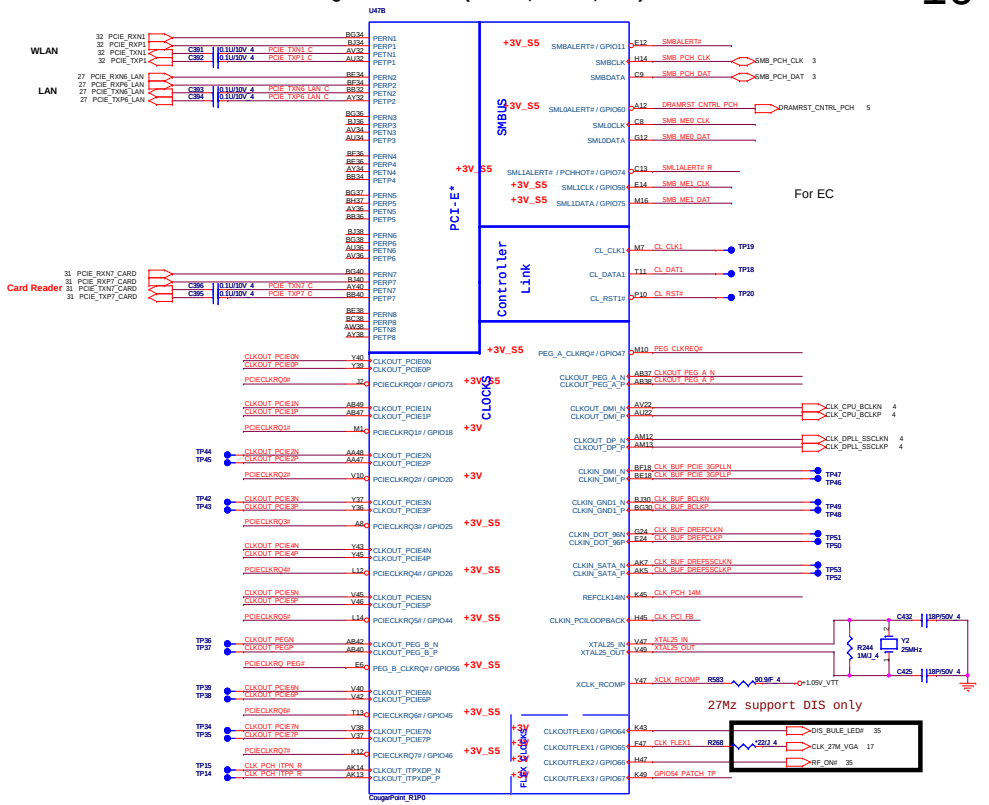
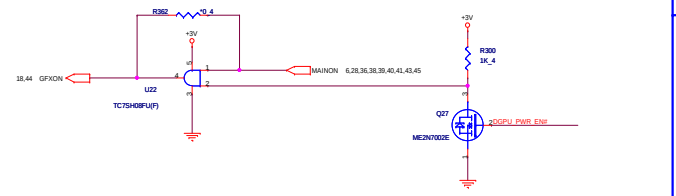
Cougar Point-M (PCI,USB,NVRAM)



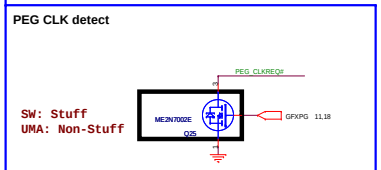
Cougar Point-M (PCI-E,SMBUS,CLK)

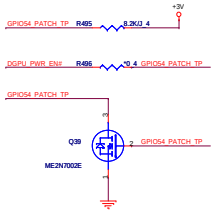


DGPU Power ON

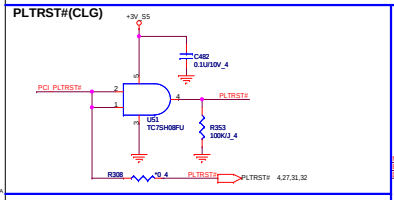


PEG CLK detect

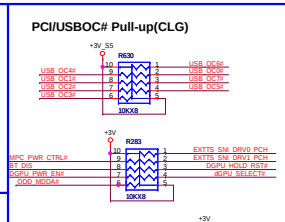




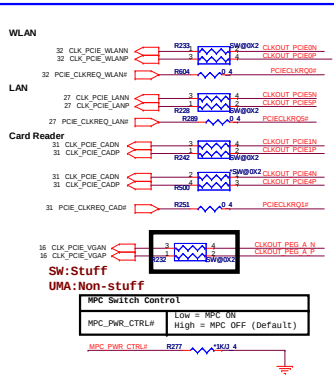
PLTRST#(CLG)



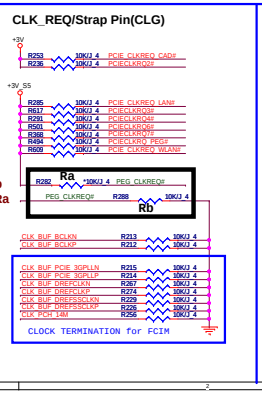
PCI/USBOC# Pull-up(CLG)



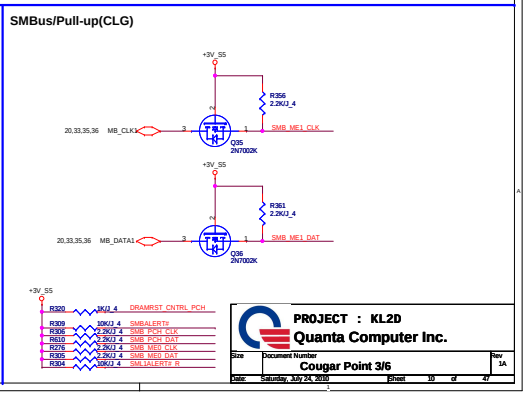
WLAN / LAN / Card Reader



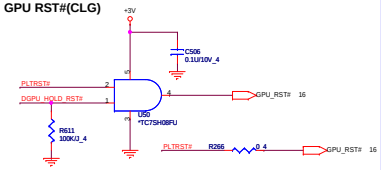
CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



GPU RST#(CLG)



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Quanta Computer Inc.
Cougar Point 3/6
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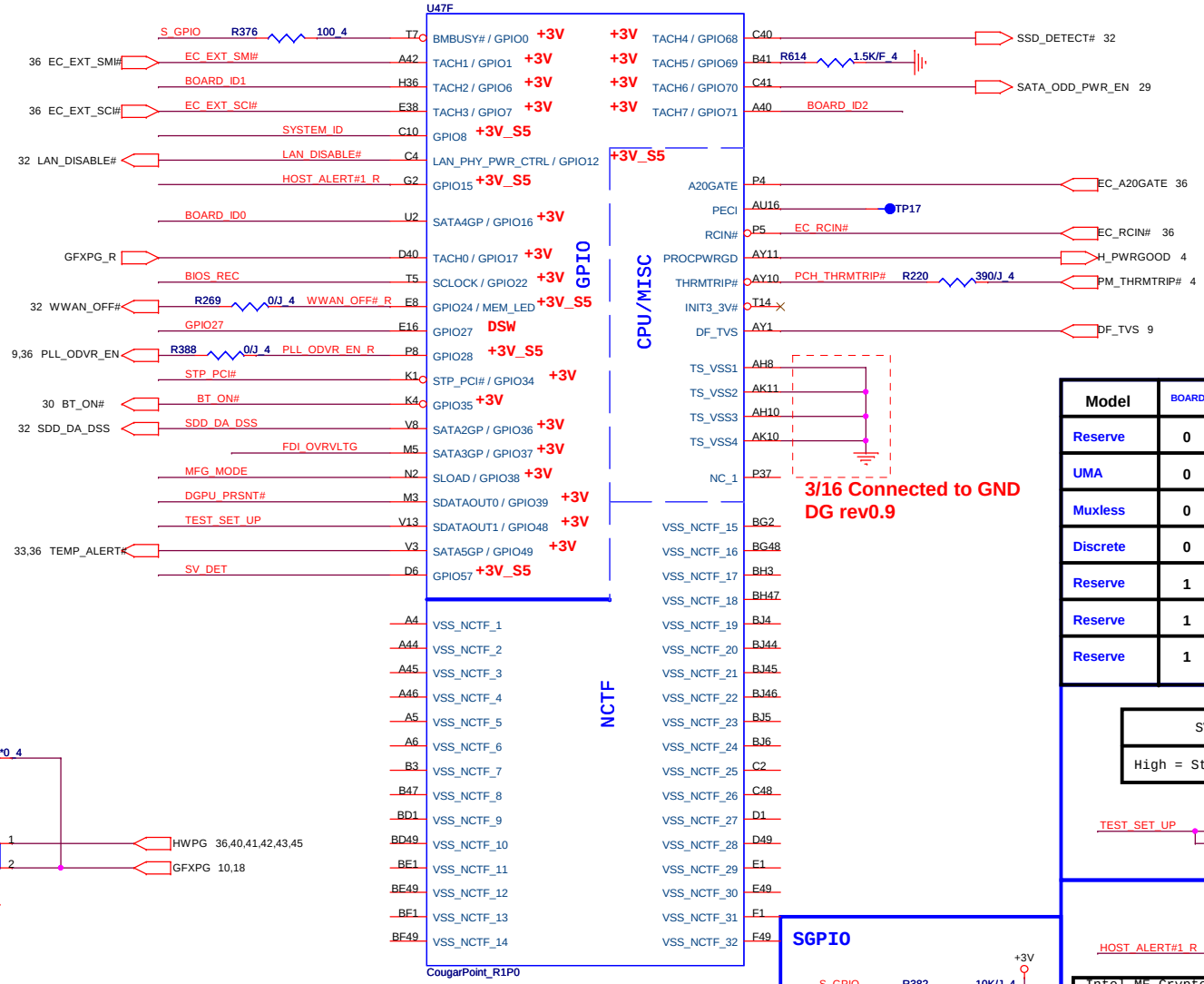
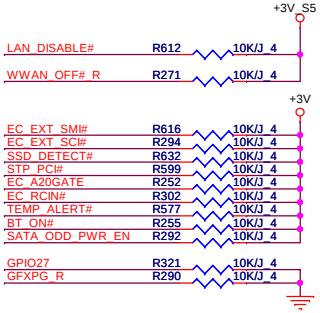
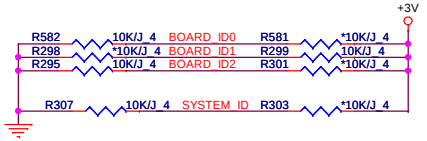
Cougar Point (GPIO,VSS_NCTF,RSVD)



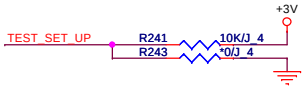
GPIO Pull-up/Pull-down(CLG)



Model	BOARD_ID2	BOARD_ID1	BOARD_ID0
Reserve	0	0	0
UMA	0	0	1
Muxless	0	1	0
Discrete	0	1	1
Reserve	1	0	0
Reserve	1	0	1
Reserve	1	1	0

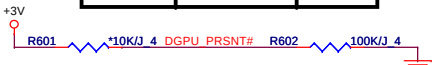


SV_SET_UP
High = Strong (Default)

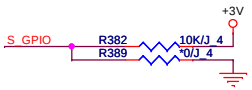


Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

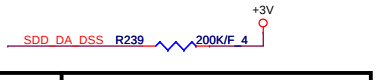
	SWITCHABLE	UMA
Stuff	R8489	R8490
No Stuff	R8490	R8489



SGPIO



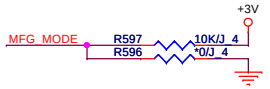
FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage



DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST



PROJECT : KL2D

Quanta Computer Inc.

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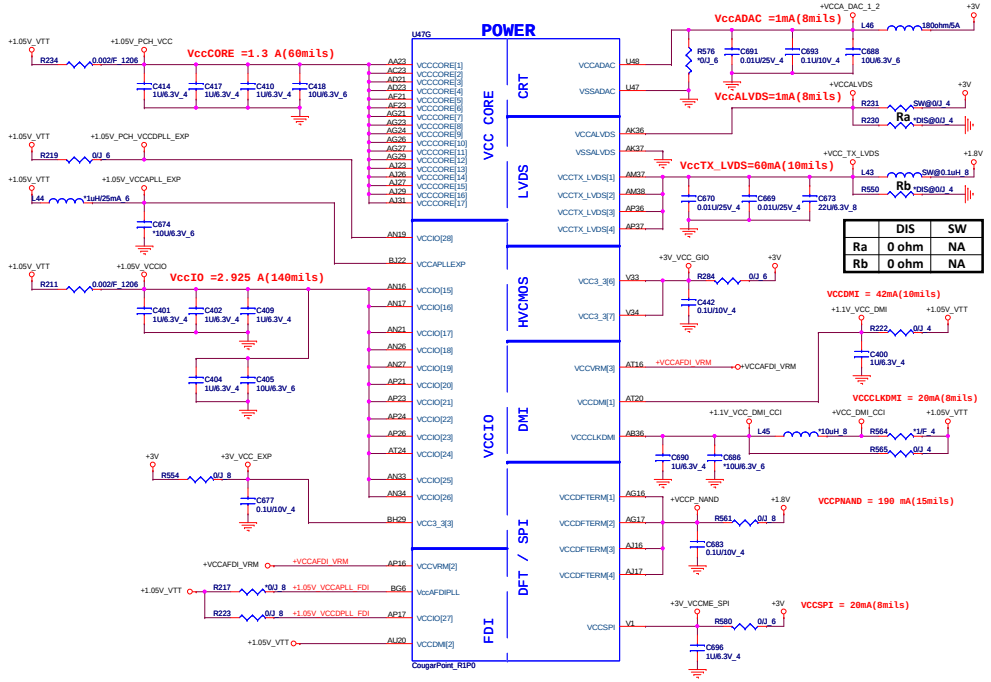
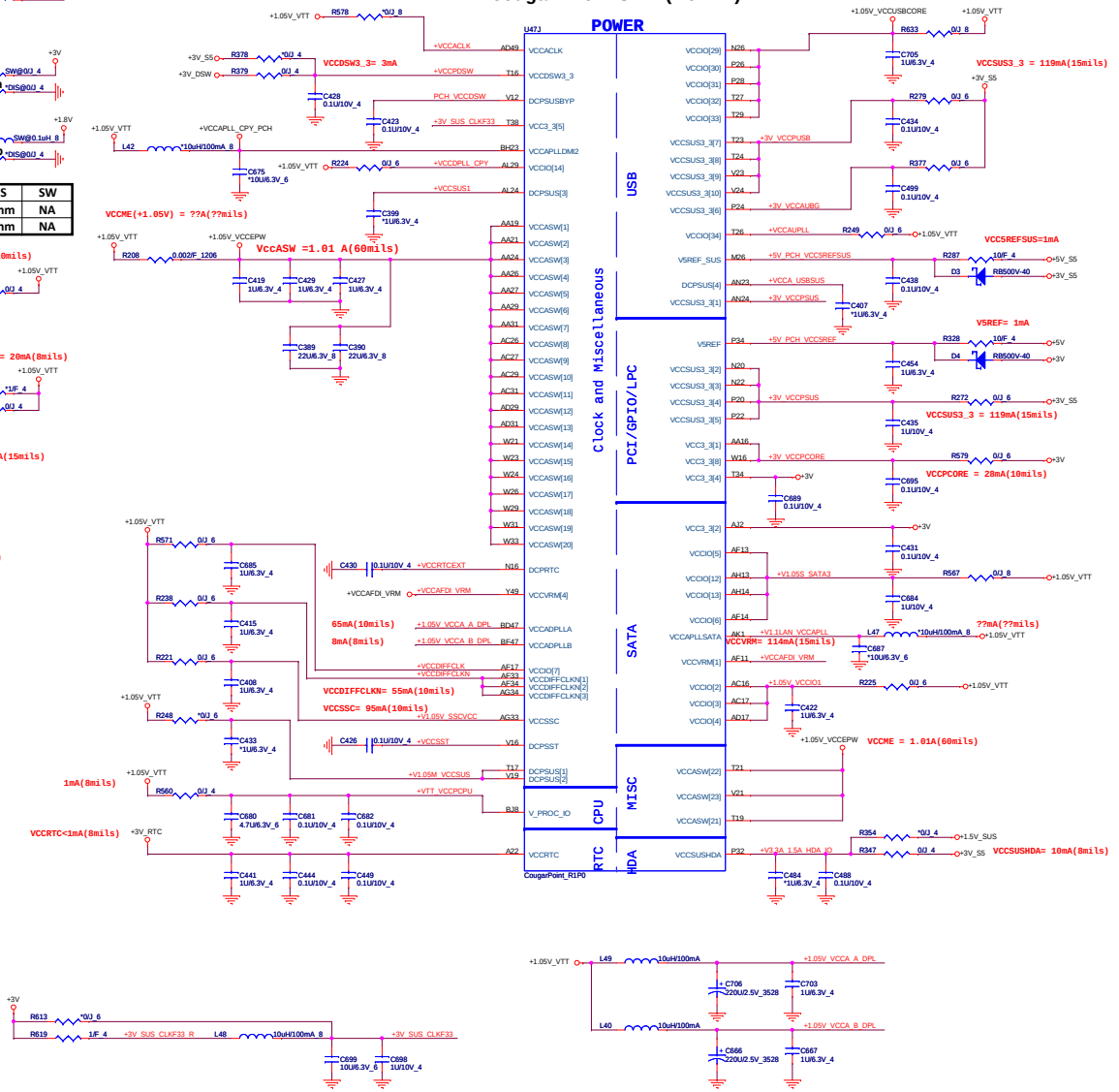
COUGAR POINT (POWER)



Cougar Point-M (POWER)



PROJECT : KL2D

Quanta Computer Inc.

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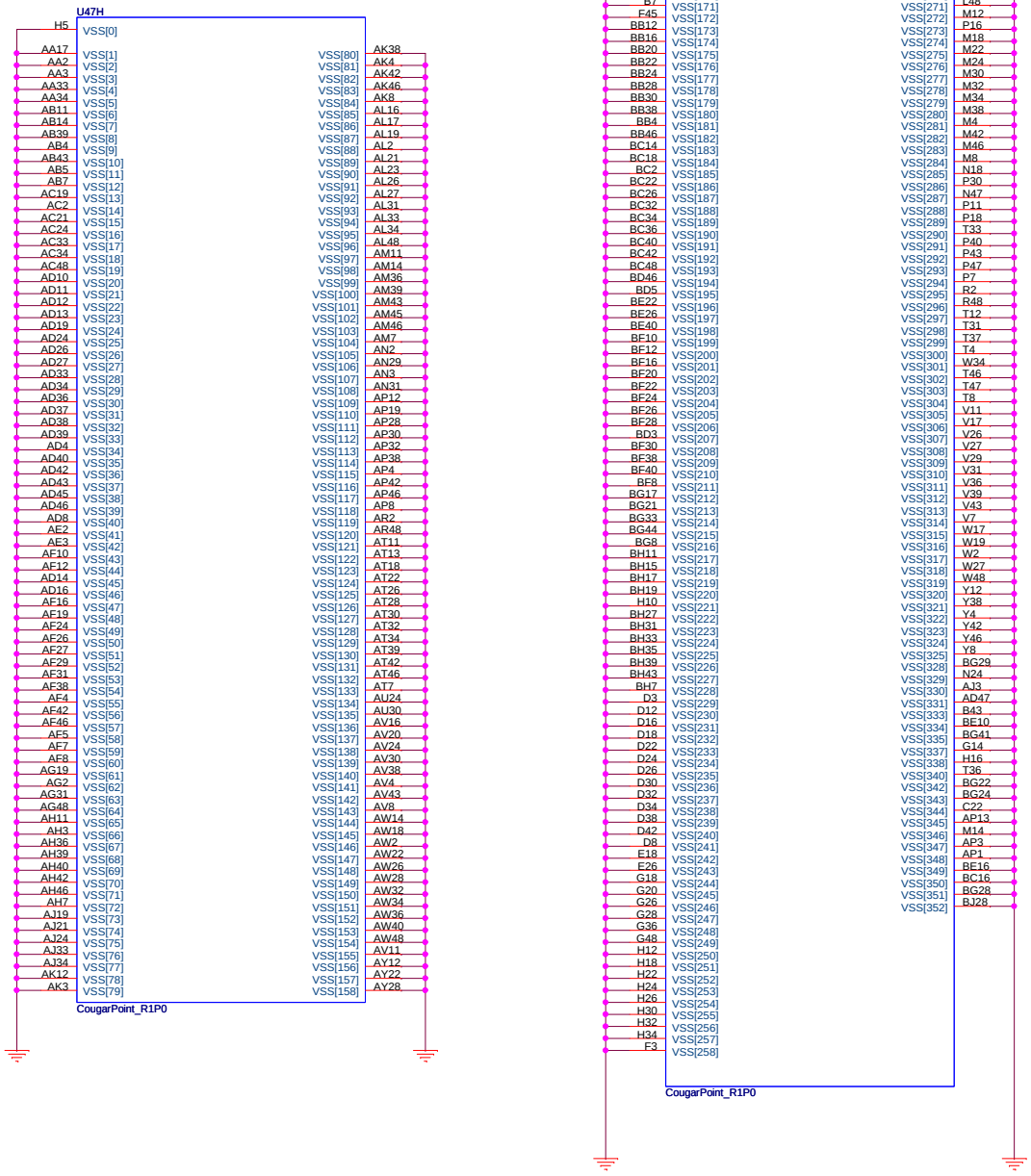
IBEX PEAK-M (GND)



PROJECT : KL2D

Quanta Computer Inc.

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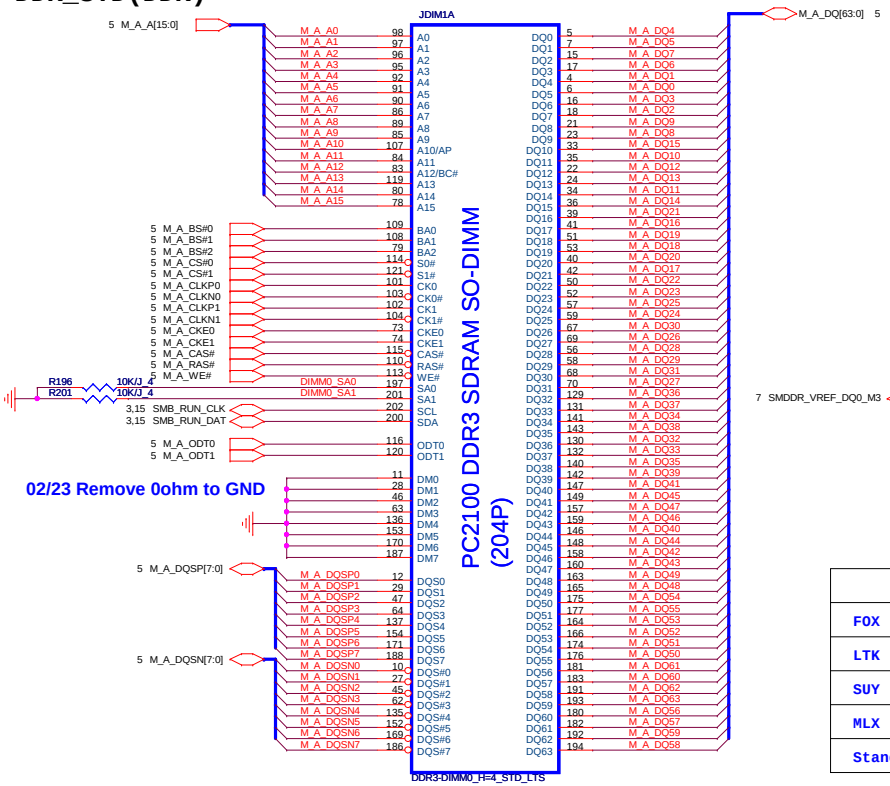
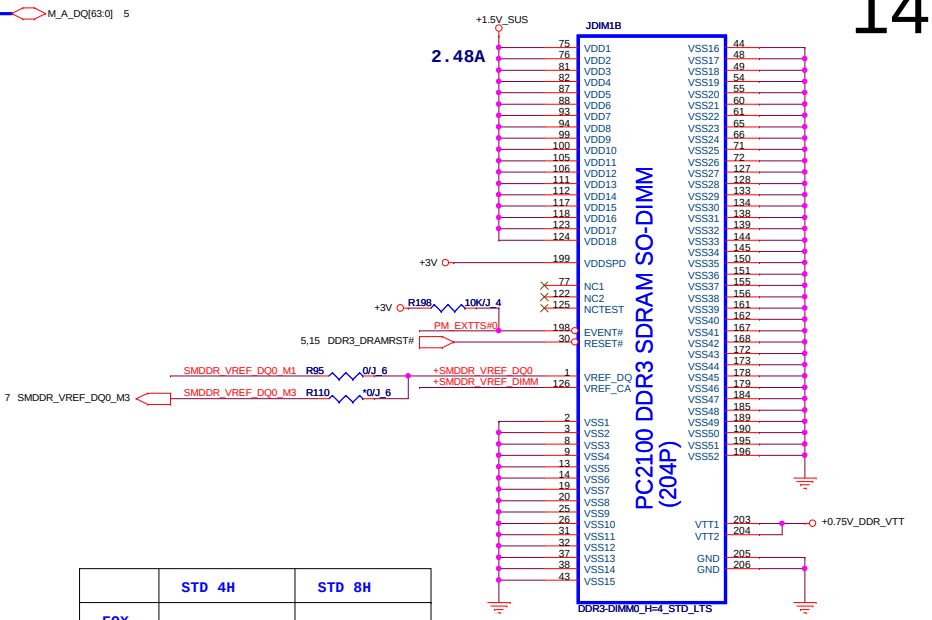
DDR_STD(DDR)



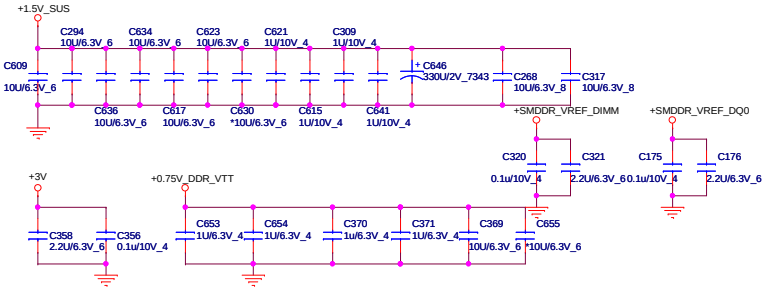
02/23 Remove 0ohm to GND

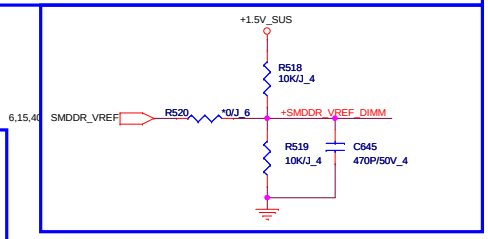


	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 4H type:DDR-C-2013289-204p		

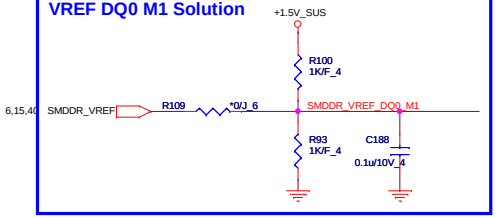
VREF DQ0 M2 Solution

Place these Caps near So-Dimm0.





VREF DQ0 M1 Solution



PROJECT : KL2D
Quanta Computer Inc.

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	DDRIII SO-DIMM-0	1A
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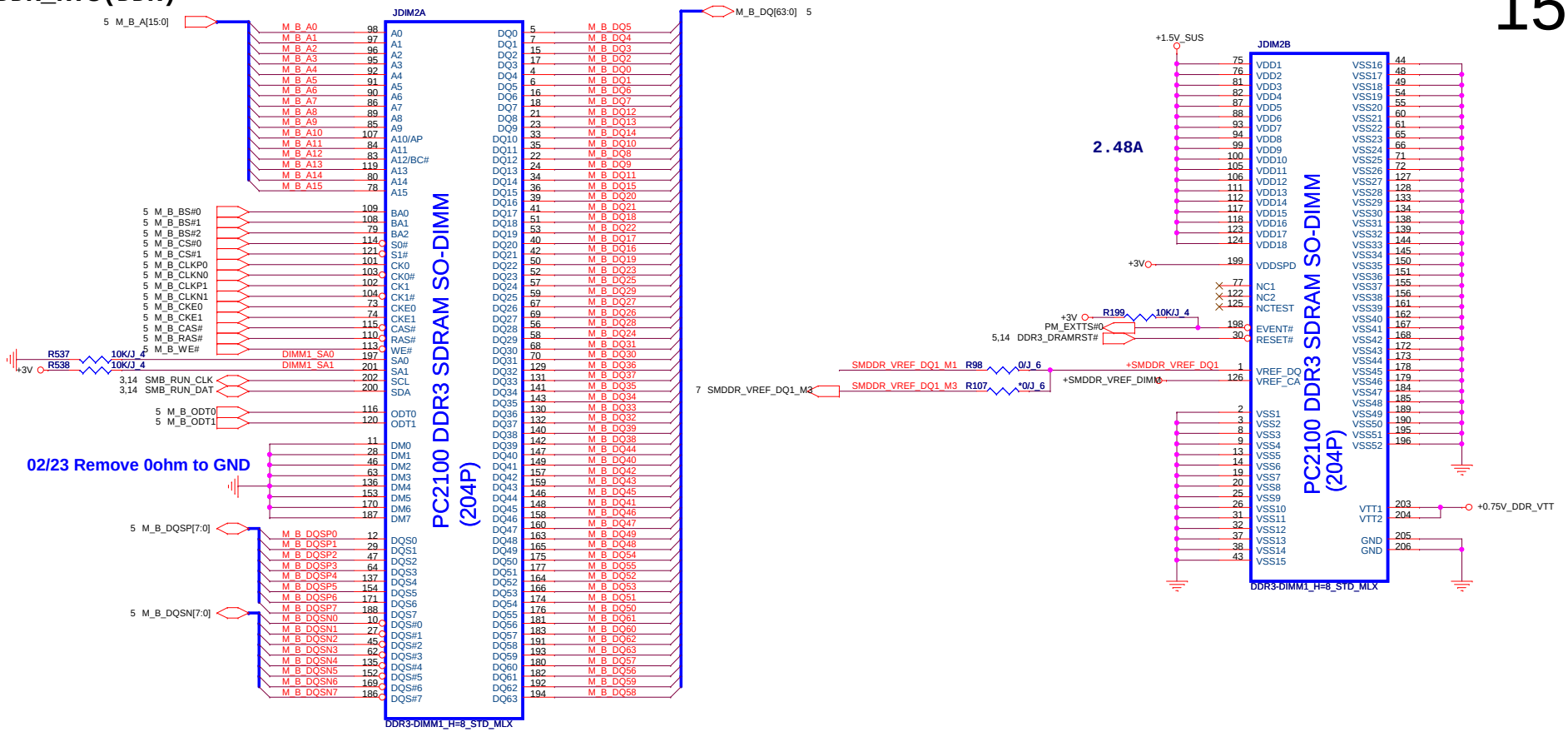
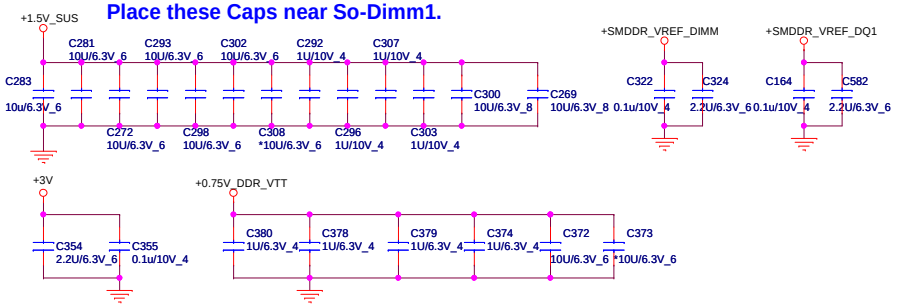
DDR_RVS(DDR)

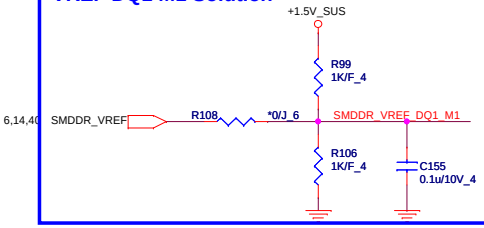


Place these Caps near So-Dimm1.



VREF DQ1 M2 Solution

VREF DQ1 M1 Solution



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A

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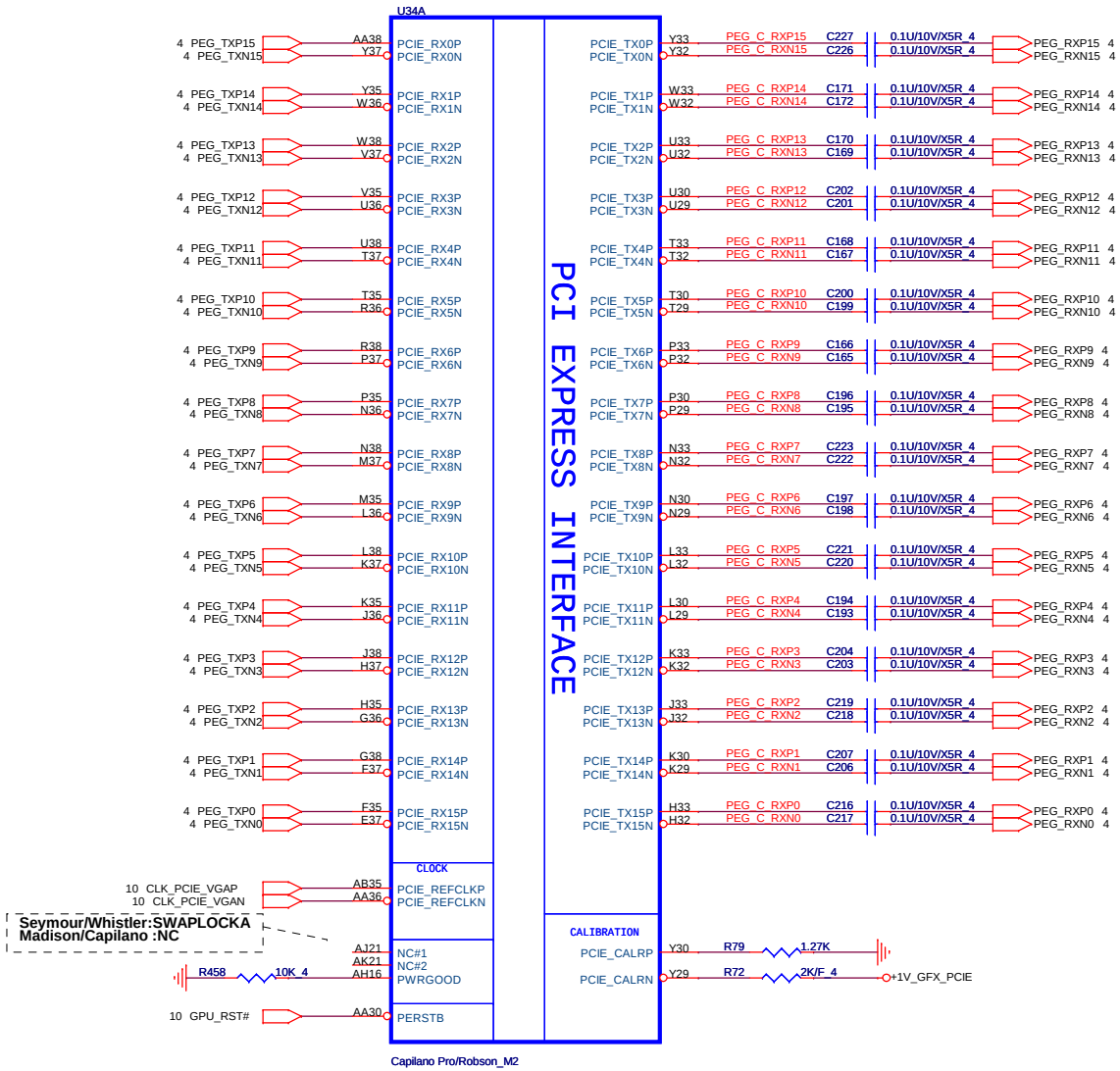

PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison PCIE I/F	1A
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Memory Straps		RAM_TYPE_CFG3	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0
800 MHz 1GB(64M*16) Hynix_Orion die	H5TQ1G63BFR-12C	0	0	0	0
800 MHz 1GB(64M*16) Samsung_E die	K4W1G1646E-HC12	0	0	0	1
		0	0	1	0
		0	0	1	1
		0	1	0	0
		0	1	0	1

Note : Required Frequency = 800 MHz

VRAM TYPE

APERTURE SIZE

MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

Accss to SCL and SDA is mandatory on BACO design for debug purposes.

NC FOR PARK

NC FOR PARK

NC FOR PARK

LVDS

Power PWM config

GenericF/G is NC on PARK

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

1.0V @ 150mA DPLL_VDDC

Use 27Mhz Crystal for A test Danny0518

NC on Seymour/Whistler

HDMI

CRT

!!! NC when M92-M2/PARK

!!! NC when M92-M2/PARK

DDC6CLK/DDC6DATA support internal HDCP(High-bandwidth Digital Content Protection) function.

Capilano Pro/Robson_M2

CONFIGURATION STRAPS			
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	1
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	11
VIP_DEVICE_STRAP_EN	BIOS_ROM_EN	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0

Layout Note: Place 150 ohm termination resistors close to ATI CHIP.

GPU Power-on sequence

1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU_PWROK

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Quanta Computer Inc.

Size	Document Number	Rev
C	Madison_IO&STRAP	1A

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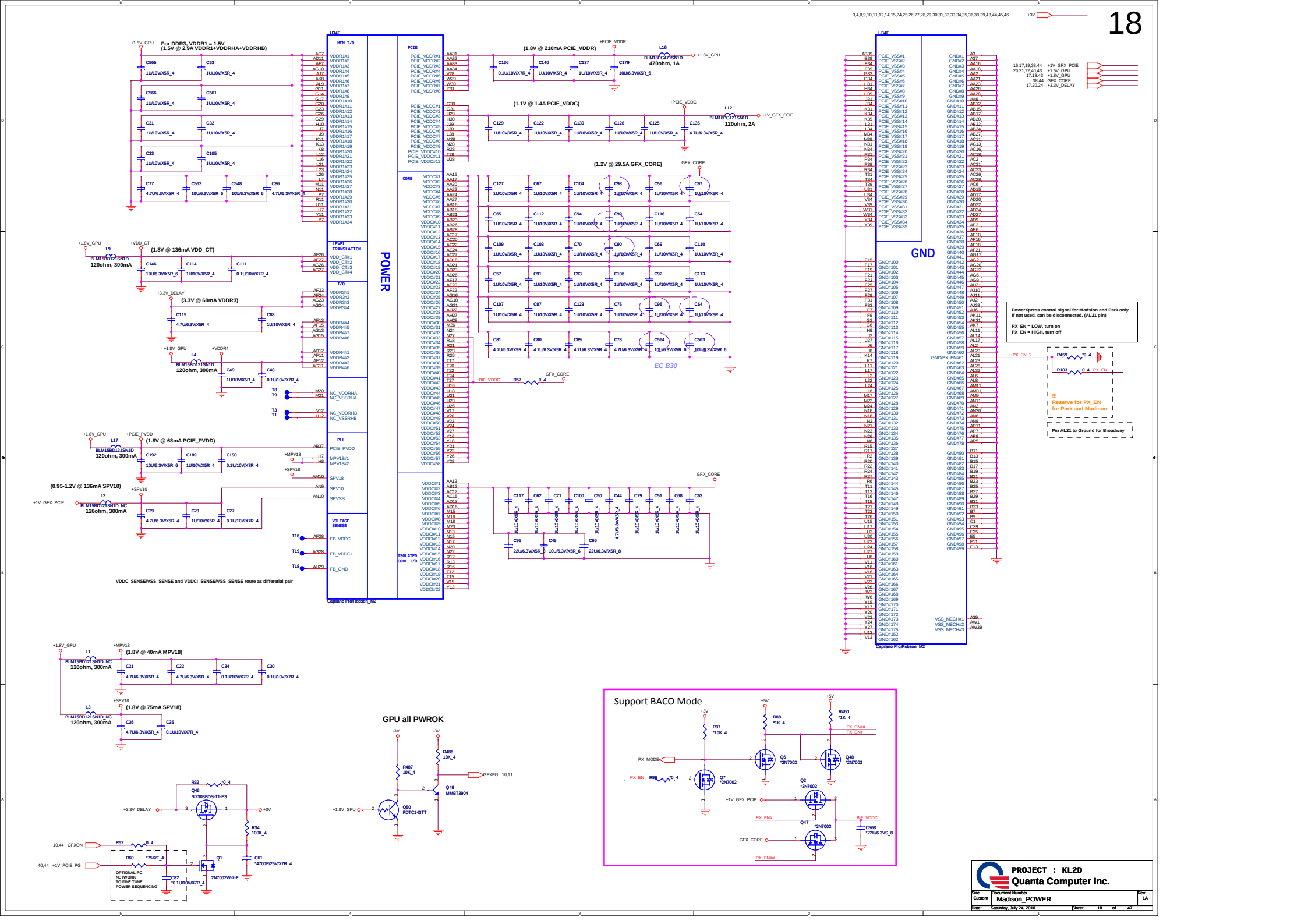

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Quanta Computer Inc.	
Size: Custom	Document Number: Madison_POWER
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16,17,18,38,44 +1V_GFX_PCIE
17,18,43 +1.8V_GPU

!!!
For M96/92, DPx_VDD10 = 1.1V
For M97 DPx_VDD10 = 1.0V

U34H

DP C/D POWER | DP A/B POWER | DP E/F POWER | DP PLL POWER

(1.8V@130mA DPC_VDD18)
DPC & DPD aren't used.
+1.8V_GPU
AP20 DPC_VDD18#1
AP21 DPC_VDD18#2
C84 *0.1U/10V/X7R_4
+1V_GFX_PCIE
AP13 DPC_VDD10#1
AT13 DPC_VDD10#2
C41 *0.1U/10V/X7R_4
AN17 DPC_VSSR#1
AP16 DPC_VSSR#2
AP17 DPC_VSSR#3
AW14 DPC_VSSR#4
AW16 DPC_VSSR#5

(1.8V@130mA DPD_VDD18)
+1.8V_GPU
AP22 DPD_VDD18#1
AP23 DPD_VDD18#2
C83 *0.1U/10V/X7R_4
+1V_GFX_PCIE
AP14 DPD_VDD10#1
AP15 DPD_VDD10#2
C43 *0.1U/10V/X7R_4
AN19 DPD_VSSR#1
AP18 DPD_VSSR#2
AP19 DPD_VSSR#3
AW20 DPD_VSSR#4
AW22 DPD_VSSR#5

(1.8V @ 400mA DPE_VDD18;
200mA for DPE/DPF respectively)
+1.8V_GPU
L15 BLM18PG600SN1D
60ohm, 500mA
+DPE_VDD18
C162 10U/6.3V/X5R_6
C154 1U/10V/X5R_4
C151 0.1U/10V/X7R_4
150/F_4 R457 AW18
DPCD_CALR
AH34 DPE_VDD18#1
AJ34 DPE_VDD18#2
+DPE_VDD10
AL33 DPE_VDD10#1
AM33 DPE_VDD10#2
AN34 DPE_VSSR#1
AP39 DPE_VSSR#2
AR39 DPE_VSSR#3
AU37 DPE_VSSR#4
DPE & DPF for LVDS

(1.1V @ 200mA DPE_VDD10;
100mA for DPE/DPF respectively)
+1V_GFX_PCIE
L10 BLM15BD121SN1D
120ohm, 300mA
+DPE_VDD10
C152 10U/6.3V/X5R_6
C149 1U/10V/X5R_4
C145 0.1U/10V/X7R_4
+DPE_VDD18
AE34 DPF_VDD18#1
AG34 DPF_VDD18#2
AK33 DPF_VDD10#1
AK34 DPF_VDD10#2
AF39 DPF_VSSR#1
AH39 DPF_VSSR#2
AK39 DPF_VSSR#3
AL34 DPF_VSSR#4
AM34 DPF_VSSR#5
150/F_4 R101 AM39
DPEF_CALR

DPA_VDD18#1 AN24
DPA_VDD18#2 AP24
+DPA_VDD18
(1.1V @ 200mA DPA_VDD10)
+DPA_VDD10
L6 BLM15BD121SN1D
120ohm, 300mA
+1V_GFX_PCIE
DPA for HDMI
DPA_VDD10#1 AP31
DPA_VDD10#2 AP32
C119 0.1U/10V/X7R_4
C121 1U/10V/X5R_4
C120 4.7U/6.3V/X5R_4
DPA_VSSR#1 AN27
DPA_VSSR#2 AP27
DPA_VSSR#3 AP28
DPA_VSSR#4 AW24
DPA_VSSR#5 AW26

(1.8V @ 110mA DPB_VDD18)
+1.8V_GPU
C76 *0.1U/10V/X7R_4
DPB_VDD18#1 AP25
DPB_VDD18#2 AP26
+DPB_VDD18
+1V_GFX_PCIE
C147 *0.1U/10V/X7R_4
(1.1V @ 200mA DPB_VDD10)
DPB_VDD10#1 AN33
DPB_VDD10#2 AP33
DPB_VSSR#1 AN29
DPB_VSSR#2 AP29
DPB_VSSR#3 AP30
DPB_VSSR#4 AW30
DPB_VSSR#5 AW32

(1.8V @ 20 mA DPA_PVDD)
+DPA_PVDD
L39 BLM15BD121SN1D
120ohm, 300mA
+1.8V_GPU
C569 0.1U/10V/X7R_4
C570 1U/10V/X5R_4
C571 10U/6.3V/X5R_6
DPA_PVDD AU28
DPA_PVSS AV27
AW28 R467 150/F_4
+1.8V_GPU
DPB_PVDD AV29
DPB_PVSS AV28
C572 *0.1U/10V/X7R_4
(1.8V @ 20 mA DPB_PVDD)
DPC & DPD aren't used.
+1.8V_GPU
DPC_PVDD AU18
DPC_PVSS AV17
C55 *0.1U/10V/X7R_4
DPD_PVDD AV19
DPD_PVSS AR18
C60 *0.1U/10V/X7R_4
(1.8V @ 40mA DPE_PVDD; 20mA
for DPE/DPF respectively)
+DPE_PVDD
L19 BLM15BD121SN1D
120ohm, 300mA
+1.8V_GPU
DPE_PVDD AM37
DPE_PVSS AN38
C177 0.1U/10V/X7R_4
C182 1U/10V/X5R_4
C185 10U/6.3V/X5R_6
NC_DPF_PVDD AL38
NC_DPF_PVSS AM35

(1.8V @ 110mA DPA_VDD18)
+DPA_VDD18
L5 BLM15BD121SN1D
120ohm, 300mA
+1.8V_GPU
C108 0.1U/10V/X7R_4
C101 1U/10V/X5R_4
C102 4.7U/6.3V/X5R_4

Capilano Pro/Robson_M2

PROJECT : KL2D
Quanta Computer Inc.

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Custom	Madison_DP_POWER	1A

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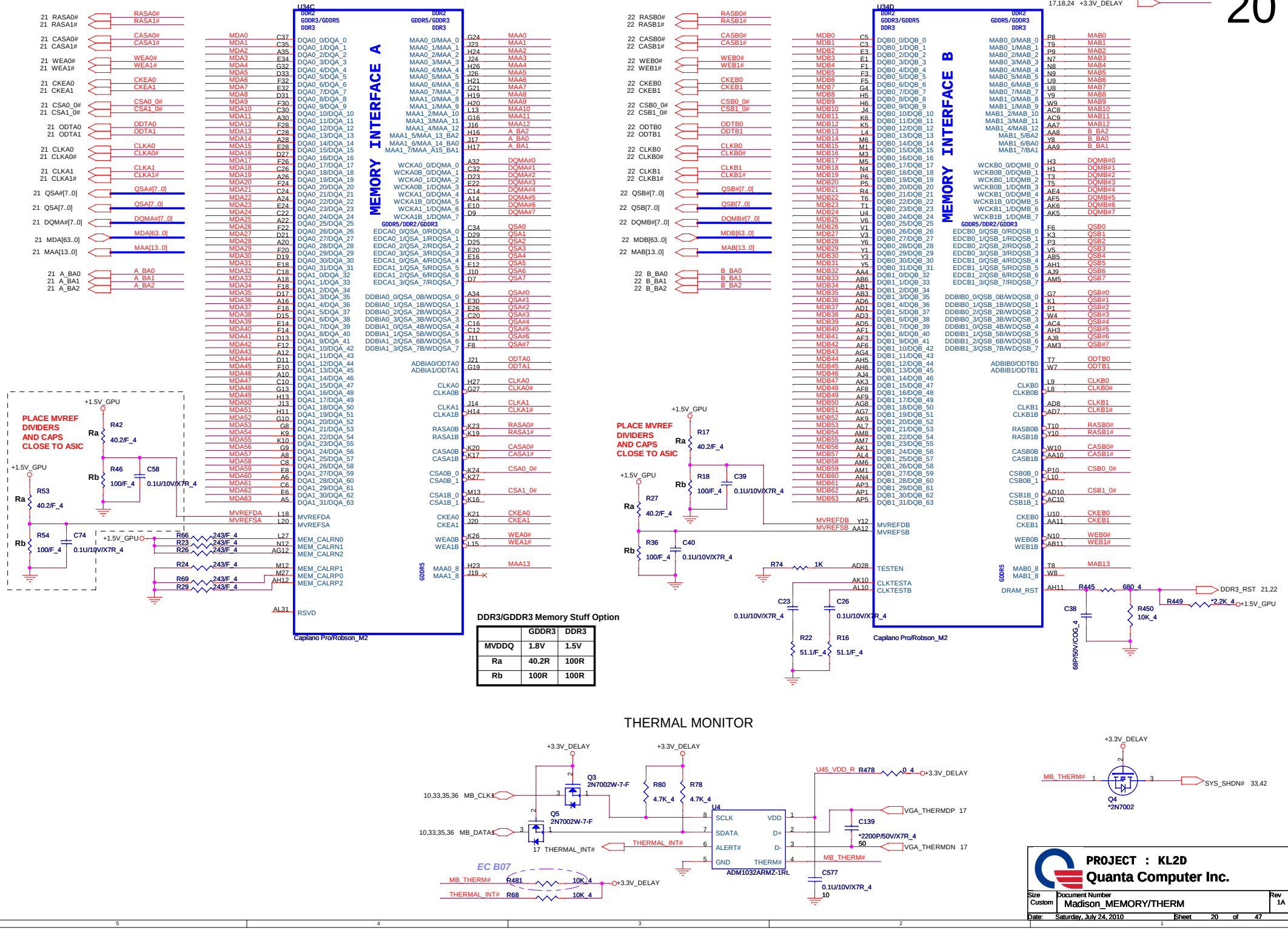

DDR3/GDDR3 Memory Stuff Option

	GDDR3	DDR3
MVDDQ	1.8V	1.5V
Ra	40.2R	100R
Rb	100R	100R

THERMAL MONITOR

DDR3 64MX16, CH A : 512MB

18,20,22,40,43 +1.5V_GPU

U5 / U38 / U3 / U35 — K4W1G1646E-HC12 — 100-BALL SDRAM DDR3

20 MDA[63..0]
20 MAA[13..0]
20 QSA#[7..0]
20 QSA[7..0]
20 DQMA#[7..0]
20 A_BA[2..0]

Placement has to be close to VRAM

CLKA0 R105 56_4 C184 0.01U/16V/X7R_4
CLKA0# R102 56_4
CLKA1 R45 56_4 C52 0.01U/16V/X7R_4
CLKA1# R50 56_4

Close to U4

C579 1U/6.3V/X5R_4, C205 1U/6.3V/X5R_4, C596 1U/6.3V/X5R_4, C595 *1U/6.3V/X5R_4, C191 1U/6.3V/X5R_4

Close to U44

C608 1U/6.3V/X5R_4, C580 *1U/6.3V/X5R_4, C578 1U/6.3V/X5R_4, C586 *1U/6.3V/X5R_4, C584 1U/6.3V/X5R_4

Close to U3

C59 1U/6.3V/X5R_4, C138 *1U/6.3V/X5R_4, C37 1U/6.3V/X5R_4, C42 *1U/6.3V/X5R_4, C47 1U/6.3V/X5R_4

Close to U41

C560 1U/6.3V/X5R_4, C581 *1U/6.3V/X5R_4, C575 1U/6.3V/X5R_4, C592 *1U/6.3V/X5R_4, C574 1U/6.3V/X5R_4

Close to U4 & U44

C225 10U/6.3V/X5R_6, C124 4.7U/6.3V/X5R_4, C585 10U/6.3V/X5R_6, C148 *10U/6.3V/X5R_6, C133 4.7U/6.3V/X5R_4

Close to U3 & U41

C72 4.7U/6.3V/X5R_4, C607 10U/6.3V/X5R_6, C576 10U/6.3V/X5R_6, C46 *10U/6.3V/X5R_6, C73 4.7U/6.3V/X5R_4

PROJECT : KL2D		
Quanta Computer Inc.		
Size: C	Document Number: Madison_DDR3_A_512M	Rev: 1A
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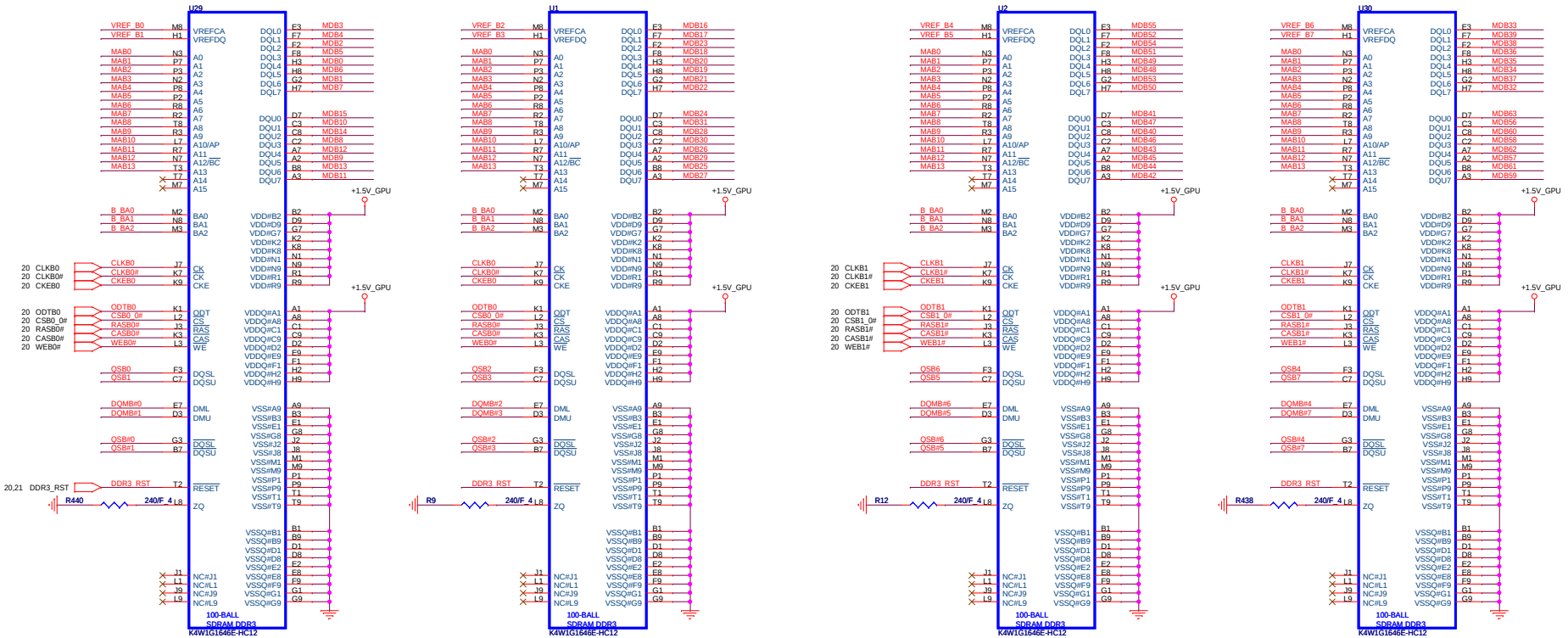
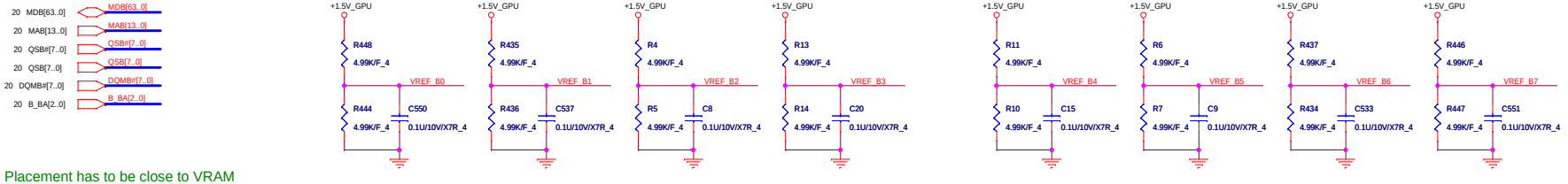
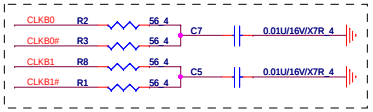
DDR3 64MX16, CH B : 512MB

18,20,21,40,43 +1.5V_GPU

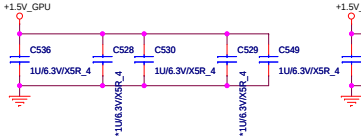




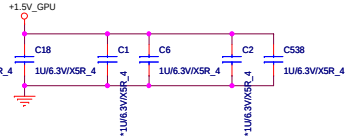
Placement has to be close to VRAM



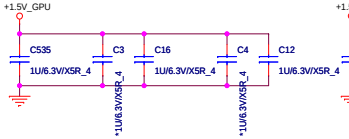
Close to U35



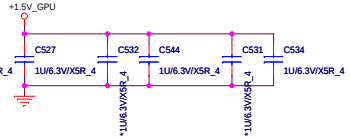
Close to U1



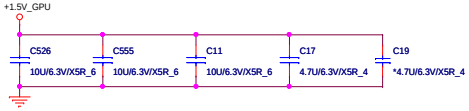
Close to U2



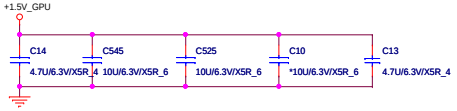
Close to U36



Close to U35 & U1



Close to U2 &U36



PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
C	Madison_DDR3_B_512M	1A

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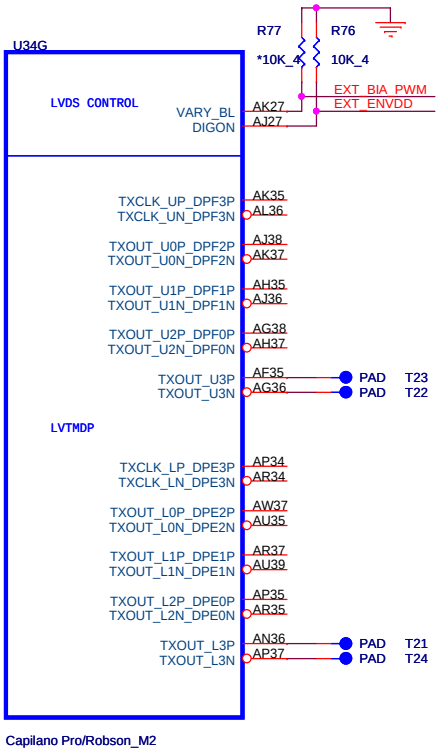
CRT SWITCH

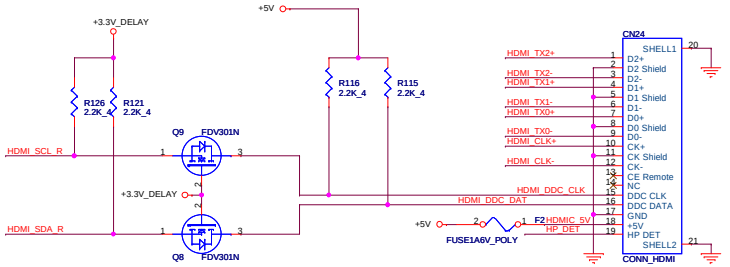


PROJECT : KL2D

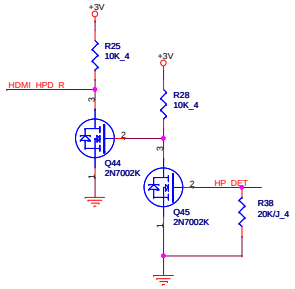
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison_LVDS/HDMI/CRT switchable	1A
Date: Saturday, July 24, 2010	Sheet 23 of 47	

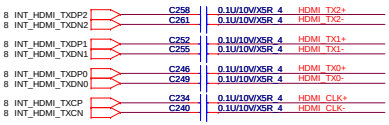
DIS/SG HDMI

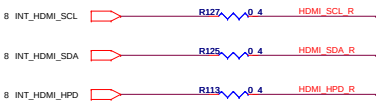


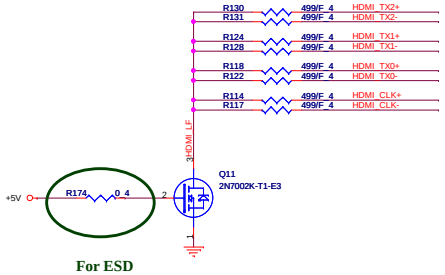
HDMI Hot-PLUG to EC and GPU



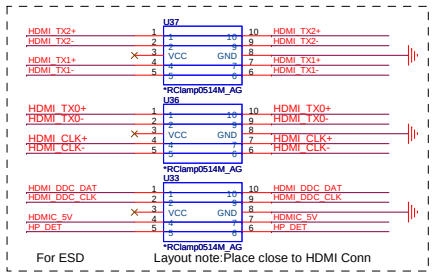
UMA Only / Muxless HDMI



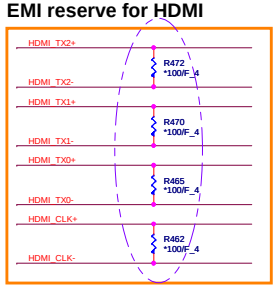




For ESD



EMI reserve for HDMI



8,9,12,18,25,26,28,29,33,34,36,38,39 +5V
3,4,8,9,10,11,12,14,15,18,25,26,27,28,29,30,31,32,33,34,35,36,38,39,43,44,45,46 +3V
17,18,20 +3.3V_DELAY

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Madison_LVDS/HDMI/CRT switchable	1A

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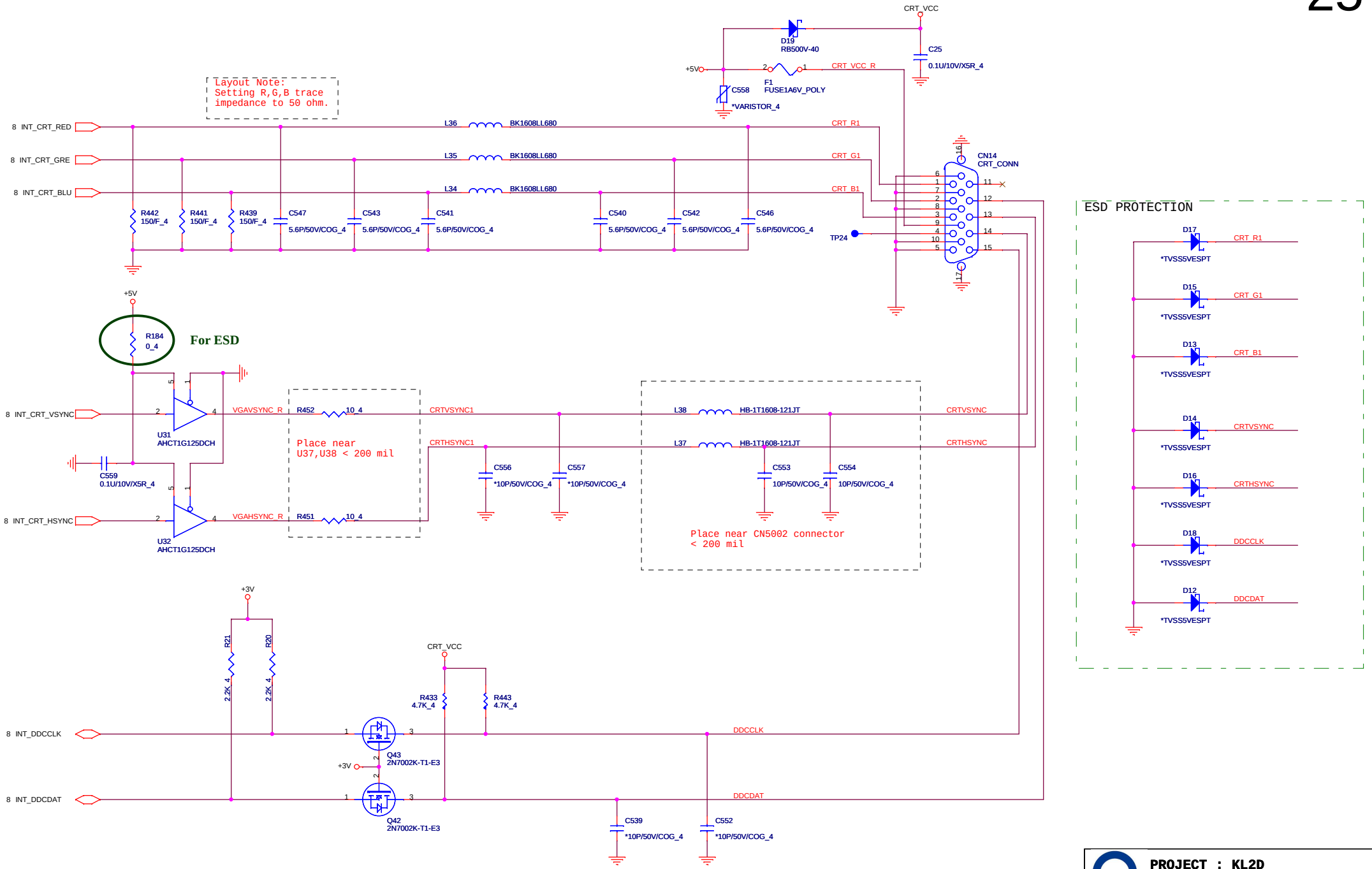
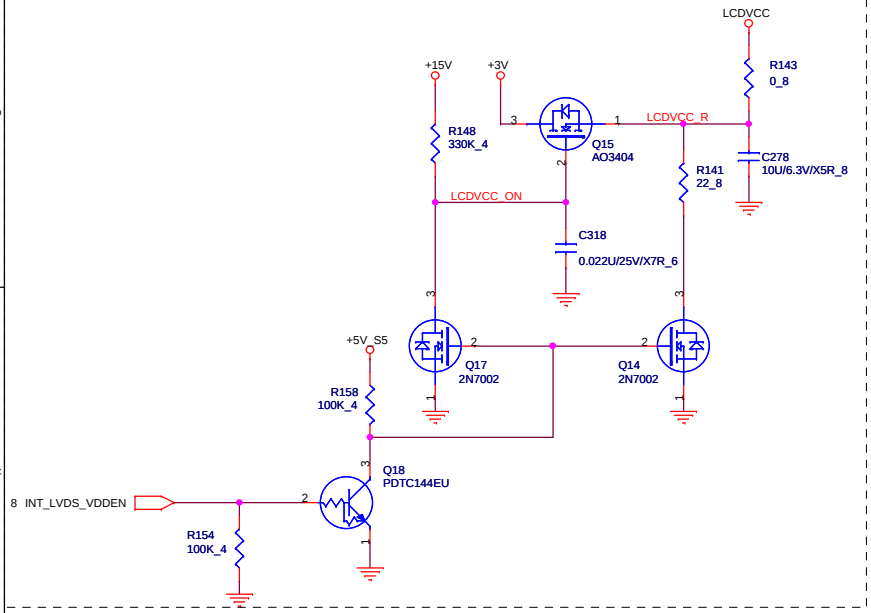
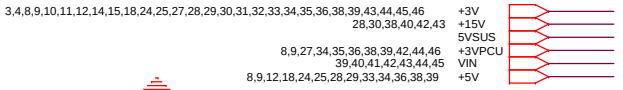


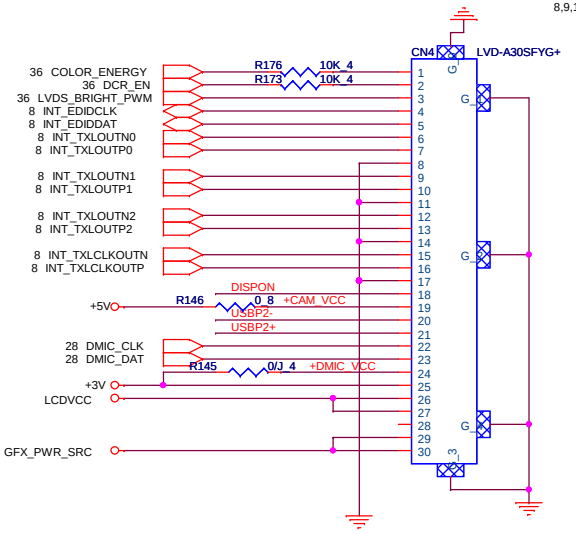
PROJECT : KL2D
Quanta Computer Inc.

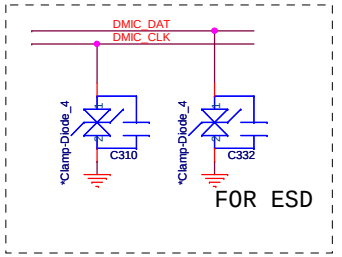
Size	Document Number	Rev
Custom	CRT CONN	1A
Date: Saturday, July 24, 2010	Sheet 25 of 47	

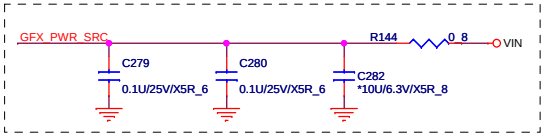
LCDVCC



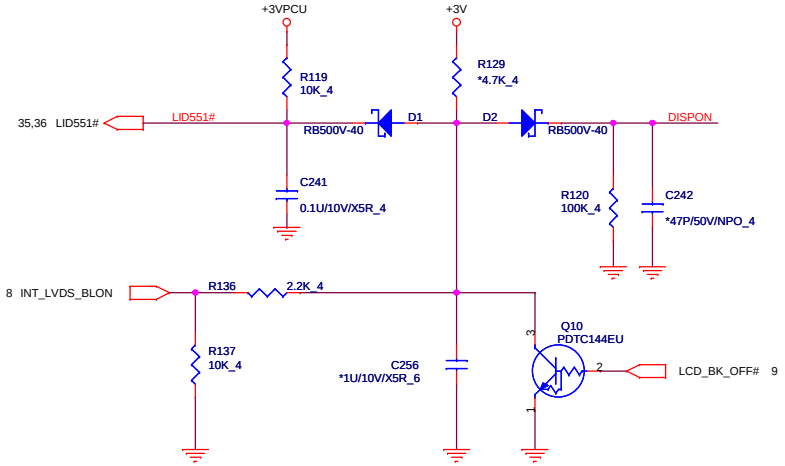


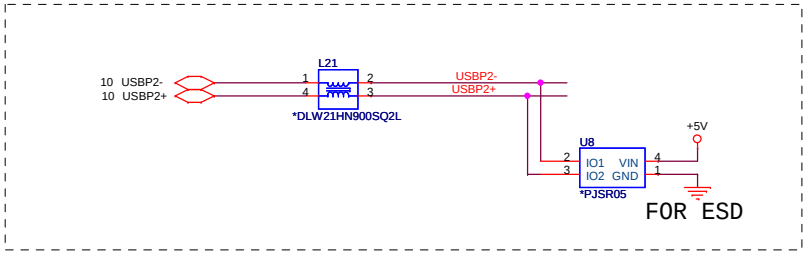






back light





PROJECT : KL2D

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN	1A
Date: Saturday, July 24, 2010	Sheet 26 of 47	

8,9,26,34,35,36,38,39,42,44,46 +3VPCU
3,4,8,9,10,11,12,14,15,18,24,25,26,28,29,30,31,32,33,34,35,36,38,39,43,44,45,46 +3V

Core Power Decoupling

VDDIO Power Decoupling

U13

BCM57780
7mm x 7mm
48-Pin QFN

Package Body

Transformer

U11 LFE9292A-R

U12 *CM1293A-04SO

U10 *CM1293A-04SO

RJ45 Connector

CN17 JM36113-N4525-7F

3.3V LANVCC

Q23 AO6402

3.3V Device ONLY

U14 M24C02-WMN6TP

U44 *74AHCT1G08GW

Q57 PDTC144EU

Q24 PDTC144EU

PROJECT : KL2D
Quanta Computer Inc.

Size: Custom | Document Number: LAN (BCM57780, RJ45) | Rev: 1A
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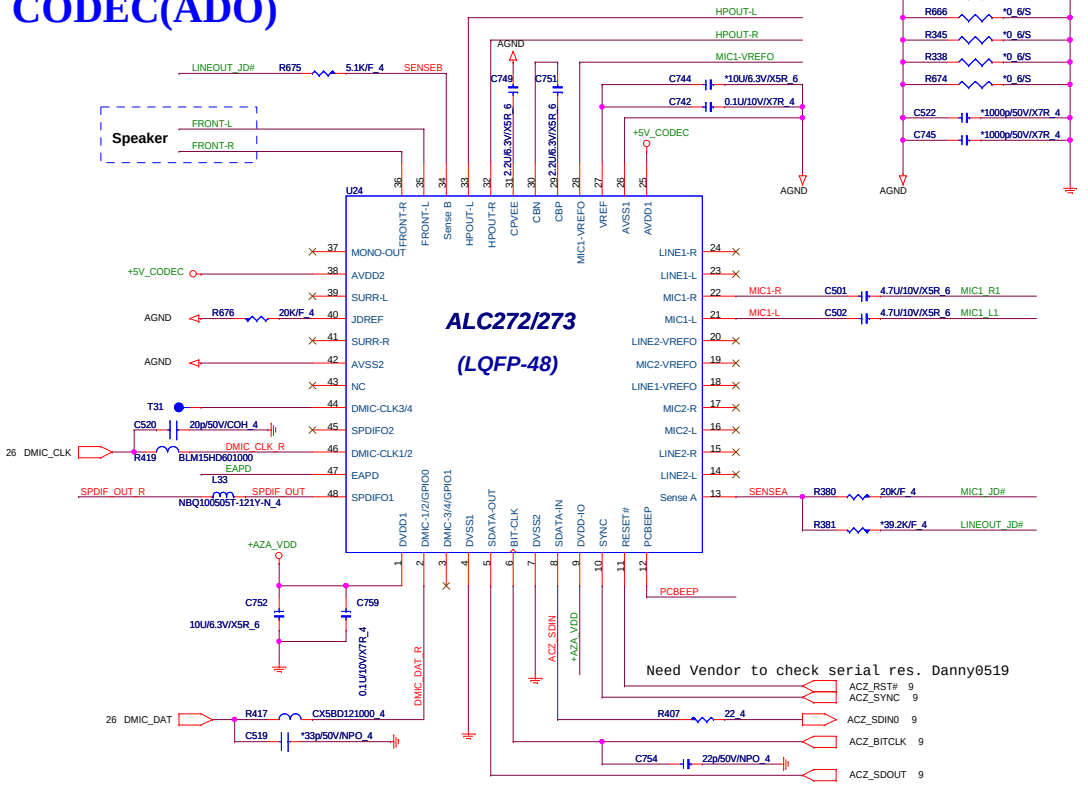
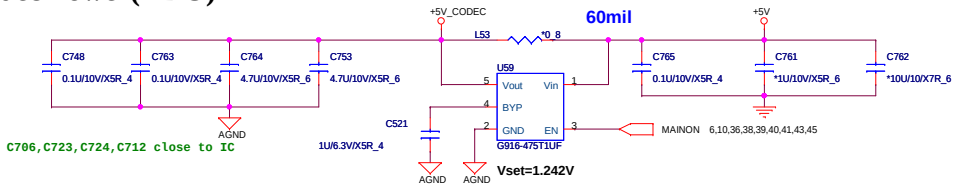
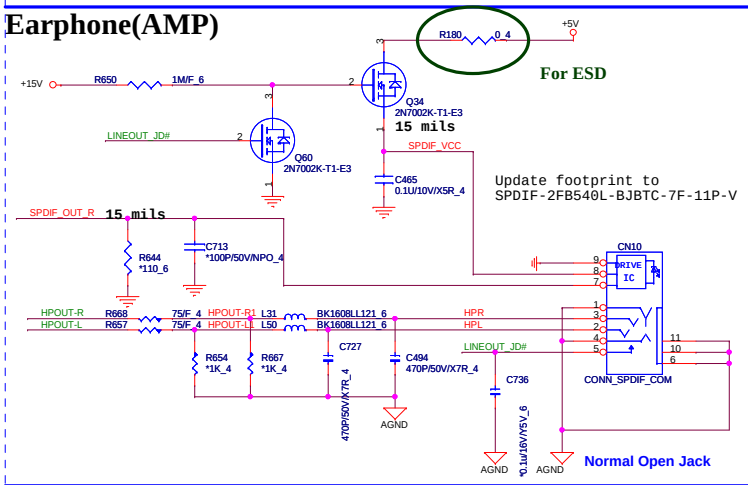
CODEC(ADO)



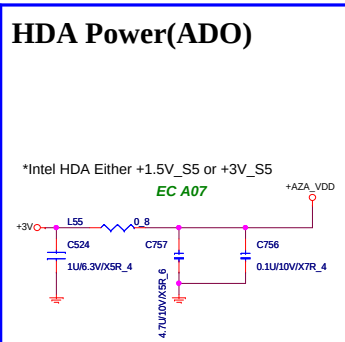
Codec Power(ADO)



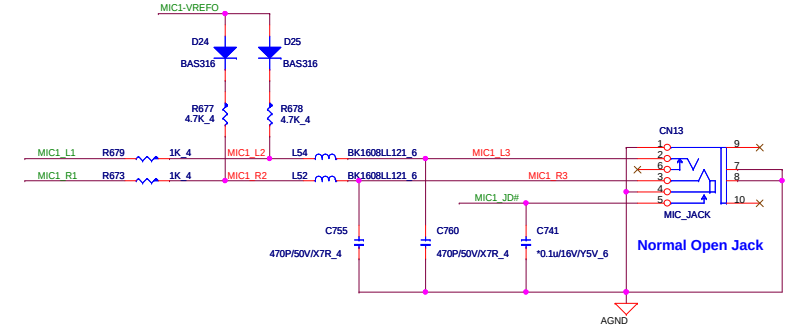
Earphone(AMP)



HDA Power(ADO)

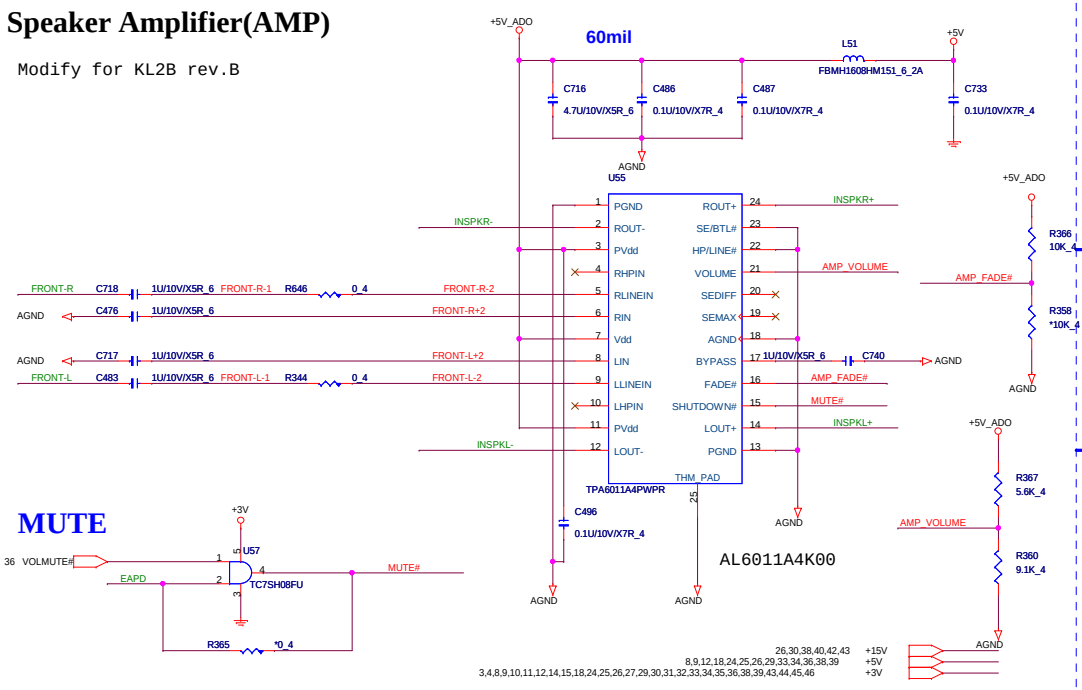


System MIC(AMP)

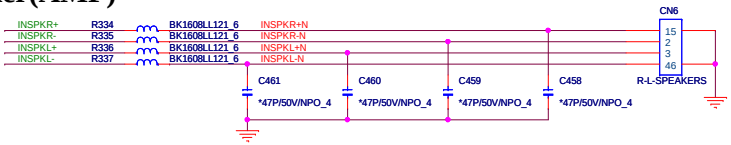


Speaker Amplifier(AMP)

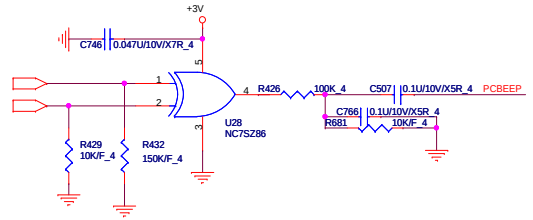
Modify for KL2B rev.B



Speaker(AMP)



PC BEEP



PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AL272/AMP/MIC/LINE-OUT	1A

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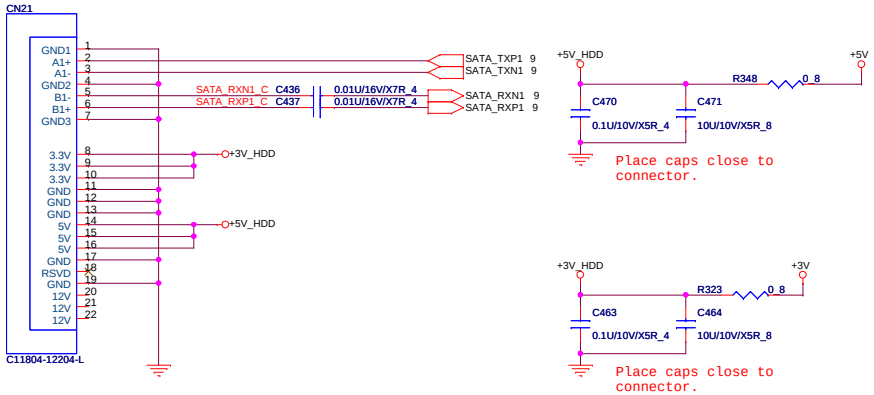
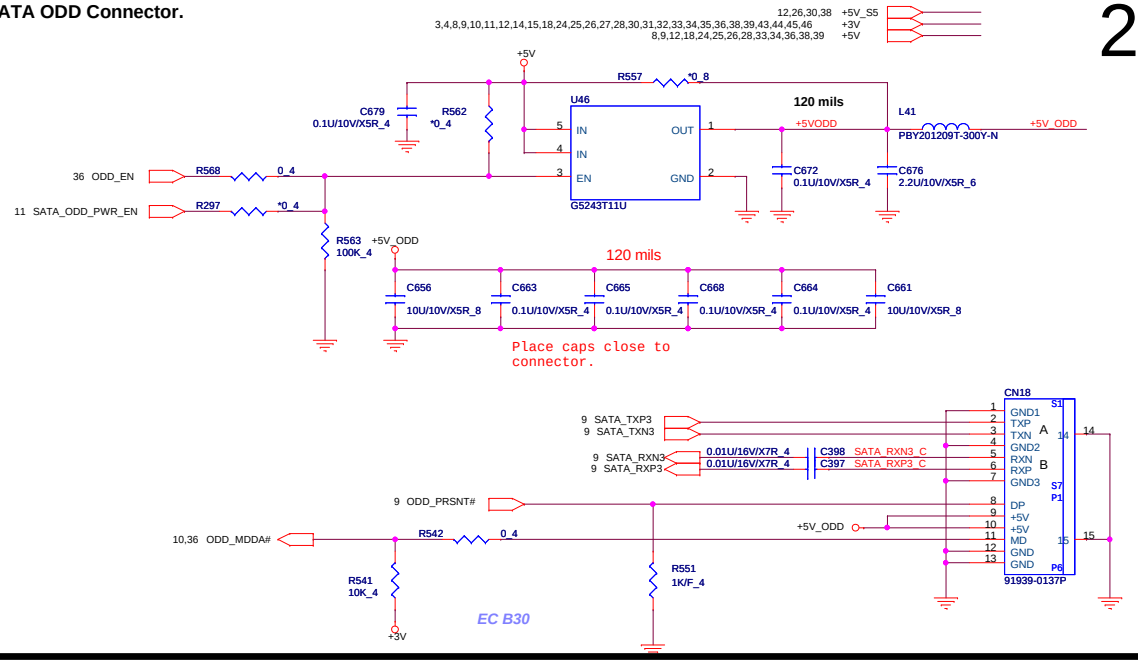
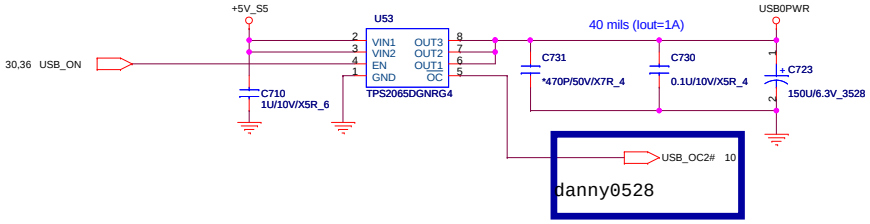
SATA HDD Connector.

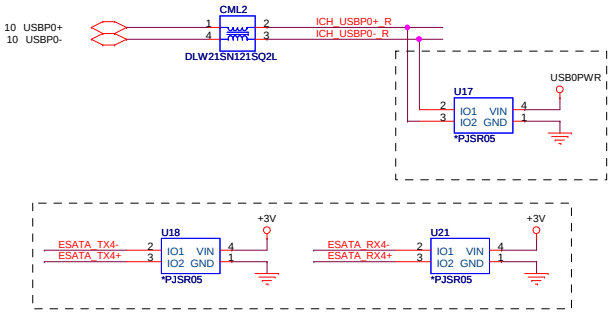


SATA ODD Connector.

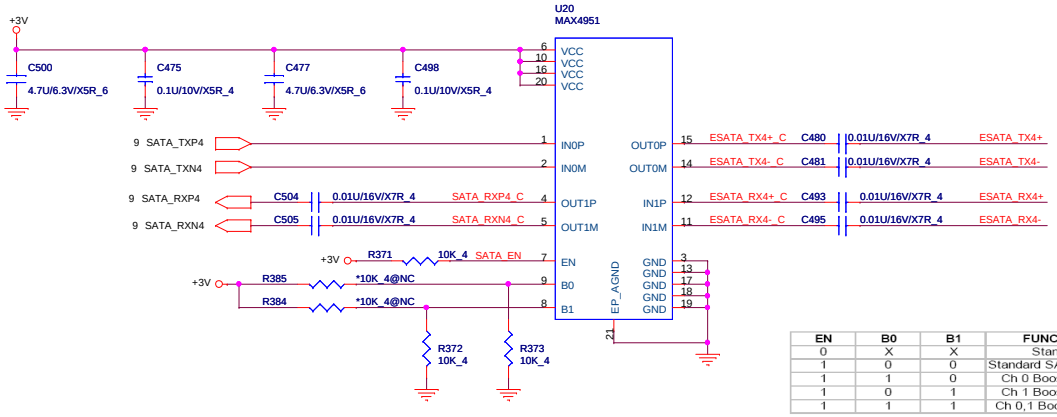


USB + E-SATA

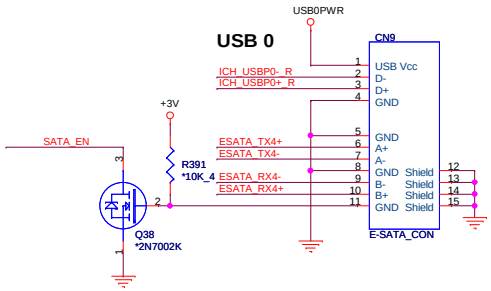




E-SATA RE-DRIVER



EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output



PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/ESATA/CD-ROM	1A
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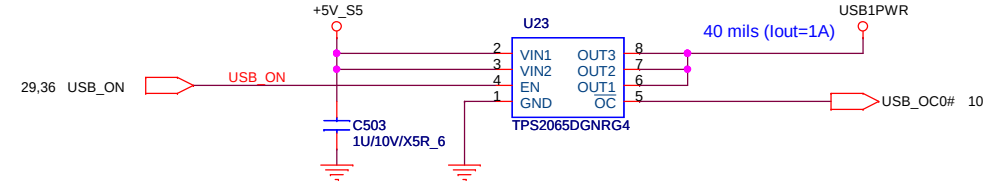
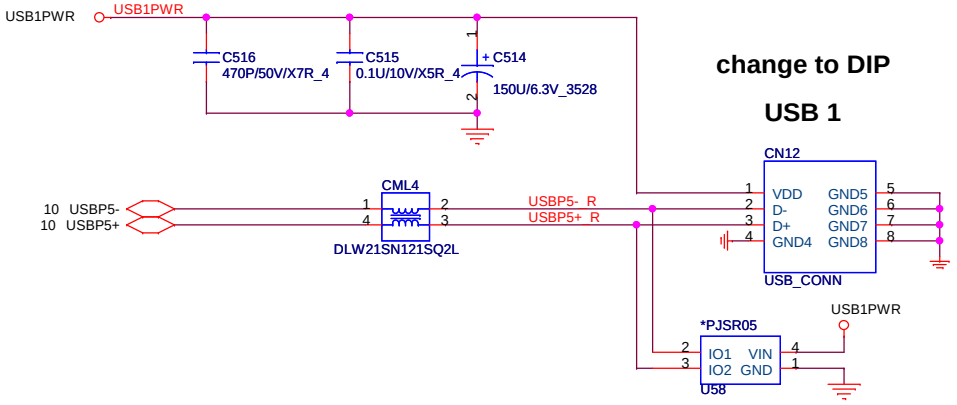
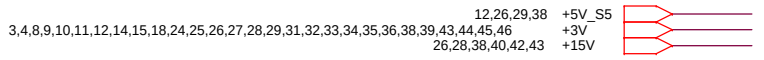
USBX3

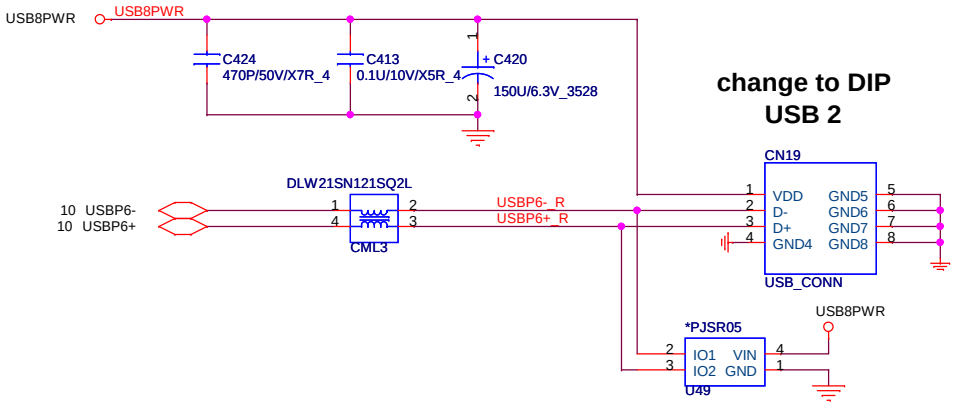


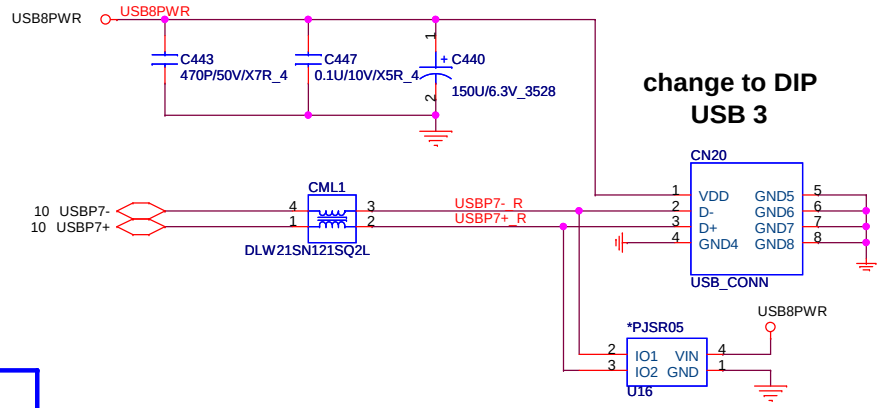


USB 1

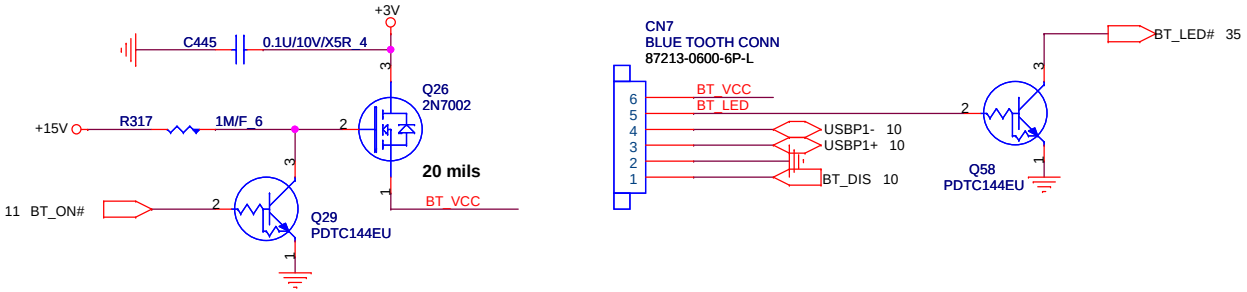


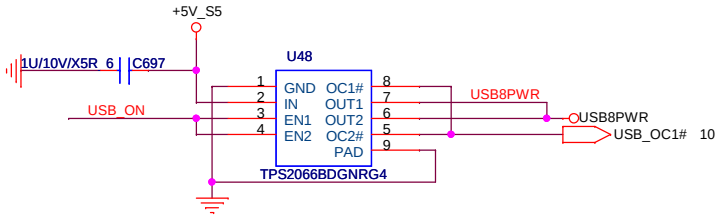
29





BLUETOOTH





PROJECT : KL2D		
Quanta Computer Inc.		
Size: Custom	Document Number: USB X3/BT	Rev: 1A
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3,4,8,9,10,11,12,14,15,18,24,25,26,27,28,29,30,32,33,34,35,36,38,39,43,44,45,46 +3V

7 IN 1 CARD READER

C640 & C639 close to APVDD(pin5)
(length must under 120mil) and
trace width = 30mil, after C640,
pls put one more 0.1uF for it.

+1.8V_VDD
C462 10U/6.3V/X5R_6
C468 0.1U/10V/X5R_4
C466 0.1U/10V/X5R_4
C735 0.1U/10V/X5R_4
C720 1000P/50V/X7R_4

+3V
R638 0_8
C732 10U/6.3V/X5R_6
C725 0.1U/10V/X5R_4
C715 0.1U/10V/X5R_4
C721 0.1U/10V/X5R_4
C712 0.1U/10V/X5R_4
+3V_CARD

JMB385 C Only
R662 *0_4

JMB387 A Only
R656 0_4

U54
JMB385 C
JMB387 A
JMICRON

XD_D4/MS_D4
XD_D5/MS_D5
XD_D6/MS_D6
XD_D7/MS_D7
XD_RE#
XD_R/B#
XD_ALE
PWR_CTRL
SD_MMC_CD#
MS_CD#
xD_CD#
CR_CPPE#
R636 *0_4/S
PCIE_CLKREQ_CAD# 10
EC C01

XD_CLE
XD_WP#/SD_WP/MMC_WP#
XD_CE#/MS_SCLK/SD_CLK_L
XD_WE#/MS_BS/SD_CMD
XD_D3/MS_D3/SD_D3
XD_D2/MS_D2/SD_D2
XD_D1/MS_D1/SD_D1
XD_D0/MS_D0/SD_D0

4,10,27,32 PLTRST#
PCIE_RX7+_C C709 0.1U/10V/X5R_4
PCIE_RX7-_C C708 0.1U/10V/X5R_4
PCIE_RXP7_CARD 10
PCIE_RXN7_CARD 10
10 CLK_PCIE_CADN
10 CLK_PCIE_CADP
R634 9.1K_4
PCIE_TXN7_CARD 10
PCIE_TXP7_CARD 10
Trace width = 12mil" at PREXT

CN11
R015-212-LM

XD_R/B#	1	(2)XD-R/B	(3)MS-DATA1	20	XD_D1/MS_D1/SD_D1
XD_RE#	2	(3)XD-RE	(2)MS-BS	21	XD_WE#/MS_BS/SD_CMD
XD_CE#/MS_SCLK/SD_CLK	3	(4)XD-CE	4IN1-GND2	22	
XD_CLE	4	(5)XD-CLE	(4)SD-VCC	23	VCC_XD
XD_ALE	5	(6)XD-ALE	(5)SD-CLK	24	XD_CE#/MS_SCLK/SD_CLK
XD_WE#/MS_BS/SD_CMD	6	(7)XD-WE	(7)SD-DAT0	25	XD_D0/MS_D0/SD_D0
XD_WP#/SD_WP/MMC_WP#	7	(8)XD-WP	(12)XD-D2	26	XD_D2/MS_D2/SD_D2
XD_D0/MS_D0/SD_D0	8	(10)XD-D0	(13)XD-D3	27	XD_D3/MS_D3/SD_D3
XD_D1/MS_D1/SD_D1	9	(11)XD-D1	(14)XD-D4	28	XD_D4/MS_D4
XD_D2/MS_D2/SD_D2	10	(9)SD-DAT2	(8)SD-DAT1	29	XD_D1/MS_D1/SD_D1
XD_D3/MS_D3/SD_D3	11	(1)SD-DAT3	(15)XD-D5	30	XD_D5/MS_D5
XD_WE#/MS_BS/SD_CMD	12	(2)SD-CMD	(16)XD-D6	31	XD_D6/MS_D6
	13	4IN1-GND1	(17)XD-D7	32	XD_D7/MS_D7
VCC_XD	14	(9)MS-VCC	(18)XD-VCC	33	VCC_XD
XD_CE#/MS_SCLK/SD_CLK	15	(8)MS-SCLK	(19)XD-CD-SW	34	XD_CD#
XD_D3/MS_D3/SD_D3	16	(7)MS-DATA3	SD-WP-SW	35	XD_WP#/SD_WP/MMC_WP#
MS_CD#	17	(6)MS-INS	SD-CD-SW	36	SD_MMC_CD#
XD_D2/MS_D2/SD_D2	18	(5)MS-DATA2			
XD_D0/MS_D0/SD_D0	19	(4)MS-DATA0			
			SHIELD1-GND	37	
			SHIELD2-GND	38	
			SHIELD3-GND	41	
			SHIELD4-GND	42	

Memory Card Power Supply

250mA
VCC_XD
PWR_CTRL

Use 0805 type and
Trace width = 30 mil"
at MC_PWR_CTRL#,
C719 0.1U/10V/X5R_4
C455 10U/6.3V/X5R_6
C452 1U/6.3V/X5R_4

XD_CE#/MS_SCLK/SD_CLK_L R649 22_4 XD_CE#/MS_SCLK/SD_CLK
C726 20P/50V/COG_4

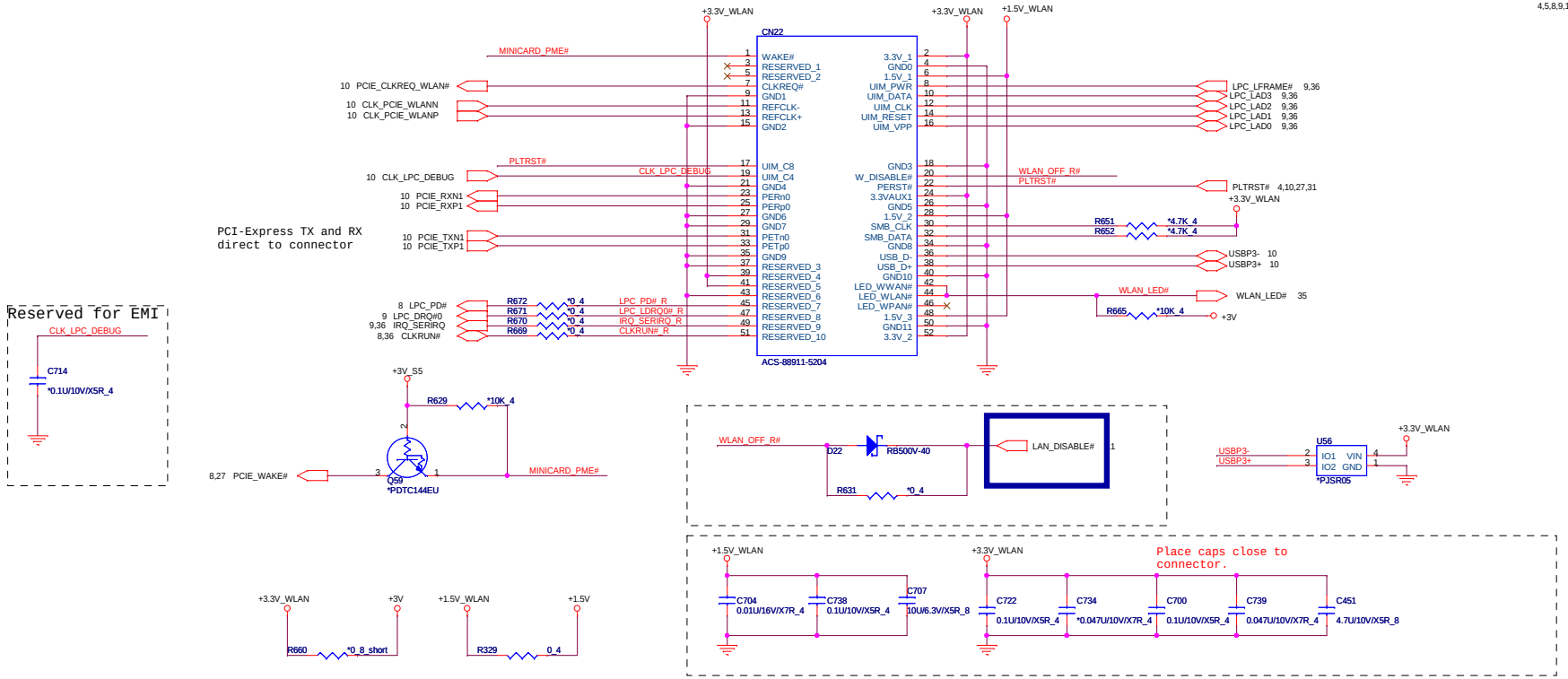
+3V_CARD
R637 4.7K_4 xD_CD#
R642 4.7K_4 MS_CD#
R643 4.7K_4 SD_MMC_CD#
R653 10K_4 XD_CLE

VCC_XD
R342 10K_4 XD_WE#/MS_BS/SD_CMD
R659 1K_4 XD_R/B#
R349 10K_4 XD_WP#/SD_WP/MMC_WP#
XD_RE# R663 200K_4
XD_ALE R655 200K_4

PROJECT : KL2D
Quanta Computer Inc.

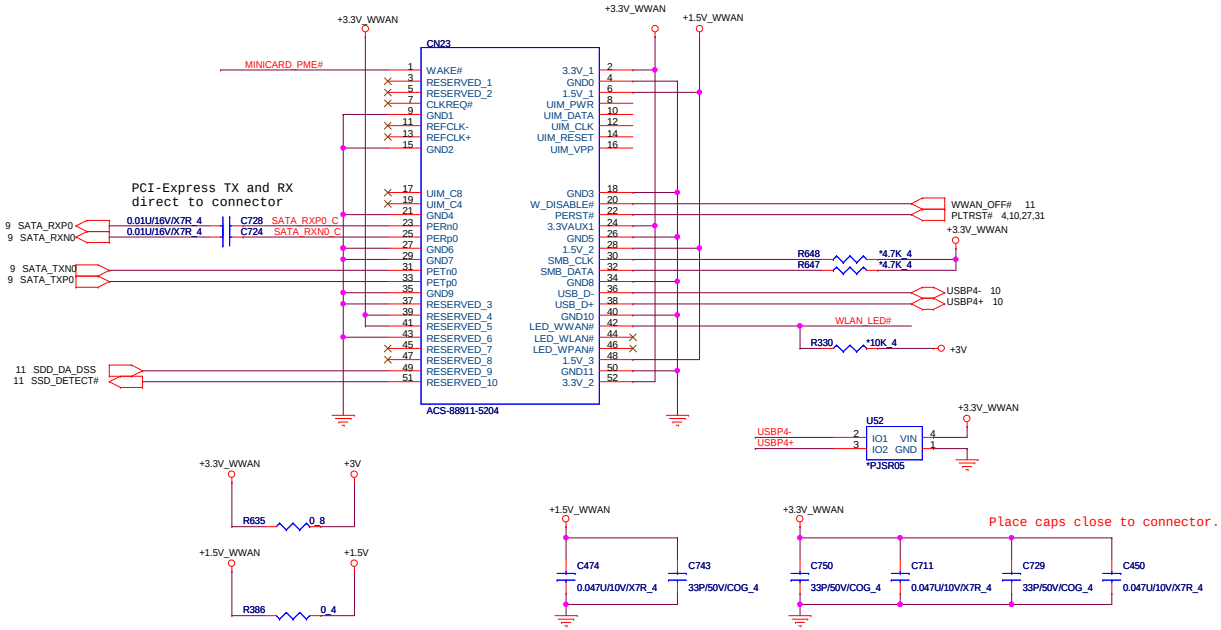
Size	Document Number	Rev
Custom	JMB385/387 Card Reader	1A
Date: Saturday, July 24, 2010	Sheet 31 of 47	

MiniCard WLA connector



MiniCard WWAN/SATA SSD connector

SIM Card CONN



FAN CONTROL

3,4,8,9,10,11,12,14,15,18,24,25,26,27,28,29,30,31,32,34,35,36,38,39,43,44,45,46 +3V
8,9,12,18,24,25,26,28,29,34,36,38,39 +5V

NOTE:
Place C625 near Q37

NOTE:
Place C623 near Q38

NOTE:
Place C624 near U48

NOTE:
Place C627 near Q39

NOTE:
Place C626 near U48

Q53
SST3904
C647
*100P/50V/X7R_4
DDR3

Q62
SST3904
C758
*100P/50V/X7R_4
WLAN-ONFI

C648
2200P/50V/X7R_4

R523 2.05K_4

R548
0_8
+5V_FAN
C660
1U/10V/X5R_6
C659
0.1U/10V/X5R_4

R522
6.8K/F_4

U42
EMC2103-2
DN
DP
VDD
GPIO1
DP2/DN3
DN2/DP3
TRIP_SET
SHDN_SEL
GND
PWM
TACH
SMCLK
GPIO2
ALERT#
SYS_SHDN#
SMDATA

R536 10K_4
R534 10K_4
R533 10K_4
R531 10K_4
R528 10K_4
R530 10K_4
R525 10K_4

D20
RB500V-40
+5V_FAN
FAN_PWM
FANSIG
CN16
FAN_CON

C631
*100P/50V/X7R_4
SST3904
Q52
CPU

C649
2200P/50V/X7R_4

+3V
R532 22_4 +3V_FAN
C650
0.1U/10V/X5R_4

Q54
2N7002
MB_CLK1 10,20,35,36

Q55
2N7002
MB_DATA1 10,20,35,36

SYS_SHDN-1#
Q56
2N7002
SYS_SHDN# 20,42

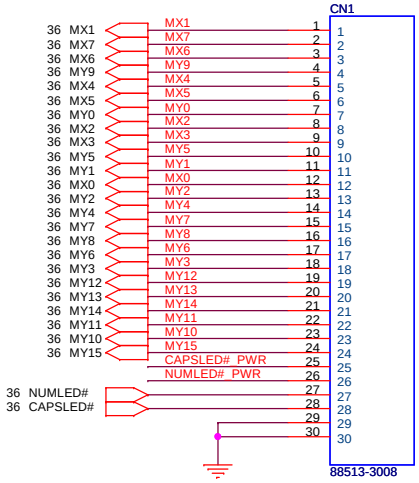
D21
*RB500V-40
TEMP_FAIL 17

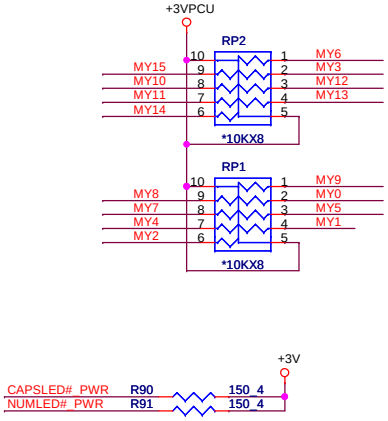
MB_ALRET#
R535 *0_4
TEMP_ALERT# 11,36

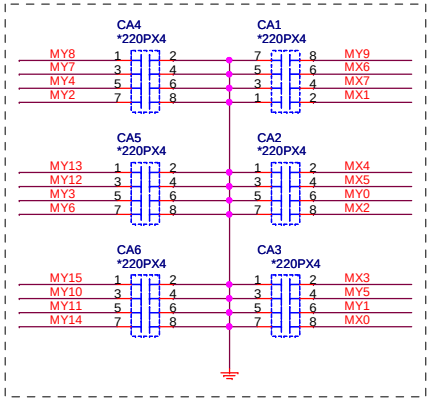
PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	FAN /THERMAL	1A
Date: Saturday, July 24, 2010	Sheet 33 of 47	

KEYBOARD



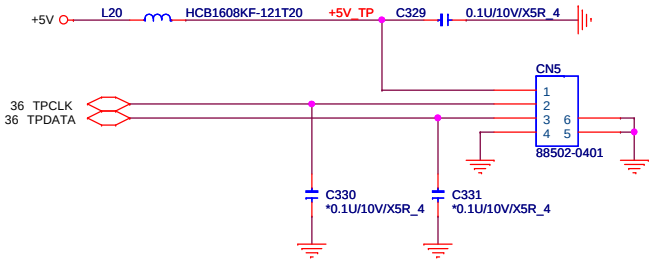




For EMI request

8,9,12,18,24,25,26,28,29,33,36,38,39 +5V
8,9,26,27,35,36,38,39,42,44,46 +3VPCU
26,28,30,38,40,42,43 +15V
3,4,8,9,10,11,12,14,15,18,24,25,26,27,28,29,30,31,32,33,35,36,38,39,43,44,45,46 +3V
5VSUS

Touch pad

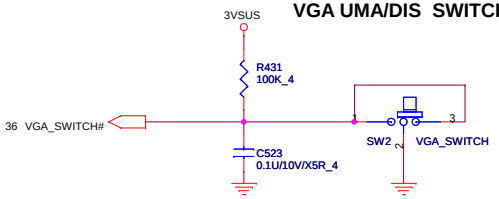


Backlight Keybaord Con.

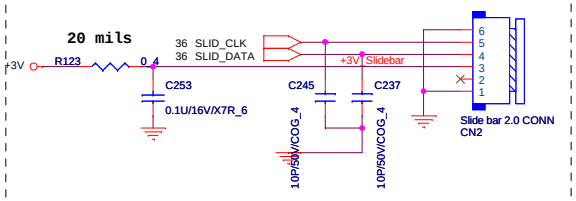
PROJECT : KL2D		
Quanta Computer Inc.		
Size: Custom	Document Number: K/B, T/P	Rev: 1A
Date: Saturday, July 24, 2010	Sheet 34 of 47	

8,9,26,27,34,36,38,39,42,44,46 +3VPCU
3,4,8,9,10,11,12,14,15,18,24,25,26,27,28,29,30,31,32,33,34,36,38,39,43,44,45,46 +3V
36,38,44 3VSUS

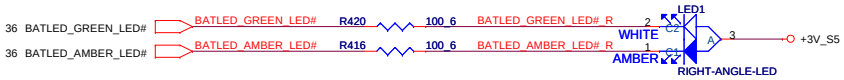
VGA UMA/DIS SWITCH



Slide bar 2.0

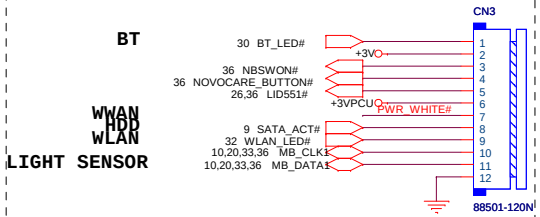


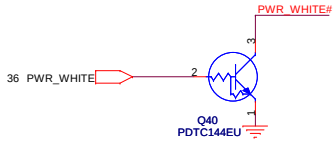
VGA

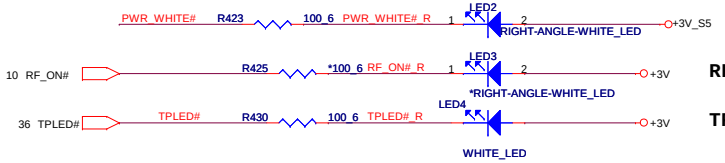


Battery

POWER BOARD







Power/suspend LED

RF

TP

Logo LED CONN

5VPCU Cable for CPU Core Power

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	B TO B CON/LED	1A
Date: Saturday, July 24, 2010	Sheet 35 of 47	

IT8518 IT8519

RF ON/OFF SWITCH

POWER SWITCH/ NOVO BUTTON

16Mbit (2M Byte), SPI

Winbond AKE38ZP0N00
SST AKE28FP0K07
MX AKE37FP0Z13

Borad ID

DIS =>R275
UMA=>R274

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

EMI suggestion:
Add a 15p bypass CAP on CLK_PCI_8512

(For PLL Power)

Rev.B

PROJECT	KL2D
Quanta Computer Inc.	
Size	Custom
Document Number	KBC IT8512E
Rev	1A
Date:	Saturday, July 24, 2010
Sheet	36 of 47

MiniCard WLAN

HOLE28 H-TC197D79PT
HOLE30 H-TC197D79PT

MiniCard WWAN

HOLE31 H-TC197D79PT

Hole for PCH support

HOLE24 H-TC197D59PT
HOLE27 H-TC197D59PT
HOLE32 H-TC197D79PT
HOLE33 H-TC197D79PT
HOLE34 H-TC197D79PT
HOLE35 H-TC197D79PT
HOLE36 H-TC197D79PT
HOLE37 H-TC197D79PT

Hole for CPU support

HOLE4 *H-C142D142N
HOLE8 *H-C142D142N
HOLE5 *H-C142D142N
HOLE7 *h-bc142tc221d142pt

VGA nut

HOLE20 H-TC197BC138I102D102P2
HOLE22 H-TC197BC138I102D102P2

PAD

HOLE25 *SPAD-S79
HOLE26 *SPAD-S79
HOLE21 *SPAD-S83X71
HOLE23 *SPAD-S87X73

Boundary Hole

HOLE1 *h-sd106p2-kl2
HOLE11 *H-C315I3146BO378D106P2
HOLE15 *H-C118D118N
HOLE18 *H-C315I126D106P2
HOLE19 *H-C315I126D106P2
HOLE13 *H-TC197BC256D106P2
HOLE17 *H-C315I126D106P2
HOLE16 *H-C315I126D106P2
HOLE14 *H-C118D118N
HOLE9 *H-TC197BC256D106P2
HOLE3 *H-C315I126D106P2

ESD Mask Copper

CO1 CO2 CO3 CO4 CO5 CO6 CO7 CO8 CO9 CO10 CO11 CO12
CO13 CO14 CO15 CO16 CO17 CO18 CO19 CO20 CO21 CO22

Boundary Hole

HOLE2 *H-TC197BC256D106P2
HOLE6 *O-KL2-1
HOLE12 *O-KL2-2

HDD PAD

EC QV08

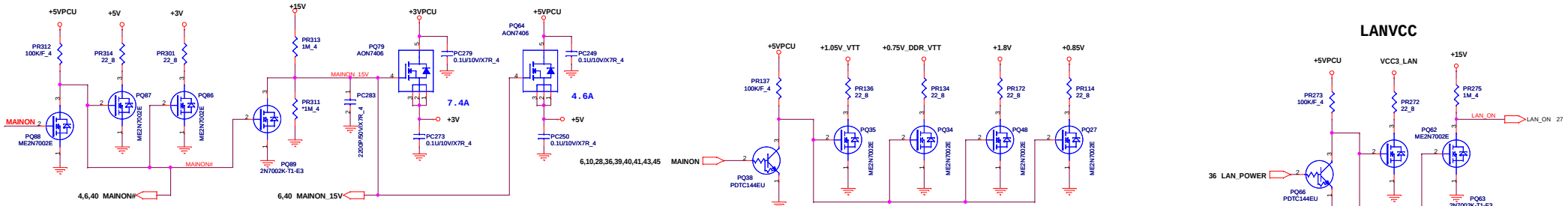
HOLE10 *H-O158X355D158X355N

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HOLD & SKEW	1A
Date: Saturday, July 24, 2010	Sheet 37 of 47	

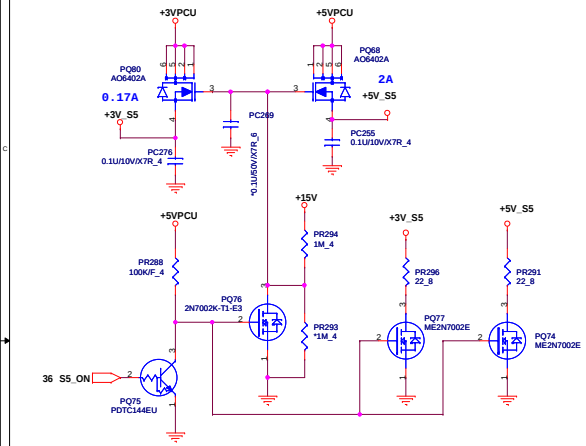
DISCHARGE

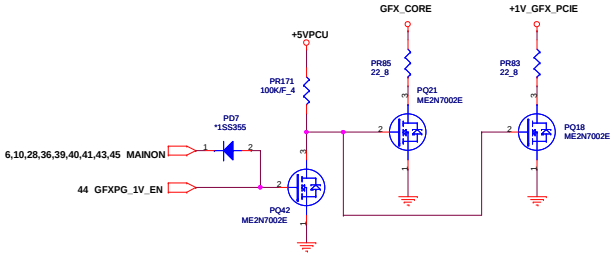
+3V, +5V

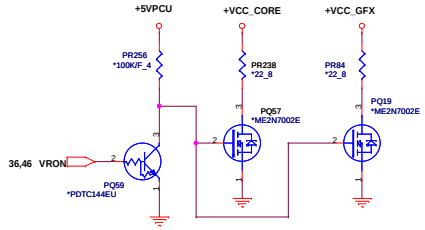


LANVCC

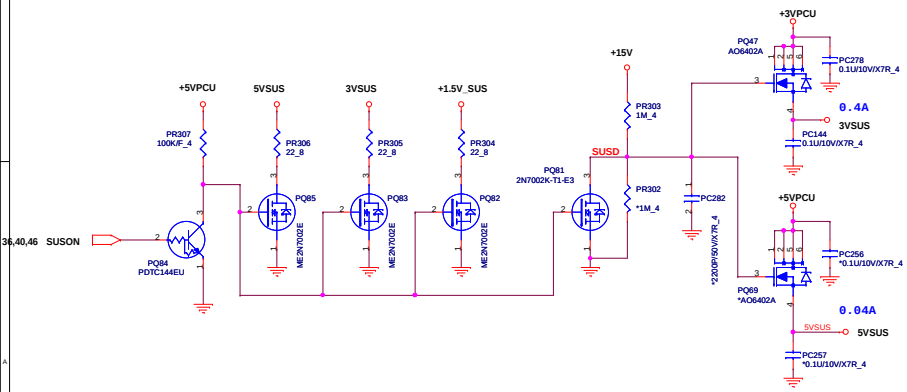
3V_S5, 5V_S5

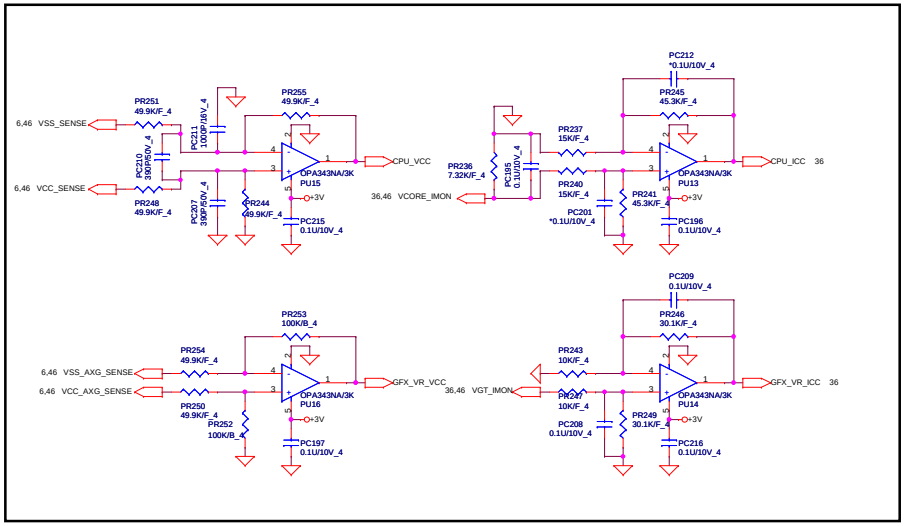






3VSUS, 5VSUS



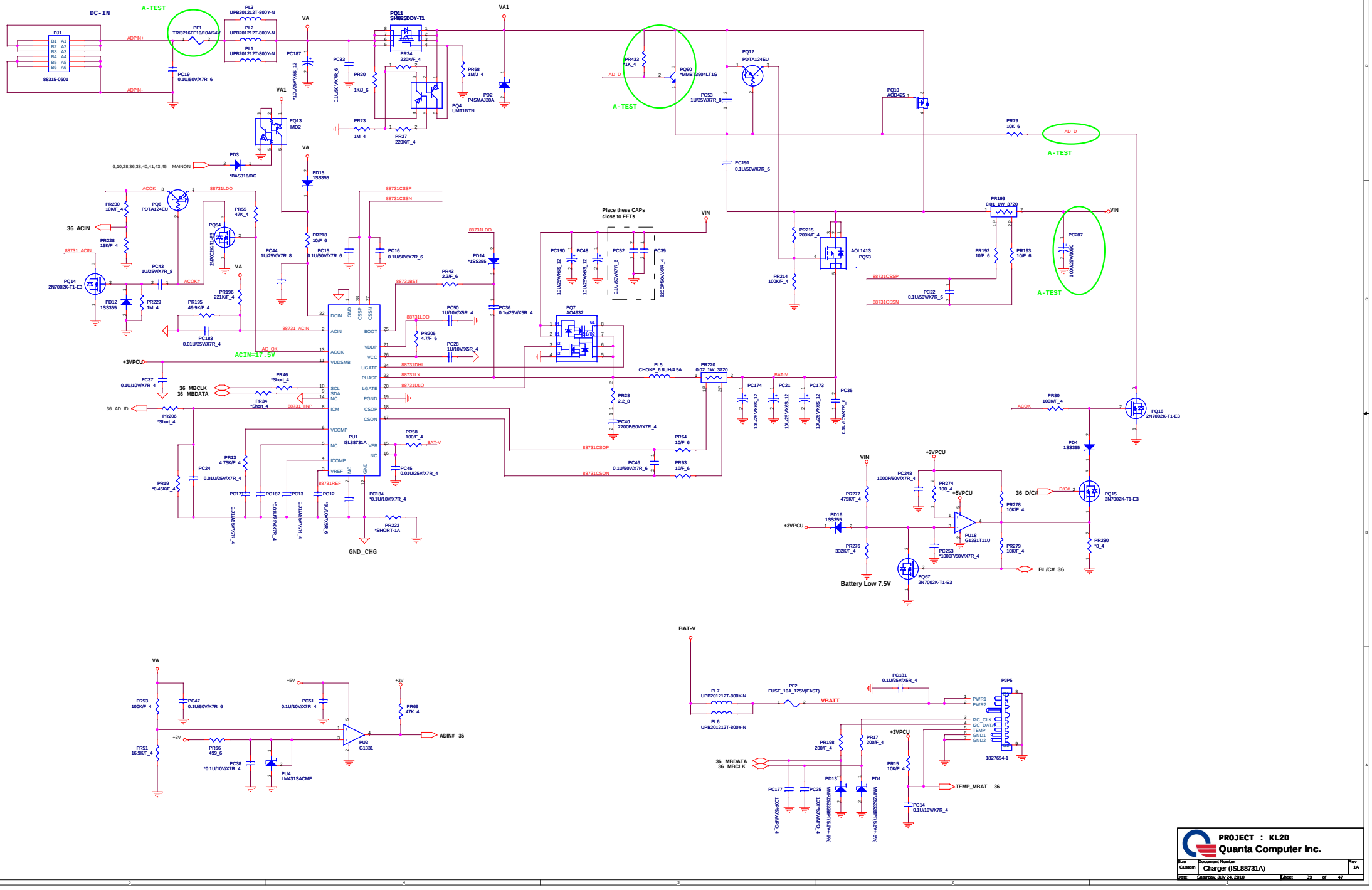


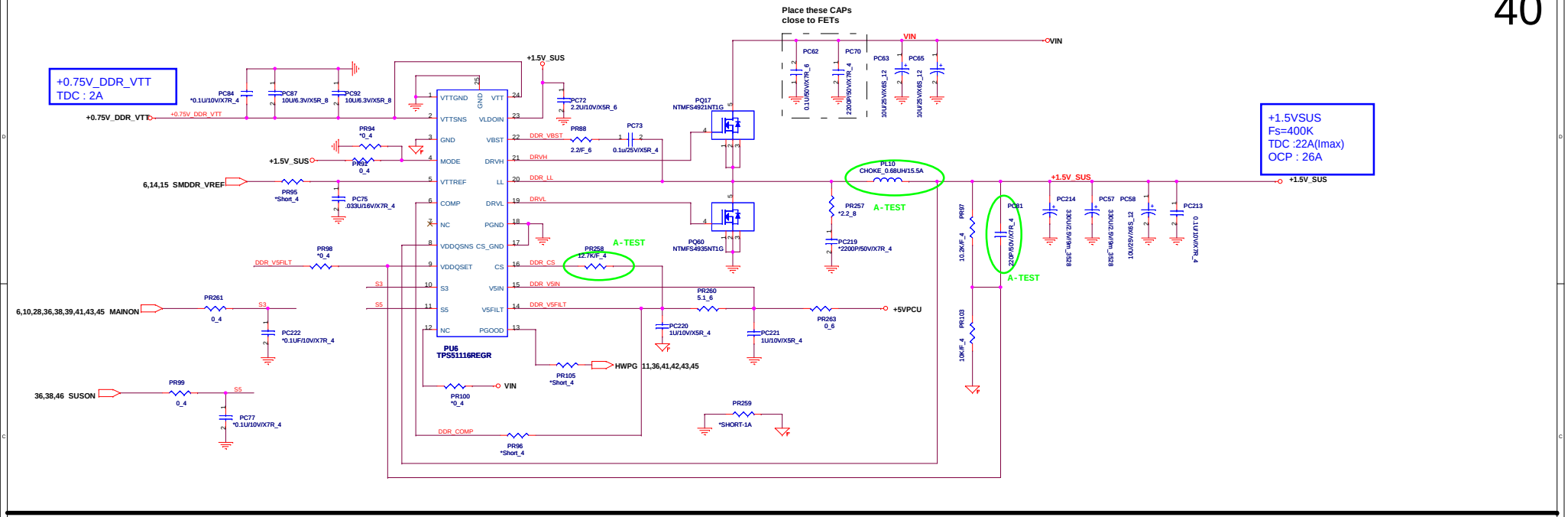
PROJECT : KL2D

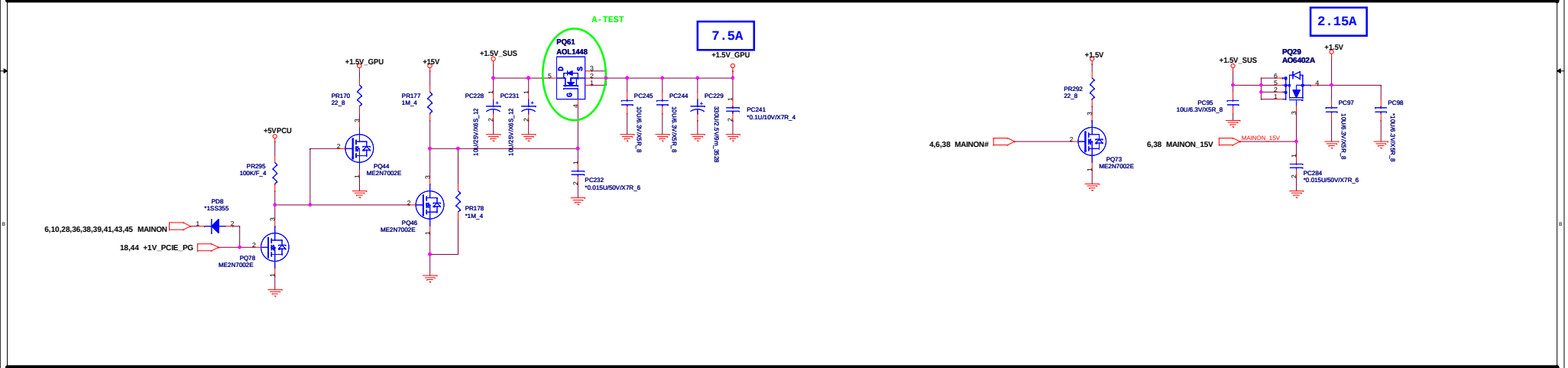
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Discharge	1A

Date: Saturday, July 24, 2010 Sheet 38 of 47


DC-IN
A-TEST
PJ1
88315-0601
ADPIN+
ADPIN-
PF1
TR/3216FF10/10A/24V
PL3
UPB201212T-800Y-N
PL2
UPB201212T-800Y-N
PL1
UPB201212T-800Y-N
PC19
0.1U/50V/X7R_6
VA
PC187
*10U/25V/X6S_12
PQ11
SM3825DDY-T1
PC33
0.1U/50V/X7R_6
PR20
1KU_6
PR24
220K/F_4
PR68
1MU_4
PD2
P4SMAJ20A
PQ4
UMT1NTN
PR23
1M_4
PR27
220K/F_4
VA1
PQ13
IMD2
PD3
*BAS316/DG
6,10,28,36,38,40,41,43,45
MAINON
PR433
1K_4
PQ90
*MMBT3904LT1G
AD_D
A-TEST
PQ12
PDTA124EU
PC53
1U/25V/X7R_8
PQ10
AOD425
PC191
0.1U/50V/X7R_6
PR79
10K_6
AD_D
A-TEST
PD15
1SS355
ACOK
88731LDO
PQ6
PDTA124EU
PR230
10K/F_4
PR55
47K_4
36 ACIN
PR228
15K/F_4
88731_ACIN
PQ54
2N7002K-T1-E3
PQ14
2N7002K-T1-E3
PD12
1SS355
PR229
1M_4
PC43
1U/25V/X7R_8
ACOK#
PR196
221K/F_4
PR195
49.9K/F_4
PC183
0.01U/25V/X7R_4
88731_ACIN
AC_OK
ACIN=17.5V
PC44
1U/25V/X7R_8
PR218
10/F_6
PC15
0.1U/50V/X7R_6
PC16
0.1U/50V/X7R_6
88731CSSP
88731CSSN
88731LDO
PD14
*1SS355
PR43
2.2/F_6
88731BST
PC36
0.1u/25V/X5R_4
PC50
1U/10V/X5R_4
88731LDO
PR205
4.7/F_6
PC28
1U/10V/X5R_4
88731DHI
88731LX
88731DLO
DCIN
ACIN
ACOK
VDDSMB
SCL
SDA
NC
ICM
VCOMP
NC
ICOMP
VREF
CSSP
CSSN
BOOT
VDDP
VCC
UGATE
PHASE
LGATE
PGND
CSOP
CSON
VFB
NC
GND
PU1
ISL88731A
+3VPCU
PC37
0.1U/10V/X7R_4
PR46
*Short_4
36 MBCLK
36 MBDATA
PR34
*Short_4
88731_INP
36 AD_ID
PR206
*Short_4
PR58
100/F_4
BAT-V
PC45
0.01U/25V/X7R_4
PR64
10/F_6
PR63
10/F_6
88731CSOP
88731CSON
PC46
0.1U/50V/X7R_6
PR13
4.75K/F_4
PC24
0.01U/25V/X7R_4
PR19
*8.45K/F_4
PC177
PC182
PC13
PC12
PC184
*0.1U/10V/X7R_4
PR222
*SHORT-1A
GND_CHG
Place these CAPs
close to FETs
VIN
PC190
PC48
PC52
PC39
PQ7
AO4932
PL5
CHOKE_6.8UH/4.5A
PR220
0.02_1W_3720
PC174
PC21
PC173
PC35
BAT-V
PR28
2.2_8
PC40
2200P/50V/X7R_4
PR215
200K/F_4
AOL1413
PQ53
PR214
100K/F_4
PC22
0.1U/50V/X7R_6
88731CSSP
88731CSSN
PR199
0.01_1W_3720
PR192
10/F_6
PR193
10/F_6
PC287
100U/25V/DC
VIN
A-TEST
PR80
100K/F_4
ACOK
PQ16
2N7002K-T1-E3
PD4
1SS355
PQ15
2N7002K-T1-E3
D/C#
36 D/C#
VIN
+3VPCU
PC248
1000P/50V/X7R_4
PR274
100_4
+5VPCU
PR277
475K/F_4
PR278
10K/F_4
PD16
1SS355
+3VPCU
PU18
G1331T11U
PC253
*1000P/50V/X7R_4
PR279
10K/F_4
PR280
*0_4
PR276
332K/F_4
PQ67
2N7002K-T1-E3
BL/C# 36
Battery Low 7.5V
VA
PR53
100K/F_4
PC47
0.1U/50V/X7R_6
PR51
16.9K/F_4
+5V
PC51
0.1U/10V/X7R_4
+3V
PR66
499_6
PC38
*0.1U/10V/X7R_4
PU4
LM431SACMF
+3V
PR69
47K_4
PU3
G1331
ADIN# 36
BAT-V
PL7
UPB201212T-800Y-N
PL6
UPB201212T-800Y-N
PF2
FUSE_10A_125V(FAST)
VBATT
PC181
0.1U/25V/X5R_4
PJP5
PWR1
PWR2
I2C_CLK
I2C_DAT
TEMP
GND1
GND2
1827654-1
PR198
200/F_4
PR17
200/F_4
+3VPCU
PR15
10K/F_4
TEMP_MBAT 36
36 MBDATA
36 MBCLK
PC177
PC25
PD13
PD1
PC14
0.1U/10V/X7R_4
PROJECT : KL2D
Quanta Computer Inc.
Size
Custom
Document Number
Charger (ISL88731A)
Rev
1A
Date: Saturday, July 24, 2010
Sheet 39 of 47

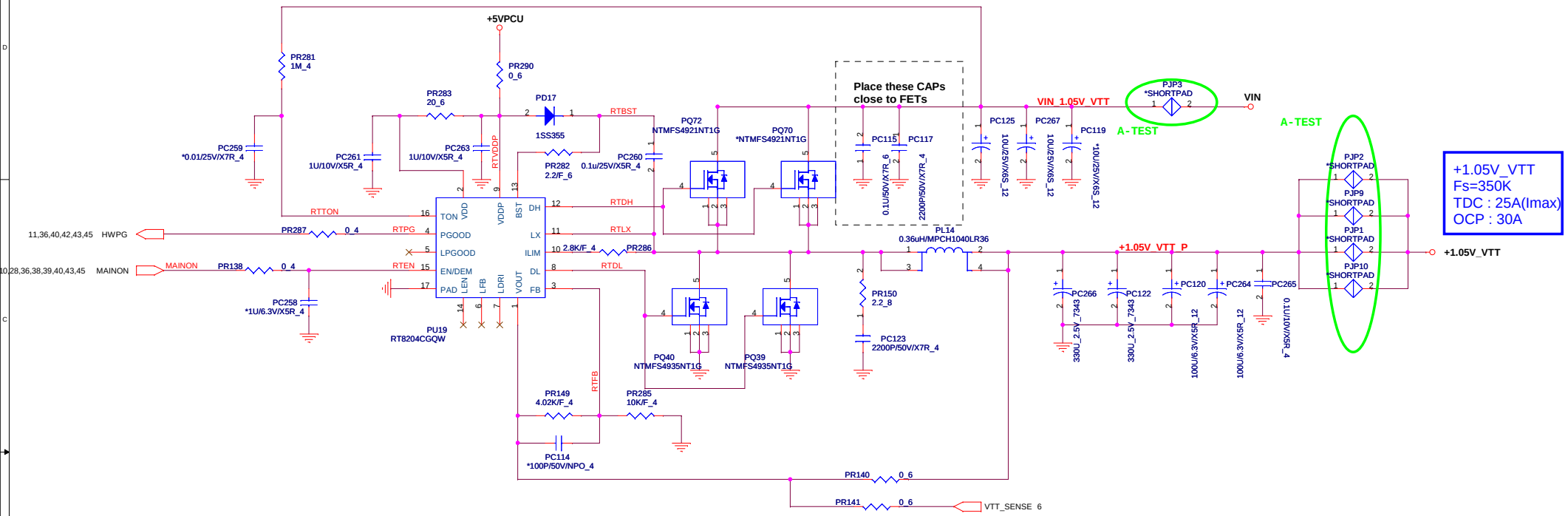




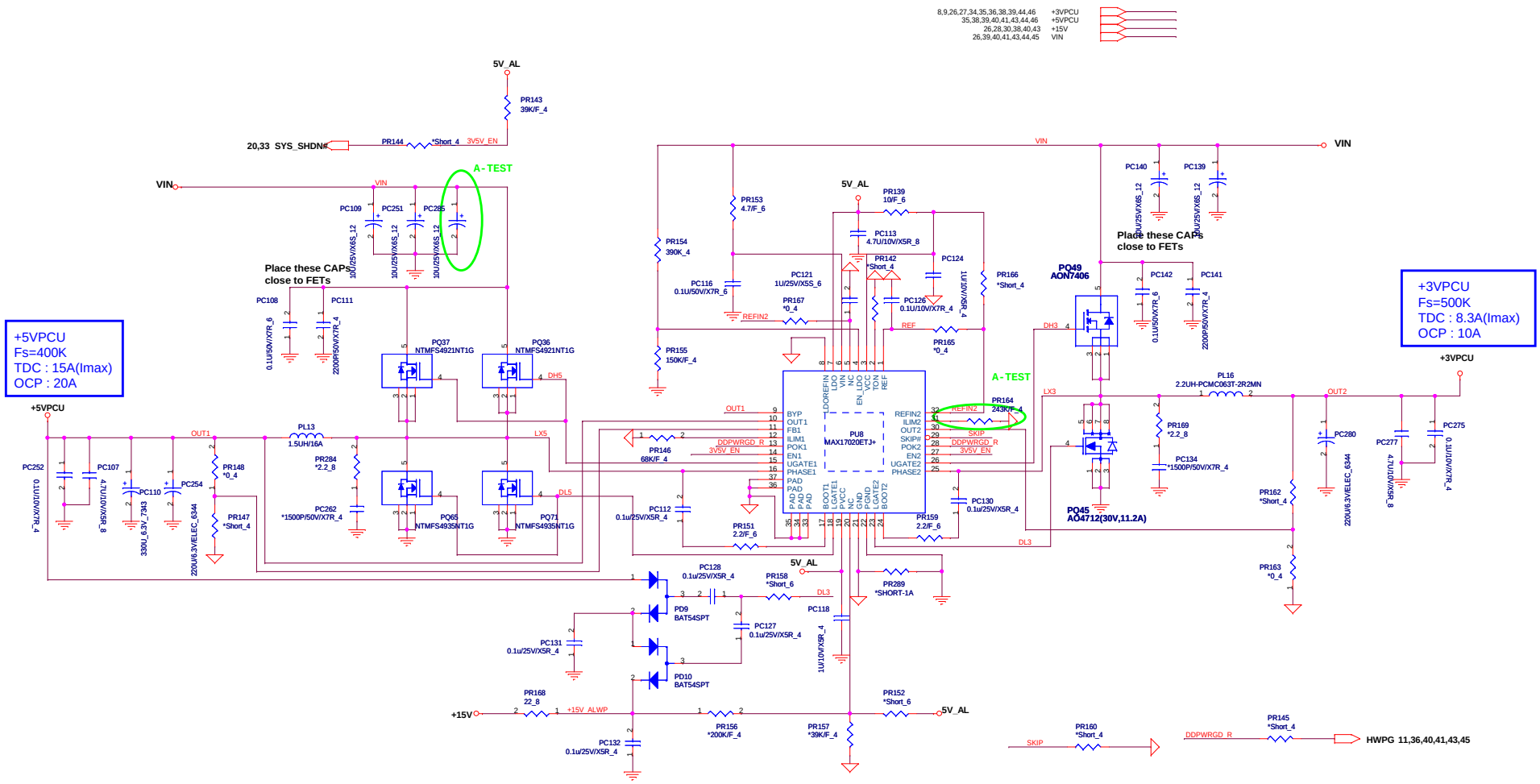
For S3 Power Saving

PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3/0.75V (TPS51116REGR)	1A
Date: Saturday, July 24, 2010	Sheet 40 of 47	



PROJECT : KL2D		
Quanta Computer Inc.		
Size: Custom	Document Number: 1.05V_VTT (RT8204)	Rev: 1A
Date: Saturday, July 24, 2010	Sheet 41 of 47	



PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
C	3V/5V (MAX17020ETJ+)	1A

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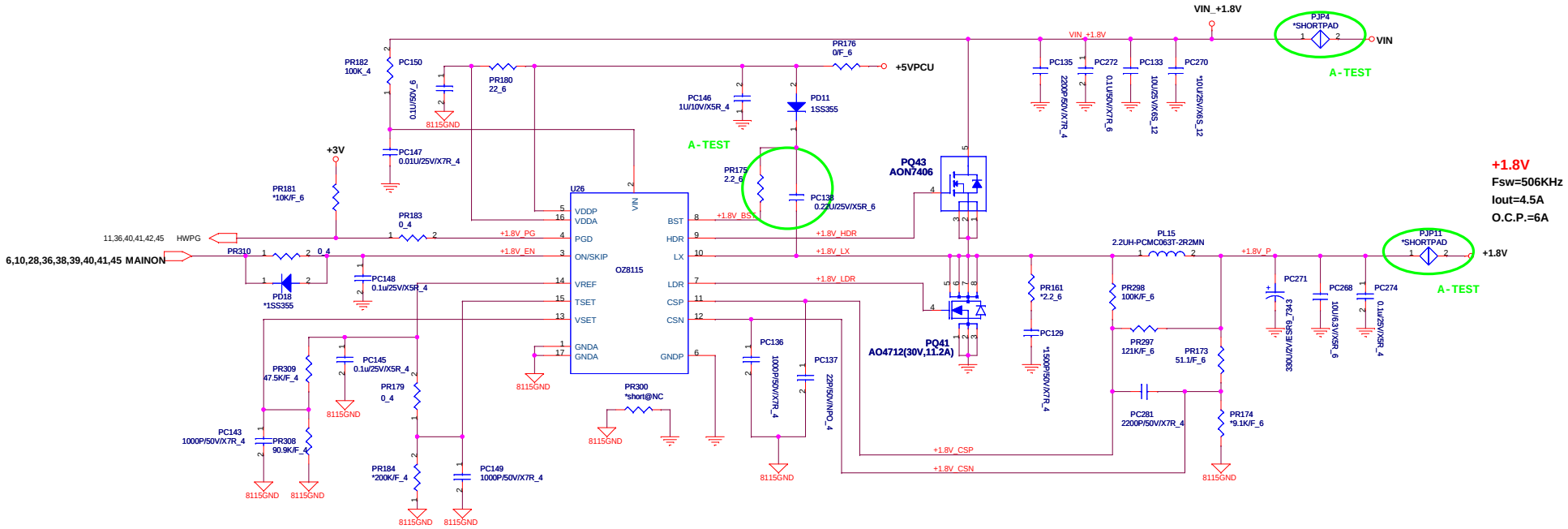

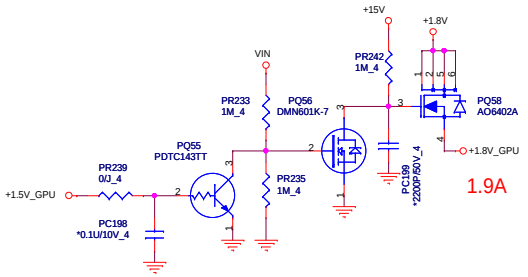

PROJECT : KL2D
Quanta Computer Inc.

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			A
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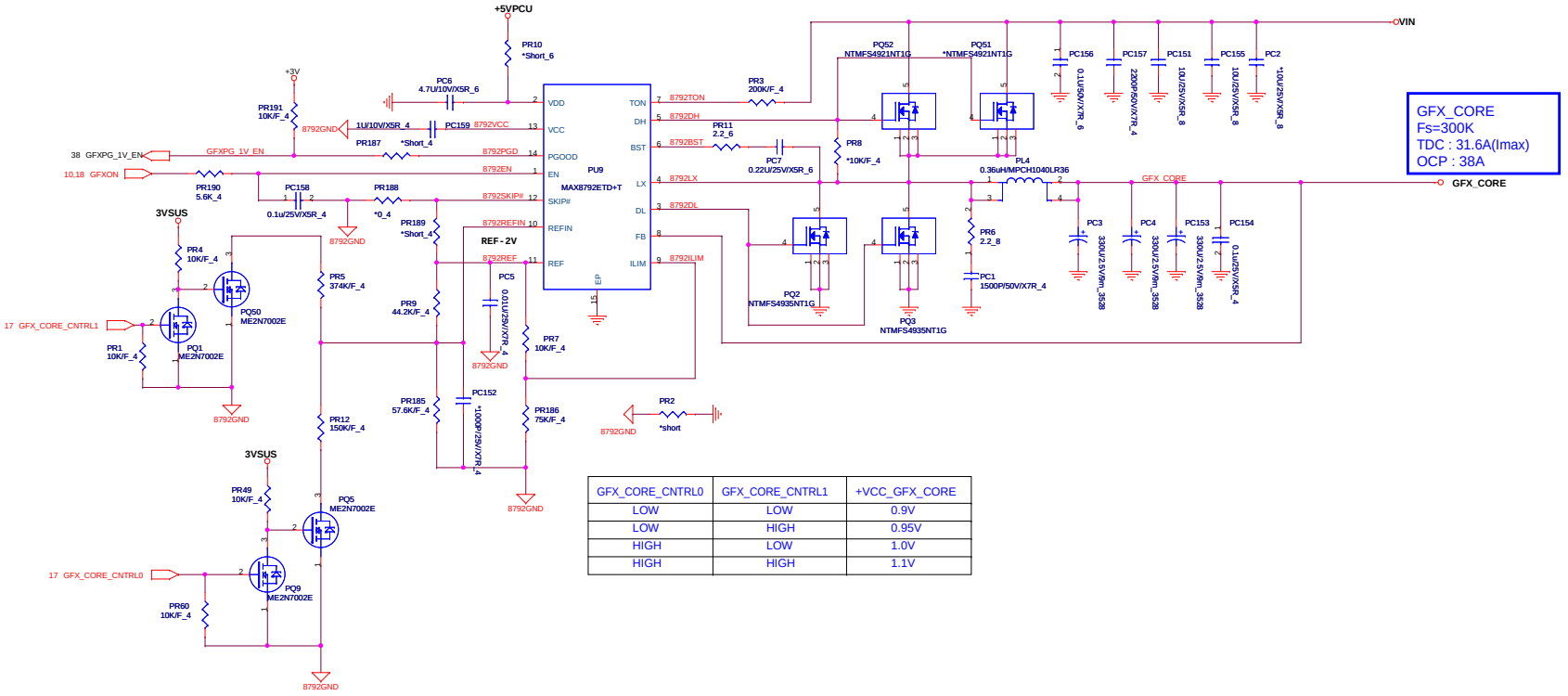
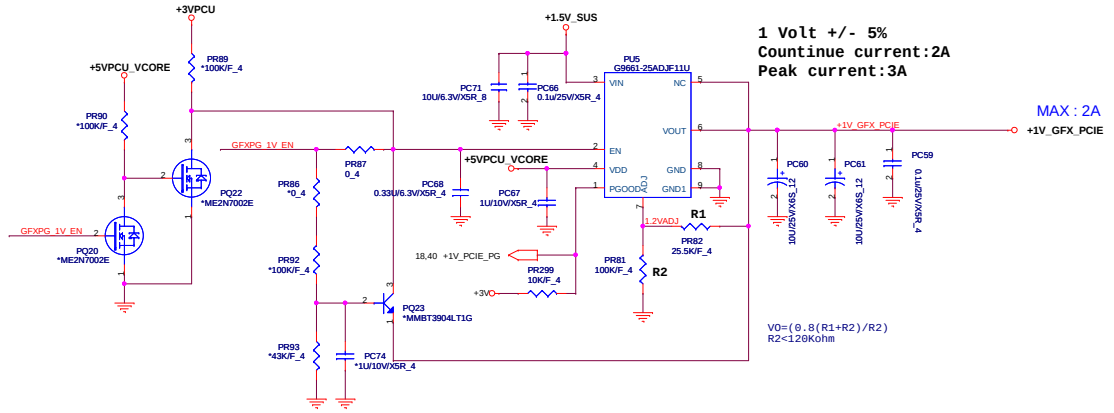
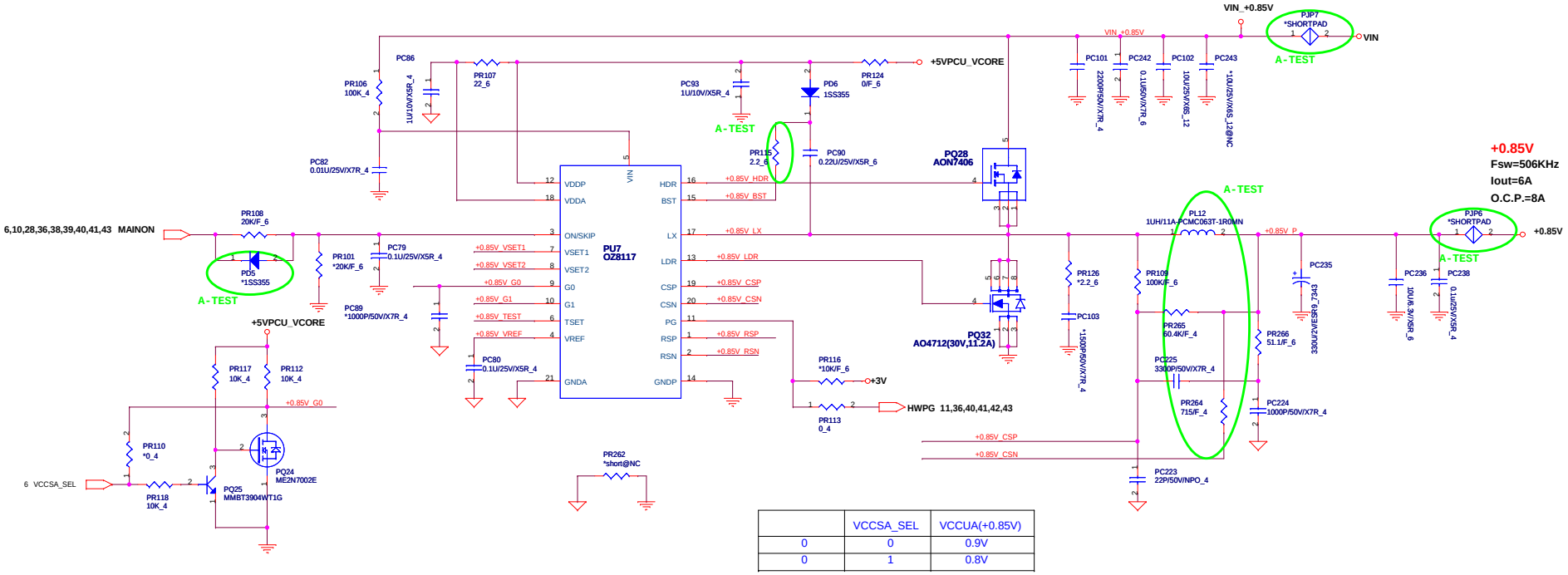


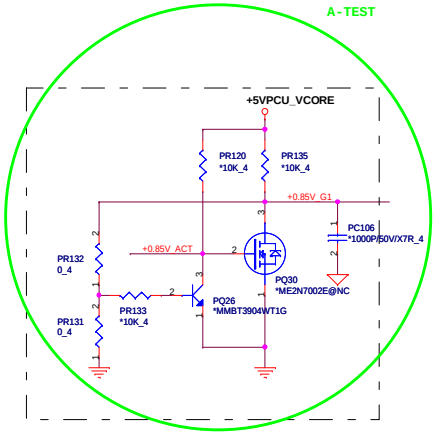
GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
LOW	HIGH	0.95V
HIGH	LOW	1.0V
HIGH	HIGH	1.1V



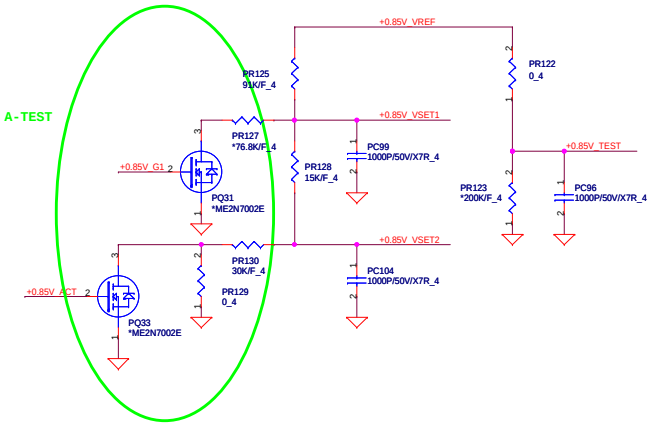
Quanta Computer Inc.	PROJECT : KL2D	
Size: Custom	Document Number: DIS_GFX_VCC (MAX8792)	Rev: 1A
Date: Saturday, July 24, 2010	Sheet 44 of 47	

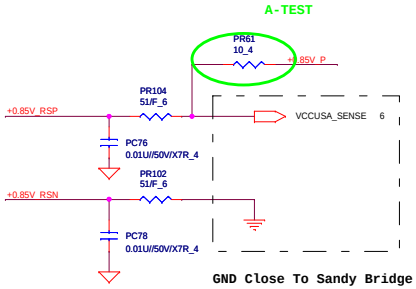


	VCCSA_SEL	VCCUA(+0.85V)
0	0	0.9V
0	1	0.8V



For Sandy Bridge And IV Bridge VID Select





GND Close To Sandy Bridge Processor (POWER) Side

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Quanta Computer Inc.
<Project Name>

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	+0.85V (uP6112)	1A

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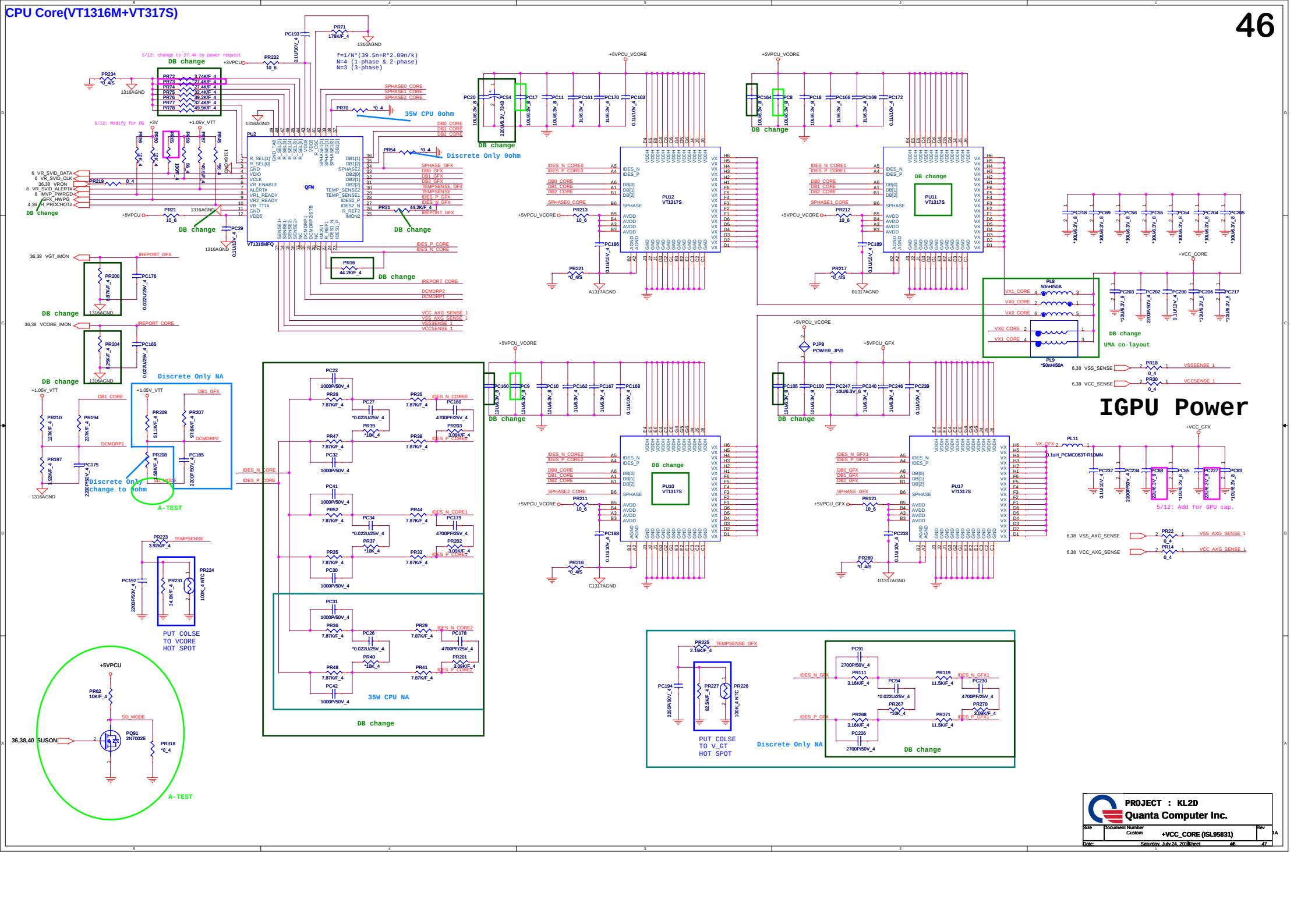
f=1/N*(39.5n+R*2.09n/k)
N=4 (1-phase & 2-phase)
N=3 (3-phase)
35W CPU 0ohm
Discrete Only 0ohm
DB change
Discrete Only NA
Discrete Only change to 0ohm
A-TEST
PUT COLSE TO VCORE HOT SPOT
35W CPU NA
PUT COLSE TO V_GT HOT SPOT
UMA co-layout
IGPU Power
5/12: Add for GPU cap.
PROJECT : KL2D
Quanta Computer Inc.
+VCC_CORE (ISL95831)
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EC #	Page	Description	Part Affected