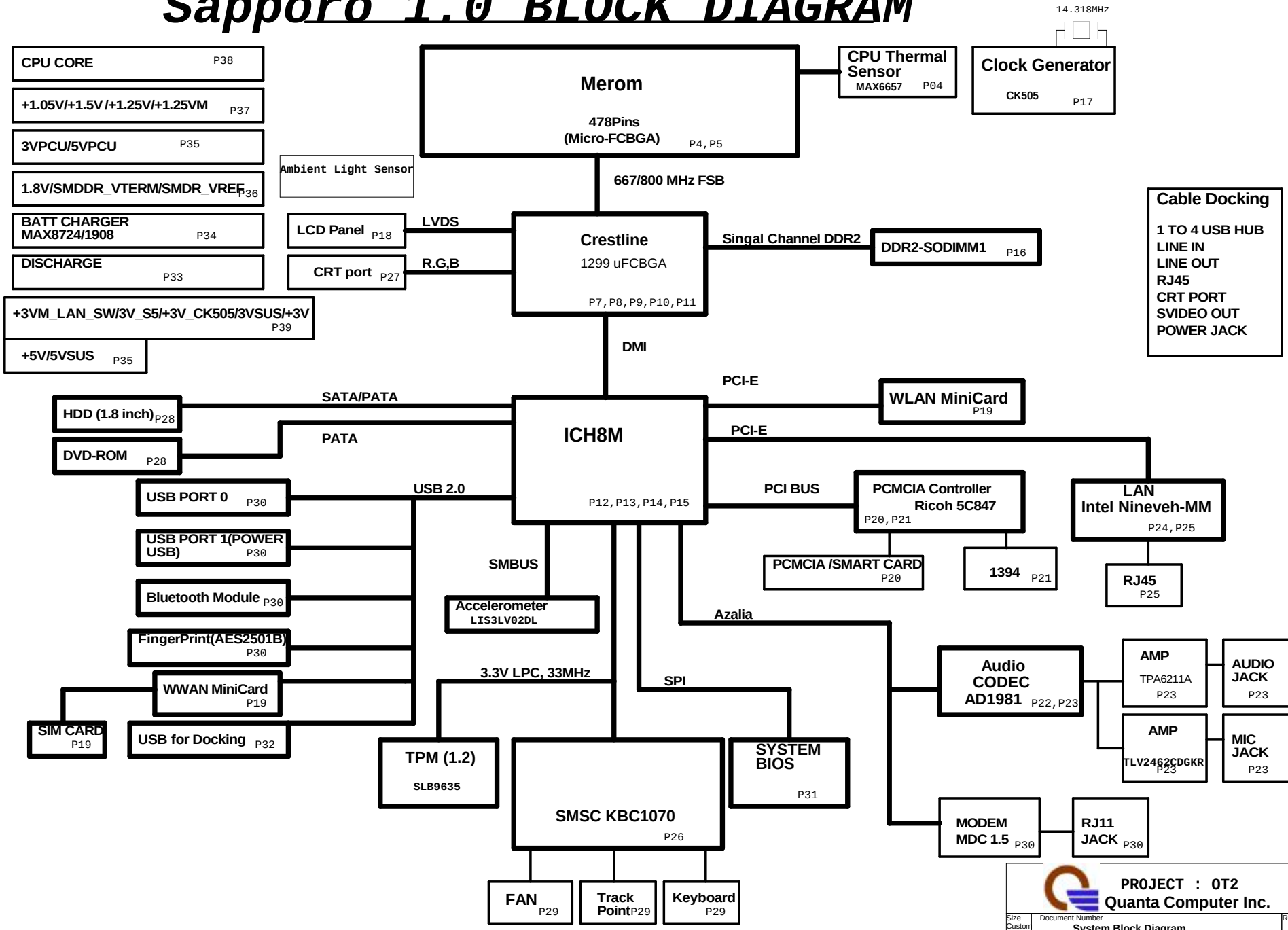
Sapporo 1.0 BLOCK DIAGRAM



PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	System Block Diagram	1A

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7-11	Crestline_	
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18	LCD CONNECTOR / LCD PWR	
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31	POWER SEQUENCE,BIOS	
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34	-CHARGER(MAX1908/8724)	
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36	MAX1992(1.8VSUS/DDR_VTERM)	
37	MAX1540 (+1.05V/+1.5V)	
38	--MAX8736	
39	+3VM/+3V_S5/1.25V_M	
40	POWER SEQUENCE	

Power & Ground

Label	ACTIVE	Description	Control Signal
VIN	S0, S3, S4, S5.M0.M1.Moff	AC ADAPTER (19V)	
MBAT	S0, S3, S4, S5.M0.M1.Moff	MAIN BATTERY + (10~17V)	
VCCRTC	S0, S3, S4, S5.M0.M1.Moff	RTC & KBC POWER (3_3V)	
+15V	S0, S3, S4, S5.M0.M1.Moff	+15V	
CPU_CORE	S0	CPU CORE POWER (1.25/1.15V)	VRON
+1.05V	S0	FSB POWER (1.05V)	MAIND
+1.05VM	M0.M1		IAMT_ON
+3V	S0		MAIND
3VSUS	S0, S3		SUSON
3V_S5	S0, S3, S4, S5		S5_ON
3VPCU	S0, S3, S4, S5.M0.M1.Moff	ALWAYS POWER (3V)	
+5V	S0		MAIND
5VSUS	S0, S3		SUSON
5V_S5	S0, S3, S4, S5		S5_ON
5VPCU	S0, S3, S4, S5.M0.M1.Moff	ALWAYS POWER (5V)	
+1.5V	S0		MAIND
+1.5VM	M0.M1		IAMT_ON
1.8VSUS	S0, S3	DDR CORE POWER	SUSON
+2.5V	S0		MAINON
SMDDR_VTERM	S0	DDR COMMAND & CONTROL PULL UP POWER	MAINON
SMDDR_VREF	S0, S3	DDR REF POWER	SUSON
VDDA	S0	AUDIO ANALOG POWER (5V)	MAINON
+3V_CK505	M0.M1		IAMT_ON
+3V_LAN_SW	M0.M1		IAMT_ON
+1.25V	S0		MAIND
+1.25VM	M0.M1		IAMT_ON

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT

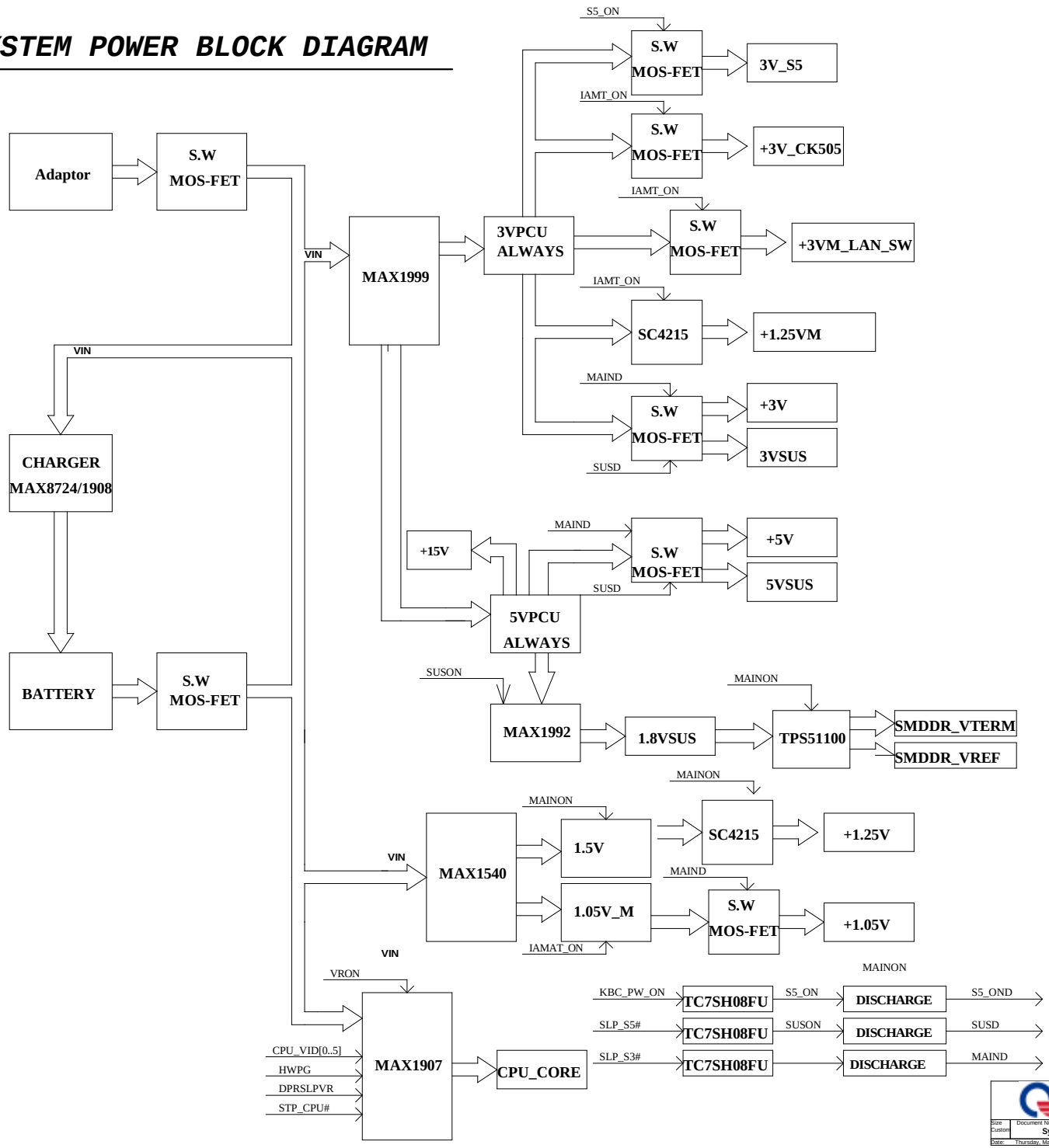
PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

SM BUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR II		
Accelemter sensor		
CHARGER		
CPU THERMAL SENSOR		

SYSTEM POWER BLOCK DIAGRAM



PROJECT : OT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	System pwr block diagram	1A

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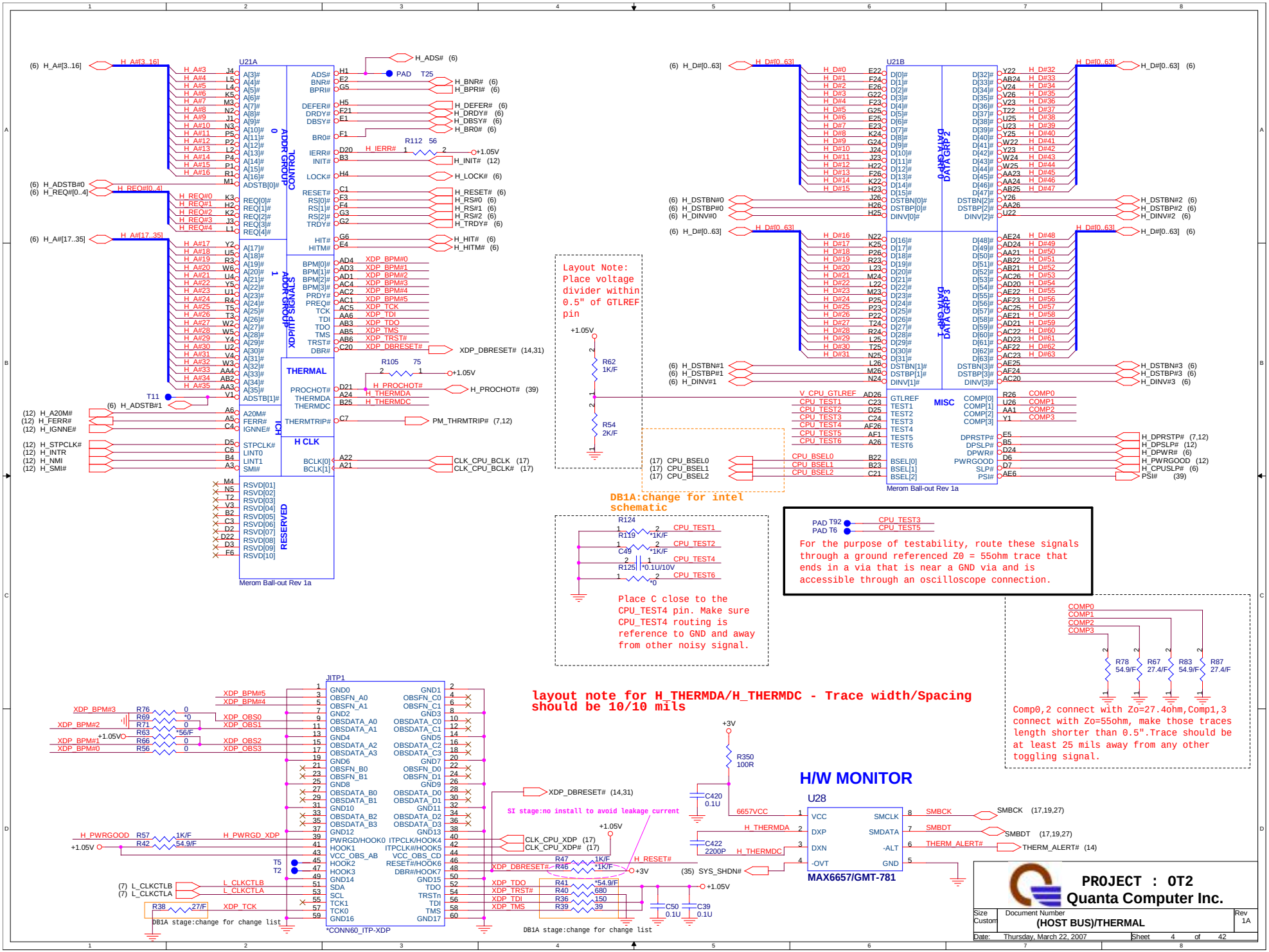
U21A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
ADDR GROUP 1
XDP/ITP SIGNALS
THERMAL
ICH
H CLK
RESERVED
Merom Ball-out Rev 1a
U21B
DATA GRP 2
DATA GRP 3
MISC
Merom Ball-out Rev 1a
Layout Note: Place voltage divider within 0.5" of GTLREF pin
DB1A:change for intel schematic
Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.
For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.
Comp0,2 connect with Zo=27.4ohm,Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5".Trace should be at least 25 mils away from any other toggling signal.
layout note for H_THERMDA/H_THERMDC - Trace width/Spacing should be 10/10 mils
JITP1
*CONN60_ITP-XDP
DB1A stage:change for change list
SI stage:no install to avoid leakage current
H/W MONITOR
U28
MAX6657/GMT-781
PROJECT : 0T2
Quanta Computer Inc.
Size Custom
Document Number (HOST BUS)/THERMAL
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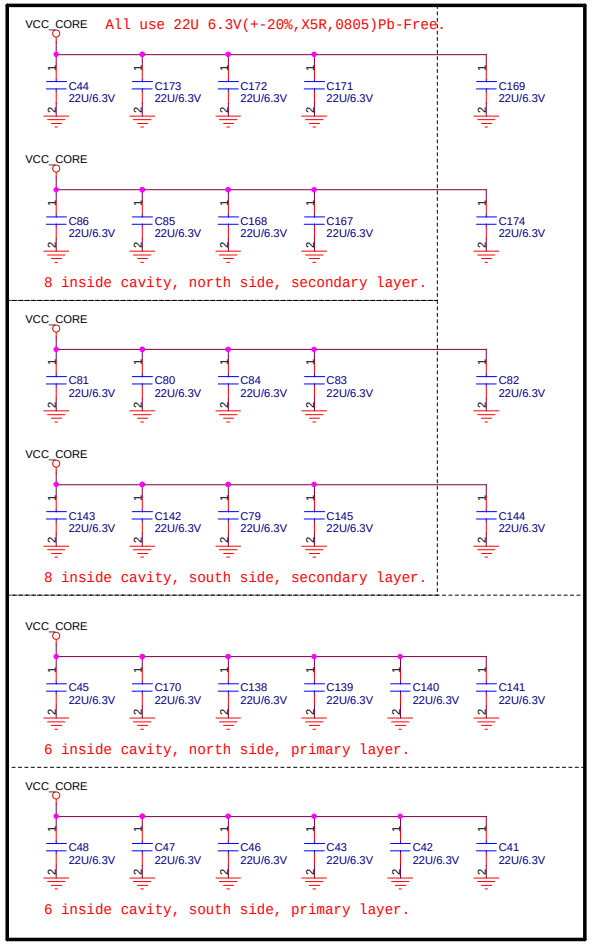

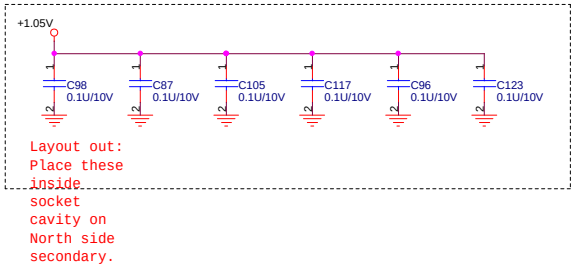

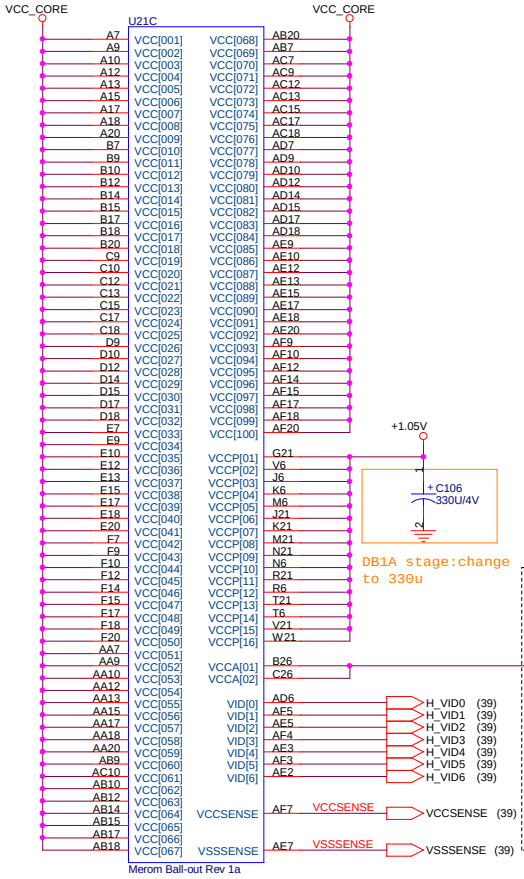

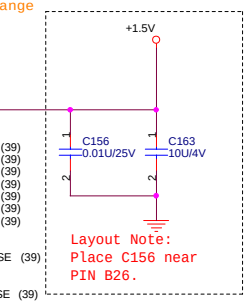

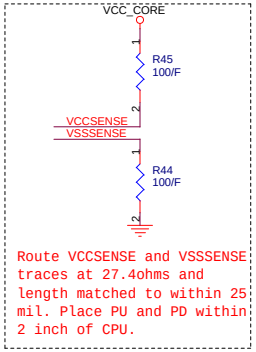

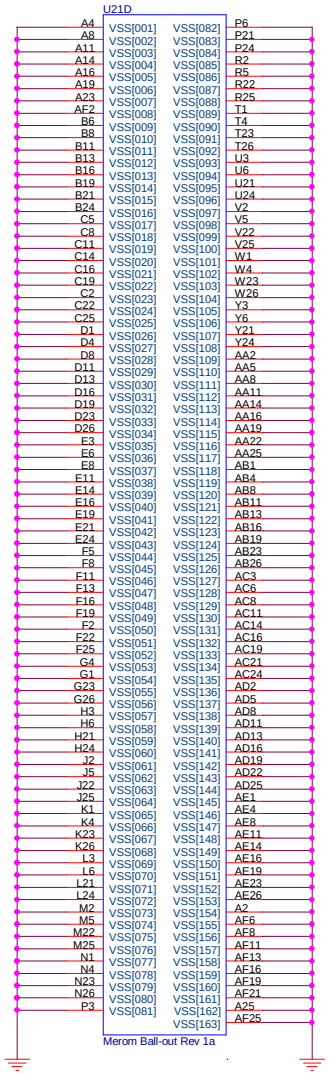

PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
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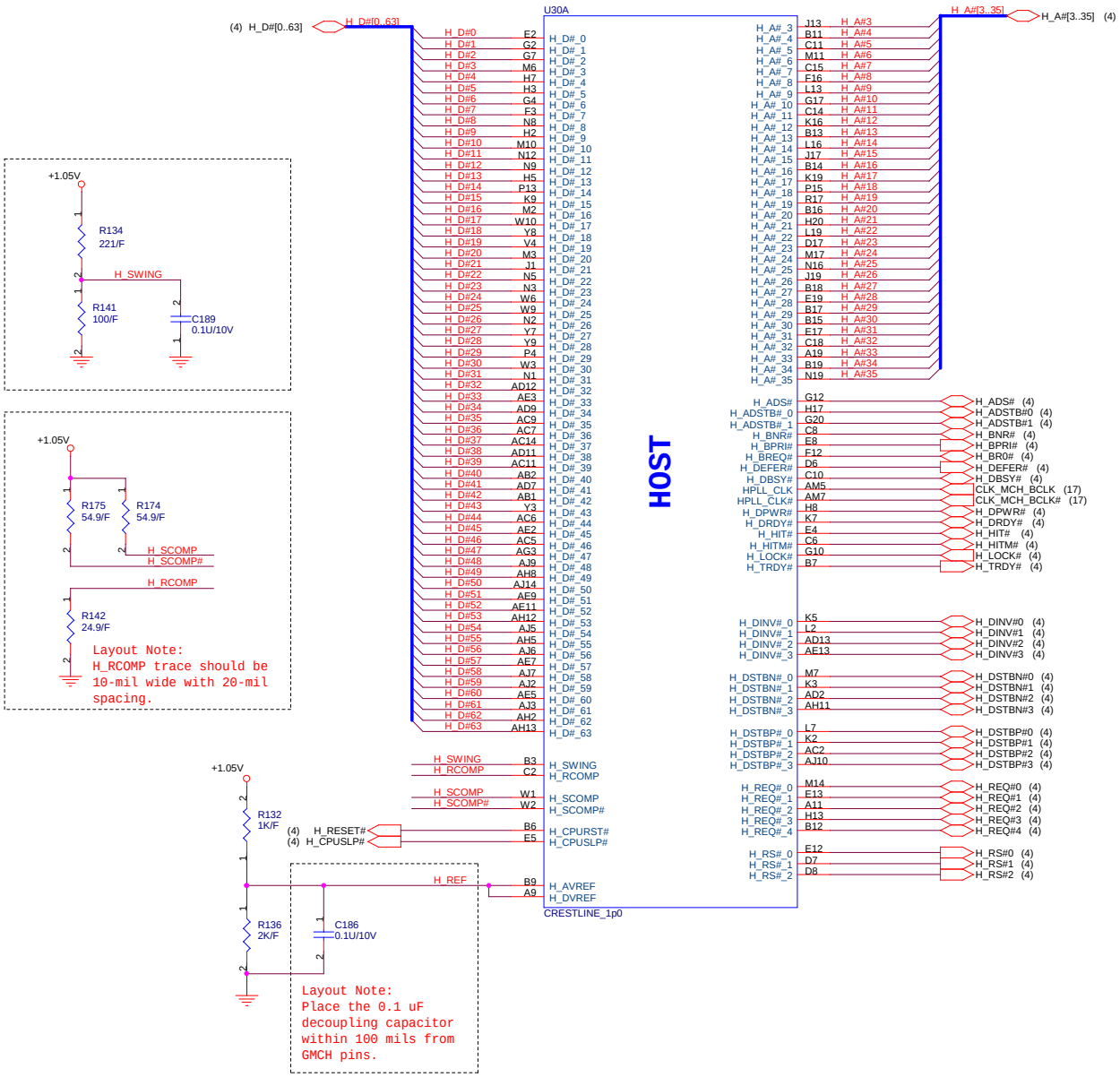

PROJECT : 0T2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline_1(HOST)	1A

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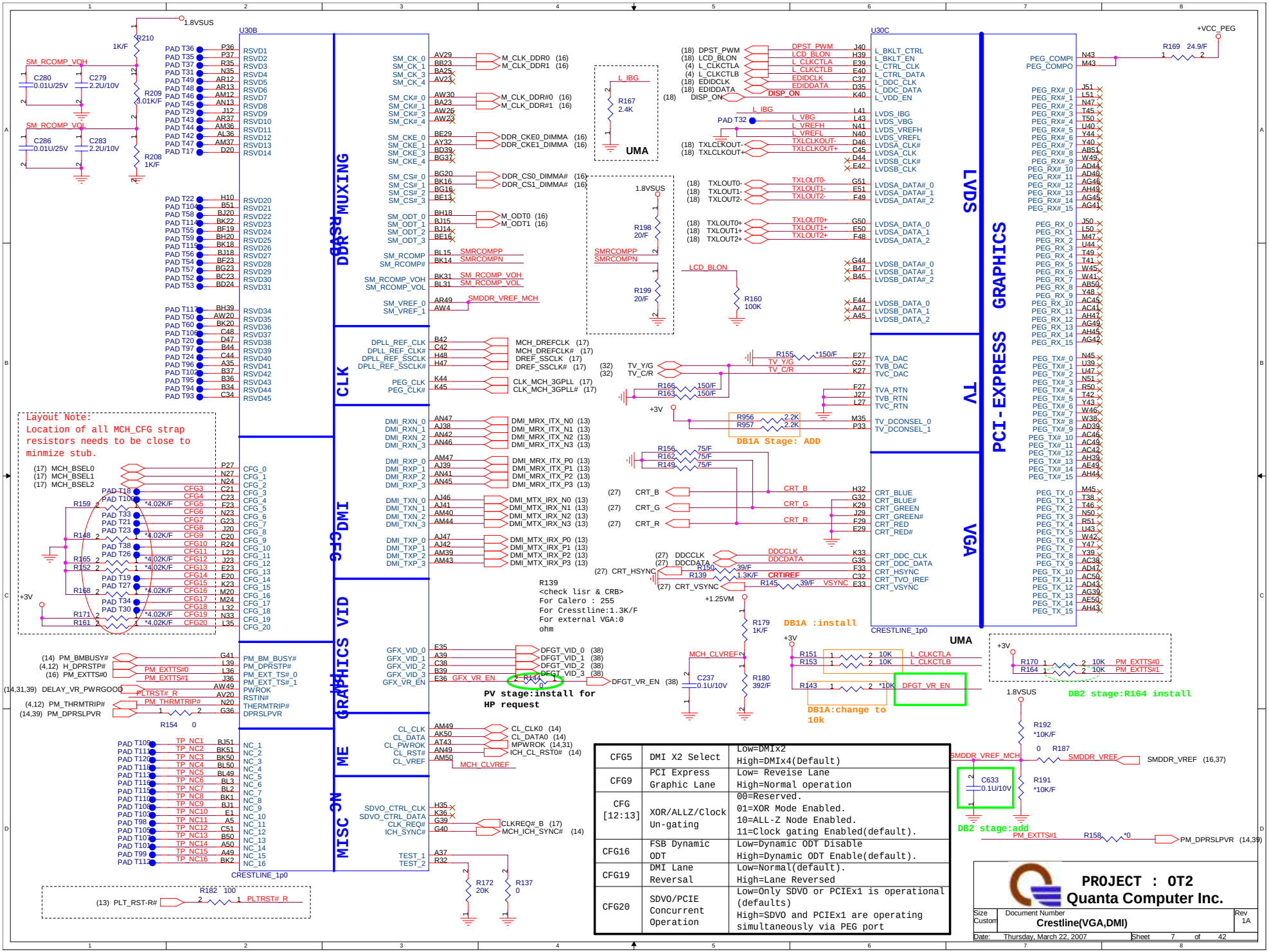

CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG [12:13]	XOR/ALLZ/Clock Un-gating	00=Reserved. 01=XOR Mode Enabled. 10=ALL-Z Node Enabled. 11=Clock gating Enabled(default).
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port

PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline(VGA,DMI)	1A

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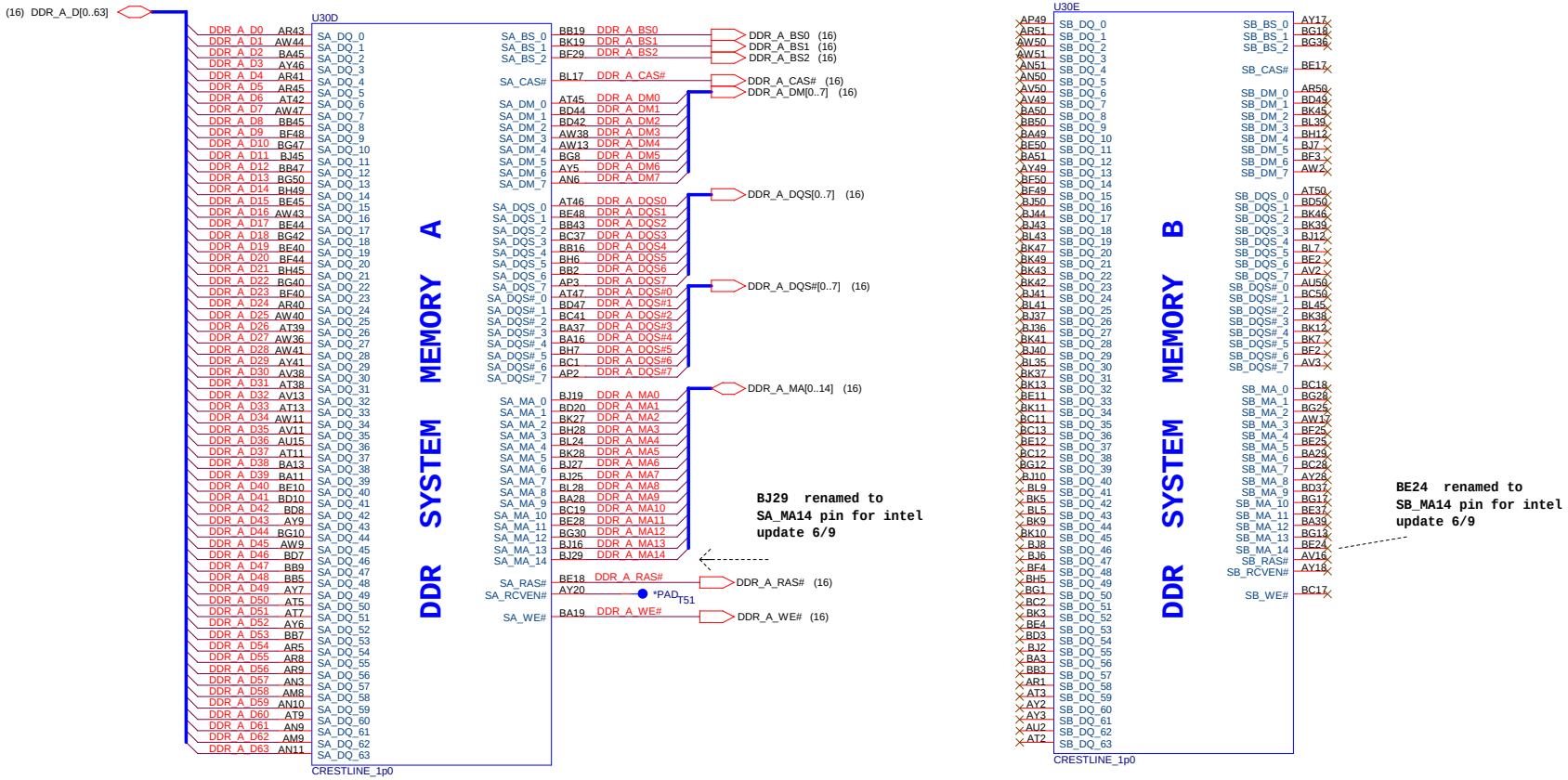

PROJECT : OT2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline(DDR2)	1A

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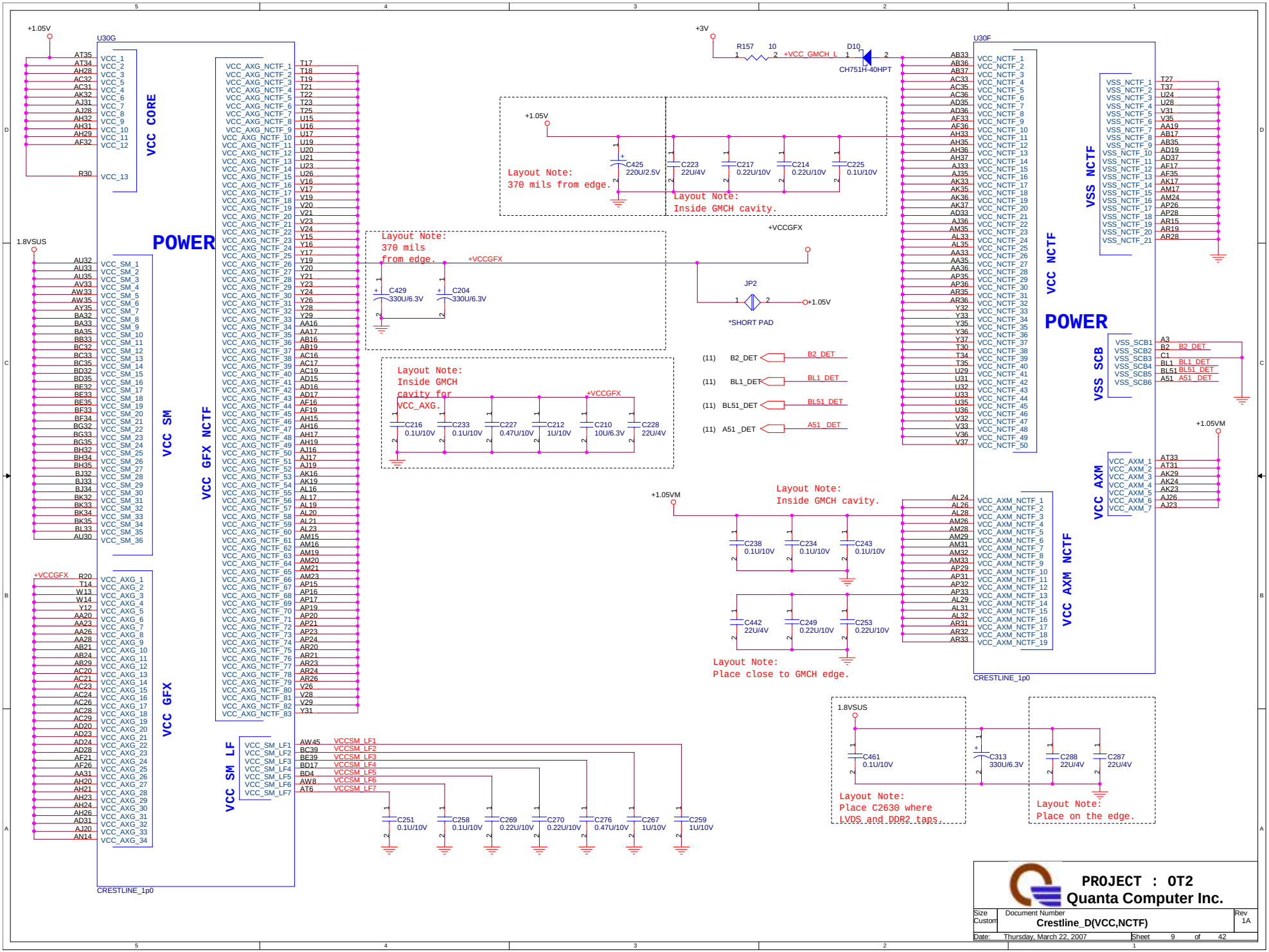
U30G
POWER
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
CRESTLINE_1p0
U30F
VCC NCTF
VSS NCTF
VSS SCB
VCC AXM
VCC AXM NCTF
+1.05V
1.8VSUS
+VCCGFX
+3V
R157 10
+VCC_GMCH_L
D10
CH751H-40HPT
Layout Note:
370 mils from edge.
Layout Note:
Inside GMCH cavity.
C425 220U/2.5V
C223 22U/4V
C217 0.22U/10V
C214 0.22U/10V
C225 0.1U/10V
C429 330U/6.3V
C204 330U/6.3V
JP2
*SHORT PAD
Layout Note:
Inside GMCH cavity for VCC_AXG.
C216 0.1U/10V
C233 0.1U/10V
C227 0.47U/10V
C212 1U/10V
C210 10U/6.3V
C228 22U/4V
(11) B2_DET
(11) BL1_DET
(11) BL51_DET
(11) A51 _DET
+1.05VM
C238 0.1U/10V
C234 0.1U/10V
C243 0.1U/10V
C442 22U/4V
C249 0.22U/10V
C253 0.22U/10V
Layout Note:
Place close to GMCH edge.
VCCSM_LF1
VCCSM_LF2
VCCSM_LF3
VCCSM_LF4
VCCSM_LF5
VCCSM_LF6
VCCSM_LF7
C251 0.1U/10V
C258 0.1U/10V
C269 0.22U/10V
C270 0.22U/10V
C276 0.47U/10V
C267 1U/10V
C259 1U/10V
C461 0.1U/10V
C313 330U/6.3V
C288 22U/4V
C287 22U/4V
Layout Note:
Place C2630 where LVDS and DDR2 taps.
Layout Note:
Place on the edge.
PROJECT : 0T2
Quanta Computer Inc.
Size Custom
Document Number
Crestline_D(VCC,NCTF)
Rev 1A
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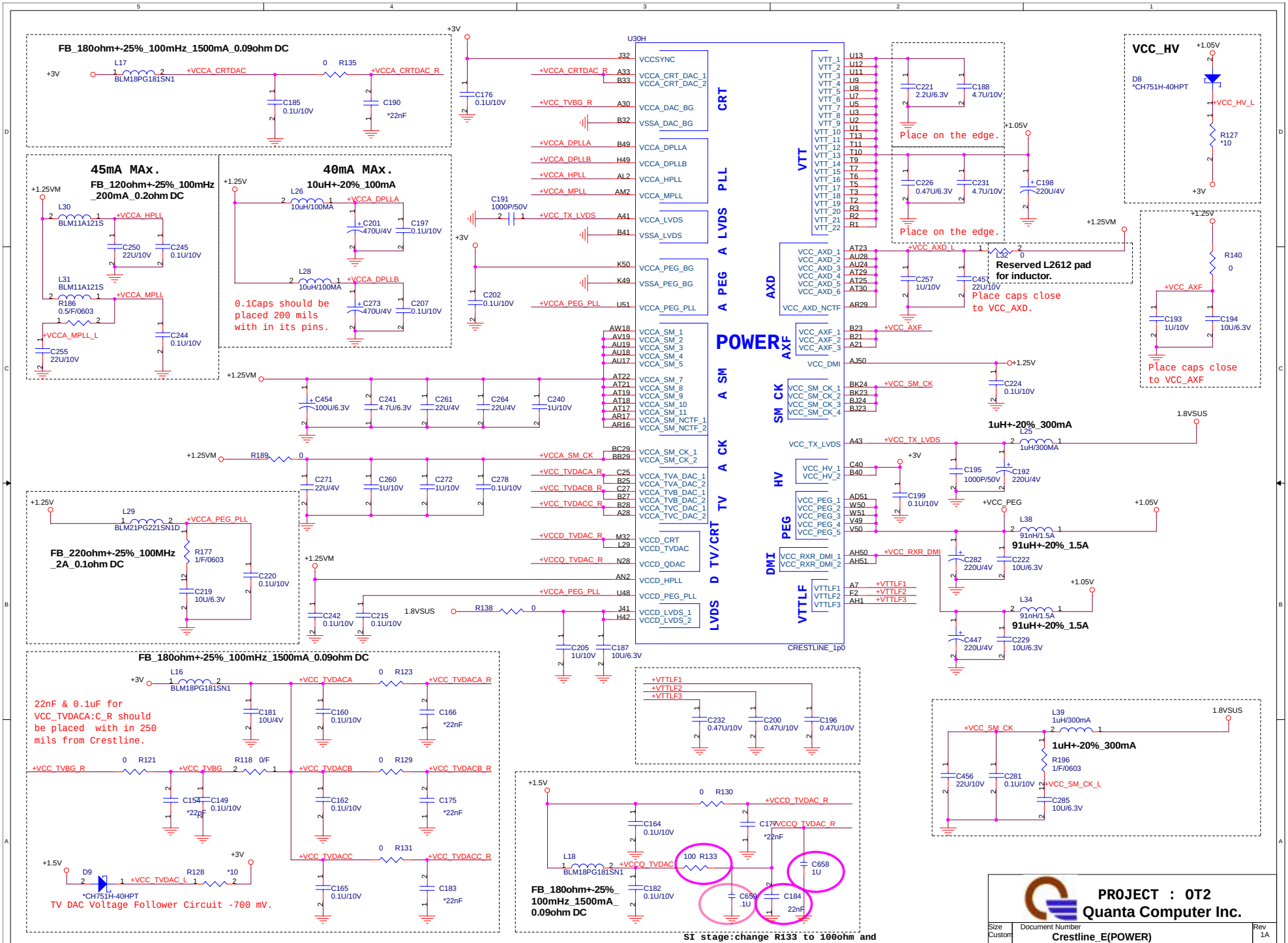
FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
45mA MAx.
FB_120ohm+-25%_100mHz_200mA_0.2ohm DC
40mA MAx.
10uH+-20%_100mA
0.1Caps should be placed 200 mils with in its pins.
FB_220ohm+-25%_100MHz_2A_0.1ohm DC
POWER
CRESTLINE_1p0
VCC_HV
Place on the edge.
Reserved L2612 pad for inductor.
Place caps close to VCC_AXD.
Place caps close to VCC_AXF
1uH+-20%_300mA
91uH+-20%_1.5A
22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.
TV DAC Voltage Follower Circuit -700 mV.
FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
SI stage:change R133 to 100ohm and C658,C659,C184 install
PROJECT : 0T2
Quanta Computer Inc.
Size Custom
Document Number
Crestline_E(POWER)
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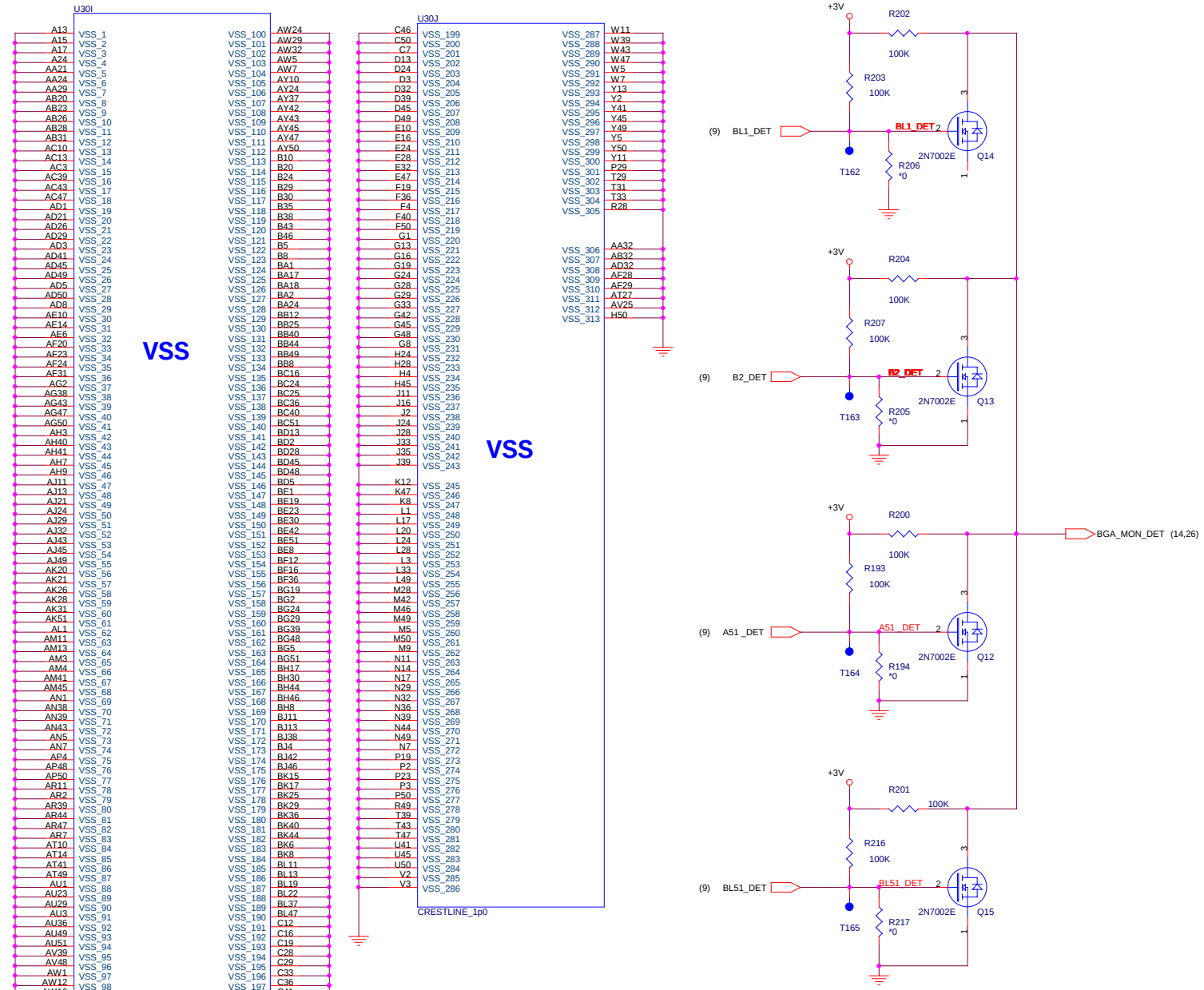
SI stage: add test pin



PROJECT : 0T2

Quanta Computer Inc.

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Custom	Crestline(VSS)	1A

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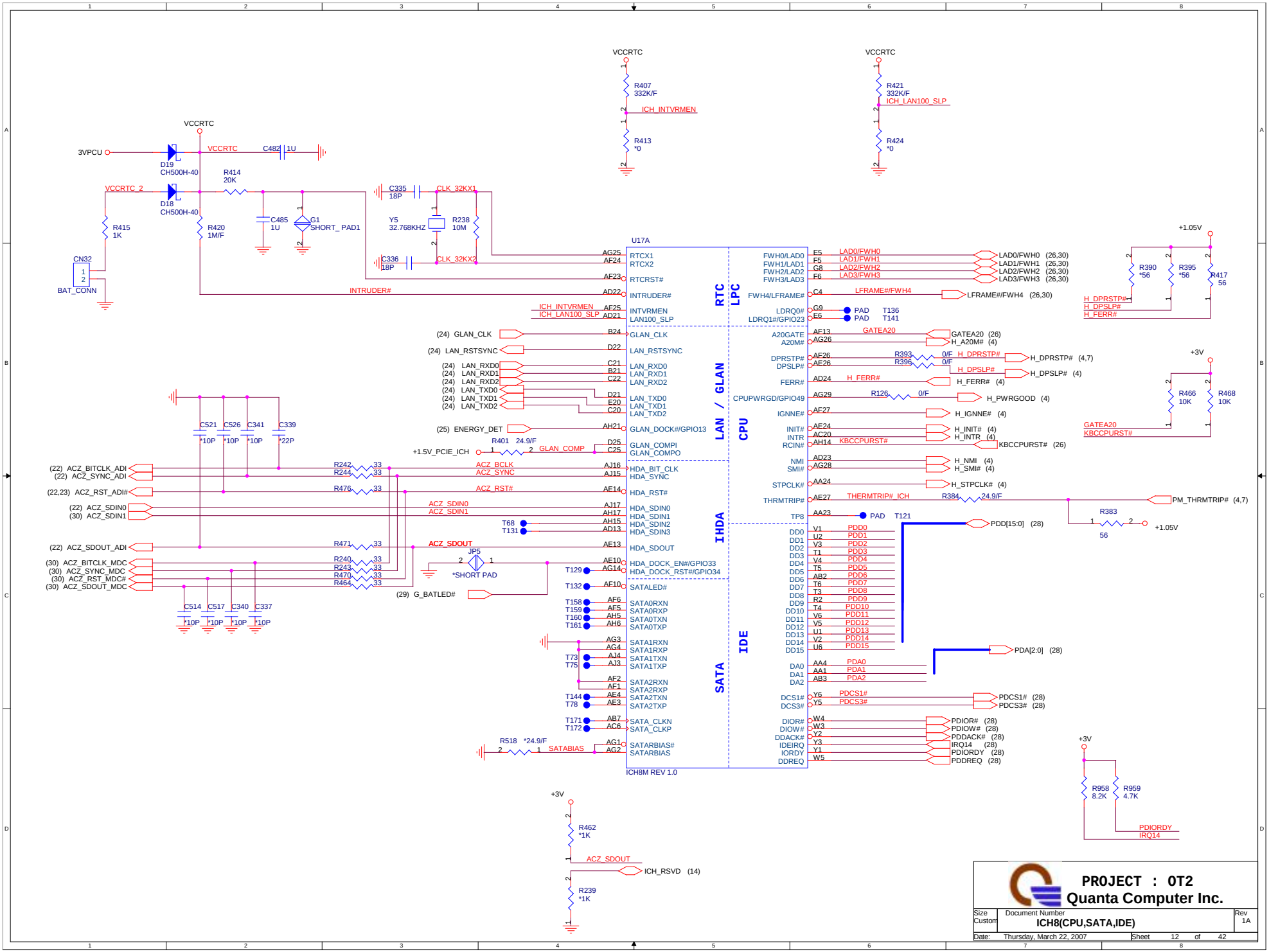
U17A
ICH8M REV 1.0
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
IDE
VCCRTC
3VPCU
D19 CH500H-40
D18 CH500H-40
VCCRTC_2
C482 1U
R414 20K
R415 1K
R420 1M/F
C485 1U
G1 SHORT_PAD1
CN32
BAT_CONN
C335 18P
C336 18P
Y5 32.768KHZ
R238 10M
CLK_32KX1
CLK_32KX2
INTRUDER#
ICH_INTVRMEN
ICH_LAN100_SLP
R407 332K/F
R413 *0
R421 332K/F
R424 *0
+1.05V
R390 *56
R395 *56
R417 56
H_DPRSTP#
H_DPSLP#
H_FERR#
+3V
R466 10K
R468 10K
GATEA20
KBCCPURST#
R383 56
PM_THRMTRIP# (4,7)
PDD[15:0] (28)
PDA[2:0] (28)
R958 8.2K
R959 4.7K
PDIORDY
IRQ14
R462 *1K
R239 *1K
ICH_RSVD (14)
ACZ_SDOUT
JP5
*SHORT PAD
(29) G_BATLED#
R518 *24.9/F
SATABIAS
R401 24.9/F
+1.5V_PCIE_ICH
GLAN_COMP
(24) GLAN_CLK
(24) LAN_RSTSYNC
(25) ENERGY_DET
(22) ACZ_BITCLK_ADI
(22) ACZ_SYNC_ADI
(22,23) ACZ_RST_ADI#
(22) ACZ_SDIN0
(30) ACZ_SDIN1
(22) ACZ_SDOUT_ADI
(30) ACZ_BITCLK_MDC
(30) ACZ_SYNC_MDC
(30) ACZ_RST_MDC#
(30) ACZ_SDOUT_MDC
C521 *10P
C526 *10P
C341 *10P
C339 *22P
C514 *10P
C517 *10P
C340 *10P
C337 *10P
R242 33
R244 33
R476 33
R471 33
R240 33
R243 33
R470 33
R464 33
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDOUT
LAD0/FWH0 (26,30)
LAD1/FWH1 (26,30)
LAD2/FWH2 (26,30)
LAD3/FWH3 (26,30)
LFRAME#/FWH4 (26,30)
PAD T136
PAD T141
GATEA20 (26)
H_A20M# (4)
H_DPRSTP# (4,7)
H_DPSLP# (4)
H_FERR# (4)
H_PWRGOOD (4)
H_IGNNE# (4)
H_INIT# (4)
H_INTR (4)
KBCCPURST# (26)
H_NMI (4)
H_SMI# (4)
H_STPCLK# (4)
PAD T121
PDCS1# (28)
PDCS3# (28)
PDIOR# (28)
PDIOW# (28)
PDDACK# (28)
IRQ14 (28)
PDIORDY (28)
PDDREQ (28)
PROJECT : 0T2
Quanta Computer Inc.
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Document Number
ICH8(CPU,SATA,IDE)
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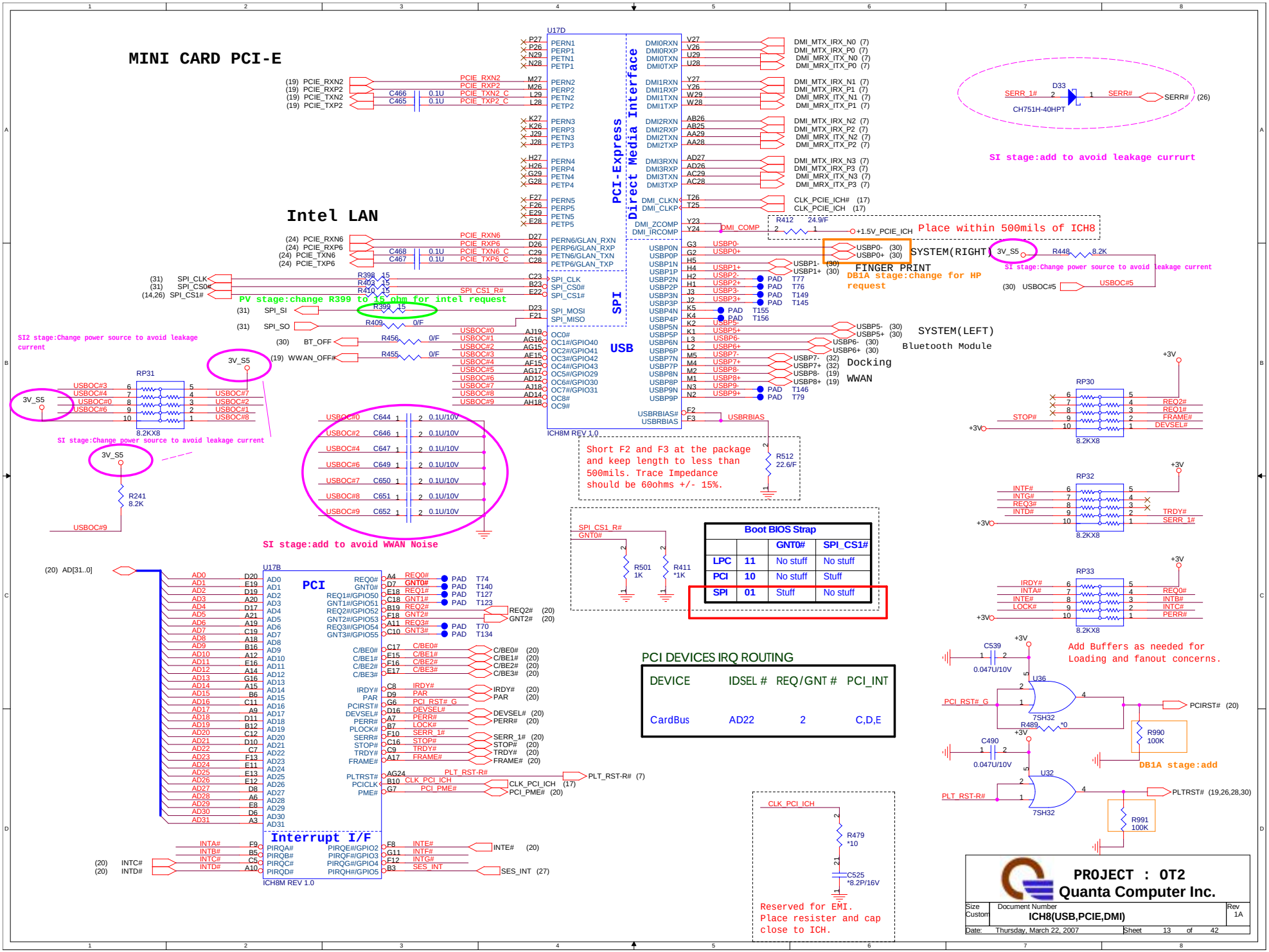
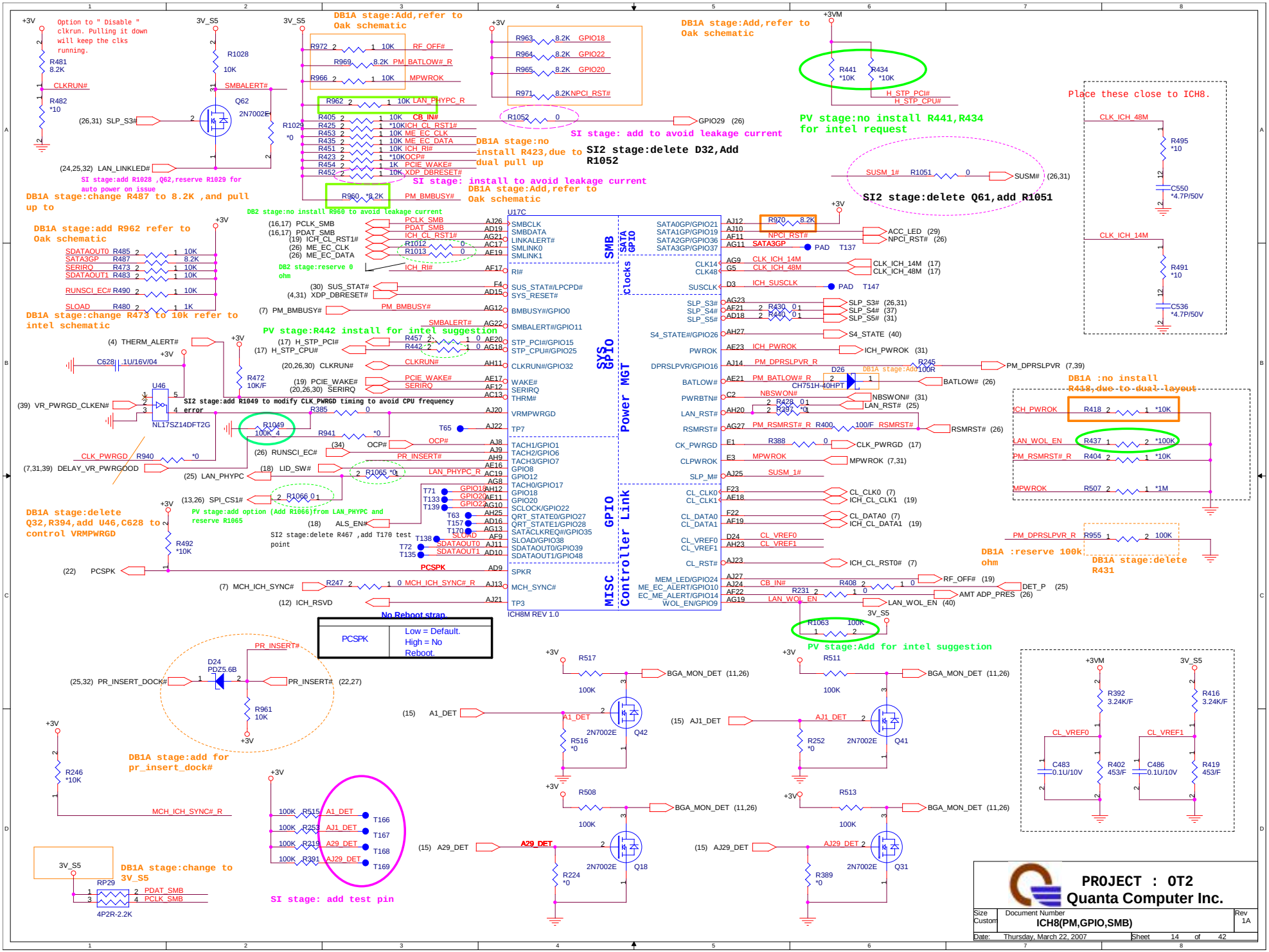


Boot BIOS Strap

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
CardBus	AD22	2	C,D,E


Option to " Disable " clkrun. Pulling it down will keep the clks running.
DB1A stage:Add,refer to Oak schematic
DB1A stage:Add,refer to Oak schematic
PV stage:no install R441,R434 for intel request
Place these close to ICH8.
SI stage: add to avoid leakage current
DB1A stage:no install R423,due to dual pull up
SI2 stage:delete D32,Add R1052
SI2 stage:delete Q61,add R1051
SI stage:add R1028 ,Q62,reserve R1029 for auto power on issue
DB1A stage:change R487 to 8.2K ,and pull up to
SI stage: install to avoid leakage current
DB1A stage:Add,refer to Oak schematic
DB2 stage:no install R960 to avoid leakage current
DB1A stage:add R962 refer to Oak schematic
DB2 stage:reserve 0 ohm
DB1A stage:change R473 to 10k refer to intel schematic
PV stage:R442 install for intel suggestion
SI2 stage:add R1049 to modify CLK_PWRGD timing to avoid CPU frequency error
DB1A :no install R418,due to dual layout
DB1A stage:delete Q32,R394,add U46,C628 to control VRMPWRGD
PV stage:add option (Add R1066)from LAN_PHYPC and reserve R1065
SI2 stage:delete R467 ,add T170 test point
DB1A :reserve 100k ohm
DB1A stage:delete R431
No Reboot strap.
PCSPK
Low = Default.
High = No Reboot.
PV stage:Add for intel suggestion
DB1A stage:add for pr_insert_dock#
DB1A stage:change to 3V_S5
SI stage: add test pin
U17C
ICH8M REV 1.0
SMB
SATA GPIO
clocks
Power MGT
GPIO
Controller Link
MISC
PROJECT : 0T2
Quanta Computer Inc.
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ICH8(PM,GPIO,SMB)
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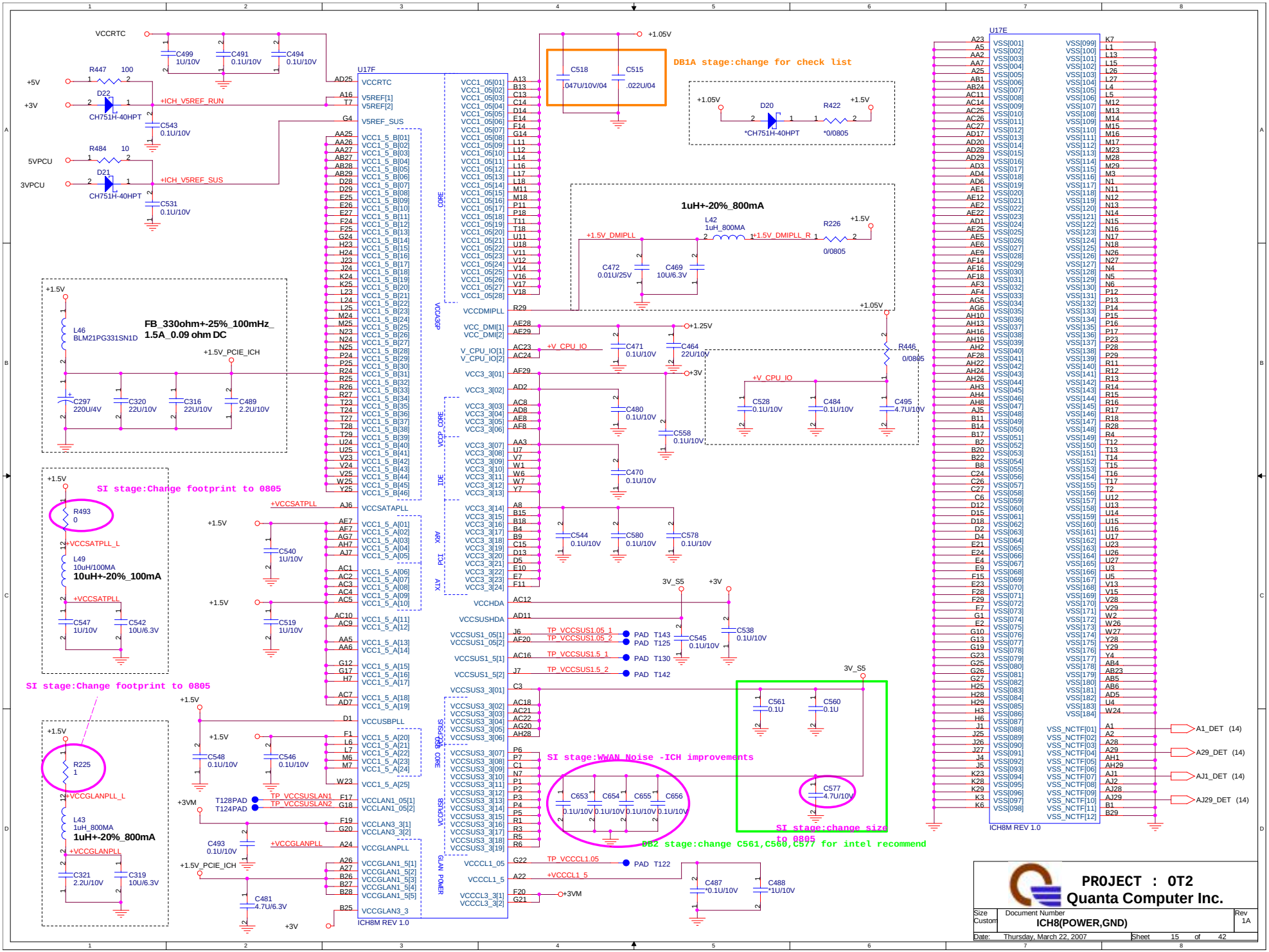
U17F
ICH8M REV 1.0
U17E
ICH8M REV 1.0
DB1A stage:change for check list
1uH+-20%_800mA
FB_330ohm+-25%_100mHz_
1.5A_0.09 ohm DC
SI stage:Change footprint to 0805
10uH+-20%_100mA
SI stage:Change footprint to 0805
1uH+-20%_800mA
SI stage:WWAN Noise -ICH improvements
SI stage:change size to 0805
DB2 stage:change C561,C560,C577 for intel recommend
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Document Number
ICH8(POWER,GND)
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A is required to route to Top SoDIMM for AMT to function.This will need to change for M08

BOT

JDIM1

PC4800 DDR2 SDRAM SO-DIMM (200P)

FOX_AS0A426-M2SN-7F

Add for intel update

SMbus address A0

CLOCK 0,1
CKE 0,1

DB2 stage:reaerve

Place these Caps near So-Dimm1.

Place these Caps near So-Dimm1.

Add for intel update

Please these resistor closely DIMMA,all trace length<750 mil.

TOP

Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

BOT

DB2 stage:on install for C327,C219---C331 for only one channel DIMM

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 SO-DIMM(200P)	1A

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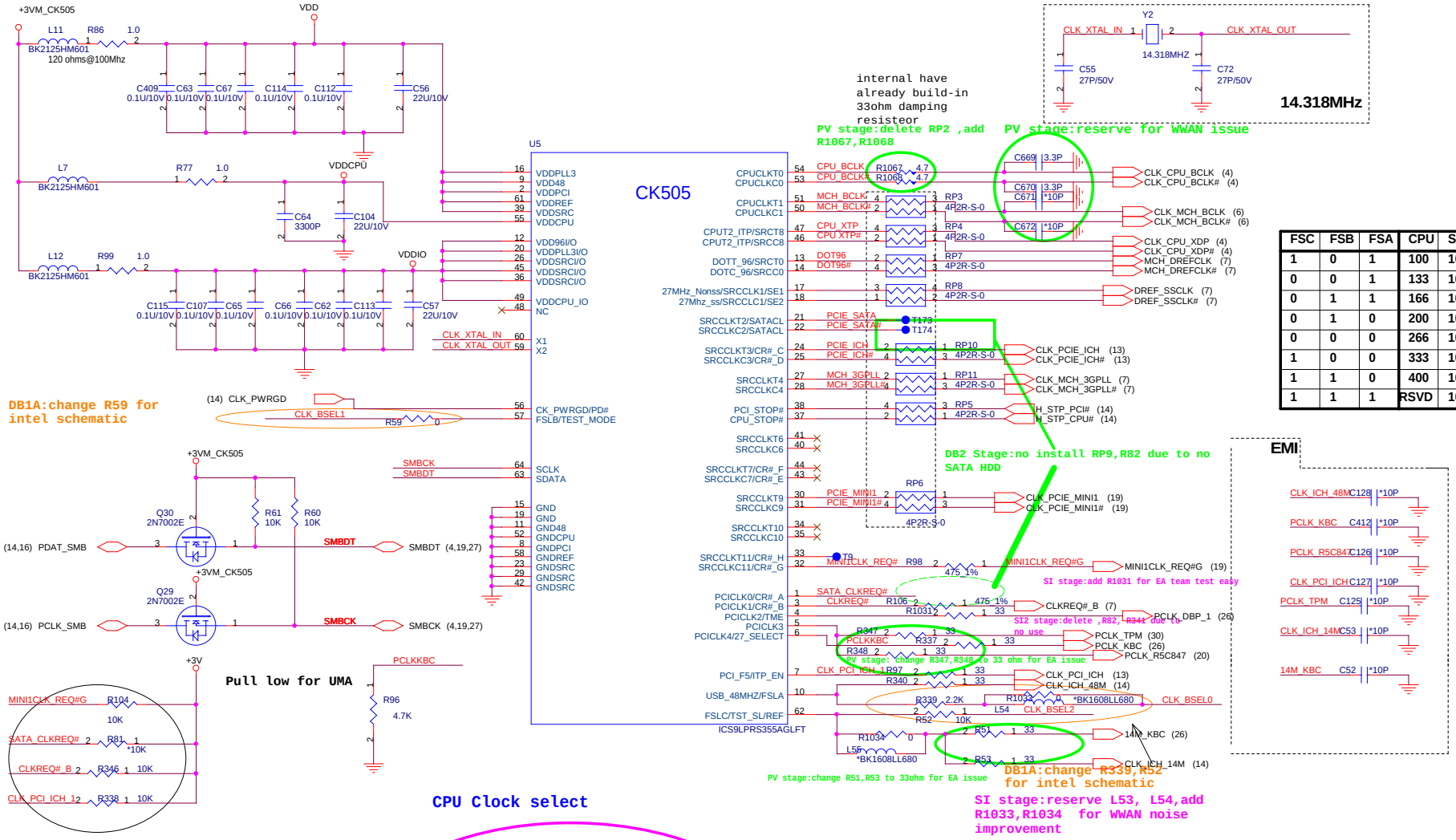


internal have already build-in 33ohm damping resisteor

PV stage:delete RP2 ,add R1067,R1068

PV stage:reserve for WWAN issue

DB2 Stage:no install RP9,R82 due to no SATA HDD

SI stage:add R1031 for EA team test easy

SI2 stage:delete ,R82, R341 due to no use

PV stage: change R347,R348 to 33 ohm for EA issue

PV stage:change R51,R53 to 33ohm for EA issue

DB1A:change R339,R52 for intel schematic

SI stage:reserve L53, L54,add R1033,R1034 for WWAN noise improvement

DB1A:change R59 for intel schematic

Pull low for UMA

SI stage: strapping options for CPU_BSEL{0:2}

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

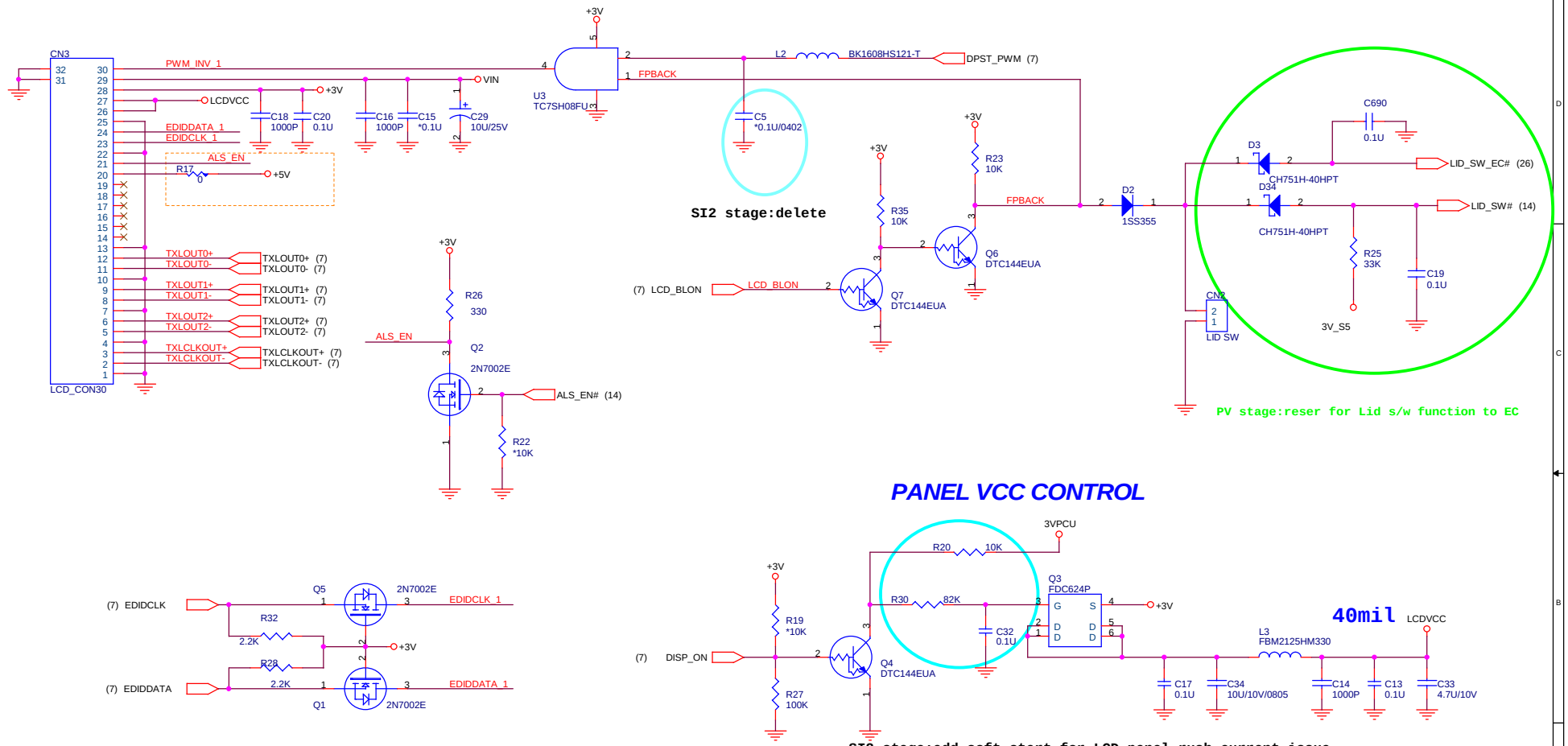
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

PROJECT : 0T2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK(CK505)	1A

Date: Thursday, March 22, 2007 Sheet 17 of 42



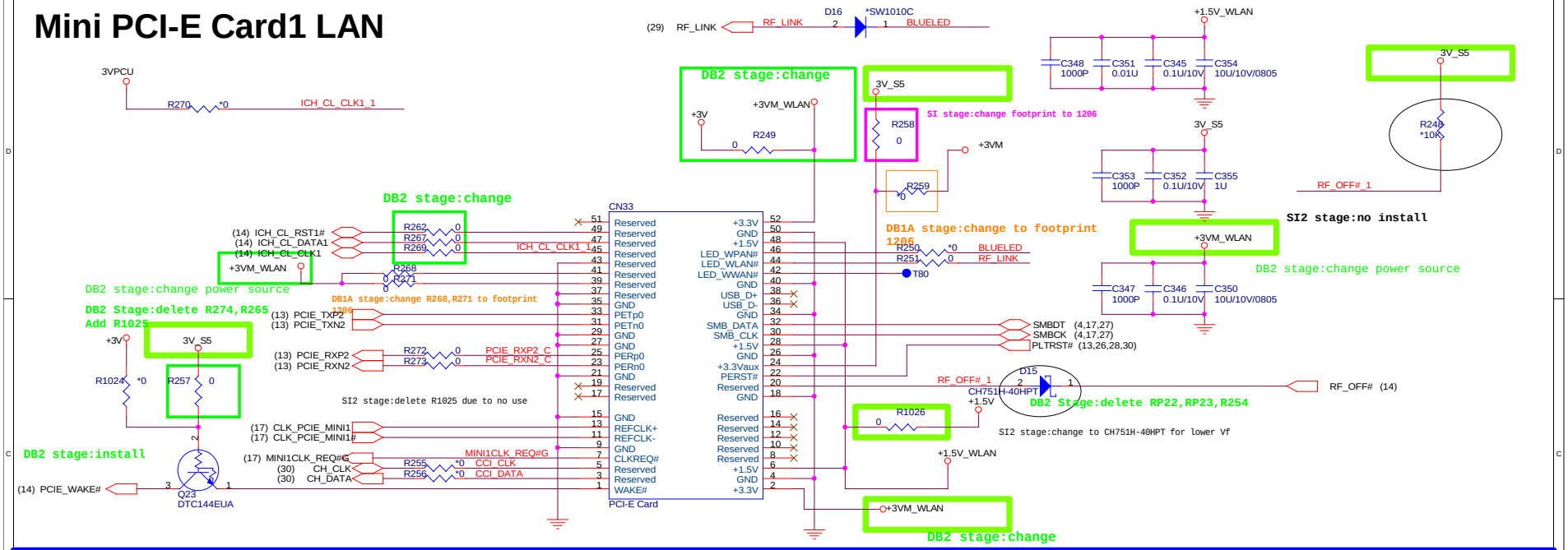
PROJECT : OT2

Quanta Computer Inc.

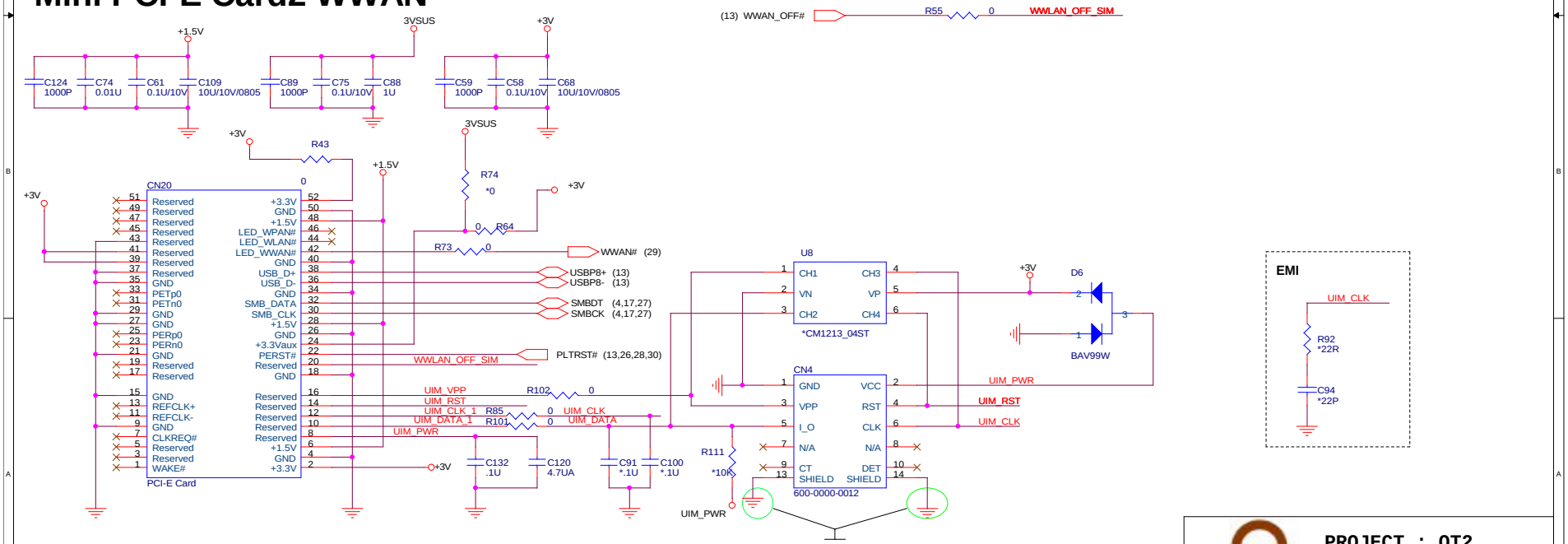
Size	Document Number	Rev
B	LCD CON	1A

Date: Thursday, March 22, 2007 Sheet 18 of 42

Mini PCI-E Card1 LAN



Mini PCI-E Card2 WWAN

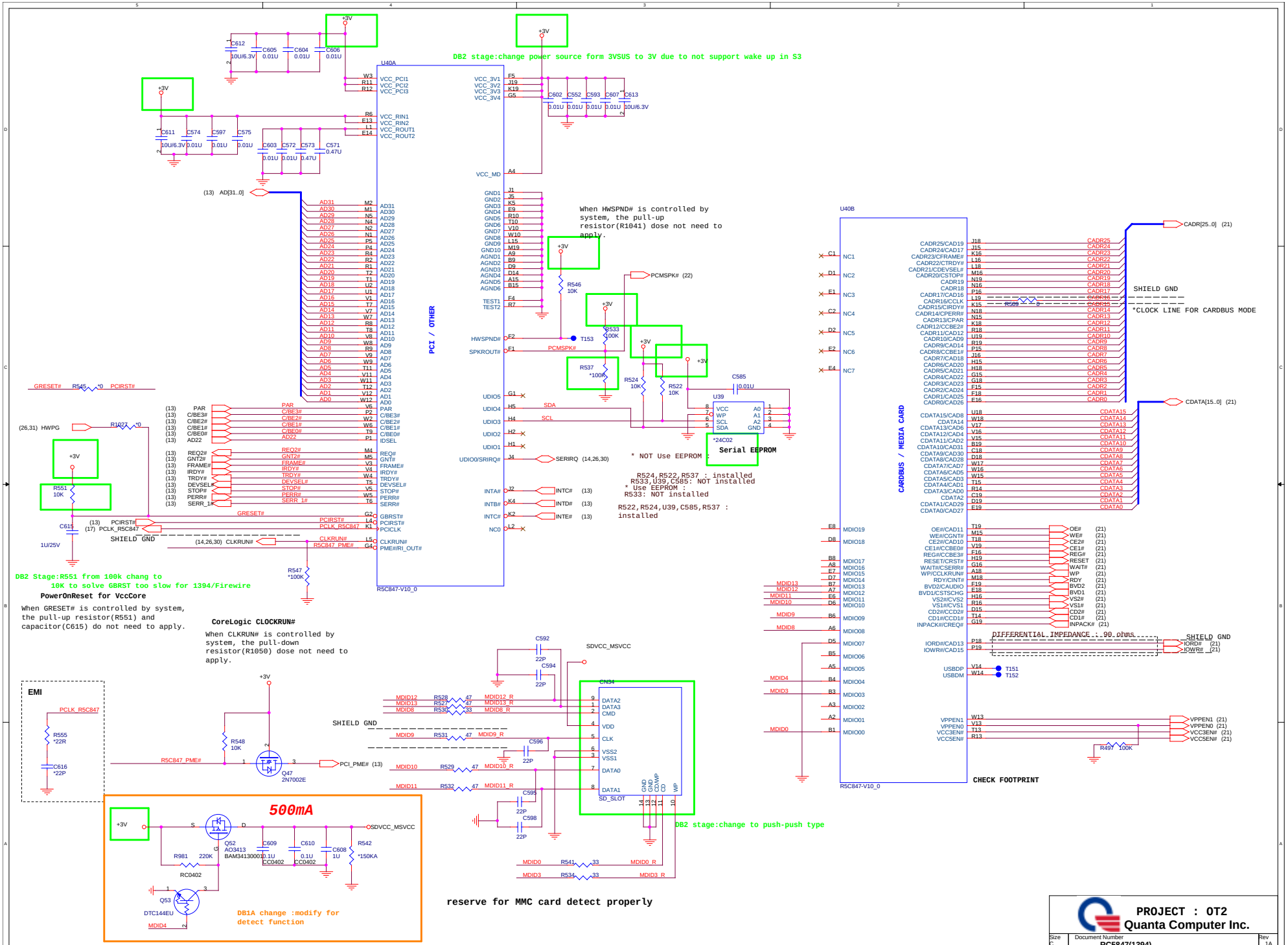


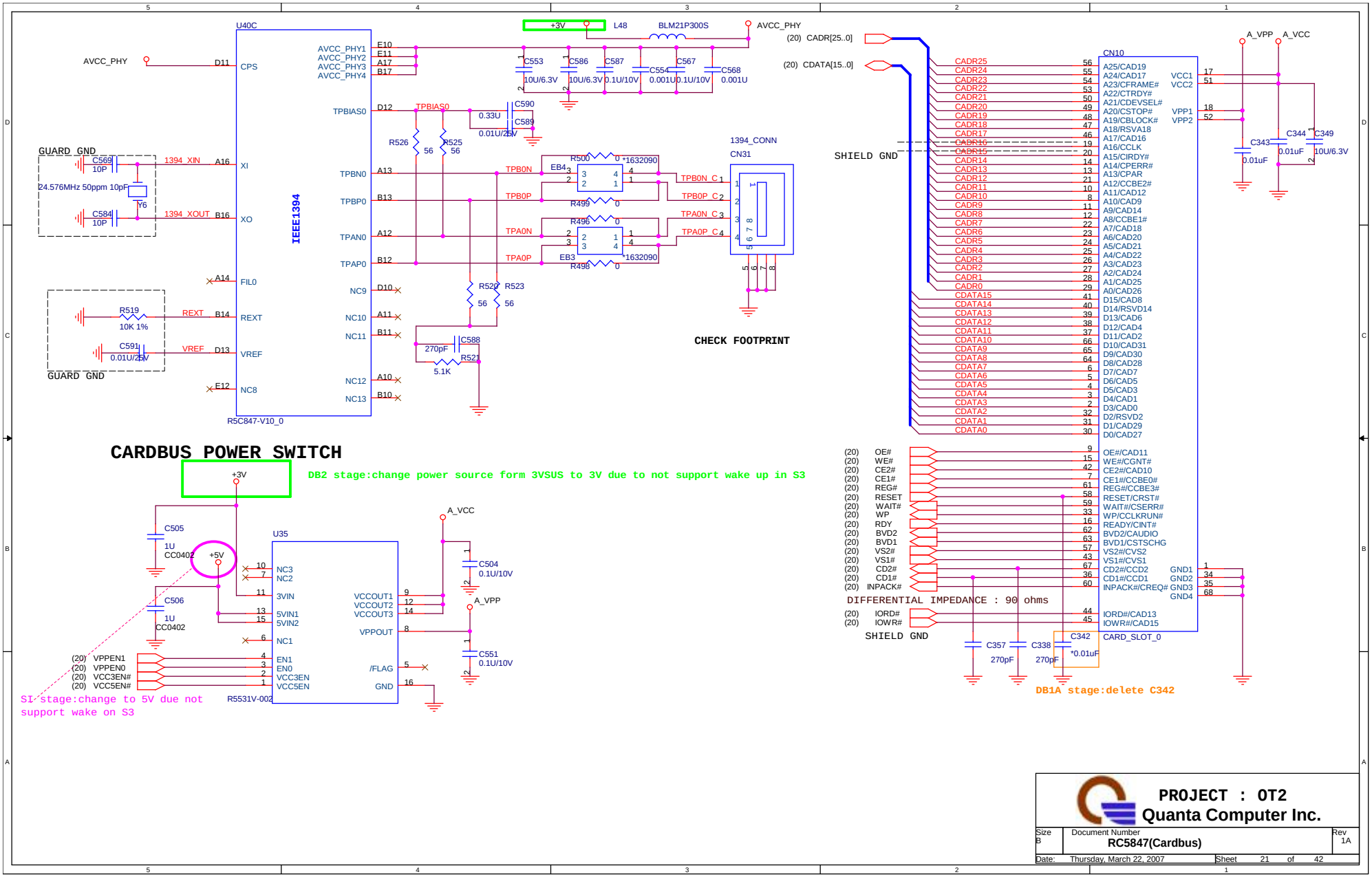
PROJECT : 0T2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	WAN/WWAN CARD	1A

Date: Thursday, March 22, 2007 Sheet 19 of 42


DB2 stage:change power source form 3VSUS to 3V due to not support wake up in S3
When HWSPND# is controlled by system, the pull-up resistor(R1041) dose not need to apply.
PCI / OTHER
U40A
R5C847-V10_0
CARDBUS / MEDIA CARD
U40B
SHIELD GND
*CLOCK LINE FOR CARDBUS MODE
Serial EEPROM
*24C02
* NOT Use EEPROM :
R524,R522,R537 : installed
R533,U39,C585: NOT installed
* Use EEPROM :
R533: NOT installed
R522,R524,U39,C585,R537 : installed
DIFFERENTIAL IMPEDANCE : 90 ohms
CHECK FOOTPRINT
PowerOnReset for VccCore
When GRESET# is controlled by system, the pull-up resistor(R551) and capacitor(C615) do not need to apply.
DB2 Stage:R551 from 100k chang to 10K to solve GBRST too slow for 1394/Firewire
CoreLogic CLOCKRUN#
When CLKRUN# is controlled by system, the pull-down resistor(R1050) dose not need to apply.
EMI
500mA
DB1A change :modify for detect function
DB2 stage:change to push-push type
reserve for MMC card detect properly
PROJECT : OT2
Quanta Computer Inc.
Size C
Document Number RC5847(1394)
Rev 1A
Date: Thursday, March 22, 2007
Sheet 20 of 42

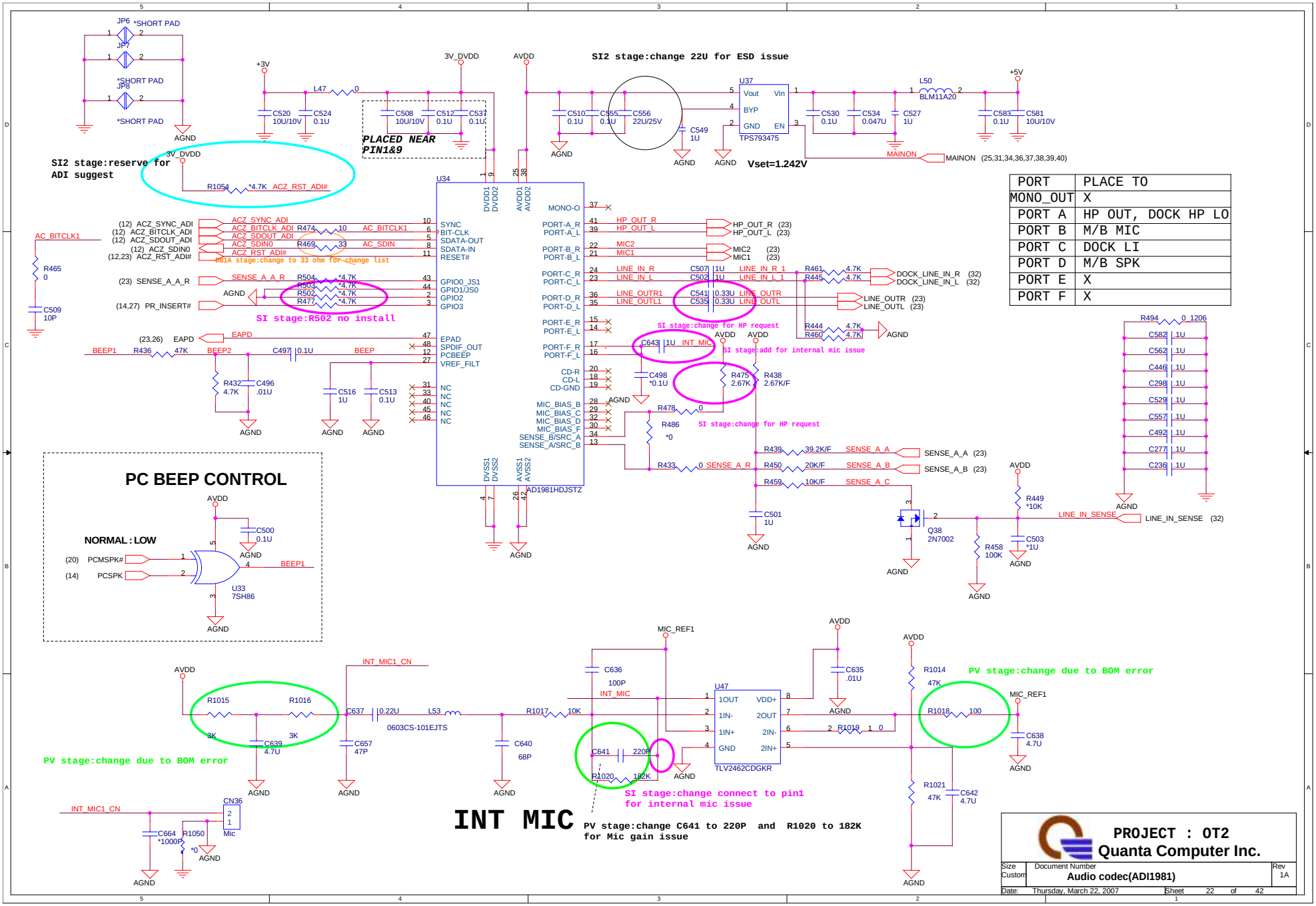


PROJECT : 0T2

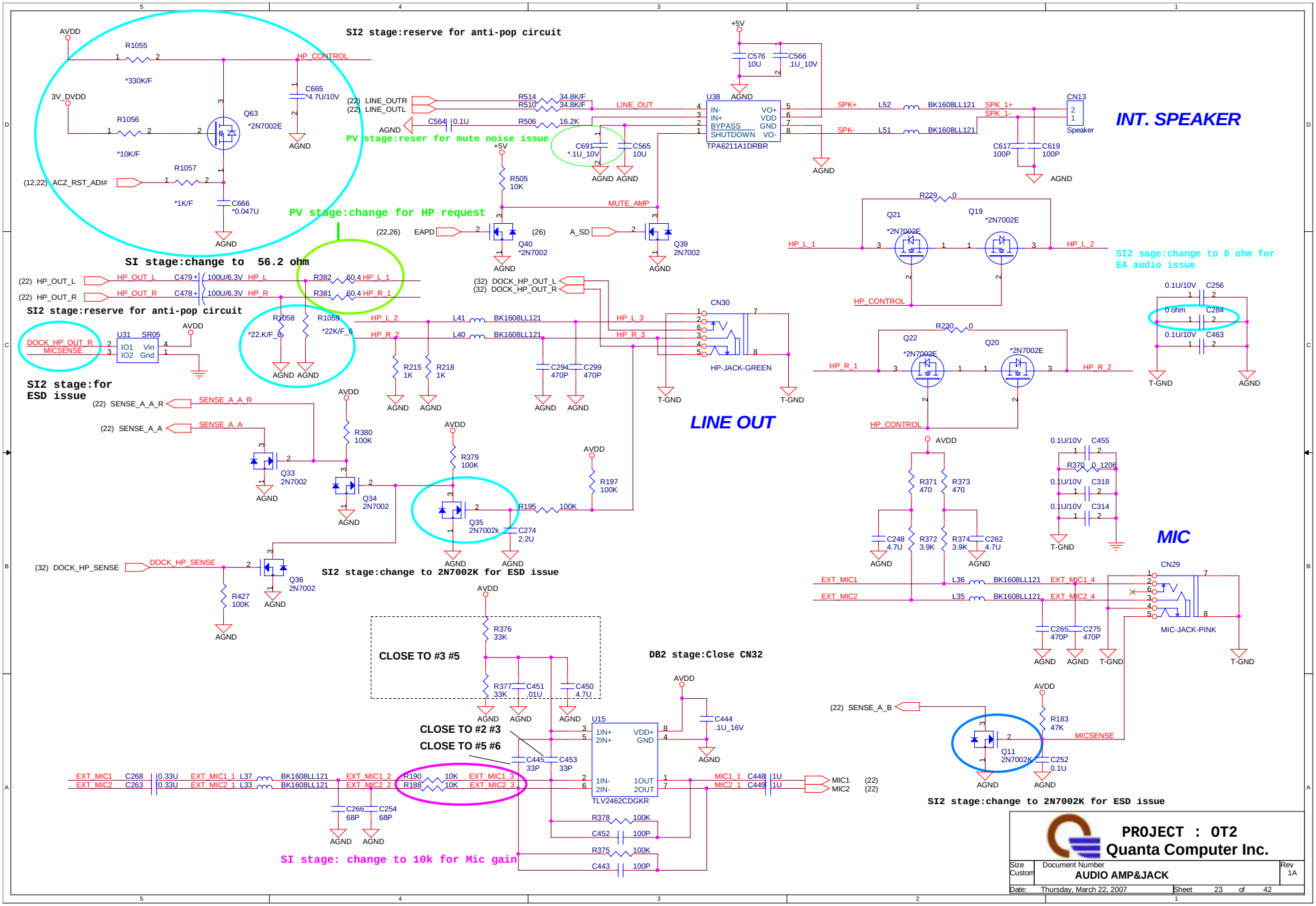
Quanta Computer Inc.

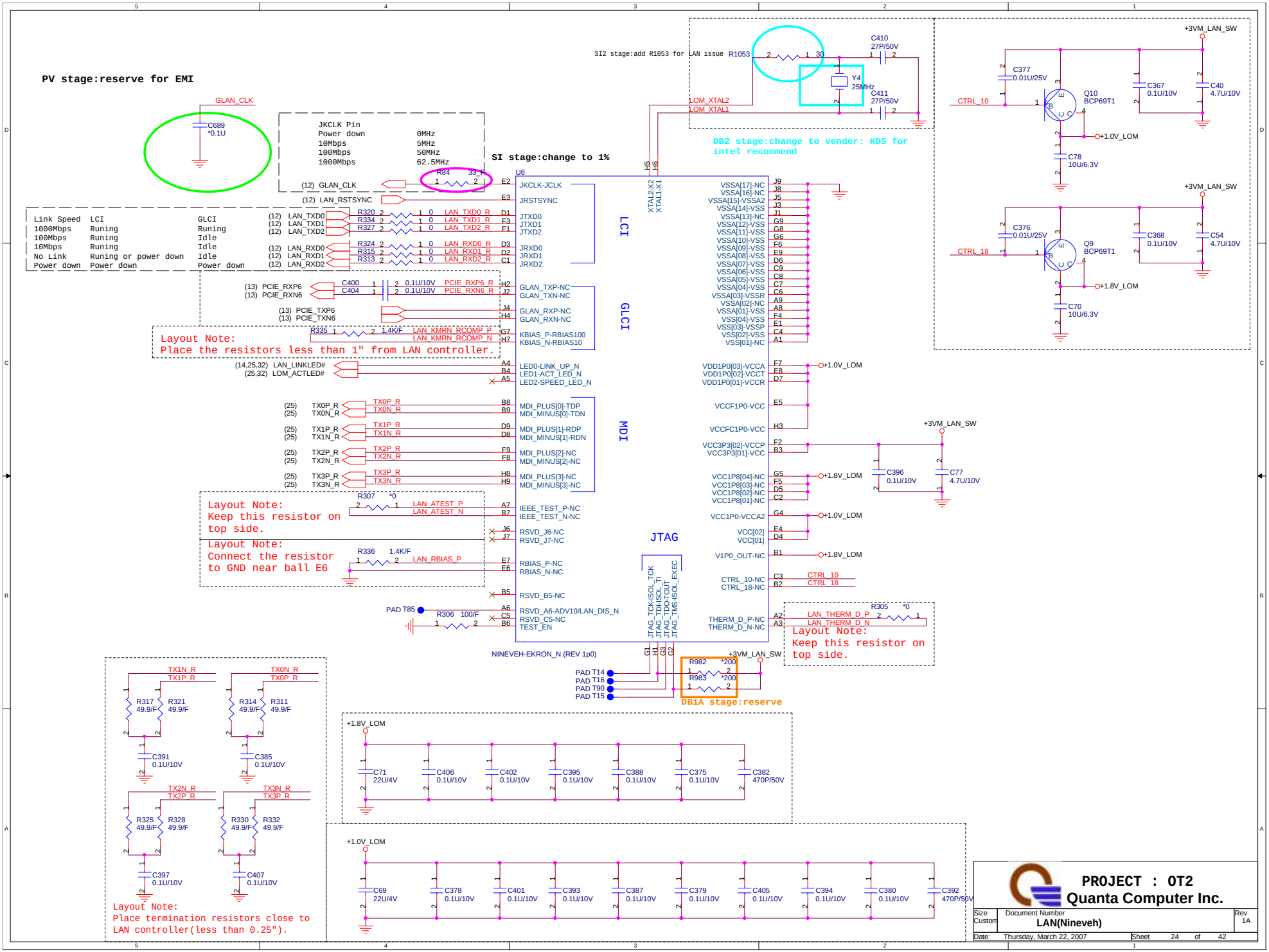
Size	Document Number	Rev
B	RC5847(Cardbus)	1A

Date: Thursday, March 22, 2007 Sheet 21 of 42



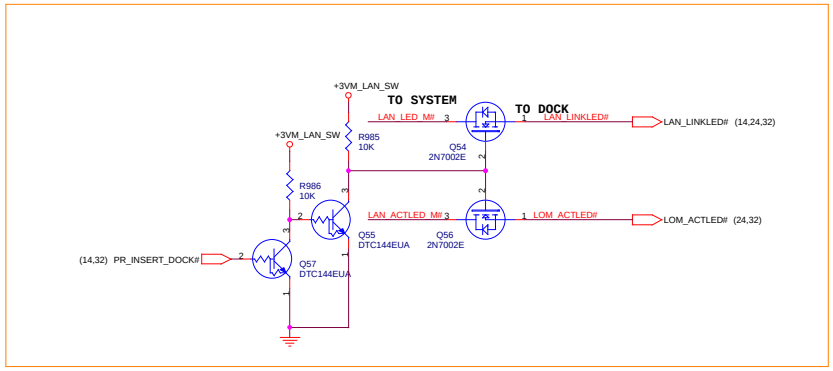
PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT, DOCK HP LO
PORT B	M/B MIC
PORT C	DOCK LI
PORT D	M/B SPK
PORT E	X
PORT F	X


SI2 stage:reserve for anti-pop circuit
AVDD
R1055
*330K/F
HP_CONTROL
3V_DVDD
R1056
*10K/F
Q63
*2N7002E
C665
*4.7U/10V
AGND
(22) LINE_OUTR
(22) LINE_OUTL
R514 34.8K/F
R510 34.8K/F
LINE_OUT
C564 0.1U
R506 16.2K
PV stage:reser for mute noise issue
C691
*.1U_10V
C565
10U
U38
IN-
IN+
BYPASS
SHUTDOWN
VO+
VDD
GND
VO-
TPA6211A1DRBR
+5V
C576
10U
C566
.1U_10V
SPK+
L52
BK1608LL121
SPK_1+
SPK_1-
SPK-
L51
BK1608LL121
CN13
Speaker
C617
100P
C619
100P
INT. SPEAKER
R1057
(12,22) ACZ_RST_ADI#
*1K/F
C666
*0.047U
R505
10K
MUTE_AMP
PV stage:change for HP request
(22,26) EAPD
Q40
*2N7002
(26) A_SD
Q39
2N7002
SI stage:change to 56.2 ohm
(22) HP_OUT_L
(22) HP_OUT_R
HP_OUT_L
HP_OUT_R
C479
C478
100U/6.3V
HP_L
HP_R
R382 60.4
R381 60.4
HP_L_1
HP_R_1
(32) DOCK_HP_OUT_L
(32) DOCK_HP_OUT_R
SI2 stage:reserve for anti-pop circuit
DOCK_HP_OUT_R
MICSENSE
U31
SR05
IO1
IO2
Vin
Gnd
R2058
*22.K/F_6
R1059
*22K/F_6
HP_L_2
HP_R_2
L41
L40
BK1608LL121
HP_L_3
HP_R_3
CN30
HP-JACK-GREEN
R215
1K
R218
1K
C294
470P
C299
470P
T-GND
LINE OUT
SI2 stage:for
ESD issue
(22) SENSE_A_A_R
SENSE_A_A_R
(22) SENSE_A_A
SENSE_A_A
R380
100K
Q33
2N7002
Q34
2N7002
R379
100K
Q35
2N7002k
R195
100K
R197
100K
C274
2.2U
(32) DOCK_HP_SENSE
DOCK_HP_SENSE
Q36
2N7002
R427
100K
SI2 stage:change to 2N7002K for ESD issue
CLOSE TO #3 #5
R376
33K
R377
33K
C451
.01U
C450
4.7U
DB2 stage:Close CN32
CLOSE TO #2 #3
CLOSE TO #5 #6
C445
33P
C453
33P
U15
1IN+
2IN+
VDD+
GND
1IN-
2IN-
1OUT
2OUT
TLV2462CDGKR
C444
.1U_16V
EXT_MIC1
EXT_MIC2
C268
C263
0.33U
EXT_MIC1_1
EXT_MIC2_1
L37
L33
BK1608LL121
EXT_MIC1_2
EXT_MIC2_2
R190
R188
10K
EXT_MIC1_3
EXT_MIC2_3
MIC1_1
MIC2_1
C448
C449
1U
MIC1 (22)
MIC2 (22)
C266
68P
C254
68P
R378 100K
C452 100P
R375 100K
C443 100P
SI stage: change to 10k for Mic gain
R229 0
Q21
*2N7002E
Q19
*2N7002E
HP_L_1
HP_L_2
HP_CONTROL
SI2 sage:change to 0 ohm for
EA audio issue
0.1U/10V C256
0 ohm C284
0.1U/10V C463
R230 0
Q22
*2N7002E
Q20
*2N7002E
HP_R_1
HP_R_2
HP_CONTROL
R371
470
R373
470
C248
4.7U
R372
3.9K
R374
3.9K
C262
4.7U
0.1U/10V C455
R370 0 1206
0.1U/10V C318
0.1U/10V C314
MIC
EXT_MIC1
EXT_MIC2
L36
L35
BK1608LL121
EXT_MIC1_4
EXT_MIC2_4
CN29
MIC-JACK-PINK
C265
470P
C275
470P
(22) SENSE_A_B
R183
47K
MICSENSE
Q11
2N7002K
C252
0.1U
SI2 stage:change to 2N7002K for ESD issue
PROJECT : 0T2
Quanta Computer Inc.
Size
Custom
Document Number
AUDIO AMP&JACK
Rev
1A
Date: Thursday, March 22, 2007
Sheet 23 of 42


PV stage:reserve for EMI
GLAN_CLK
C689
*0.1U
JKCLK Pin
Power down 0MHz
10Mbps 5MHz
100Mbps 50MHz
1000Mbps 62.5MHz
SI stage:change to 1%
R84 33_R
(12) GLAN_CLK
(12) LAN_RSTSYNC
Link Speed LCI GLCI
1000Mbps Runing Runing
100Mbps Runing Idle
10Mbps Runing Idle
No Link Runing or power down Idle
Power down Power down Power down
(12) LAN_TXD0 R320 LAN_TXD0_R
(12) LAN_TXD1 R334 LAN_TXD1_R
(12) LAN_TXD2 R327 LAN_TXD2_R
(12) LAN_RXD0 R324 LAN_RXD0_R
(12) LAN_RXD1 R315 LAN_RXD1_R
(12) LAN_RXD2 R313 LAN_RXD2_R
(13) PCIE_RXP6 C400 0.1U/10V PCIE_RXP6_R
(13) PCIE_RXN6 C404 0.1U/10V PCIE_RXN6_R
(13) PCIE_TXP6
(13) PCIE_TXN6
R335 1.4K/F LAN_KMRN_RCOMP_P
LAN_KMRN_RCOMP_N
Layout Note:
Place the resistors less than 1" from LAN controller.
(14,25,32) LAN_LINKLED#
(25,32) LOM_ACTLED#
(25) TX0P_R TX0P_R
(25) TX0N_R TX0N_R
(25) TX1P_R TX1P_R
(25) TX1N_R TX1N_R
(25) TX2P_R TX2P_R
(25) TX2N_R TX2N_R
(25) TX3P_R TX3P_R
(25) TX3N_R TX3N_R
R307 *0
LAN_ATEST_P
LAN_ATEST_N
Layout Note:
Keep this resistor on top side.
Layout Note:
Connect the resistor to GND near ball E6
R336 1.4K/F LAN_RBIAS_P
PAD T85
R306 100/F
U6
JKCLK-JCLK
JRSTSYNC
JTXD0
JTXD1
JTXD2
JRXD0
JRXD1
JRXD2
GLAN_TXP-NC
GLAN_TXN-NC
GLAN_RXP-NC
GLAN_RXN-NC
KBIAS_P-RBIAS100
KBIAS_N-RBIAS10
LED0-LINK_UP_N
LED1-ACT_LED_N
LED2-SPEED_LED_N
MDI_PLUS[0]-TDP
MDI_MINUS[0]-TDN
MDI_PLUS[1]-RDP
MDI_MINUS[1]-RDN
MDI_PLUS[2]-NC
MDI_MINUS[2]-NC
MDI_PLUS[3]-NC
MDI_MINUS[3]-NC
IEEE_TEST_P-NC
IEEE_TEST_N-NC
RSVD_J6-NC
RSVD_J7-NC
RBIAS_P-NC
RBIAS_N-NC
RSVD_B5-NC
RSVD_A6-ADV10/LAN_DIS_N
RSVD_C5-NC
TEST_EN
LCI
GLCI
MDI
JTAG
JTAG_TCK-ISOL_TCK
JTAG_TDI-ISOL_TI
JTAG_TDO-TOUT
JTAG_TMS-ISOL_EXEC
XTAL2-X2
XTAL1-X1
VSSA[17]-NC
VSSA[16]-NC
VSSA[15]-VSSA2
VSSA[14]-VSS
VSSA[13]-NC
VSSA[12]-VSS
VSSA[11]-VSS
VSSA[10]-VSS
VSSA[09]-VSS
VSSA[08]-VSS
VSSA[07]-VSS
VSSA[06]-VSS
VSSA[05]-VSS
VSSA[04]-VSS
VSSA[03]-VSSR
VSSA[02]-NC
VSSA[01]-VSS
VSS[04]-VSS
VSS[03]-VSSP
VSS[02]-VSS
VSS[01]-NC
VDD1P0[03]-VCCA
VDD1P0[02]-VCCT
VDD1P0[01]-VCCR
VCCF1P0-VCC
VCCFC1P0-VCC
VCC3P3[02]-VCCP
VCC3P3[01]-VCC
VCC1P8[04]-NC
VCC1P8[03]-NC
VCC1P8[02]-NC
VCC1P8[01]-NC
VCC1P0-VCCA2
VCC[02]
VCC[01]
V1P0_OUT-NC
CTRL_10-NC
CTRL_18-NC
THERM_D_P-NC
THERM_D_N-NC
+1.0V_LOM
+1.8V_LOM
CTRL_10
CTRL_18
+3VM_LAN_SW
C396 0.1U/10V
C77 4.7U/10V
R305 *0
LAN_THERM_D_P
LAN_THERM_D_N
Layout Note:
Keep this resistor on top side.
NINEVEH-EKRON_N (REV 1p0)
PAD T14
PAD T16
PAD T90
PAD T15
R982 *200
R983 *200
DB1A stage:reserve
SI2 stage:add R1053 for LAN issue R1053
C410 27P/50V
Y4 25MHz
C411 27P/50V
LOM_XTAL2
LOM_XTAL1
DB2 stage:change to vender: KDS for intel recommend
C377 0.01U/25V
Q10 BCP69T1
C367 0.1U/10V
C40 4.7U/10V
C78 10U/6.3V
C376 0.01U/25V
Q9 BCP69T1
C368 0.1U/10V
C54 4.7U/10V
C70 10U/6.3V
R317 49.9/F
R321 49.9/F
R314 49.9/F
R311 49.9/F
C391 0.1U/10V
C385 0.1U/10V
R325 49.9/F
R328 49.9/F
R330 49.9/F
R332 49.9/F
C397 0.1U/10V
C407 0.1U/10V
Layout Note:
Place termination resistors close to LAN controller(less than 0.25").
C71 22U/4V
C406 0.1U/10V
C402 0.1U/10V
C395 0.1U/10V
C388 0.1U/10V
C375 0.1U/10V
C382 470P/50V
C69 22U/4V
C378 0.1U/10V
C401 0.1U/10V
C393 0.1U/10V
C387 0.1U/10V
C379 0.1U/10V
C405 0.1U/10V
C394 0.1U/10V
C380 0.1U/10V
C392 470P/50V
PROJECT : 0T2
Quanta Computer Inc.
Size Custom
Document Number LAN(Nineveh)
Rev 1A
Date: Thursday, March 22, 2007
Sheet 24 of 42

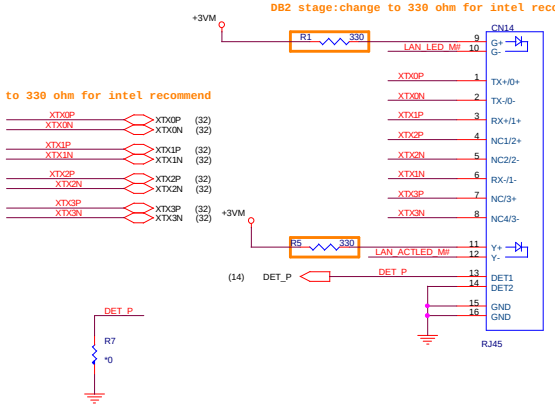
LAN

RJ45 Connector

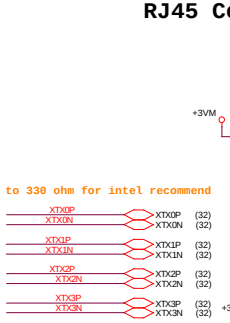


DB1A tage:Remove U1, RP24, RP25, RP26, RP27, and RP1,C24,C26,C28,R941-R951

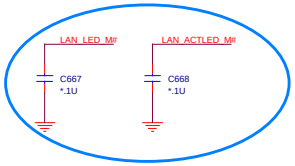
DB2 stage:change to 330 ohm for intel recommend



DB2 stage:change to 330 ohm for intel recommend

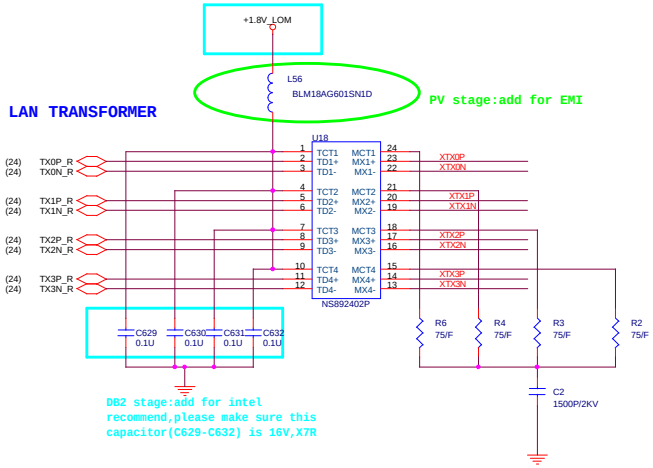


SI2 stage:EMI suggest



DB2 stage:change to +1.8V_LOM for intel recommend

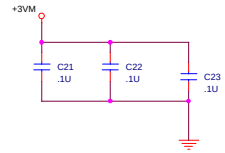
LAN TRANSFORMER



PV stage:add for EMI

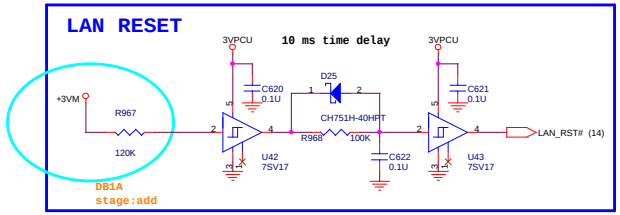
DB2 stage:add for intel recommend,please make sure this capacitor(C629-C632) is 16V,X7R

SI2 stage:change power source for HP request



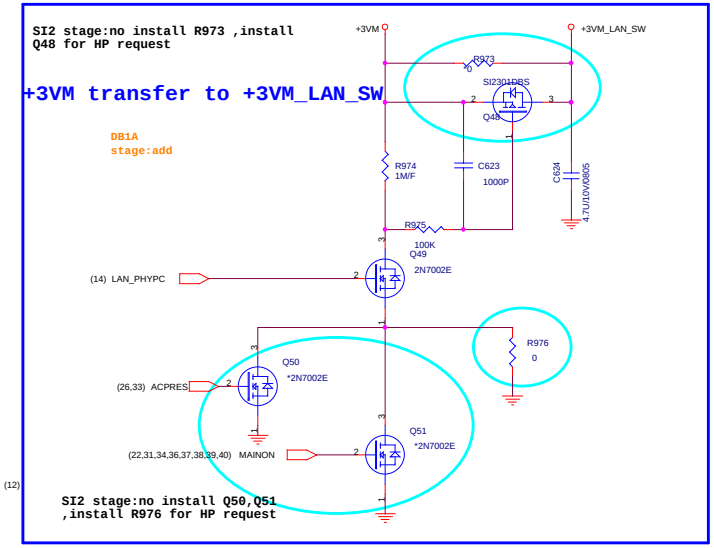
PVstage:delete C27

LAN RESET



SI2 stage:no install R973 ,install Q48 for HP request

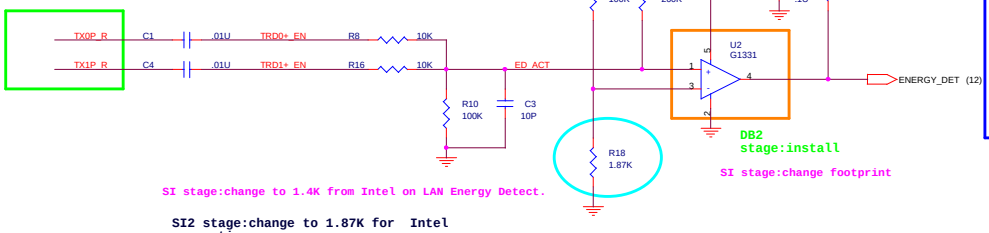
+3VM transfer to +3VM_LAN_SW



SI2 stage:no install Q50,Q51 ,install R976 for HP request

LAN Energy Detect circuit

82556 Support Deep Smart Power Down Feature for power saving



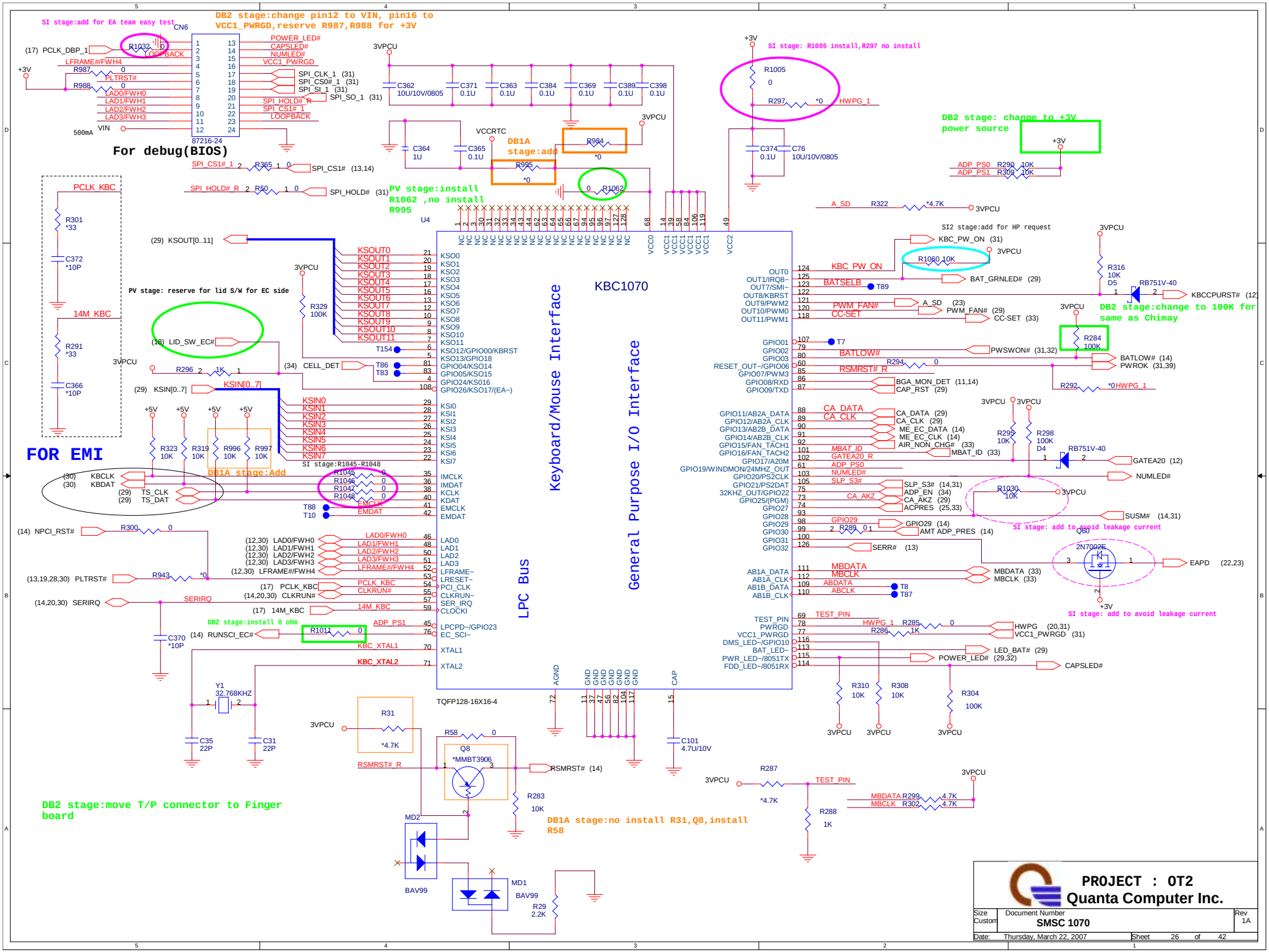
SI stage:change to 1.4K from Intel on LAN Energy Detect.

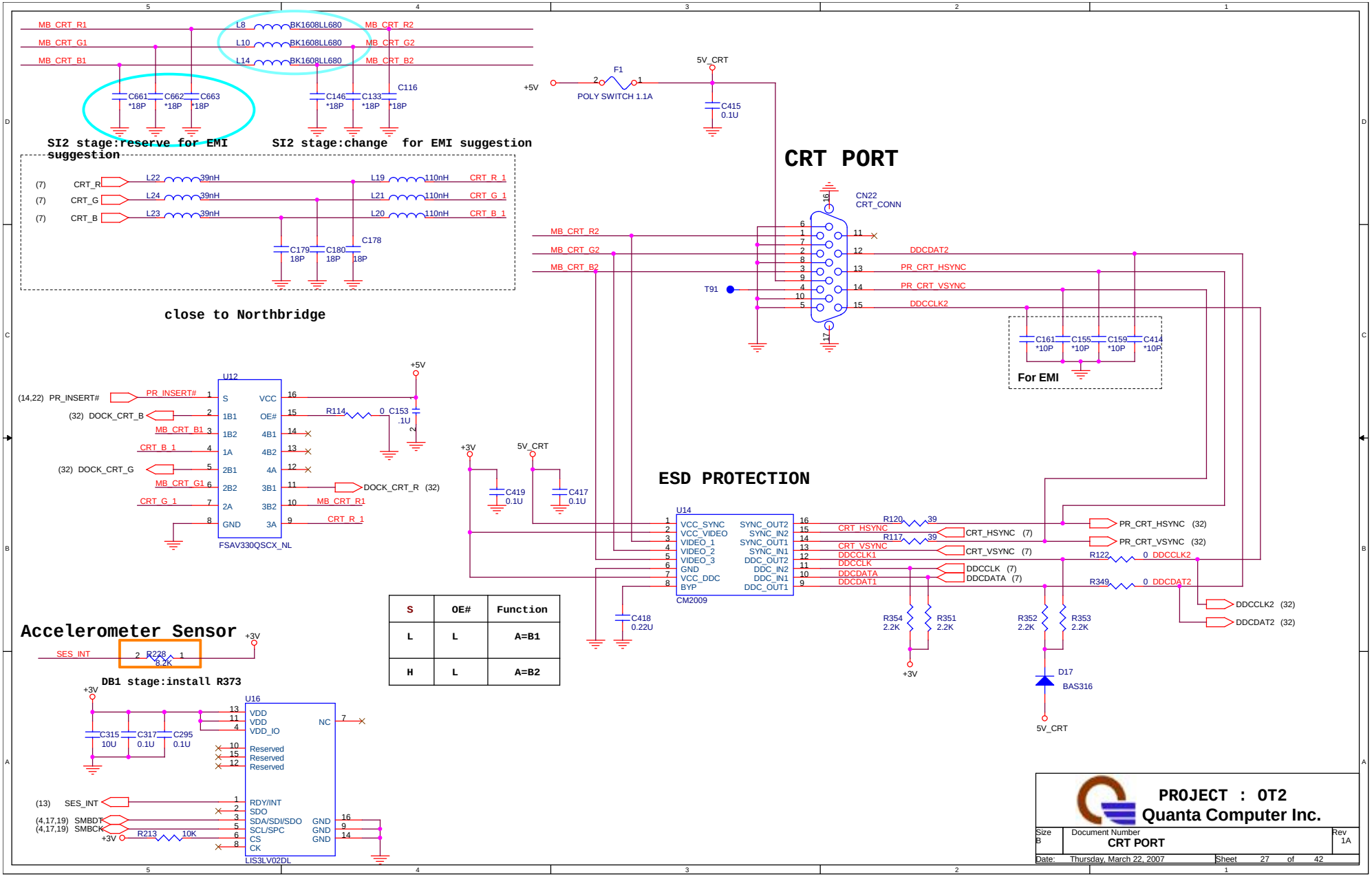
SI2 stage:change to 1.87K for Intel suggestion

PROJECT : OT2
Quanta Computer Inc.

Size	Document Number	Rev
C	Transformer&RJ45	1A

Date: Thursday, March 22, 2007 Sheet 25 of 42

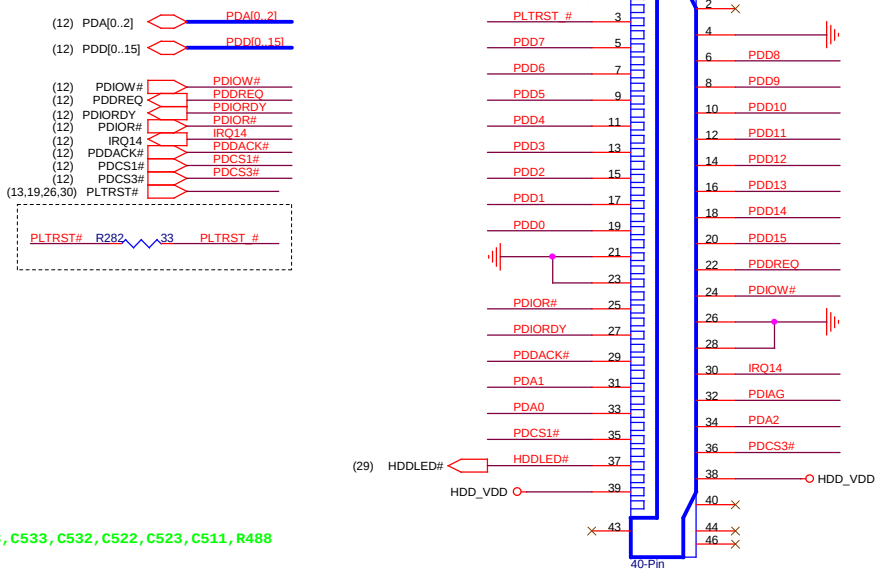

SI stage:add for EA team easy test
DB2 stage:change pin12 to VIN, pin16 to VCC1_PWRGD,reserve R987,R988 for +3V
CN6
87216-24
For debug(BIOS)
SI stage: R1005 install,R297 no install
DB2 stage: change to +3V power source
DB1A stage:add
PV stage:install R1062 ,no install R995
U4
KBC1070
Keyboard/Mouse Interface
General Purpose I/O Interface
LPC Bus
TQFP128-16X16-4
PV stage: reserve for lid S/W for EC side
SI2 stage:add for HP request
DB2 stage:change to 100K for same as Chimay
SI stage:R1045-R1048
DB1A stage:Add
FOR EMI
SI stage: add to avoid leakage current
DB2 stage:install 0 ohm
DB2 stage:move T/P connector to Finger board
DB1A stage:no install R31,Q8,install R58
PROJECT : 0T2
Quanta Computer Inc.
Size Custom
Document Number SMSC 1070
Rev 1A
Date: Thursday, March 22, 2007
Sheet 26 of 42

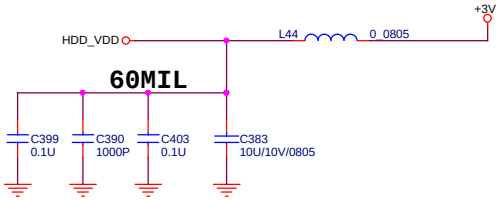


S	OE#	Function
L	L	A=B1
H	L	A=B2

HDD, CD-ROM

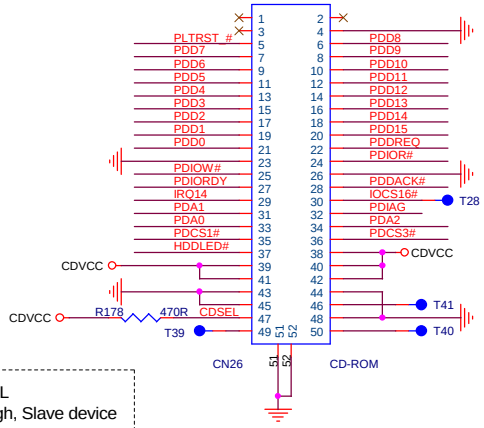
1.8 inch HDD CONNECTOR

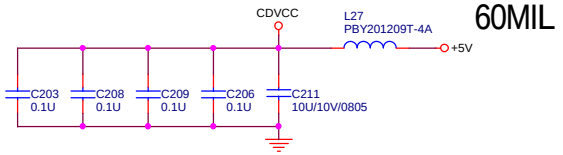




DB2 Stage:delete CN9,R463,C533,C532,C522,C523,C511,R488

CD-ROM



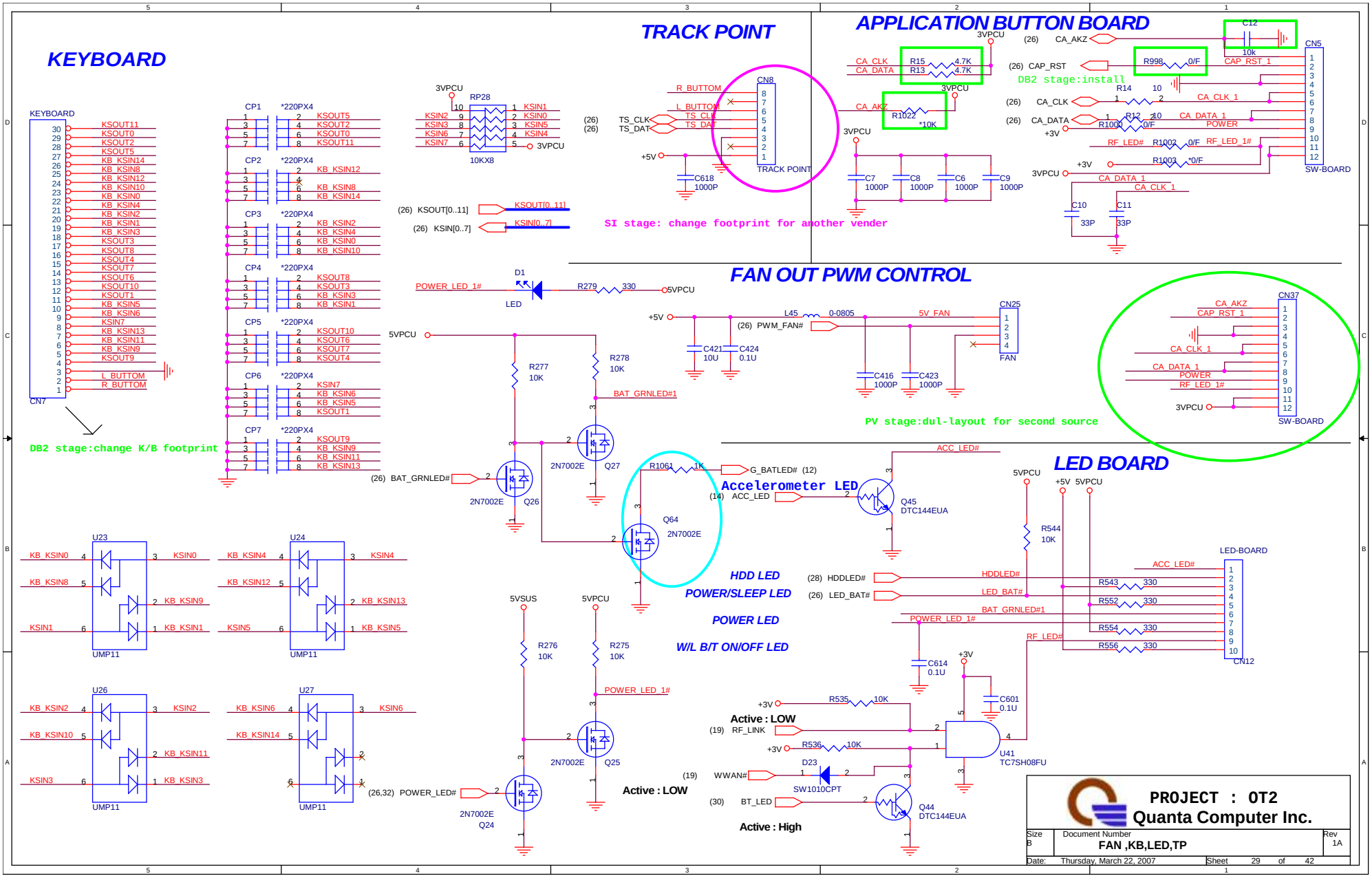


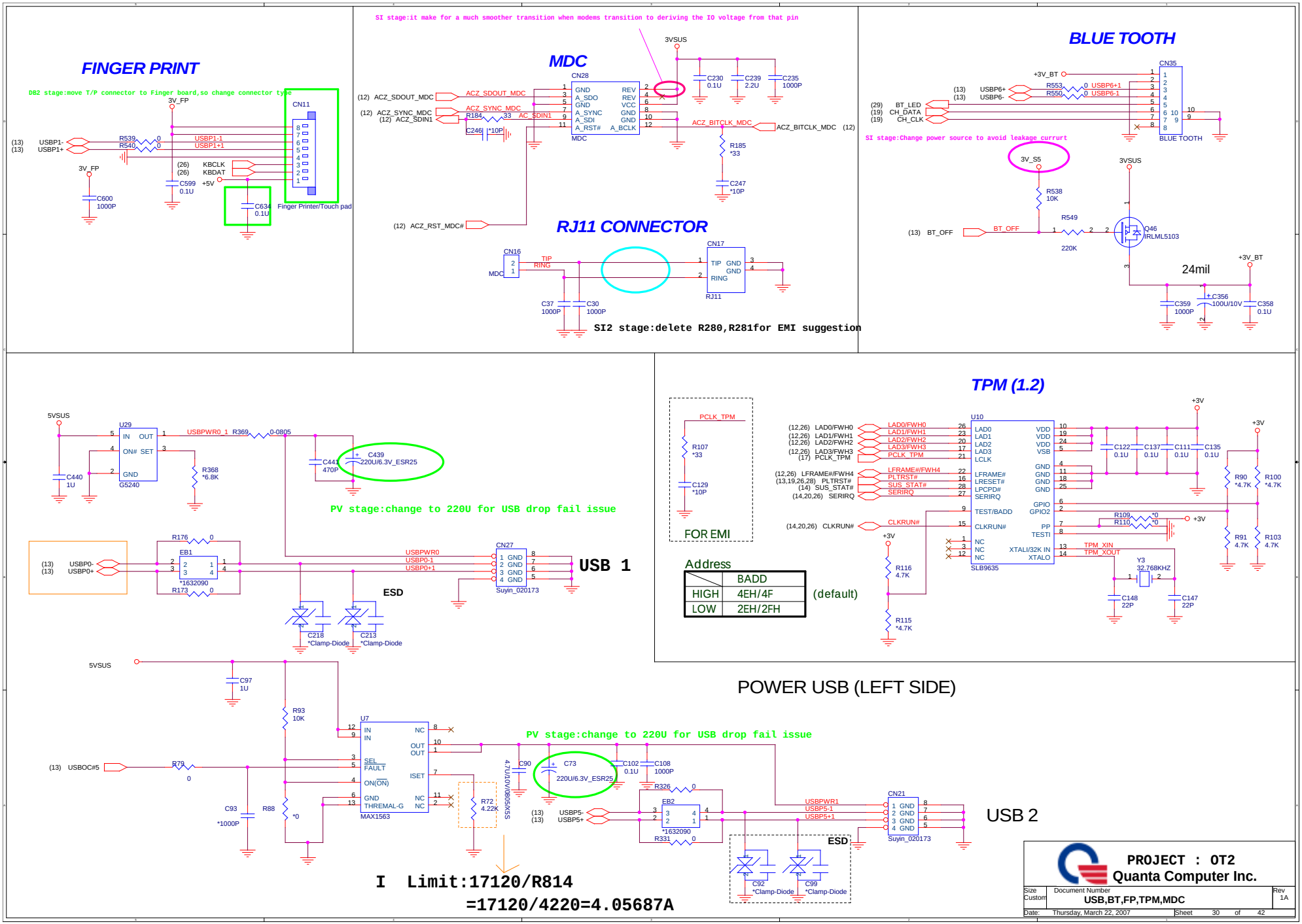
CDSEL
--> High, Slave device

PROJECT : 0T2
Quanta Computer Inc.

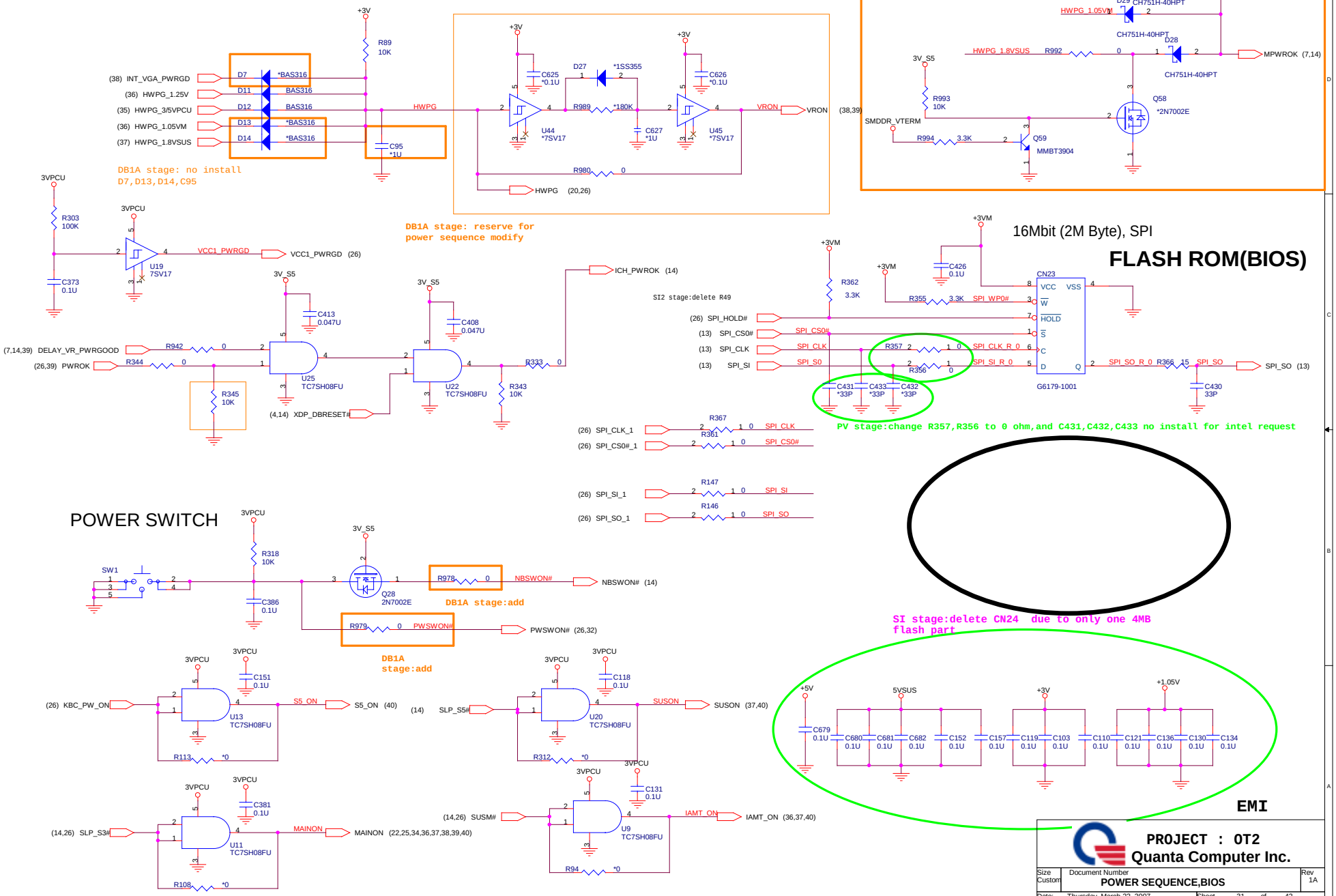
Size	Document Number	Rev
B	HDD,CD-ROM	1A

Date: Thursday, March 22, 2007 Sheet 28 of 42


KEYBOARD
TRACK POINT
APPLICATION BUTTON BOARD
FAN OUT PWM CONTROL
LED BOARD
DB2 stage:change K/B footprint
SI stage: change footprint for another vender
DB2 stage:install
PV stage:dul-layout for second source
Accelerometer LED
HDD LED
POWER/SLEEP LED
POWER LED
W/L B/T ON/OFF LED
Active : LOW
Active : High
PROJECT : 0T2
Quanta Computer Inc.
Document Number
FAN ,KB,LED,TP
Rev 1A
Size B
Date: Thursday, March 22, 2007
Sheet 29 of 42


FINGER PRINT
DB2 stage:move T/P connector to Finger board,so change connector type
CN11
Finger Printer/Touch pad
MDC
SI stage:it make for a much smoother transition when modems transition to deriving the IO voltage from that pin
CN28
RJ11 CONNECTOR
CN16
CN17
SI2 stage:delete R280,R281for EMI suggestion
BLUE TOOTH
CN35
SI stage:Change power source to avoid leakage currurt
24mil
TPM (1.2)
FOR EMI
Address
BADD
HIGH 4EH/4F
LOW 2EH/2FH
(default)
U10
SLB9635
Y3 32.768KHZ
POWER USB (LEFT SIDE)
USB 1
PV stage:change to 220U for USB drop fail issue
ESD
CN27
Suyin_020173
U29
G5240
U7
MAX1563
USB 2
CN21
I Limit:17120/R814
=17120/4220=4.05687A
PROJECT : OT2
Quanta Computer Inc.
Size Custom
Document Number USB,BT,FP,TPM,MDC
Rev 1A
Date: Thursday, March 22, 2007
Sheet 30 of 42

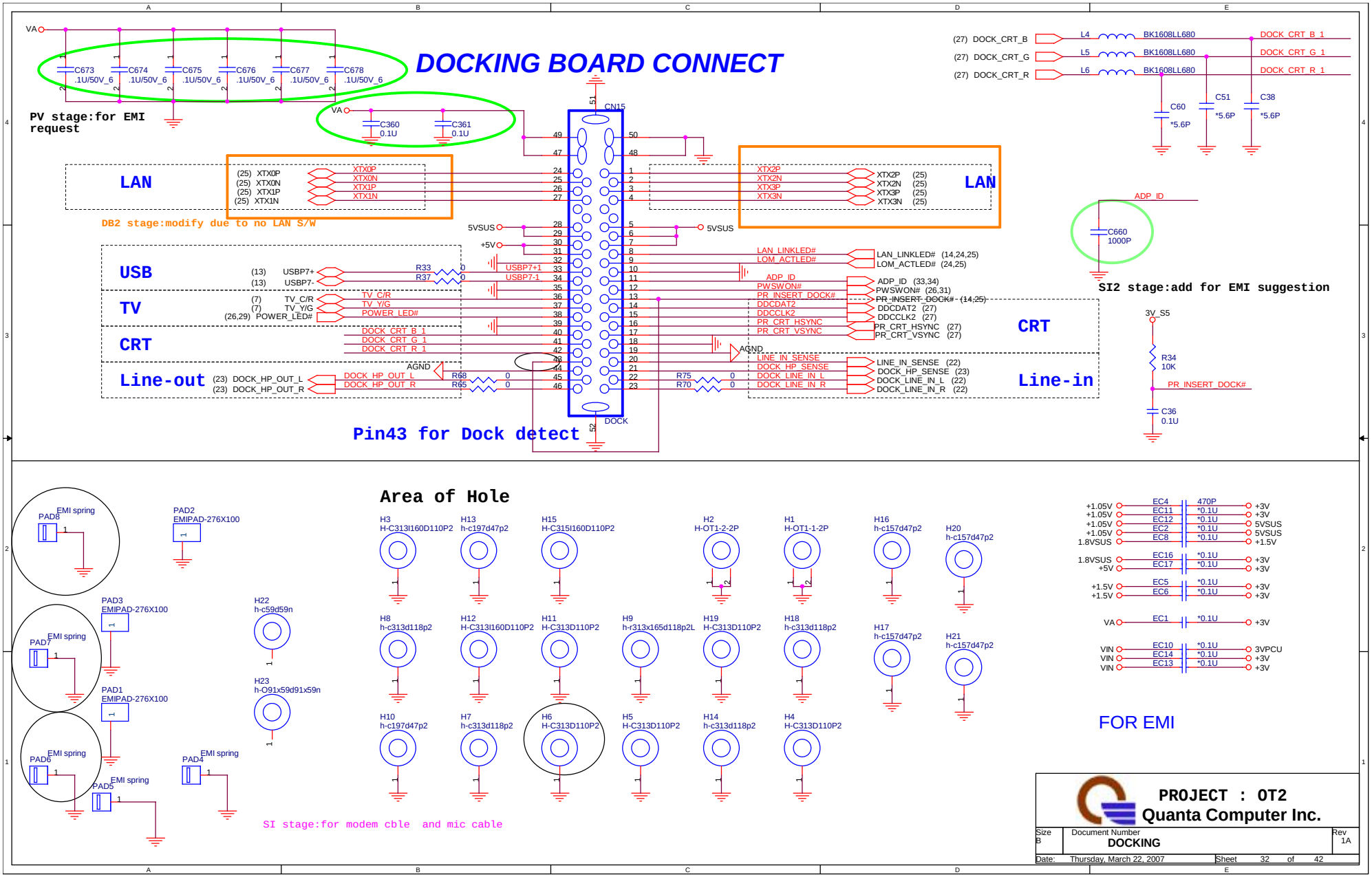
POWER SEQUENCE

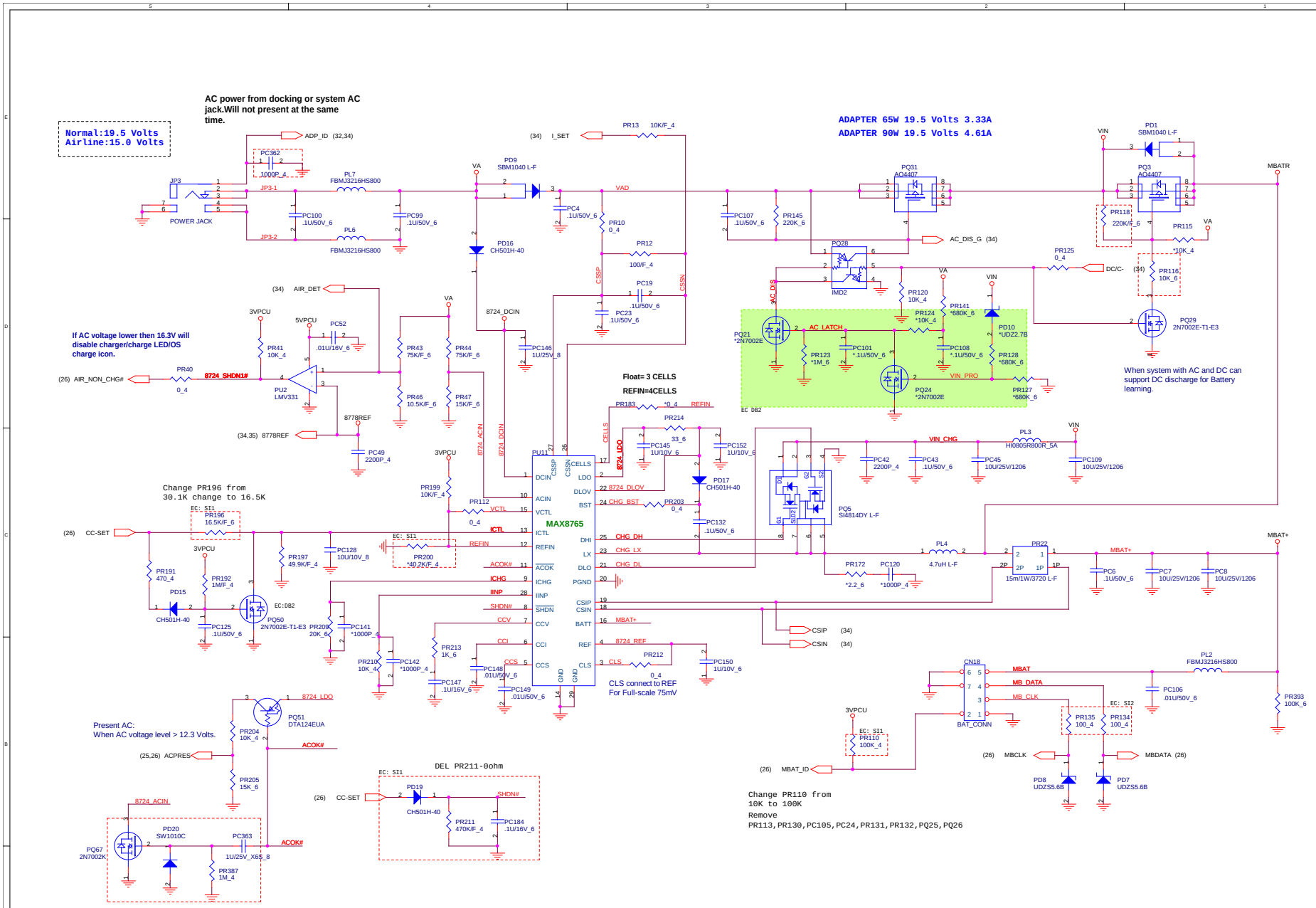


PROJECT : 0T2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	POWER SEQUENCE,BIOS	1A

Date: Thursday, March 22, 2007 Sheet 31 of 42

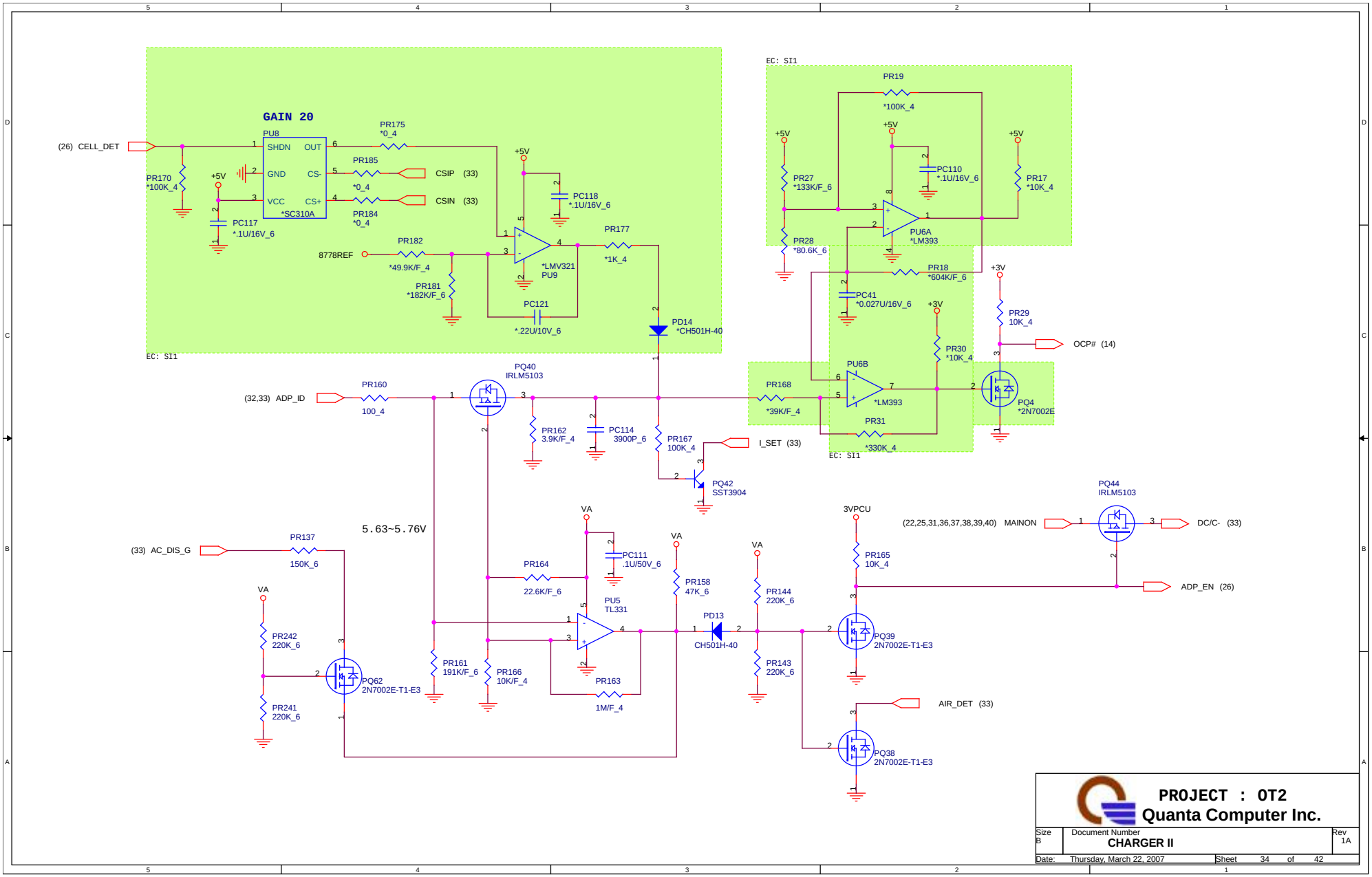

DOCKING BOARD CONNECT
PV stage:for EMI request
C673 .1U/50V_6
C674 .1U/50V_6
C675 .1U/50V_6
C676 .1U/50V_6
C677 .1U/50V_6
C678 .1U/50V_6
C360 0.1U
C361 0.1U
CN15
DOCK
LAN
DB2 stage:modify due to no LAN S/W
USB
TV
CRT
Line-out
Line-in
Pin43 for Dock detect
(27) DOCK_CRT_B
(27) DOCK_CRT_G
(27) DOCK_CRT_R
L4 BK1608LL680
L5 BK1608LL680
L6 BK1608LL680
DOCK_CRT_B_1
DOCK_CRT_G_1
DOCK_CRT_R_1
C60 *5.6P
C51 *5.6P
C38 *5.6P
ADP_ID
C660 1000P
SI2 stage:add for EMI suggestion
3V_S5
R34 10K
PR_INSERT_DOCK#
C36 0.1U
Area of Hole
PAD8 EMI spring
PAD2 EMIPAD-276X100
PAD3 EMIPAD-276X100
PAD7 EMI spring
PAD1 EMIPAD-276X100
PAD6 EMI spring
PAD5 EMI spring
PAD4 EMI spring
H22 h-c59d59n
H23 h-O91x59d91x59n
H3 H-C313l160D110P2
H13 h-c197d47p2
H15 H-C315l160D110P2
H2 H-OT1-2-2P
H1 H-OT1-1-2P
H16 h-c157d47p2
H20 h-c157d47p2
H8 h-c313d118p2
H12 H-C313l160D110P2
H11 H-C313D110P2
H9 h-r313x165d118p2L
H19 H-C313D110P2
H18 h-c313d118p2
H17 h-c157d47p2
H21 h-c157d47p2
H10 h-c197d47p2
H7 h-c313d118p2
H6 H-C313D110P2
H5 H-C313D110P2
H14 h-c313d118p2
H4 H-C313D110P2
SI stage:for modem cble and mic cable
EC4 470P
EC11 *0.1U
EC12 *0.1U
EC2 *0.1U
EC8 *0.1U
EC16 *0.1U
EC17 *0.1U
EC5 *0.1U
EC6 *0.1U
EC1 *0.1U
EC10 *0.1U
EC14 *0.1U
EC13 *0.1U
FOR EMI
PROJECT : OT2
Quanta Computer Inc.
Size B
Document Number DOCKING
Rev 1A
Date: Thursday, March 22, 2007
Sheet 32 of 42

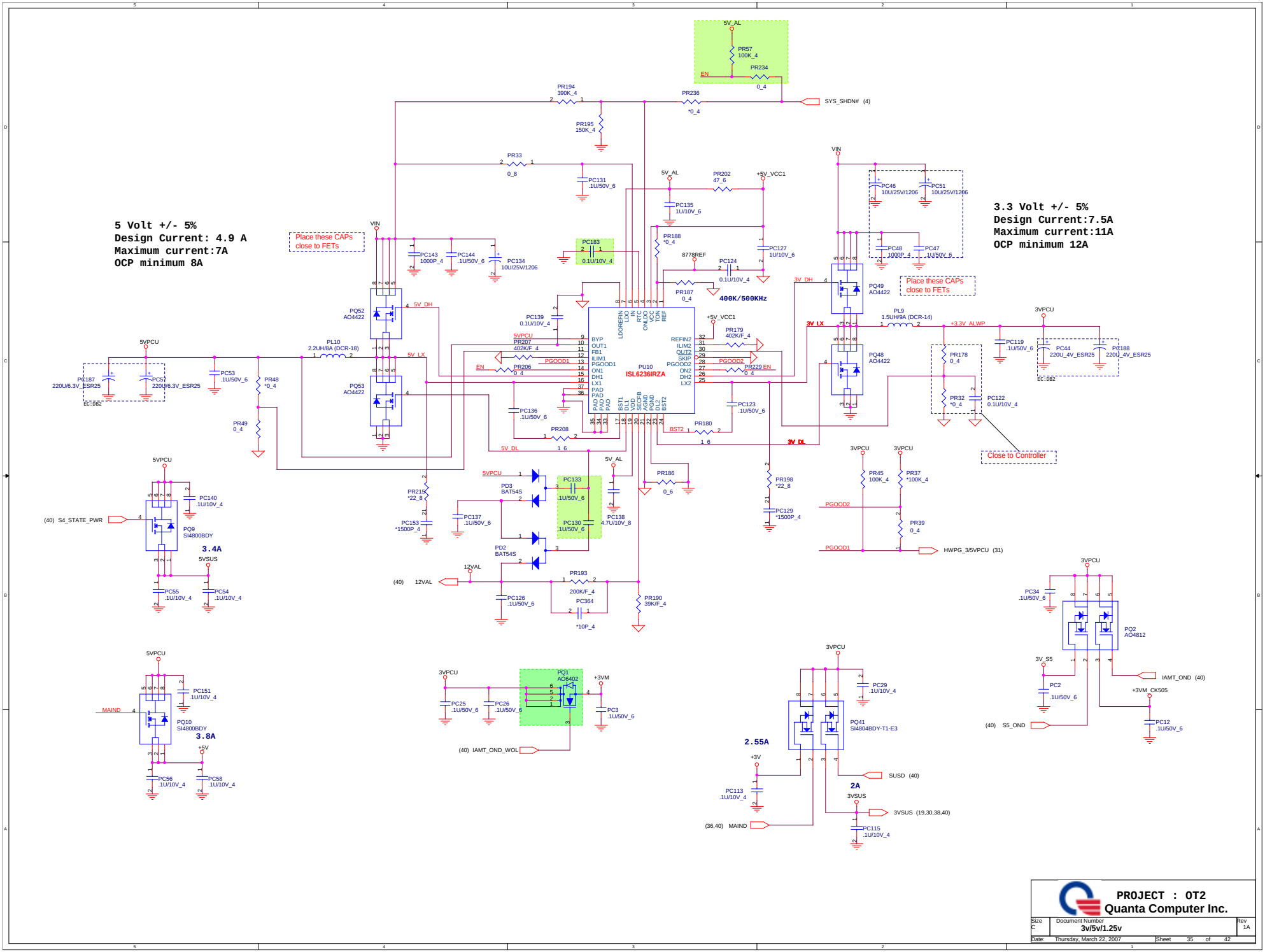


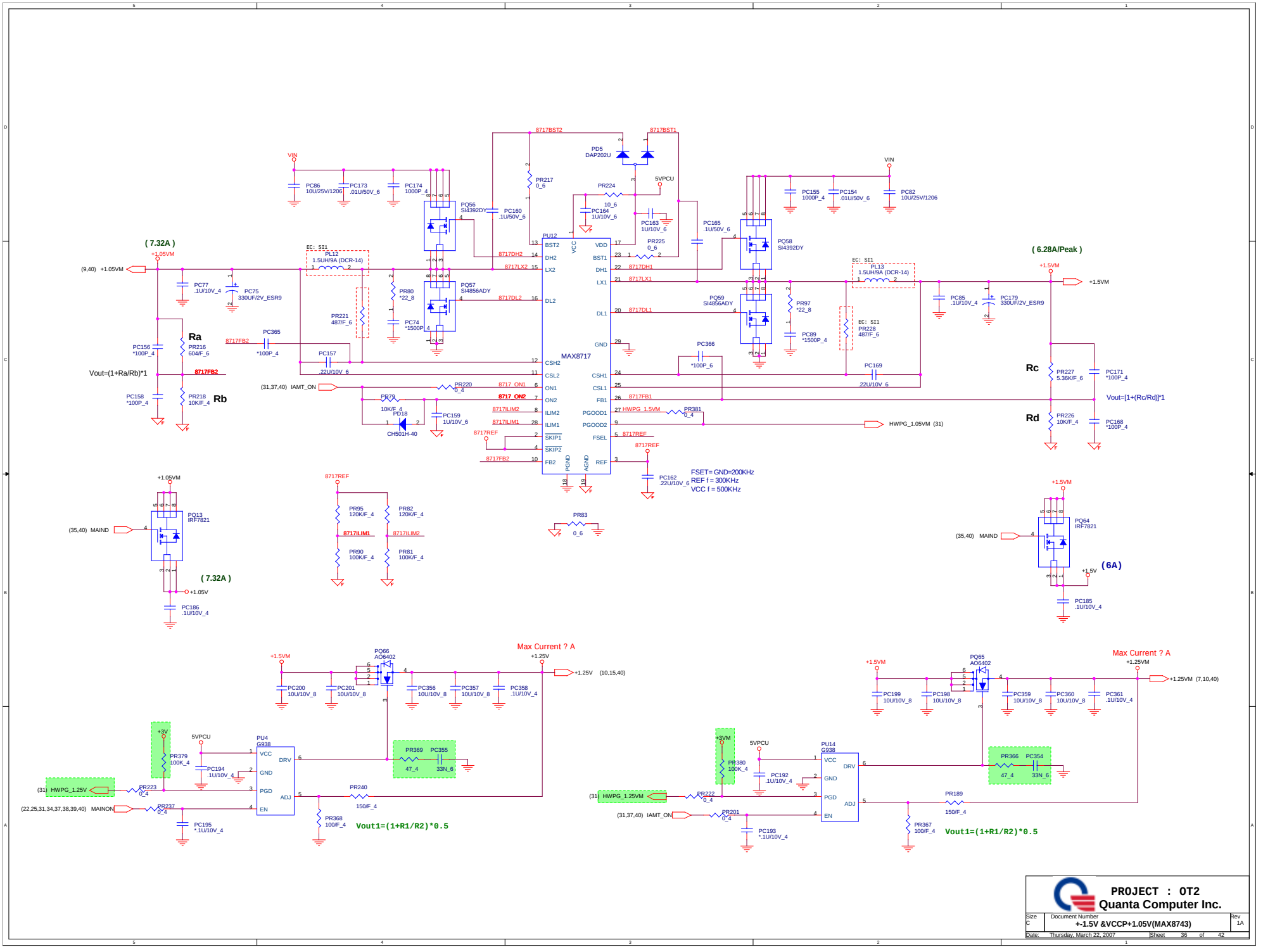
PROJECT : OT2
Quanta Computer Inc.

Size	Document Number	Rev
C	CHARGE(MAX1908/8724)	1A

Date: Thursday, March 22, 2007 Sheet 33 of 42


GAIN 20
PU8
SHDN
OUT
GND
CS-
VCC
CS+
*SC310A
(26) CELL_DET
PR170
*100K_4
+5V
PC117
*.1U/16V_6
PR175
*0_4
PR185
*0_4
PR184
*0_4
CSIP (33)
CSIN (33)
PC118
*.1U/16V_6
PR177
*1K_4
8778REF
PR182
*49.9K/F_4
PR181
*182K/F_6
*LMV321
PU9
PC121
*.22U/10V_6
PD14
*CH501H-40
EC: SI1
PR19
*100K_4
PR27
*133K/F_6
PR28
*80.6K_6
PC110
*.1U/16V_6
PU6A
*LM393
PR17
*10K_4
PR18
*604K/F_6
PC41
*0.027U/16V_6
+3V
PR29
10K_4
OCP# (14)
PR30
*10K_4
PU6B
*LM393
PR168
*39K/F_4
PR31
*330K_4
PQ4
*2N7002E
(32,33) ADP_ID
PR160
100_4
PQ40
IRLM5103
PR162
3.9K/F_4
PC114
3900P_6
PR167
100K_4
I_SET (33)
PQ42
SST3904
5.63~5.76V
(33) AC_DIS_G
PR137
150K_6
VA
PR242
220K_6
PR241
220K_6
PQ62
2N7002E-T1-E3
PR161
191K/F_6
PR166
10K/F_4
PR164
22.6K/F_6
PC111
.1U/50V_6
PU5
TL331
PR163
1M/F_4
PR158
47K_6
PD13
CH501H-40
PR144
220K_6
PR143
220K_6
3VPCU
PR165
10K_4
PQ39
2N7002E-T1-E3
AIR_DET (33)
PQ38
2N7002E-T1-E3
(22,25,31,36,37,38,39,40) MAINON
PQ44
IRLM5103
DC/C- (33)
ADP_EN (26)
PROJECT : 0T2
Quanta Computer Inc.
Size B
Document Number
CHARGER II
Rev 1A
Date: Thursday, March 22, 2007
Sheet 34 of 42

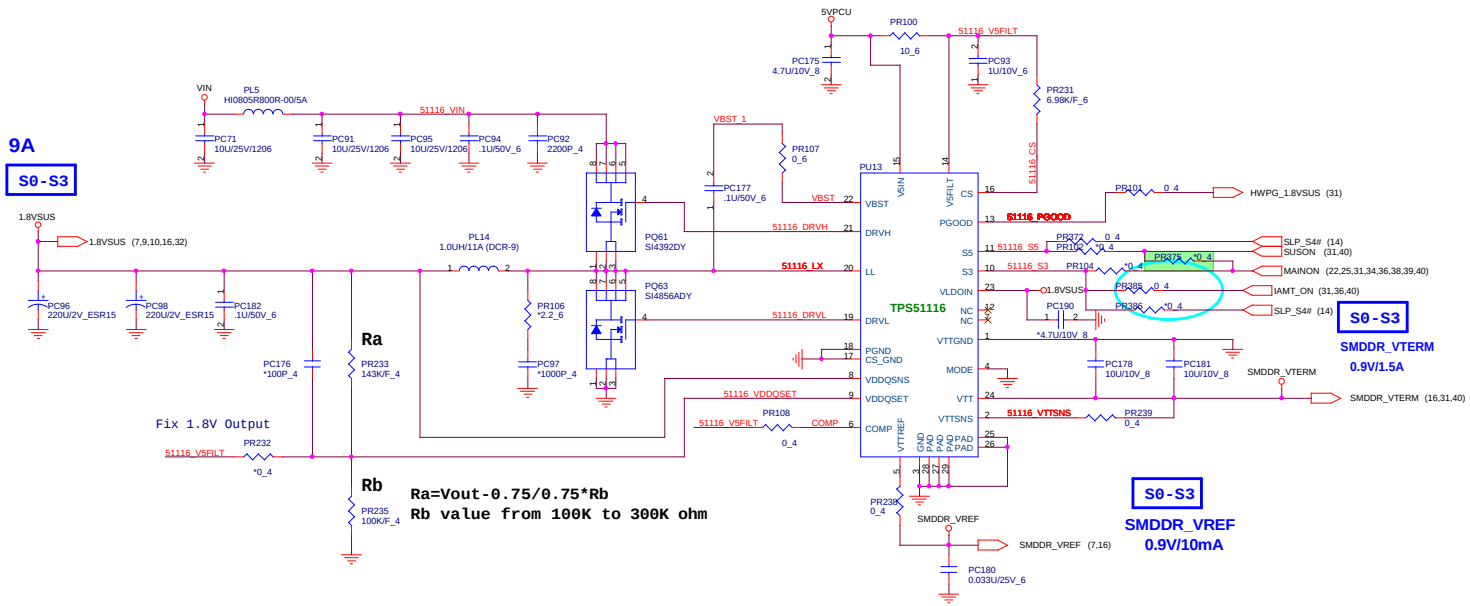

5 Volt +/- 5%
Design Current: 4.9 A
Maximum current:7A
OCP minimum 8A
3.3 Volt +/- 5%
Design Current:7.5A
Maximum current:11A
OCP minimum 12A
Place these CAPs close to FETs
Place these CAPs close to FETs
Close to Controller
400K/500KHz
ISL6236IRZA
PU10
PQ52 AO4422
PQ53 AO4422
PQ49 AO4422
PQ48 AO4422
PQ9 SI4800BDY
PQ10 SI4800BDY
PQ1 AO6402
PQ41 SI4804BDY-T1-E3
PQ2 AO4812
PL10 2.2UH/8A (DCR-18)
PL9 1.5UH/9A (DCR-14)
PD3 BAT54S
PD2 BAT54S
3.4A
3.8A
2.55A
2A
SYS_SHDN# (4)
(40) S4_STATE_PWR
MAIND
(40) 12VAL
(40) IAMT_OND_WOL
IAMT_OND (40)
(40) S5_OND
SUSD (40)
3VSUS (19,30,38,40)
(36,40) MAIND
HWPG_3/5VPCU (31)
PROJECT : OT2
Quanta Computer Inc.
Size C
Document Number 3v/5v/1.25v
Rev 1A
Date: Thursday, March 22, 2007
Sheet 35 of 42



PROJECT : OT2
Quanta Computer Inc.

Size	Document Number	Rev
C	+-1.5V &VCCP+1.05V(MAX8743)	1A

Date: Thursday, March 22, 2007 Sheet 36 of 42



V_TRIP(mV)=R_TRIP(Kohm)*10(uA)

I_OCP=V_trip/Rds_on+I_Ripple/2

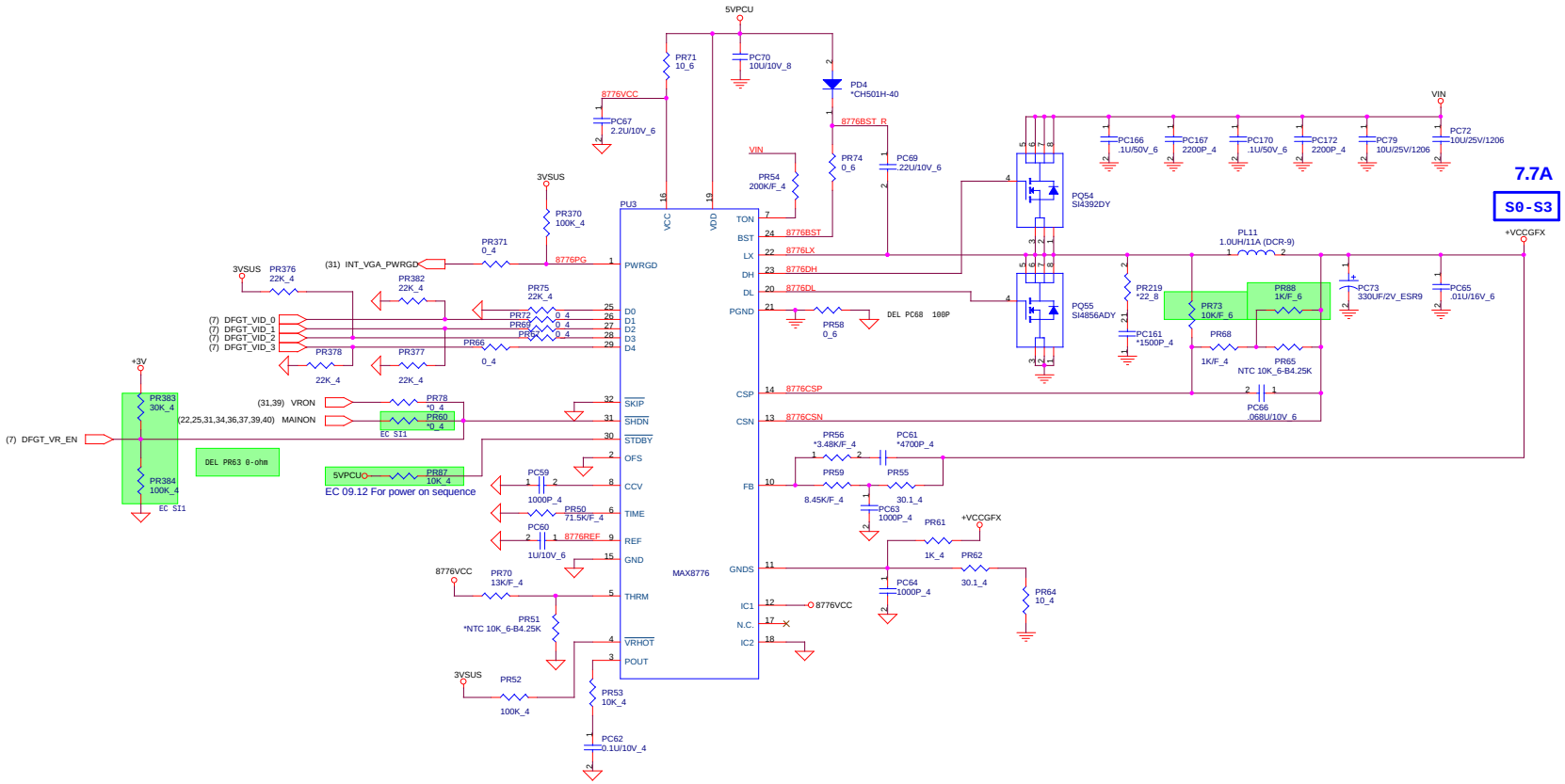
VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V _vddqsns/2	DDR2
FB	Adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

PROJECT : OT2
Quanta Computer Inc.

Size	Document Number	Rev
C	ti51116(1.8VSUS/DDR_VTERM)	1A

Date: Thursday, March 22, 2007 Sheet 37 of 42



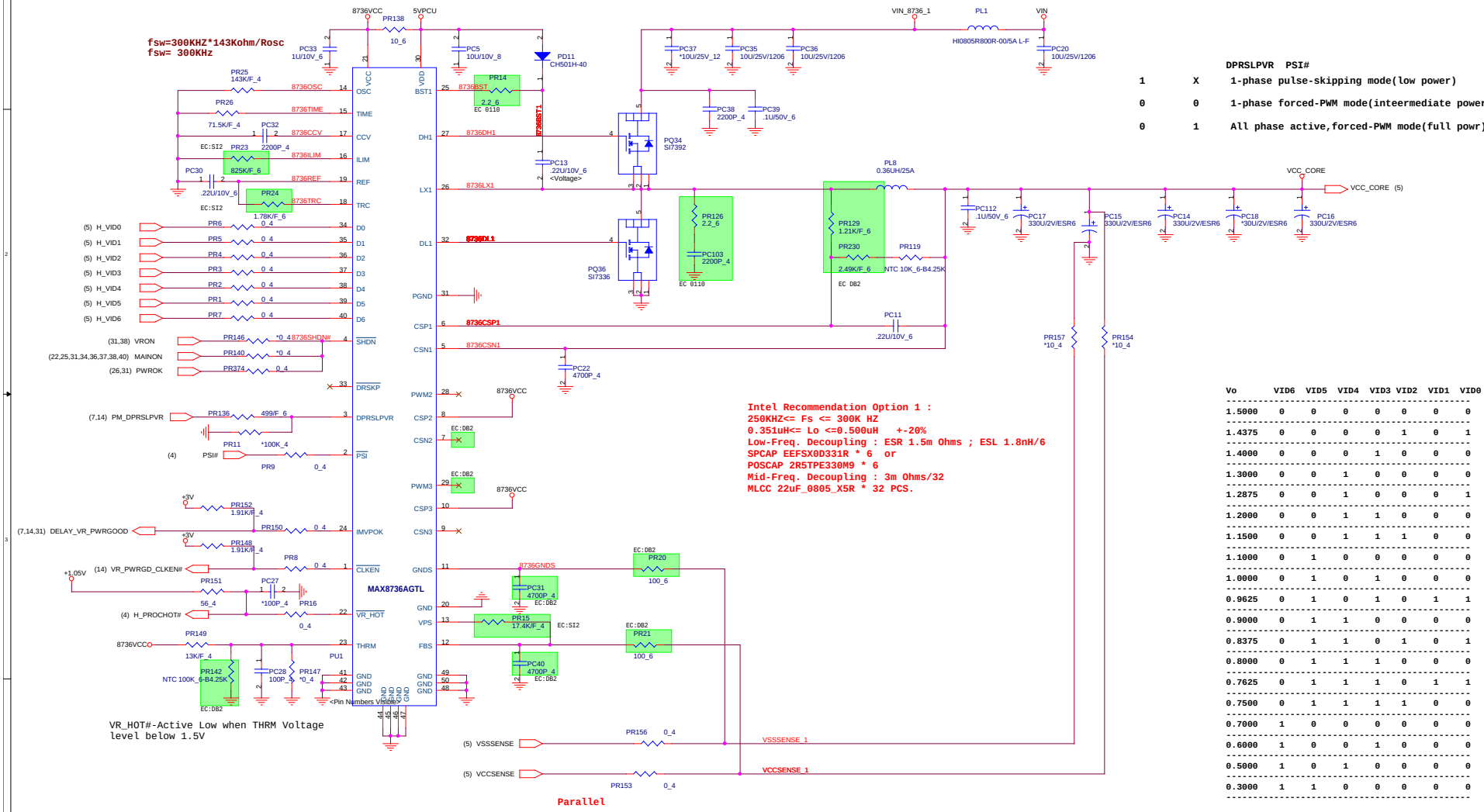
PROJECT : OT2
Quanta Computer Inc.

Size	Document Number	Rev
C	GMCH (MAX8776)	1A

Date: Thursday, March 22, 2007 Sheet 38 of 42

DPRSLPVR	DPRSTP#	PSI#	State	CPU Current
1	0	0	Deeper Sleep	< 3A
1	0	1	Deeper Sleep	> 3A
0	1	0	Active Mode	< 18A
0	1	1	Active Mode	> 15A

RVPS = RDROOP / (RSENSE x GM) = 5.1mV/A / (0.001 x 200uS) =25.5K
RTRC = RSENSE x 5k / (RDROOP(AC) x # of Phases) = 0.001 x 5k / ((5.1mV/A x 80%) x 1phases) =1.24K
RILIMPK = Battery V x RTRC / (IPK x RSENSE) = 8V x 1.24K / (Ioutput peak x 0.001) OCP=17.7A
fsw=300kHZ*143kohm/Rosc
dV_Target/dt=12.5mV/us*71.5kohm/R_TIME



	DPRSLPVR	PSI#
	1	X
	0	0
	0	1

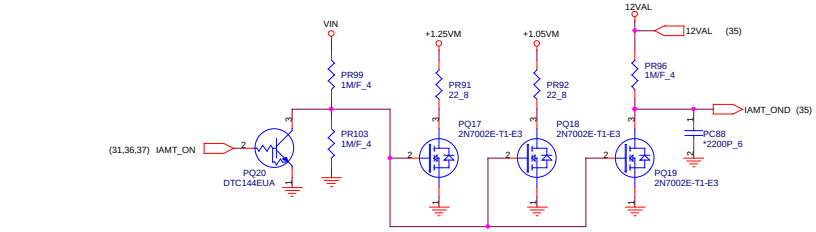
1-phase pulse-skipping mode(low power)
1-phase forced-PWM mode(inteermediate power)
All phase active,forced-PWM mode(full powr)

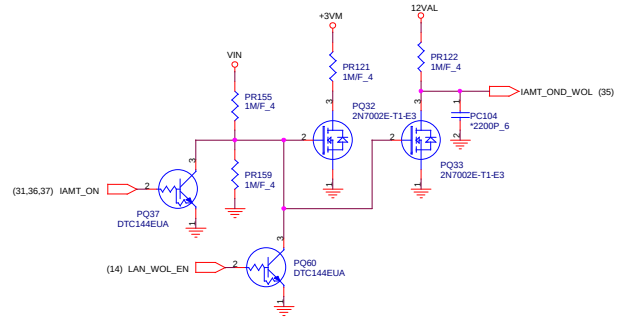
Vo	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.5000	0	0	0	0	0	0	0
1.4375	0	0	0	0	1	0	1
1.4000	0	0	0	1	0	0	0
1.3000	0	0	1	0	0	0	0
1.2875	0	0	1	0	0	0	1
1.2000	0	0	1	1	0	0	0
1.1500	0	0	1	1	1	0	0
1.1000	0	1	0	0	0	0	0
1.0000	0	1	0	1	0	0	0
0.9625	0	1	0	1	0	1	1
0.9000	0	1	1	0	0	0	0
0.8375	0	1	1	0	1	0	1
0.8000	0	1	1	1	0	0	0
0.7625	0	1	1	1	0	1	1
0.7500	0	1	1	1	1	0	0
0.7000	1	0	0	0	0	0	0
0.6000	1	0	0	1	0	0	0
0.5000	1	0	1	0	0	0	0
0.3000	1	1	0	0	0	0	0

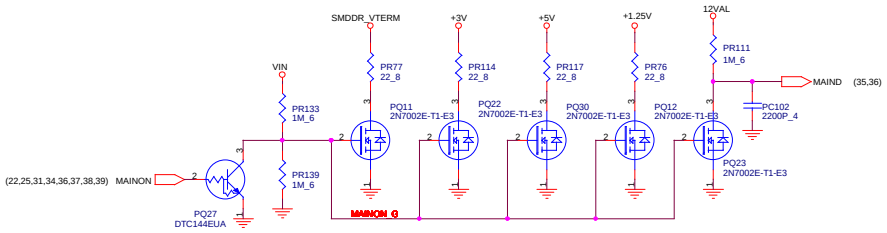
PROJECT : OT2
Quanta Computer Inc.

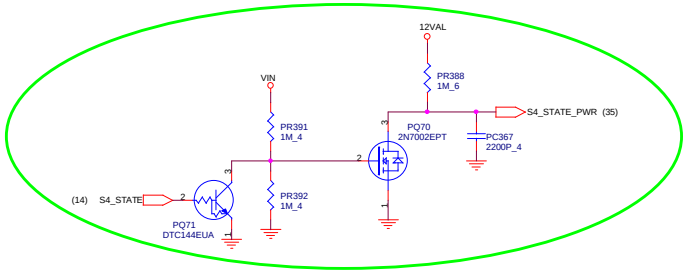
Size	Document Number	Rev
C	MAX8736	1A

Date: Thursday, March 22, 2007 Sheet 39 of 42

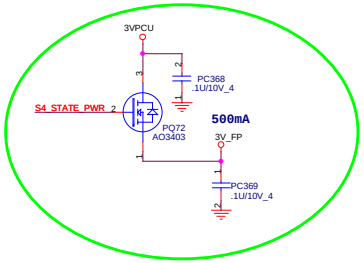




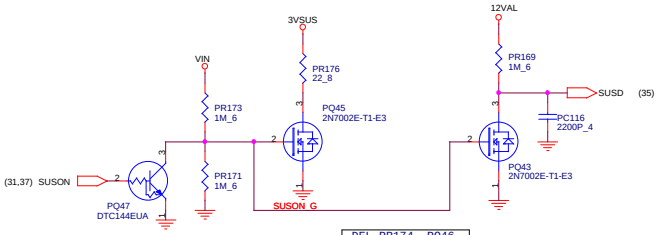




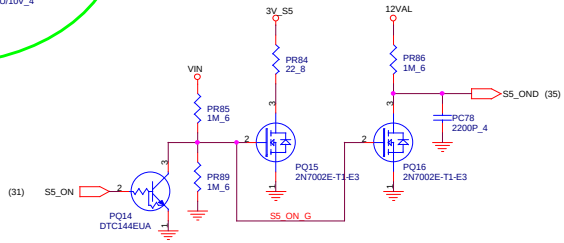
PV stager:add for HP request



PV stager:add for HP request



DEL PR174, PQ46
For S4-STATE



PROJECT : OT2
Quanta Computer Inc.

Size	Document Number	Rev
C	DISCHARGE	1A

Date: Thursday, March 22, 2007 Sheet 40 of 42

MODEL

OT2 MB
31OT2MBXXXX

CHANGE LIST

Date	Reason for change	Page	modify list
DB2 --->SI			
2006.11	change from 5VSUS to +5v due to not support wake up from suspend		change U35 pin13,15 to +5V
	change footprint to 0805 to easy prepare material		change U2, C577 footprint
	avoild leakage cruuent		change power plan from 3VSUS to 3V_S5 at RP31 , R241 , R448 , R538,change card bus switch poewr from 5VSUS to 5V R452 Install, R46 on instal;delete R496,Add D32 Add D33,D34 ;delete R293 ,and add Q60
	EC VCC2 pin is used in a comparator to sample when Vcc2 is going up or down. It will draw some current. Approx 300ua		R1005 install,R297 no install
	For auto boot issue		reserve R1029,add R1028 ,Q62 for auto power issue
	remove Kill switch function		remove Q37,R443,R426,CN1,R977
	add for EA team easy test		add R1031,R1032
	for internal mic issue		add C643, and modify pin 1 for U47 OP circuit and add C657
	modify footprint firm right angle tyoe to straight type		CN36
	change footprint for another vender for easy insert		change footprint for track point connector CN8
	move D31 close to ICH8 to solve battery LED issue ,else it will cause LED function abnormally		D31 close to ICH8 and pull up 10k(R1035) to +3V
	WWAN noise --- ICH improvement		reserve L53, L54,add R1033,R1034
	due to use 4MB flash part		delete CN24
	add strapping options for CPU_BSEL{0:2} so we can hardwire the clock to the FSB frequency if needed		R1036-R1044
	PU13.11, add IAMT_ON control signal option with 0-Ohm NO INSTALL to control power up of 0.9V This is to save system power in S3 when iAMT is disabled.		add PR385
	For ENERGY_DET, Change R18 to 1.4K, this is a change from Intel on LAN Energy Detect.		R18
DB2 --->SI2			
Date	schematic error and change to avoid leakage voltage		RP31 pin10 from 3V_S5 to 3VSUS
2007.1	change Lan crystal layout for intel suggestion		Lan crystal layout
	to avoid the ripple for signal CLK_PWRGD		add R1049 for intel suggestion
	tune Adp_Id signal for layout. to avoid overlay		for EMI suggestion
	for EMI suggestion		reseve C661,C662,C663
	for EMI suggestion(CRT)		L8,L10,L14 change to BK1608LL680
	for EMI suggestion(internal Mic)		reserve R664, R1050 for Mic
	for EMI suggestion(modem)		delete R280,R281 due to useless
	PWM signal(LCD)to avoid work abnormally		C5 no install
	change to 1.87K for Intel suggestion		change R18 to 1.87k
	Q61,D32 is for leakage voltage issue ,but will influence LAN function ,change to 0 ohm		delete Q61,add R1051;deleteD32,Add R1052

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MODEL

DB2 --->SI2

OT2 MB
31OT2MBXXXX

CHANGE LIST

Date	Reason for change	Page	modify list
2007.1	For LCD rush current issue		change R30 to 82K,C32 to 0.1u ,and change R20 power source to 3VPCU
	due to no use		delete R341,R1025,L9,L13,L15,L8,L10,L14,R342,R95,R81
SI2--->PV 2007.1			

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Custom	change list-2	1A

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