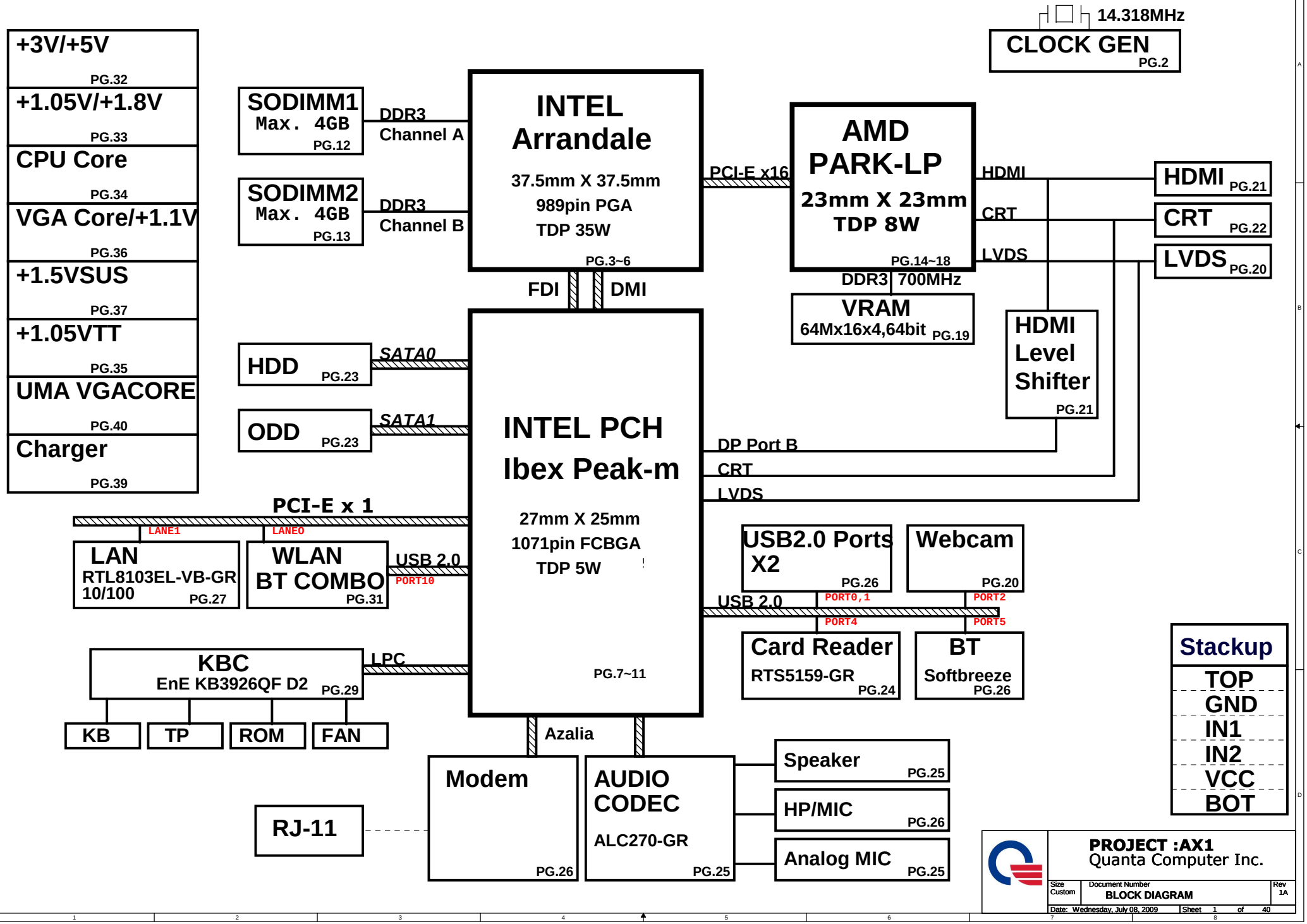
# AX1 INTEL UMA/DISCRETE SYSTEM DIAGRAM




PROJECT :AX1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | BLOCK DIAGRAM | 1A |

Date: Wednesday, July 08, 2009 Sheet 1 of 40

25mA
+1.05V
+VDDIO_CLK
L33
HCB1608KF-181T15_6
C454 0.1U/10V_4
C436 0.1U/10V_4
C423 10U/6.3V_6S
C442 *10U/6.3V_8S
Place each 0.1uF cap close to pin

150mA
+3V
+VDDSE_CLK
L37
HCB1608KF-181T15_6
C469 4.7U/6.3V_6
C465 0.1U/10V_4
C480 0.1U/10V_4
Place each 0.1uF cap close to pin

150mA
+3V
+VDDCORE_CLK
L35
*HCB1608KF-181T15_6
+1.5V
L34
HCB1608KF-181T15_6
C425 4.7U/6.3V_6
C435 0.1U/10V_4
C481 0.1U/10V_4
C437 0.1U/10V_4
Place each 0.1uF cap close to pin

Y1
XTAL_IN
XTAL_OUT
14.318MHZ
C460 33P/50V_4
C455 33P/50V_4

+3V
R298 *10K/F_4
CPU_SEL
R300 10K/F_4

| | 0 | 1 |
|---|---|---|
| CPU_SEL | CPU0/1=133MHz (default) | CPU0/1=100MHz |

U13
9LRS3197
QFN32
+VDDSE_CLK
+VDDCORE_CLK
C482 *0.047U/10V
+VDDIO_CLK
C415 *0.047U/10V
<8,12,13> CGDAT_SMB
<8,12,13> CGCLK_SMB
+3V
<8> CLK_ICH_14M
R279 10K/F_4
R293 33_4
CPU_SEL
C477 *10P/50V_4
Place R8044 within 0.5" of C/G
CK_PWRGD_R
XTAL_OUT
XTAL_IN
VDD_LCD
VDD_REF
VDD_USB
VDD_SRC
VDD_CPU
VDD_CPU_IO
VDD_SRC_IO
SDATA
SCLK
CPU_STOP#
REF_0/CPU_SEL
CK_PWRGD/PD#_3.3
XOUT
XIN
VSS_SATA
VSS_USB
VSS_LCD
CPU-0
CPU-0#
CPU-1
CPU-1#
DOT96T_LPR
DOT96C_LPR
SRC-1
SRC-1#
SATA
SATA#
27MHz_nonSS
27MHz_SS
GND
VSS_REF
VSS_CPU
VSS_SRC
CLK_BUF_BCLK_P
CLK_BUF_BCLK_N
RP24 *4P2R-S-0
CLK_BUF_BCLK_P <8>
CLK_BUF_BCLK_N <8>
CLK_BUF_DREFCLK
CLK_BUF_DREFCLK#
RP27 *4P2R-S-0
CLK_BUF_DREFCLK <8>
CLK_BUF_DREFCLK# <8>
CLK_BUF_PCIE_3GPLL
CLK_BUF_PCIE_3GPLL#
RP25 *4P2R-S-0
CLK_BUF_PCIE_3GPLL <8>
CLK_BUF_PCIE_3GPLL# <8>
CLK_BUF_DREFSSCLK
CLK_BUF_DREFSSCLK#
RP26 *4P2R-S-0
CLK_BUF_DREFSSCLK <8>
CLK_BUF_DREFSSCLK# <8>
CLK_VGA_27M_NOSS
R304 22_4
R494 22_4
0918 SI Modify
CLK_VGA_27M_SS
R303 *33_4
EVGA-XTALI <15>
27M_TCK <15>
CLK_27M_SS <15>
Discrete only

+3V
R282 1K/F_4
CK_PWRGD_R
Q15 2N7002E
R280 100K/F_4
<34> VR_PWRGD_CLKEN#

+1.05V <7,8,9,11,13,33,34,40>
+1.5V <31,38>
+3V <3,7,8,9,10,11,12,13,15,20,21,22,23,24,25,26,27,28,29,30,31,34,38>

EMI request
+3V
C812 .1U/10V_4
C813 .1U/10V_4
C814 .1U/10V_4
C815 .1U/10V_4
+1.05V
C816 .1U/10V_4
C817 .1U/10V_4
C818 .1U/10V_4
C819 .1U/10V_4
C820 .1U/10V_4
C821 .1U/10V_4

CPU
H6 H4 H3 H11
*H-TC248BC197D150P2

GPU
H10 H9
*H-TC248BC197D150P2
H0 H1 H2 H5 H7 H8
*H-c354d118p2
*H-c236d118p2
*H-c276d118p2

H12 H13 H16 H17 H18
*H-c354d118p2
*H-c354d354n
*H-TSBC394D118P2
*H-TSBC276D118P2
*H-O-AX1-1

PAD0 PAD1 PAD2 PAD3 PAD4 PAD5 PAD6 PAD7 PAD8

PROJECT :AX1
Quanta Computer Inc.
Size: Custom
Document Number: Clock Gen(9LRS3197)/HOLES
Rev: 1A
Date: Thursday, November 12, 2009
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| | DIS | UMA |
|---|---|---|
| Ra | NA | 0 ohm |
| Rb | 0 ohm | NA |
| Rc | 0 ohm | NA |

U16A

DMI

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

2.7GT/s data rate

IC,AUB_CFD_rPGA,R1P0

U16B

MISC

THERMAL

CLOCKS

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

IC,AUB_CFD_rPGA,R1P0

for S3 power reduction

SI modify

Discrete Only

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND ( Check list 1.0 ).

SI modify

Use a voltage divider with VDDQ (1.5 V) rail ON in S3) and resistor combination of 1.5K ±1% (to VDDQ)/750±1% (to GND) to convert to processor VTT level.

JTAG MAPPING

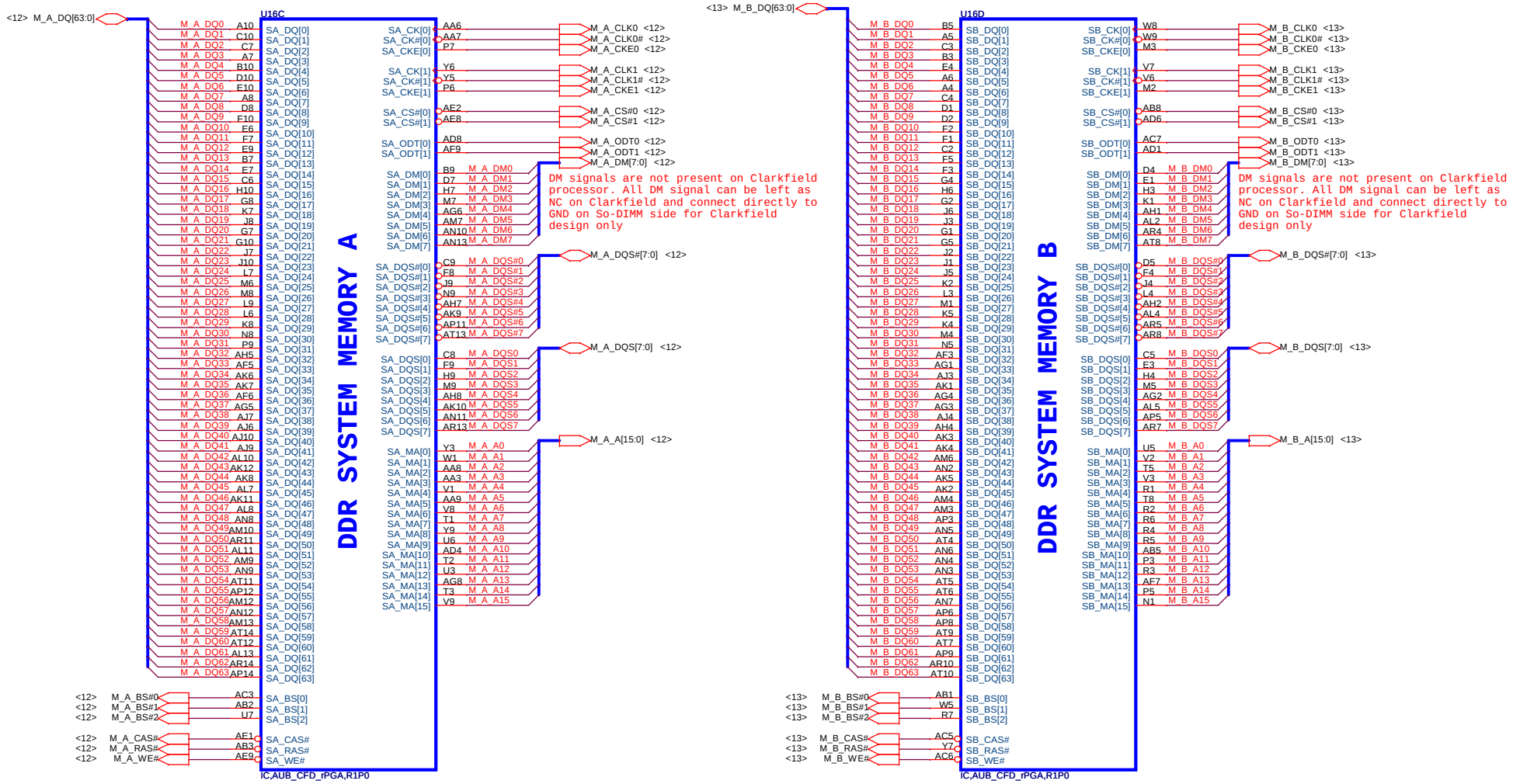
| Scan Chain (Default) | STUFF -> Ra, Rc, Re<br>NO STUFF -> Rb, Rd |
|---|---|
| CPU Only | STUFF -> Ra, Rb<br>NO STUFF -> Rc, Rd, Re |
| GMCH Only | STUFF -> Rd, Re<br>NO STUFF -> Ra, Rb, Rc |

**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PROCESSER 1/4(HOST&PEX) | 2A |

Date: Monday, November 30, 2009 | Sheet 3 of 40

# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)




**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PROCESSER 2/4(DDR) | 1A |

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18A

| | DIS | UMA |
|---|---|---|
| Rc | NA | 4.7K |
| Rd | NA | 0 ohm |
| Re | NA | 0 ohm |
| Rf | NA | NA |

| | DIS | UMA |
|---|---|---|
| Ra | 0 ohm | NA |

UMA only

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

2A

for S3 power reduction

SI modify

for S3 power reduction

SI modify

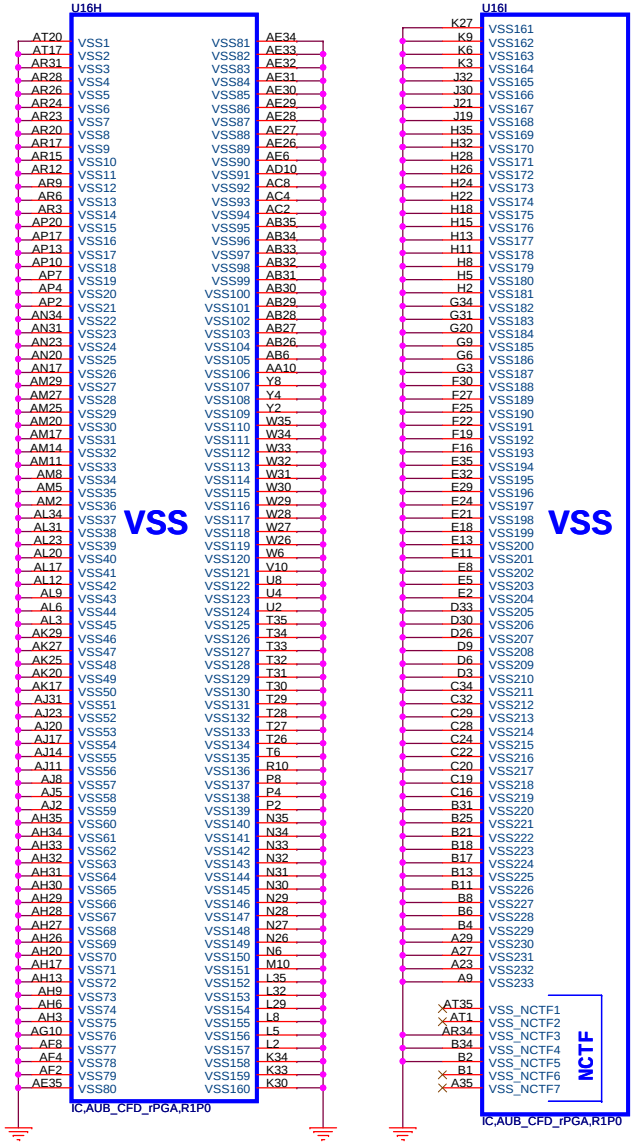
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

**PROJECT :AX1**
Quanta Computer Inc.

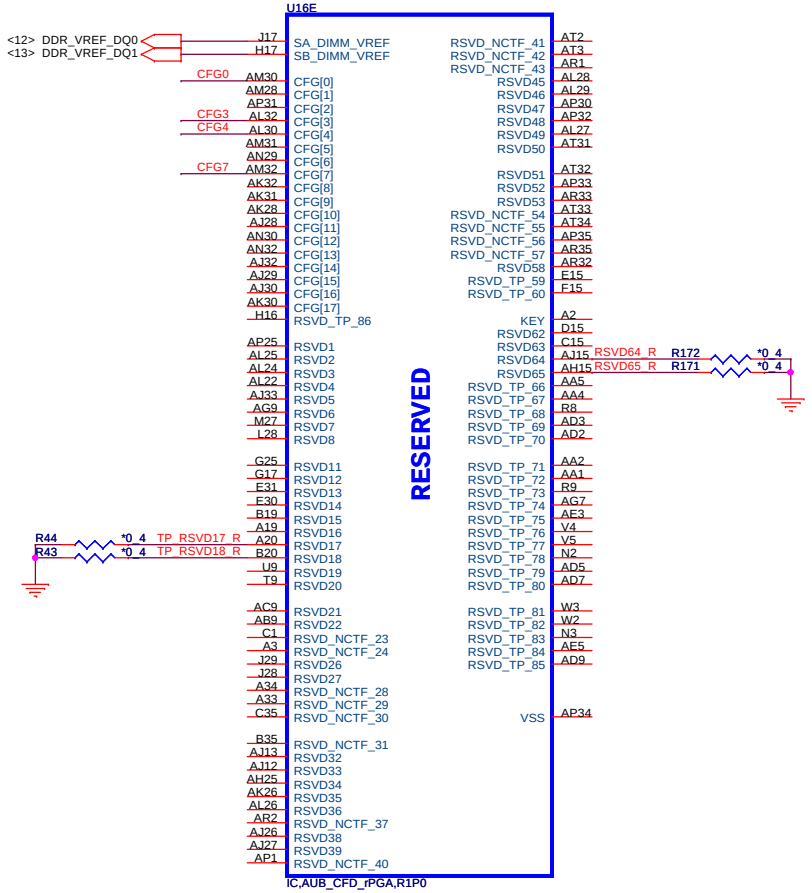
| Size | Document Number | Rev |
|---|---|---|
| Custom | PROCESSER 3/4(POWER) | 1A |

Date: Thursday, December 03, 2009 | Sheet 5 of 40

# AUBURNDALE/CLARKSFIELD PROCESSOR (GND)




# AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)





CFG[ 1:0 ] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

| | 1 | 0 |
|---|---|---|
| CFG4 (Display Port Presence) | Disabled; No Physical Display Port attached to Embedded Diplay Port | Enabled; An external Display port device is connected to the Embedded Display port |
| CFG0 (PCI-Epress Configuration Select) | Single PEG | Bifurcation enabled |
| CFG3 (PCI-Epress Static Lane Reversal) | Normal Operation | Lane Numbers Reversed 15 -> 0 , 14 -> 1 |

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

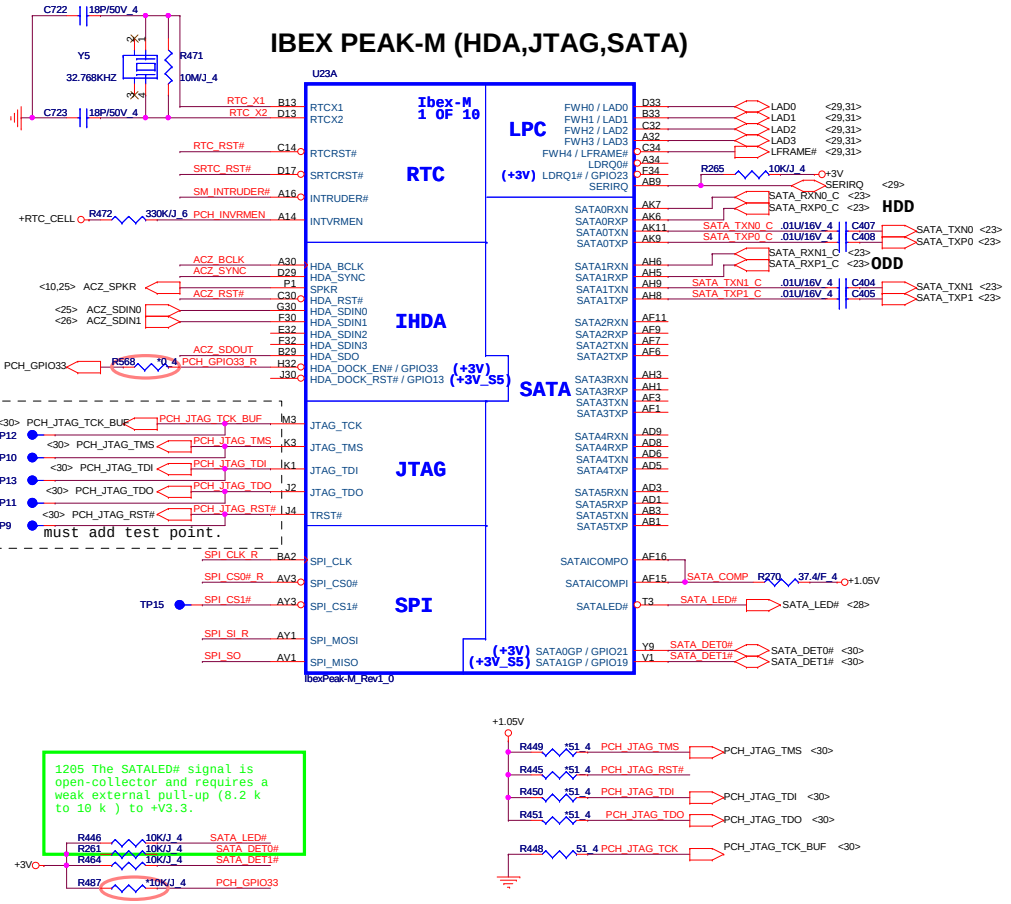
**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PROCESSER 4/4 (GND) | 1A |

Date: Thursday, November 12, 2009 | Sheet 6 of 40

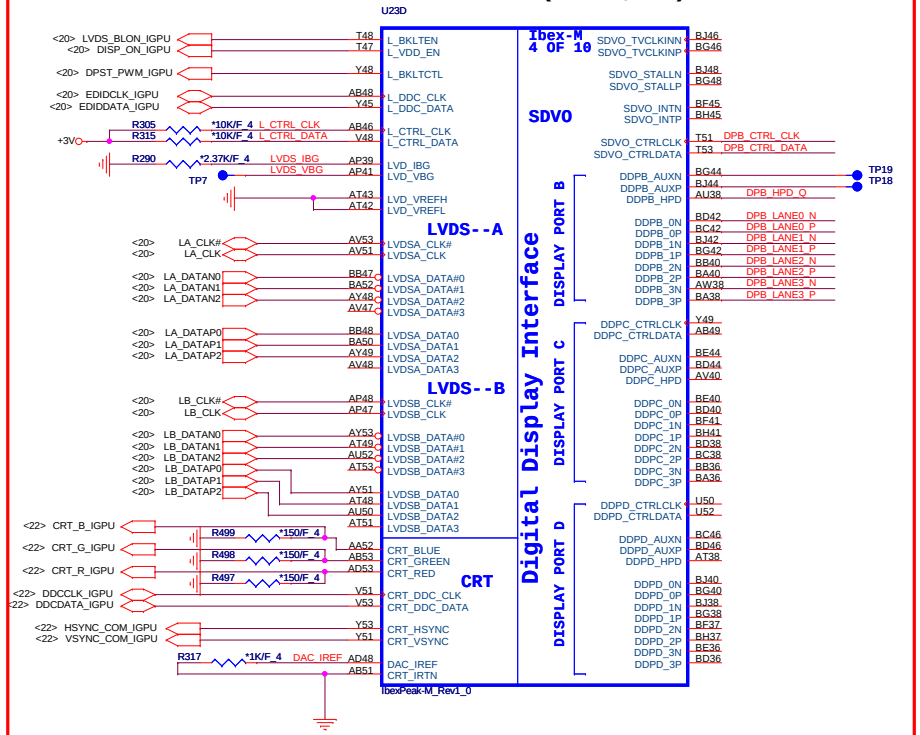
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

# IBEX PEAK-M (HDA,JTAG,SATA)

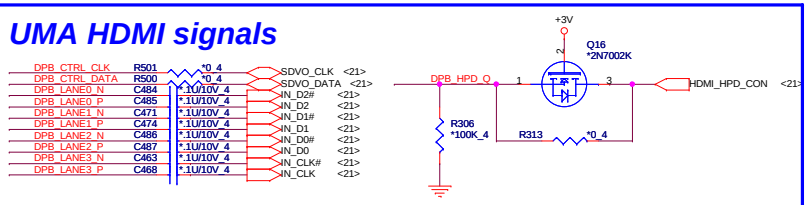



# UMA CRT,LVDS&HDMI signals

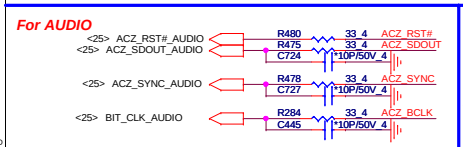
## IBEX PEAK-M (LVDS,DDI)



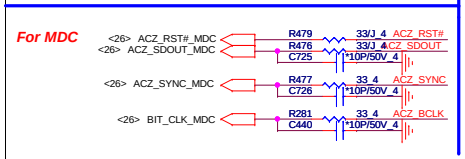

# UMA HDMI signals




## For AUDIO

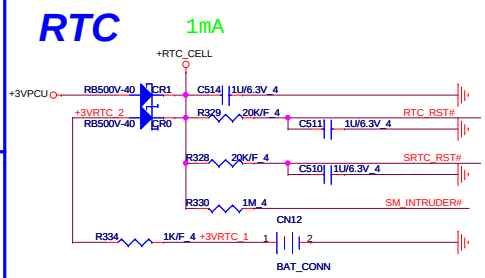


## For MDC

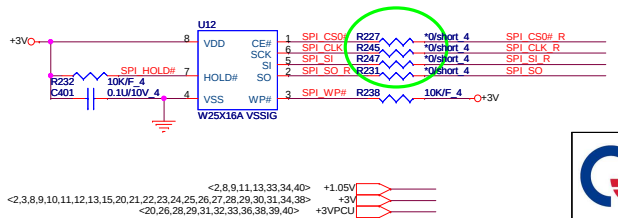


# RTC

1mA




# 4M byte SPI ROM




| Vendor | PN |
|---|---|
| Socket | DG008000031 |
| WINBOND | AKE39ZP0N00 |
| MAX | AKE39FP0N00 |

**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 1/5 (SATA,HDA,LPC) | 1A |

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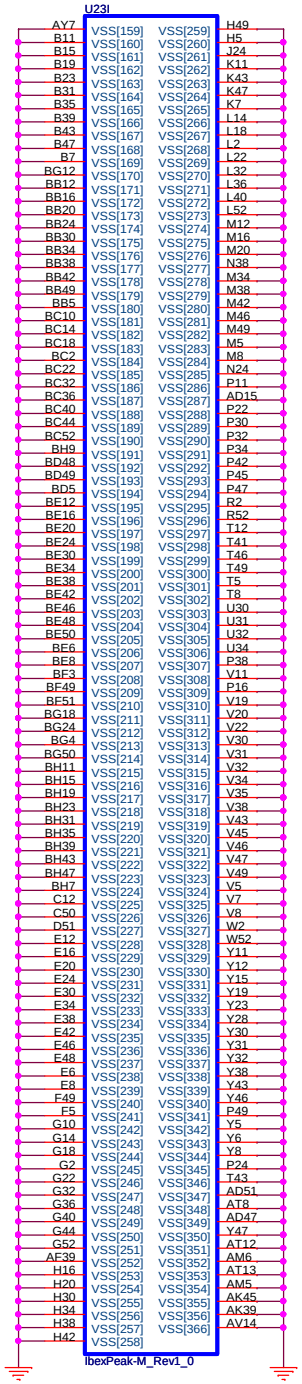
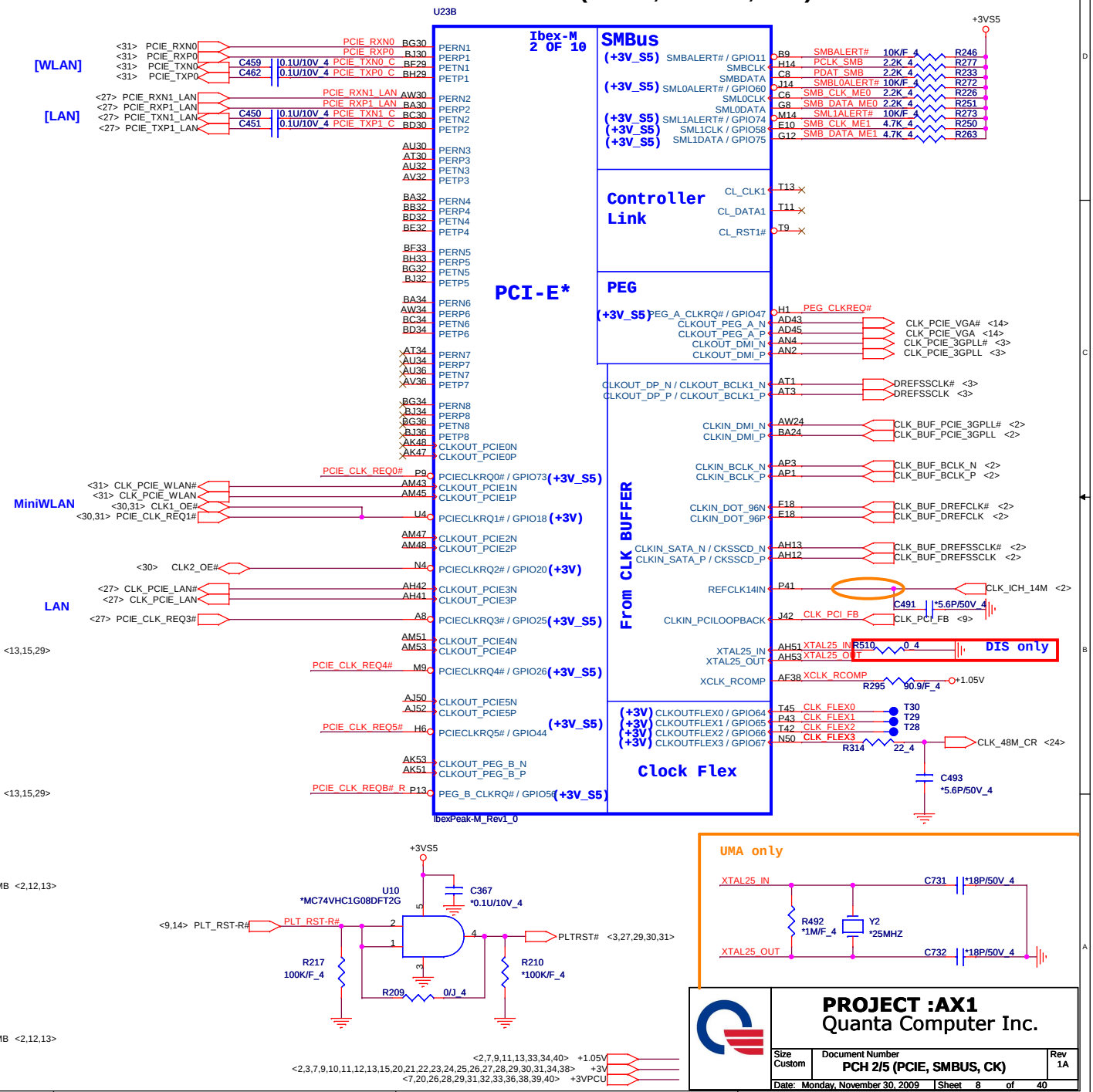
# IBEX PEAK-M (GND)

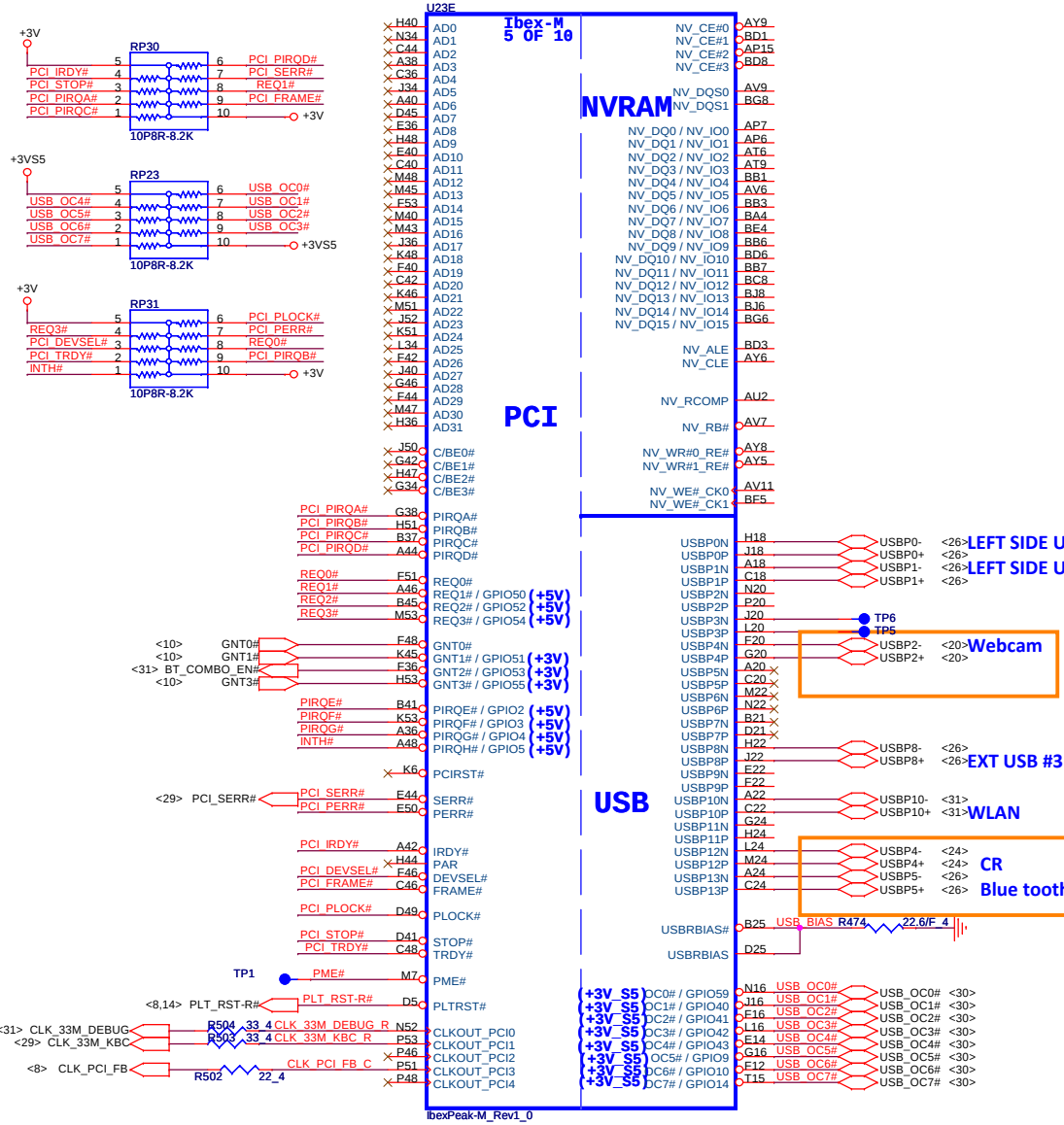



# IBEX PEAK-M (PCI-E,SMBUS,CLK)




08

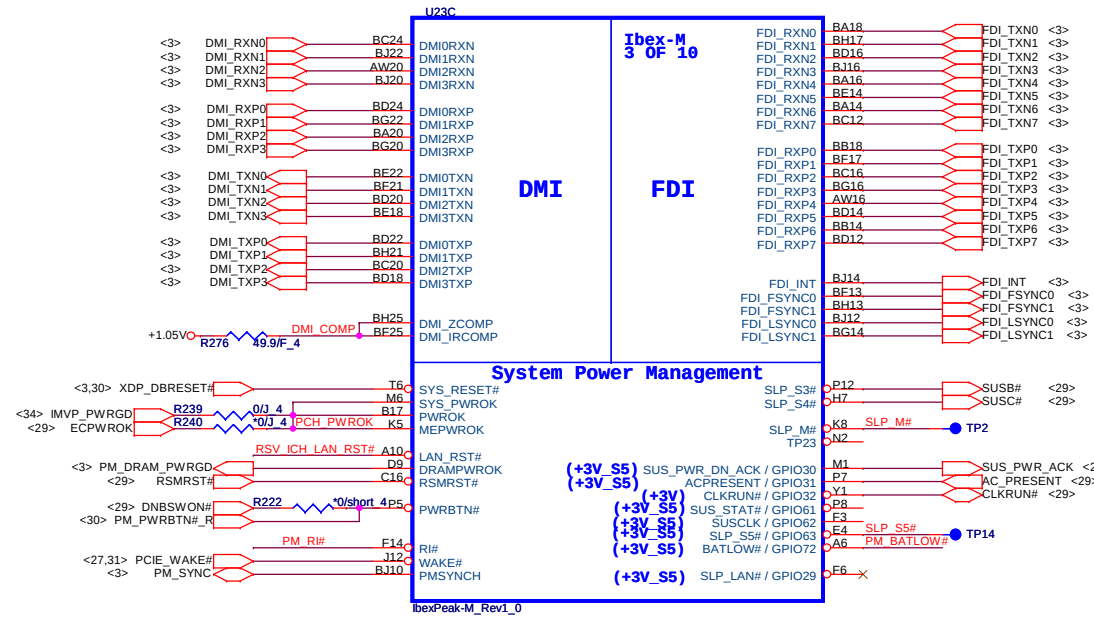
# IBEX PEAK-M (PCI,USB,NVRAM)

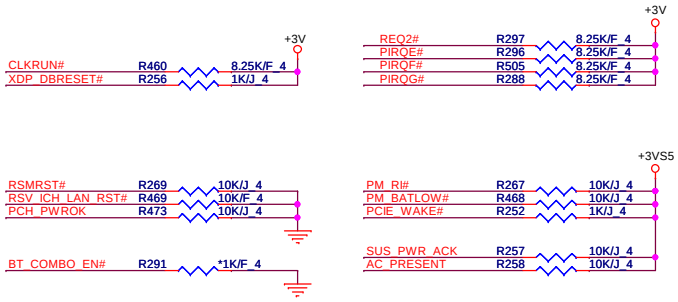



SI Modify

Change Port2 to Port4
Change Port4 to Port12
change Port5 to Port13

# IBEX PEAK-M (DMI,FDI,GPIO)



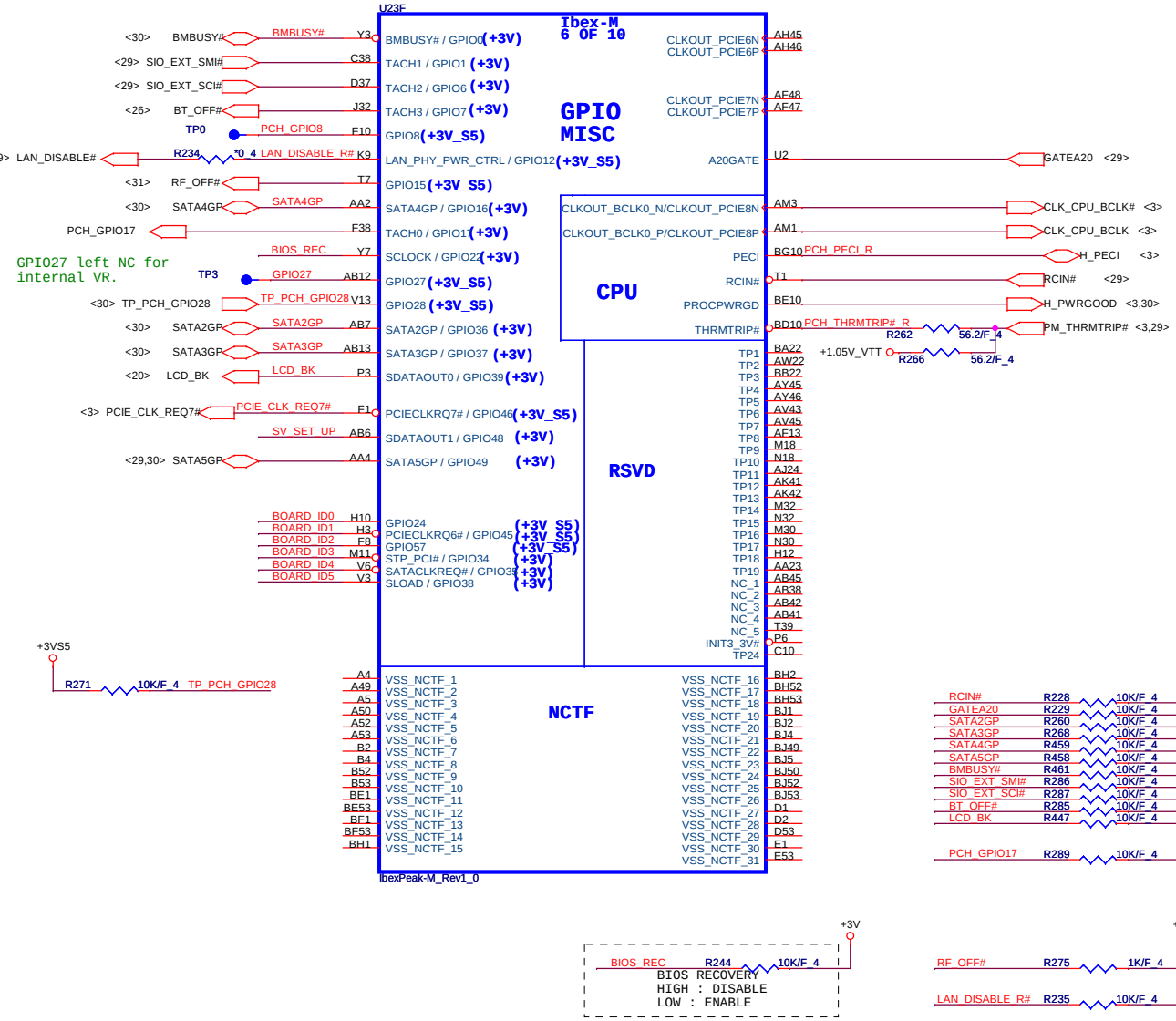




<2,7,8,11,13,33,34,40> +1.05V
<2,3,7,8,10,11,12,13,15,20,21,22,23,24,25,26,27,28,29,30,31,34,38> +3V
<3,8,10,11,30,38> +3VS5

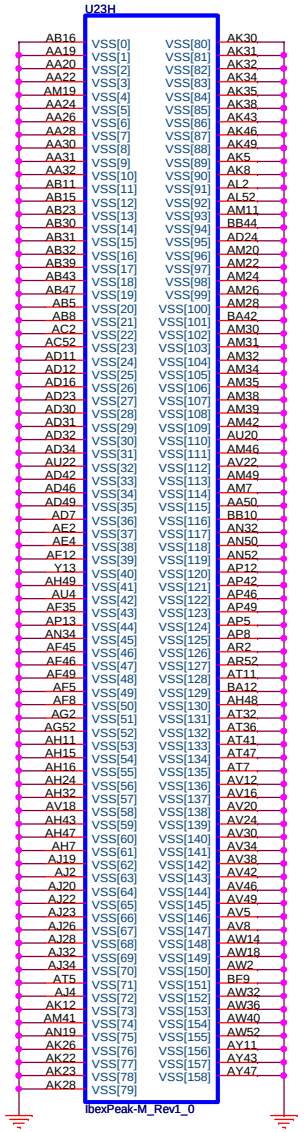
**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 3/5 (PCI,ONFI,USB,DMI) | 1A |
| Date: Monday, November 30, 2009 | Sheet 9 of 40 | |

# IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)




# IBEX PEAK-M (GND)




10

<9> GNT3# R507 *10K_NC

| A16 swap override Strap/Top-Block Swap Override jumper | |
|---|---|
| GNT3# | Low = A16 swap override/Top-Block Swap Override enabled<br>High = Default |

SV_SET_UP R259 10K/F_4 +3V

| | |
|---|---|
| SV_SET_UP | 1-X High = Strong (Default) |

<9> GNT0# GNT0# R302 *1K/F_4
<9> GNT1# GNT1# R506 *1K/F_4

| Boot BIOS Strap | | |
|---|---|---|
| PCI_GNT0# | GNT#1 | Boot BIOS Location |
| 0 | 0 | LPC |
| 0 | 1 | Reserved (NAND) |
| 1 | 0 | PCI |
| 1 | 1 | SPI |

| Danbury Technology Enabled | |
|---|---|
| NV_ALE | High = Enable<br>Low = Disable |

| DMI Termination Voltage | |
|---|---|
| NV_CLE | Set to Vcc when LOW<br>Set to Vcc/2 when HIGH |

**No Reboot Strap**

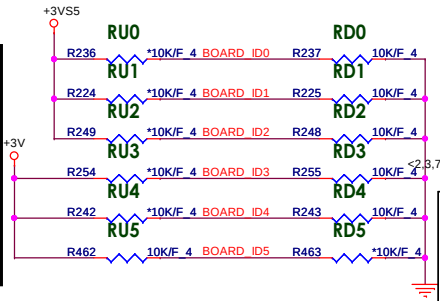
<7,25> ACZ_SPKR *1K/F_4 R466 +3V
<7,29> PCH_GPIO33 R283 *100K/F_4

<3,5,11,29,30,34,35,40> +1.05V_VTT
<5,11,33,38> +1.8V
<2,3,7,8,9,11,12,13,15,20,21,22,23,24,25,26,27,28,29,30,31,34,38> +3V
<3,8,9,11,30,38> +3VS5

## BOARD ID SETTING

**Board ID5: For idenify UMA and DIS**
**Board ID4: For idenify FF and DF**
**Board ID3: Reserve**
**Board ID2: Reserve**
**Board ID1: Reserve**

| Board ID | ID0 | ID1 | ID2 | ID3 | ID4 | ID5 |
|---|---|---|---|---|---|---|
| UMA FF | 0 | 0 | 0 | 0 | 0 | 0 |
| UMA DF | 0 | 0 | 0 | 0 | 1 | 0 |
| DIS | 0 | 0 | 0 | 0 | 0 | 1 |
| | | | | | | |



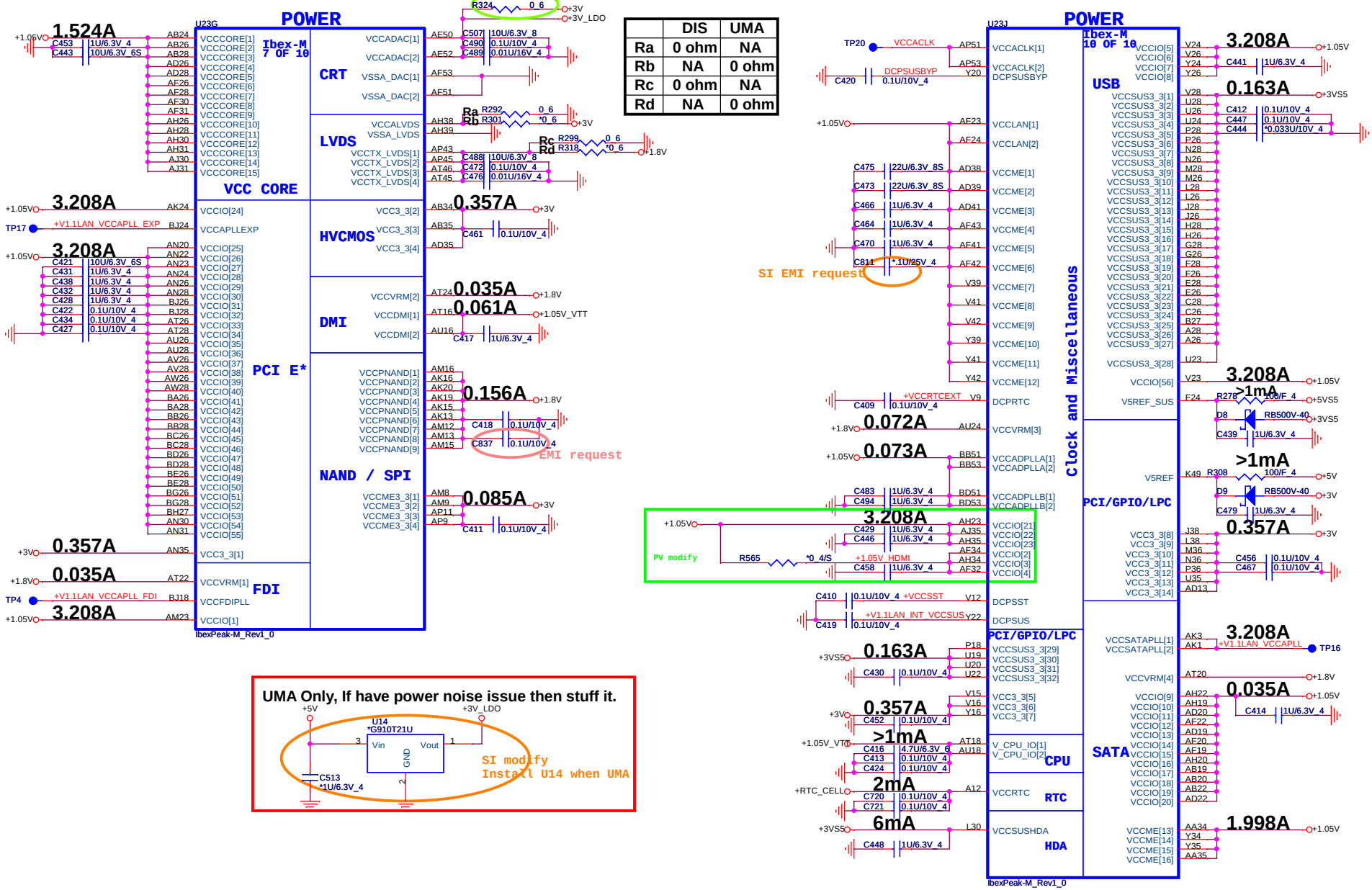


**PROJECT :AX1**
Quanta Computer Inc.


| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 4/5 (GPIO & Strap) | 1A |
| Date: Thursday, November 12, 2009 | Sheet 10 of 40 | |

SI modify
Uninstall on UMA
Install on DIS

| | DIS | UMA |
|---|---|---|
| Ra | 0 ohm | NA |
| Rb | NA | 0 ohm |
| Rc | 0 ohm | NA |
| Rd | NA | 0 ohm |




UMA Only, If have power noise issue then stuff it.



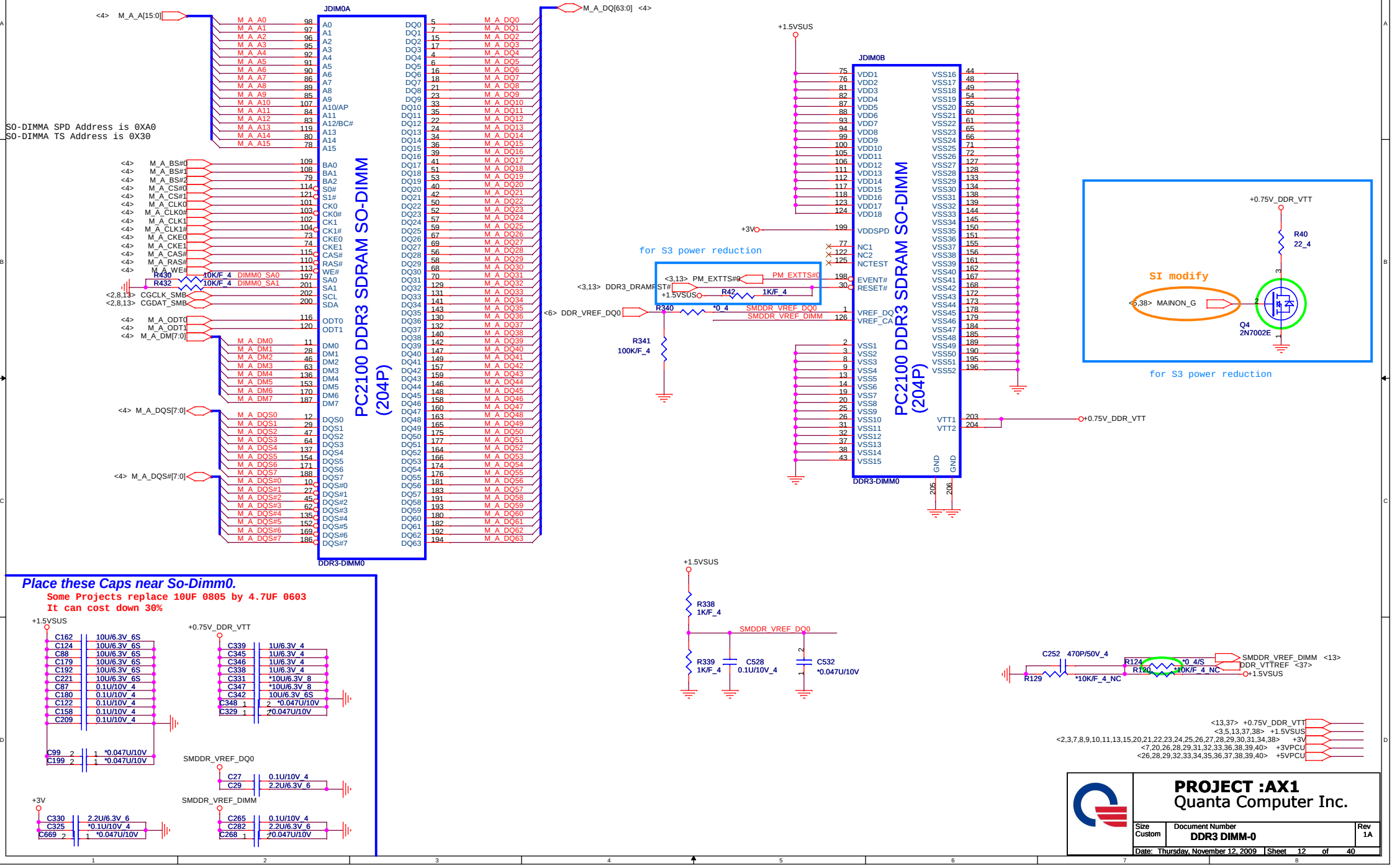

<2,7,8,9,13,33,34,40> +1.05V
<3,5,10,29,30,34,35,40> +1.05V_VTT
<5,33,38> +1.8V
<2,3,7,8,9,10,12,13,15,20,21,22,23,24,25,26,27,28,29,30,31,34,38> +3V
<3,8,9,10,30,38> +3VS5
<20,21,22,23,25,28,31,38> +5V
<32,38> +5VS5

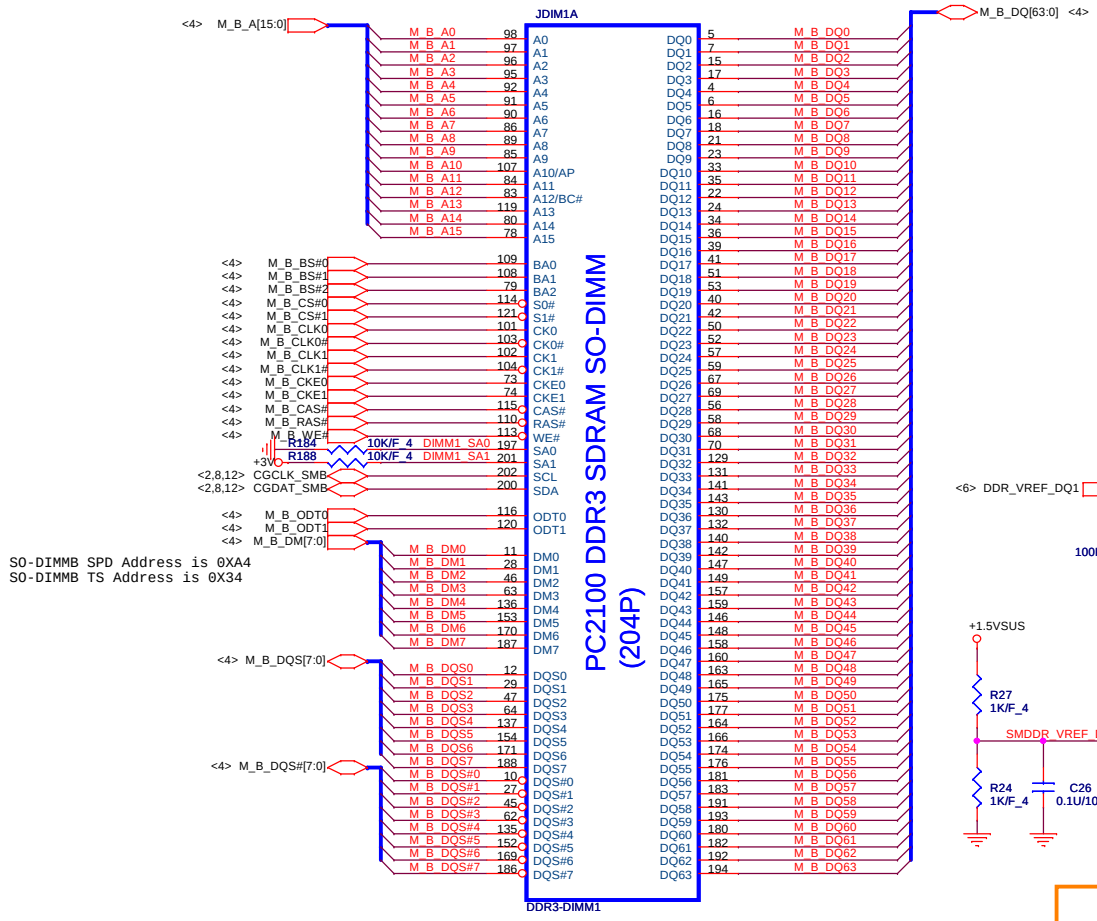
**PROJECT :AX1**
Quanta Computer Inc.

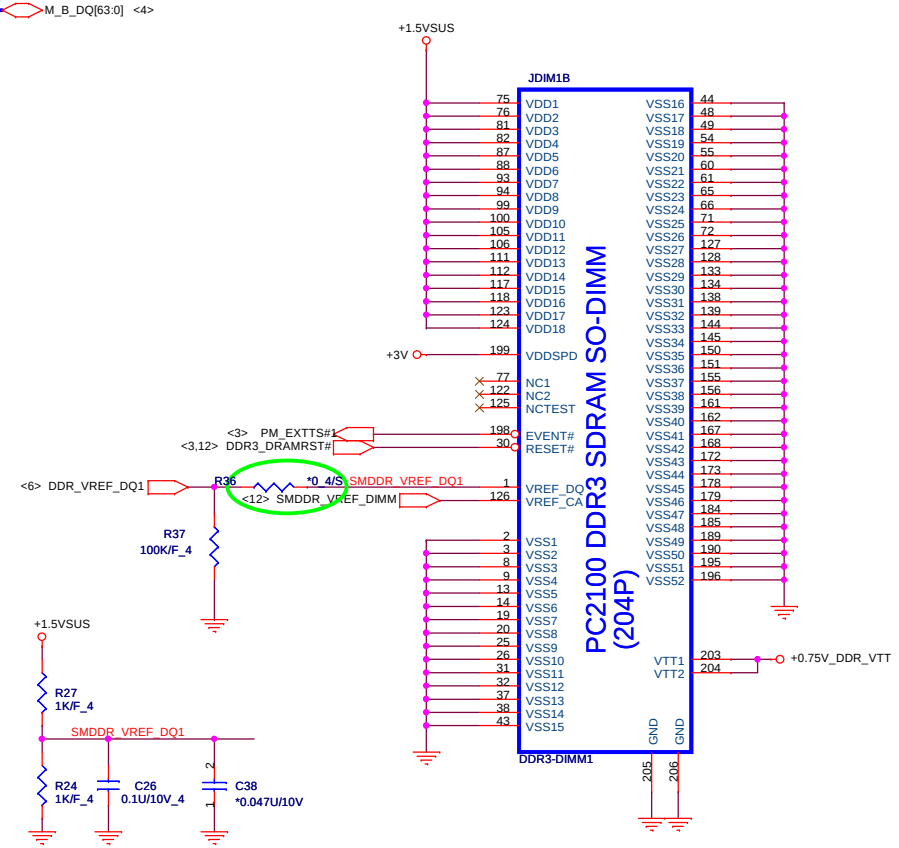
| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 5/5 (POWER) | 1A |

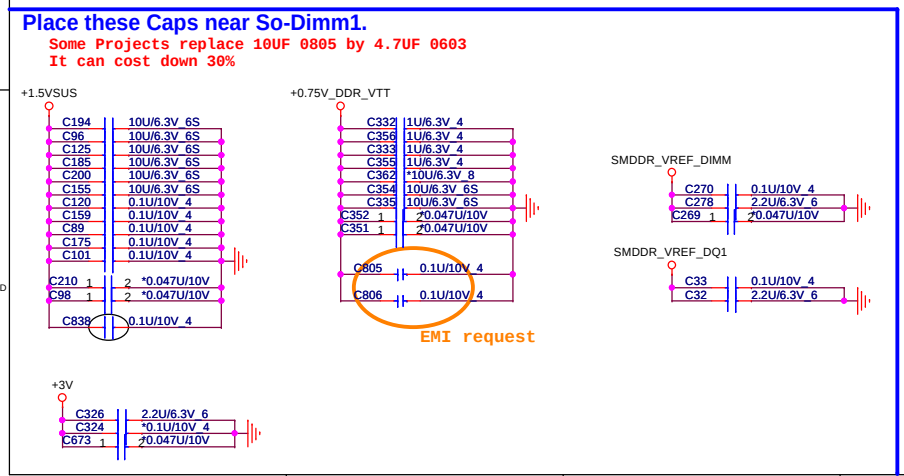
Date: Thursday, November 12, 2009 | Sheet 11 of 40

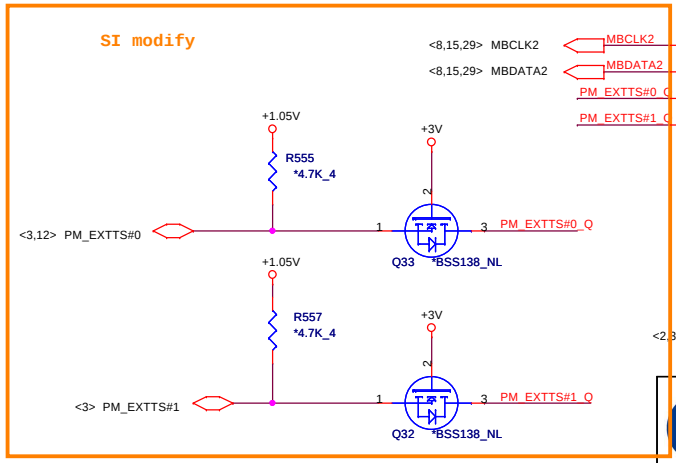
SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30








**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | DDR3 DIMM-1 | 1A |

Date: Thursday, December 03, 2009 | Sheet 13 of 40

POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=0.9~1.2V

2.5GT/s bit rate

U17A

PCI EXPRESS INTERFACE

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| <3> PEG_TX15 | PEG_TX15 | AF30 | PCIE_RX0P | PCIE_TX0P | AH30 | C_PEG_RXP15 C123 | 0.1U/10V_4 |
| <3> PEG_TX#15 | PEG_TX#15 | AE31 | PCIE_RX0N | PCIE_TX0N | AG31 | C_PEG_RXN15 C136 | 0.1U/10V_4 |
| <3> PEG_TX14 | PEG_TX14 | AE29 | PCIE_RX1P | PCIE_TX1P | AG29 | C_PEG_RXP14 C151 | 0.1U/10V_4 |
| <3> PEG_TX#14 | PEG_TX#14 | AD28 | PCIE_RX1N | PCIE_TX1N | AF28 | C_PEG_RXN14 C160 | 0.1U/10V_4 |
| <3> PEG_TX13 | PEG_TX13 | AD30 | PCIE_RX2P | PCIE_TX2P | AF27 | C_PEG_RXP13 C139 | 0.1U/10V_4 |
| <3> PEG_TX#13 | PEG_TX#13 | AC31 | PCIE_RX2N | PCIE_TX2N | AF26 | C_PEG_RXN13 C149 | 0.1U/10V_4 |
| <3> PEG_TX12 | PEG_TX12 | AC29 | PCIE_RX3P | PCIE_TX3P | AD27 | C_PEG_RXP12 C163 | 0.1U/10V_4 |
| <3> PEG_TX#12 | PEG_TX#12 | AB28 | PCIE_RX3N | PCIE_TX3N | AD26 | C_PEG_RXN12 C166 | 0.1U/10V_4 |
| <3> PEG_TX11 | PEG_TX11 | AB30 | PCIE_RX4P | PCIE_TX4P | AC25 | C_PEG_RXP11 C168 | 0.1U/10V_4 |
| <3> PEG_TX#11 | PEG_TX#11 | AA31 | PCIE_RX4N | PCIE_TX4N | AC24 | C_PEG_RXN11 C174 | 0.1U/10V_4 |
| <3> PEG_TX10 | PEG_TX10 | AA29 | PCIE_RX5P | PCIE_TX5P | Y23 | C_PEG_RXP10 C190 | 0.1U/10V_4 |
| <3> PEG_TX#10 | PEG_TX#10 | Y28 | PCIE_RX5N | PCIE_TX5N | Y24 | C_PEG_RXN10 C183 | 0.1U/10V_4 |
| <3> PEG_TX9 | PEG_TX9 | Y30 | PCIE_RX6P | PCIE_TX6P | AB27 | C_PEG_RXP9 C181 | 0.1U/10V_4 |
| <3> PEG_TX#9 | PEG_TX#9 | W31 | PCIE_RX6N | PCIE_TX6N | AB26 | C_PEG_RXN9 C176 | 0.1U/10V_4 |
| <3> PEG_TX8 | PEG_TX8 | W29 | PCIE_RX7P | PCIE_TX7P | W27 | C_PEG_RXP8 C205 | 0.1U/10V_4 |
| <3> PEG_TX#8 | PEG_TX#8 | V28 | PCIE_RX7N | PCIE_TX7N | W26 | C_PEG_RXN8 C193 | 0.1U/10V_4 |
| <3> PEG_TX7 | PEG_TX7 | V30 | PCIE_RX8P | PCIE_TX8P | V25 | C_PEG_RXP7 C208 | 0.1U/10V_4 |
| <3> PEG_TX#7 | PEG_TX#7 | U31 | PCIE_RX8N | PCIE_TX8N | V24 | C_PEG_RXN7 C214 | 0.1U/10V_4 |
| <3> PEG_TX6 | PEG_TX6 | U29 | PCIE_RX9P | PCIE_TX9P | V27 | C_PEG_RXP6 C228 | 0.1U/10V_4 |
| <3> PEG_TX#6 | PEG_TX#6 | T28 | PCIE_RX9N | PCIE_TX9N | U26 | C_PEG_RXN6 C218 | 0.1U/10V_4 |
| <3> PEG_TX5 | PEG_TX5 | T30 | PCIE_RX10P | PCIE_TX10P | U25 | C_PEG_RXP5 C229 | 0.1U/10V_4 |
| <3> PEG_TX#5 | PEG_TX#5 | R31 | PCIE_RX10N | PCIE_TX10N | U24 | C_PEG_RXN5 C241 | 0.1U/10V_4 |
| <3> PEG_TX4 | PEG_TX4 | R29 | PCIE_RX11P | PCIE_TX11P | T25 | C_PEG_RXP4 C243 | 0.1U/10V_4 |
| <3> PEG_TX#4 | PEG_TX#4 | P28 | PCIE_RX11N | PCIE_TX11N | T27 | C_PEG_RXN4 C250 | 0.1U/10V_4 |
| <3> PEG_TX3 | PEG_TX3 | P30 | PCIE_RX12P | PCIE_TX12P | R26 | C_PEG_RXP3 C262 | 0.1U/10V_4 |
| <3> PEG_TX#3 | PEG_TX#3 | N31 | PCIE_RX12N | PCIE_TX12N | R24 | C_PEG_RXN3 C253 | 0.1U/10V_4 |
| <3> PEG_TX2 | PEG_TX2 | N29 | PCIE_RX13P | PCIE_TX13P | P27 | C_PEG_RXP2 C266 | 0.1U/10V_4 |
| <3> PEG_TX#2 | PEG_TX#2 | M28 | PCIE_RX13N | PCIE_TX13N | P26 | C_PEG_RXN2 C279 | 0.1U/10V_4 |
| <3> PEG_TX1 | PEG_TX1 | M30 | PCIE_RX14P | PCIE_TX14P | P24 | C_PEG_RXP1 C283 | 0.1U/10V_4 |
| <3> PEG_TX#1 | PEG_TX#1 | L31 | PCIE_RX14N | PCIE_TX14N | P23 | C_PEG_RXN1 C286 | 0.1U/10V_4 |
| <3> PEG_TX0 | PEG_TX0 | L29 | PCIE_RX15P | PCIE_TX15P | M27 | C_PEG_RXP0 C295 | 0.1U/10V_4 |
| <3> PEG_TX#0 | PEG_TX#0 | K30 | PCIE_RX15N | PCIE_TX15N | N26 | C_PEG_RXN0 C289 | 0.1U/10V_4 |

| | | | |
|---|---|---|---|
| PEG_RX15 <3> | PEG_RX#15 <3> |
| PEG_RX14 <3> | PEG_RX#14 <3> |
| PEG_RX13 <3> | PEG_RX#13 <3> |
| PEG_RX12 <3> | PEG_RX#12 <3> |
| PEG_RX11 <3> | PEG_RX#11 <3> |
| PEG_RX10 <3> | PEG_RX#10 <3> |
| PEG_RX9 <3> | PEG_RX#9 <3> |
| PEG_RX8 <3> | PEG_RX#8 <3> |
| PEG_RX7 <3> | PEG_RX#7 <3> |
| PEG_RX6 <3> | PEG_RX#6 <3> |
| PEG_RX5 <3> | PEG_RX#5 <3> |
| PEG_RX4 <3> | PEG_RX#4 <3> |
| PEG_RX3 <3> | PEG_RX#3 <3> |
| PEG_RX2 <3> | PEG_RX#2 <3> |
| PEG_RX1 <3> | PEG_RX#1 <3> |
| PEG_RX0 <3> | PEG_RX#0 <3> |

CLOCK

| | | | |
|---|---|---|---|
| <8> CLK_PCIE_VGA | AK30 | PCIE_REFCLKP | |
| <8> CLK_PCIE_VGA# | AK32 | PCIE_REFCLKN | |

M93-S3--NC
PARK-S3--install
10K/F_4 R149 N10 NC_PWRGOOD

<8,9> PLT_RST-R# AL27 PERSTB

CALIBRATION

PCIE_CALRP Y22 M72_PCIE_CALRP R83 1.27K/F_4
PCIE_CALRN AA22 M72_PCIE_CALRN R82 2K/F_4 +1.1V_VGA

PARK

100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing

U17G

DP E/F POWER

| | | |
|---|---|---|
| +1.8V_DPE_VDD18 | AG15 AG16 | DPE_VDD18#1 DPE_VDD18#2 |
| +1.1V_DPE_VDD10 | AG20 AG21 | DPE_VDD10#1 DPE_VDD10#2 |
| | AG14 AH14 AM14 AM16 AM18 | DPE_VSSR#1 DPE_VSSR#2 DPE_VSSR#3 DPE_VSSR#4 DPE_VSSR#5 |
| +1.8V_DPE_VDD18 | AF16 AG17 | DPF_VDD18#1 DPF_VDD18#2 |
| +1.1V_DPE_VDD10 | AF22 AG22 | DPF_VDD10#1 DPF_VDD10#2 |
| | AF23 AG23 AM20 AM22 AM24 | DPF_VSSR#1 DPF_VSSR#2 DPF_VSSR#3 DPF_VSSR#4 DPF_VSSR#5 |
| R110 150/F_4 DPEF_CALR | AF17 | DPEF_CALR |
| +1.8V_DPE_PVDD | AG18 AF19 | DPE_PVDD DPE_PVSS |
| +1.8V_DPF_PVDD R108 *0_4/S | AG19 AF20 | NC_DPF_PVDD NC_DPF_PVSS |

M93-S3--NC
PARK-S3--install

DP A/B POWER

| | | |
|---|---|---|
| AE11 AF11 | +1.8V_DPA_VDD18 | NC_DPA_VDD18#1 NC_DPA_VDD18#2 |
| AF6 AF7 | +1.1V_DPB_VDD10 | DPA_VDD10#1 DPA_VDD10#2 |
| AE1 AE3 AG1 AG6 AH5 | | DPA_VSSR#1 DPA_VSSR#2 DPA_VSSR#3 DPA_VSSR#4 DPA_VSSR#5 |
| AE13 AF13 | +1.8V_DPA_VDD18 | NC_DPB_VDD18#1 NC_DPB_VDD18#2 |
| AF8 AF9 | +1.1V_DPB_VDD10 | DPB_VDD10#1 DPB_VDD10#2 |
| AF10 AG9 AH8 AM6 AM8 | | DPB_VSSR#1 DPB_VSSR#2 DPB_VSSR#3 DPB_VSSR#4 DPB_VSSR#5 |
| AE10 DPAB_CALR R88 150/F_4 | | DPAB_CALR |
| AG8 AG7 | +1.8V_DPA_PVDD | DPA_PVDD DPA_PVSS |
| AG10 AG11 | +1.8V_DPA_PVDD | DPB_PVDD DPB_PVSS |

DP PLL POWER

PARK

BLM18PG181SN1D(180,1.5A)_6
L46 +1.1V_DPB_VDD10 +1.1V_VGA 1.1V(S100,D200mA)
C632 0.1U/10V_4 C634 10U/6.3V_6S C633 1U/10V_4

(Park-S3:110mA@1.0V)
(M9X-S2/S3:200mA@1.1V)

+1.1V_DPE_VDD10 +1.1V_DPE_VDD10 L20 +1.1V_VGA
C137 0.1U/10V_4 C127 1U/10V_4 C107 10U/6.3V_6S
BLM18PG181SN1D(180,1.5A)_6

1.8V -(300mA)
+1.8V_DPE_VDD18 L21 +1.8V_VGA
C140 0.1U/10V_4 C128 1U/10V_4 C135 10U/6.3V_6S
BLM18PG181SN1D(180,1.5A)_6

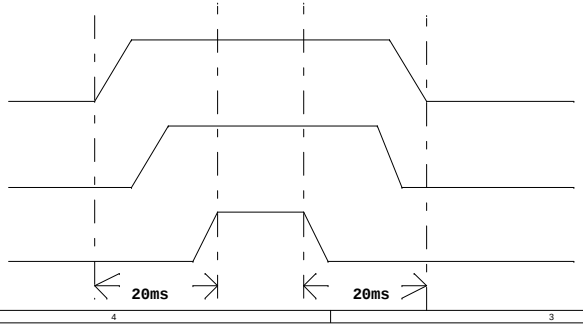
+1.8V_DPF_PVDD +1.8V_DPF_PVDD L43 1.8V(20mA) +1.8V_VGA
C606 0.1U/10V_4 C608 1U/10V_4 C596 10U/6.3V_6S
BLM18PG181SN1D(180,1.5A)_6
Reserve for PARK

Reserve for PARK
+1.8V_DPA_VDD18 +1.8V_DPA_VDD18 L18 1.8V(130mA) +1.8V_VGA
C100 0.1U/10V_4 C119 1U/10V_4 C97 10U/6.3V_6S
BLM18PG181SN1D(180,1.5A)_6

+1.8V_DPA_PVDD +1.8V_DPA_PVDD L47 1.8V(20mA) +1.8V_VGA
C629 0.1U/10V_4 C628 1U/10V_4 C626 10U/6.3V_6S
BLM18PG181SN1D(180,1.5A)_6

+1.8V_DPE_PVDD +1.8V_DPE_PVDD L16 1.8V(20mA) +1.8V_VGA
C85 0.1U/10V_4 C83 1U/10V_4 C79 10U/6.3V_6S
BLM18PG181SN1D(180,1.5A)_6

| | |
|---|---|
| VGA Core | BPP |
| VGA Core | VDDC |
| +1.8V | PCIE_VDDR |
| +1.8V | PCIE_PVDD |
| +1.8V | VDDR1 |
| +3V_VGA | VDDR3 |




**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | M93_PCIE_Interface | 1A |

Date: Thursday, November 12, 2009 Sheet 14 of 40

| MEM_ID[3:0] | Vendor | Type | Vendor P/N |
|---|---|---|---|
| 0000 | Samsung (E die) | 64*16-800MHZ | K4W1G1646E-HC12 |
| 0001 | Hynix | 64*16 -800MHZ | H5TQ1G63BFR-12C |

| | PWRCNTL1 | PWRCNTL0 | V-CORE |
|---|---|---|---|
| L | 0 | 0 | 0.9V |
| M | 0 | 1 | 0.95V |
| H | 1 | 0 | 1.05V |
| TBD | 1 | 1 | NA |

U17B

M93-S3/M92-S2

Memory ID

DVO

DPA

DPB

DPC

I2C

GENERAL PURPOSE I/O

DAC1

DAC2

PLL/CLOCK

DDC/AUX

THERMAL

Reserve for PARK

For M93-S3: Use 150 Ohms Pull Down
For M92-S2: Use 0R to VDDR4
For Park-S3: NC

GPIO22(ROMCS#)
PD without external VBIOS ROM

0916: AMD modify

Need check again

1.8V(120mADPLL_PVDD)

1.1V(300mA DPLL_VDDC)

1.8V(20mA TSVDD)

CL=20PF

For Int Clk 27Mhz

Thermal Sensor

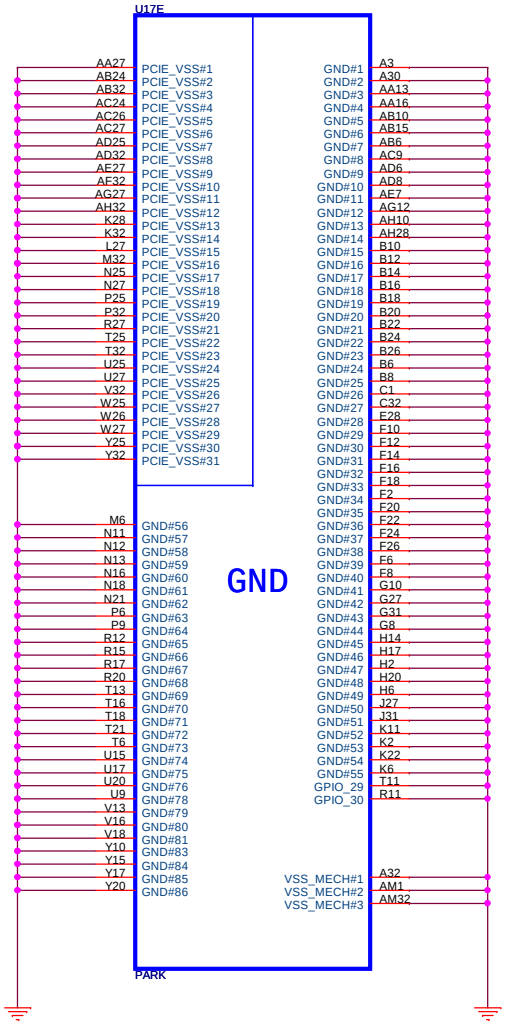
I2C ADDRESS: 9AH

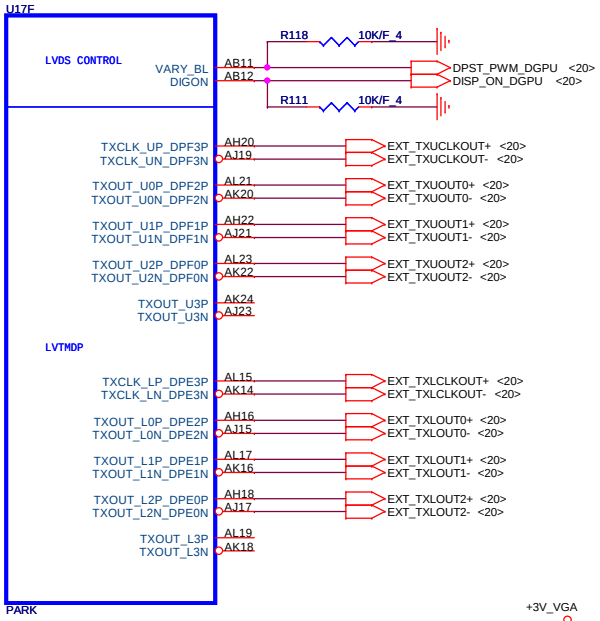
PROJECT :AX1
Quanta Computer Inc.

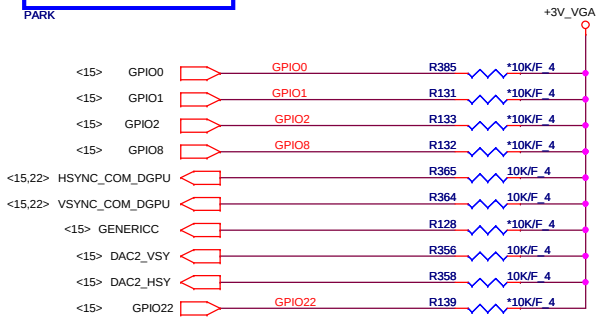
| Size | Document Number | Rev |
|---|---|---|
| Custom | M93_MAIN | 1A |

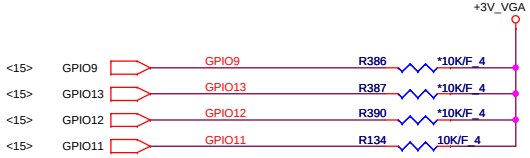
Date: Thursday, November 12, 2009 | Sheet 15 of 40

w/s 10 / 10




## CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

| STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS | |
|---|---|---|---|
| TX_PWRS_ENB | GPIO0 | **Transmitter Power Savings Enable**<br>0: 50% Tx output swing for mobile mode<br>1: full Tx output swing (Default setting for Desktop) | 1 |
| TX_DEEMPH_EN | GPIO1 | **PCI Express Transmitter De-emphasis Enable**<br>0: Tx de-emphasis disabled for mobile mode<br>1: Tx de-emphasis enabled (Default setting for Desktop) | 1 |
| BIF_GEN2_EN_A | GPIO2 | Enable CLKREQ# Power Management<br>0 - CLKREQ# power management capability is disabled<br>1 - CLKREQ# power management capability is enabled | 0 |
| RSVD<br>BIF_VGA_DIS<br>RSVD | GPIO8<br>GPIO9<br>GPIO21 | VGA ENABLED | 0<br>0<br>0 |
| BIOS_ROM_EN<br><br>ROMIDCFG(2:0)<br><br>VIP_DEVICE_STRAP_ENA | GPIO_22_ROMCSB<br><br>GPIO[13:11]<br><br>V2SYNC | ENABLE EXTERNAL BIOS ROM<br><br>SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT<br><br>IGNORE VIP DEVICE STRAPS | 0<br><br>0 0 1<br><br>0 |
| RSVD<br>AUD[1]<br>AUD[0] | GENERICC<br>HSYNC<br>VSYNC | AUD[1] AUD[0]<br>0 0 No audio function<br>0 1 Audio for DisplayPort and HDMI if dongle is detected<br>1 0 Audio for DisplayPort only<br>1 1 Audio for both DisplayPort and HDMI | 0<br>0<br>11 |

## AMD RESERVED CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

H2SYNC GENERICC

**PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

GPIO21_BB_EN

## Memory Aperture size

| GPIO9<br>BIOSROM | | GPIO13<br>ROMIDCFG2 | GPIO12<br>ROMIDCFG1 | GPIO11<br>ROMIDCFG0 |
|---|---|---|---|---|
| 0 | 128M | 0 | 0 | 0 |
| 0 | 256M | 0 | 0 | 1 |
| 0 | 64M | 0 | 1 | 0 |
| 0 | 32M | 0 | 1 | 1 |
| 0 | 512M | 1 | 0 | 0 |
| 0 | 1G | 1 | 0 | 1 |
| 0 | 2G | 1 | 1 | 0 |
| 0 | 4G | 1 | 1 | 1 |

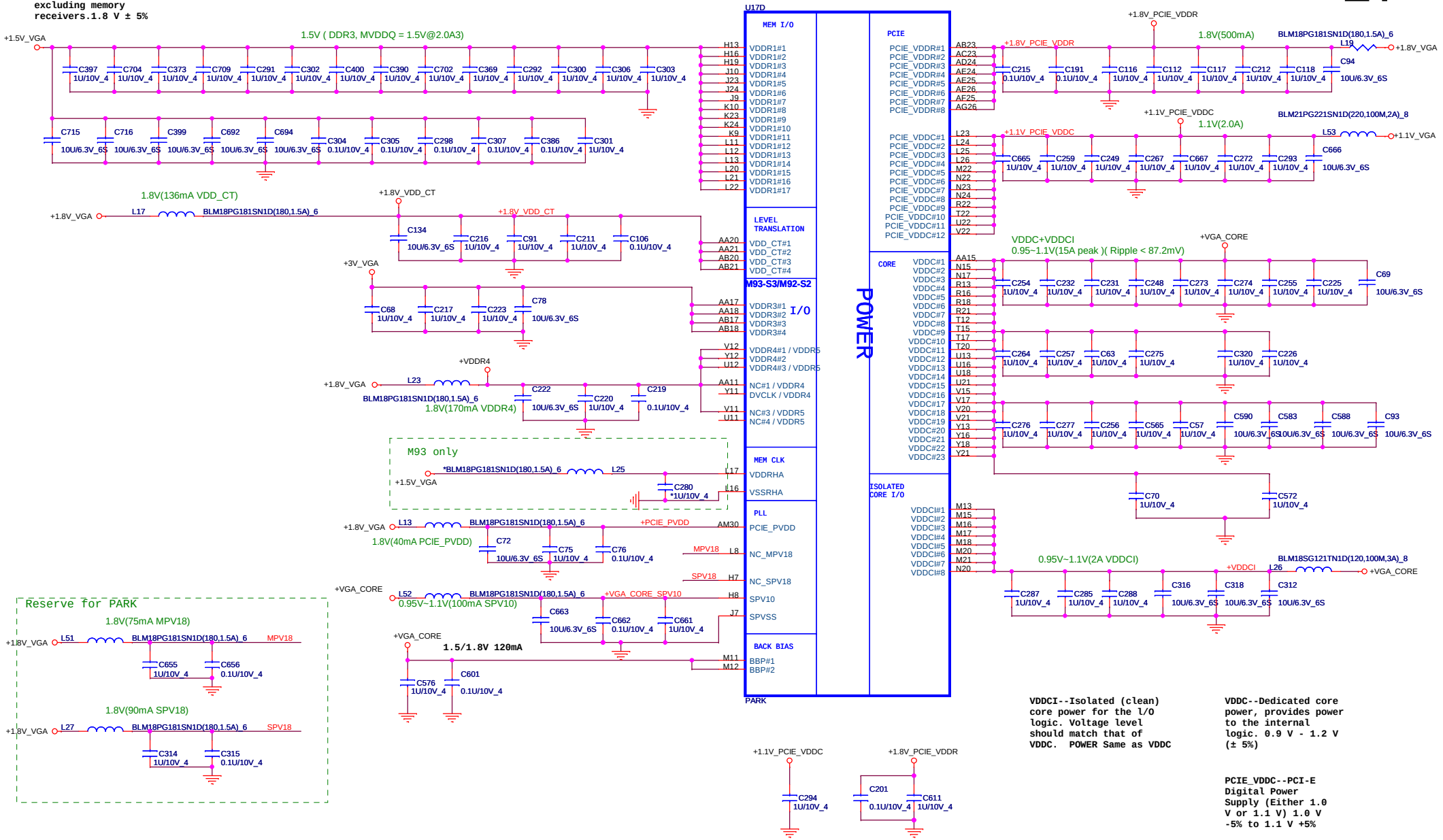
**It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.**

**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | M93_GND / LVDS /Straps | 1A |
| Date: Thursday, November 12, 2009 | Sheet 16 of 40 | |

VDD_CT -- Level translation between core and I/O, excluding memory receivers.1.8 V ± 5%

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%




VDDCI--Isolated (clean) core power for the l/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

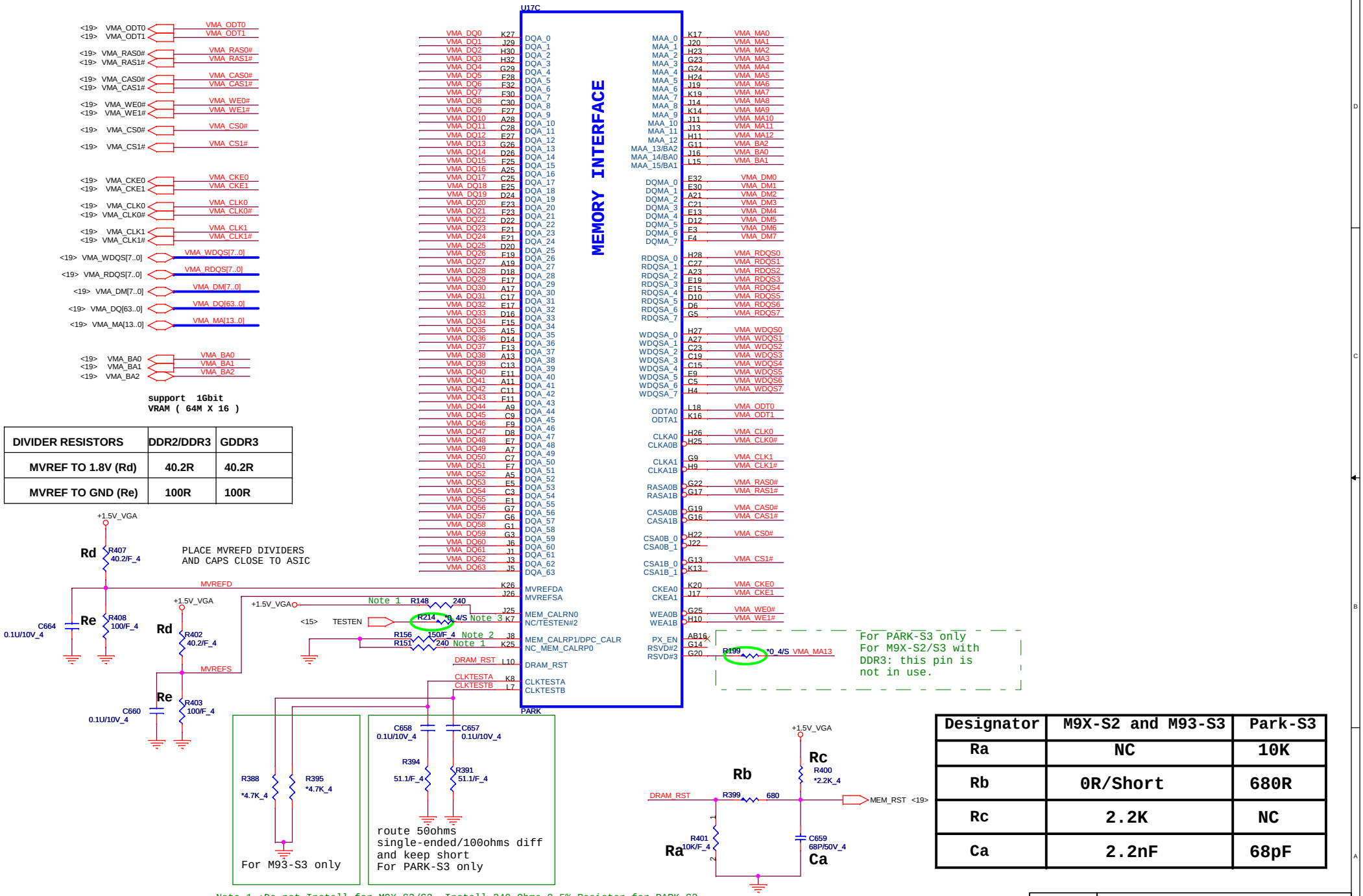
VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%

**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | M93_Power_and_NC | 1A |

Date: Tuesday, November 10, 2009 | Sheet 17 of 40


U17C
MEMORY INTERFACE
DQA_0
DQA_1
DQA_2
DQA_3
DQA_4
DQA_5
DQA_6
DQA_7
DQA_8
DQA_9
DQA_10
DQA_11
DQA_12
DQA_13
DQA_14
DQA_15
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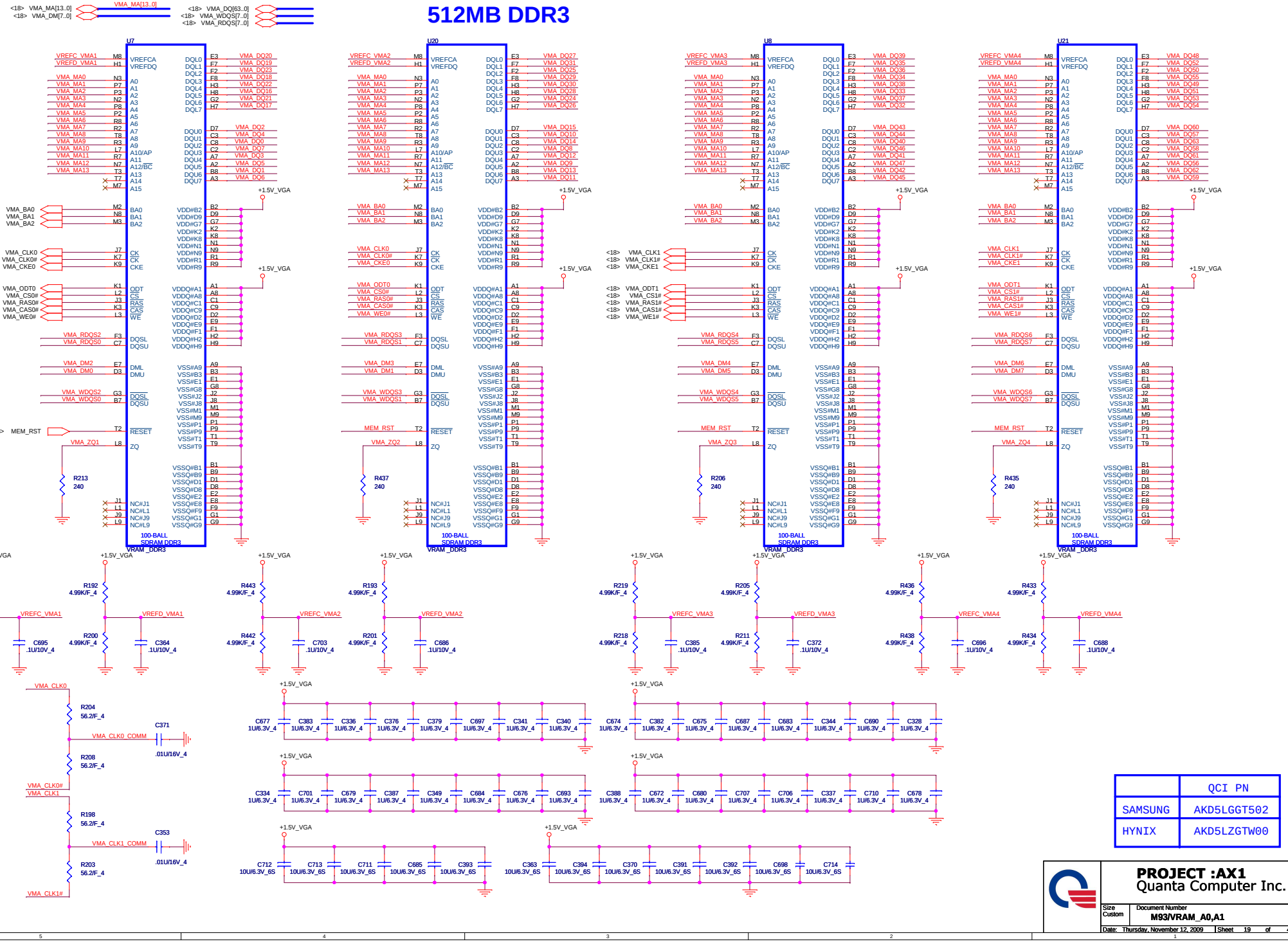
DQA_60
DQA_61
DQA_62
DQA_63
MVREFDA
MVREFSA
MEM_CALRN0
NC/TESTEN#2
MEM_CALRP1/DPC_CALR
NC_MEM_CALRP0
DRAM_RST
CLKTESTA
CLKTESTB
PARK
MAA_0
MAA_1
MAA_2
MAA_3
MAA_4
MAA_5
MAA_6
MAA_7
MAA_8
MAA_9
MAA_10
MAA_11
MAA_12
MAA_13/BA2
MAA_14/BA0
MAA_15/BA1
DQMA_0
DQMA_1
DQMA_2
DQMA_3
DQMA_4
DQMA_5
DQMA_6
DQMA_7
RDQSA_0
RDQSA_1
RDQSA_2
RDQSA_3
RDQSA_4
RDQSA_5
RDQSA_6
RDQSA_7
WDQSA_0
WDQSA_1
WDQSA_2
WDQSA_3
WDQSA_4
WDQSA_5
WDQSA_6
WDQSA_7
ODTA0
ODTA1
CLKA0
CLKA0B
CLKA1
CLKA1B
RASA0B
RASA1B
CASA0B
CASA1B
CSA0B_0
CSA0B_1
CSA1B_0
CSA1B_1
CKEA0
CKEA1
WEA0B
WEA1B
PX_EN
RSVD#2
RSVD#3
VMA_ODT0
VMA_ODT1
VMA_RAS0#
VMA_RAS1#
VMA_CAS0#
VMA_CAS1#
VMA_WE0#
VMA_WE1#
VMA_CS0#
VMA_CS1#
VMA_CKE0
VMA_CKE1
VMA_CLK0
VMA_CLK0#
VMA_CLK1
VMA_CLK1#
VMA_WDQS[7..0]
VMA_RDQS[7..0]
VMA_DM[7..0]
VMA_DQ[63..0]
VMA_MA[13..0]
VMA_BA0
VMA_BA1
VMA_BA2
support 1Gbit
VRAM ( 64M X 16 )
DIVIDER RESISTORS
DDR2/DDR3
GDDR3
MVREF TO 1.8V (Rd)
40.2R
40.2R
MVREF TO GND (Re)
100R
100R
+1.5V_VGA
Rd
R407
40.2/F_4
PLACE MVREFD DIVIDERS
AND CAPS CLOSE TO ASIC
MVREFD
Re
R408
100/F_4
C664
0.1U/10V_4
Rd
R402
40.2/F_4
MVREFS
Re
R403
100/F_4
C660
0.1U/10V_4
Note 1
R148
240
R214
*0_4/S
Note 3
TESTEN
R156
150/F_4
Note 2
R151
240
Note 1
DRAM_RST
CLKTESTA
CLKTESTB
R388
*4.7K_4
R395
*4.7K_4
For M93-S3 only
C658
0.1U/10V_4
C657
0.1U/10V_4
R394
51.1/F_4
R391
51.1/F_4
route 50ohms
single-ended/100ohms diff
and keep short
For PARK-S3 only
R199
*0_4/S
VMA_MA13
For PARK-S3 only
For M9X-S2/S3 with
DDR3: this pin is
not in use.
Rb
Rc
R400
*2.2K_4
DRAM_RST
R399
680
MEM_RST
Ra
R401
10K/F_4
C659
68P/50V_4
Ca
Designator
M9X-S2 and M93-S3
Park-S3
Ra
NC
10K
Rb
0R/Short
680R
Rc
2.2K
NC
Ca
2.2nF
68pF
Note 1 :Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24
PROJECT :AX1
Quanta Computer Inc.
Size
Custom
Document Number
M93_MEM_Interface
Rev
1A
Date: Thursday, November 12, 2009
Sheet 18 of 40

# 512MB DDR3



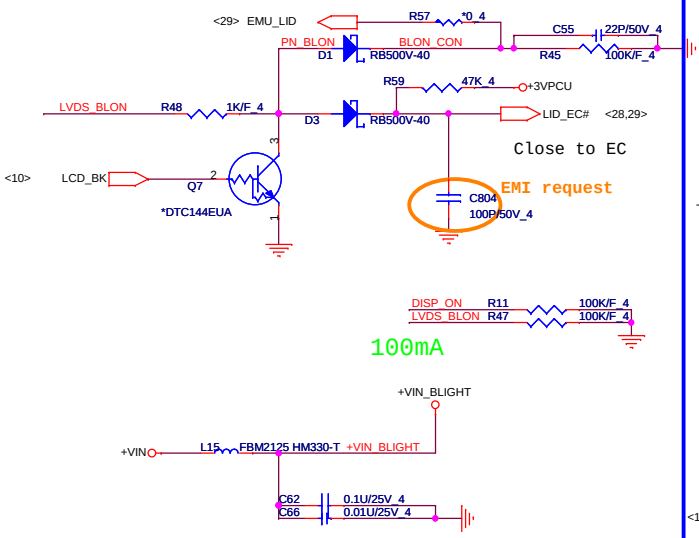

| | QCI PN |
|---|---|
| SAMSUNG | AKD5LGGT502 |
| HYNIX | AKD5LZGTW00 |

**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | M93/VRAM_A0,A1 | 1A |

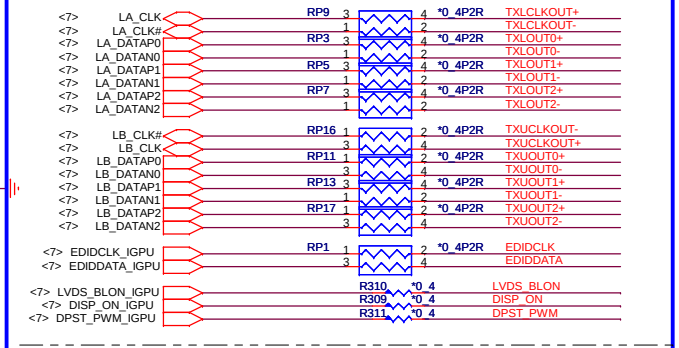
Date: Thursday, November 12, 2009 | Sheet 19 of 40

# LID Switch

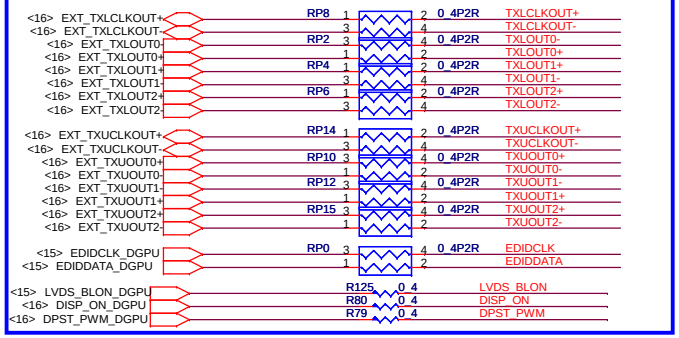



**1. If LCD connector near GPU, then place these series Resistors near GPU**
**2. If LCD connector near PCH, then place these series Resistors near PCH**

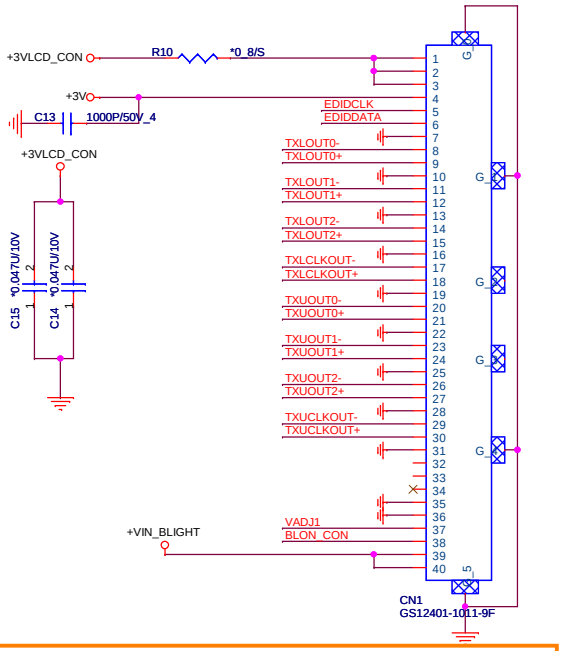
OPTION SIGNAL FROM PCH FOR UMA VGA

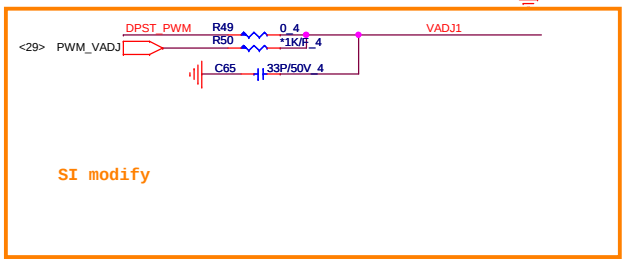



OPTION SIGNAL FROM ATI M93 to VGA

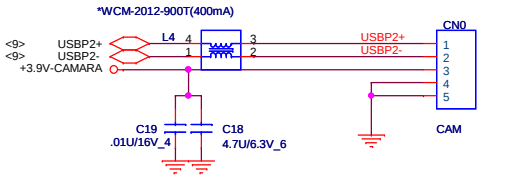


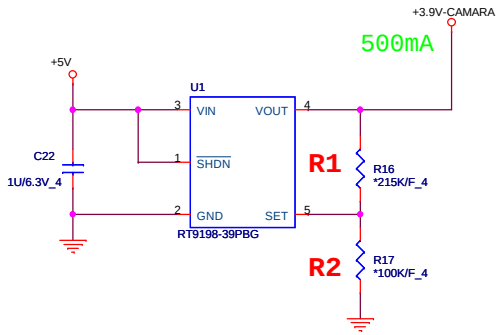


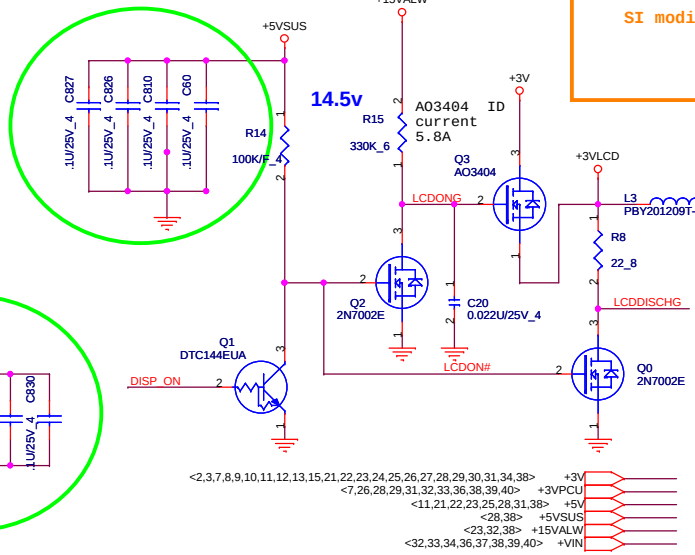



# CAMERA






**PROJECT :AX1**
Quanta Computer Inc.

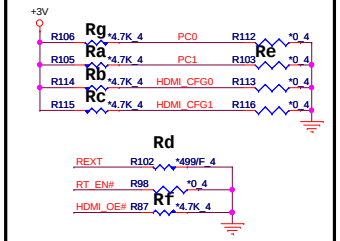
| Size | Document Number | Rev |
|---|---|---|
| Custom | LCD CONN/LID/CAM | 1A |
| Date: Thursday, November 12, 2009 | Sheet 20 of 40 | |

| Signals | | PDT | CHR | PIM |
|---|---|---|---|---|
| PC1 | Ra | NC | NC | NC |
| HDMI_CFG0 | Rb | NC | NC | NC |
| HDMI_CFG1 | Rc | 4.7K | NC | NC |
| REXT | Rd | 499 | 1.2K | 4.7K |
| PC1 | Re | NC | 4.7K | 4.7K |
| HDMI_OE# | Rf | NC | 4.7K | NC |
| PC0 | Rg | 4.7K | 4.7K | 4.7K |

9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella

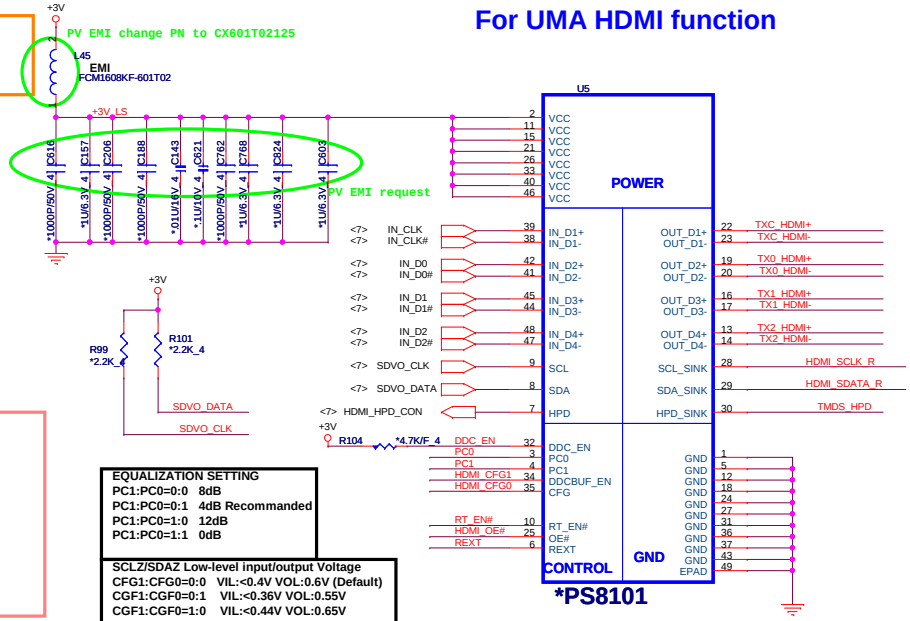
CHR : need Na R1182, add R1027 for capella

Vendor:PDT P/N:AL008101000
Vendor:CHR P/N:AL007318002
Vendor:PIM P/N:ALP411LS004




PV2 modify, close to U5

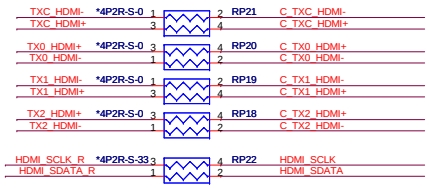

## For UMA HDMI function




**EQUALIZATION SETTING**
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

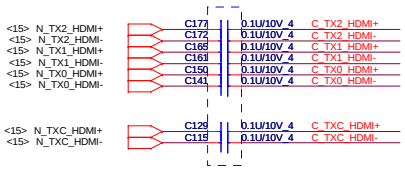
**SCLZ/SDAZ Low-level input/output Voltage**
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

**FOR UMA ONLY**
**FROM LEVEL SHIFTER**

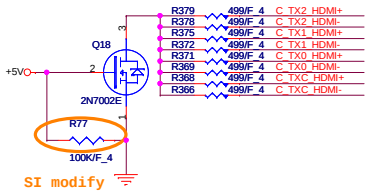



**FOR DISCRETE ONLY**
**FROM M93/PARK**

**PLACE CLOSE HDMI CONN**



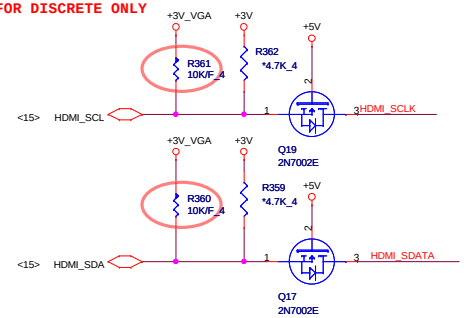

**FOR DISCRETE ONLY**



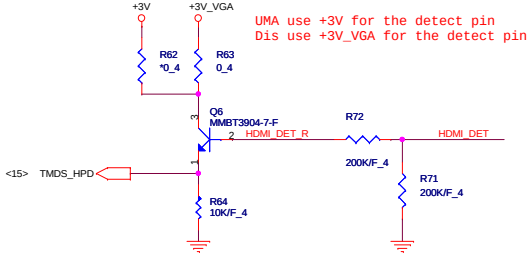

SI modify

## DISCRETE HDMI I2C SELECT
## Close to HDMI Connector

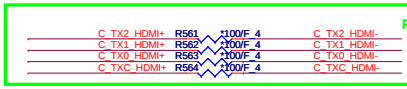
**FOR DISCRETE ONLY**

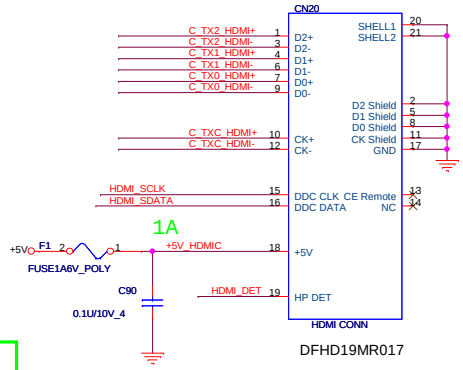



## UMA & DISCRETEHDMI HPD SENSE

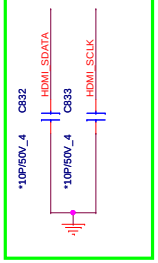


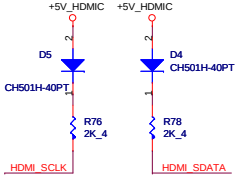

PV EMI request




reserved for EMI




**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | HDMI CONN | 1A |

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# CRT PORT

1A

FUSE1A6V_POLY

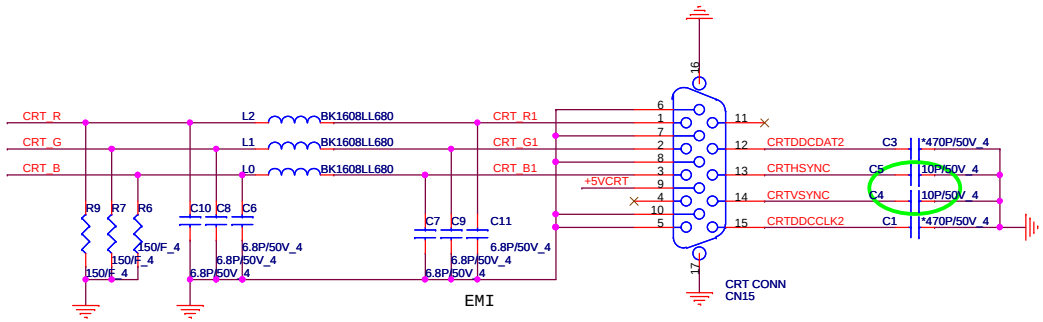
40 MIL

40 mils F0

+5V 2 1 +5VCRT +5VCRT

C0 0.1U/10V_4

SSM14 spec is 40V 1A

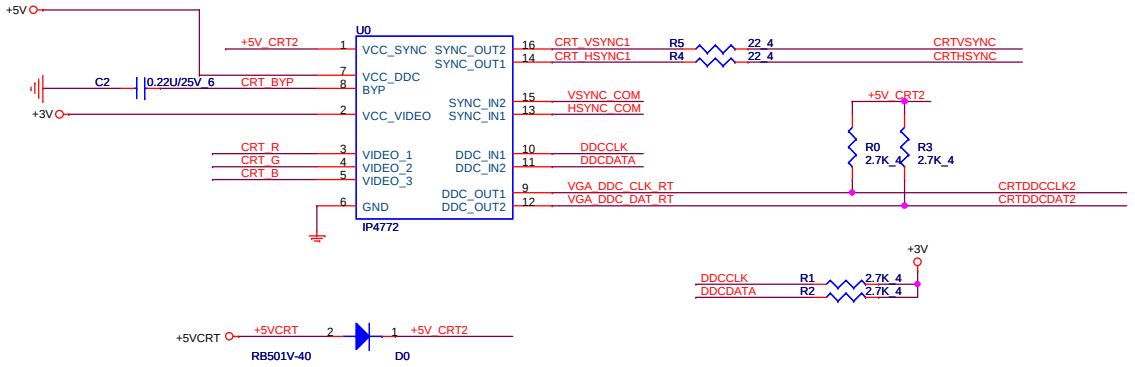



## FOR UMA

<7> CRT_R_IGPU — R23 *0_4 — CRT_R
<7> CRT_G_IGPU — R26 *0_4 — CRT_G
<7> CRT_B_IGPU — R29 *0_4 — CRT_B
<7> HSYNC_COM_IGPU — R21 *0_4 — HSYNC_COM
<7> VSYNC_COM_IGPU — R19 *0_4 — VSYNC_COM
<7> DDCCLK_IGPU — R32 *0_4 — DDCCLK
<7> DDCDATA_IGPU — R35 *0_4 — DDCDATA

## FOR DISCRETE

<15> CRT_R_DGPU — R22 0_4 — CRT_R
<15> CRT_G_DGPU — R25 0_4 — CRT_G
<15> CRT_B_DGPU — R28 0_4 — CRT_B
<15,16> HSYNC_COM_DGPU — R20 0_4 — HSYNC_COM
<15,16> VSYNC_COM_DGPU — R18 0_4 — VSYNC_COM
<15> DDCCLK_DGPU — R31 0_4 — DDCCLK
<15> DDCDATA_DGPU — R34 0_4 — DDCDATA





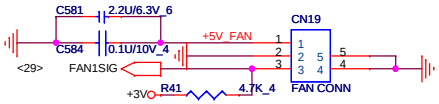


**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | CRT | 1A |

Date: Thursday, December 03, 2009 Sheet 22 of 40

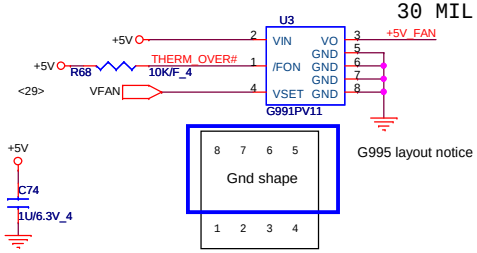
# CPU FAN



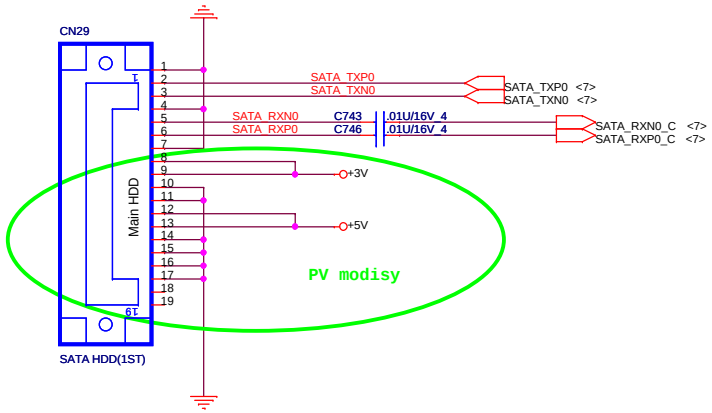

DFHD03MR008

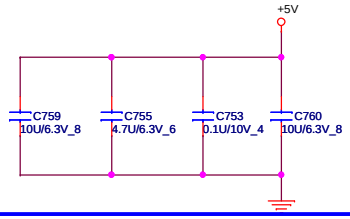
FANPWR = 1.6*VSET

30 MIL

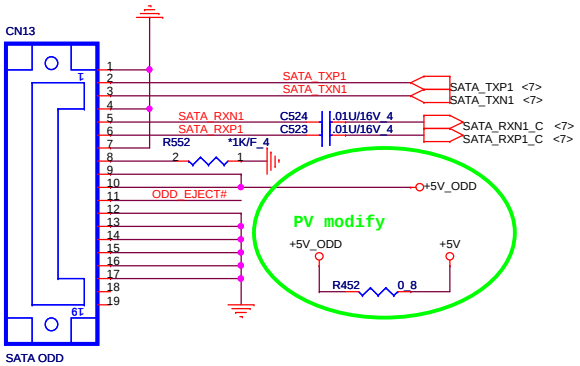


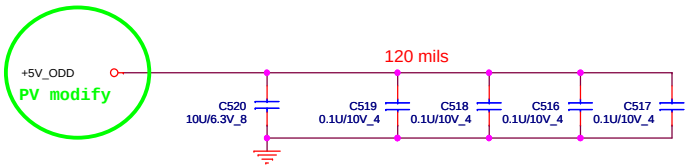

# SATA HDD CONNECTOR



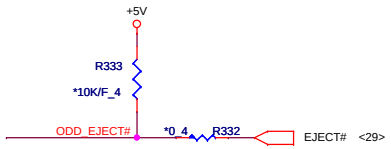




# SATA ODD CONNECTOR

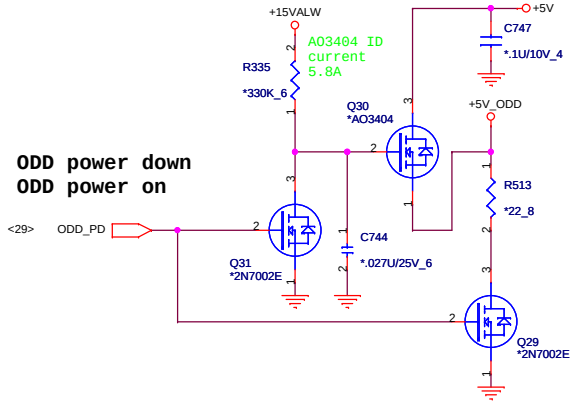



SI Add



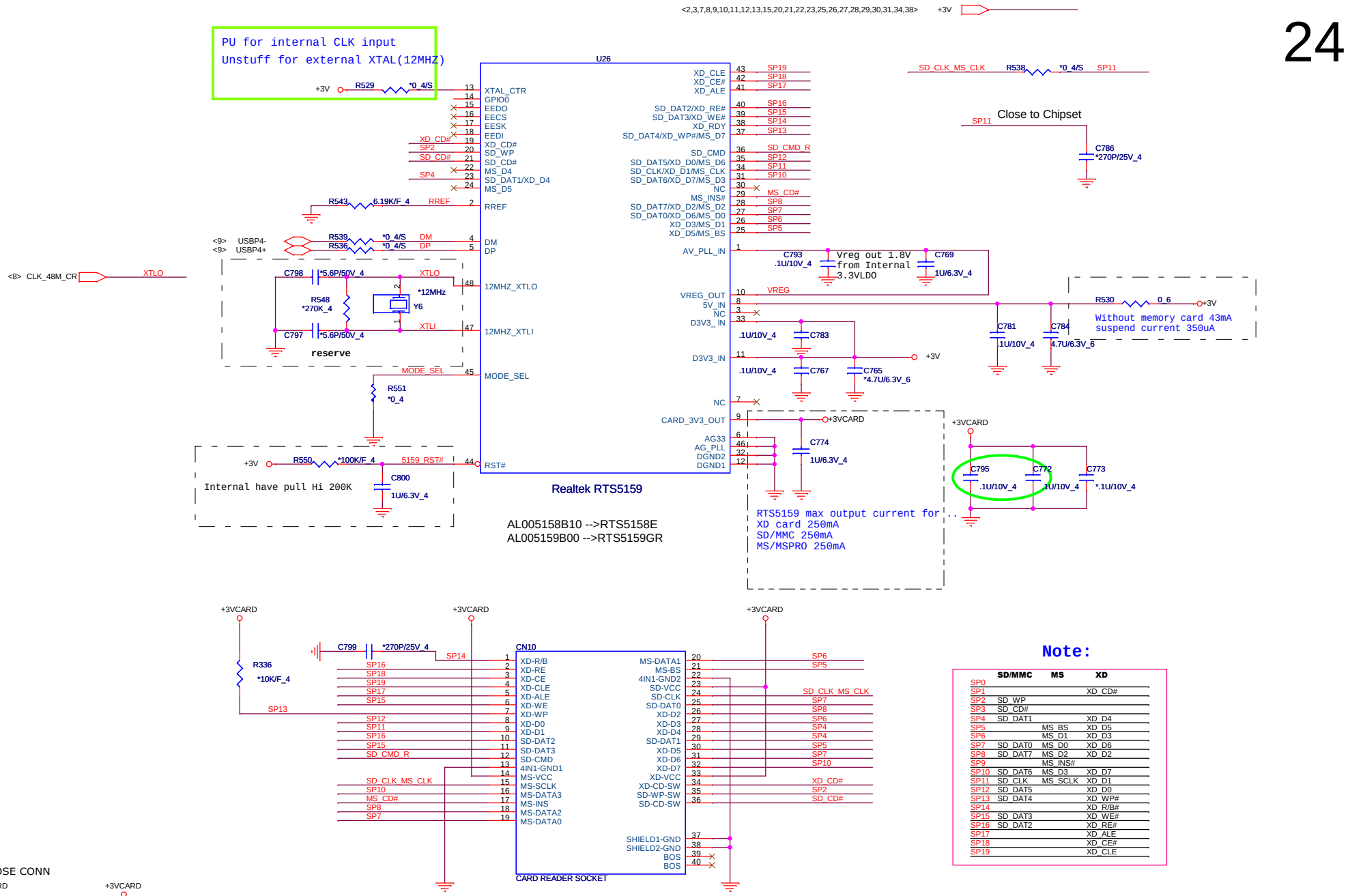

High : ODD power down
Low : ODD power on

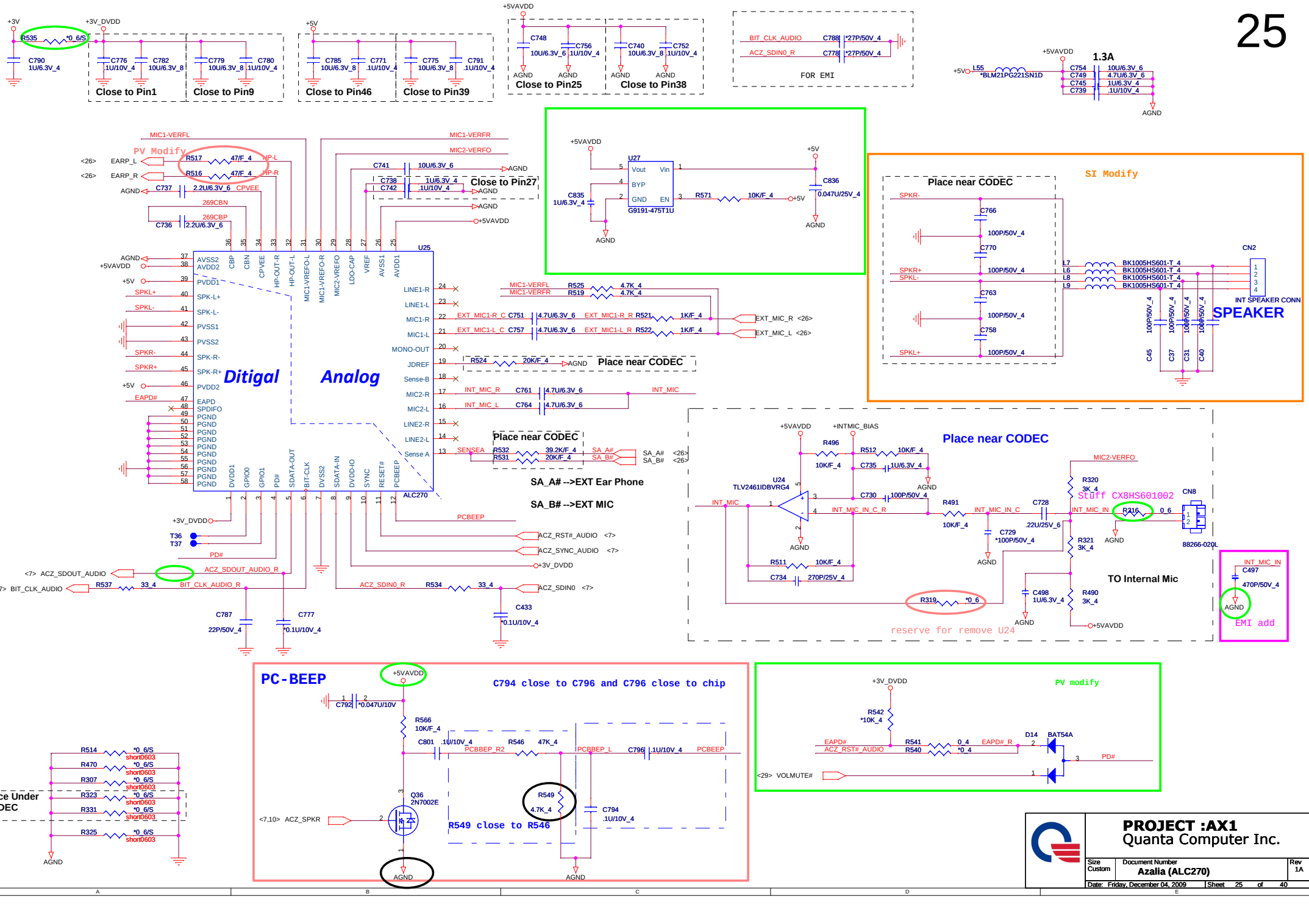



**PROJECT :AX1**
Quanta Computer Inc.

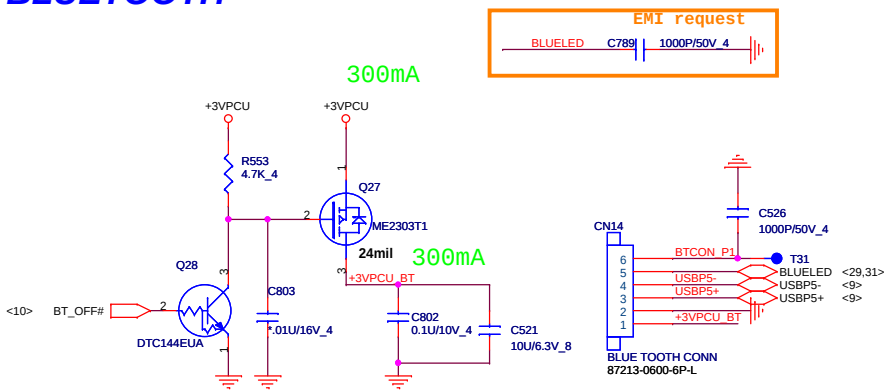
| Size | Document Number | Rev |
|---|---|---|
| Custom | HDD/ODD/FAN | 1A |

Date: Thursday, November 12, 2009 | Sheet 23 of 40

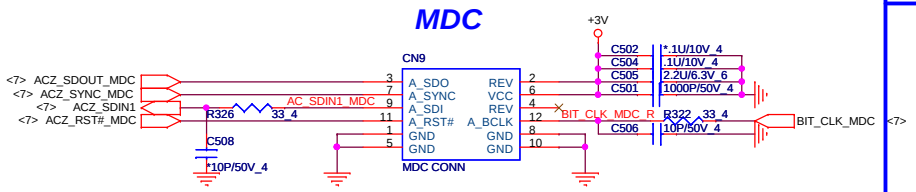

PU for internal CLK input
Unstuff for external XTAL(12MHZ)
U26
Realtek RTS5159
AL005158B10 -->RTS5158E
AL005159B00 -->RTS5159GR
RTS5159 max output current for ..
XD card 250mA
SD/MMC 250mA
MS/MSPRO 250mA
Close to Chipset
Vreg out 1.8V
from Internal
3.3VLDO
Without memory card 43mA
suspend current 350uA
Internal have pull Hi 200K
reserve
CN10
CARD READER SOCKET
5 IN1 CARD-READER (PUSH-PUSH)
Support SD/SD PRO/MMC/MS/MS PRO/xD Cards
CLOSE CONN
Note:
SD/MMC MS XD
SP0
SP1 XD_CD#
SP2 SD_WP
SP3 SD_CD#
SP4 SD_DAT1 XD_D4
SP5 MS_BS XD_D5
SP6 MS_D1 XD_D3
SP7 SD_DAT0 MS_D0 XD_D6
SP8 SD_DAT7 MS_D2 XD_D2
SP9 MS_INS#
SP10 SD_DAT6 MS_D3 XD_D7
SP11 SD_CLK MS_SCLK XD_D1
SP12 SD_DAT5 XD_D0
SP13 SD_DAT4 XD_WP#
SP14 XD_R/B#
SP15 SD_DAT3 XD_WE#
SP16 SD_DAT2 XD_RE#
SP17 XD_ALE
SP18 XD_CE#
SP19 XD_CLE

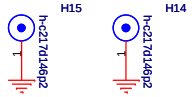


# BLUETOOTH



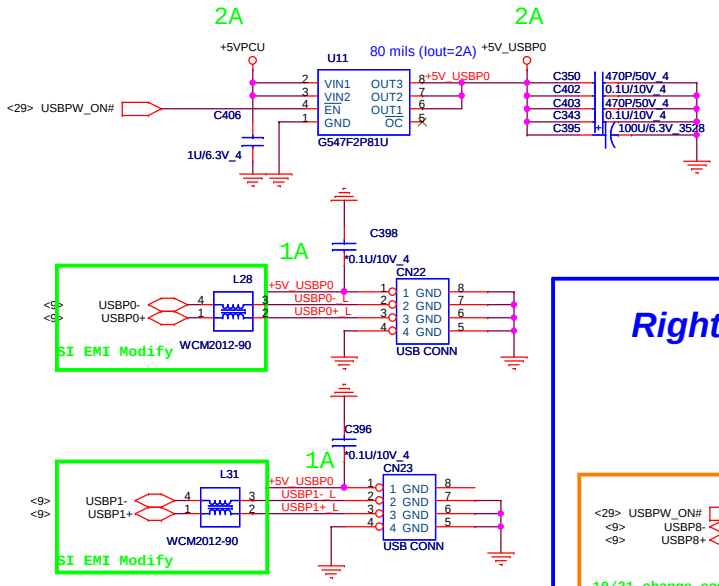

# Modem CONN



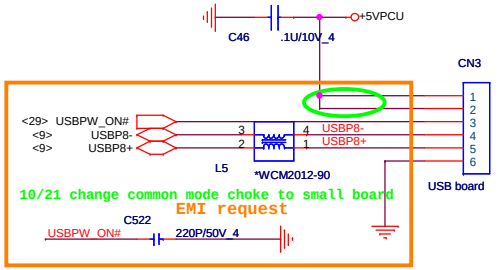



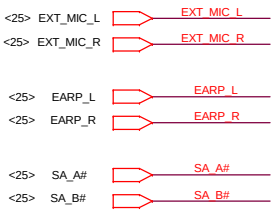

Nut PN:MBCA6002013

# LEFT SIDE USBX1




# Right SIDE USBX1

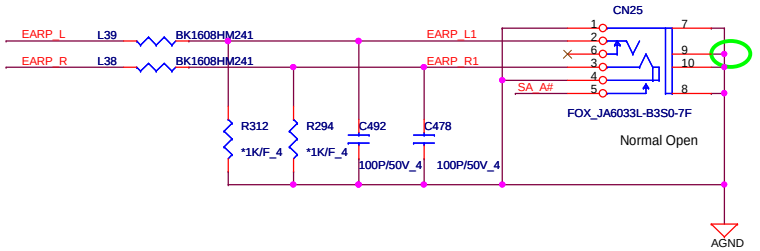


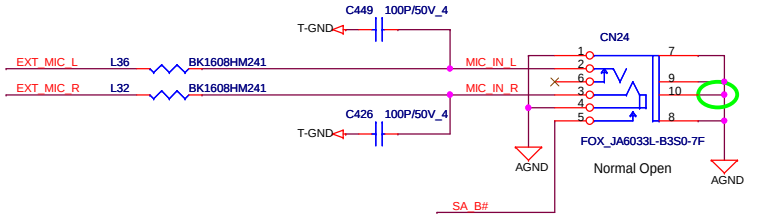

**SA_A# -->EXT Ear Phone**

**SA_B# -->EXT MIC**

# Line out

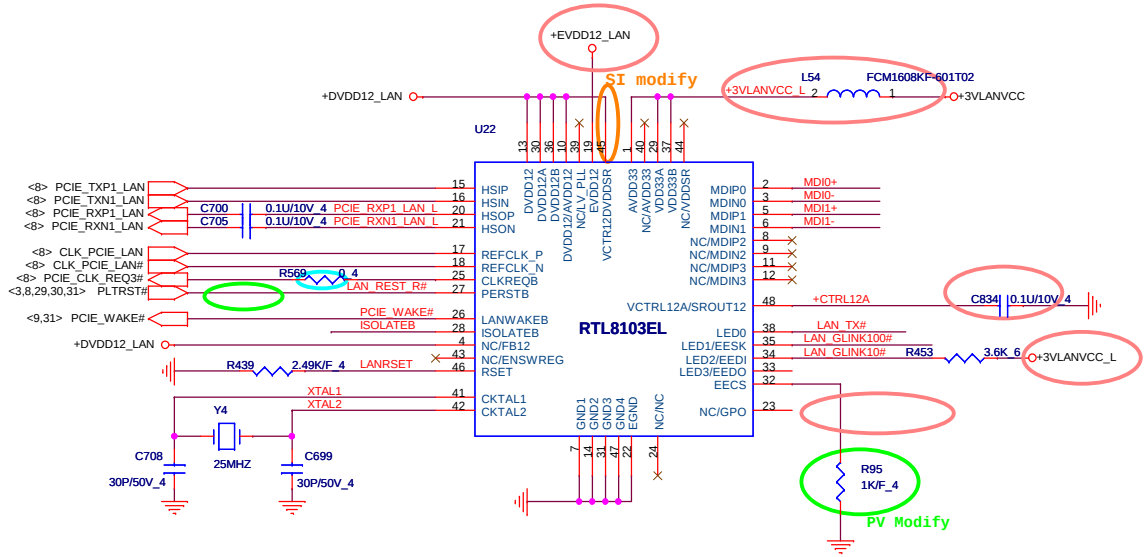


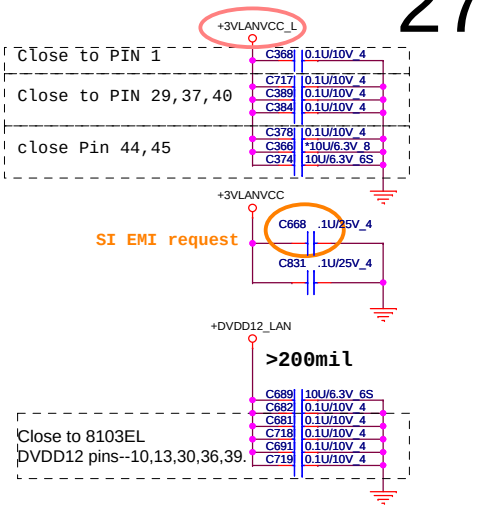

# MIC

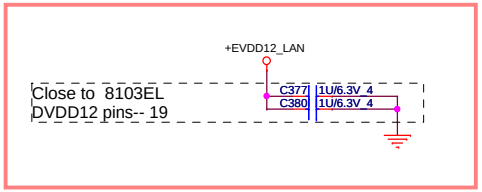


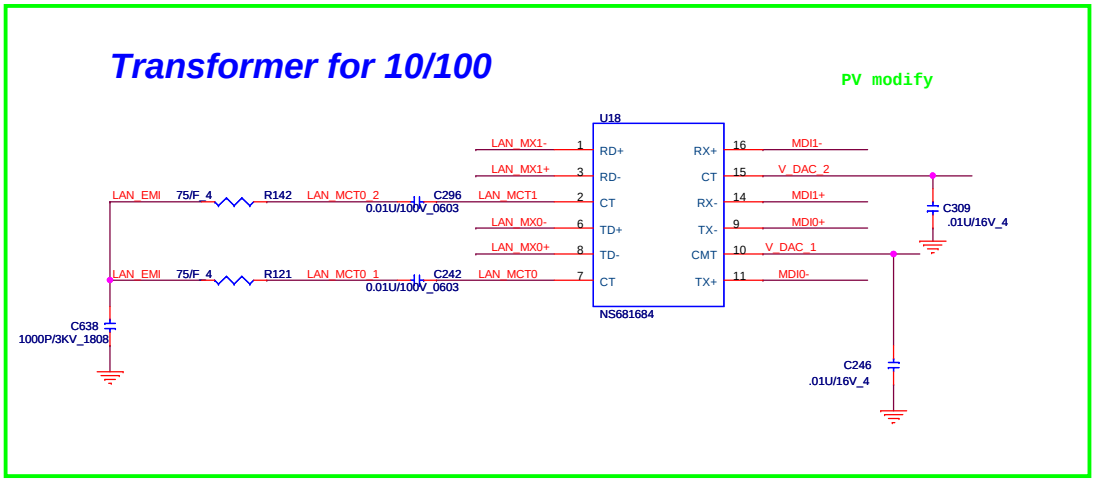

**PROJECT :AX1**
Quanta Computer Inc.

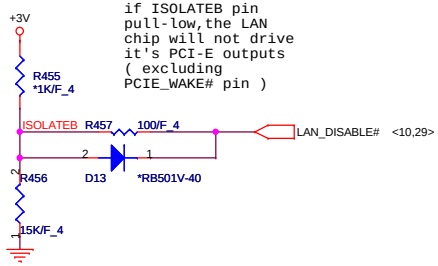
| Size | Document Number | Rev |
|---|---|---|
| Custom | USB/BT/Modem/Audio JacK | 1A |
| Date: Monday, November 30, 2009 | Sheet 26 of 40 | |

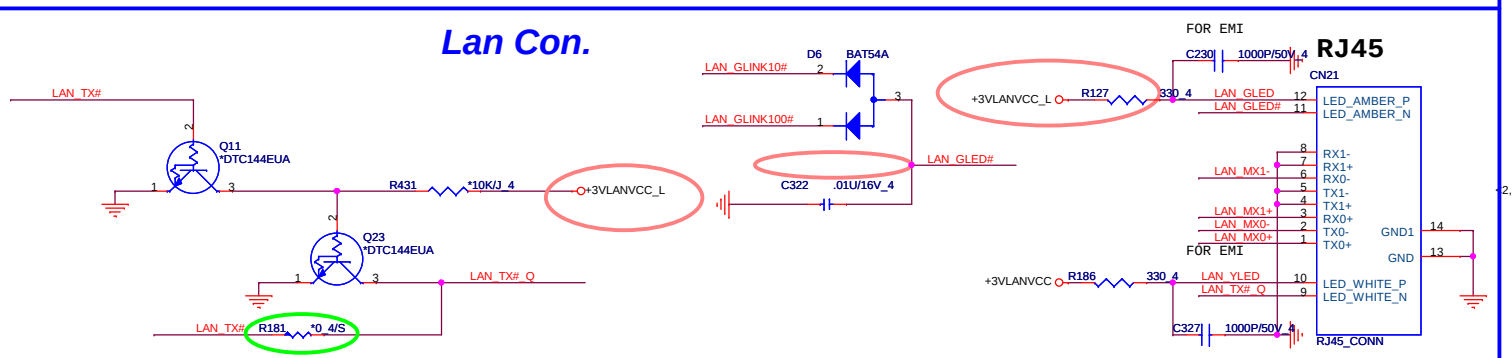


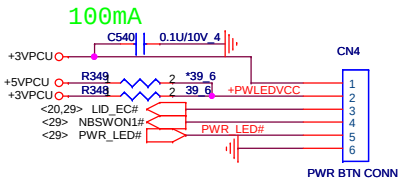



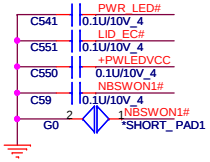



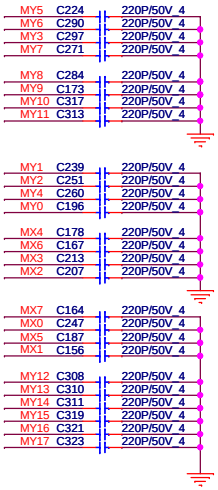
# POWER BOTTON CONNECT

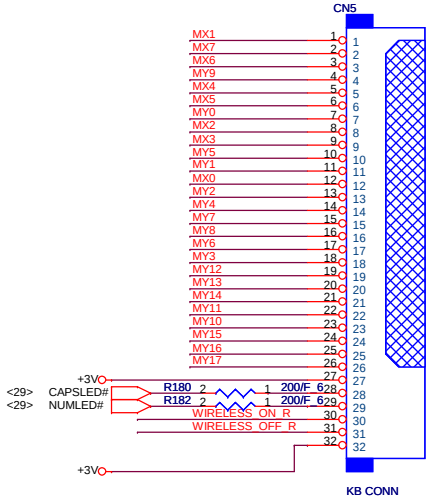


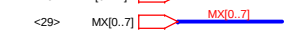

1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND



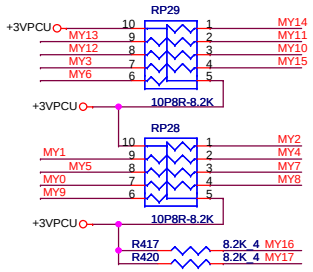

# KEYBOARD Con.



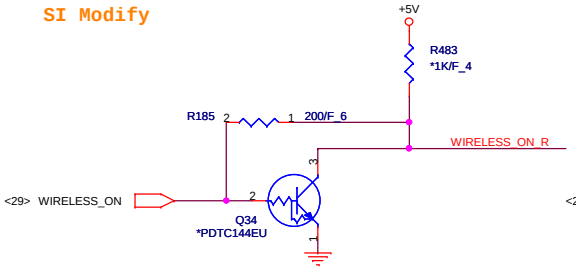



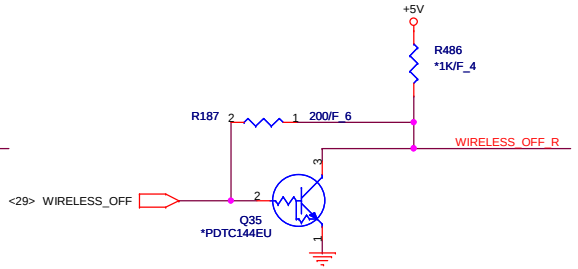




## KEYBOARD PULL-UP

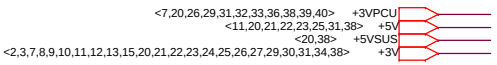



## SI Modify

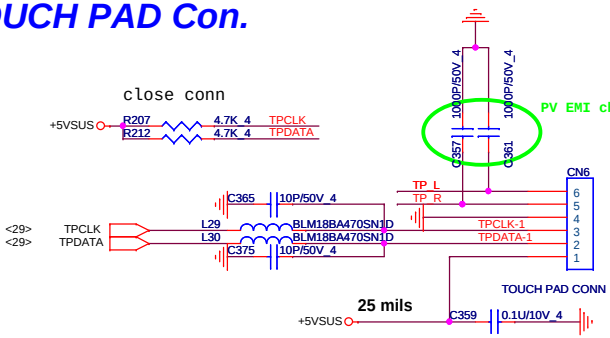


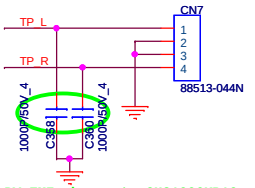





# TOUCH PAD Con.




# To TOUCH PAD SW board




**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | LED/KB/SW/TP | 1A |

Date: Thursday, November 12, 2009 Sheet 28 of 40

500mA

U4

KB3926QF D2

SI Add

for Battery charge/charge and cap board

for VGA/CPU thermal

SI modify

for EMI

For KB3926 B, C version

## adapter Type check

Change to 1SS355 as Current loss

## thermal shutdown circuit

SI Modify

## adapter select for EC

Hi ==> 120W

Low ==> 65W/90W

## 512K byte SPI EC ROM

Socket: DG008000031

MXIC AKE3KZP0001

WINBOND AKE37ZN0N00

AMIT AKE38ZN0800

| Project Model | GPIO42 |
|---|---|
| AX 14" | High |
| AX 15.6" | Low |
| AX 17.3" | Middle (1.5V) |

GPIO42 control fan table

Change to RB500 as Current loss

Add Pin 117,103 for DSM,116 for Bluetooth

Delete T10 and tie pin 117 from Lan for DSM

AC present: AC_IN-->high, CPU_PROCHOT-->low , H_PROCHOT#-->high

Remove AC: AC_IN-->low, CPU_PROCHOT-->low , H_PROCHOT#-->low

Remove AC and re-cove prochot: AC_IN-->low, CPU_PROCHOT--> high, H_PROCHOT#--> high

**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | EC (KB3926)/ROM | 1A |

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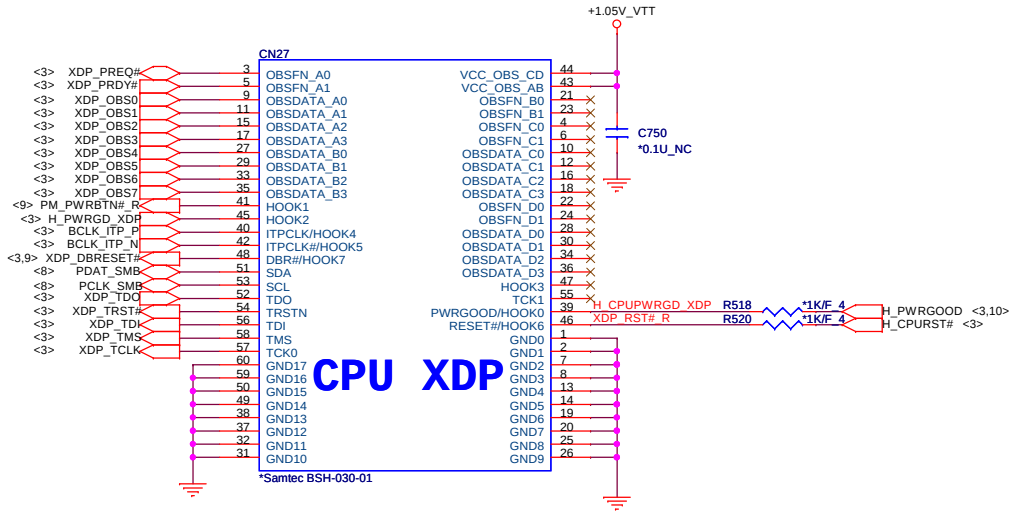
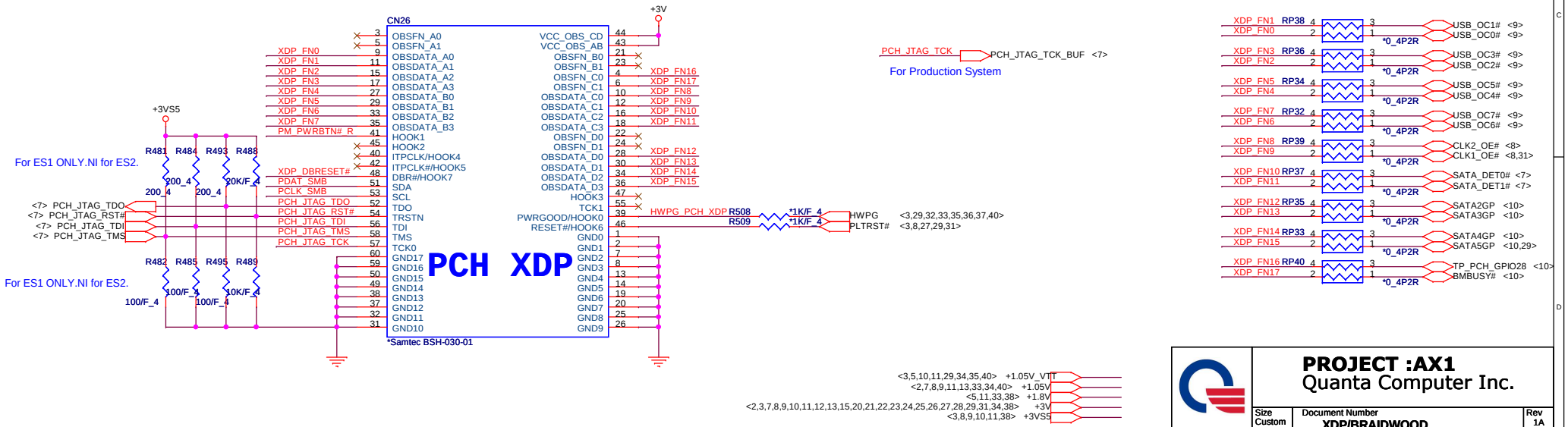


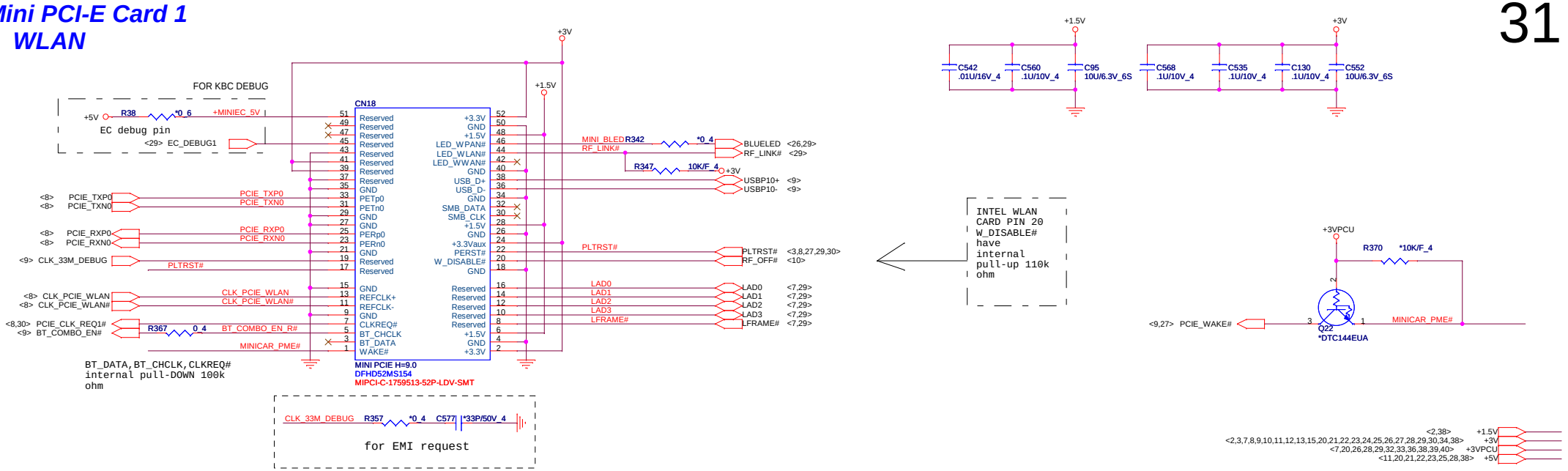

**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | XDP/BRAIDWOOD | 1A |

Date: Thursday, November 12, 2009 | Sheet 30 of 40

# Mini PCI-E Card 1
# WLAN









INTEL WLAN CARD PIN 20 W_DISABLE# have internal pull-up 110k ohm




<2,38> +1.5V
<2,3,7,8,9,10,11,12,13,15,20,21,22,23,24,25,26,27,28,29,30,34,38> +3V
<7,20,26,28,29,32,33,36,38,39,40> +3VPCU
<11,20,21,22,23,25,28,38> +5V

**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | MINI PCIE CONN X1 | 1A |

Date: Thursday, November 12, 2009 Sheet 31 of 40

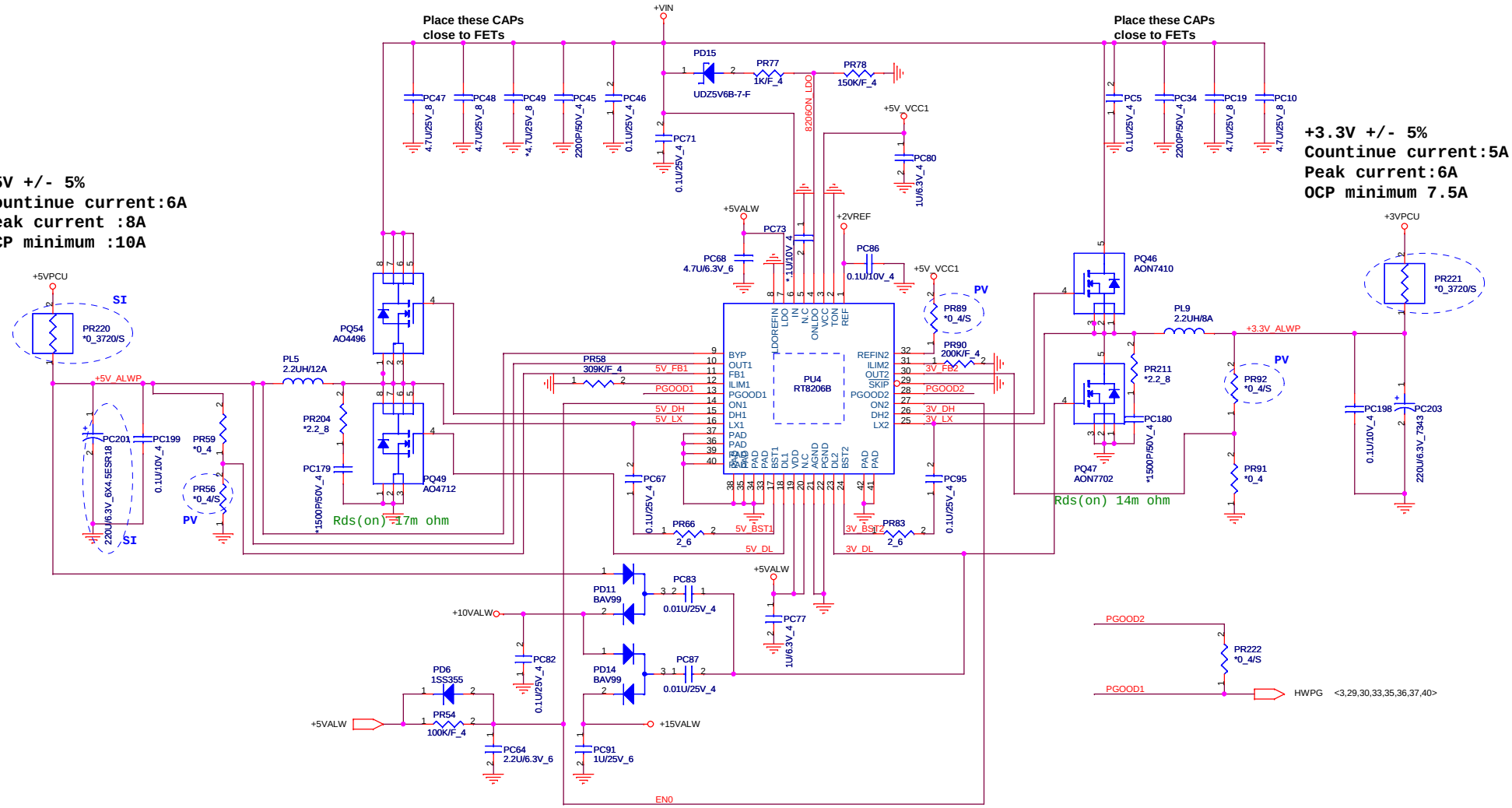
# DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

**+5V +/- 5%**
**Countinue current:6A**
**Peak current :8A**
**OCP minimum :10A**

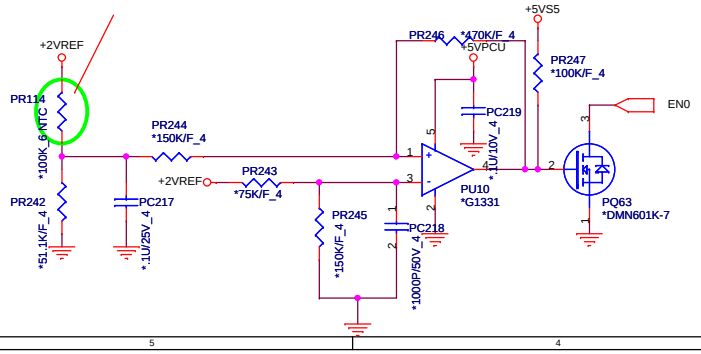
**+3.3V +/- 5%**
**Countinue current:5A**
**Peak current:6A**
**OCP minimum 7.5A**

Place these CAPs close to FETs

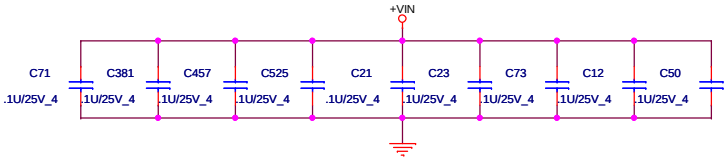
Place these CAPs close to FETs




**NTC need place under CPU Socket**
**CPU Thermal protection at 90 +/-3 degrreC**



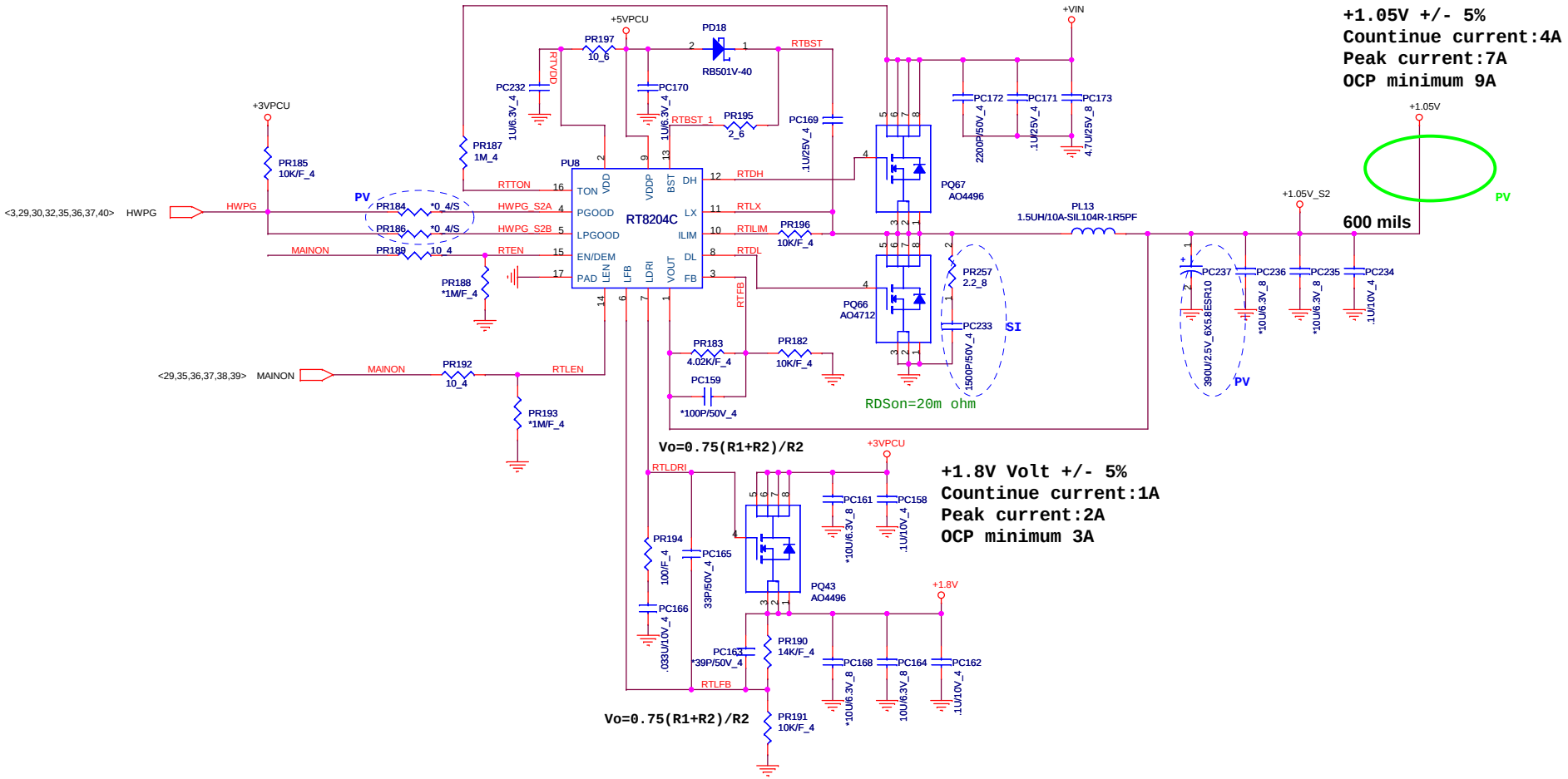

EMI request



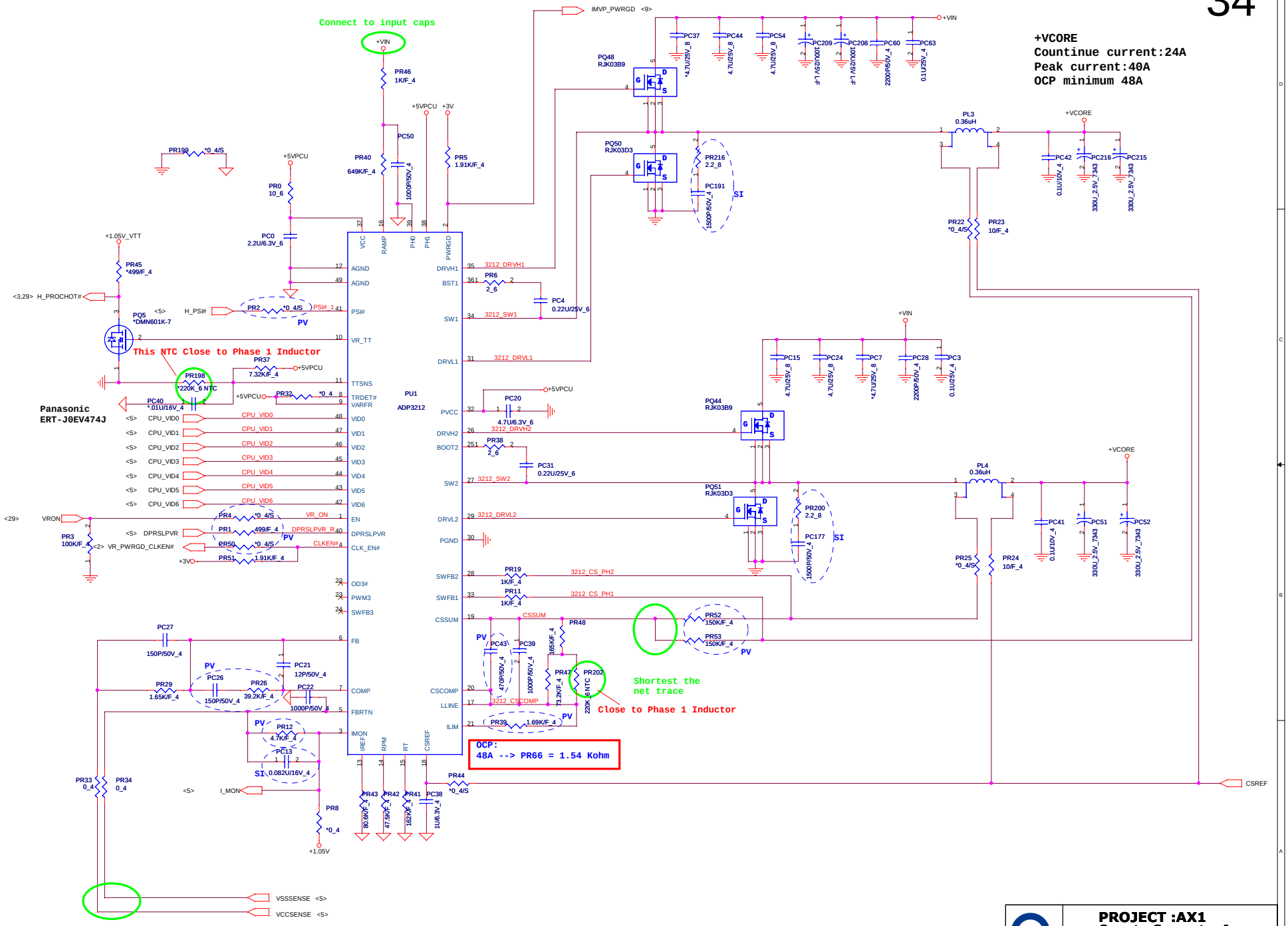

**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | +5V/+3V (RT8206B) | 1A |

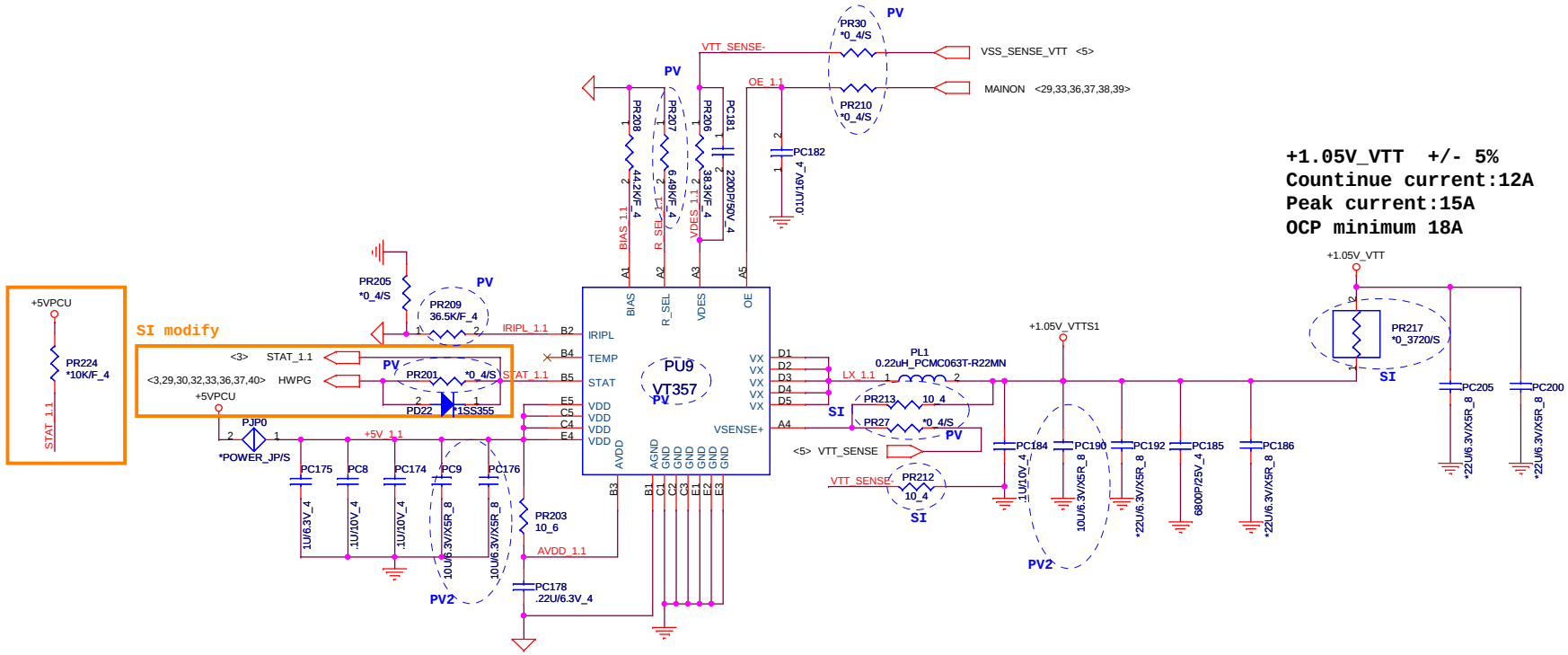
Date: Thursday, November 12, 2009 | Sheet 32 of 40




| | | | |
|---|---|---|---|
| | **PROJECT :AX1** Quanta Computer Inc. | | |
| Size: Custom | Document Number: +1.05V/+1.8V (RT8204C) | | Rev: 1A |
| Date: Thursday, November 12, 2009 | Sheet 33 of 40 | | |




| | | |
|---|---|---|
| PROJECT :AX1 Quanta Computer Inc. | | |
| Size: Custom | Document Number: CPU Core (ADP3212) | Rev: 1A |
| Date: Thursday, November 12, 2009 | Sheet 34 of 40 | |

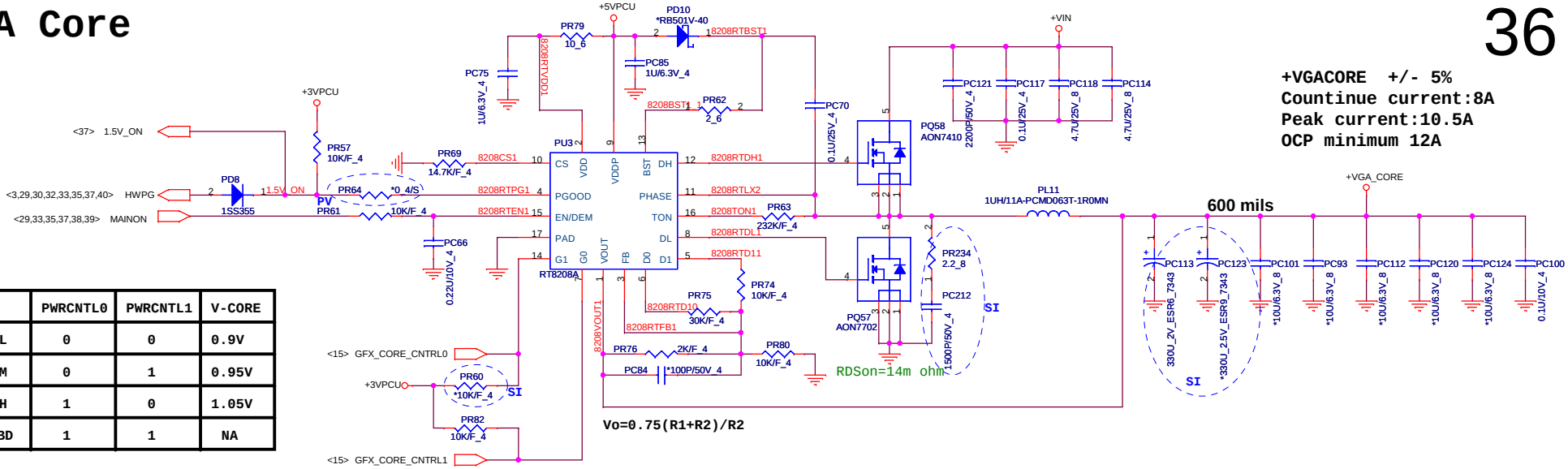



| | | |
|---|---|---|
| | **PROJECT :AX1**<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: +1.05V_VTT (VT358) | Rev: 1A |
| Date: Thursday, November 12, 2009 | Sheet 35 of 40 | |

# VGA Core



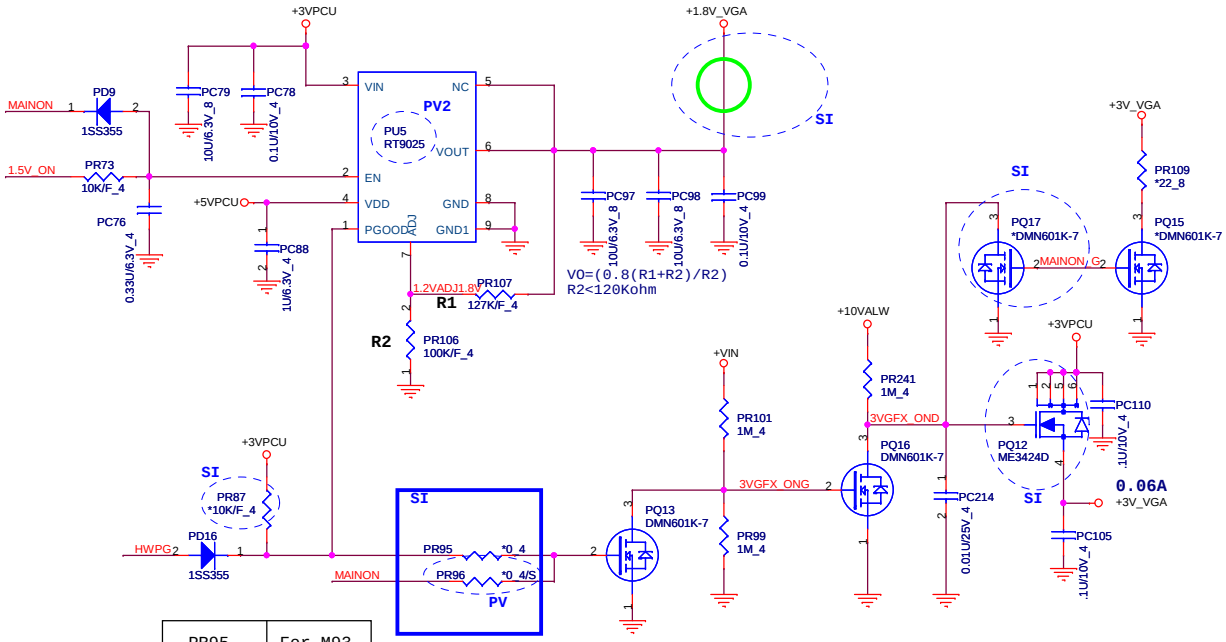
+VGACORE +/- 5%
Countinue current:8A
Peak current:10.5A
OCP minimum 12A




Vo=0.75(R1+R2)/R2

| | PWRCNTL0 | PWRCNTL1 | V-CORE |
|---|---|---|---|
| L | 0 | 0 | 0.9V |
| M | 0 | 1 | 0.95V |
| H | 1 | 0 | 1.05V |
| TBD | 1 | 1 | NA |

+1.8V +/- 5%
Countinue current:1.2A
Peak current:3A



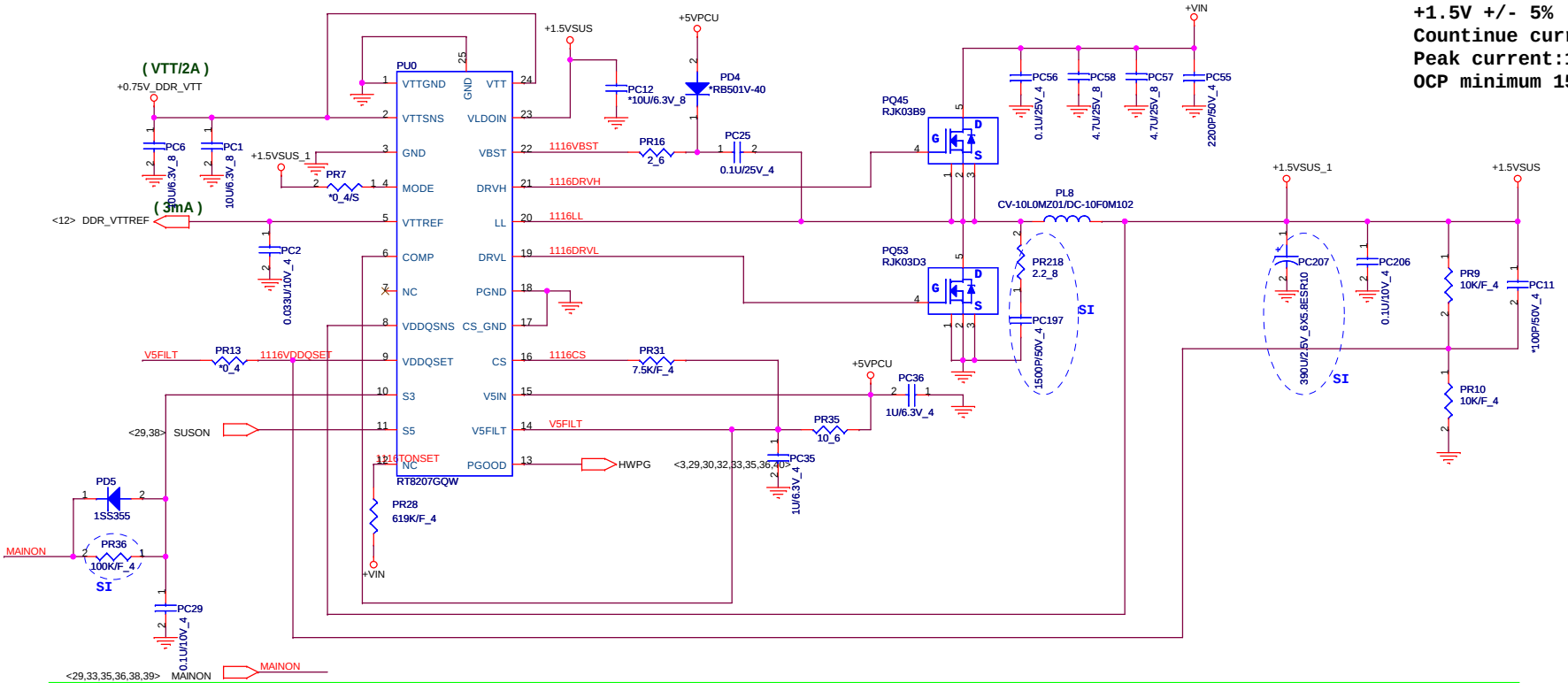

| | |
|---|---|
| PR95 | For M93 |
| PR96 | For PARK |

**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | +VGACORE (RT8208/1.8V) | 1A |

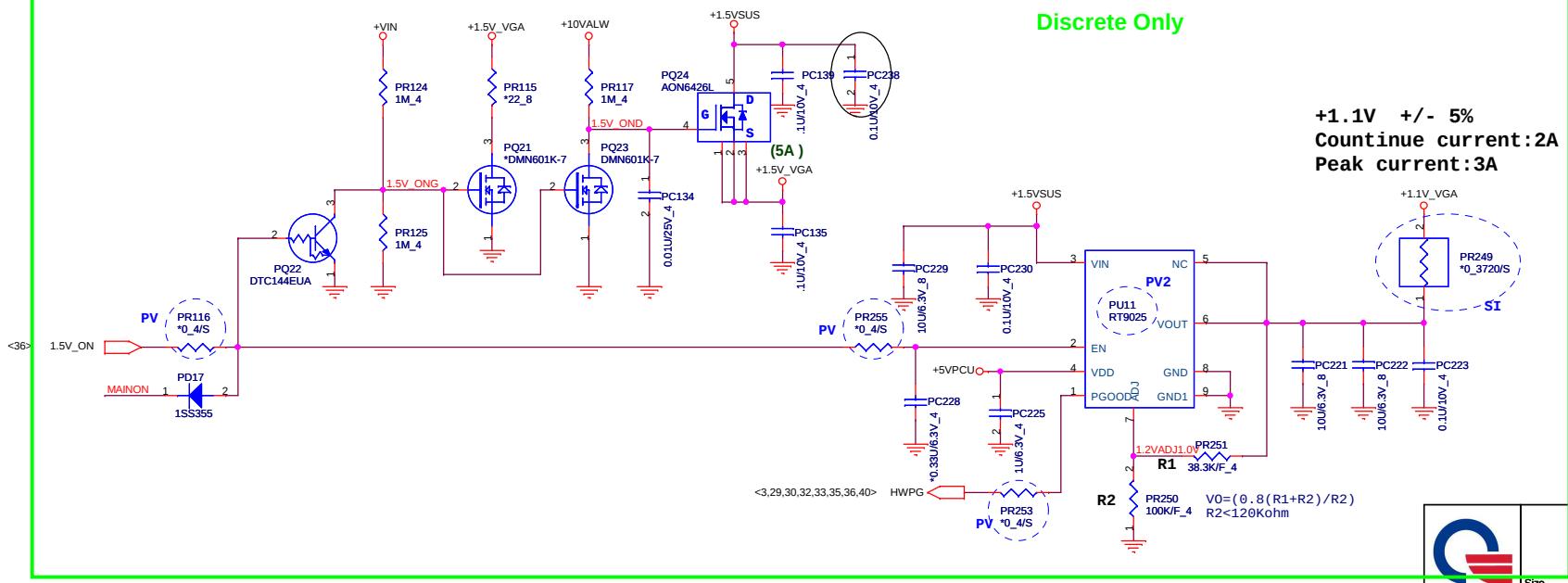
Date: Thursday, November 12, 2009 | Sheet 36 of 40

+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A




Discrete Only

+1.1V +/- 5%
Countinue current:2A
Peak current:3A




**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | DDR3 (RT8207) | 1A |

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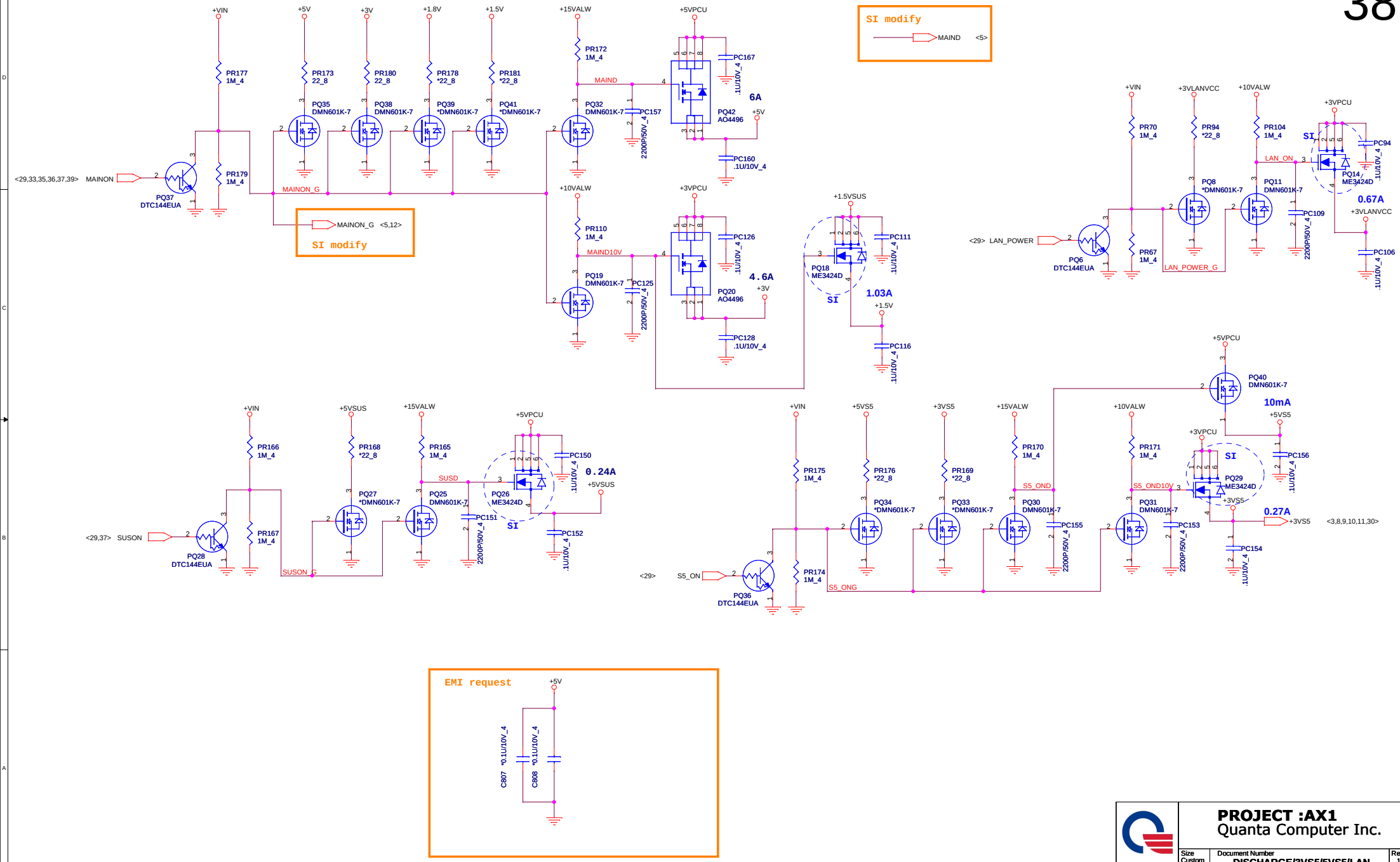
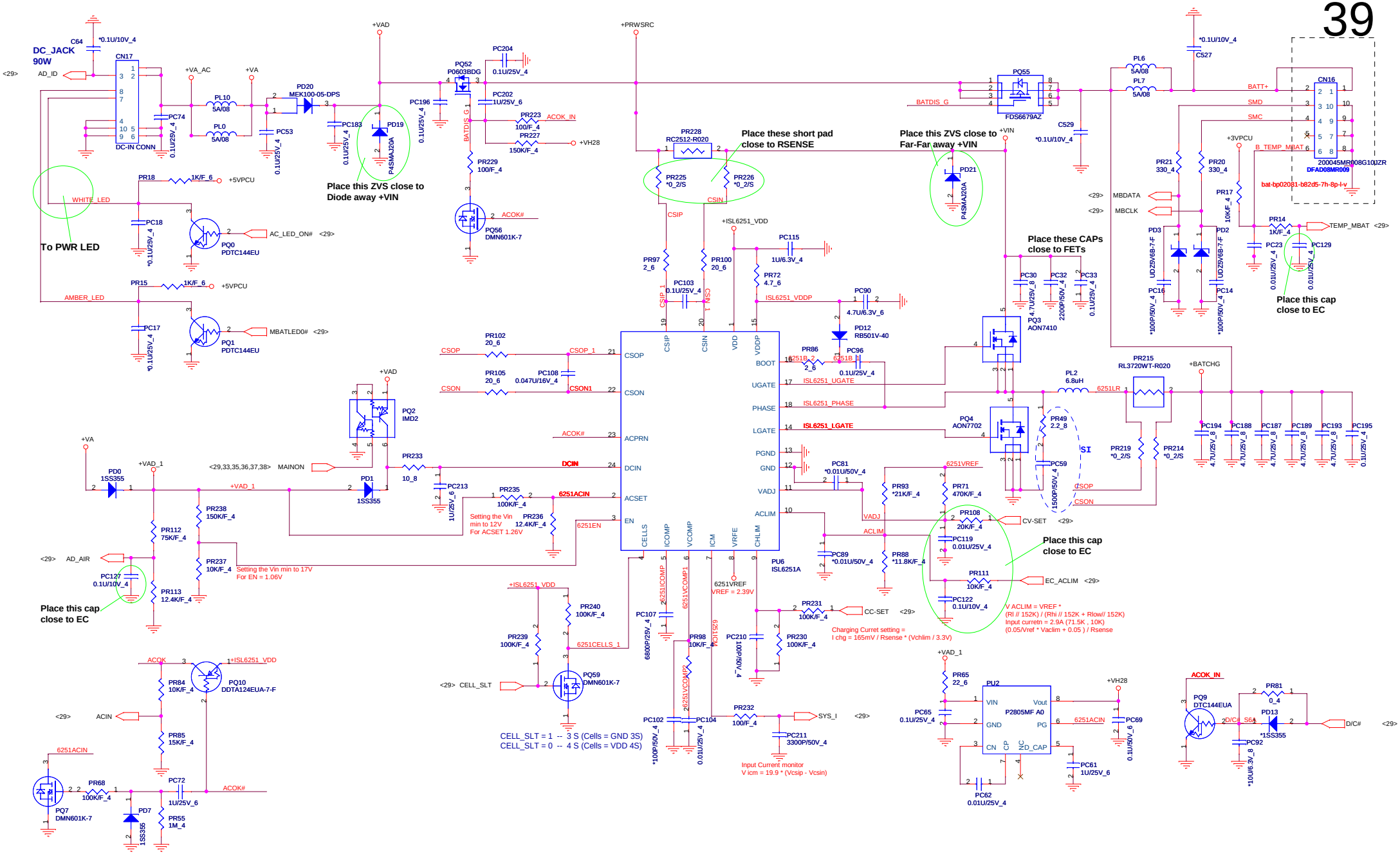



**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | DISCHARGE/3VS5/5VS5/LAN | 1A |

Date: Thursday, November 12, 2009 | Sheet 38 of 40



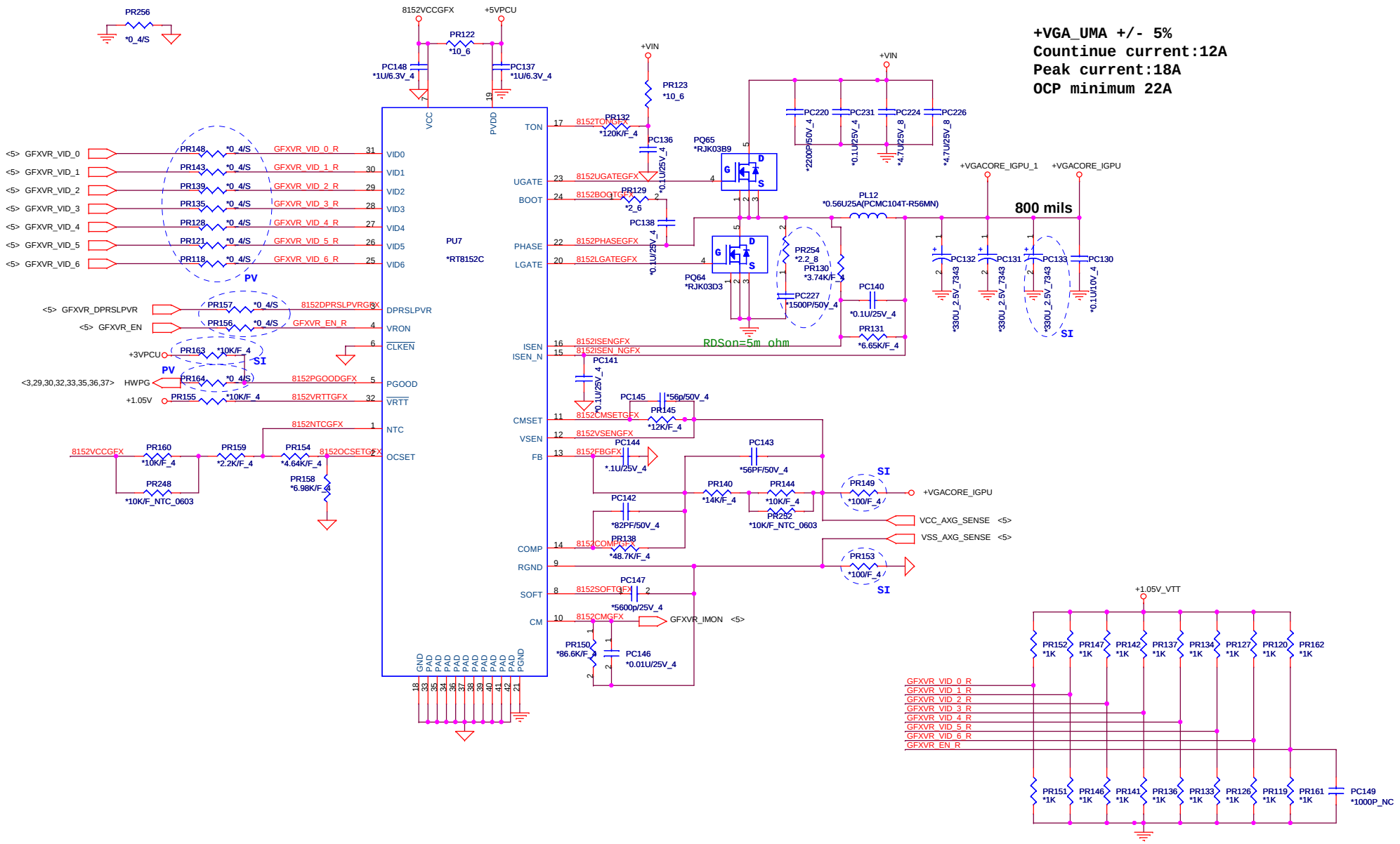


**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | CHARGER (ISL6251) | 1A |

Date: Thursday, November 12, 2009 | Sheet 39 of 40

+VGA_UMA +/- 5%
Countinue current:12A
Peak current:18A
OCP minimum 22A




**PROJECT :AX1**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | UMA GPU CORE (RT8152C) | 1A |

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