ARES/ARTEMIS Block Diagram

MV - PHASE

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

RUN POWER SW PG 36,37

AC/BATT CONNECTOR PG 34

BATT CHARGER PG 34

CPU VR PG 38

DC/DC +3VSUS +5VSUS PG 33

Turion64 Sempron

25W/35W
AMD Socket S1 638P
PG 2,3,4

DDRII-SODIMM1 PG 5 — *DDRII 667mhz*

DDRII-SODIMM2 PG 5 — *DDRII 667mhz*

HT Link

nVIDIA MCP67 MCP67D

Integraded VGA Function
836PIN
PG 5,6,7,8,9,10,11

PCI-E X 1

Mini PCI-E Card
PCI Express Mini Card
(Wireless LAN/WAN)
PG 27

Express Card
(NEW CARD)
PG 28

SIM CARD PG 27

PCI-Express 16X

NVDIA NB8M-64bit
Graphics
PG 12,13,14,15,16,17

Option for 17" only
HDMI CON PG 18

TV_OUT
CRT_OUT

CRT/S-VIDEO PG 19

LVDS(2 Channel)

Panel Connector
15" / 17" PG 18

CLOCK INTERFACE

SATA1

Option for 17" only
SATA - HDD PG 26

SATA0

SATA - HDD PG 26

PATA (66/100/133)

PATA- CD-ROM PG 26

USB2.0

Bluetooth PG 28

FingrPrint PG 28

USB2.0 I/O Ports X3 PG 26

Camera 1.3MP PG 23

Mini PCI-E Card x1
Express Card x1
Cable Docking x1

PCI BUS / 33MHz

LAN

HD AUDIO

Conexant
Venice AMOM
CX20561-12
PG 23

Two-element microphone PG 23

Audio Jacks
-Phone
-SPDIF
-MIC
PG 23

REALTEK
RTL8201CL (10/100)
RTL8211B (10/100/Gigabit)
PG 20

RICOH
RICOH R5C832
R5C833
PG 21

LAN RJ45 PG 20

IEEE1394 CONN PG 21

Memory Card Reader PG 22

AUDIO Amplifier TPA0312 PG 25

Jack to Speaker PG 25

MDC DAA CX20548-S PG 24

MODEM RJ 11 PG 20

LPC

TPM SLB9635 PG 28

ENE KBC
KB3920 Bx
KB3926
PG 30,31

Keyboard Touch Pad PG 29

CIR PG 23

Capacitive Sense SW PG 29

X-Bus

FAN PG 31

SPI ROM PG 30

Cable Docking PG 31

- TV_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

VAULE DEFINE

A=0603,B=0805,C=1206,F=1%, OTHER IS 0402
V=Y5V,U=Y5U,R=X5R,S=X6S, X=X7R,G=COG,O=NPO

EXAMPLE

10R=10ohm(0402)
10A=10ohm(0603)
10B=10ohm(0805)
10C=10ohm(1206)
10/F=10ohm(0402 and 1%)

EXAMPLE

0.1U/16V/R=0.1U/16V/X5R(0402)
0.47UA/10V/X=0.47U/10V/X7R(0603)
10UB/10V/U=10U/10V/Y5U(0805)

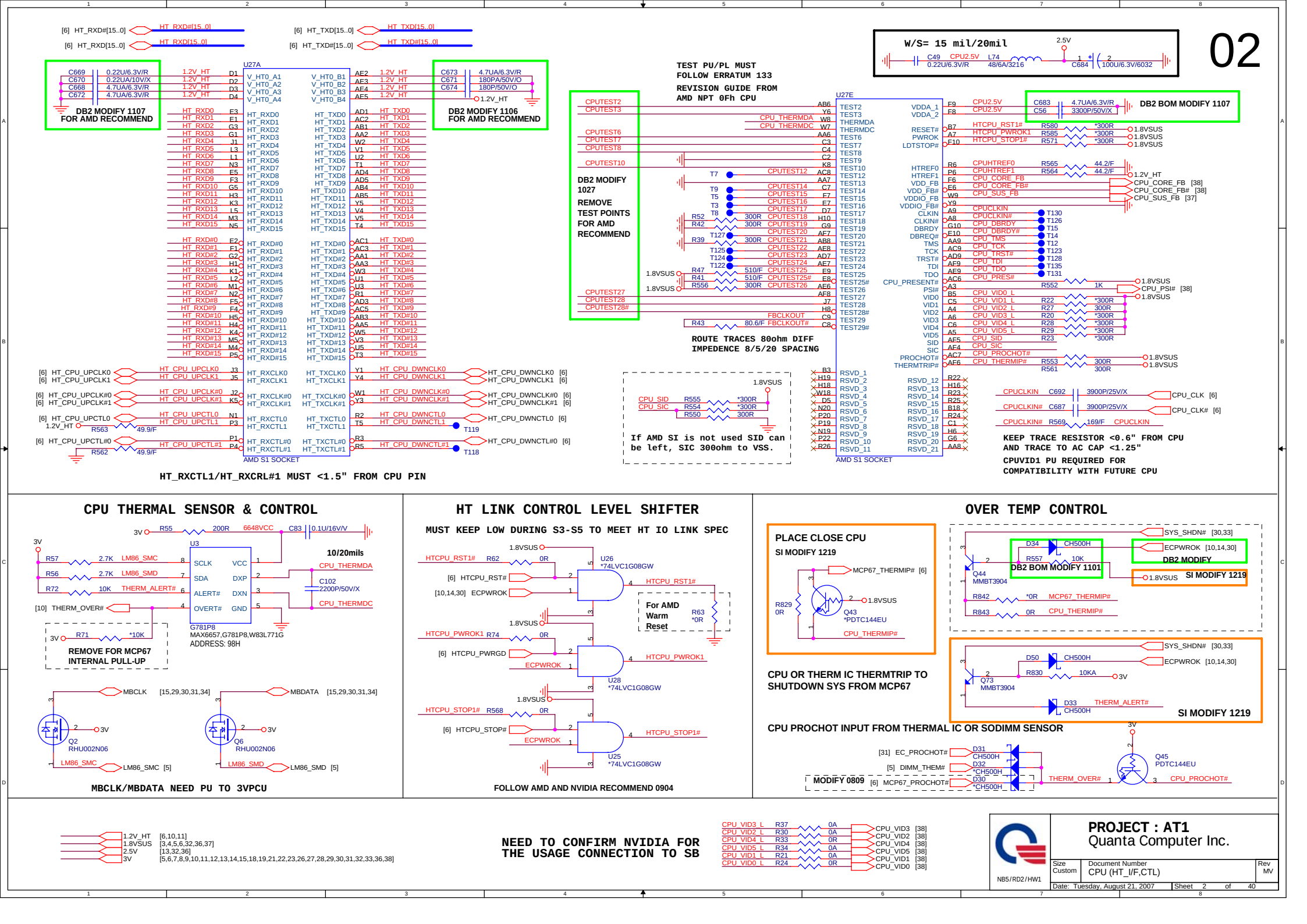
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTA#,INTB#	RICOH832

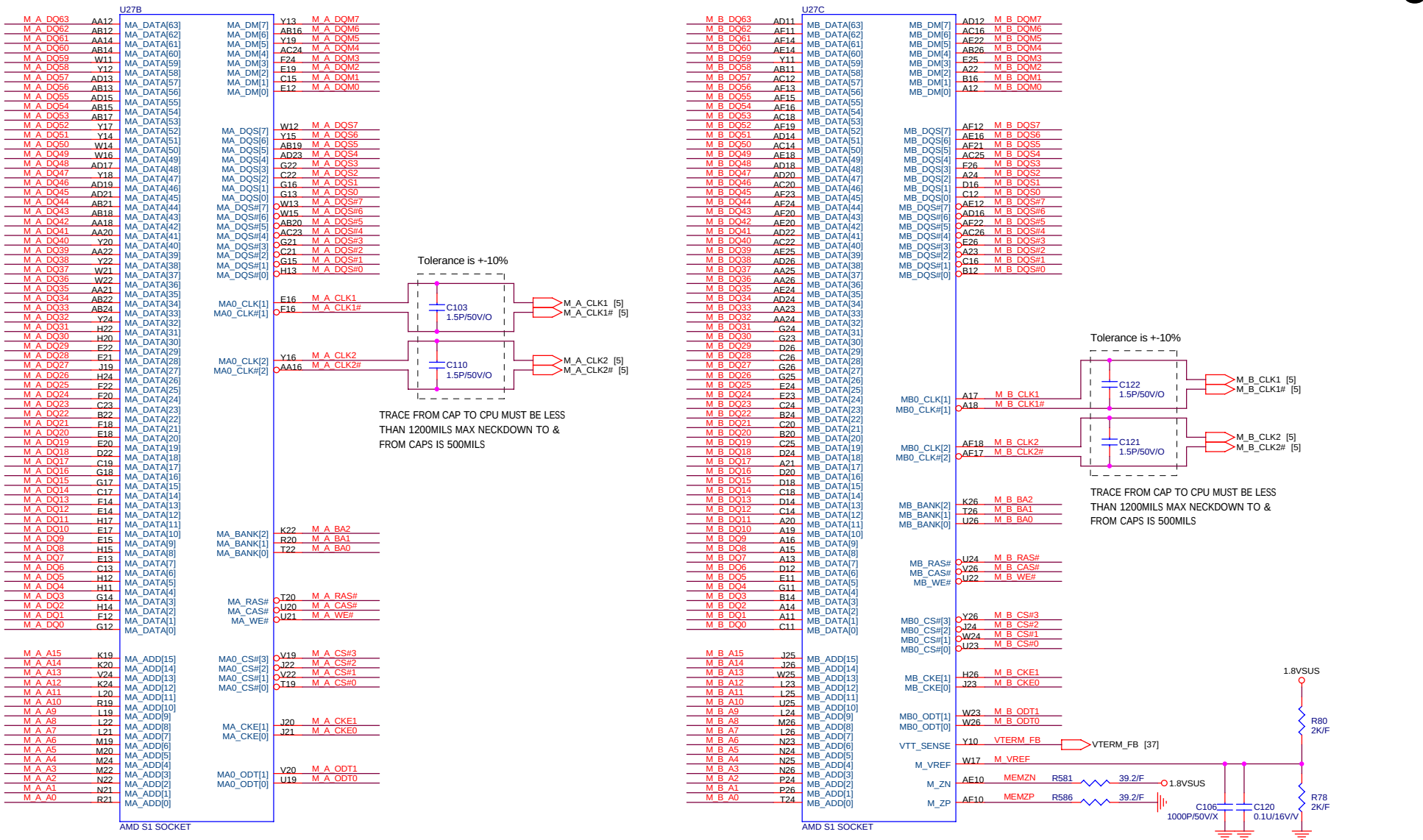
NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

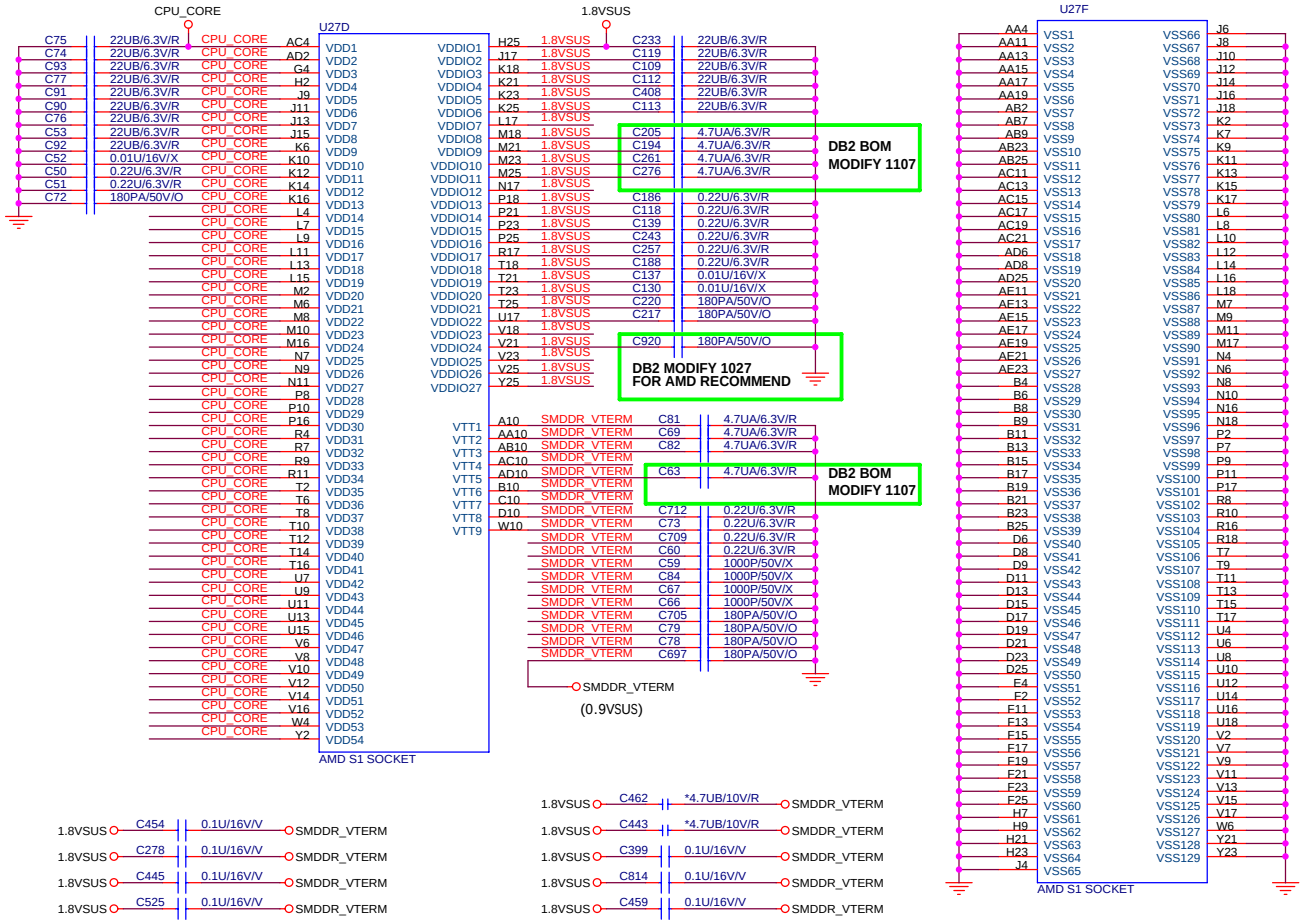
Size	Document Number	Rev
Custom	BLOCK DIAGRAM	MV

Date: Tuesday, August 21, 2007 Sheet 1 of 40


02
W/S= 15 mil/20mil
2.5V
C49 CPU2.5V L74 C684
0.22U/6.3V/R 48/6A/3216 100U/6.3V/6032
U27A
U27E
DB2 MODIFY 1107
FOR AMD RECOMMEND
DB2 MODIFY 1106
FOR AMD RECOMMEND
DB2 BOM MODIFY 1107
TEST PU/PL MUST
FOLLOW ERRATUM 133
REVISION GUIDE FROM
AMD NPT 0Fh CPU
DB2 MODIFY
1027
REMOVE
TEST POINTS
FOR AMD
RECOMMEND
ROUTE TRACES 80ohm DIFF
IMPEDENCE 8/5/20 SPACING
If AMD SI is not used SID can
be left, SIC 300ohm to VSS.
KEEP TRACE RESISTOR <0.6" FROM CPU
AND TRACE TO AC CAP <1.25"
CPUVID1 PU REQUIRED FOR
COMPATIBILITY WITH FUTURE CPU
AMD S1 SOCKET
HT_RXCTL1/HT_RXCRL#1 MUST <1.5" FROM CPU PIN
CPU THERMAL SENSOR & CONTROL
10/20mils
REMOVE FOR MCP67
INTERNAL PULL-UP
G781P8
MAX6657,G781P8,W83L771G
ADDRESS: 98H
MBCLK
MBDATA
RHU002N06
MBCLK/MBDATA NEED PU TO 3VPCU
HT LINK CONTROL LEVEL SHIFTER
MUST KEEP LOW DURING S3-S5 TO MEET HT IO LINK SPEC
For AMD
Warm
Reset
FOLLOW AMD AND NVIDIA RECOMMEND 0904
OVER TEMP CONTROL
PLACE CLOSE CPU
SI MODIFY 1219
DB2 BOM MODIFY 1101
DB2 MODIFY
SI MODIFY 1219
CPU OR THERM IC THERMTRIP TO
SHUTDOWN SYS FROM MCP67
CPU PROCHOT INPUT FROM THERMAL IC OR SODIMM SENSOR
MODIFY 0809
NEED TO CONFIRM NVIDIA FOR
THE USAGE CONNECTION TO SB
PROJECT : AT1
Quanta Computer Inc.
NB5/RD2/HW1
Size Custom
Document Number CPU (HT_I/F,CTL)
Rev MV
Date: Tuesday, August 21, 2007
Sheet 2 of 40


U27B
M_A_DQ63 AA12
M_A_DQ62 AB12
M_A_DQ61 AA14
M_A_DQ60 AB14
M_A_DQ59 W11
M_A_DQ58 Y12
M_A_DQ57 AD13
M_A_DQ56 AB13
M_A_DQ55 AD15
M_A_DQ54 AB15
M_A_DQ53 AB17
M_A_DQ52 Y17
M_A_DQ51 Y14
M_A_DQ50 W14
M_A_DQ49 W16
M_A_DQ48 AD17
M_A_DQ47 Y18
M_A_DQ46 AD19
M_A_DQ45 AD21
M_A_DQ44 AB21
M_A_DQ43 AB18
M_A_DQ42 AA18
M_A_DQ41 AA20
M_A_DQ40 Y20
M_A_DQ39 AA22
M_A_DQ38 Y22
M_A_DQ37 W21
M_A_DQ36 W22
M_A_DQ35 AA21
M_A_DQ34 AB22
M_A_DQ33 AB24
M_A_DQ32 Y24
M_A_DQ31 H22
M_A_DQ30 H20
M_A_DQ29 E22
M_A_DQ28 E21
M_A_DQ27 J19
M_A_DQ26 H24
M_A_DQ25 F22
M_A_DQ24 F20
M_A_DQ23 C23
M_A_DQ22 B22
M_A_DQ21 F18
M_A_DQ20 E18
M_A_DQ19 E20
M_A_DQ18 D22
M_A_DQ17 C19
M_A_DQ16 G18
M_A_DQ15 G17
M_A_DQ14 C17
M_A_DQ13 F14
M_A_DQ12 E14
M_A_DQ11 H17
M_A_DQ10 E17
M_A_DQ9 E15
M_A_DQ8 H15
M_A_DQ7 E13
M_A_DQ6 C13
M_A_DQ5 H12
M_A_DQ4 H11
M_A_DQ3 G14
M_A_DQ2 H14
M_A_DQ1 F12
M_A_DQ0 G12
MA_DATA[63:0]
MA_DM[7:0] Y13 AB16 Y19 AC24 F24 E19 C15 E12 M_A_DQM7 M_A_DQM6 M_A_DQM5 M_A_DQM4 M_A_DQM3 M_A_DQM2 M_A_DQM1 M_A_DQM0
MA_DQS[7:0] W12 Y15 AB19 AD23 G22 C22 G16 G13 M_A_DQS7 M_A_DQS6 M_A_DQS5 M_A_DQS4 M_A_DQS3 M_A_DQS2 M_A_DQS1 M_A_DQS0
MA_DQS#[7:0] W13 W15 AB20 AC23 G21 C21 G15 H13 M_A_DQS#7 M_A_DQS#6 M_A_DQS#5 M_A_DQS#4 M_A_DQS#3 M_A_DQS#2 M_A_DQS#1 M_A_DQS#0
MA0_CLK[1] E16 M_A_CLK1
MA0_CLK#[1] F16 M_A_CLK1#
MA0_CLK[2] Y16 M_A_CLK2
MA0_CLK#[2] AA16 M_A_CLK2#
Tolerance is +-10%
C103 1.5P/50V/O
C110 1.5P/50V/O
M_A_CLK1 [5]
M_A_CLK1# [5]
M_A_CLK2 [5]
M_A_CLK2# [5]
TRACE FROM CAP TO CPU MUST BE LESS THAN 1200MILS MAX NECKDOWN TO & FROM CAPS IS 500MILS
MA_BANK[2:0] K22 R20 T22 M_A_BA2 M_A_BA1 M_A_BA0
MA_RAS# T20 M_A_RAS#
MA_CAS# U20 M_A_CAS#
MA_WE# U21 M_A_WE#
MA_ADD[15:0]
M_A_A15 K19
M_A_A14 K20
M_A_A13 V24
M_A_A12 K24
M_A_A11 L20
M_A_A10 R19
M_A_A9 L19
M_A_A8 L22
M_A_A7 L21
M_A_A6 M19
M_A_A5 M20
M_A_A4 M24
M_A_A3 M22
M_A_A2 N22
M_A_A1 N21
M_A_A0 R21
MA0_CS#[3:0] V19 J22 V22 T19 M_A_CS#3 M_A_CS#2 M_A_CS#1 M_A_CS#0
MA_CKE[1:0] J20 J21 M_A_CKE1 M_A_CKE0
MA0_ODT[1:0] V20 U19 M_A_ODT1 M_A_ODT0
AMD S1 SOCKET
U27C
M_B_DQ63 AD11
M_B_DQ62 AE11
M_B_DQ61 AE14
M_B_DQ60 AE14
M_B_DQ59 Y11
M_B_DQ58 AB11
M_B_DQ57 AC12
M_B_DQ56 AE13
M_B_DQ55 AE15
M_B_DQ54 AE16
M_B_DQ53 AC18
M_B_DQ52 AF19
M_B_DQ51 AD14
M_B_DQ50 AC14
M_B_DQ49 AE18
M_B_DQ48 AD18
M_B_DQ47 AD20
M_B_DQ46 AC20
M_B_DQ45 AE23
M_B_DQ44 AE24
M_B_DQ43 AE20
M_B_DQ42 AE20
M_B_DQ41 AD22
M_B_DQ40 AC22
M_B_DQ39 AE25
M_B_DQ38 AD26
M_B_DQ37 AA25
M_B_DQ36 AA26
M_B_DQ35 AE24
M_B_DQ34 AD24
M_B_DQ33 AA23
M_B_DQ32 AA24
M_B_DQ31 G24
M_B_DQ30 G23
M_B_DQ29 D26
M_B_DQ28 C26
M_B_DQ27 G26
M_B_DQ26 G25
M_B_DQ25 E24
M_B_DQ24 E23
M_B_DQ23 C24
M_B_DQ22 B24
M_B_DQ21 C20
M_B_DQ20 B20
M_B_DQ19 C25
M_B_DQ18 D24
M_B_DQ17 A21
M_B_DQ16 D20
M_B_DQ15 D18
M_B_DQ14 C18
M_B_DQ13 D14
M_B_DQ12 C14
M_B_DQ11 A20
M_B_DQ10 A19
M_B_DQ9 A16
M_B_DQ8 A15
M_B_DQ7 A13
M_B_DQ6 D12
M_B_DQ5 E11
M_B_DQ4 G11
M_B_DQ3 B14
M_B_DQ2 A14
M_B_DQ1 A11
M_B_DQ0 C11
MB_DATA[63:0]
MB_DM[7:0] AD12 AC16 AF22 AB26 E25 A22 B16 A12 M_B_DQM7 M_B_DQM6 M_B_DQM5 M_B_DQM4 M_B_DQM3 M_B_DQM2 M_B_DQM1 M_B_DQM0
MB_DQS[7:0] AF12 AE16 AF21 AC25 F26 A24 D16 C12 M_B_DQS7 M_B_DQS6 M_B_DQS5 M_B_DQS4 M_B_DQS3 M_B_DQS2 M_B_DQS1 M_B_DQS0
MB_DQS#[7:0] AE12 AD16 AF22 AC26 E26 A23 C16 B12 M_B_DQS#7 M_B_DQS#6 M_B_DQS#5 M_B_DQS#4 M_B_DQS#3 M_B_DQS#2 M_B_DQS#1 M_B_DQS#0
MB0_CLK[1] A17 M_B_CLK1
MB0_CLK#[1] A18 M_B_CLK1#
MB0_CLK[2] AF18 M_B_CLK2
MB0_CLK#[2] AF17 M_B_CLK2#
Tolerance is +-10%
C122 1.5P/50V/O
C121 1.5P/50V/O
M_B_CLK1 [5]
M_B_CLK1# [5]
M_B_CLK2 [5]
M_B_CLK2# [5]
TRACE FROM CAP TO CPU MUST BE LESS THAN 1200MILS MAX NECKDOWN TO & FROM CAPS IS 500MILS
MB_BANK[2:0] K26 T26 U26 M_B_BA2 M_B_BA1 M_B_BA0
MB_RAS# U24 M_B_RAS#
MB_CAS# V26 M_B_CAS#
MB_WE# U22 M_B_WE#
MB_ADD[15:0]
M_B_A15 J25
M_B_A14 J26
M_B_A13 W25
M_B_A12 L23
M_B_A11 L25
M_B_A10 U25
M_B_A9 L24
M_B_A8 M26
M_B_A7 L26
M_B_A6 N23
M_B_A5 N24
M_B_A4 N25
M_B_A3 N26
M_B_A2 P24
M_B_A1 P26
M_B_A0 T24
MB0_CS#[3:0] Y26 J24 W24 U23 M_B_CS#3 M_B_CS#2 M_B_CS#1 M_B_CS#0
MB_CKE[1:0] H26 J23 M_B_CKE1 M_B_CKE0
MB0_ODT[1:0] W23 W26 M_B_ODT1 M_B_ODT0
VTT_SENSE Y10 VTERM_FB
VTERM_FB [37]
M_VREF W17 M_VREF
M_ZN AE10 MEMZN R581 39.2/F
M_ZP AF10 MEMZP R586 39.2/F
1.8VSUS
R80 2K/F
R78 2K/F
C106 1000P/50V/X
C120 0.1U/16V/V
M_VREF : W =20MIL AND SPACE = 20MIL
AMD S1 SOCKET
[5] M_A_DQ[0..63] M_A_DQ[0..63]
[4,5] M_A_A[0..15] M_A_A[0..15]
[5] M_A_DQM[0..7] M_A_DQM[0..7]
[5] M_A_DQS[0..7] M_A_DQS[0..7]
[5] M_A_DQS#[0..7] M_A_DQS#[0..7]
[4,5] M_A_BA[0..2] M_A_BA[0..2]
[4,5] M_A_CS#[0..3] M_A_CS#[0..3]
M_A_RAS# M_A_CAS# M_A_WE# M_A_RAS# [4,5] M_A_CAS# [4,5] M_A_WE# [4,5]
M_A_CKE[0..1] M_A_CKE[0..1] [4,5]
M_A_ODT[0..1] M_A_ODT[0..1] [4,5]
[5] M_B_DQ[0..63] M_B_DQ[0..63]
[4,5] M_B_A[0..15] M_B_A[0..15]
[5] M_B_DQM[0..7] M_B_DQM[0..7]
[5] M_B_DQS[0..7] M_B_DQS[0..7]
[5] M_B_DQS#[0..7] M_B_DQS#[0..7]
[4,5] M_B_BA[0..2] M_B_BA[0..2]
[4,5] M_B_CS#[0..3] M_B_CS#[0..3]
M_B_RAS# M_B_CAS# M_B_WE# M_B_RAS# [4,5] M_B_CAS# [4,5] M_B_WE# [4,5]
M_B_CKE[0..1] M_B_CKE[0..1] [4,5]
M_B_ODT[0..1] M_B_ODT[0..1] [4,5]
1.8VSUS [2,4,5,6,32,36,37]
NB5/RD2/HW1
PROJECT : AT1
Quanta Computer Inc.
Size Custom
Document Number CPU (MEM_I/F)
Rev MV
Date: Tuesday, August 21, 2007
Sheet 3 of 40

CPU POWER PLANE AND BY PASS CAP

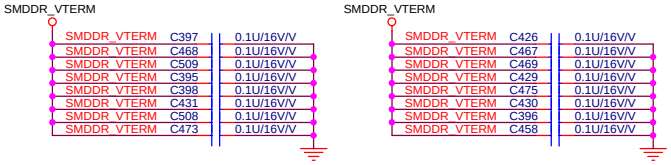


DDR2 TERMINATION BYPASS CAP

04

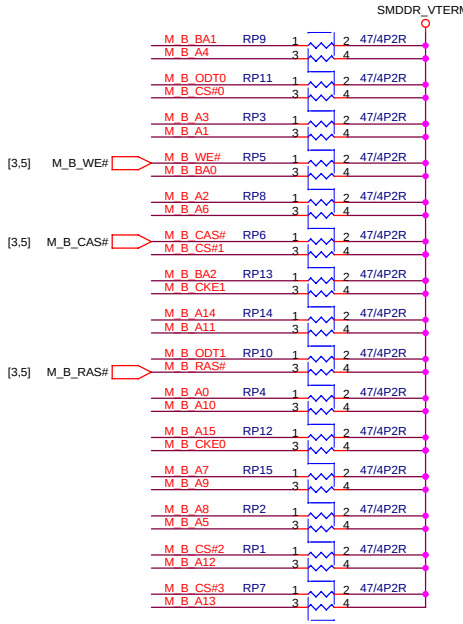
CHANNEL A

CHANNEL B

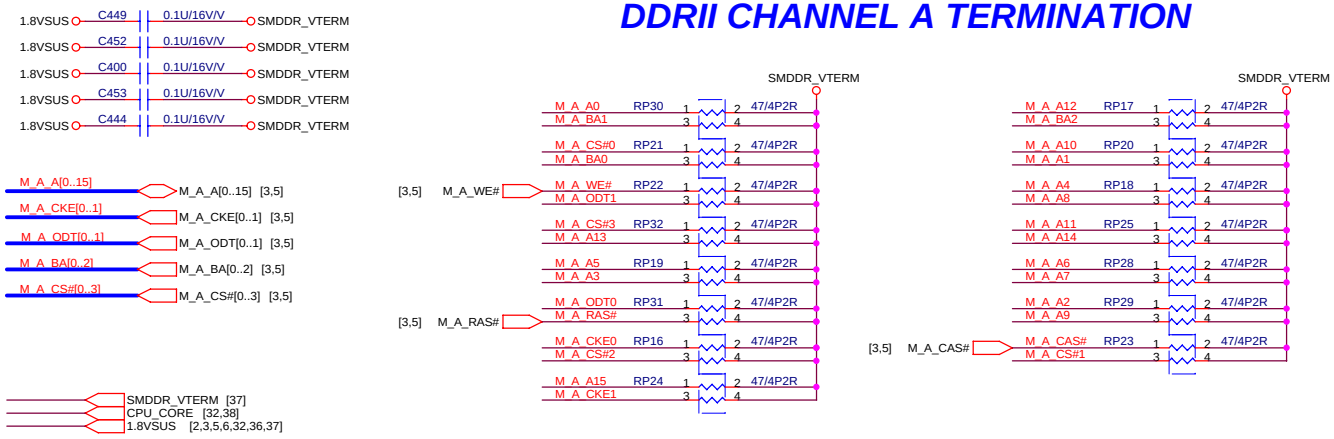


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

DDRII CHANNEL B TERMINATION



DDRII CHANNEL A TERMINATION



PROJECT :	AT1
	Quanta Computer Inc.
Size: Custom	Document Number: CPU (POWER,GND),DDR2_TERM
Rev: MV	
NB5/RD2/HW1	Date: Tuesday, August 21, 2007
	Sheet 4 of 40

M_A_RAS# M_A_CAS# M_A_WE# → M_A_RAS# [3,4] M_A_CAS# [3,4] M_A_WE# [3,4]
M_A_CLK1 M_A_CLK1# M_A_CLK2 M_A_CLK2# → M_A_CLK1 [3] M_A_CLK1# [3] M_A_CLK2 [3] M_A_CLK2# [3]
M_A_BA[0..2] → M_A_BA[0..2] [3,4]
M_A_CS#[0..3] → M_A_CS#[0..3] [3,4]
M_A_CKE[0..1] → M_A_CKE[0..1] [3,4]
M_A_ODT[0..1] → M_A_ODT[0..1] [3,4]
M_A_DQ[0..63] → M_A_DQ[0..63] [3]
M_A_A[15..0] → M_A_A[15..0] [3,4]
M_A_DQM[0..7] → M_A_DQM[0..7] [3]
M_A_DQS[0..7] → M_A_DQS[0..7] [3]
M_A_DQS#[0..7] → M_A_DQS#[0..7] [3]

M_B_RAS# M_B_CAS# M_B_WE# → M_B_RAS# [3,4] M_B_CAS# [3,4] M_B_WE# [3,4]
M_B_CLK1 M_B_CLK1# M_B_CLK2 M_B_CLK2# → M_B_CLK1 [3] M_B_CLK1# [3] M_B_CLK2 [3] M_B_CLK2# [3]
M_B_BA[0..2] → M_B_BA[0..2] [3,4]
M_B_CS#[0..3] → M_B_CS#[0..3] [3,4]
M_B_CKE[0..1] → M_B_CKE[0..1] [3,4]
M_B_ODT[0..1] → M_B_ODT[0..1] [3,4]
M_B_DQ[0..63] → M_B_DQ[0..63] [3]
M_B_A[0..15] → M_B_A[0..15] [3,4]
M_B_DQM[0..7] → M_B_DQM[0..7] [3]
M_B_DQS[0..7] → M_B_DQS[0..7] [3]
M_B_DQS#[0..7] → M_B_DQS#[0..7] [3]

CKE 0,1

CN28A
2-1734073-1
PC2100 DDR2 SDRAM SO-DIMM (200P)
HEIGHT=9.2mm

M_A_DQ5	5	DQ0	DQ32	123	M_A_DQ32		
M_A_DQ1	7	DQ1	DQ33	125	M_A_DQ36		
M_A_DQ2	17	DQ2	DQ34	135	M_A_DQ34		
M_A_DQ3	19	DQ3	DQ35	137	M_A_DQ37		
M_A_DQ0	4	DQ4	DQ36	124	M_A_DQ33		
M_A_DQ4	6	DQ5	DQ37	126	M_A_DQ38		
M_A_DQ6	14	DQ6	DQ38	134	M_A_DQ39		
M_A_DQ7	16	DQ7	DQ39	136	M_A_DQ35		
M_A_DQ9	23	DQ8	DQ40	141	M_A_DQ40		
M_A_DQ8	25	DQ9	DQ41	143	M_A_DQ41		
M_A_DQ10	35	DQ10	DQ42	151	M_A_DQ42		
M_A_DQ14	37	DQ11	DQ43	153	M_A_DQ46		
M_A_DQ13	20	DQ12	DQ44	140	M_A_DQ44		
M_A_DQ12	22	DQ13	DQ45	142	M_A_DQ45		
M_A_DQ15	36	DQ14	DQ46	152	M_A_DQ43		
M_A_DQ11	38	DQ15	DQ47	154	M_A_DQ47		
M_A_DQ17	43	DQ16	DQ48	157	M_A_DQ55		
M_A_DQ21	45	DQ17	DQ49	159	M_A_DQ54		
M_A_DQ18	55	DQ18	DQ50	173	M_A_DQ49		
M_A_DQ16	57	DQ19	DQ51	175	M_A_DQ52		
M_A_DQ20	44	DQ20	DQ52	158	M_A_DQ48		
M_A_DQ19	46	DQ21	DQ53	160	M_A_DQ53		
M_A_DQ22	56	DQ22	DQ54	174	M_A_DQ50		
M_A_DQ23	58	DQ23	DQ55	176	M_A_DQ51		
M_A_DQ24	61	DQ24	DQ56	179	M_A_DQ57		
M_A_DQ25	63	DQ25	DQ57	181	M_A_DQ61		
M_A_DQ27	73	DQ26	DQ58	189	M_A_DQ63		
M_A_DQ30	75	DQ27	DQ59	191	M_A_DQ62		
M_A_DQ28	62	DQ28	DQ60	180	M_A_DQ56		
M_A_DQ29	64	DQ29	DQ61	182	M_A_DQ60		
M_A_DQ26	74	DQ30	DQ62	192	M_A_DQ59		
M_A_DQ31	76	DQ31	DQ63	194	M_A_DQ58		
M_A_A0	102	A0	DM0	10	M_A_DQM0		
M_A_A1	101	A1	DM1	26	M_A_DQM1		
M_A_A2	100	A2	DM2	52	M_A_DQM2		
M_A_A3	99	A3	DM3	67	M_A_DQM3		
M_A_A4	98	A4	DM4	130	M_A_DQM4		
M_A_A5	97	A5	DM5	147	M_A_DQM5		
M_A_A6	94	A6	DM6	170	M_A_DQM6		
M_A_A7	92	A7	DM7	185	M_A_DQM7		
M_A_A8	93	A8	DQS0	13	M_A_DQS0		
M_A_A9	91	A9	DQS0	11	M_A_DQS#0		
M_A_A10	105	A10/AP	DQS1	31	M_A_DQS1		
M_A_A11	90	A11	DQS1	29	M_A_DQS#1		
M_A_A12	89	A12	DQS2	51	M_A_DQS2		
			DQS2	49	M_A_DQS#2		
M_A_BA0	107	BA0	DQS3	70	M_A_DQS3		
M_A_BA1	106	BA1	DQS3	68	M_A_DQS#3		
M_A_BA2	85	NC/BA2	DQS4	131	M_A_DQS4		
			DQS4	129	M_A_DQS#4		
M_A_CLK1	30		DQS5	148	M_A_DQS5		
M_A_CLK1#	32	CLK0	DQS5	146	M_A_DQS#5		
		CLK0	DQS6	169	M_A_DQS6		
M_A_CLK2	164		DQS6	167	M_A_DQS#6		
M_A_CLK2#	166	CLK1	DQS7	188	M_A_DQS7		
		CKL1	DQS7	186	M_A_DQS#7		
DDR_SMBCLK	197	SCL					
DDR_SMBDTA	195	SDA	CS0	110	M_A_CS#0		
DIM1_SA0	198	SA0	CS1	115	M_A_CS#1		
DIM1_SA1	200	SA1	RAS	108	M_A_RAS#		
			CAS	113	M_A_CAS#		
3V	199	VDDSPD	WE	109	M_A_WE#		
			CKE0	79	M_A_CKE0		
			CKE1	80	M_A_CKE1		

R320 10K DIM1_SA0
R321 10K DIM1_SA1
SMbus address A0

Q13 2N7002E
DDR_SMBDTA 1 3 CGDAT_SMB [10]
2 3V

Q11 2N7002E
DDR_SMBCLK 1 3 CGCLK_SMB [10]
2 3V

CKE 2,3

CN26A
1565917-4
PC2100 DDR2 SDRAM SO-DIMM (200P)
HEIGHT=5.2mm

M_B_DQ1	5	DQ0	DQ32	123	M_B_DQ36		
M_B_DQ4	7	DQ1	DQ33	125	M_B_DQ37		
M_B_DQ3	17	DQ2	DQ34	135	M_B_DQ38		
M_B_DQ2	19	DQ3	DQ35	137	M_B_DQ34		
M_B_DQ0	4	DQ4	DQ36	124	M_B_DQ32		
M_B_DQ5	6	DQ5	DQ37	126	M_B_DQ33		
M_B_DQ7	14	DQ6	DQ38	134	M_B_DQ39		
M_B_DQ6	16	DQ7	DQ39	136	M_B_DQ35		
M_B_DQ9	23	DQ8	DQ40	141	M_B_DQ44		
M_B_DQ8	25	DQ9	DQ41	143	M_B_DQ41		
M_B_DQ14	35	DQ10	DQ42	151	M_B_DQ47		
M_B_DQ15	37	DQ11	DQ43	153	M_B_DQ46		
M_B_DQ12	20	DQ12	DQ44	140	M_B_DQ40		
M_B_DQ13	22	DQ13	DQ45	142	M_B_DQ45		
M_B_DQ10	36	DQ14	DQ46	152	M_B_DQ42		
M_B_DQ11	38	DQ15	DQ47	154	M_B_DQ43		
M_B_DQ17	43	DQ16	DQ48	157	M_B_DQ55		
M_B_DQ20	45	DQ17	DQ49	159	M_B_DQ54		
M_B_DQ19	55	DQ18	DQ50	173	M_B_DQ53		
M_B_DQ18	57	DQ19	DQ51	175	M_B_DQ48		
M_B_DQ16	44	DQ20	DQ52	158	M_B_DQ51		
M_B_DQ21	46	DQ21	DQ53	160	M_B_DQ50		
M_B_DQ22	56	DQ22	DQ54	174	M_B_DQ49		
M_B_DQ23	58	DQ23	DQ55	176	M_B_DQ52		
M_B_DQ24	61	DQ24	DQ56	179	M_B_DQ57		
M_B_DQ25	63	DQ25	DQ57	181	M_B_DQ60		
M_B_DQ30	73	DQ26	DQ58	189	M_B_DQ62		
M_B_DQ31	75	DQ27	DQ59	191	M_B_DQ59		
M_B_DQ28	62	DQ28	DQ60	180	M_B_DQ61		
M_B_DQ29	64	DQ29	DQ61	182	M_B_DQ56		
M_B_DQ27	74	DQ30	DQ62	192	M_B_DQ58		
M_B_DQ26	76	DQ31	DQ63	194	M_B_DQ63		
M_B_A0	102	A0	DM0	10	M_B_DQM0		
M_B_A1	101	A1	DM1	26	M_B_DQM1		
M_B_A2	100	A2	DM2	52	M_B_DQM2		
M_B_A3	99	A3	DM3	67	M_B_DQM3		
M_B_A4	98	A4	DM4	130	M_B_DQM4		
M_B_A5	97	A5	DM5	147	M_B_DQM5		
M_B_A6	94	A6	DM6	170	M_B_DQM6		
M_B_A7	92	A7	DM7	185	M_B_DQM7		
M_B_A8	93	A8	DQS0	13	M_B_DQS0		
M_B_A9	91	A9	DQS0	11	M_B_DQS#0		
M_B_A10	105	A10/AP	DQS1	31	M_B_DQS1		
M_B_A11	90	A11	DQS1	29	M_B_DQS#1		
M_B_A12	89	A12	DQS2	51	M_B_DQS2		
			DQS2	49	M_B_DQS#2		
M_B_BA0	107	BA0	DQS3	70	M_B_DQS3		
M_B_BA1	106	BA1	DQS3	68	M_B_DQS#3		
M_B_BA2	85	NC/BA2	DQS4	131	M_B_DQS4		
			DQS4	129	M_B_DQS#4		
M_B_CLK1	30		DQS5	148	M_B_DQS5		
M_B_CLK1#	32	CLK0	DQS5	146	M_B_DQS#5		
		CLK0	DQS6	169	M_B_DQS6		
M_B_CLK2	164		DQS6	167	M_B_DQS#6		
M_B_CLK2#	166	CLK1	DQS7	188	M_B_DQS7		
		CKL1	DQS7	186	M_B_DQS#7		
DDR_SMBCLK	197	SCL					
DDR_SMBDTA	195	SDA	CS0	110	M_B_CS#0		
DIM2_SA0	198	SA0	CS1	115	M_B_CS#1		
DIM2_SA1	200	SA1	RAS	108	M_B_RAS#		
			CAS	113	M_B_CAS#		
3V	199	VDDSPD	WE	109	M_B_WE#		
			CKE0	79	M_B_CKE0		
			CKE1	80	M_B_CKE1		

DIM2_SA0 R280 10K
DIM2_SA1 R266 10K
3V
SMbus address A2

DDR_SMBDTA R281 2.2K 3V
DDR_SMBCLK R282 2.2K

SMDDR_VREF_DIM 1 → VREF
C526 C819 C840 C813 C815 C402 C817 C821 C822 C824 C816: 2.2UA/6.3V/R 1.8VSUS 81 / 2.2UA/6.3V/R 1.8VSUS 82 / 2.2UA/6.3V/R 1.8VSUS 87 / 0.1U/16V/V 1.8VSUS 88 / 0.1U/16V/V 1.8VSUS 95 / 0.1U/16V/V 1.8VSUS 96 / 0.1U/16V/V 1.8VSUS 103 / 0.1U/16V/V 1.8VSUS 104 / 0.1U/16V/V 1.8VSUS 111 / 0.1U/16V/V 1.8VSUS 112 / 0.1U/16V/V 1.8VSUS 117 / 1.8VSUS 118
1.8VSUS
M_A_ODT0 114 M_A_ODT1 119
M_A_CS#2 83 M_A_A15 84 M_A_A14 86 M_A_A13 116 M_A_CS#3 120
50 69 163
162 165 168 171 172 177 178 183 184 187 190 193 196 201
VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12
ODT0 ODT1
NC_1 NC_2 NC_3 NC_4/A15 NC_5/A14 NC_6/A13 NC_7 NC_8
VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58
VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_59
PC2100 DDR2 SDRAM SO-DIMM (200P)
CN28B
2-1734073-1

SMDDR_VREF_DIM 1 → VREF
C820 C818 C466 C838 C839 C836 C835 C401 C450 C823 C837: 2.2UA/6.3V/R 1.8VSUS 81 / 2.2UA/6.3V/R 1.8VSUS 82 / 2.2UA/6.3V/R 1.8VSUS 87 / 0.1U/16V/V 1.8VSUS 88 / 0.1U/16V/V 1.8VSUS 95 / 0.1U/16V/V 1.8VSUS 96 / 0.1U/16V/V 1.8VSUS 103 / 0.1U/16V/V 1.8VSUS 104 / 0.1U/16V/V 1.8VSUS 111 / 0.1U/16V/V 1.8VSUS 112 / 0.1U/16V/V 1.8VSUS 117 / 1.8VSUS 118
1.8VSUS
M_B_ODT0 114 M_B_ODT1 119
M_B_CS#2 83 M_B_A15 84 M_B_A14 86 M_B_A13 116 M_B_CS#3 120
50 69 163
162 165 168 171 172 177 178 183 184 187 190 193 196 201
VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12
ODT0 ODT1
NC_1 NC_2 NC_3 NC_4/A15 NC_5/A14 NC_6/A13 NC_7 NC_8
VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58
VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_59
PC2100 DDR2 SDRAM SO-DIMM (200P)
CN26B
1565917-4

SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

Close DDR2 socket
3V
C520 0.1U/16V/V 3V
C483 2.2UA/6.3V/R 3V
C507 *2.2UA/6.3V/R
C463 0.1U/16V/V

SMDDR_VREF_DIM R259 *0R SMDDR_VREF [37]
R258 2K/F R253 2K/F 1.8VSUS
C474 0.1U/16V/V C407 2.2UA/6.3V/R
SMDDR_VREF_DIM C457 0.1U/16V/V
SMDDR_VREF_DIM C472 2.2UA/6.3V/R

SMDDR_VREF_DIM :
TRACE WIDTH > 20 MIL
PUT BYPASS CAP ON EACH DIMM

Address:92h
U34 *G751 (LM75CIMM3)
3V
A0 A1 A2 SDA SCL +VS O.S GND
C804 *0.1U/16V/V
DIMM_THEM# → DIMM_THEM# [2]
[2] LM86_SMD
[2] LM86_SMC
LM86_SMD LM86_SMC

3V R673 *10K DIMM_THEM#

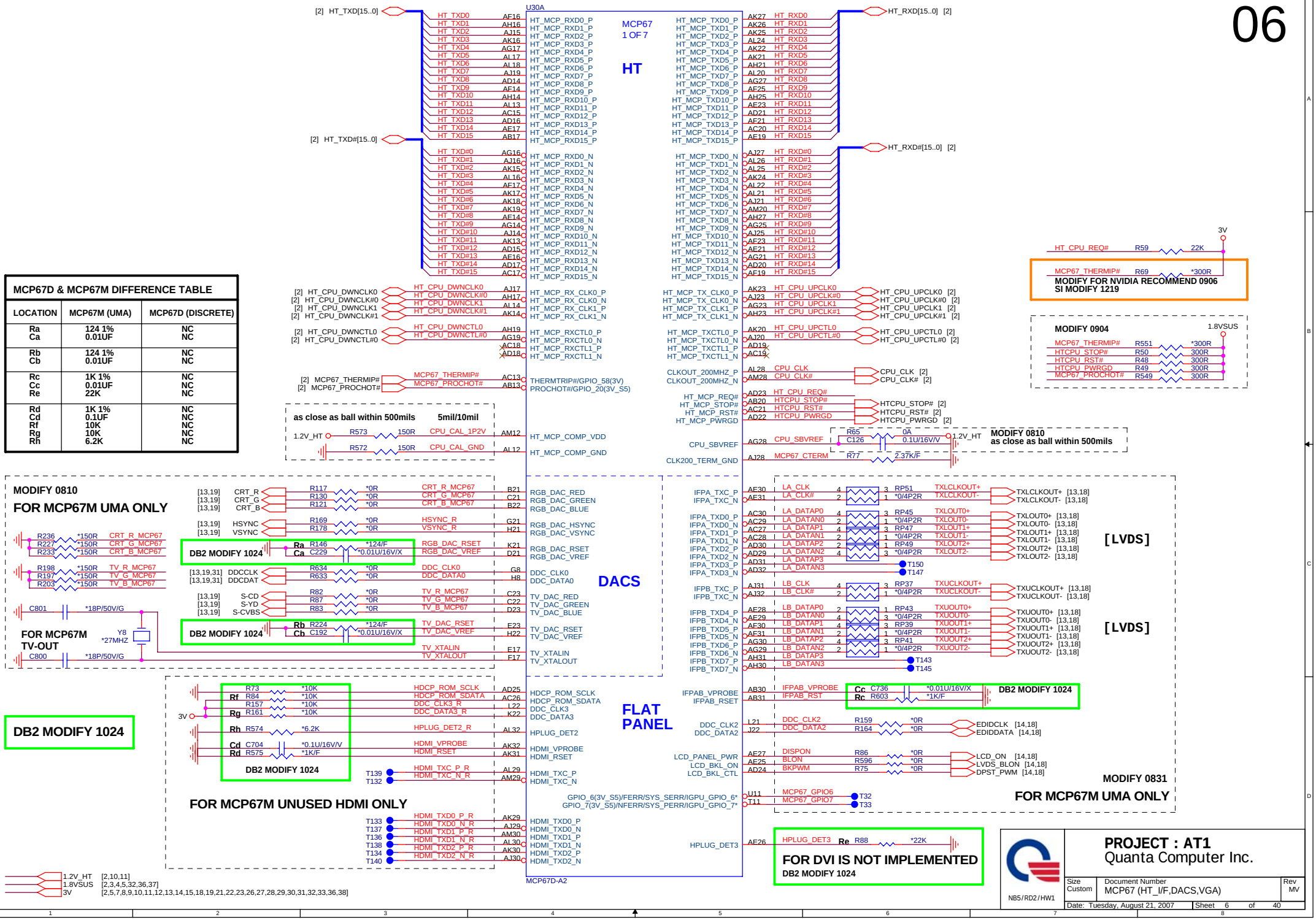
1.8VSUS [2,3,4,6,32,36,37]
3V [2,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR SO-DIMMx2 (200P)	MV
Date: Tuesday, August 21, 2007	Sheet 5 of 40	

MCP67D & MCP67M DIFFERENCE TABLE		
LOCATION	MCP67M (UMA)	MCP67D (DISCRETE)
Ra Ca	124 1% 0.01UF	NC NC
Rb Cb	124 1% 0.01UF	NC NC
Rc Cc Re	1K 1% 0.01UF 22K	NC NC NC
Rd Cd Rf Rg Rh	1K 1% 0.1UF 10K 10K 6.2K	NC NC NC NC NC



C51D SUPPORT PCI-E LANE REVERSE

U30B

MCP67
2 OF 7

PCIE

[12] PEG_RXP[15..0]

PEG_RXP0 F23 PEG_RXP1 F24 PEG_RXP2 D25 PEG_RXP3 C28 PEG_RXP4 C29 PEG_RXP5 D29 PEG_RXP6 F26 PEG_RXP7 F28 PEG_RXP8 H23 PEG_RXP9 H25 PEG_RXP10 H27 PEG_RXP11 K24 PEG_RXP12 K27 PEG_RXP13 K28 PEG_RXP14 J31 PEG_RXP15 K31

[12] PEG_RXN[15..0]

PEG_RXN0 G23 PEG_RXN1 F25 PEG_RXN2 D26 PEG_RXN3 D28 PEG_RXN4 C30 PEG_RXN5 D30 PEG_RXN6 F27 PEG_RXN7 F29 PEG_RXN8 H24 PEG_RXN9 H26 PEG_RXN10 H28 PEG_RXN11 K25 PEG_RXN12 K26 PEG_RXN13 K29 PEG_RXN14 J30 PEG_RXN15 K30

PE0_RX0_P PE0_RX1_P PE0_RX2_P PE0_RX3_P PE0_RX4_P PE0_RX5_P PE0_RX6_P PE0_RX7_P PE0_RX8_P PE0_RX9_P PE0_RX10_P PE0_RX11_P PE0_RX12_P PE0_RX13_P PE0_RX14_P PE0_RX15_P

PE0_RX0_N PE0_RX1_N PE0_RX2_N PE0_RX3_N PE0_RX4_N PE0_RX5_N PE0_RX6_N PE0_RX7_N PE0_RX8_N PE0_RX9_N PE0_RX10_N PE0_RX11_N PE0_RX12_N PE0_RX13_N PE0_RX14_N PE0_RX15_N

PE0_TX0_P PE0_TX1_P PE0_TX2_P PE0_TX3_P PE0_TX4_P PE0_TX5_P PE0_TX6_P PE0_TX7_P PE0_TX8_P PE0_TX9_P PE0_TX10_P PE0_TX11_P PE0_TX12_P PE0_TX13_P PE0_TX14_P PE0_TX15_P

D24 C_PEG_TXP0 A24 C_PEG_TXP1 B25 C_PEG_TXP2 B26 C_PEG_TXP3 C27 C_PEG_TXP4 A28 C_PEG_TXP5 A29 C_PEG_TXP6 A30 C_PEG_TXP7 B31 C_PEG_TXP8 C31 C_PEG_TXP9 D31 C_PEG_TXP10 E31 C_PEG_TXP11 F31 C_PEG_TXP12 G29 C_PEG_TXP13 H29 C_PEG_TXP14 H32 C_PEG_TXP15

C789 0.1U/16V/V PEG_TXP_C0 C774 0.1U/16V/V PEG_TXP_C1 C791 0.1U/16V/V PEG_TXP_C2 C776 0.1U/16V/V PEG_TXP_C3 C793 0.1U/16V/V PEG_TXP_C4 C778 0.1U/16V/V PEG_TXP_C5 C795 0.1U/16V/V PEG_TXP_C6 C780 0.1U/16V/V PEG_TXP_C7 C797 0.1U/16V/V PEG_TXP_C8 C782 0.1U/16V/V PEG_TXP_C9 C784 0.1U/16V/V PEG_TXP_C10 C771 0.1U/16V/V PEG_TXP_C11 C767 0.1U/16V/V PEG_TXP_C12 C760 0.1U/16V/V PEG_TXP_C13 C755 0.1U/16V/V PEG_TXP_C14 C753 0.1U/16V/V PEG_TXP_C15

PEG_TXP_C[15..0] [12]

C24 C_PEG_TXN0 B24 C_PEG_TXN1 C25 C_PEG_TXN2 C26 C_PEG_TXN3 D27 C_PEG_TXN4 B28 C_PEG_TXN5 B29 C_PEG_TXN6 B30 C_PEG_TXN7 B32 C_PEG_TXN8 C32 C_PEG_TXN9 D32 C_PEG_TXN10 E30 C_PEG_TXN11 F30 C_PEG_TXN12 G30 C_PEG_TXN13 H30 C_PEG_TXN14 H31 C_PEG_TXN15

C790 0.1U/16V/V PEG_TXN_C0 C775 0.1U/16V/V PEG_TXN_C1 C792 0.1U/16V/V PEG_TXN_C2 C777 0.1U/16V/V PEG_TXN_C3 C794 0.1U/16V/V PEG_TXN_C4 C779 0.1U/16V/V PEG_TXN_C5 C796 0.1U/16V/V PEG_TXN_C6 C781 0.1U/16V/V PEG_TXN_C7 C798 0.1U/16V/V PEG_TXN_C8 C783 0.1U/16V/V PEG_TXN_C9 C785 0.1U/16V/V PEG_TXN_C10 C770 0.1U/16V/V PEG_TXN_C11 C764 0.1U/16V/V PEG_TXN_C12 C757 0.1U/16V/V PEG_TXN_C13 C754 0.1U/16V/V PEG_TXN_C14 C751 0.1U/16V/V PEG_TXN_C15

PEG_TXN_C[15..0] [12]

FOR USED NB8X ONLY

IF NOT USED, LEAVE NC

MCP67D & MCP67M DIFFERENCE TABLE			
LOCATION	MCP67M (UMA)	MCP67M (DISCRETE)	MCP67D (DISCRETE)
Ra	NC	0R	0R
Rb Rc	NC NC	22R 22R	22R 22R

NET NAME	MCP67D (DISCRETE)	MCP67M (GPU)
PE0_PRSNTX16	LOW	NC

IF NOT USED NB8X, LEAVE NC

[G7xM/NB8X]

[12] CLK_PCIE_VGA
[12] CLK_PCIE_VGA#

Rb R649 22R
Rc R648 22R

PE0_REFCLK_P R29 PE0_REFCLK_N R30

PE0_REFCLK_P PE0_REFCLK_N

PE0_PRSNTX1#/DDC_CLK1 PE0_PRSNTX4#/DDC_DATA1 PE0_PRSNTX8#/EXP_EN PE0_PRSNTX16#

U31 PE0_PRSNTX1 U30 PE0_PRSNTX4 U29 PE0_PRSNTX8 U28 PE0_PRSNTX16

Ra R135 0R
R640 *10K
R636 *10K
R108 *10K
R138 *10K
3V

PE0_PRSNTX1#
PE0_PRSNTX4#
PE0_PRSNTX8#
Internal Pull-up

DB2 MODIFY

[NEW CARD]

[28] PCIE_RXP0 [28] PCIE_RXN0 [28] CLK_NEW_OE# [28] CPPE#

PCIE_RXP0 PCIE_RXN0 CLK_NEW_OE# CPPE#

L29 L30 W27 W28

PE1_RX_P PE1_RX_N PEA_CLKREQ# PEA_PRSNT#

PE1_TX_P PE1_TX_N PE1_REFCLK_P PE1_REFCLK_N

M28 PCIE_TXP0_C M29 PCIE_TXN0_C T32 CLK_PCIE_NEW_C_R T31 CLK_PCIE_NEW_C#_R

C171 0.1U/16V/V C175 0.1U/16V/V R647 22R R645 22R

PCIE_TXP0 [28] PCIE_TXN0 [28] CLK_PCIE_NEW_C [28] CLK_PCIE_NEW_C# [28]

[NEW CARD]

[MINI CARD]

[27] PCIE_RXP1 [27] PCIE_RXN1 [27] CLK_MINI_OE#

PCIE_RXP1 PCIE_RXN1 CLK_MINI_OE#

M26 M27 U26 U27

PE2_RX_P PE2_RX_N PEB_CLKREQ# PEB_PRSNT#

PE2_TX_P PE2_TX_N PE2_REFCLK_P PE2_REFCLK_N

M24 PCIE_TXP1_C M25 PCIE_TXN1_C T29 CLK_PCIE_MINI_R T30 CLK_PCIE_MINI#_R

C180 0.1U/16V/V C182 0.1U/16V/V R643 22R R641 22R

PCIE_TXP1 [27] PCIE_TXN1 [27] CLK_PCIE_MINI [27] CLK_PCIE_MINI# [27]

[MINI CARD]

[MINI CARD]

[27] PCIE_RXP2 [27] PCIE_RXN2 [27] CLK_MINI2_OE#

PCIE_RXP2 PCIE_RXN2 CLK_MINI2_OE#

N23 N22 U25 U24

PE3_RX_P PE3_RX_N PEC_CLKREQ# PEC_PRSNT#

PE3_TX_P PE3_TX_N PE3_REFCLK_P PE3_REFCLK_N

M22 PCIE_TXP2_C M23 PCIE_TXN2_C T27 CLK_PCIE_MINI2_R T28 CLK_PCIE_MINI2#_R

C912 *0.1U/16V/V C913 *0.1U/16V/V R801 *22R R802 *22R

PCIE_TXP2 [27] PCIE_TXN2 [27] CLK_PCIE_MINI2 [27] CLK_PCIE_MINI2# [27]

[MINI CARD]
DB2 MODIFY

N30 N31 R22 U23

PE4_RX_P PE4_RX_N PED_CLKREQ#/GPIO_16(3V) PED_PRSNT#

PE4_TX_P PE4_TX_N PE4_REFCLK_P PE4_REFCLK_N

M30 M31 T25 T26

P31 P30 T22 V31

PE5_RX_P PE5_RX_N PEE_CLKREQ#/GPIO_17(3V) PEE_PRSNT#

PE5_TX_P PE5_TX_N PE5_REFCLK_P PE5_REFCLK_N

P29 P28 T23 T24

P26 P27 U22 V30

PE6_RX_P PE6_RX_N PEF_CLKREQ#/GPIO_18(3V) PEF_PRSNT#

PE6_TX_P PE6_TX_N PE6_REFCLK_P PE6_REFCLK_N

P24 P25 P23 R23

DB2 MODIFY

PE_RST# PE_RST1#

W30 PCIE_RST# W29

DB2 MODIFY
PCIE_RST# [12,27,28]

PE_CLK_COMP

V24 PE_COMP R118 *2.37K/F

MV MODIFY 0423

DB2 MODIFY 1025
Ra,Rb IF NOT USED : LEAVE NC (INTERNAL PU)

CLK_MINI2_OE# Rb R811 10K R812 *10K 3V R813 10K

CLK_MINI_OE# Ra R98 *10K 3V

CLK_NEW_OE# R109 *10K 3V

CPPE# R107 *10K

CLOCK BYPASS

C747 *10P/50V/G CLK_PCIE_NEW_C
C746 *10P/50V/G CLK_PCIE_NEW_C#
C750 *10P/50V/G CLK_PCIE_VGA
C749 *10P/50V/G CLK_PCIE_VGA#
C744 *10P/50V/G CLK_PCIE_MINI
C742 *10P/50V/G CLK_PCIE_MINI#

MCP67D-A2

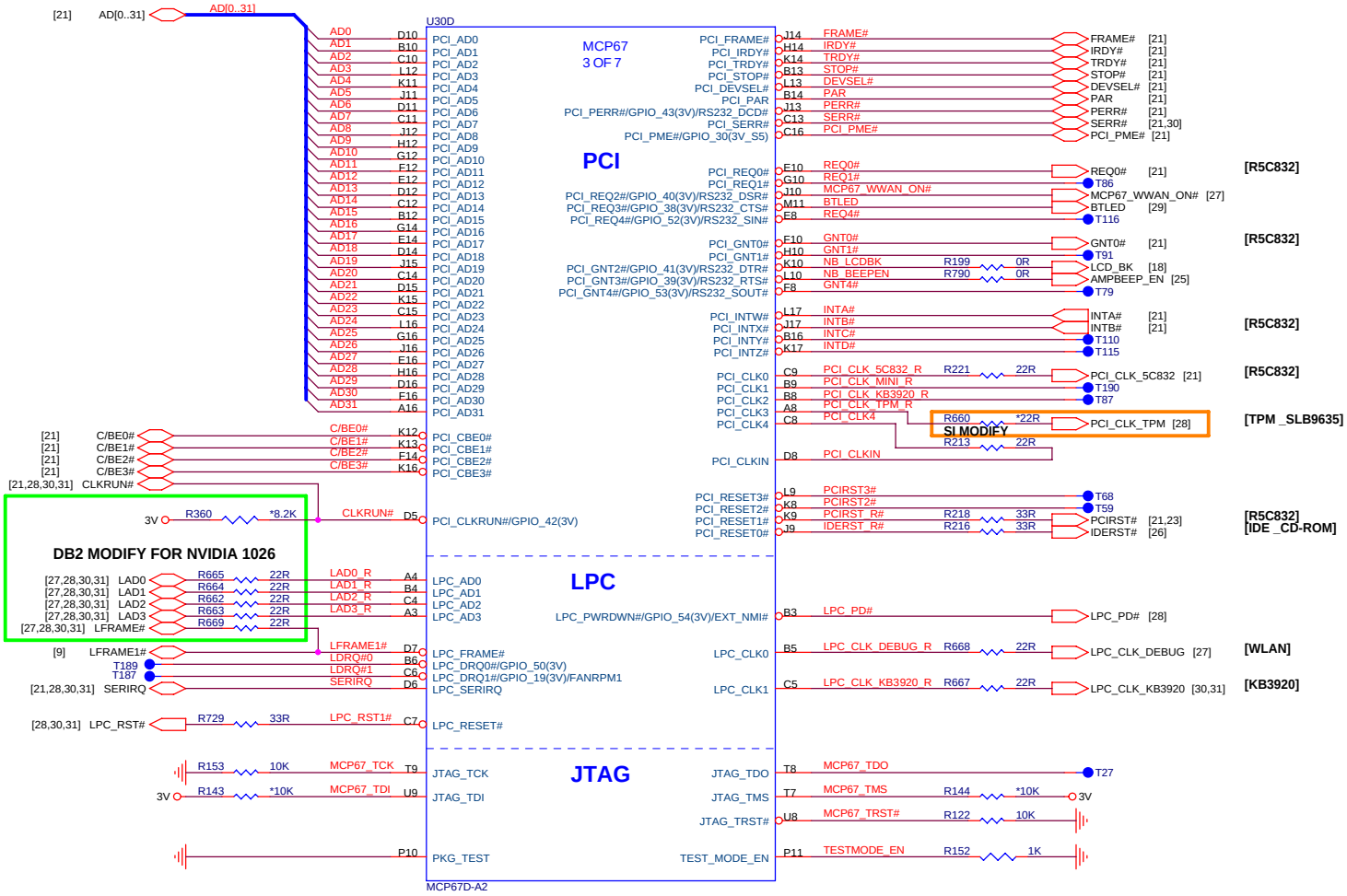
3V [2,5,6,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]

NB5/RD2/HW1

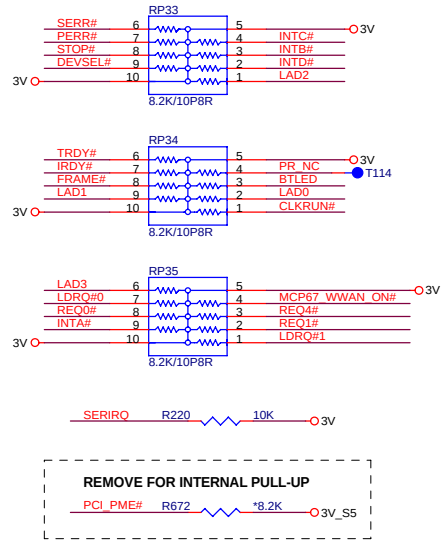
PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MCP67 (PCI-E_I/F)	MV

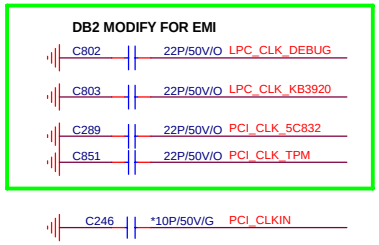
Date: Tuesday, August 21, 2007 Sheet 7 of 40



PCI/LPC PULL-UP



CLOCK BYPASS



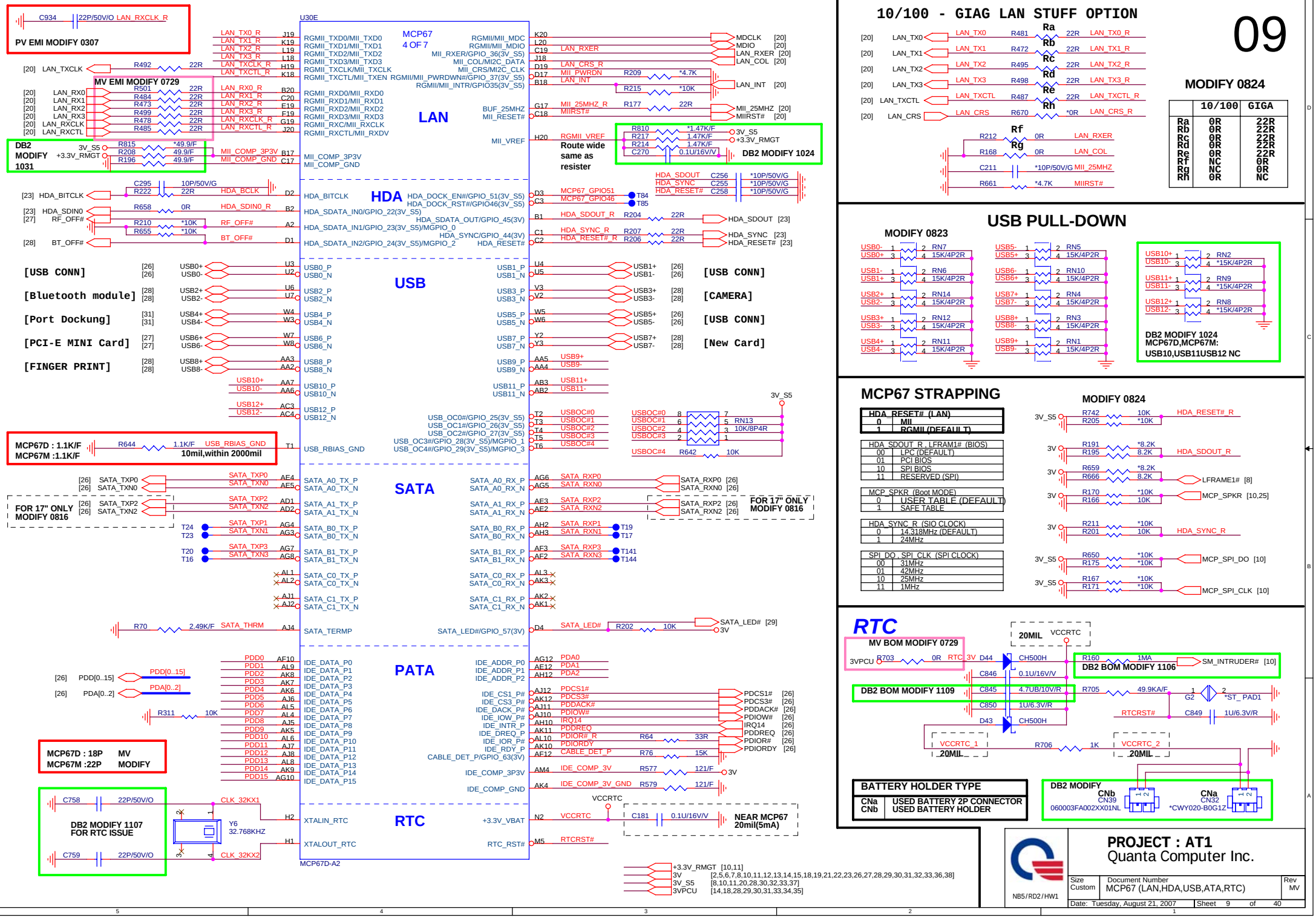
3V [2,5,6,7,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3V_S5 [9,10,11,20,28,30,32,33,37]

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MCP67 (PCI,LPC,JTAG)	MV

NB5/RD2/HW1

Date: Tuesday, August 21, 2007 Sheet 8 of 40



10/100 - GIAG LAN STUFF OPTION

09

	10/100	GIGA
Ra	0R	22R
Rb	0R	22R
Rc	0R	22R
Rd	0R	22R
Re	0R	22R
Rf	NC	0R
Rg	NC	0R
Rh	0R	NC

MODIFY 0824

USB PULL-DOWN

MODIFY 0823

DB2 MODIFY 1024
MCP67D,MCP67M:
USB10,USB11USB12 NC

MCP67 STRAPPING

HDA_RESET# (LAN)	
0	MII
1	RGMII (DEFAULT)

HDA_SDOUT_R , LFRAM1# (BIOS)	
00	LPC (DEFAULT)
01	PCI BIOS
10	SPI BIOS
11	RESERVED (SPI)

MCP_SPKR (Boot MODE)	
0	USER TABLE (DEFAULT)
1	SAFE TABLE

HDA_SYNC_R (SIO CLOCK)	
0	14.318MHz (DEFAULT)
1	24MHz

SPI_DO , SPI_CLK (SPI CLOCK)	
00	31MHz
01	42MHz
10	25MHz
11	1MHz

MODIFY 0824

RTC

MV BOM MODIFY 0729

DB2 BOM MODIFY 1109

DB2 BOM MODIFY 1106

BATTERY HOLDER TYPE	
CNa	USED BATTERY 2P CONNECTOR
CNb	USED BATTERY HOLDER

DB2 MODIFY
CNb CN39 060003FA002XX01NL
CNa CN32 *CWY020-B0G1Z

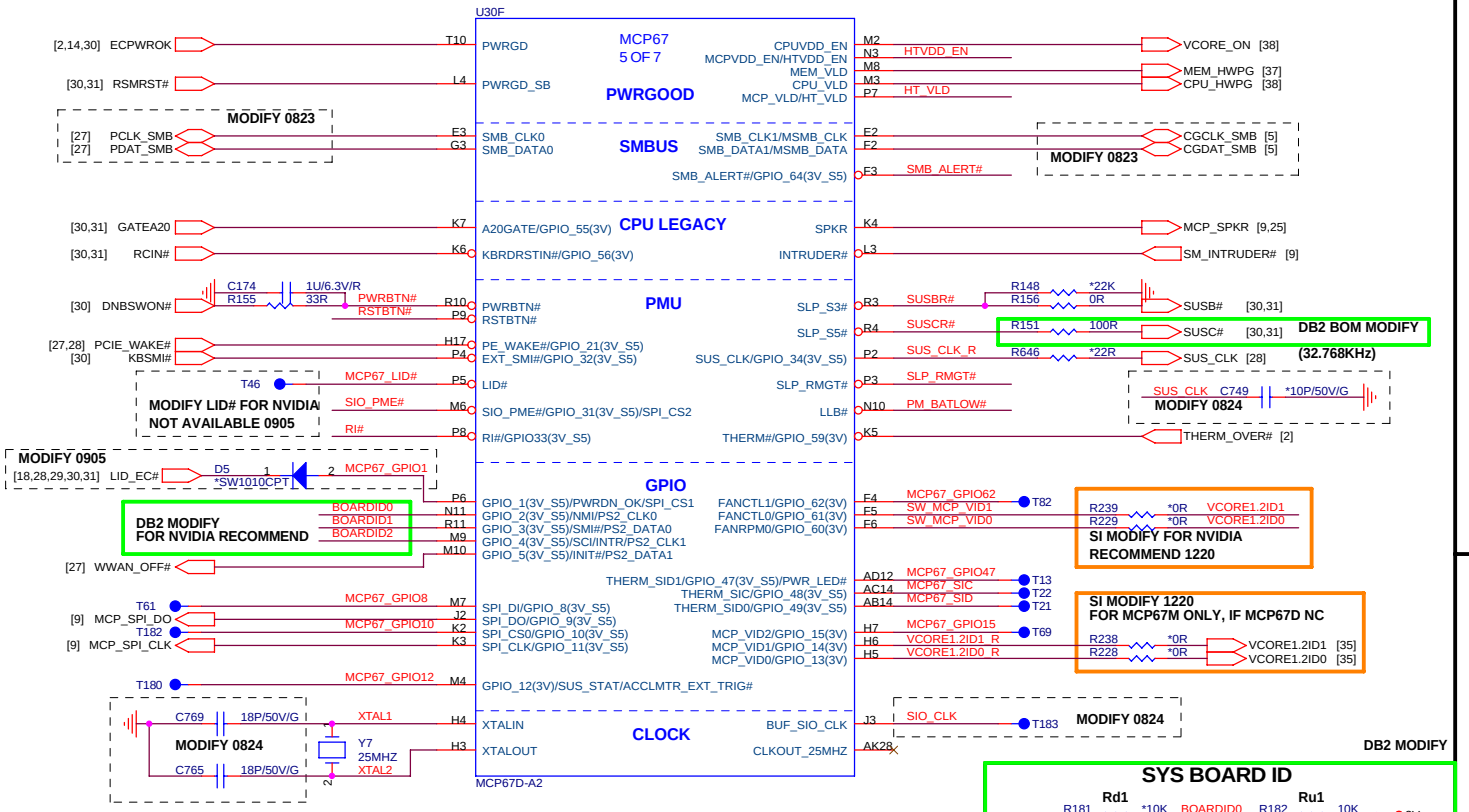
NEAR MCP67 20mil(5mA)

PROJECT : AT1
Quanta Computer Inc.

NB5/RD2/HW1

Size	Document Number	Rev
Custom	MCP67 (LAN,HDA,USB,ATA,RTC)	MV

Date: Tuesday, August 21, 2007 Sheet 9 of 40

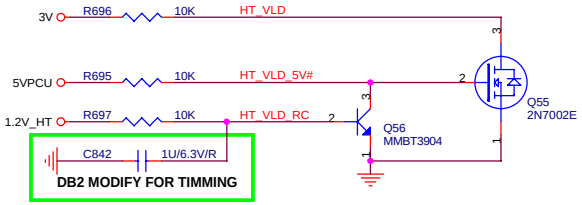


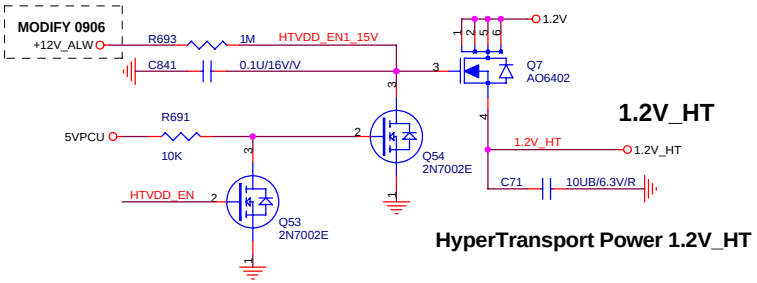
Board ID :	0/1	0/1	0/1
DIFINE	RESERVE / RESERVE	UMA / DISCRETE	AT1 / AT2

	ARES/ARTEMIS 1.0			ARES/ARTEMIS 1.1		
SKU (BOARD ID)	AT1A (UMA)	AT1B (UMA ONLY)	AT2A (UMA)	AT1A (UMA)	AT1B (UMA ONLY)	AT2A (UMA)
Board ID	000	000	001	010	010	011
ID0 STUFF	Rd1	Rd1	Ru1	Rd1	Rd1	Ru1
ID1 STUFF	Rd2	Rd2	Rd2	Ru2	Ru2	Ru2
ID2 STUFF	Rd3	Rd3	Rd3	Rd3	Rd3	Rd3

	SI Setting		PV Setting		ARES/ARTEMIS 1.1	
SKU (BOARD ID)	AT1A (DISCRETE)	AT2A (DISCRETE)	AT1A (DISCRETE)	AT2A (DISCRETE)	AT1A (DISCRETE)	AT2A (DISCRETE)
Board ID	010	111	000	001	010	011
ID0 STUFF	Rd1	Ru1	Rd1	Ru1	Rd1	Ru1
ID1 STUFF	Ru2	Ru2	Rd2	Rd2	Ru2	Ru2
ID2 STUFF	Rd3	Ru3	Rd3	Rd3	Rd3	Rd3

HyperTransport Link 1.2 V_HT Power Valid



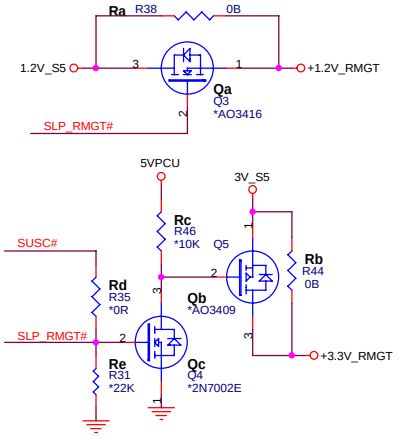


HyperTransport Power 1.2V_HT

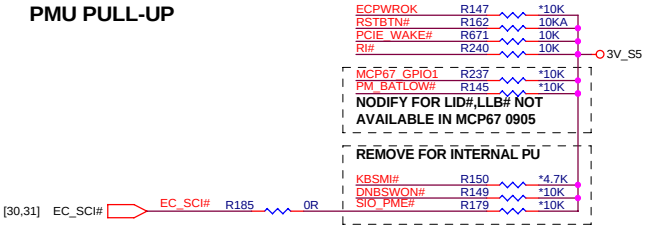
CORE POWER CIRCIUT FOR SLEEP MODE
MCP67M SUPPORT ONLY

10

MCP67M & MCP67D DIFFERENCE TABLE		
	MCP67M UMA	MCP67D DISCRETE
Ra	NC	STUFF
Rb	NC	STUFF
Rc	STUFF	NC
Rd	NC	NC
Re	STUFF	NC
Qa	STUFF	NC
Qb	STUFF	NC
Qc	STUFF	NC

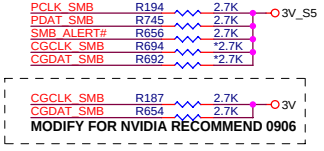


PMU PULL-UP



CPU LEGACY PULL-UP

SMB/I2C PULL-UP



+1.2V_RMGT [11]
1.2V_S5 [11,32,35]
1.2V_HT [2,6,11]
1.2V [11,12,13,15,36]
+3.3V_RMGT [9,11]
3V [2,5,6,7,8,9,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3V_S5 [8,9,11,20,28,30,32,33,37]
5VPCU [23,33,34,35,36,37,38]
+12V_ALW [18,32,33]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MCP67 (PG,SMB,PMU,GPIO,CLK)	MV
Date: Tuesday, August 21, 2007	Sheet 10 of 40	

MCP67 POWER PLANE/GND & BYPASS

4717mA

390mA

242mA

100mA

52mA

1533mA

308mA

75mA

350mA

47mA

15mA

25mA

268mA

52mA

30mA

117mA

8mA

91mA

70mA

15mA

127mA

DB2 BOM MODIFY 1106
FOR LEAD-FREE

DB2 MODIFY 1024

DB2 MODIFY 1024
FOR USED
MCP67M
UMA ONLY

NVIDIA
RECOMMEND

La STUFF
Lb EMPTY
FOR MCP6B

DB2 MODIFY 1024

ONLY FOR MCP67D (DISCRETE)

MCP67 Signal Name	Component
+3VDAC	NC
+1.8V_IFP	NC
+3.3V_HDMI	NC
+3.3V_PLL_IFPP	NC
+3.3V_PLL	NC

TRACE WIDTH / SPACING :

+1.2V_HT_PLL	25mil / 10mil
+3.3V_PLL	25mil / 10mil
+3VDAC	25mil / 10mil
+1.8V_IFP	
+3.3V_HDMI	25mil / 10mil
+3.3V_PLL_IFPP	25mil / 10mil
1.2V_PEA	25mil / 10mil
+1.2V_PED	25mil / 10mil
+1.2V_PLLPE	25mil / 10mil
+1.2V_PLLPE_SS	25mil / 10mil
+1.2V_SP_D	25mil / 10mil
+1.2V_SP_A	25mil / 10mil
+1.2V_PLL_SP_VDD	
+1.2V_PLL_SP_SS	25mil / 10mil
+1.2V_RMGT	
+3.3V_RMGT	
+3.3V_PLL_MAC_DUAL	
+3.3V_USB_DUAL	25mil / 10mil
1.2V_DUAL	25mil / 10mil
+3V_DUAL	25mil / 10mil
+1.2V_RBB	25mil / 10mil

3V [2,5,6,7,8,9,10,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3V_S5 [8,9,10,20,28,30,32,33,37]
+3.3V_RMGT [9,10]
1.8V [13,15,16,17,32,37]
1.2V_VCORE [35,36]
1.2V [10,12,13,15,36]
1.2V_HT [2,6,10]
1.2V_S5 [10,32,35]
+1.2V_RMGT [10]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MCP67 (POWER,GND)	MV

Date: Tuesday, August 21, 2007 Sheet 11 of 40

U33F

GND_0 GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16 GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_25 GND_26 GND_27 GND_28 GND_29 GND_30 GND_31 GND_32 GND_33 GND_34 GND_35 GND_36 GND_37 GND_38 GND_39 GND_40 GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67 GND_68 GND_69 GND_70 GND_71 GND_72 GND_73 GND_74 GND_75 GND_76 GND_77 GND_78 GND_79 GND_80 GND_81 GND_82 GND_83 GND_84 GND_85 GND_86 GND_87 GND_88 GND_89 GND_90 GND_91 GND_92 GND_93 GND_94 GND_95 GND_96 GND_97 GND_98 GND_99 GND_100 GND_101 GND_102 GND_103 GND_104 GND_105 GND_106 GND_107 GND_108 GND_109 GND_110 GND_111 GND_112 GND_113 GND_114 GND_115 GND_116 GND_117 GND_118 GND_119 GND_120 GND_121 GND_122 GND_123 GND_124 GND_125 GND_126 GND_127 GND_128 GND_129 GND_130 GND_131 GND_132 GND_133 GND_134 GND_135 GND_136 GND_137 GND_138 GND_139 GND_140 GND_141 GND_142 GND_143 GND_144 GND_145 GND_146 GND_147 GND_148 GND_149 GND_150 GND_151 GND_152 GND_153

NB8M-GS-B-A1/H

PEG_RXP0 PEG_RXN0 PEG_RXP1 PEG_RXN1 PEG_RXP2 PEG_RXN2 PEG_RXP3 PEG_RXN3 PEG_RXP4 PEG_RXN4 PEG_RXP5 PEG_RXN5 PEG_RXP6 PEG_RXN6 PEG_RXP7 PEG_RXN7 PEG_RXP8 PEG_RXN8 PEG_RXP9 PEG_RXN9 PEG_RXP10 PEG_RXN10 PEG_RXP11 PEG_RXN11 PEG_RXP12 PEG_RXN12 PEG_RXP13 PEG_RXN13 PEG_RXP14 PEG_RXN14 PEG_RXP15 PEG_RXN15

C_PEG_RXP0 C_PEG_RXN0 C_PEG_RXP1 C_PEG_RXN1 C_PEG_RXP2 C_PEG_RXN2 C_PEG_RXP3 C_PEG_RXN3 C_PEG_RXP4 C_PEG_RXN4 C_PEG_RXP5 C_PEG_RXN5 C_PEG_RXP6 C_PEG_RXN6 C_PEG_RXP7 C_PEG_RXN7 C_PEG_RXP8 C_PEG_RXN8 C_PEG_RXP9 C_PEG_RXN9 C_PEG_RXP10 C_PEG_RXN10 C_PEG_RXP11 C_PEG_RXN11 C_PEG_RXP12 C_PEG_RXN12 C_PEG_RXP13 C_PEG_RXN13 C_PEG_RXP14 C_PEG_RXN14 C_PEG_RXP15 C_PEG_RXN15

0.1U/16V/V

PEG_TXP_C0 PEG_TXN_C0 PEG_TXP_C1 PEG_TXN_C1 PEG_TXP_C2 PEG_TXN_C2 PEG_TXP_C3 PEG_TXN_C3 PEG_TXP_C4 PEG_TXN_C4 PEG_TXP_C5 PEG_TXN_C5 PEG_TXP_C6 PEG_TXN_C6 PEG_TXP_C7 PEG_TXN_C7 PEG_TXP_C8 PEG_TXN_C8 PEG_TXP_C9 PEG_TXN_C9 PEG_TXP_C10 PEG_TXN_C10 PEG_TXP_C11 PEG_TXN_C11 PEG_TXP_C12 PEG_TXN_C12 PEG_TXP_C13 PEG_TXN_C13 PEG_TXP_C14 PEG_TXN_C14 PEG_TXP_C15 PEG_TXN_C15

CLK_PCIE_VGA CLK_PCIE_VGA# VGA_RST#

U33A

PEX_TX0 PEX_TX0# PEX_TX1 PEX_TX1# PEX_TX2 PEX_TX2# PEX_TX3 PEX_TX3# PEX_TX4 PEX_TX4# PEX_TX5 PEX_TX5# PEX_TX6 PEX_TX6# PEX_TX7 PEX_TX7# PEX_TX8 PEX_TX8# PEX_TX9 PEX_TX9# PEX_TX10 PEX_TX10# PEX_TX11 PEX_TX11# PEX_TX12 PEX_TX12# PEX_TX13 PEX_TX13# PEX_TX14 PEX_TX14# PEX_TX15 PEX_TX15#

PEX_RX0 PEX_RX0# PEX_RX1 PEX_RX1# PEX_RX2 PEX_RX2# PEX_RX3 PEX_RX3# PEX_RX4 PEX_RX4# PEX_RX5 PEX_RX5# PEX_RX6 PEX_RX6# PEX_RX7 PEX_RX7# PEX_RX8 PEX_RX8# PEX_RX9 PEX_RX9# PEX_RX10 PEX_RX10# PEX_RX11 PEX_RX11# PEX_RX12 PEX_RX12# PEX_RX13 PEX_RX13# PEX_RX14 PEX_RX14# PEX_RX15 PEX_RX15#

PEX_REFCLK PEX_REFCLK# PEX_RST#

RFU0 RFU1

PEX_TSTCLK_OUT PEX_TSTCLK_OUT#

PCIE

NB8M-GS-B-A1/H

VGA_VDD

PEX_IOVDD_0 PEX_IOVDD_1 PEX_IOVDD_2 PEX_IOVDD_3 PEX_IOVDD_4 PEX_IOVDD_5 — 1.2V

C292 C296 C371 C237 0.1U/16V/V 1U/6.3V/R

PLACE NEAR GPU

C808 4.7UB/10V/R — DB2 BOM MODIFY 1109

VGA_VDDQ

PEX_IOVDDQ_0 PEX_IOVDDQ_1 PEX_IOVDDQ_2 PEX_IOVDDQ_3 PEX_IOVDDQ_4 PEX_IOVDDQ_5 PEX_IOVDDQ_6 PEX_IOVDDQ_7 PEX_IOVDDQ_8 PEX_IOVDDQ_9 PEX_IOVDDQ_10 — 1.2V

C320 C361 C291 C308 C347 C264 C319 C332 C314 0.1U/16V/V 0.47UA/10V/X 1U/6.3V/R 10UA/6.3V/R

PLACE NEAR GPU

VDD_0 VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12 VDD_13 VDD_15 VDD_16 VDD_17 VDD_18 VDD_19 — VGA_CORE

C312 C311 C325 C329 C274 C271 C324 C284 C273 C267 C283 C330 C272 C297 C335 C249 C268 0.1U/16V/V 10UA/6.3V/R 0.47UA/10V/X

PLACE NEAR GPU

VDD_20 VDD_21 VDD_22 VDD_23 VDD_24 VDD_25 VDD_26 VDD_27 VDD_28 VDD_29 VDD_30 VDD_31 VDD_32 VDD_33 VDD_34 VDD_35 VDD_36

C318 C317 C298 C304 C322 C277 C337 C341 C300 1U/6.3V/R 0.47UA/10V/X 10UA/6.3V/R

1.2V [10,11,13,15,36]
VGA_CORE [35]
3V [2,5,6,7,8,9,10,11,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]

VDD_LP_0 VDD_LP_1 VDD_LP_2 VDD_LP_3 VDD_LP_4 VDD_LP_5

VDD_SENSE GND_SENSE — C328 *0.01U/16V/X — T94 T95

VDD33_0 VDD33_1 VDD33_2 VDD33_3 VDD33_4 VDD33_5 VDD33_6 VDD33_7 VDD33_8 VDD33_9 VDD33_10 VDD33_11 VDD33_12 — VGA_VDD3 R119 0B 3V

C198 C197 C193 C362 C250 C230 C199 0.1U/16V/V 0.47UA/10V/X 1U/6.3V/R

PLACE NEAR GPU

PEX_PLLAVDD PEX_PLLDVDD PEX_PLLGND — 15mil — PEX_PLLAVDD PEX_PLLDVDD

L14 L12 10nHA/0.3A

C263 C135 C134 C128 C131 C123 C282 C101 1U/6.3V/R 0.01U/16V/X 0.1U/16V/V 4.7UA/6.3V/R

1.2V

PLACE NEAR GPU

NV_PLLAVDD — 15mil — NV_PLLAVDD — VGA_CORE

SI MODIFY 1215
FOR NVIDIA RECOMMEND

NC_0 NC_1 NC_2 — AM8 AM9 B32

SPDIF — J6 SPDIF_VGA

3V

D2 CH501H — Ra R126 *24.3K/F

D1 CH501H — Rb R120 3.6KA/F

SPDIF_VGA — SI MODIFY C166 C 0.01U/16V/X — SPDIF — SPDIF [23,31] — Rc R136 *76.8/F

For 3.3V swing, we can remove Ra, Rb and Rc and replace C with 0ohm resistor.

[7,27,28] PCIE_RST# — C761 0.1U/16V/V — 3V — U31 *TC7SH08FU — R653 100K

G7XM:STUFF,G8X:NC — D41 CH500H

T88 T93 — VGA_RFU0 VGA_RFU1

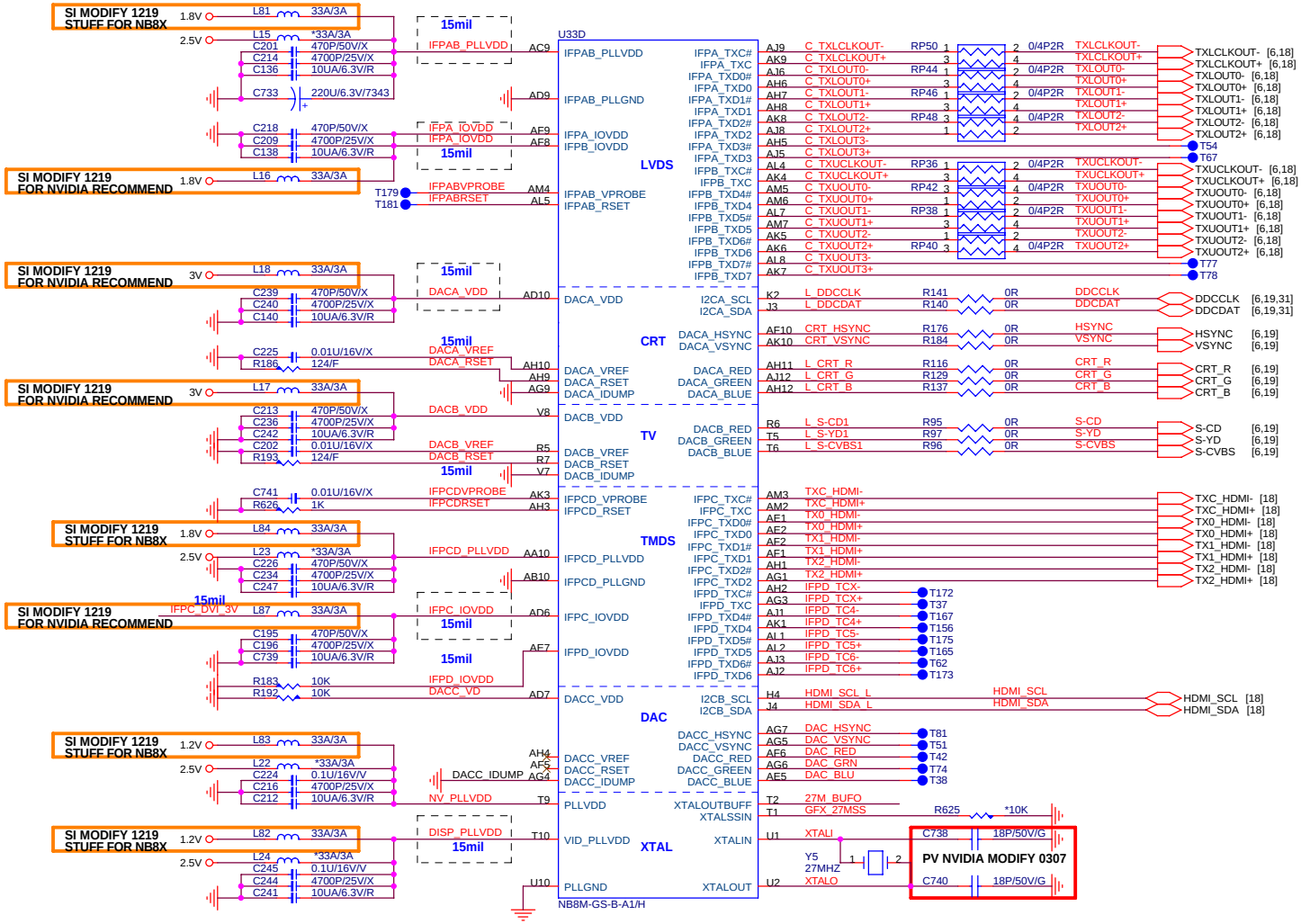
T186 T184 — PEX_TSTCK PEX_TSTCK#

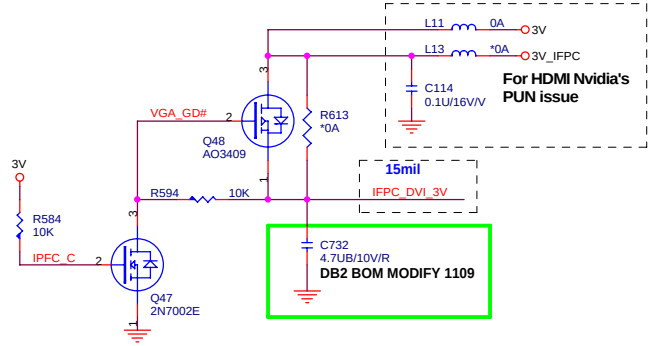
PROJECT : AT1
Quanta Computer Inc.

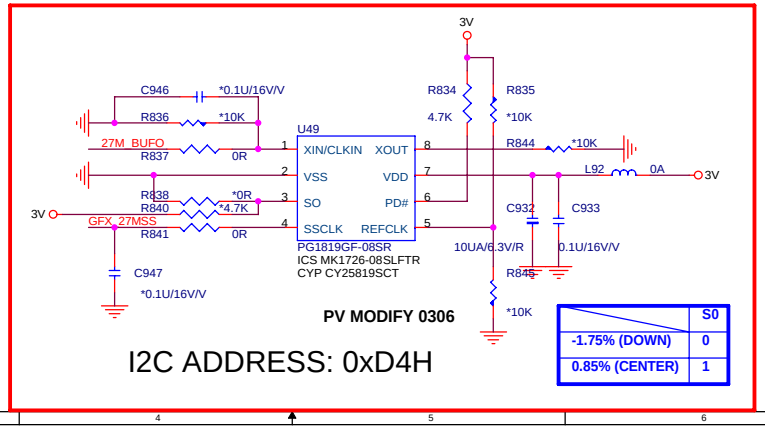
Size	Document Number	Rev
Custom	NV_NB8M (PCIE_I/F,GND)	MV

NB5/RD2/HW1

Date: Tuesday, August 21, 2007 Sheet 12 of 40







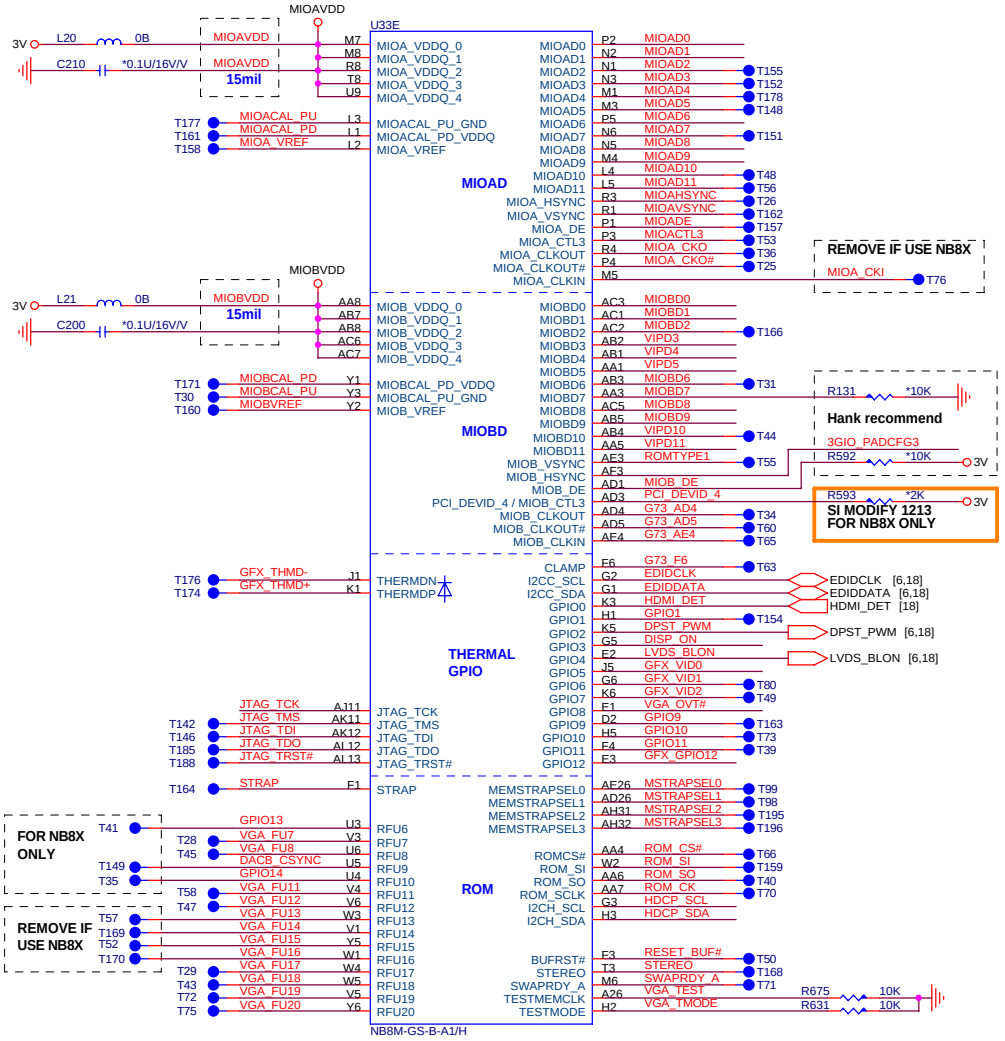
1.2V	[10,11,12,15,36]
1.8V	[11,15,16,17,32,37]
2.5V	[2,32,36]
3V	[2,5,6,7,8,9,10,11,12,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
5V	[18,19,22,23,25,26,27,28,29,31,32,33,36,38]

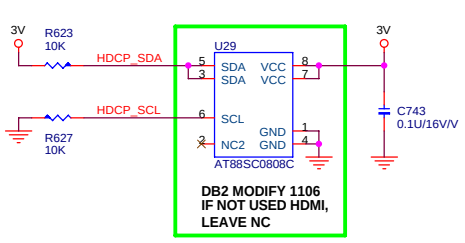
NB5/RD2/HW1

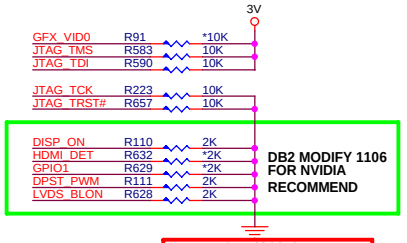
PROJECT : AT1
Quanta Computer Inc.

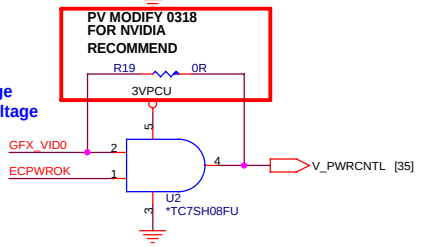
Size	Document Number	Rev
Custom	NV_NB8M (LVDS,CRT,TV,HDMI)	MV

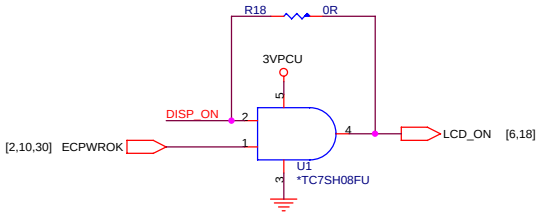
Date: Tuesday, August 21, 2007 Sheet 13 of 40





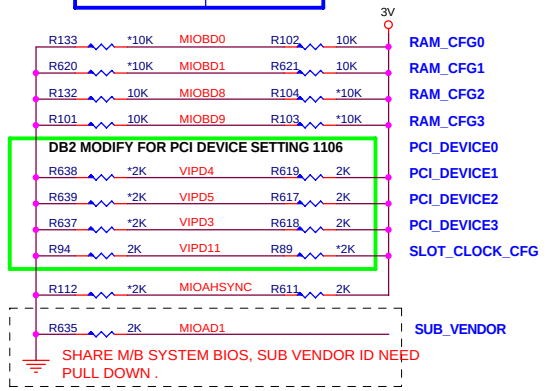






PCI DEVICE ID SETTING

PCI_DEVICE[4:0]	DESCRIPTION
00111	NB8M
OTHERS	RESERVED

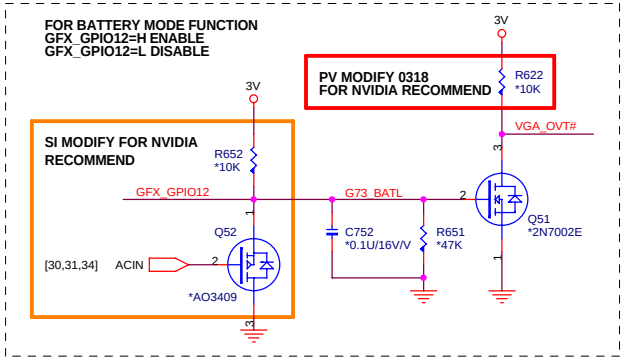


NB8X 64bit VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infineon
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

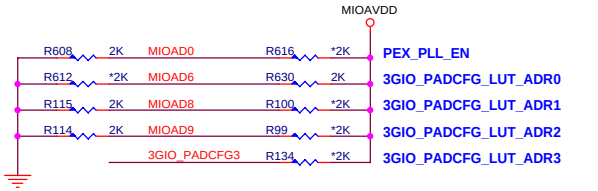
NB8X 128bit VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infineon
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infineon
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix



3GIO_PADCFG STRAP

3GIO_PDACFG[3:0]	DESCRIPTION
0000	DESKTOP
0001	MOBILE
OTHERS	RESERVED



3V [2,5,6,7,8,9,10,11,12,13,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3VPCU [9,18,28,29,30,31,33,34,35]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

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Channel C is available for 128bit only

U33B

FBA

VMA_DQ0 N27
VMA_DQ1 M27
VMA_DQ2 N28
VMA_DQ3 L29
VMA_DQ4 K27
VMA_DQ5 K28
VMA_DQ6 J29
VMA_DQ7 J28
VMA_DQ8 P30
VMA_DQ9 N31
VMA_DQ10 N30
VMA_DQ11 N32
VMA_DQ12 L31
VMA_DQ13 L30
VMA_DQ14 J30
VMA_DQ15 L32
VMA_DQ16 H30
VMA_DQ17 K30
VMA_DQ18 H31
VMA_DQ19 E30
VMA_DQ20 H32
VMA_DQ21 E31
VMA_DQ22 D30
VMA_DQ23 E30
VMA_DQ24 H28
VMA_DQ25 H29
VMA_DQ26 E29
VMA_DQ27 J27
VMA_DQ28 E27
VMA_DQ29 E27
VMA_DQ30 E28
VMA_DQ31 F28
VMA_DQ32 AD29
VMA_DQ33 AE29
VMA_DQ34 AD28
VMA_DQ35 AC28
VMA_DQ36 AB29
VMA_DQ37 AA30
VMA_DQ38 Y28
VMA_DQ39 AB30
VMA_DQ40 AM30
VMA_DQ41 AE30
VMA_DQ42 AJ31
VMA_DQ43 AJ30
VMA_DQ44 AJ32
VMA_DQ45 AK29
VMA_DQ46 AM31
VMA_DQ47 AL30
VMA_DQ48 AE32
VMA_DQ49 AE30
VMA_DQ50 AF31
VMA_DQ51 AD30
VMA_DQ52 AC31
VMA_DQ53 AC32
VMA_DQ54 AB32
VMA_DQ55 AB31
VMA_DQ56 AG27
VMA_DQ57 AF28
VMA_DQ58 AH28
VMA_DQ59 AG28
VMA_DQ60 AG29
VMA_DQ61 AD27
VMA_DQ62 AE27
VMA_DQ63 AE28

FBAD0 … FBAD63

VMA_DM0 M29
VMA_DM1 M30
VMA_DM2 G30
VMA_DM3 F29
VMA_DM4 AA29
VMA_DM5 AK30
VMA_DM6 AC30
VMA_DM7 AG30

FBADQM0 … FBADQM7

VMA_WDQS0 L28
VMA_WDQS1 K31
VMA_WDQS2 G32
VMA_WDQS3 G28
VMA_WDQS4 AB28
VMA_WDQS5 AL32
VMA_WDQS6 AE32
VMA_WDQS7 AH30

FBADQS_WP0 … FBADQS_WP7

VMA_RDQS0 M28
VMA_RDQS1 K32
VMA_RDQS2 G31
VMA_RDQS3 G27
VMA_RDQS4 AA28
VMA_RDQS5 AL31
VMA_RDQS6 AE31
VMA_RDQS7 AH29

FBADQS_RN0 … FBADQS_RN7

FBA_PLLVDD/H_PLLVDD
FBA_PLLAVDD
FBA_PLLGND
FB_VREF1 E32

NB8M-GS-B-A1/H

FBVDD_0 A12
FBVDD_1 A15
FBVDD_2 A18
FBVDD_3 A21
FBVDD_4 A24
FBVDD_5 A27
FBVDD_6 A3
FBVDD_7 A30
FBVDD_8 A6
FBVDD_9 A9
FBVDD_10 AA32
FBVDD_11 AD32
FBVDD_12 AG32
FBVDD_13 AK32
FBVDD_14 C32
FBVDD_15 F32
FBVDD_16 J32
FBVDD_17 M32
FBVDD_18 R32
FBVDD_19 V32

C420 0.1U/16V/V
C208 0.1U/16V/V
C419 0.1U/16V/V
C763 0.1U/16V/V
C799 0.1U/16V/V
C369 0.1U/16V/V
C352 0.1U/16V/V
C167 0.1U/16V/V
C333 0.47UA/10V/X
C360 0.47UA/10V/X
C279 0.47UA/10V/X
C810 0.47UA/10V/X
C235 10UA/6.3V/R
C356 10UA/6.3V/R

1.8V

PLACE NEAR GPU

FBVDDQ_0 AA25
FBVDDQ_1 AA26
FBVDDQ_2 AB25
FBVDDQ_3 AB26
FBVDDQ_4 G11
FBVDDQ_5 G12
FBVDDQ_6 G15
FBVDDQ_7 G18
FBVDDQ_8 G21
FBVDDQ_9 G22
FBVDDQ_10 H11
FBVDDQ_11 H12
FBVDDQ_12 H15
FBVDDQ_13 H18
FBVDDQ_14 H21
FBVDDQ_15 H22
FBVDDQ_16 L25
FBVDDQ_17 L26
FBVDDQ_18 M25
FBVDDQ_19 M26
FBVDDQ_20 R25
FBVDDQ_21 R26
FBVDDQ_22 V25
FBVDDQ_23 V26

C343 0.1U/16V/V
C427 0.1U/16V/V
C345 0.1U/16V/V
C365 0.1U/16V/V
C339 0.1U/16V/V
C372 0.1U/16V/V
C381 0.1U/16V/V
C380 0.1U/16V/V
C354 0.47UA/10V/X
C348 0.47UA/10V/X
C265 0.47UA/10V/X
C355 0.47UA/10V/X
C350 10UA/6.3V/R
C812 10UA/6.3V/R

1.8V

PLACE NEAR GPU

FBA_CMD0 P32 VMA_MA3 — VMA_MA3 [16]
FBA_CMD1 U27 VMA_MA0 — VMA_MA0 [16]
FBA_CMD2 P31 VMA_MA2 — VMA_MA2 [16]
FBA_CMD3 U30 VMA_MA1 — VMA_MA1 [16]
FBA_CMD4 Y31 VMA_MA3H — VMA_MA3H [16]
FBA_CMD5 W32 VMA_MA4H — VMA_MA4H [16]
FBA_CMD6 W31 VMA_MA5H — VMA_MA5H [16]
FBA_CMD7 T32 VMA_BA2 — T196
FBA_CMD8 V27 VMA_CS0# — VMA_CS0# [16]
FBA_CMD9 T28 VMA_WE# — VMA_WE# [16]
FBA_CMD10 T31 VMA_BA0 — VMA_BA0 [16]
FBA_CMD11 U32 VMA_CKE — VMA_CKE [16]
FBA_CMD12 W29 VMA_RST#
FBA_CMD13 W30 VMA_MA2H — VMA_MA2H [16]
FBA_CMD14 T27 VMA_MA12 — VMA_MA12 [16]
FBA_CMD15 V28 VMA_RAS# — VMA_RAS# [16]
FBA_CMD16 V30 VMA_MA11 — VMA_MA11 [16]
FBA_CMD17 U31 VMA_MA10 — VMA_MA10 [16]
FBA_CMD18 R27 VMA_BA1 — VMA_BA1 [16]
FBA_CMD19 V29 VMA_MA8 — VMA_MA8 [16]
FBA_CMD20 T30 VMA_MA9 — VMA_MA9 [16]
FBA_CMD21 W28 VMA_MA6 — VMA_MA6 [16]
FBA_CMD22 R29 VMA_MA5 — VMA_MA5 [16]
FBA_CMD23 R30 VMA_MA7 — VMA_MA7 [16]
FBA_CMD24 P29 VMA_MA4 — VMA_MA4 [16]
FBA_CMD25 U28 VMA_CAS# — VMA_CAS# [16]
FBA_CMD26 Y32 VMA_MA13 — T193

FBA_CLK0 P28 VMA_CLK0 — VMA_CLK0 [16]
FBA_CLK0# R28 VMA_CLK0# — VMA_CLK0# [16]
FBA_CLK1 Y27 VMA_CLK1 — VMA_CLK1 [16]
FBA_CLK1# AA27 VMA_CLK1# — VMA_CLK1# [16]

RFU2 Y30 — FBA_CMD27 — T194 — RESERVED FOR NB8X
RFU3 AC26 — G73_AC26 — T96
FBA_DEBUG AC27 — VMA_DEBUG — T97
FBA_REFCLK D32 — VMA_REFCK — T199
FBA_REFCLK# D31 — VMA_REFCK# — T197 — REMOVE IF USE NB8X

L32 220A/0.2A
C377 0.1U/16V/V
C378 4.7UA/6.3V/R
1.2V
DB2 MODIFY 1024
STUFF FOR NB8X

FBA_PLLVDD G23
FBA_PLLAVDD G25 — 15mil — L40 33A/3A — 1.2V
FBA_PLLGND G24
C406 4.7UA/6.3V/R
C389 470P/50V/X
C391 4700P/25V/X
C370 0.1U/16V/V
For EMI

VREF=FBVDDQ*Rbot/(Rtop+Rbot)
1.8V — R682 *1K — FB_VREF1 — E32
DB2 MODIFY 1103
STUFF FOR NB8X
R680 *1K
15mil
C825 *0.1U/16V/V
PV MODIFY FOR NVIDIA RECOMMEND 0318

U33C

FBC

VMC_DQ0 B7
VMC_DQ1 A7
VMC_DQ2 C7
VMC_DQ3 A2
VMC_DQ4 B2
VMC_DQ5 C4
VMC_DQ6 A5
VMC_DQ7 B5
VMC_DQ8 F9
VMC_DQ9 F10
VMC_DQ10 D12
VMC_DQ11 D9
VMC_DQ12 E12
VMC_DQ13 D11
VMC_DQ14 E8
VMC_DQ15 D8
VMC_DQ16 E7
VMC_DQ17 F7
VMC_DQ18 D6
VMC_DQ19 D5
VMC_DQ20 D3
VMC_DQ21 E4
VMC_DQ22 C3
VMC_DQ23 B4
VMC_DQ24 C10
VMC_DQ25 B10
VMC_DQ26 C8
VMC_DQ27 A10
VMC_DQ28 C11
VMC_DQ29 C12
VMC_DQ30 A11
VMC_DQ31 B11
VMC_DQ32 B28
VMC_DQ33 C27
VMC_DQ34 C26
VMC_DQ35 B26
VMC_DQ36 C30
VMC_DQ37 B31
VMC_DQ38 C29
VMC_DQ39 A31
VMC_DQ40 D28
VMC_DQ41 D27
VMC_DQ42 F26
VMC_DQ43 D24
VMC_DQ44 E23
VMC_DQ45 B24
VMC_DQ46 E24
VMC_DQ47 F23
VMC_DQ48 B23
VMC_DQ49 A23
VMC_DQ50 C25
VMC_DQ51 C23
VMC_DQ52 A22
VMC_DQ53 C22
VMC_DQ54 C21
VMC_DQ55 B22
VMC_DQ56 E22
VMC_DQ57 D22
VMC_DQ58 D21
VMC_DQ59 E21
VMC_DQ60 E18
VMC_DQ61 D19
VMC_DQ62 D18
VMC_DQ63 E19

FBCD0 … FBCD63

VMC_DM0 A4
VMC_DM1 F11
VMC_DM2 F5
VMC_DM3 C9
VMC_DM4 C28
VMC_DM5 F24
VMC_DM6 C24
VMC_DM7 E20

FBCDQM0 … FBCDQM7

VMC_WDQS0 C5
VMC_WDQS1 E10
VMC_WDQS2 E5
VMC_WDQS3 B8
VMC_WDQS4 A29
VMC_WDQS5 D25
VMC_WDQS6 B25
VMC_WDQS7 E20

FBCDQS_WP0 … FBCDQS_WP7

VMC_RDQS0 C6
VMC_RDQS1 F9
VMC_RDQS2 E6
VMC_RDQS3 A8
VMC_RDQS4 B29
VMC_RDQS5 E25
VMC_RDQS6 A25
VMC_RDQS7 F21

FBCDQS_RN0 … FBCDQS_RN7

NB8M-GS-B-A1/H

FBVTT_0 AA23
FBVTT_1 AB23
FBVTT_2 H16
FBVTT_3 H17
FBVTT_4 J10
FBVTT_5 J23
FBVTT_6 J24
FBVTT_7 J9
FBVTT_8 K11
FBVTT_9 K12
FBVTT_10 K21
FBVTT_11 K22
FBVTT_12 K24
FBVTT_13 K9
FBVTT_14 L23
FBVTT_15 M23
FBVTT_16 T25
FBVTT_17 U25

C344 0.1U/16V/V
C756 1U/6.3V/R
C358 0.1U/16V/V
C827 0.1U/16V/V
C303 0.47UA/10V/X
C313 0.47UA/10V/X
C253 10UA/6.3V/R
C357 0.1U/16V/V
C374 0.1U/16V/V
C290 0.1U/16V/V
C336 0.47UA/10V/X
C219 0.47UA/10V/X
C327 10UA/6.3V/R

1.8V

PLACE NEAR GPU

FBC_CMD0 C13 VMC_MA3 — VMC_MA3 [17]
FBC_CMD1 A16 VMC_MA0 — VMC_MA0 [17]
FBC_CMD2 A13 VMC_MA2 — VMC_MA2 [17]
FBC_CMD3 B17 VMC_MA1 — VMC_MA1 [17]
FBC_CMD4 B20 VMC_MA3H — VMC_MA3H [17]
FBC_CMD5 A19 VMC_MA4H — VMC_MA4H [17]
FBC_CMD6 B19 VMC_MA5H — VMC_MA5H [17]
FBC_CMD7 B14 VMC_BA2 — T92
FBC_CMD8 E16 VMC_CS0# — VMC_CS0# [17]
FBC_CMD9 A14 VMC_WE# — VMC_WE# [17]
FBC_CMD10 C15 VMC_BA0 — VMC_BA0 [17]
FBC_CMD11 B16 VMC_CKE — VMC_CKE [17]
FBC_CMD12 F17 VMC_RST#
FBC_CMD13 C19 VMC_MA2H — VMC_MA2H [17]
FBC_CMD14 D15 VMC_MA12 — VMC_MA12 [17]
FBC_CMD15 C17 VMC_RAS# — VMC_RAS# [17]
FBC_CMD16 A17 VMC_MA11 — VMC_MA11 [17]
FBC_CMD17 C16 VMC_MA10 — VMC_MA10 [17]
FBC_CMD18 D14 VMC_BA1 — VMC_BA1 [17]
FBC_CMD19 F16 VMC_MA8 — VMC_MA8 [17]
FBC_CMD20 C14 VMC_MA9 — VMC_MA9 [17]
FBC_CMD21 C18 VMC_MA6 — VMC_MA6 [17]
FBC_CMD22 E14 VMC_MA5 — VMC_MA5 [17]
FBC_CMD23 B13 VMC_MA7 — VMC_MA7 [17]
FBC_CMD24 E15 VMC_MA4 — VMC_MA4 [17]
FBC_CMD25 F15 VMC_CAS# — VMC_CAS# [17]
FBC_CMD26 A20 VMC_MA13 — T192

FBC_CLK0 E13 VMC_CLK0 — VMC_CLK0 [17]
FBC_CLK0# E13 VMC_CLK0# — VMC_CLK0# [17]
FBC_CLK1 F18 VMC_CLK1 — VMC_CLK1 [17]
FBC_CLK1# E17 VMC_CLK1# — VMC_CLK1# [17]

RFU4 C20 FBC_CMD27 — T191
RFU5 D1 G73_D1 — T153
RESERVED FOR NB8X

FBC_DEBUG F12 — VMC_DEBUG — T90

FBC_REFCLK B1 VMC_REFCK — R610 0R — R605 0R — I2CS_SDA R609 2.2K — I2CS_SCL R604 2.2K — 3V
FBC_REFCLK# C1 VMC_REFCK# — T83
G73_G8
PV MODIFY FOR NVIDIA RECOMMEND 0318

FBC_PLLVDD G8
FBC_PLLAVDD G10 — 15mil — FBC_PLLAVDD — L27 *33A/3A — 1.2V
FBC_PLLGND G9
C221 *470P/50V/X
C251 *4700P/25V/X
C262 *4.7UA/6.3V/R
DB2 MODIFY 1103
IF NOT USED C PORT DDR2,
FB_PLLAVDD LEAVE NC

FBCAL_PD_VDDQ
FBCAL_PU_GND
FBCAL_TERM_GND
FBCAL_PD K26 — R242 40.2A/F — 1.8V
FBCAL_PU H26 — R243 40.2/F
FBCAL_TERM J26 — R241 *40.2/F
SI MODIFY FOR NVIDIA RECOMMEND 1220

FB_VREF2 A28 — 15mil — FB_VREF2 — R677 *1K — 1.8V
C811 *0.1U/16V/V
R676 *1K
IF NOT USED C PORT DDR2,
FB_VREF2 LEAVE NC

VMA_RST# R678 0R VMA_ODT — VMA_ODT [16]
R679 10K
VMC_RST# R226 *0R VMC_ODT — VMC_ODT [17]
Ra
R225 *10K
Rb
DB2 MODIFY 1103
IF NOT USED C PORT DDR2,
Ra,Rb LEAVE NC

MBDATA [2,29,30,31,34]
R820 *0R — Q71 *RHU002N06 — 3V — I2CS_SDA
MBCLK [2,29,30,31,34]
R821 *0R — Q72 *RHU002N06 — 3V — I2CS_SCL
SI MODIFY
FOR NVIDIA
RECOMMEND
1212

[16] VMA_DQ[63..0]
[16] VMA_DM[7..0]
[16] VMA_WDQS[7..0]
[16] VMA_RDQS[7..0]

[17] VMC_DQ[63..0]
[17] VMC_DM[7..0]
[17] VMC_WDQS[7..0]
[17] VMC_RDQS[7..0]

1.2V [10,11,12,13,36]
1.8V [11,13,16,17,32,37]
3V [2,5,6,7,8,9,10,11,12,13,14,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV_NB8M (MEM_I/F)	MV

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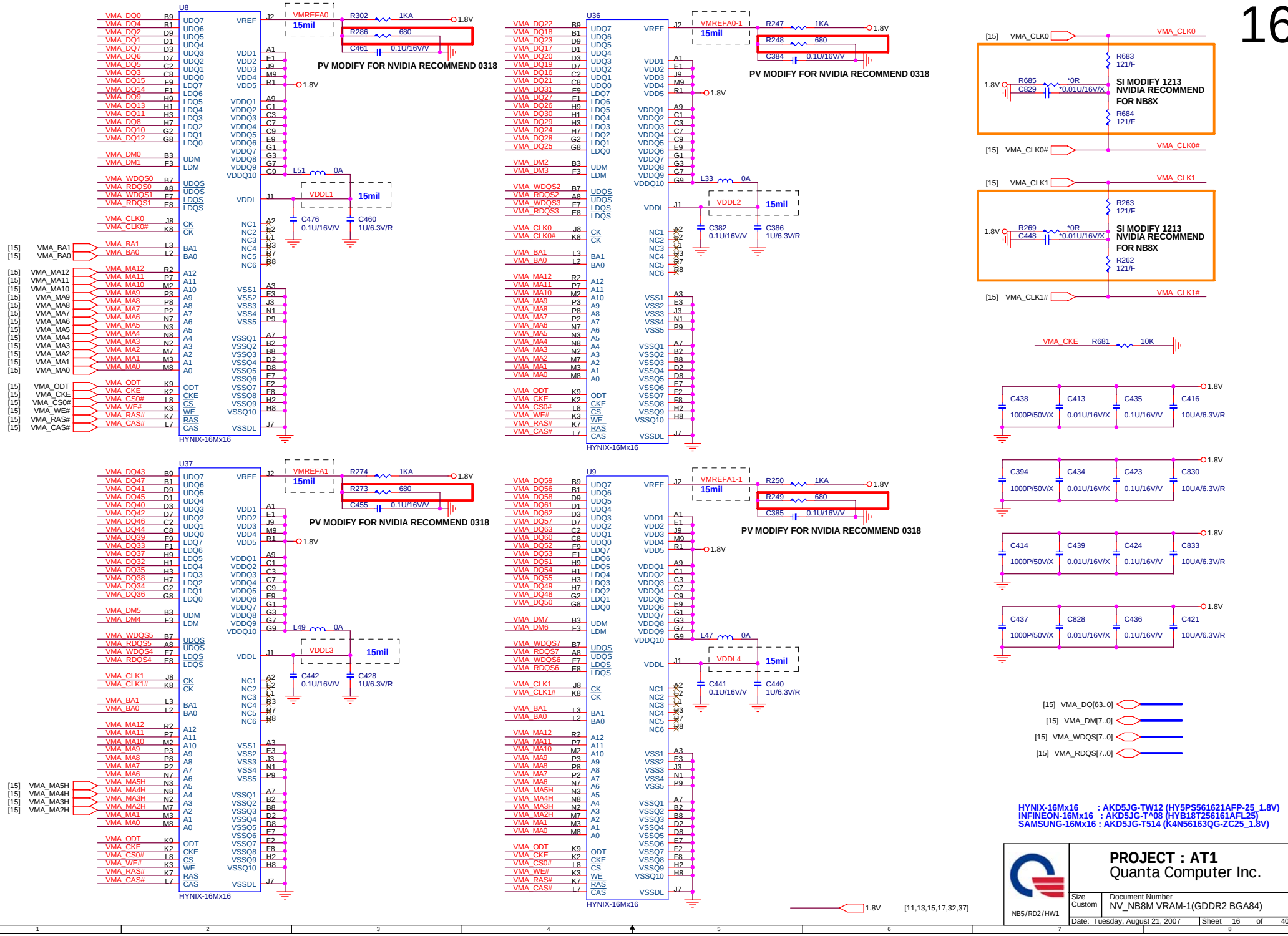
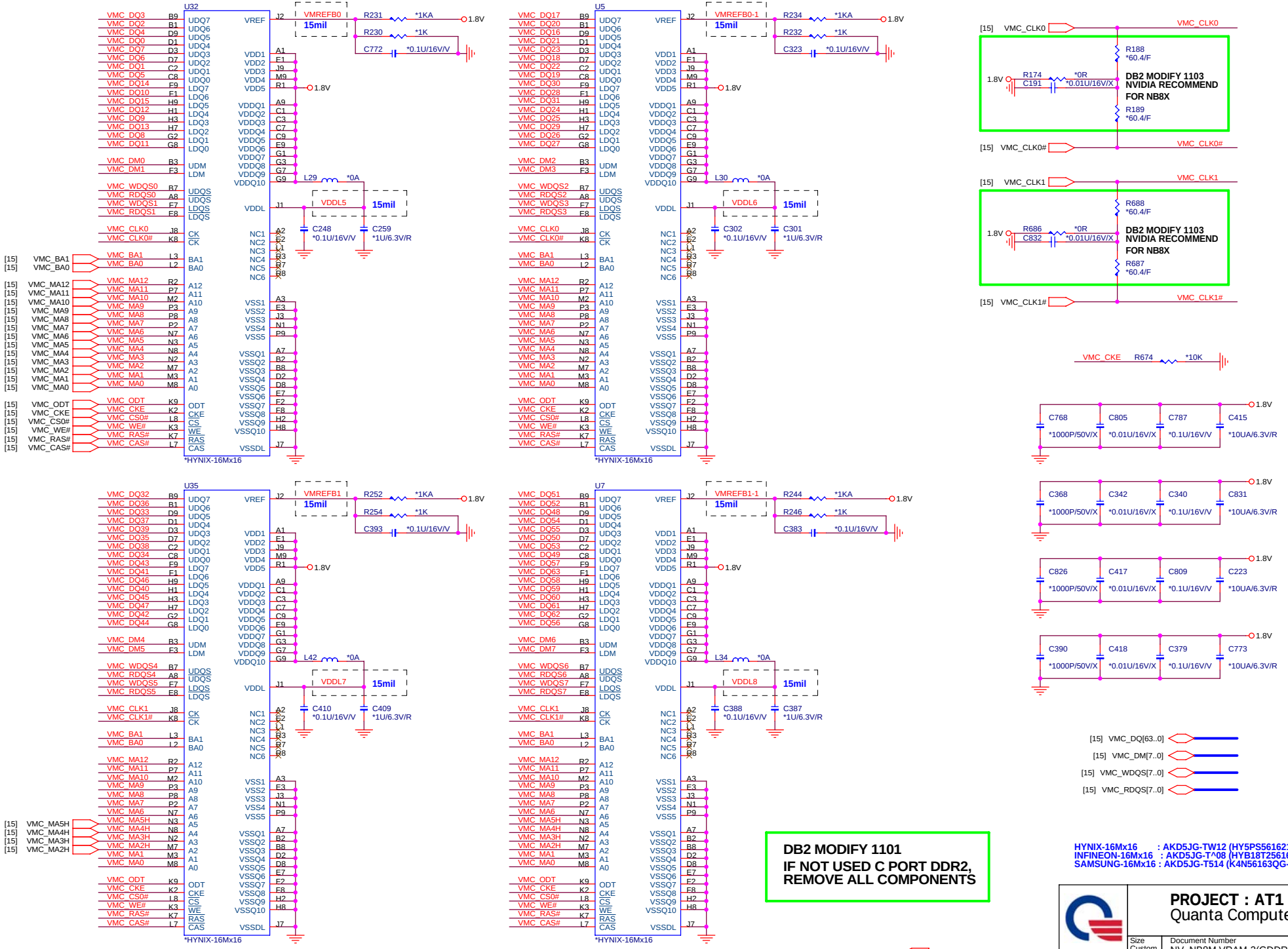

U8
U36
U37
U9
HYNIX-16Mx16
VREF
VDD1
VDD2
VDD3
VDD4
VDD5
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9
VDDQ10
VDDL
VSS1
VSS2
VSS3
VSS4
VSS5
VSSQ1
VSSQ2
VSSQ3
VSSQ4
VSSQ5
VSSQ6
VSSQ7
VSSQ8
VSSQ9
VSSQ10
VSSDL
NC1
NC2
NC3
NC4
NC5
NC6
UDM
LDM
UDQS
LDQS
CK
CK#
BA1
BA0
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
ODT
CKE
CS
WE
RAS
CAS
VMREFA0
VMREFA0-1
VMREFA1
VMREFA1-1
15mil
R302 1KA
R286 680
C461 0.1U/16V/V
R247 1KA
R248 680
C384 0.1U/16V/V
R274 1KA
R273 680
C455 0.1U/16V/V
R250 1KA
R249 680
C385 0.1U/16V/V
PV MODIFY FOR NVIDIA RECOMMEND 0318
1.8V
L51 0A
L33 0A
L49 0A
L47 0A
VDDL1
VDDL2
VDDL3
VDDL4
C476 0.1U/16V/V
C460 1U/6.3V/R
C382 0.1U/16V/V
C386 1U/6.3V/R
C442 0.1U/16V/V
C428 1U/6.3V/R
C441 0.1U/16V/V
C440 1U/6.3V/R
VMA_CLK0
VMA_CLK0#
VMA_CLK1
VMA_CLK1#
R683 121/F
R685 *0R
C829 *0.01U/16V/X
R684 121/F
R263 121/F
R269 *0R
C448 *0.01U/16V/X
R262 121/F
SI MODIFY 1213
NVIDIA RECOMMEND
FOR NB8X
VMA_CKE
R681 10K
C438 1000P/50V/X
C413 0.01U/16V/X
C435 0.1U/16V/V
C416 10UA/6.3V/R
C394 1000P/50V/X
C434 0.01U/16V/X
C423 0.1U/16V/V
C830 10UA/6.3V/R
C414 1000P/50V/X
C439 0.01U/16V/X
C424 0.1U/16V/V
C833 10UA/6.3V/R
C437 1000P/50V/X
C828 0.01U/16V/X
C436 0.1U/16V/V
C421 10UA/6.3V/R
VMA_DQ[63..0]
VMA_DM[7..0]
VMA_WDQS[7..0]
VMA_RDQS[7..0]
HYNIX-16Mx16 : AKD5JG-TW12 (HY5PS561621AFP-25_1.8V)
INFINEON-16Mx16 : AKD5JG-T^08 (HYB18T256161AFL25)
SAMSUNG-16Mx16 : AKD5JG-T514 (K4N56163QG-ZC25_1.8V)
[11,13,15,17,32,37]
NB5/RD2/HW1
PROJECT : AT1
Quanta Computer Inc.
Size Custom
Document Number NV_NB8M VRAM-1(GDDR2 BGA84)
Rev MV
Date: Tuesday, August 21, 2007
Sheet 16 of 40


U32
U5
U35
U7
*HYNIX-16Mx16
VMREFB0
VMREFB0-1
VMREFB1
VMREFB1-1
15mil
R231 *1KA
R230 *1K
C772 *0.1U/16V/V
R234 *1KA
R232 *1K
C323 *0.1U/16V/V
R252 *1KA
R254 *1K
C393 *0.1U/16V/V
R244 *1KA
R246 *1K
C383 *0.1U/16V/V
1.8V
L29 *0A
L30 *0A
L42 *0A
L34 *0A
VDDL5
VDDL6
VDDL7
VDDL8
C248 *0.1U/16V/V
C259 *1U/6.3V/R
C302 *0.1U/16V/V
C301 *1U/6.3V/R
C410 *0.1U/16V/V
C409 *1U/6.3V/R
C388 *0.1U/16V/V
C387 *1U/6.3V/R
[15] VMC_BA1
[15] VMC_BA0
[15] VMC_MA12
[15] VMC_MA11
[15] VMC_MA10
[15] VMC_MA9
[15] VMC_MA8
[15] VMC_MA7
[15] VMC_MA6
[15] VMC_MA5
[15] VMC_MA4
[15] VMC_MA3
[15] VMC_MA2
[15] VMC_MA1
[15] VMC_MA0
[15] VMC_ODT
[15] VMC_CKE
[15] VMC_CS0#
[15] VMC_WE#
[15] VMC_RAS#
[15] VMC_CAS#
[15] VMC_MA5H
[15] VMC_MA4H
[15] VMC_MA3H
[15] VMC_MA2H
[15] VMC_CLK0
VMC_CLK0
R188 *60.4/F
R174 *0R
C191 *0.01U/16V/X
DB2 MODIFY 1103
NVIDIA RECOMMEND
FOR NB8X
R189 *60.4/F
[15] VMC_CLK0#
VMC_CLK0#
[15] VMC_CLK1
VMC_CLK1
R688 *60.4/F
R686 *0R
C832 *0.01U/16V/X
R687 *60.4/F
[15] VMC_CLK1#
VMC_CLK1#
VMC_CKE R674 *10K
C768 C805 C787 C415
*1000P/50V/X *0.01U/16V/X *0.1U/16V/V *10UA/6.3V/R
C368 C342 C340 C831
C826 C417 C809 C223
C390 C418 C379 C773
[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]
DB2 MODIFY 1101
IF NOT USED C PORT DDR2,
REMOVE ALL COMPONENTS
HYNIX-16Mx16 : AKD5JG-TW12 (HY5PS561621AFP-25_1.8V)
INFINEON-16Mx16 : AKD5JG-T^08 (HYB18T256161AFL25)
SAMSUNG-16Mx16 : AKD5JG-T514 (K4N56163QG-ZC25_1.8V)
1.8V [11,13,15,16,32,37]
NB5/RD2/HW1
PROJECT : AT1
Quanta Computer Inc.
Size Custom
Document Number NV_NB8M VRAM-2(GDDR2 BGA84)
Rev MV
Date: Tuesday, August 21, 2007
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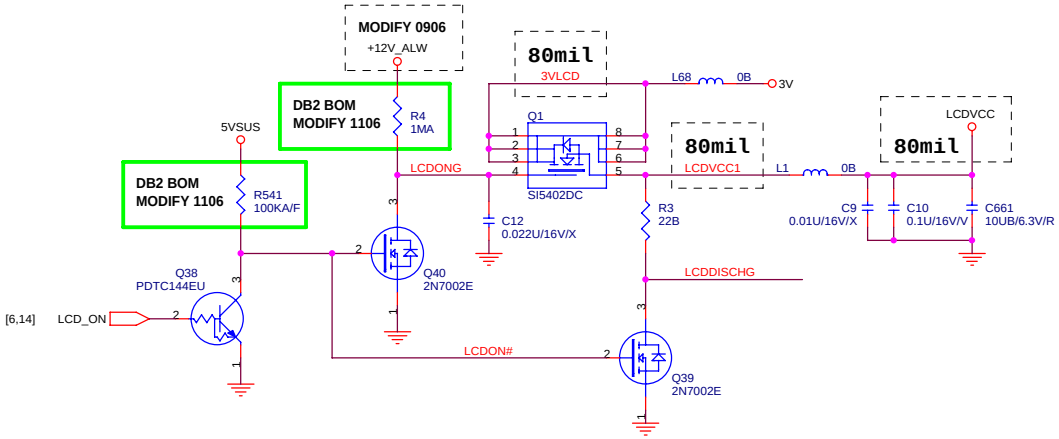
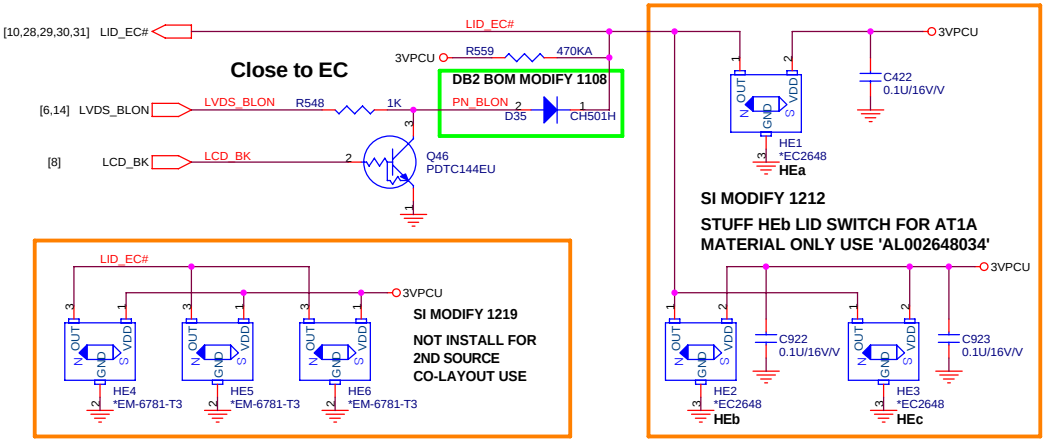
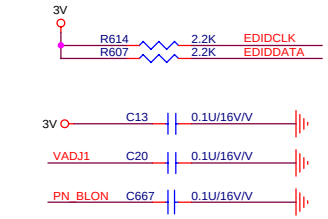
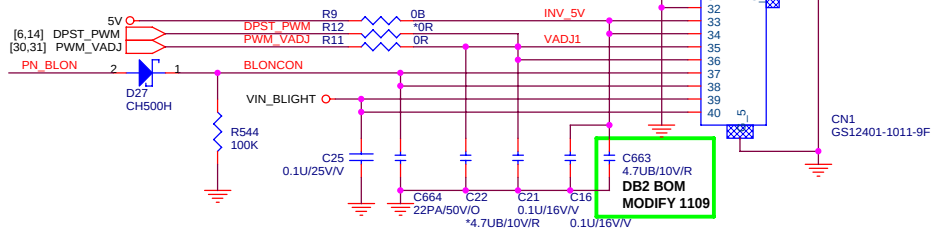
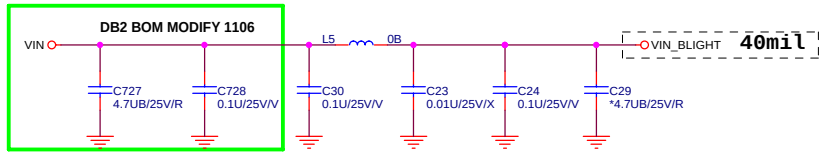
LCD CONNECTOR

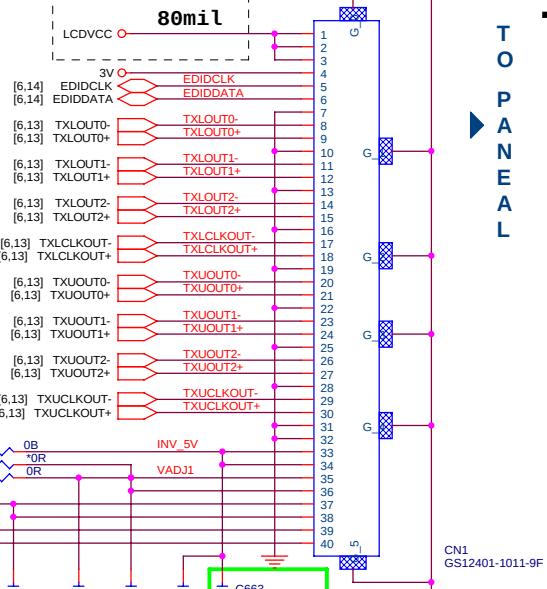






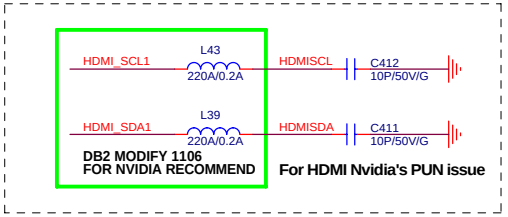


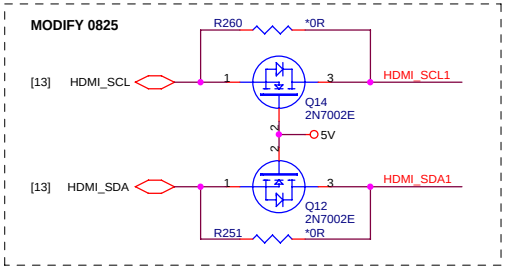


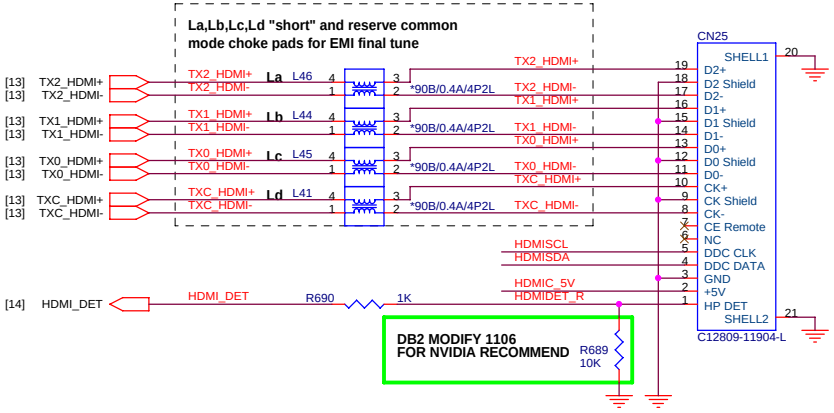


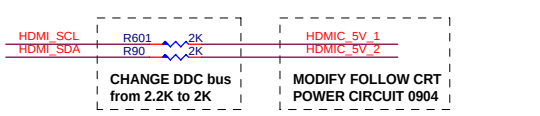
TO PANEAL

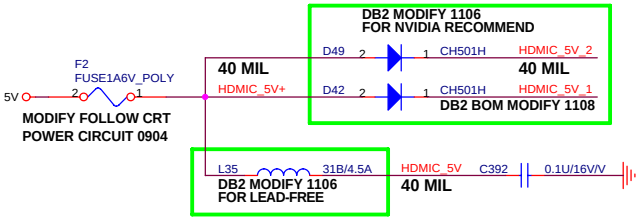
HDMI PORT











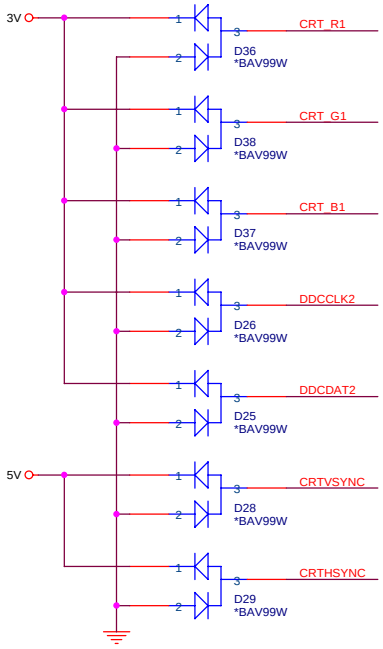
3V	[2,5,6,7,8,9,10,11,12,13,14,15,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3VPCU	[9,14,28,29,30,31,33,34,35]
5V	[13,19,22,23,25,26,27,28,29,31,32,33,36,38]
5VSUS	[26,28,30,31,32,33,37]
+12V_ALW	[10,32,33]
VIN	[31,32,33,34,35,36,37,38]

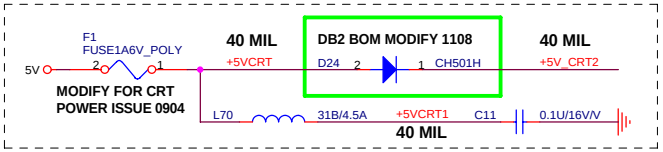
NB5/RD2/HW1

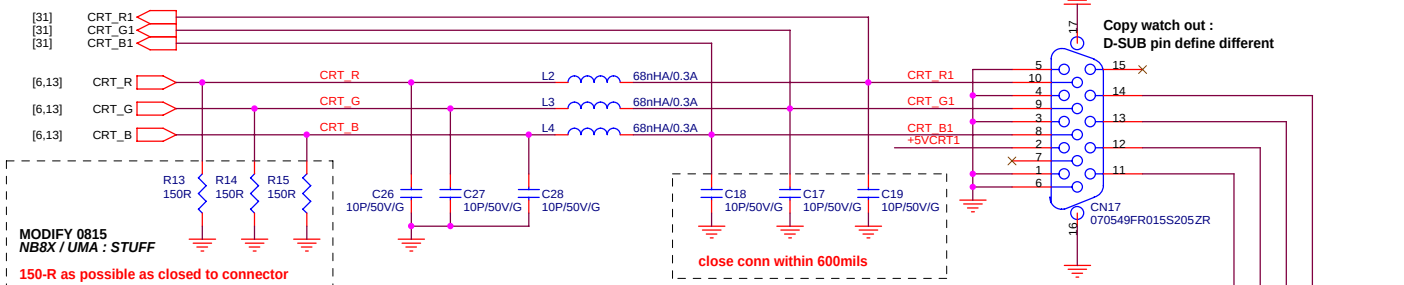
PROJECT : AT1
Quanta Computer Inc.

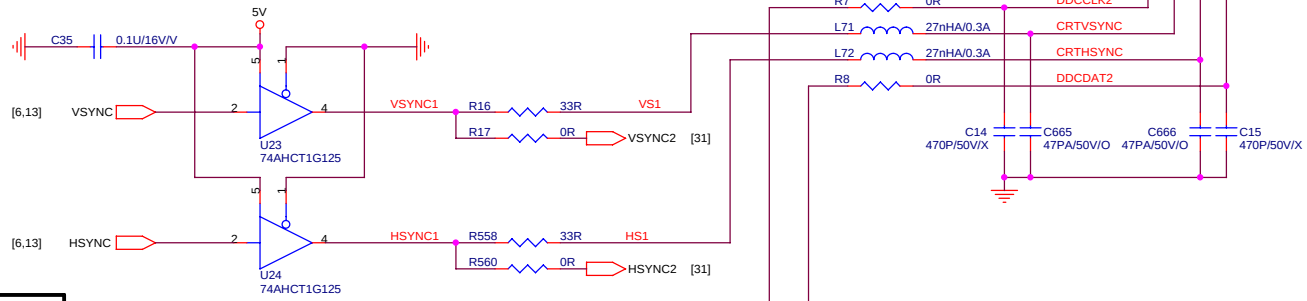
Size	Document Number	Rev
Custom	LCD,HDMI,LID_SW	MV
Date: Tuesday, August 21, 2007	Sheet 18 of 40	

CRT PORT

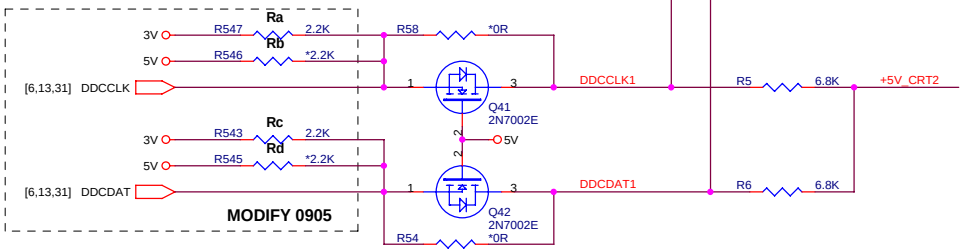






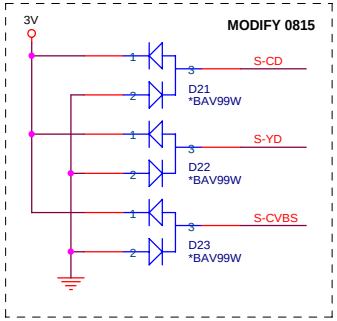


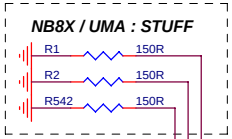
NB8X & MCP67M DIFFERENCE		
LOCATION	NB8X (DISCRETE)	MCP67M (UMA)
Ra Rb	2.2K NC	NC 2.2K
Rc Rd	2.2K NC	NC 2.2K

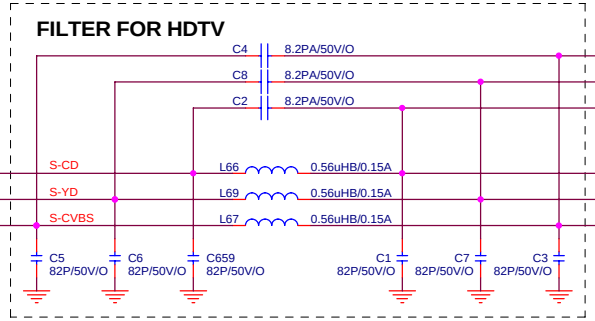


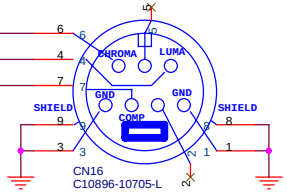
3V
5V
[2,5,6,7,8,9,10,11,12,13,14,15,18,21,22,23,26,27,28,29,30,31,32,33,36,38]
[13,18,22,23,25,26,27,28,29,31,32,33,36,38]

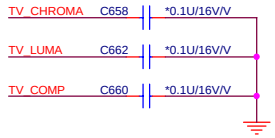
TV_OUT











PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT,TV_OUT	MV

NB5/RD2/HW1

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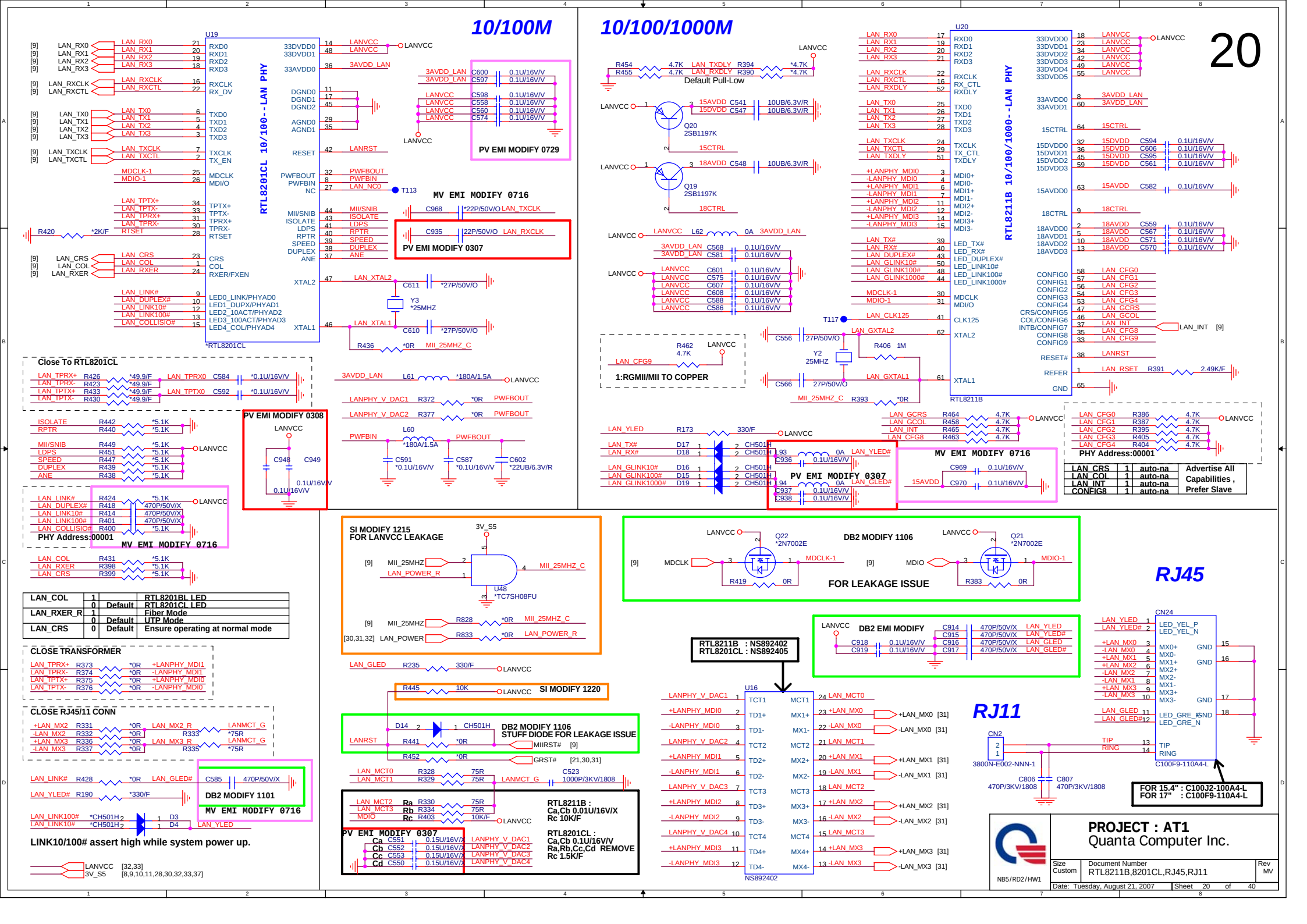
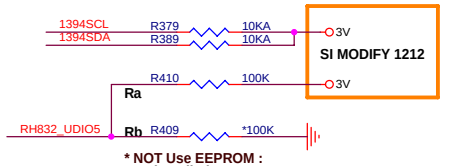


LAN_COL	1		RTL8201BL LED
	0	Default	RTL8201CL LED
LAN_RXER_R	1		Fiber Mode
	0	Default	UTP Mode
LAN_CRS	0	Default	Ensure operating at normal mode

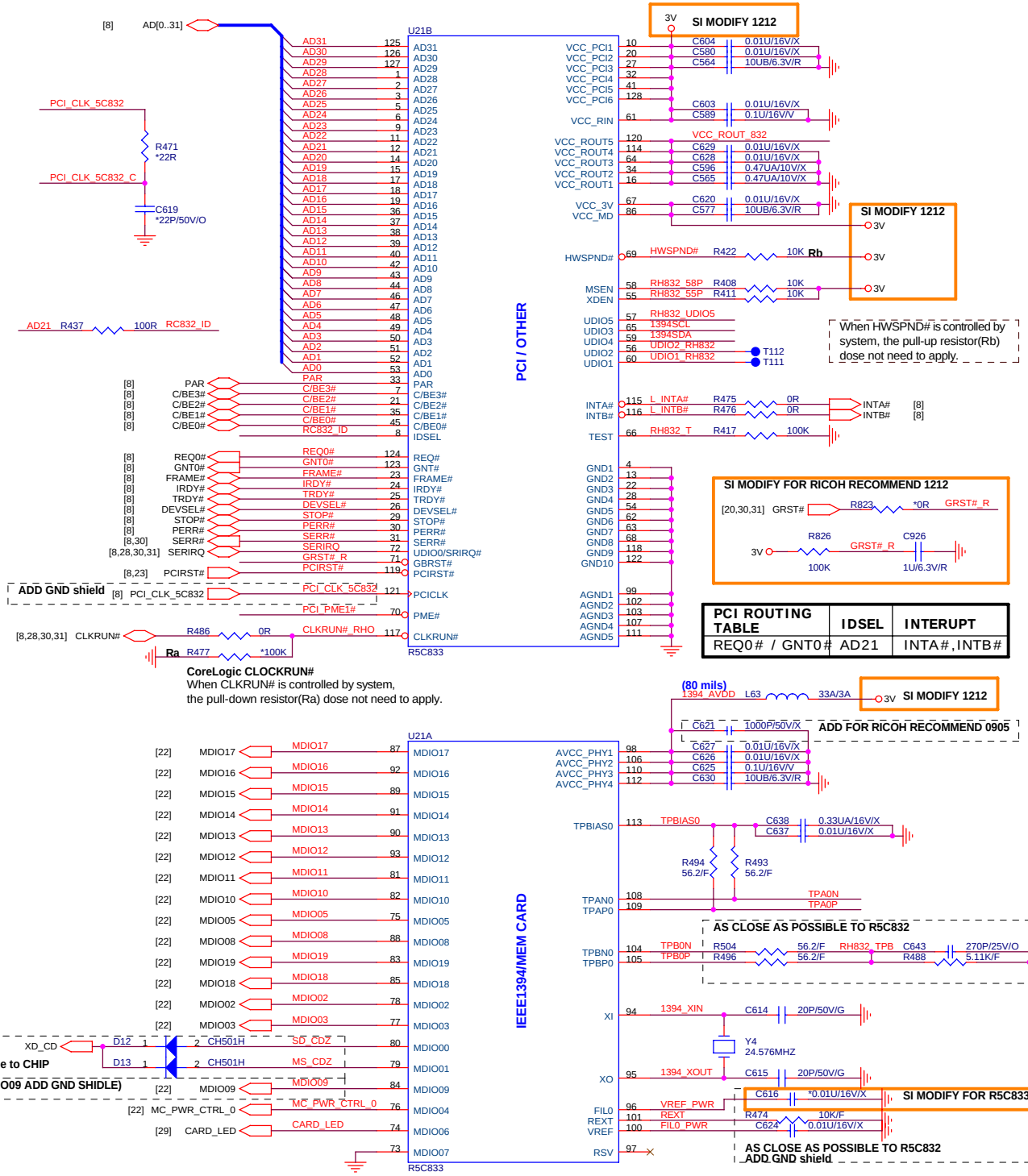
LAN_CRS	1	auto-na	Advertise All Capabilities , Prefer Slave
LAN_COL	1	auto-na	
LAN_INT	1	auto-na	
CONFIG8	1	auto-na	

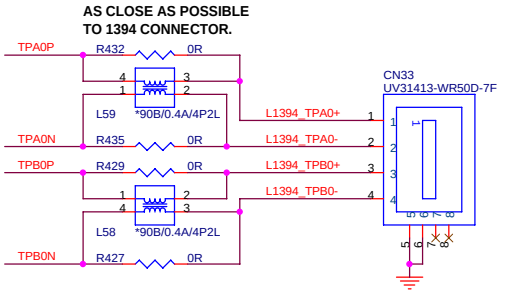
Serial EEPROM



*** NOT Use EEPROM :**
Ra : installed
Rb : NOT installed

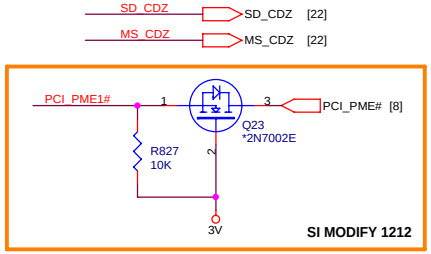
*** Use EEPROM :**
Ra : NOT installed
Rb : installed





***TPA/TPA#,TPB/TPB# pair trace : As close as possible.**
***TPA/TPA#,TPB/TPB# pair trace : Same length electrically.And layout with shields.**

***Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).**



3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,22,23,26,27,28,29,30,31,32,33,36,38]

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	R5C832V00,1394 PORT	MV

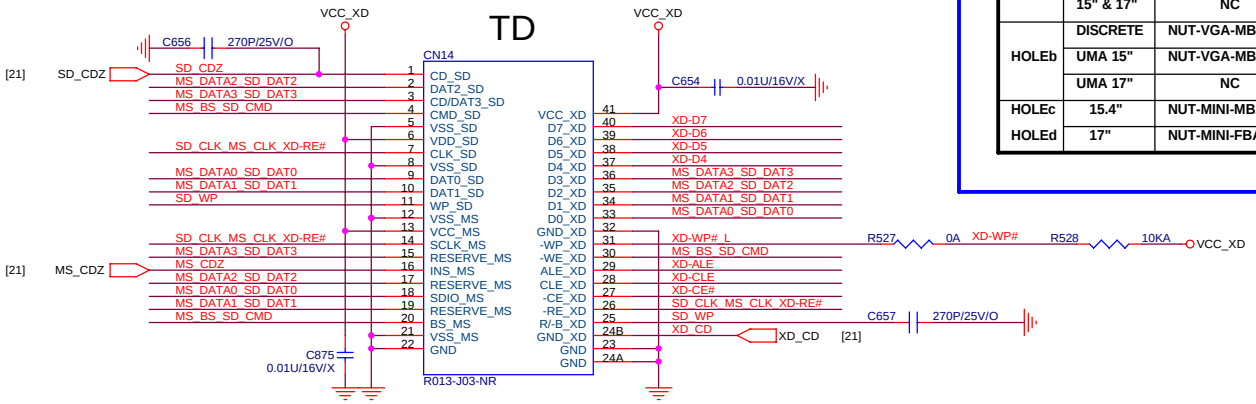
NB5/RD2/HW1

Date: Tuesday, August 21, 2007 Sheet 21 of 40

4 IN1 CARD READER

XD,MMC/SD,MS/MSP

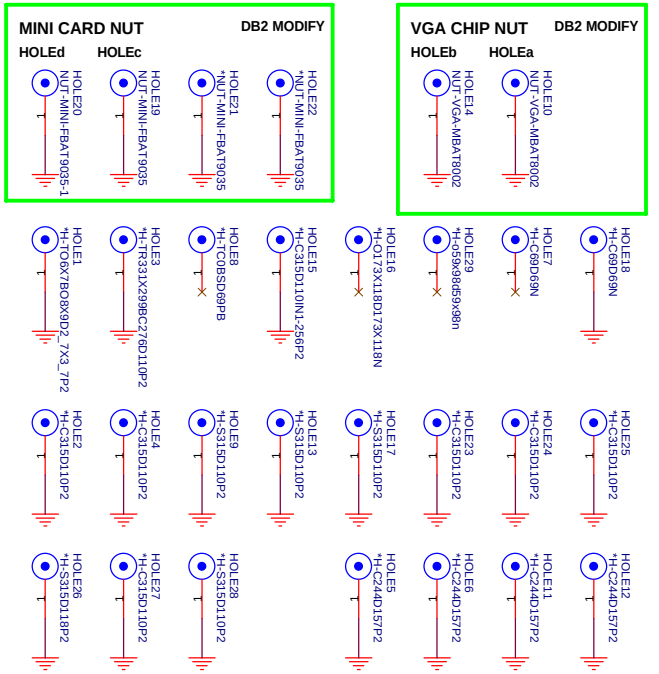
TD

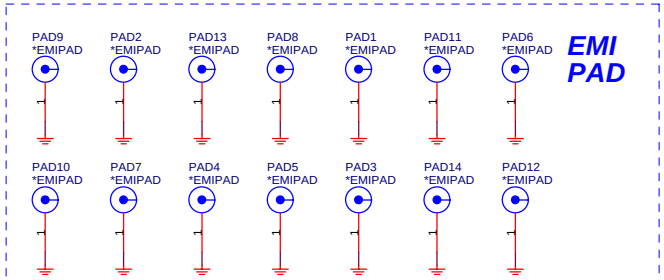


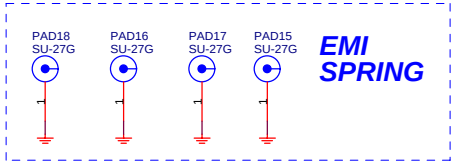
Note: Need to add WP# and CD# pad for Proconn

15.4" & 17" AND DISCRETE & UMA		
HOLE	STATUS	NUT
HOLEa	DISCRETE	NUT-VGA-MBAT8002
	15" & 17"	NC
HOLEb	DISCRETE	NUT-VGA-MBAT8002
	UMA 15"	NUT-VGA-MBAT8002
	UMA 17"	NC
HOLEc	15.4"	NUT-MINI-MBAT8004
HOLEd	17"	NUT-MINI-FBAT9035

SCREW HOLE

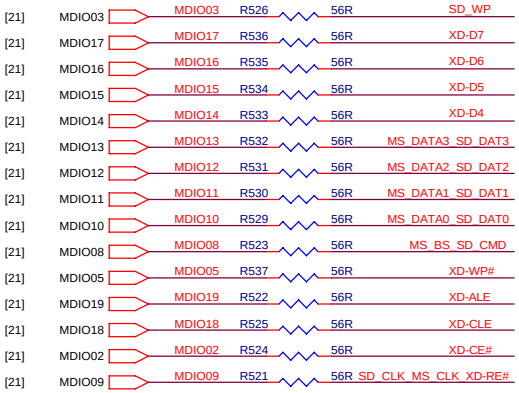


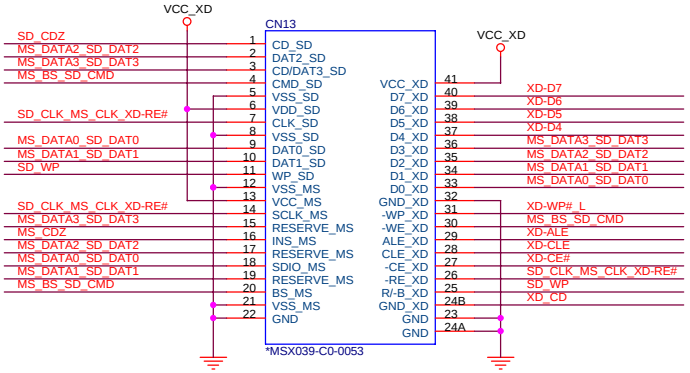




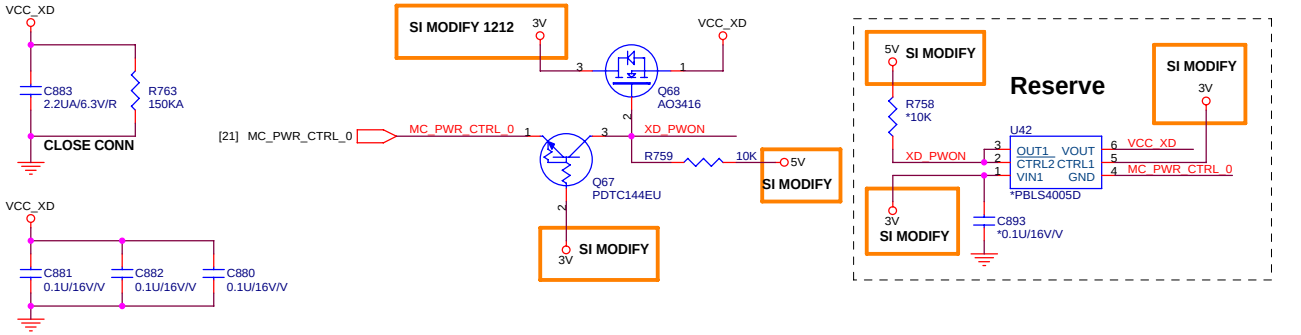
3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,23,26,27,28,29,30,31,32,33,36,38]
5V [13,18,19,23,25,26,27,28,29,31,32,33,36,38]

2ND SOURCE





*** NOT INSTALL FOR 2ND SOURCE CO-LAYOUT USED***



PROJECT : AT1
Quanta Computer Inc.

NB5/RD2/HW1

Size	Document Number	Rev
Custom	CARD_READER,HOLE,NUT,SPRING	MV

Date: Tuesday, August 21, 2007 Sheet 22 of 40

VDDIO is used in determining which HD Audio bus voltage is present on the system. When VDDIO is +1.5V, the device will use 1.5v signaling on the HDA interface pins; when VDDIO is +3.3v, the device will use 3.3v signaling on the HDA interface pins.

For associated Line Side Device portion of this design see Conexant RD02-D450 reference schematic

R819 AT1/2 ADD ATLS NC

R818 ATSA add 4.7K

INTERNAL SPEAKERS

HEADPHONE & DOCKING

INTERNAL MIC

EXTERNAL MIC

DOCKING EXTERNAL MIC

GAIN	10K GPIO RESISTORS GPIO1	GPIO2
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-16dB	Omit	Populate

Default gain is -6dB without populating the 10K ohm pull down resistors going to GPIO1 and GPIO2

RA FOR ATLS only

TO AUDIO/B CON.

DB2 MODIFY 1027
NC for HP spec does not support SPDIF

SI MODIFY 1212

HP_PLUG=H ---- EAR PHONE
HP_PLUG=L ---- PR_SPKER
MIC JACK DECT PIN IS NORMAL CLOSE TYPE

MIC_PLUG=L ---- INTERNAL MIC
MIC_PLUG=H ---- EXTERNAL MIC
MIC JACK DECT PIN IS NORMAL CLOSE TYPE

3800-E14N-00R

EXTERNAL MIC SW(PORTB L/R)

INTERNAL MIC SW(MIC L/R)

DOCK MIC DETECT

EAR PHONE SYSTEM/DOCK SW

3AVDD	[25]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,26,27,28,29,30,31,32,33,36,38]
5V	[13,18,19,22,25,26,27,28,29,31,32,33,36,38]
5VPCU	[10,33,34,35,36,37,38]

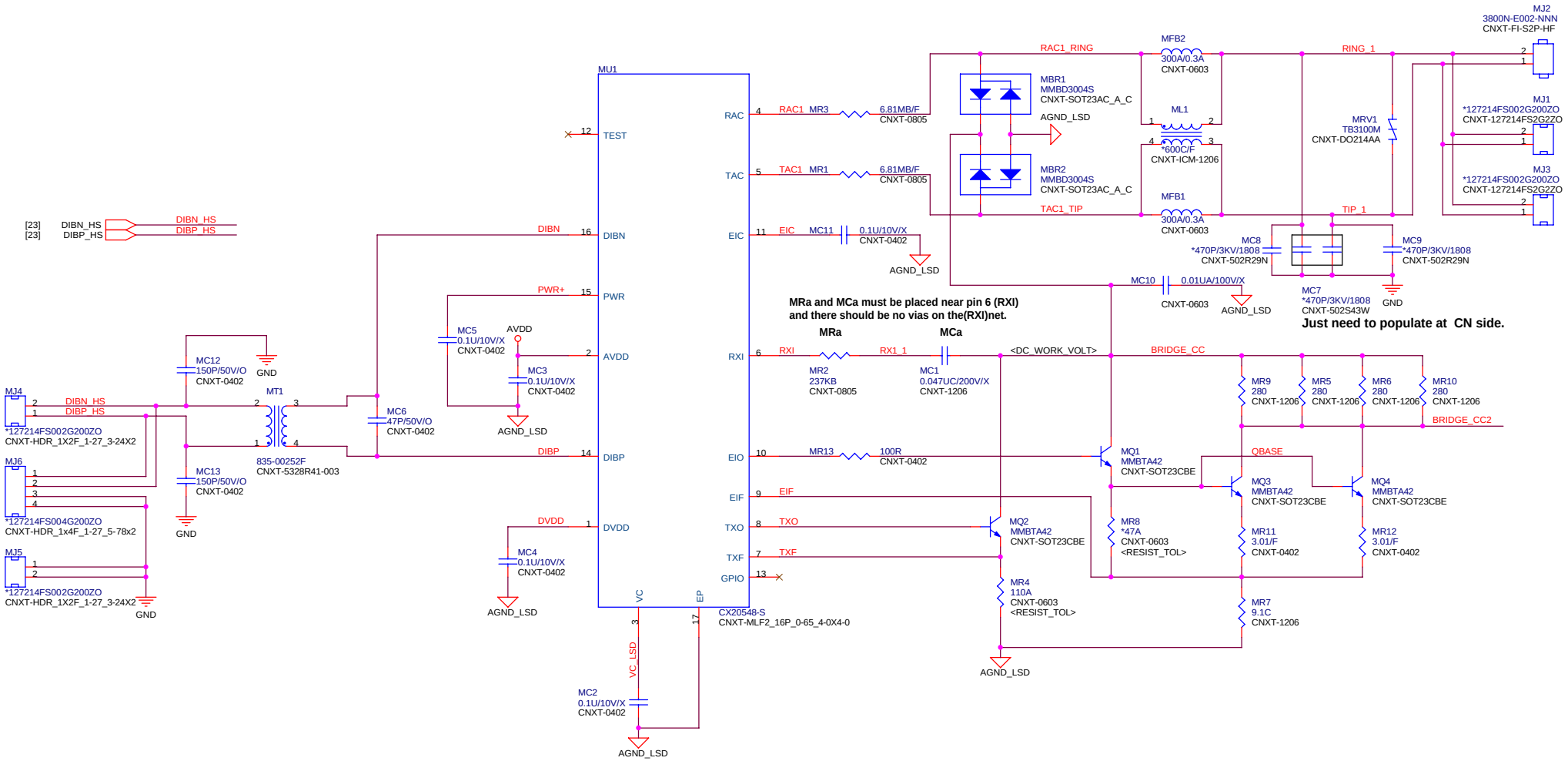
NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDA_CX20561-12,AUDIO_BOARD	MV

Date: Tuesday, August 21, 2007 Sheet 23 of 40

Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005
4		



	PROJECT : AT1 Quanta Computer Inc.		
NB5/RD2/HW1	Size: Custom	Document Number: MODEM(DAA)_CX20548-S	Rev: MV
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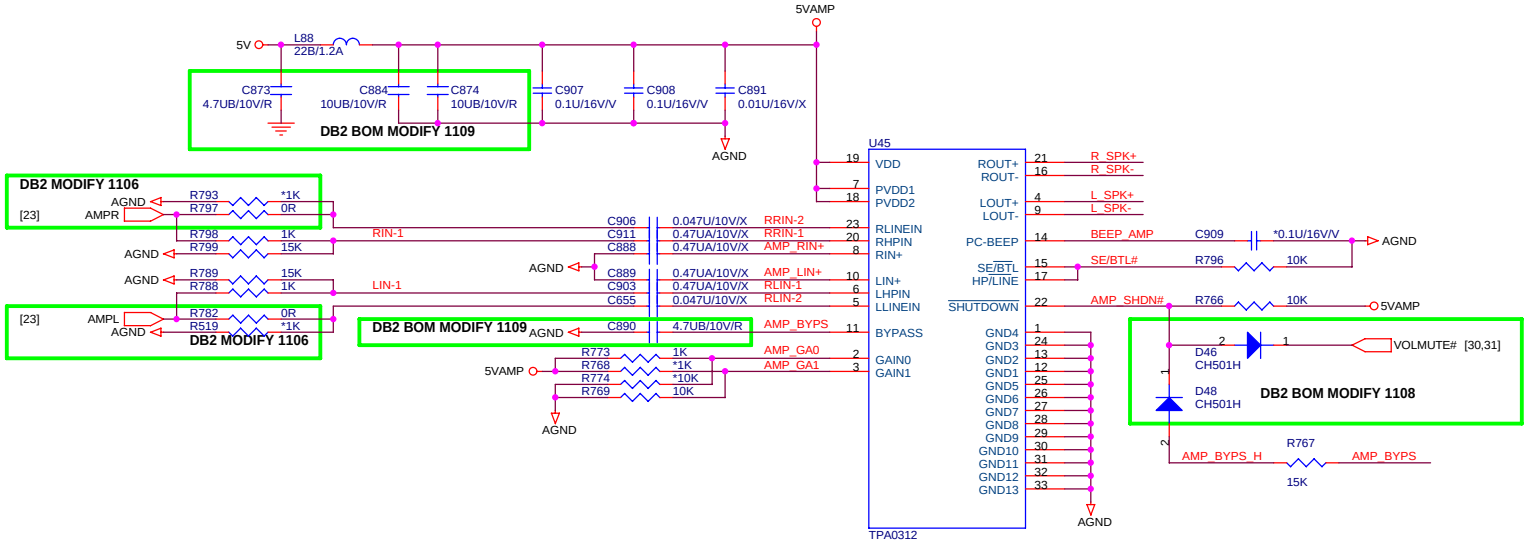
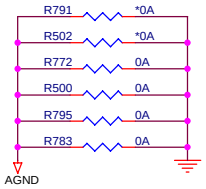
AUDIO AMPLIFIER

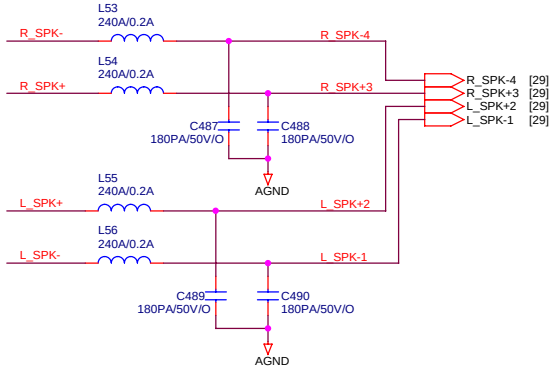


0312 Gain Table

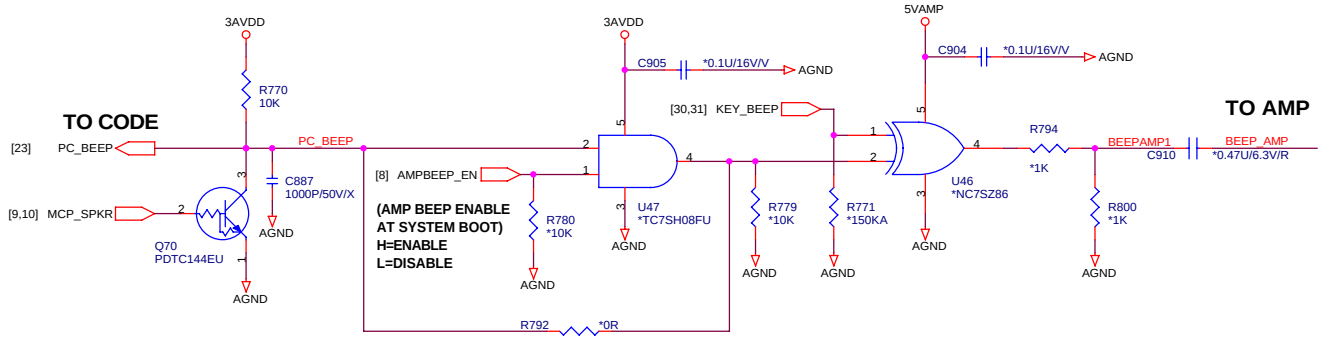
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	**0**	**0**	**15.6dB**
1	1	0	21.6dB
x	x	1	4.1dB



INT. SPEAKER



PCSPK BEEP



3AVDD 5V [23] [13,18,19,22,23,26,27,28,29,31,32,33,36,38]

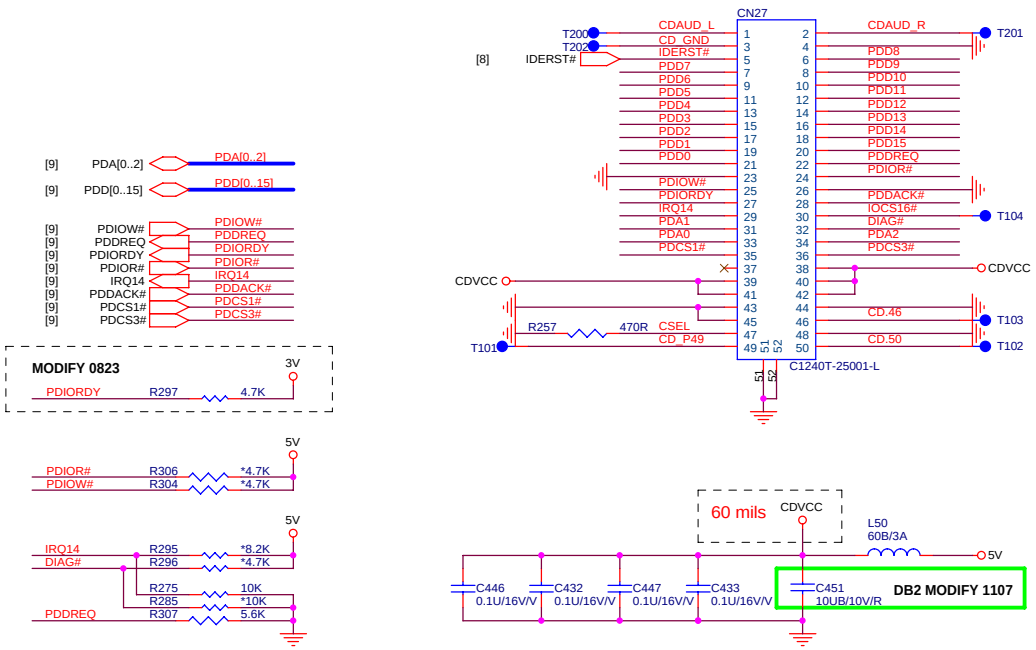
PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA0312	MV

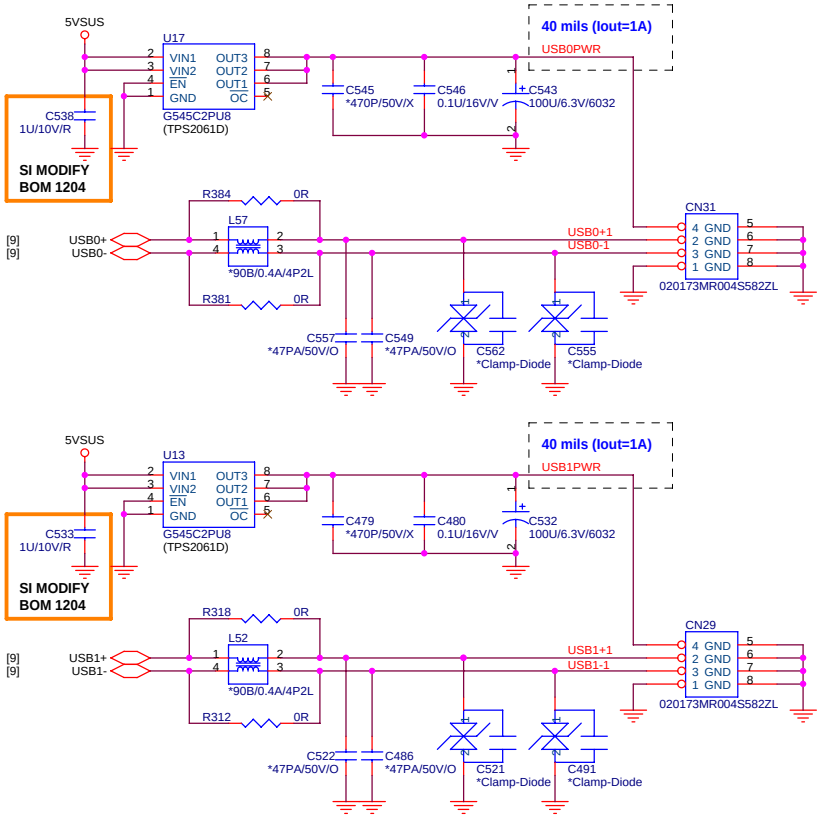
NB5/RD2/HW1

Date: Tuesday, August 21, 2007 Sheet 25 of 40

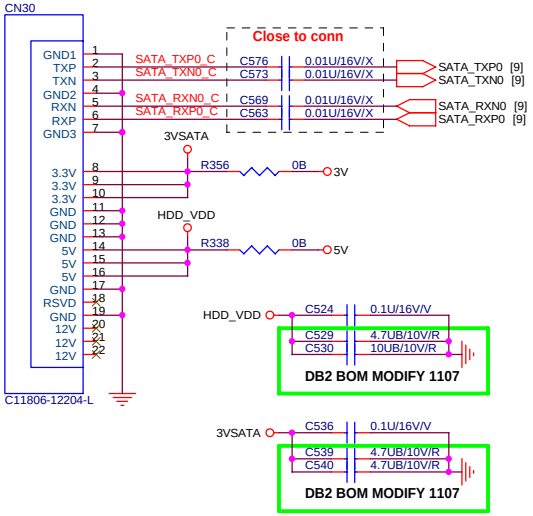
CD-ROM



USB DIP CONNECTOR X 2

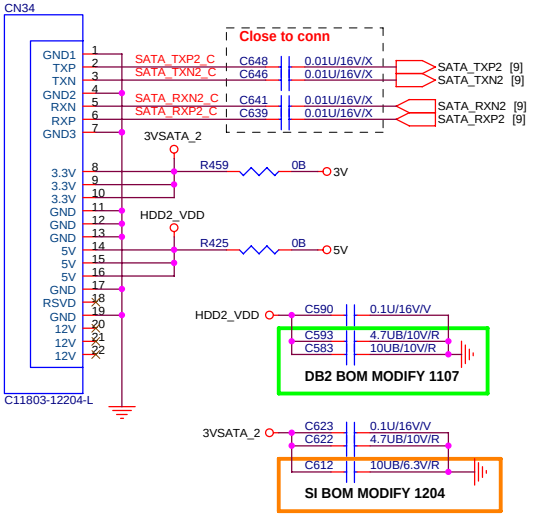


SATA_1 CONNECTOR

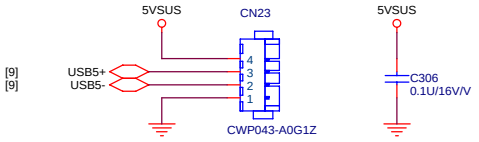


For 17"W Second HDD

SATA_2 CONNECTOR



USB WIRE TO DC BOARD X 1



3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,27,28,29,30,31,32,33,36,38]
5VSUS [18,28,30,31,32,33,37]
5V [13,18,19,22,23,25,27,28,29,31,32,33,36,38]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDDx2,CD-ROM,USBx3	MV
Date: Tuesday, August 21, 2007	Sheet 26 of 40	

Mini PCI-E Card 1
WLAN

1) Pins 39, 41 should be 3V
2) Pins 37, 43 should be GND

CN36

DB2 MODIFY

PV MODIFY from HP #259418 3/16

MODIFY FOR EMI SOLUTION 0911

FOR 15.4" ONLY

SW3 *NSS508-012N-AAAD1B-A

Q65 2N7002E

Q62 2N7002E

Q64 PDTC144EU

Mini PCI-E Card 2
(WWAN/SIM)
FOR 15.4" ONLY (RESERVE)

No need to stuff.

U40

(To GPIO pin)

SI BOM MODIFY 1213

FOR KBC DEBUG

CN37

DB2 MODIFY FORWLAN

FOR 17" SW BOARD

SI MODIFY 1213 FOR WLAN

U39 *CM1213_04ST

CN35 *CFS064-A0G16

D47 *BAV99W

Q61 *PDTC144EU

Q66 *PDTC144EU

*1827680-1

67910-0002

1.5V	[28,31,32,36]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,28,29,30,31,32,33,36,38]
3VSUS	[28,29,32,33]
5V	[13,18,19,22,23,25,26,28,29,31,32,33,36,38]

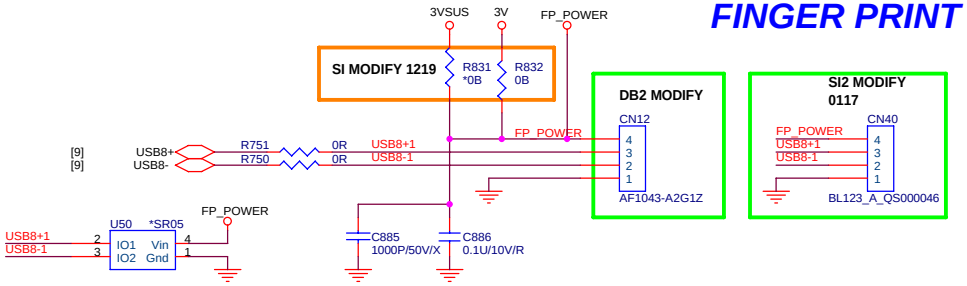
PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI CARDx2 (WLAN,WWAN,SIM)	MV

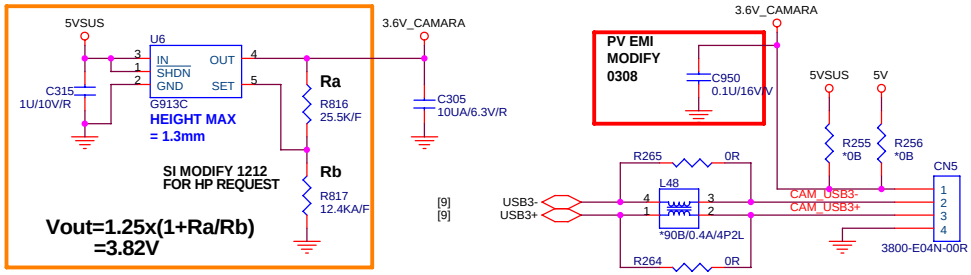
NB5/RD2/HW1

Date: Tuesday, August 21, 2007 Sheet 27 of 40

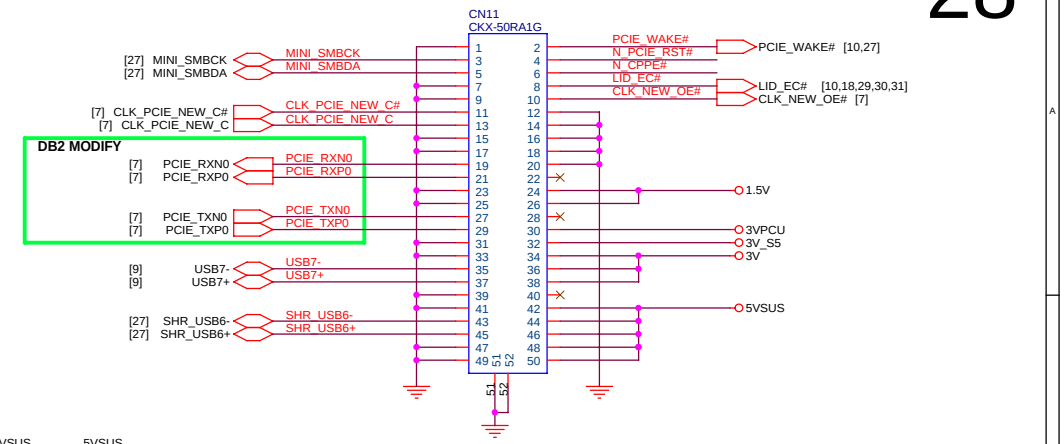
FINGER PRINT

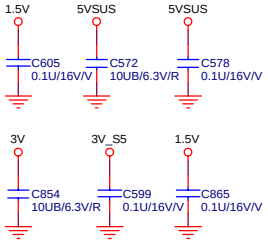


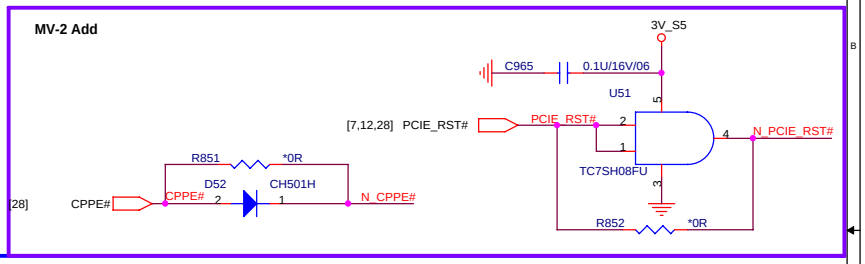
CAMERA



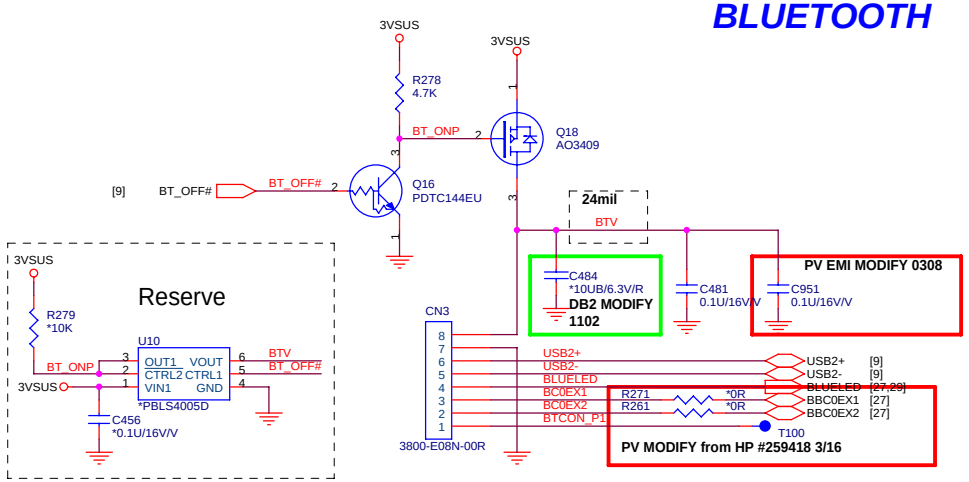
NEW CARD

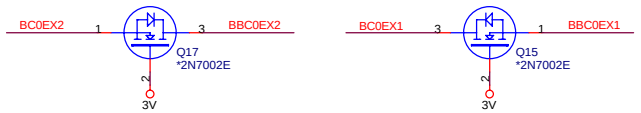




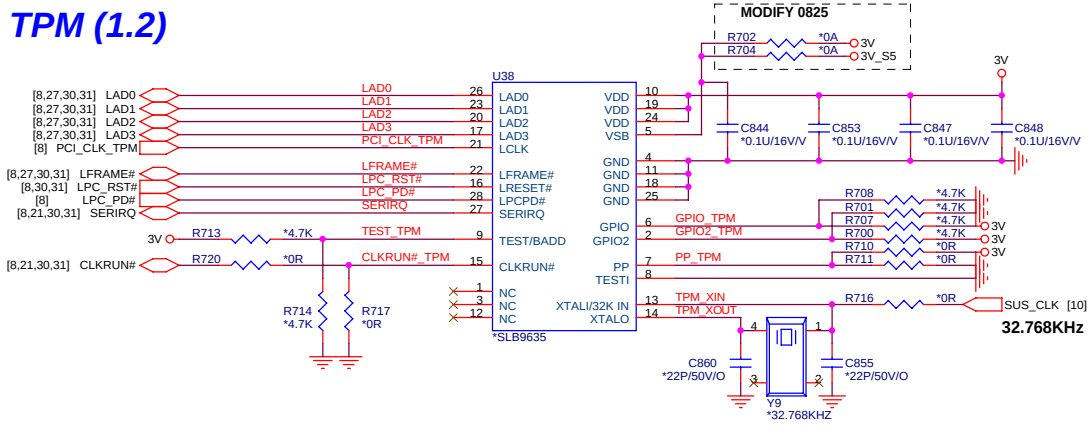


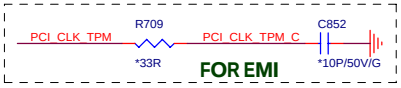
BLUETOOTH





TPM (1.2)





Address

	BADD
HIGH	4EH/4F (dafault)
LOW	2EH/2FH

*** DEFAULT**

PP (PHYSICAL PRESENCE)	
*L	PLATFORM PROTECT
H	USER ACCESS

1.5V	[27,31,32,36]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,29,30,31,32,33,36,38]
3VSUS	[27,29,32,33]
3V_S5	[8,9,10,11,20,30,32,33,37]
3VPCU	[9,14,18,29,30,31,33,34,35]
5V	[13,18,19,22,23,25,26,27,29,31,32,33,36,38]
5VSUS	[18,26,30,31,32,33,37]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD,CAMER,TPM,F/P,B/T	MV

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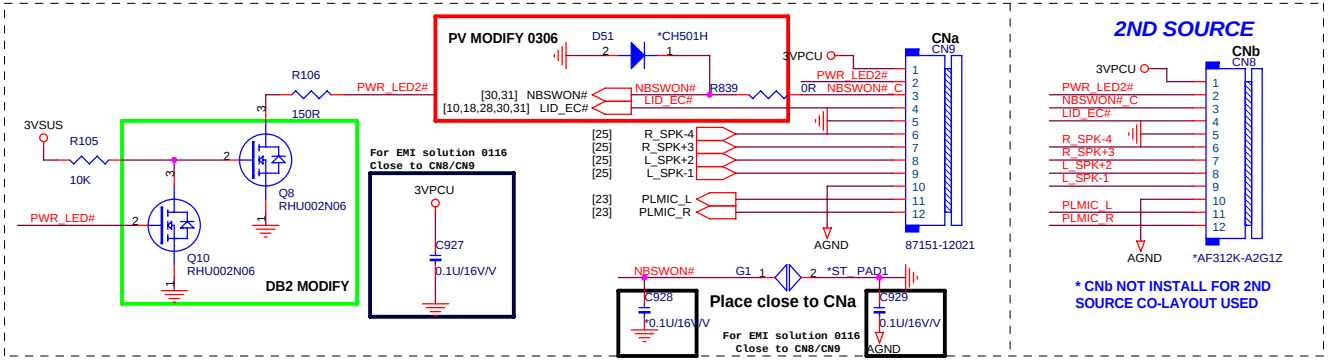
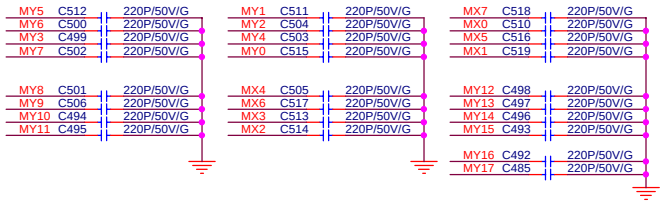
FOR POWER ON AND INTERNAL SPK / MIC SW BOARD

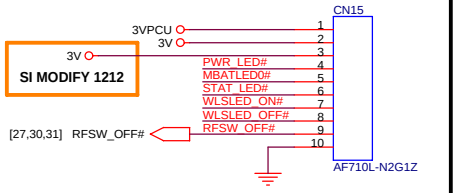


2ND SOURCE

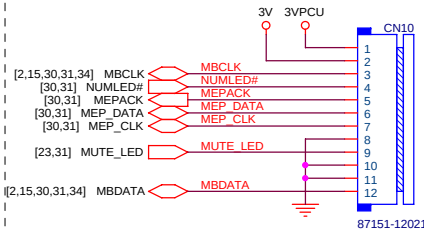
* CNb NOT INSTALL FOR 2ND SOURCE CO-LAYOUT USED



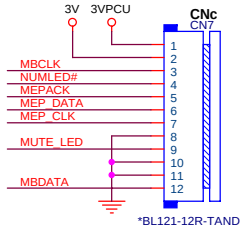
FOR 17" LED AND WIRLESS SW BOARD



FOR QLB SW BOARD

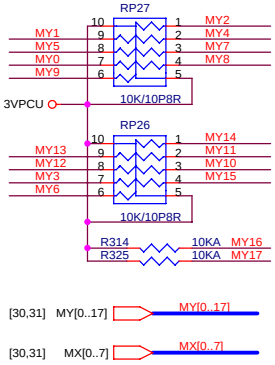


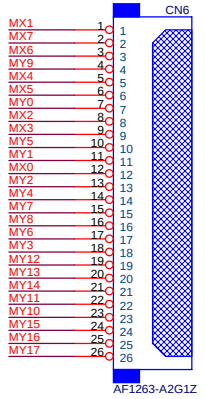
2ND SOURCE

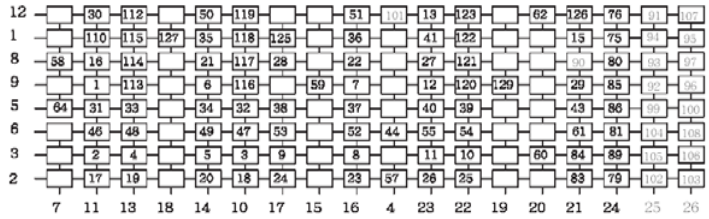


* CNc NOT INSTALL FOR 2ND SOURCE CO-LAYOUT USED

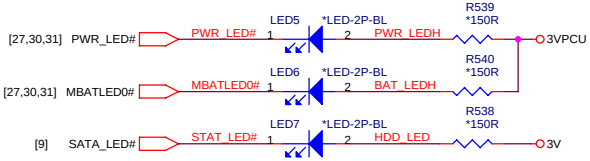
KEYBOARD PULL-UP





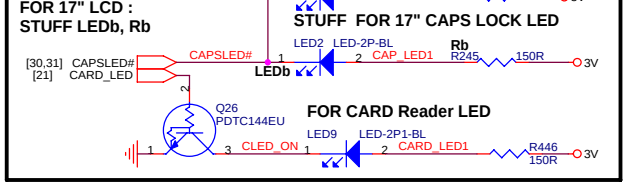


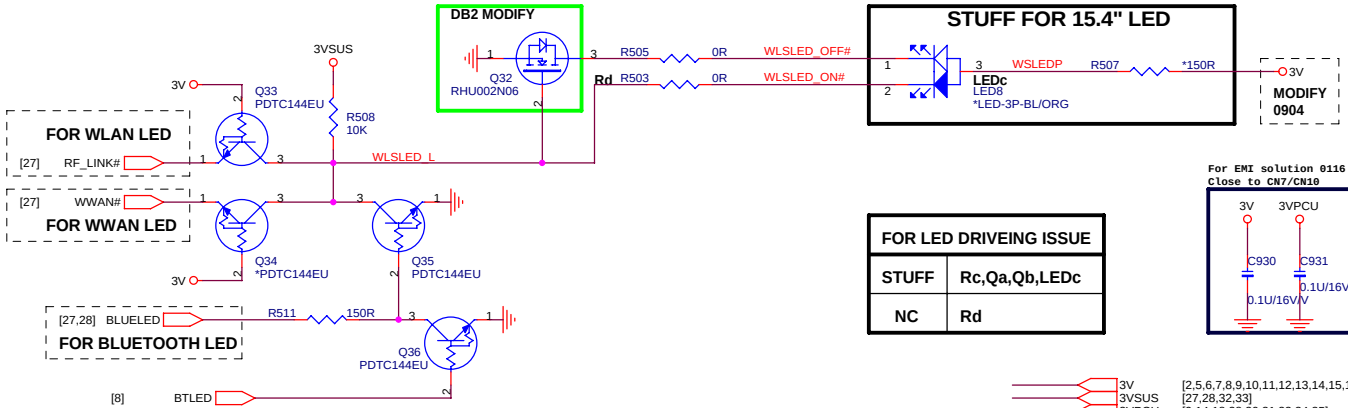
STUFF FOR 15.4" LED USED



FOR 15.4" LCD : STUFF LEDa, Ra

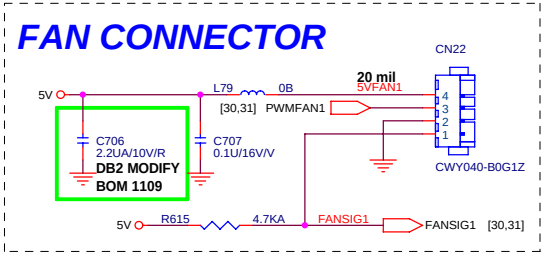
FOR 17" LCD : STUFF LEDb, Rb





FOR LED DRIVEING ISSUE	
STUFF	Rc,Qa,Qb,LEDc
NC	Rd

FAN CONNECTOR



3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,30,31,32,33,36,38]
3VSUS	[27,28,32,33]
3VPCU	[9,14,18,28,30,31,33,34,35]
5V	[13,18,19,22,23,25,26,27,28,31,32,33,36,38]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB,FAN,LED,SW (PWR,QLB,LED)	MV

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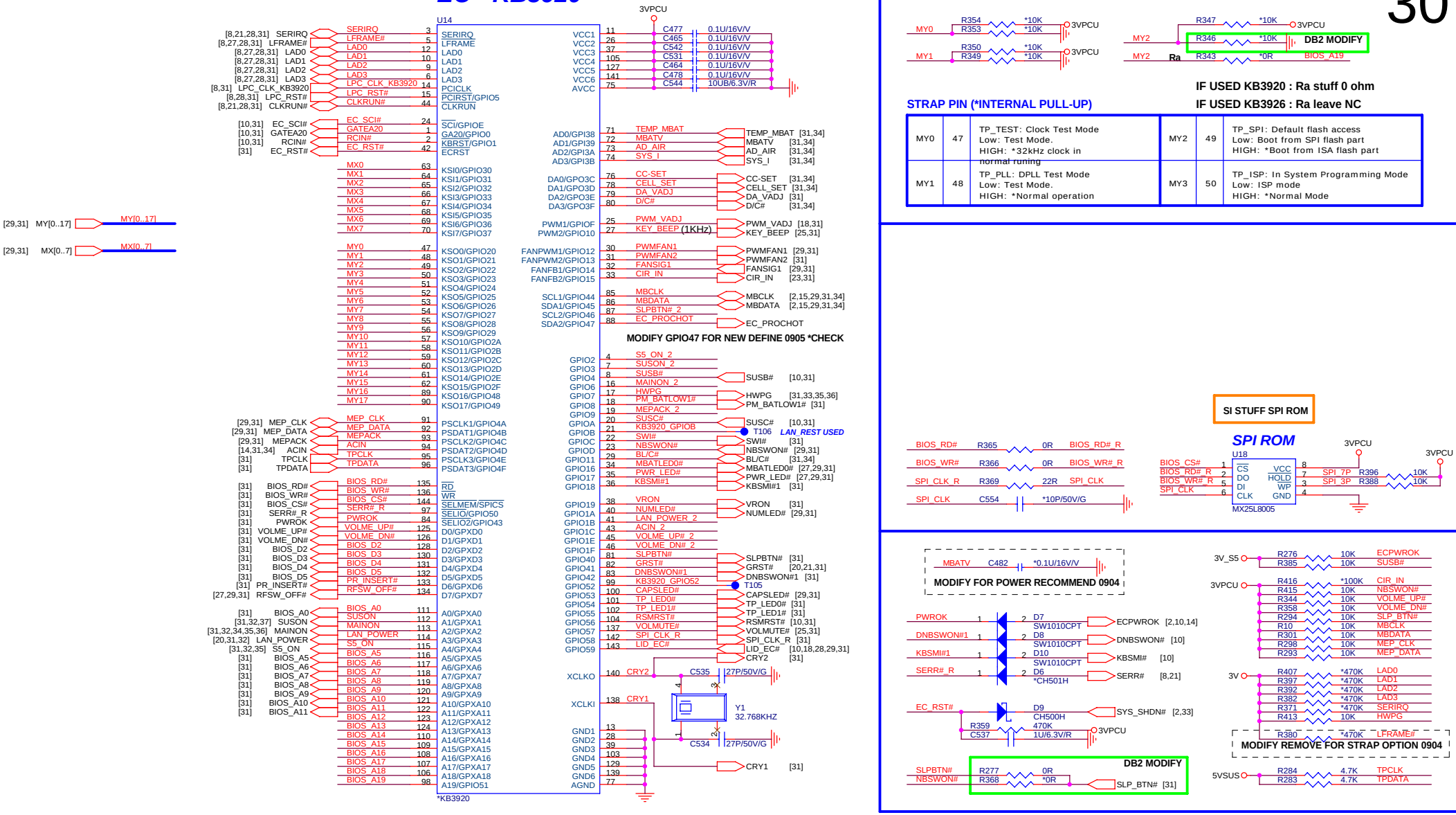
EC - KB3920



DB2 MODIFY

IF USED KB3920 : Ra stuff 0 ohm

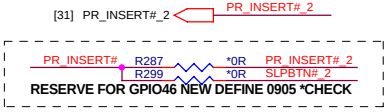
IF USED KB3926 : Ra leave NC

STRAP PIN (*INTERNAL PULL-UP)

MY0	47	TP_TEST: Clock Test Mode Low: Test Mode. HIGH: *32kHz clock in normal runing	MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: *Boot from ISA flash part
MY1	48	TP_PLL: DPLL Test Mode Low: Test Mode. HIGH: *Normal operation	MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: *Normal Mode

SI STUFF SPI ROM

SPI ROM



3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,31,32,33,36,38]
3V_S5	[8,9,10,11,20,28,32,33,37]
3VPCU	[9,14,18,28,29,31,33,34,35]
5VSUS	[18,26,28,31,32,33,37]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB3920,SPI_ROM	MV

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EC - KB3926

U15 — KB3926

[8,21,28,30] SERIRQ	SERIRQ	3	SERIRQ	VCC1	9
[8,27,28,30] LFRAME#	LFRAME#	4	LFRAME	VCC2	22
[8,27,28,30] LAD0	LAD0	10	LAD0	VCC3	33
[8,27,28,30] LAD1	LAD1	8	LAD1	VCC4	96
[8,27,28,30] LAD2	LAD2	7	LAD2	VCC5	111
[8,27,28,30] LAD3	LAD3	5	LAD3	VCC6	125
[8,30] LPC_CLK_KB3920	LPC_CLK_KB3920	12	PCICLK	AVCC	67 — 3VPCU
[8,28,30] LPC_RST#	LPC_RST#	13	PCIRST/GPIO5		
[8,21,28,30] CLKRUN#	CLKRUN#	38	CLKRUN		
			SCI/GPIOE		
[10,30] EC_SCI#	EC_SCI#	20	GA20/GPIO0		
[10,30] GATEA20	GATEA20	1	KBRST/GPIO1		
[10,30] RCIN#	RCIN#	2	ECRST		
[30] EC_RST#	EC_RST#	37			
			AD0/GPI38	63	TEMP_MBAT — TEMP_MBAT [30,34]
			AD1/GPI39	64	MBATV — MBATV [30,34]
			AD2/GPI3A	65	AD_AIR — AD_AIR [30,34]
			AD3/GPI3B	66	SYS_I — SYS_I [30,34]
	MX0	55			
	MX1	56	KSI0/GPIO30		
	MX2	57	KSI1/GPIO31		
	MX3	58	KSI2/GPIO32		
	MX4	59	KSI3/GPIO33		
	MX5	60	KSI4/GPIO34		
	MX6	61	KSI5/GPIO35		
	MX7	62	KSI6/GPIO36		
			KSI7/GPIO37		
	MY0	39			
	MY1	40	KSO0/GPIO20		
	MY2	41	KSO1/GPIO21		
	MY3	42	KSO2/GPIO22		
	MY4	43	KSO3/GPIO23		
	MY5	44	KSO4/GPIO24		
	MY6	45	KSO5/GPIO25		
	MY7	46	KSO6/GPIO26		
	MY8	47	KSO7/GPIO27		
	MY9	48	KSO8/GPIO28		
	MY10	49	KSO9/GPIO29		
	MY11	50	KSO10/GPIO2A		
	MY12	51	KSO11/GPIO2B		
	MY13	52	KSO12/GPIO2C		
	MY14	53	KSO13/GPIO2D		
	MY15	54	KSO14/GPIO2E		
	MY16	81	KSO15/GPIO2F		
	MY17	82	KSO16/GPIO48		
			KSO17/GPIO49		
			PWM1/GPIOE	21	PWM_VADJ — PWM_VADJ [18,30]
			PWM2/GPIO10	23	KEY_BEEP (1KHz) — KEY_BEEP [25,30]
			DA0/GPO3C	68	CC-SET — CC-SET [30,34]
			DA1/GPO3D	70	CELL_SET — CELL_SET [30,34]
			DA2/GPO3E	71	DA_VADJ — DA_VADJ [30]
			DA3/GPO3F	72	D/C# — D/C# [30,34]
			FANPWM1/GPIO12	26	PWMFAN1 — PWMFAN1 [29,30]
			FANPWM2/GPIO13	27	PWMFAN2 — PWMFAN2 [30]
			FANFB1/GPIO14	28	FANSIG1 — FANSIG1 [29,30]
			FANFB2/GPIO15	29	CIR_IN — CIR_IN [23,30]
			SCL1/GPIO44	77	MBCLK — MBCLK [2,15,29,30,34]
			SDA1/GPIO45	78	MBDATA — MBDATA [2,15,29,30,34]
			SCL2/GPIO46	79	PR_INSERT#_2 — PR_INSERT#_2 [30]
			SDA2/GPIO47	80	EC_PROCHOT# — EC_PROCHOT# [2]
					MODIFY GPIO46,47 FOR NEW DEFINE 0905 *CHECK
			GPIO4	6	SUSB# — SUSB# [10,30]
			GPIO7	14	HWPG — HWPG [30,33,35,36]
			GPIO8	15	PM_BATLOW1# — PM_BATLOW1# [30]
[29,30] MEP_CLK	MEP_CLK	83			
[29,30] MEP_DATA	MEP_DATA	84	PSCLK1/GPIO4A		
[29,30] MEPACK	MEPACK	85	PSDAT1/GPIO4B		
[14,30,34] ACIN	ACIN	86	PSCLK2/GPIO4C		
[30] TPCLK	TPCLK	87	PSDAT2/GPIO4D		
[30] TPDATA	TPDATA	88	PSCLK3/GPIO4E		
			PSDAT3/GPIO4F		
[30] BIOS_RD#	BIOS_RD#	119	RD		
[30] BIOS_WR#	BIOS_WR#	120	WR		
[30] BIOS_CS#	BIOS_CS#	128	SELMEM/SPICS		
[30] SERR#_R	SERR#_R	89	SELIO/GPIO50		
[30] PWROK	PWROK	76	SELIO2/GPIO43		
[30] VOLME_UP#	VOLME_UP#	109	D0/GPXD0		
[30] VOLME_DN#	VOLME_DN#	110	D1/GPXD1		
[30] BIOS_D2	BIOS_D2	112	D2/GPXD2		
[30] BIOS_D3	BIOS_D3	114	D3/GPXD3		
[30] BIOS_D4	BIOS_D4	115	D4/GPXD4		
[30] BIOS_D5	BIOS_D5	116	D5/GPXD5		
[30] PR_INSERT#	PR_INSERT#	117	D6/GPXD6		
[27,29,30] RFSW_OFF#	RFSW_OFF#	118	D7/GPXD7		
			GPIOA	16	SUSC# — SUSC# [10,30]
			GPIOB	17	KB3926_GPIOB — T107 LAN_REST USED
			GPIOC	18	SWI# — SWI# [30]
			GPIOD	19	NBSWON# — NBSWON# [29,30]
			GPIO11	25	BL/C# — BL/C# [30,34]
			GPIO16	30	MBATLED0# — MBATLED0# [27,29,30]
			GPIO17	31	PWR_LED# — PWR_LED# [27,29,30]
			GPIO18	32	KBSMI#1 — KBSMI#1 [30]
			GPIO19	34	VRON — VRON [30]
			GPIO1A	36	NUMLED# — NUMLED# [29,30]
[30] BIOS_A0	BIOS_A0	97	A0/GPXA0		
[30,32,37] SUSON	SUSON	98	A1/GPXA1		
[30,32,34,35,36] MAINON	MAINON	99	A2/GPXA2		
[20,30,32] LAN_POWER	LAN_POWER	100	A3/GPXA3		
[30,32,35] S5_ON	S5_ON	101	A4/GPXA4		
[30] BIOS_A5	BIOS_A5	102	A5/GPXA5		
[30] BIOS_A6	BIOS_A6	103	A6/GPXA6		
[30] BIOS_A7	BIOS_A7	104	A7/GPXA7		
[30] BIOS_A8	BIOS_A8	105	A8/GPXA8		
[30] BIOS_A9	BIOS_A9	106	A9/GPXA9		
[30] BIOS_A10	BIOS_A10	107	A10/GPXA10		
[30] BIOS_A11	BIOS_A11	108	A11/GPXA11		
			GPIO40	73	SLPBTN# — SLPBTN# [30]
			GPIO41	74	GRST# — GRST# [20,21,30]
			GPIO42	75	DNBSWON#1 — DNBSWON#1 [30]
			GPIO52	90	KB3926_GPIO52 — T109
			GPIO53	91	CAPSLED# — CAPSLED# [29,30]
			GPIO54	92	TP_LED0# — TP_LED0# [30]
			GPIO55	93	TP_LED1# — TP_LED1# [30]
			GPIO56	95	RSMRST# — RSMRST# [10,30]
			GPIO57	121	VOLMUTE# — VOLMUTE# [25,30]
			GPIO58	126	SPI_CLK_R — SPI_CLK_R [30]
			GPIO59	127	LID_EC# — LID_EC# [10,18,28,29,30]
			XCLKO	123	CRY2 — CRY2 [30]
			XCLKI	122	CRY1 — CRY1 [30]
T108	KB3926_V18R	124	V18R		
			GND1	11	
			GND2	24	
			GND3	35	
			GND4	94	
			GND5	113	
			AGND	69	

SPI H/W STRAPPING: BIOS_A0 — R315 1K — DB2 MODIFY 1101

[29,30] MY[0..17] — MY[0..17]

[29,30] MX[0..7] — MX[0..7]

LPC_CLK_KB3920 — R421 *0R — LPC_CLK_KB3920_C — C579 *10P/50V/G
MODIFY FOR EMI SOLUTION 0911

CABLE DOCK

CN21 — QL1122L-H212CR-7F-44P

DB2 MODIFY 1107 FOR EMI SOLUTION

[19] CRT_G1	CRT_G1	R36 0R	CRT_GDK	38	
[19] CRT_R1	CRT_R1	R32 0R	CRT_RDK	40	
[6,13,19] DDCDAT	DDCDAT	R51 0R	DDAT_DK	34	
[19] CRT_B1	CRT_B1	R40 0R	CRT_BDK	36	
[19] HSYNC2	HSYNC2	R25 0R	HSY_DK	30	
[6,13,19] DDCCLK	DDCCLK	R53 0R	DCLK_DK	32	
			USB4-1	26	
[19] VSYNC2	VSYNC2	R26 0R	VSY_DK	28	
			USB4+1	22	
[20] +LAN_MX3	+LAN_MX3			24	
[20] -LAN_MX3	-LAN_MX3			18	
[20] +LAN_MX2	+LAN_MX2			20	
[20] -LAN_MX2	-LAN_MX2			14	
[20] +LAN_MX1	+LAN_MX1			16	
[20] -LAN_MX1	-LAN_MX1			10	
[20] +LAN_MX0	+LAN_MX0			12	
[20] -LAN_MX0	-LAN_MX0			6	
				8	
VIN				2	
				4	
			VSS	42	
				46	

VA_P			VDD	44	
			VDD	43	VA_P
				39	
	SYD_DK	R566 0R	TV_LUMA	37	TV_LUMA [19]
	SCD_DK	R567 0R	TV_CHROMA	35	TV_CHROMA [19]
	SCVBS_DK	R570 0R	TV_COMP	33	TV_COMP [19]
	VIDEO_GND	R576 0R		31	
	CIRIN_DK	R578 0R	CIR_IN	29	CIR_IN [23,30]
	PWR_ON			27	
	MUTE_LED			25	MUTE_LED [23,29]
	SLP_BTN#			23	SLP_BTN# [30]
	JACK_DETECT#			21	JACK_DETECT# [23]
	VOLME_UP#			19	VOLME_UP# [30]
	VOLME_DN#			17	VOLME_DN# [30]
	SPDIF_DOCK			15	
	AUDIO_G	R606 0R	AGND	13	
	RSPK_DK			11	
	LSPK_DK			9	
	RMIC_DK	R588 0R	DOCK_MIC_R	7	DOCK_MIC_R [23]
	LMIC_DK	R599 0R	DOCK_MIC_L	5	DOCK_MIC_L [23]
	MIC_GND	R597 0R	AGND	3	
	DOCK_PRESENT			1	
			VSS	41	
				45	

SPDIF	C723	*270P/25V/O	
JACK_DETECT#	C713	270P/25V/O	
CIR_IN	C710	*120P/50V/O	
VOLME_DN#	C716	*120P/50V/O	

DB2 MODIFY 1030 FOR POWER RECOMMEND

VA — L89 0.015B/4A — L73 0.015B/4A — 150 mils — VA_P
C681 0.1U/25V/V — C682 0.1U/25V/V — MODIFY 0831

5VSUS — R582 1K — DB2 MODIFY 1106 — DK_PWRON — D40 SW1010CPT
5V — D39 SW1010CPT
R60 1.5K/F — PWR_ON
S0: 4V
S3: 2.5V
S4/S5: 0V
*Check voltage on DB

3VPCU — R595 *100K — R600 *0R — PR_INSERT_L# — [30] PR_INSERT#
DOCK_PRESENT — R598 1K — DKPR# — Q50 *MMBT3904 — R602 2KA/F

1.5V — R587 33R — SPDDK_V — SPD_DK — L80 0A — SPDIF_DOCK
Q49 MMBT3904
[12,23] SPDIF — SPDIF — R591 510/F — SPDIF_DK — R589 510/F — C722 68P/50V/G

R67 0A — RSPK_DK — C107 *100U/6.3V/3528 — DOCK_RSPK+ [23]
LSPK_DK — C142 *100U/6.3V/3528 — DOCK_LSPK+ [23]
R81 0A

R61 0R — [9] USB4- — [9] USB4+ — L8 *90B/0.33A/4P2L — R66 0R — USB4-1 — USB4+1

RESERVE FOR EMI SOULTION

TV_LUMA	C55	*82P/50V/O	RSPK_DK	C104	*10P/50V/G
TV_CHROMA	C64	*82P/50V/O	LSPK_DK	C116	*10P/50V/G
TV_COMP	C70	*82P/50V/O	RMIC_DK	C721	*10P/50V/G
SYD_DK	C685	*82P/50V/O	LMIC_DK	C725	*10P/50V/G
SCD_DK	C690	*82P/50V/O			
SCVBS_DK	C699	*82P/50V/O			
CRT_GDK	C36	*10P/50V/G	USB4+1	C95	*10P/50V/G
CRT_RDK	C33	*10P/50V/G	USB4-1	C88	*10P/50V/G
CRT_BDK	C57	*10P/50V/G			
CRT_G1	C37	*10P/50V/G	+LAN_MX0	C762	*10P/50V/G
CRT_R1	C32	*10P/50V/G	-LAN_MX0	C766	*10P/50V/G
CRT_B1	C46	*10P/50V/G	+LAN_MX1	C125	*10P/50V/G
HSY_DK	C31	*10P/50V/G	-LAN_MX1	C117	*10P/50V/G
VSY_DK	C87	*10P/50V/G	+LAN_MX2	C281	*10P/50V/G
DDAT_DK	C65	*10P/50V/G	-LAN_MX2	C294	*10P/50V/G
DCLK_DK	C85	*10P/50V/G	+LAN_MX3	C786	*10P/50V/G
			-LAN_MX3	C788	*10P/50V/G

TOUCH PAD CONNECTOR

SW1 — MX4 — MY7 — *TACT-SWITCH
(Amber) TP_LED0# — LED3 — TPLD1 *150R — R342 — 3V
(Blue) TP_LED1# — TPLD2 *150R — R341 — 3V
*LED-4P-BL/ORG
FOR 15.4"

SW2 — MX4 — MY7 — TACT-SWITCH
(Amber) TP_LED0# — LED4 — TPLD3 150R — R402 — 3V
(Blue) TP_LED1# — TPLD4 150R — R412 — 3V
LED-4P-BL/ORG
FOR 17"

5VSUS — C403 0.1U/16V/V — 25 mils 5VTP — CN4 AF1043-A2G1Z
L36 80A/0.6A — TPCLK — L37 220A/0.2A — TPCLK-1
TPDATA — L38 220A/0.2A — TPDATA-1
C404 *10P/50V/G — C405 *10P/50V/G

1.5V	[27,28,32,36]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,32,33,36,38]
3VPCU	[9,14,18,28,29,30,33,34,35]
5VSUS	[18,26,28,30,32,33,37]
5V	[13,18,19,22,23,25,26,27,28,29,32,33,36,38]
VA	[34]
VIN	[18,32,33,34,35,36,37,38]

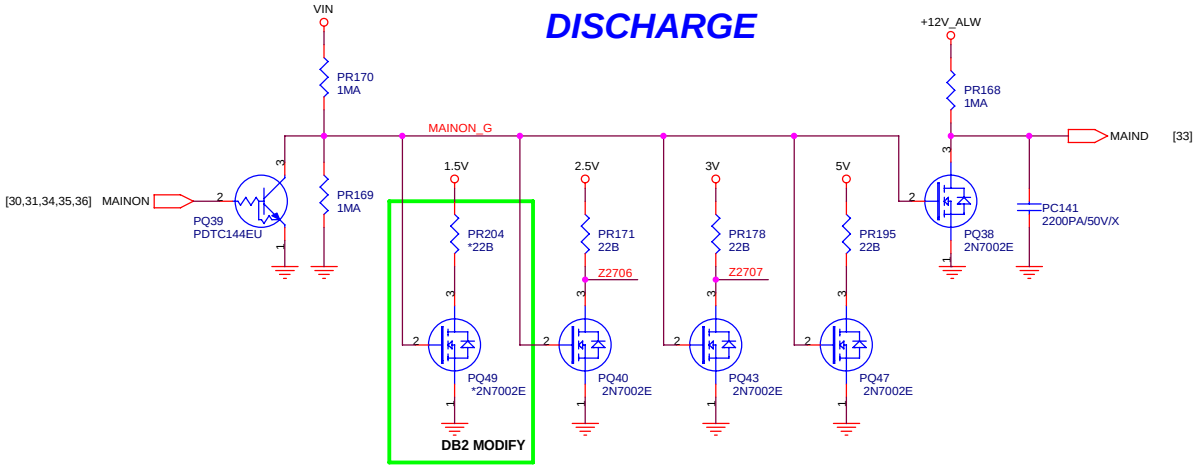
NB5/RD2/HW1

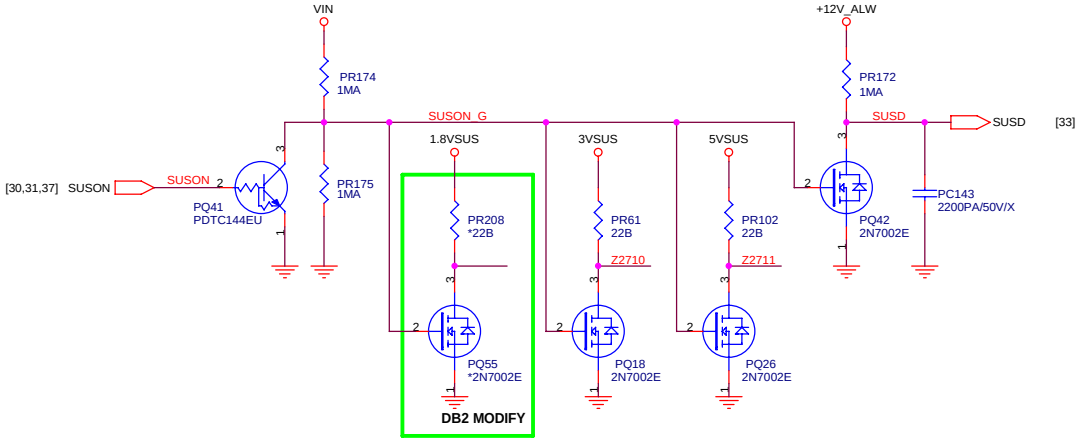
PROJECT : AT1
Quanta Computer Inc.

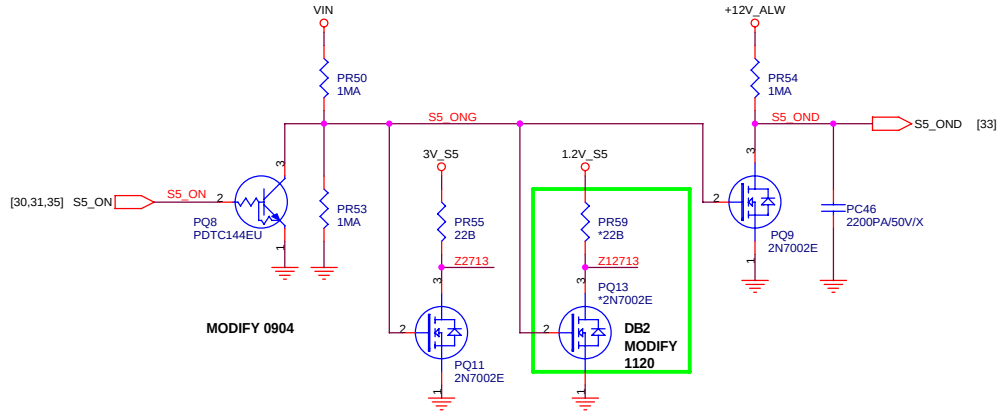
Size	Document Number	Rev
Custom	KB3926,DOCKING,TOUCH_PAD	MV

Date: Tuesday, August 21, 2007 — Sheet 31 of 40

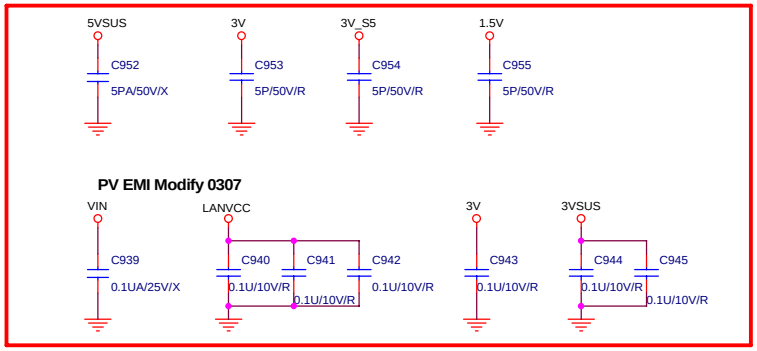
DISCHARGE

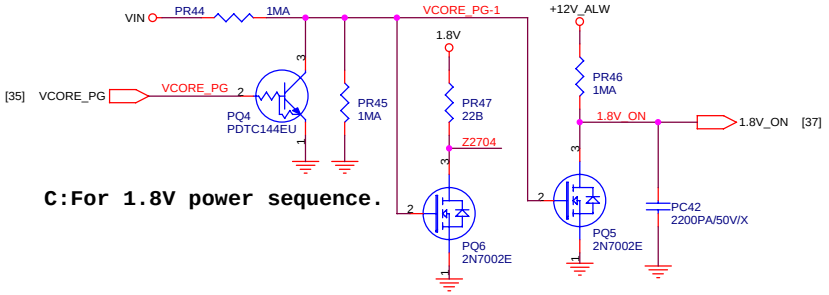




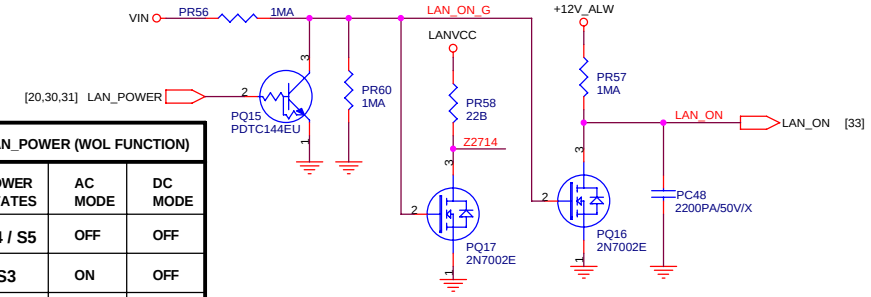


SI POWER MODIFY

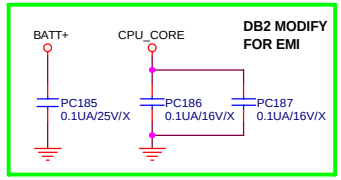




C:For 1.8V power sequence.



LAN_POWER (WOL FUNCTION)		
POWER STATES	AC MODE	DC MODE
S4 / S5	OFF	OFF
S3	ON	OFF
S0	ON	ON



CPU_CORE	[4,38]
1.2V_S5	[10,11,35]
1.5V	[27,28,31,36]
1.8V	[11,13,15,16,17,37]
1.8VSUS	[2,3,4,5,6,36,37]
2.5V	[2,13,36]
LANVCC	[20,33]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,33,36,38]
3VSUS	[27,28,29,33]
3V_S5	[8,9,10,11,20,28,30,33,37]
5V	[13,18,19,22,23,25,26,27,28,29,31,33,36,38]
5VSUS	[18,26,28,30,31,33,37]
+12V_ALW	[10,18,33]
VIN	[18,31,33,34,35,36,37,38]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE	MV

Date: Tuesday, August 21, 2007 Sheet 32 of 40

DC/DC 3VPCU/ 5VPCU/ +12V_ALW

TOPN: OUT1/OUT2
GND=400KHz/500KHz
REF = 400KHz /300KHz
VCC5=200KHz/300KHz

5 Volt +/- 5%

5VPCU
C/C:8A
P/C:10A

Vout=0.7(Ra+Rb)/Rb
Rb around 49.9k

3.3 Volt +/- 5%

3VPCU
C/C:8A
P/C:10A

Place these CAPs close to FETs

Place these CAPs close to FETs

PU6 ISL6236

Rds(on) 13m ohm

Rds(on) 13m ohm

I_lim*MOSFET(RDSON)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM

DB2 MODIFY

DB2 MODIFY

SI01 power

SI power

SI power

SI power

SI power

1A
S0-S5

1.6A
S0-S3

4.59A
S0-S1

5A
S0-S3

LANVCC
0.2A

PV EMI Modify 0307

3V
9.0A
S0-S1

+12V_ALW	[10,18,32]
LANVCC	[20,32]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,36,38]
3VSUS	[27,28,29,32]
3V_S5	[8,9,10,11,20,28,30,32,37]
3VPCU	[9,14,18,28,29,30,31,34,35]
5V	[13,18,19,22,23,25,26,27,28,29,31,32,36,38]
5VSUS	[18,26,28,30,31,32,37]
5VPCU	[10,23,34,35,36,37,38]
VIN	[18,31,32,34,35,36,37,38]

PROJECT : AT1
Quanta Computer Inc.

Size: Custom	Document Number: ISL6236 (5VPCU,3VPCU)	Rev: MV
NB5/RD2/HW1	Date: Tuesday, August 21, 2007	Sheet 33 of 40

Adapter 19V/3.4A/65W 19V/4.75A/90W

Battery 6/8/12cell MAX8724

AT1: UN;AT2:install

From Docking CNN

PQ30:1st-SI4856;2nd-IR7836

360mil

Setting the Vin min to 8V

V=I*0.01*3*R

I_INPUT=V_CLS/4.096*0.075/0.01

CELLS	Cell	
LOW	2	0.4
FLOAT	3	REFIN/2-0.2~REFIN/2+0.2
HIGH	4	REFIN-0.4

90W PRa=15.4KOhm(CS31543F929)19.0V/4.23A=80.5W
65W PRa=30.9KOhm (CS33093F911) 18.5V/2.94A=54.5W

FOR AT2 17"

FOR AT1 15.4"

0 = 4 CELL
1 = 3 CELL

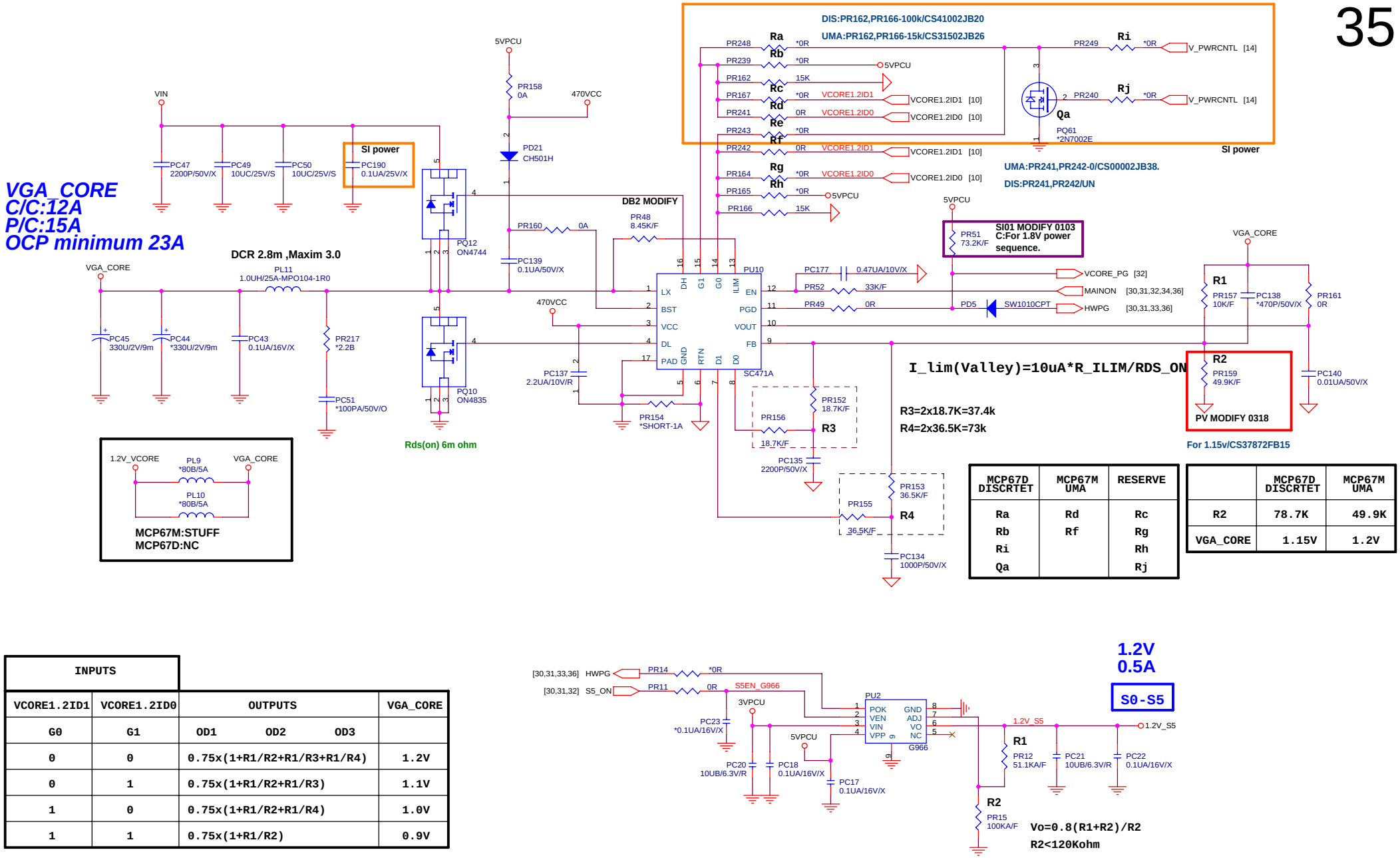
Battery Low 7.5V

PROJECT : AT1
Quanta Computer Inc.

NB5/RD2/HW1

Size	Document Number	Rev
Custom	MAX8724 CHARGER	MV

Date: Tuesday, August 21, 2007 Sheet 34 of 40



MCP67D DISCRTET	MCP67M UMA	RESERVE
Ra	Rd	Rc
Rb	Rf	Rg
Ri		Rh
Qa		Rj

	MCP67D DISCRTET	MCP67M UMA
R2	78.7K	49.9K
VGA_CORE	1.15V	1.2V

INPUTS					
VCORE1.2ID1	VCORE1.2ID0	OUTPUTS			VGA_CORE
G0	G1	OD1	OD2	OD3	
0	0	0.75x(1+R1/R2+R1/R3+R1/R4)			1.2V
0	1	0.75x(1+R1/R2+R1/R3)			1.1V
1	0	0.75x(1+R1/R2+R1/R4)			1.0V
1	1	0.75x(1+R1/R2)			0.9V

1.2V_S5 [10,11,32]
1.2V_VCORE [11,36]
VGA_CORE [12]
3VPCU [9,14,18,28,29,30,31,33,34]
5VPCU [10,23,33,34,36,37,38]
VIN [18,31,32,33,34,36,37,38]

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SC471A (VGA_CORE),1.2V_S5	MV

NB5/RD2/HW1

Date: Tuesday, August 21, 2007 Sheet 35 of 40

MAX1992

S0-S1

1.2V
C/C:6A
P/C:8A
OCP minimum 10A

DCR 14m ,Maxim 15mohm

Vout=0.7V(1+Ra/Rb)

Vcs=I_L(A)*L_DCR(mOHM)=V_ILIM(mV)/10

MODIFY 0825
1.2V_VCORE PL7 80B/5A 1.2V
PL6 80B/5A
MCP67M:NC
MCP67D:STUFF

PC15 0.1UA/25V/X DB2 MODIFY

For EMI.

PJ1 *SHORT-1A

1.5A
S0-S1

SI POWER 5V PR186 10K
[30,31,33,35] HWPG PR189 *0R
EN_G966
PU12 POK VEN VIN VPP GND ADJ VO NC G966
1.8VSUS 5V
R1 PR201 88.7K/F
R2 PR203 100K/F
PC153 *0.1UA/16V/X
PC151 10UB/6.3V/R
PC154 0.1UA/16V/X
PC157 0.1UA/16V/X
PC170 10UB/6.3V/R
PC168 0.1UA/16V/X
1.5V

Vo=0.8(R1+R2)/R2
R2<120Kohm

SI power
PU13 VIN VOUT SHDN GND SET G913C
PC191 1UA/10V/R
PR244 10K
R1 PR245 100K/F
R2 PR246 100K/F
PC192 4.7UB/10V/R
2.5V 0.1A
S0-S1

Vout=1.25(1+R1/R2)

1.2V_VCORE [11,35]
1.2V [10,11,12,13,15]
1.5V [27,28,31,32]
1.8VSUS [2,3,4,5,6,32,37]
2.5V [2,13,32]
3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,38]
5V [13,18,19,22,23,25,26,27,28,29,31,32,33,38]
5VPCU [10,23,33,34,35,37,38]
VIN [18,31,32,33,34,35,37,38]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MAX1992 (1.2V),1.5V,2.5V	MV

Date: Tuesday, August 21, 2007 Sheet 36 of 40

S0-S3

1.8VSUS
C/C:12A
P/C:15.2A
OCP minimum 25A

1.8 Volt +/-5%

DCR 2.8m ,Maxim 3.0

I_lim(Valley)=10uA*R_ILIM/RDS_ON

For OCP set.

S0-S3

SMDDR_VTERM
1.53A / 0.9V

SI MODIFY FOR POWER SEQUENCE 1211

0.9 Volt +/-5%
Design Current:1.5A
Maximum Current: 1.8A

Fix 1.8V Output

Ra=(Vout-0.75)/0.75*Rb

Rb value from 100K to 300K ohm

Rds(on) 4.2m ohm

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

V_TRIP(mV)=R_TRIP(Kohm)*10(uA)

I_OCP=V_trip/Rds_on+I_Ripple/2

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V _vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V

S0-S3

SMDDR_VTERM
0.9V
?A

0.9V/1.2A

1.8V
4.75A

S0-S1

SMDDR_VTERM [4]
1.8V [11,13,15,16,17,32]
1.8VSUS [2,3,4,5,6,32,36]
3V_S5 [8,9,10,11,20,28,30,32,33]
5VSUS [18,26,28,30,31,32,33]
5VPCU [10,23,33,34,35,36,38]
VIN [18,31,32,33,34,35,36,38]

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TI51116 (1.8VSUS,VTER),1.8V	MV

Date: Tuesday, August 21, 2007 Sheet 37 of 40

NB5/RD2/HW1

CPU_CORE MAX8774

Slew rate=(12.5mVus)*(71.5K/R_TIME)
VFB=V_VID+0.125(VREF-VOFS)
VRHOT is low when VTHRM below 1.5V
Tsw=16.26pF(R_TON+6.5K)ohm
CCV CAP=470pF*(2/total phase)*300kHZ/fsw

TON=200K Ohm/ 300K Hz

MV MODIFY 0423

D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V
0	0	0	0	0	1	1.5250V
0	0	0	0	1	0	1.5000V
0	0	0	0	1	1	1.4750V
0	0	0	1	0	0	1.4500V
0	0	0	1	0	1	1.4250V
0	0	0	1	1	0	1.4000V
0	0	0	1	1	1	1.3750V
0	0	1	0	0	0	1.3500V
0	0	1	0	0	1	1.3250V
0	0	1	0	1	0	1.3000V
0	0	1	0	1	1	1.2750V
0	0	1	1	0	0	1.2500V
0	0	1	1	0	1	1.2250V
0	0	1	1	1	0	1.2000V
0	0	1	1	1	1	1.1750V
0	1	0	0	0	0	1.1500V
0	1	0	0	0	1	1.1250V
0	1	0	0	1	0	1.1000V
0	1	0	0	1	1	1.0750V
0	1	0	1	0	0	1.0500V
0	1	0	1	0	1	1.0250V
0	1	0	1	1	0	1.0000V
0	1	0	1	1	1	0.9750V
0	1	1	0	0	0	0.9500V
0	1	1	0	0	1	0.9250V
0	1	1	0	1	0	0.9000V
0	1	1	0	1	1	0.8750V
0	1	1	1	0	0	0.8500V
0	1	1	1	0	1	0.8250V
0	1	1	1	1	0	0.8000V
0	1	1	1	1	1	0.7750V

D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	0.7625V
1	0	0	0	0	1	0.7500V
1	0	0	0	1	0	0.7375V
1	0	0	0	1	1	0.7250V
1	0	0	1	0	0	0.7125V
1	0	0	1	0	1	0.7000V
1	0	0	1	1	0	0.6875V
1	0	0	1	1	1	0.6750V
1	0	1	0	0	0	0.6625V
1	0	1	0	0	1	0.6500V
1	0	1	0	1	0	0.6375V
1	0	1	0	1	1	0.6250V
1	0	1	1	0	0	0.6125V
1	0	1	1	0	1	0.6000V
1	0	1	1	1	0	0.5875V
1	0	1	1	1	1	0.5750V
1	1	0	0	0	0	0.5625V
1	1	0	0	0	1	0.5500V
1	1	0	0	1	0	0.5375V
1	1	0	0	1	1	0.5250V
1	1	0	1	0	0	0.5125V
1	1	0	1	0	1	0.5000V
1	1	0	1	1	0	0.4875V
1	1	0	1	1	1	0.4750V
1	1	1	0	0	0	0.4625V
1	1	1	0	0	1	0.4500V
1	1	1	0	1	0	0.4375V
1	1	1	0	1	1	0.4250V
1	1	1	1	0	0	0.4125V
1	1	1	1	0	1	0.4000V
1	1	1	1	1	0	0.3875V
1	1	1	1	1	1	0.3750V

CPU_CORE
C/C:35A
P/C:35A
OCP minimum 44A

DCR=1.1m/+-5%

DB2 BOM MODIFY 1108

SI MODIFY FOR POWER SEQUENCE 1211

CPU_CORE [4,32]
3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36]
5V [13,18,19,22,23,25,26,27,28,29,31,32,33,36]
5VPCU [10,23,33,34,35,36,37]
VIN [18,31,32,33,34,35,36,37]

PROJECT : AT1
Quanta Computer Inc.

NB5/RD2/HW1

Size	Document Number	Rev
Custom	MAX8774 (CPU_CORE)	MV

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