AT5 BLOCK DIAGRAM

01

04-- 0402 footprint
06-- 0603 footprint
08-- 0805 footprint
12-- 1206 footprint
F-- 1% tolerance

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

CPU Merom
478P (uPGA)/35W
PAG 3,4

CPU THERMAL SENSOR
PAG 5

14.318MHz

CLOCK GEN
ICS9LPRS355AGLFT
64pinsTSSOP
PAG 2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

NORTH BRIDGE
Crestline
PAG 7,8,9,10,11,12

DDRII-SODIMM1 PAG 13,14 — DDRII 533,667 MHz
DDRII-SODIMM2 PAG 13,14 — DDRII 533,667 MHz

PCI-Express 16X
NVDIA G3-64 for 15.4"
NVDIA G3-128 for 17"
820p FCBGA PAG 15,16,17,18,19,20

Option for 17" only
HDMI CON PAG 26

TV_OUT
CRT_OUT
CRT/S-VIDEO PAG 25

LVDS(2 Channel)
Panel Connector 15" / 17" PAG 26

NBSRCCLK, NBSRCCLK#

Cable Docking PAG 38
- TV_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

DMI LINK

SOUTH BRIDGE
ICH-8M
PAG 21,22,23,24

USB2.0
5 — **Bluetooth** PAG 35
0,1,2 — **USB2.0 I/O Ports** X3 PAG 32
3 — **Camera** X1 PAG 32
4,6,7 — **Mini PCI-E Card x1**, **Express Card x1**, **Cable Docking x1**

Option for 17" only
SATA - HDD PAG 35 — *SATA2*
SATA - HDD PAG 32 — *SATA0 150MB*
PATA- CD-ROM PAG 32 — *PATA (66/100/133)*

PCI BUS / 33MHz
PCI-E
Azalia

Realtek ALC 268 PAG 29
Two-element microphone PAG 29
Audio Jacks (Phone/ MIC) PAG 29

Mini PCI-E Card PCI Express Mini Card (Wireless LAN/WAN) PAG 39
LAN Realtek PCIE-LAN RTL8101E/8111B 10/100/GagaLAN PAG 33,34
Express Card (NEW CARD) PAG 35
RICOH RICOH 832 PAG 27,28

SIM CARD PAG 32
RJ45 PAG 33
IEEE1394 CONN PAG 28
Memory CardReader PAG 27

LPC

ENE KBC
KB3920 Bx
KB3926 Bx
PAG 37,48

Keyboard Touch Pad PAG 36
CIR PAG 36
Capacitive Sense SW PAG 36

X-Bus
FAN PAG 38
Flash PAG 37
SPI PAG 37

AUDIO Amplifier PAG 30
Jack to Speaker PAG 30

MDC DAA SI3080 PAG 31
MODEM RJ 11 PAG 33

SYSTEM CHARGER(MAX8724) PAG 41
SYSTEM POWER MAX8778 PAG 42
DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAG 46
VCCP +1.5V AND GMCH 1.05V(MAX8717) PAG 43
VGACORE(1.025V)MAX1992 PAG 45
CPU CORE MAX8771 PAG 44

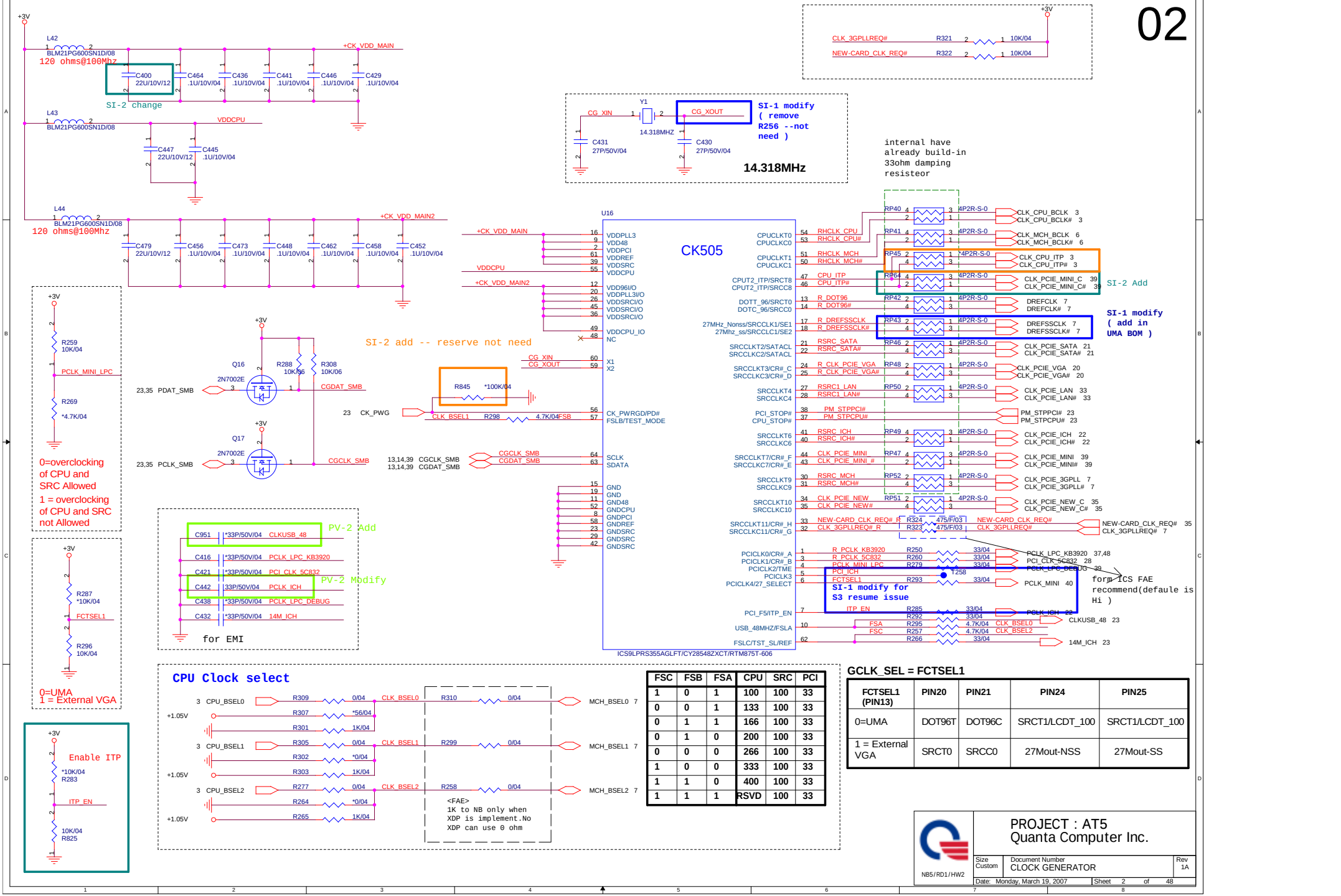
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

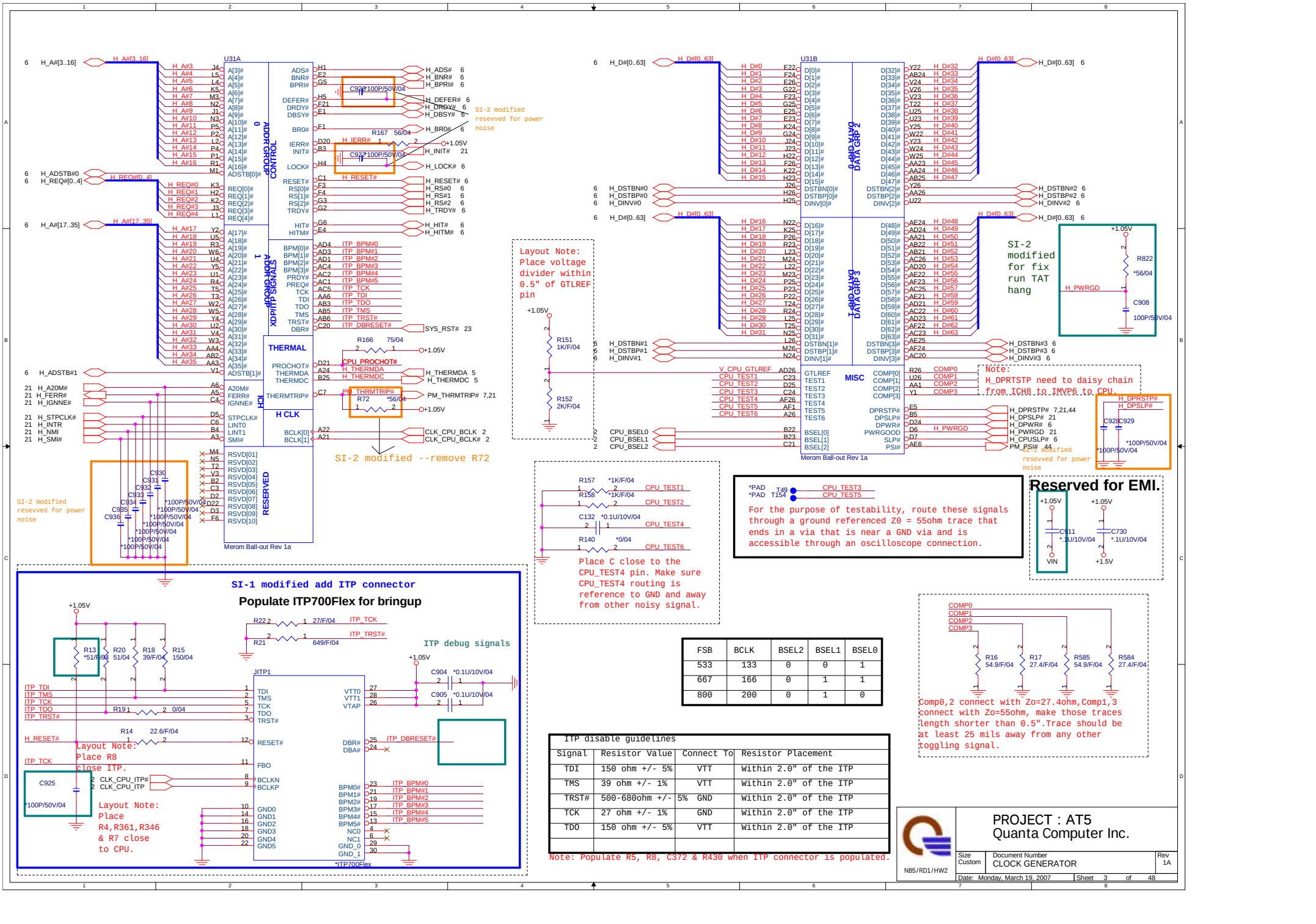
Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Monday, March 19, 2007 | Sheet 1 of 48



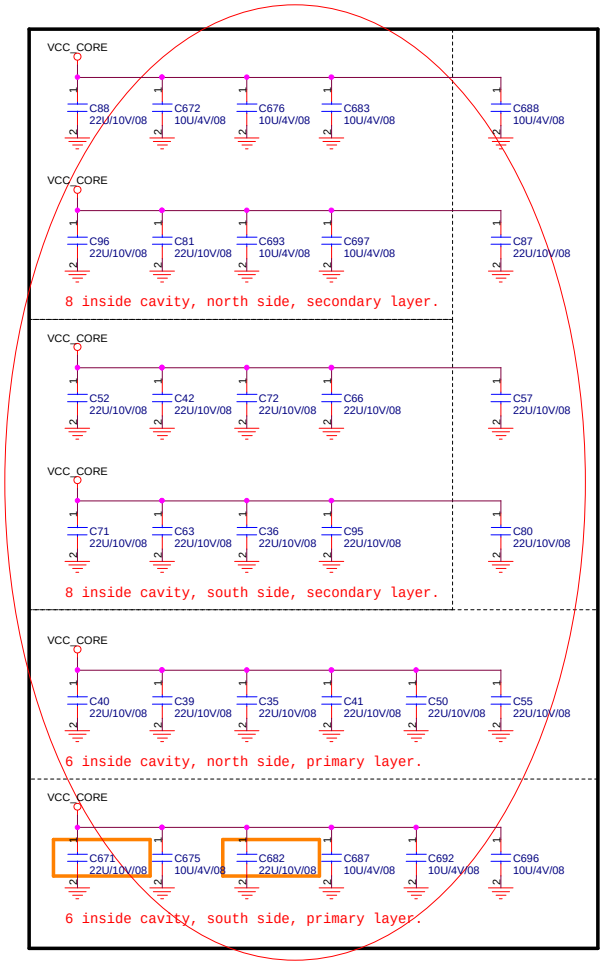
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

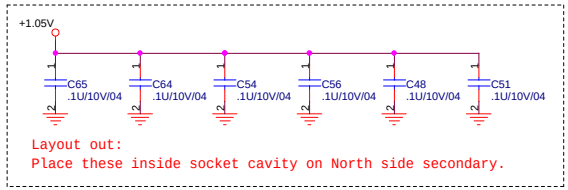
FCTSEL1 (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

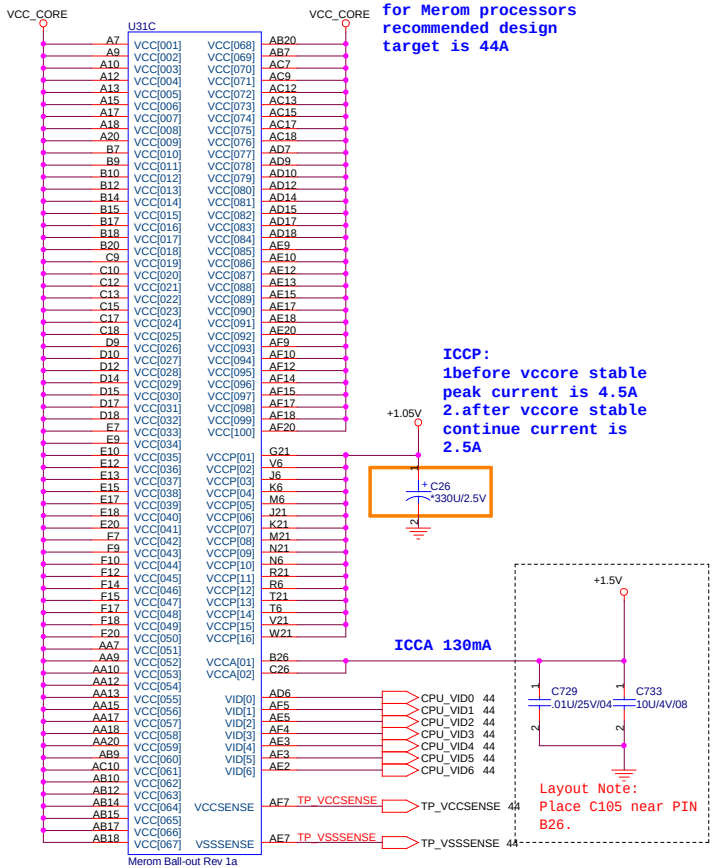


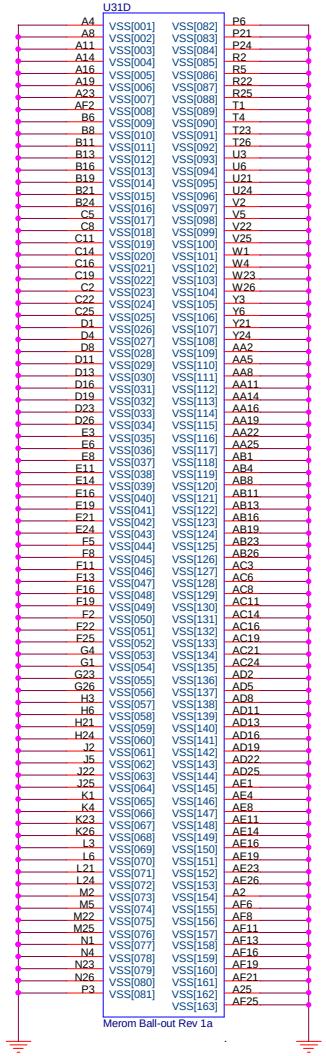
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP







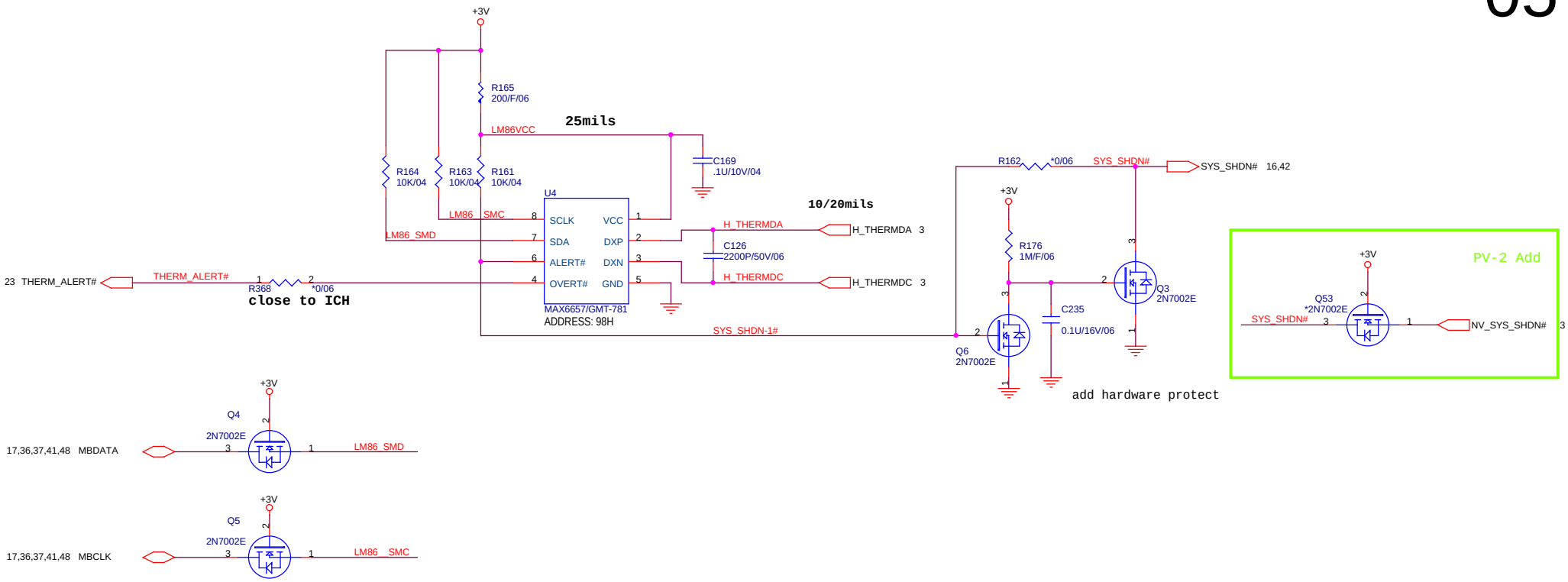


PROJECT : AT5
Quanta Computer Inc.

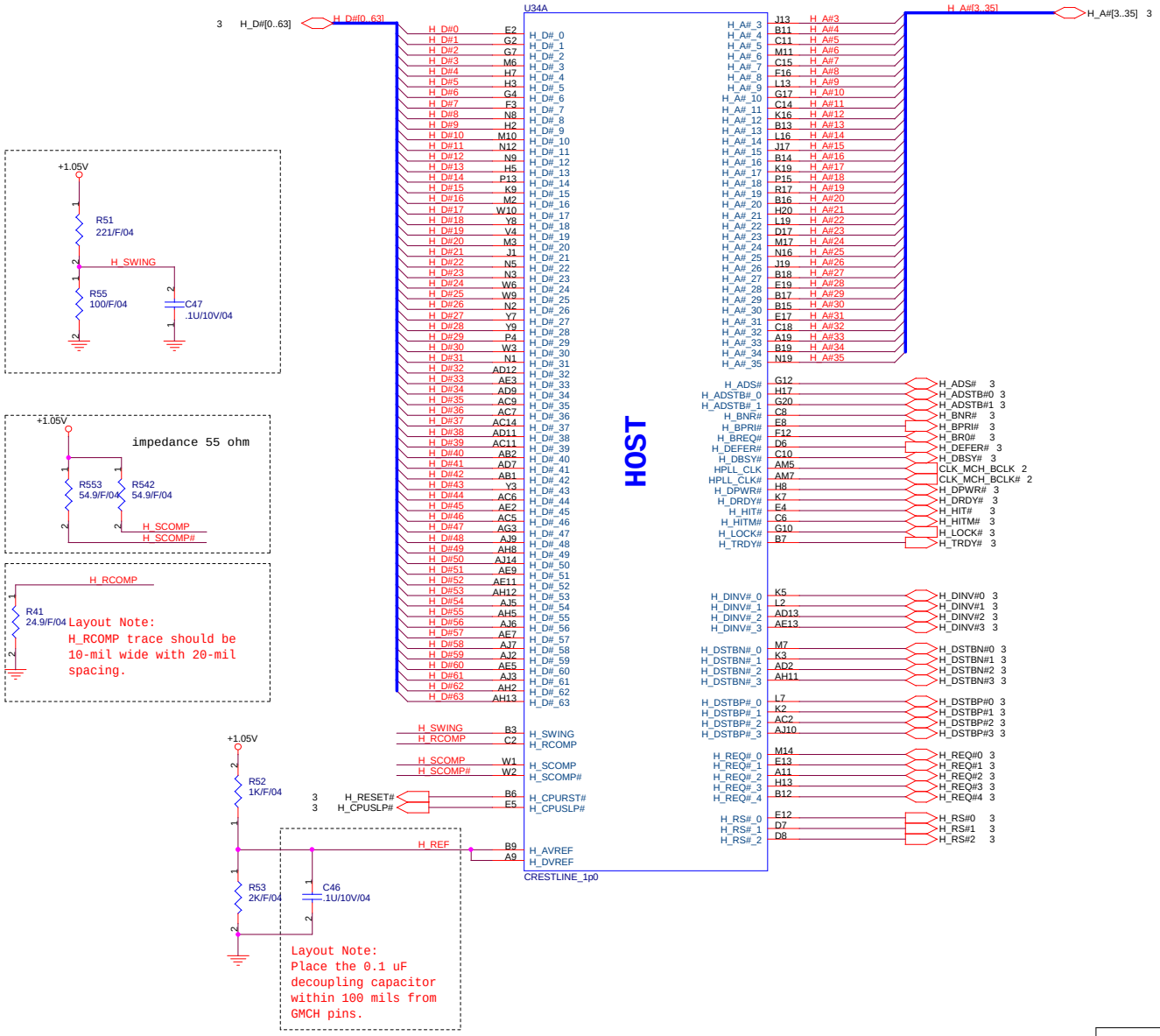
Size	Document Number	Rev
Custom	Merom Processor (POWER)	1A

NB5/RD1/HW2

Date: Monday, March 19, 2007 | Sheet 4 of 48



NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.	
Size B	Document Number THERMAL LM86	Rev 1A
Date: Monday, March 19, 2007	Sheet 5 of 48	



PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (HOST)	1A

NB5/RD1/HW2

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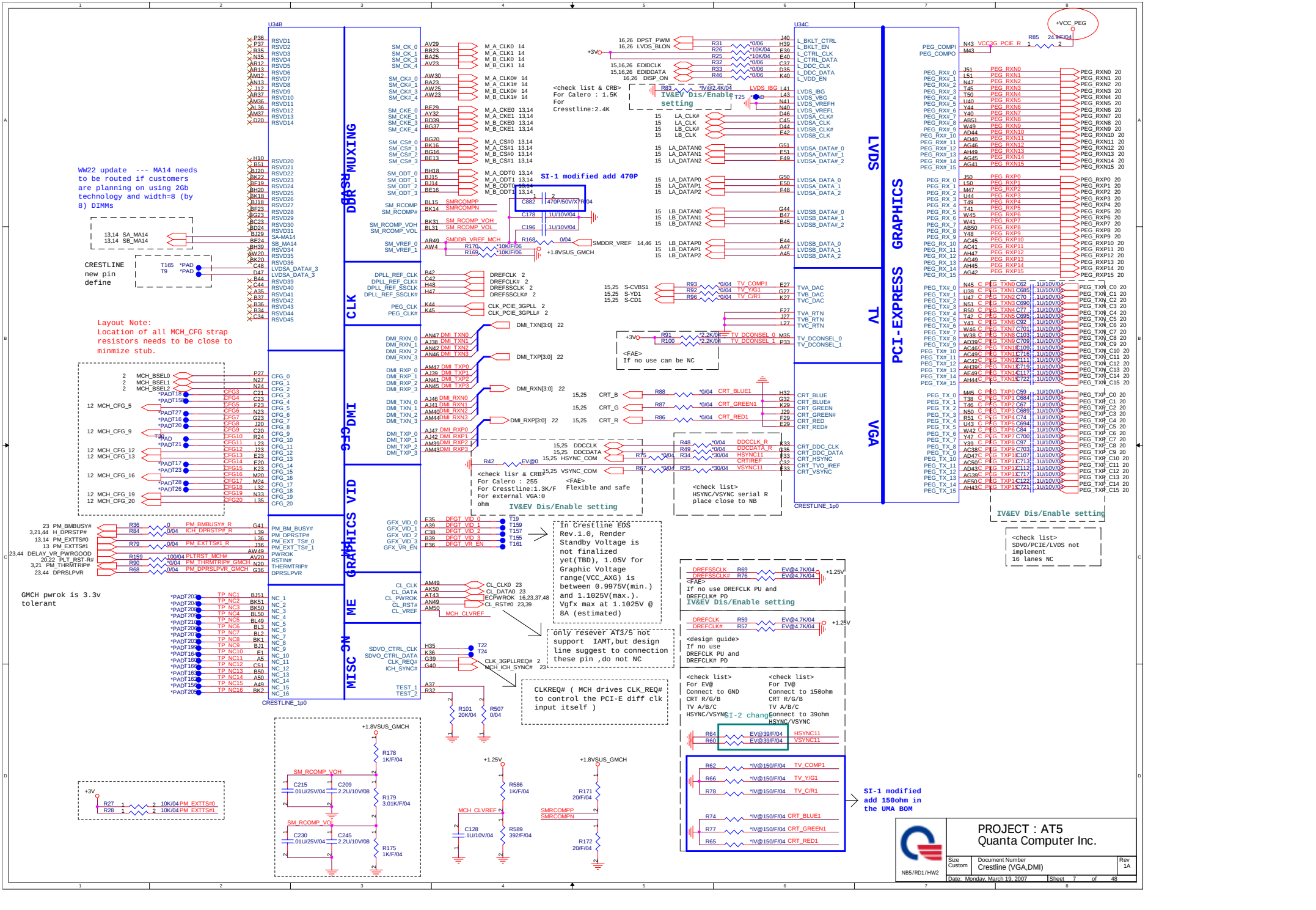
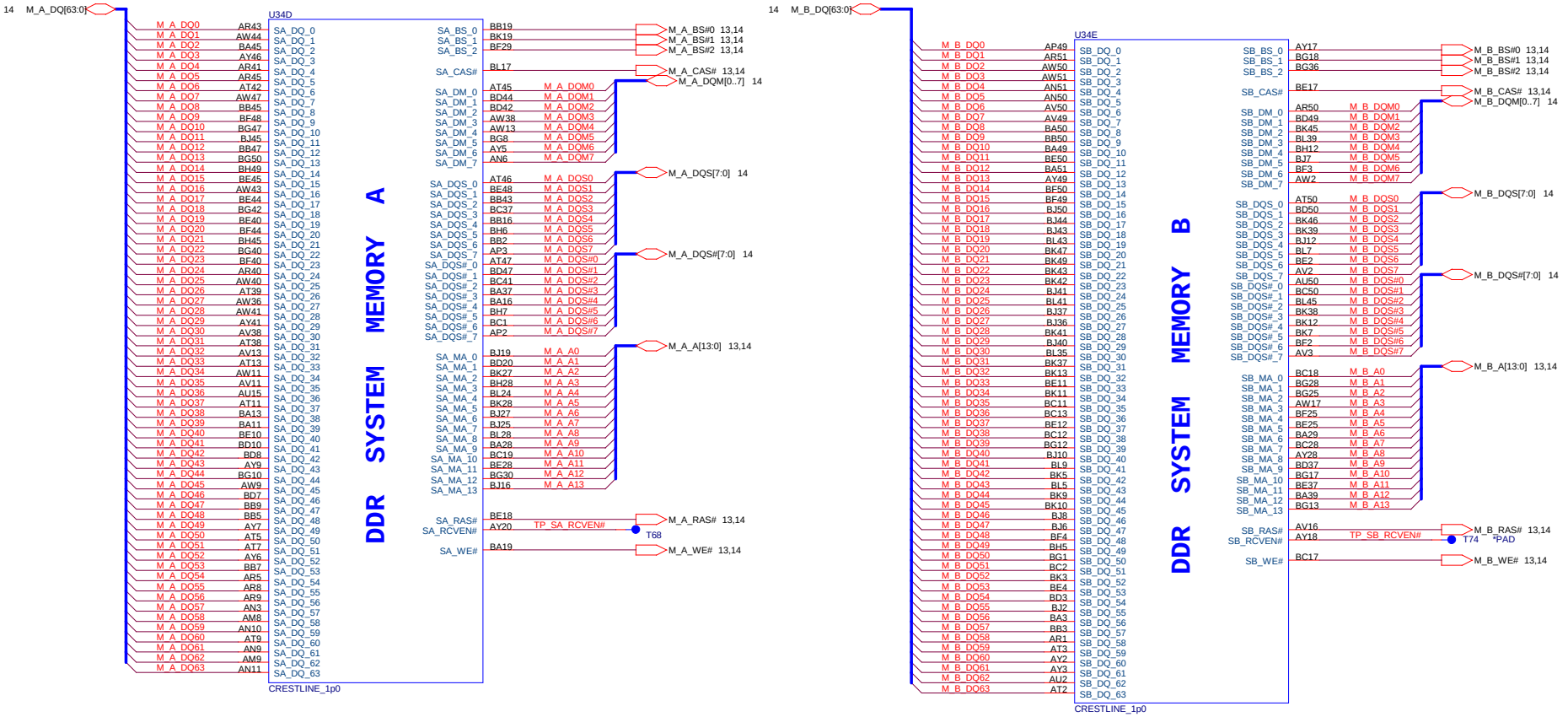

U34B
U34C
DDR MUXING
CLK
DMI
GRAPHICS VID
MISC
NC
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
WW22 update --- MA14 needs to be routed if customers are planning on using 2Gb technology and width=8 (by 8) DIMMs
CRESTLINE new pin define
Layout Note: Location of all MCH_CFG strap resistors needs to be close to minmize stub.
SI-1 modified add 470P
IV&EV Dis/Enable setting
SI-2 change
SI-1 modified add 150ohm in the UMA BOM
CRESTLINE_1p0
PROJECT : AT5
Quanta Computer Inc.
Crestline (VGA,DMI)
NB5/RD1/HW2
Date: Monday, March 19, 2007
Sheet 7 of 48

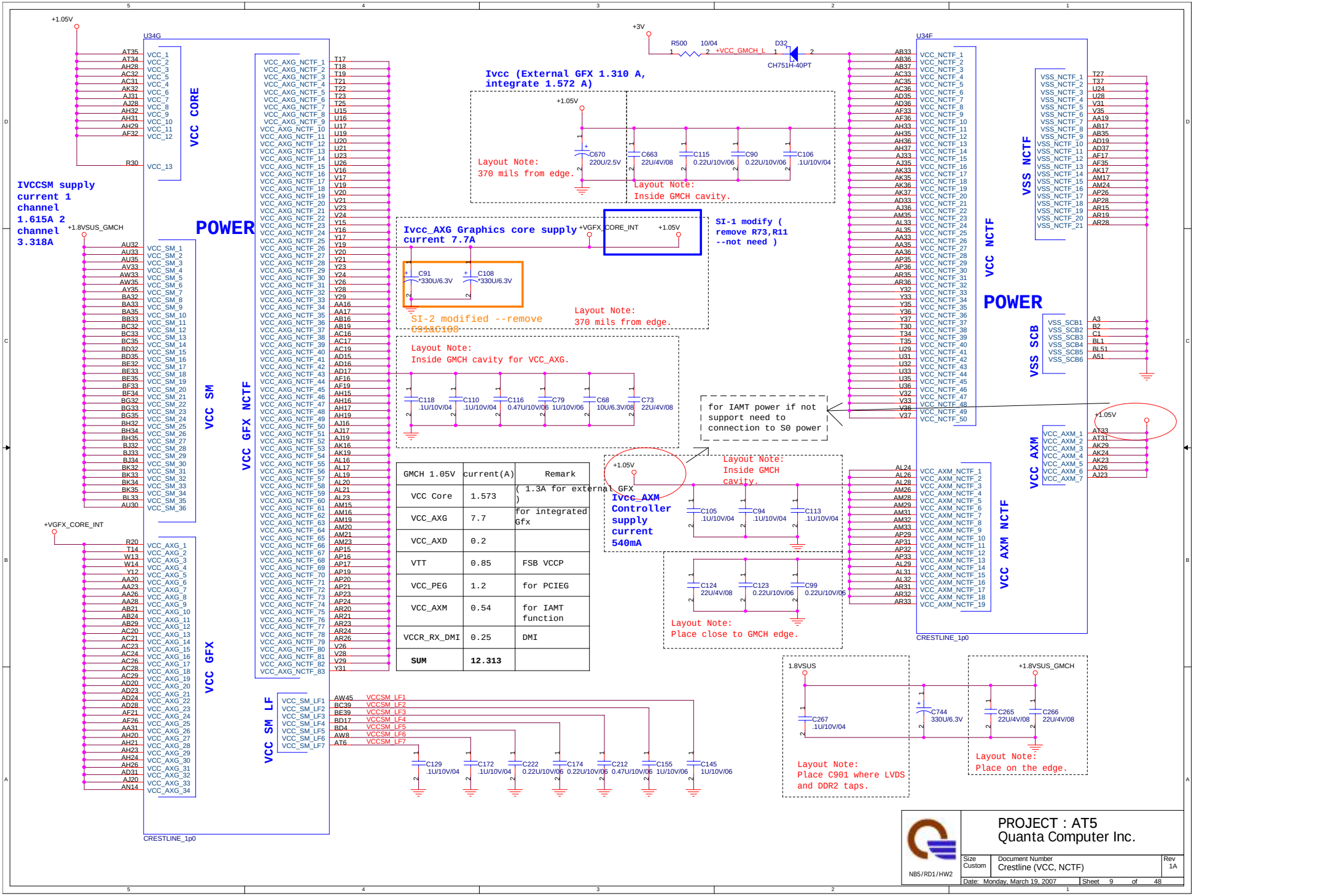


NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (DDR)	1A

Date: Monday, March 19, 2007 Sheet 8 of 48



GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (VCC, NCTF)	1A
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NB5/RD1/HW2

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V

CRT/TV Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TVC_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVDAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TVB_DAC	3.3V	GND	VCCSYNC	3.3V	GND

IV&EV Dis/Enable setting

<FAE>
INT VGA disable
VCCSYNC connect
to GND

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

SI-1 modify
(NET name
wrong)

FB_120ohm+-25%_100mHz
_200mA_0.2ohm DC

10uH+-20%_100mA

0.1Caps should be
placed 200 mils
with in its pins.

IV&EV Dis/Enable setting

Ivcca_PEG_BG
supply current
100mA

Ivcc_VTT FSB
supply
current
0.85A

Place on the edge.

Reserved L81 pad for
inductor.

Place caps close
to VCC_AXD.

Ivcc_DMI supply
current 100mA

Place caps close
to VCC_AXF

+3V_VCC_HV

40 mil
wide

Ivcc_PEG
supply current
1.2A

SI-1 modified change

Ivcc_RX_DMI
supply current
250mA

SI-2
modified
for WW44
request

SI-2 add for UMA to
fix TV-out noise

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

22nF & 0.1uF for
VCC_TVDACA:C_R should
be placed with in 250
mils from Crestline.

IV&EV Dis/Enable setting

FB_220ohm+-25%_100MHz
_2A_0.1ohm DC

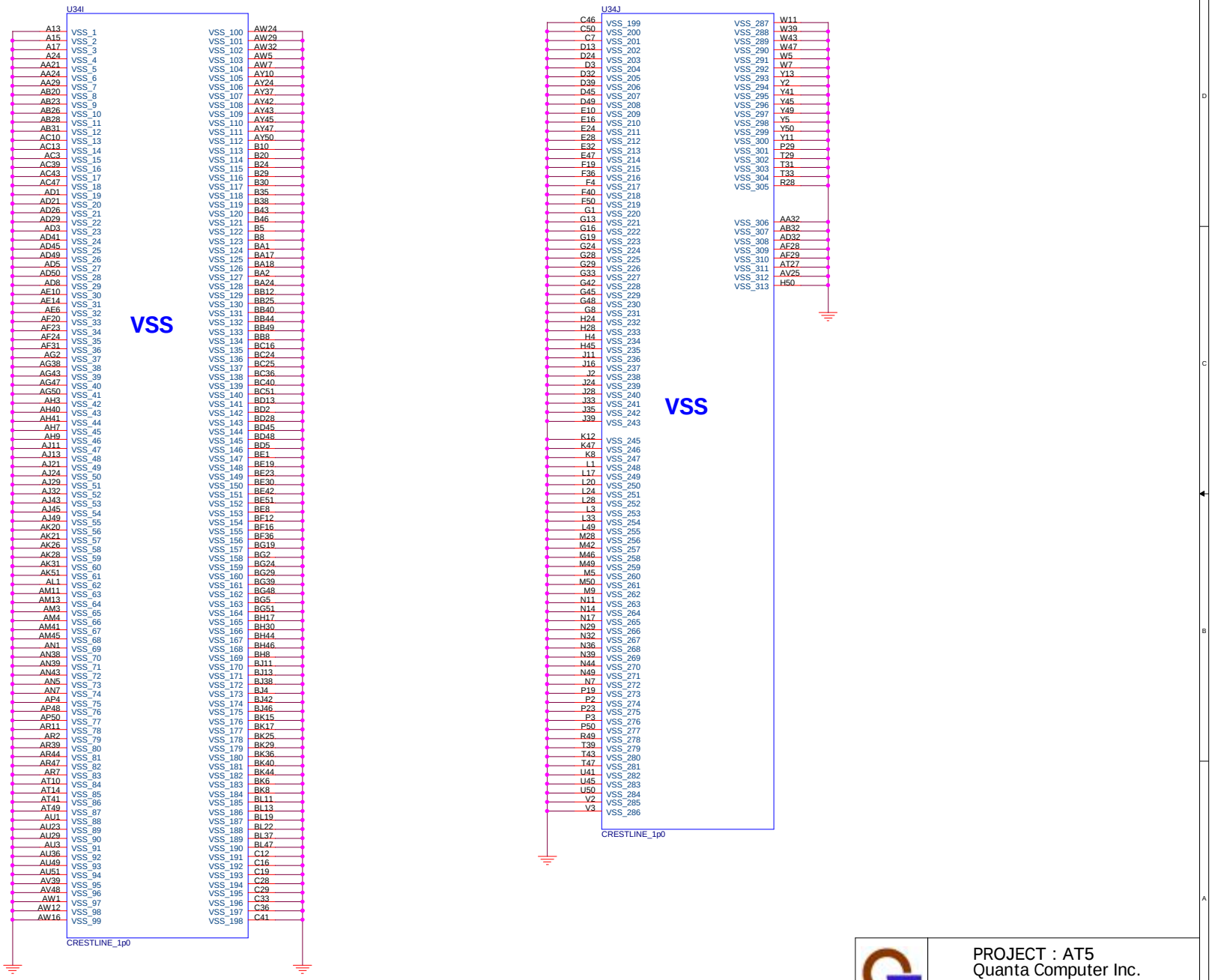
CRESTLINE_1p0

Size: Custom	Document Number: Crestline (POWER)
Date: Monday, March 19, 2007	Sheet 10 of 48

PROJECT : AT5
Quanta Computer Inc.

N85/RD1/HW2

Rev 1A


U34I
A13 A15 A17 A24 AA21 AA24 AA29 AB20 AB23 AB26 AB28 AB31 AC10 AC13 AC3 AC39 AC43 AC47 AD1 AD21 AD26 AD29 AD3 AD41 AD45 AD49 AD5 AD50 AD8 AE10 AE14 AE6 AF20 AF23 AF24 AF31 AG2 AG38 AG43 AG47 AG50 AH3 AH40 AH41 AH7 AH9 AJ11 AJ13 AJ21 AJ24 AJ29 AJ32 AJ43 AJ45 AJ49 AK20 AK21 AK26 AK28 AK31 AK51 AL1 AM11 AM13 AM3 AM4 AM41 AM45 AN1 AN38 AN39 AN43 AN5 AN7 AP4 AP48 AP50 AR11 AR2 AR39 AR44 AR47 AR7 AT10 AT14 AT41 AT49 AU1 AU23 AU29 AU3 AU36 AU49 AU51 AV39 AV48 AW1 AW12 AW16
VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58 VSS_59 VSS_60 VSS_61 VSS_62 VSS_63 VSS_64 VSS_65 VSS_66 VSS_67 VSS_68 VSS_69 VSS_70 VSS_71 VSS_72 VSS_73 VSS_74 VSS_75 VSS_76 VSS_77 VSS_78 VSS_79 VSS_80 VSS_81 VSS_82 VSS_83 VSS_84 VSS_85 VSS_86 VSS_87 VSS_88 VSS_89 VSS_90 VSS_91 VSS_92 VSS_93 VSS_94 VSS_95 VSS_96 VSS_97 VSS_98 VSS_99
VSS_100 VSS_101 VSS_102 VSS_103 VSS_104 VSS_105 VSS_106 VSS_107 VSS_108 VSS_109 VSS_110 VSS_111 VSS_112 VSS_113 VSS_114 VSS_115 VSS_116 VSS_117 VSS_118 VSS_119 VSS_120 VSS_121 VSS_122 VSS_123 VSS_124 VSS_125 VSS_126 VSS_127 VSS_128 VSS_129 VSS_130 VSS_131 VSS_132 VSS_133 VSS_134 VSS_135 VSS_136 VSS_137 VSS_138 VSS_139 VSS_140 VSS_141 VSS_142 VSS_143 VSS_144 VSS_145 VSS_146 VSS_147 VSS_148 VSS_149 VSS_150 VSS_151 VSS_152 VSS_153 VSS_154 VSS_155 VSS_156 VSS_157 VSS_158 VSS_159 VSS_160 VSS_161 VSS_162 VSS_163 VSS_164 VSS_165 VSS_166 VSS_167 VSS_168 VSS_169 VSS_170 VSS_171 VSS_172 VSS_173 VSS_174 VSS_175 VSS_176 VSS_177 VSS_178 VSS_179 VSS_180 VSS_181 VSS_182 VSS_183 VSS_184 VSS_185 VSS_186 VSS_187 VSS_188 VSS_189 VSS_190 VSS_191 VSS_192 VSS_193 VSS_194 VSS_195 VSS_196 VSS_197 VSS_198
AW24 AW29 AW32 AW5 AW7 AY10 AY24 AY37 AY42 AY43 AY45 AY47 AY50 B10 B20 B24 B29 B30 B35 B38 B43 B46 B5 B8 BA1 BA17 BA18 BA2 BA24 BB12 BB25 BB40 BB44 BB49 BB8 BC16 BC24 BC25 BC36 BC40 BC51 BD13 BD2 BD28 BD45 BD48 BD5 BE1 BE19 BE23 BE30 BE42 BE51 BE8 BF12 BF16 BF36 BG19 BG2 BG24 BG29 BG39 BG48 BG5 BG51 BH17 BH30 BH44 BH46 BH8 BJ11 BJ13 BJ38 BJ4 BJ42 BJ46 BK15 BK17 BK25 BK29 BK36 BK40 BK44 BK6 BK8 BL11 BL13 BL19 BL22 BL37 BL47 C12 C16 C19 C28 C29 C33 C36 C41
VSS
CRESTLINE_1p0
U34J
C46 C50 C7 D13 D24 D3 D32 D39 D45 D49 E10 E16 E24 E28 E32 E47 F19 F36 F4 F40 F50 G1 G13 G16 G19 G24 G28 G29 G33 G42 G45 G48 G8 H24 H28 H4 H45 J11 J16 J2 J24 J28 J33 J35 J39
K12 K47 K8 L1 L17 L20 L24 L28 L3 L33 L49 M28 M42 M46 M49 M5 M50 M9 N11 N14 N17 N29 N32 N36 N39 N44 N49 N7 P19 P2 P23 P3 P50 R49 T39 T43 T47 U41 U45 U50 V2 V3
VSS_199 VSS_200 VSS_201 VSS_202 VSS_203 VSS_204 VSS_205 VSS_206 VSS_207 VSS_208 VSS_209 VSS_210 VSS_211 VSS_212 VSS_213 VSS_214 VSS_215 VSS_216 VSS_217 VSS_218 VSS_219 VSS_220 VSS_221 VSS_222 VSS_223 VSS_224 VSS_225 VSS_226 VSS_227 VSS_228 VSS_229 VSS_230 VSS_231 VSS_232 VSS_233 VSS_234 VSS_235 VSS_236 VSS_237 VSS_238 VSS_239 VSS_240 VSS_241 VSS_242 VSS_243
VSS_245 VSS_246 VSS_247 VSS_248 VSS_249 VSS_250 VSS_251 VSS_252 VSS_253 VSS_254 VSS_255 VSS_256 VSS_257 VSS_258 VSS_259 VSS_260 VSS_261 VSS_262 VSS_263 VSS_264 VSS_265 VSS_266 VSS_267 VSS_268 VSS_269 VSS_270 VSS_271 VSS_272 VSS_273 VSS_274 VSS_275 VSS_276 VSS_277 VSS_278 VSS_279 VSS_280 VSS_281 VSS_282 VSS_283 VSS_284 VSS_285 VSS_286
VSS_287 VSS_288 VSS_289 VSS_290 VSS_291 VSS_292 VSS_293 VSS_294 VSS_295 VSS_296 VSS_297 VSS_298 VSS_299 VSS_300 VSS_301 VSS_302 VSS_303 VSS_304 VSS_305
VSS_306 VSS_307 VSS_308 VSS_309 VSS_310 VSS_311 VSS_312 VSS_313
W11 W39 W43 W47 W5 W7 Y13 Y2 Y41 Y45 Y49 Y5 Y50 Y11 P29 T29 T31 T33 R28
AA32 AB32 AD32 AF28 AF29 AT27 AV25 H50
VSS
CRESTLINE_1p0
PROJECT : AT5
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number Crestline (VSS)
Rev 1A
Date: Monday, March 19, 2007
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Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

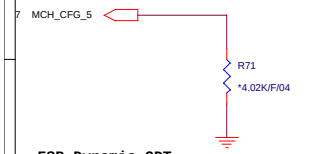
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down

Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

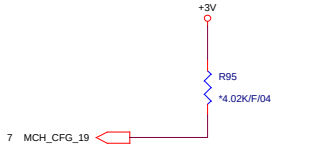
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

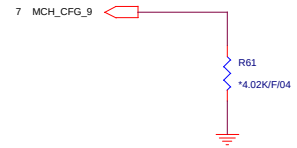


XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

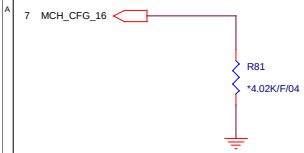


SDVO Present

Strap define at External DVI control page

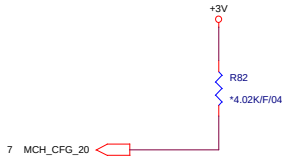
FSB Dynamic ODT

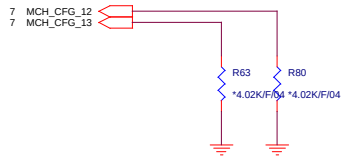
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port





NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- GMCH STRAP-3(6 of 6)	1A

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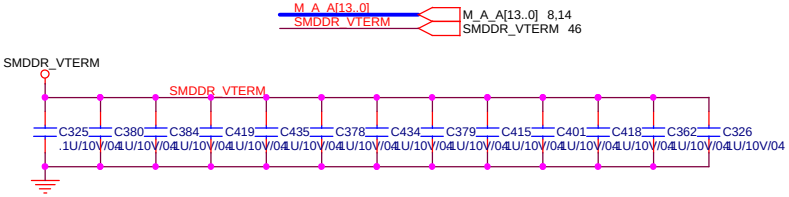
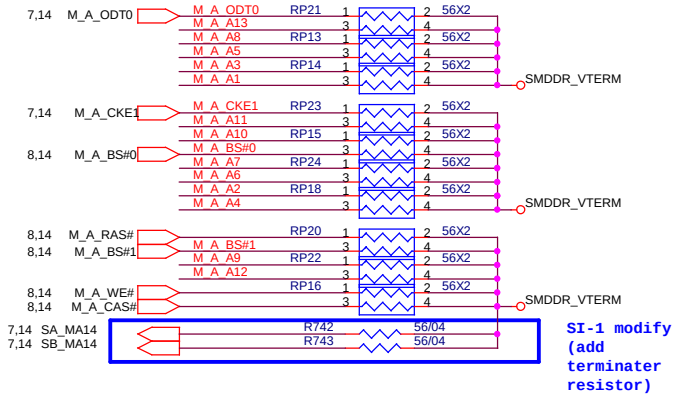
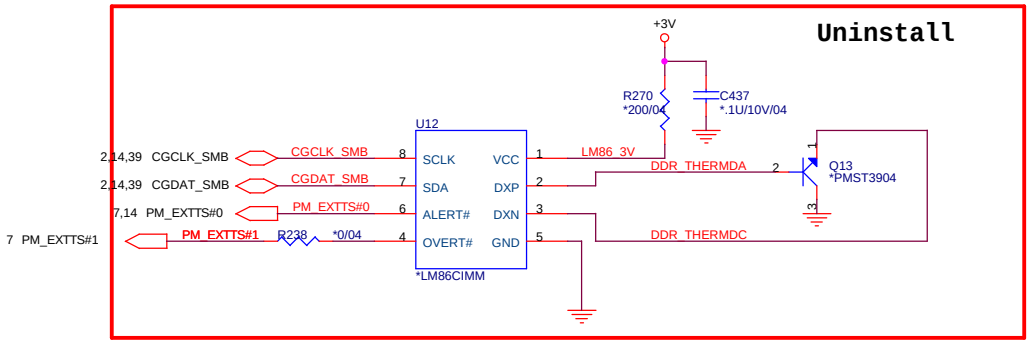
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

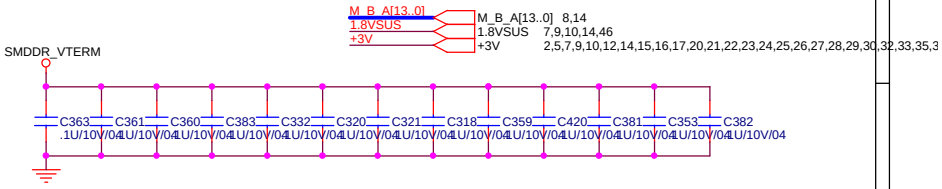




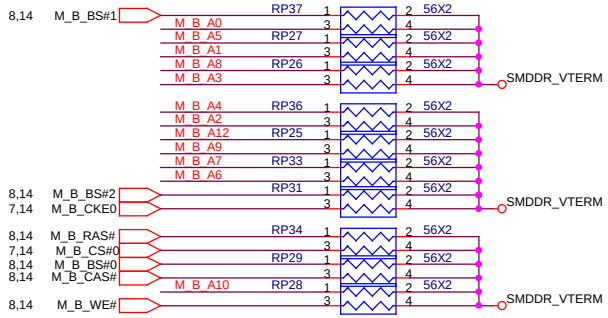
SI-1 modify (add terminater resistor)

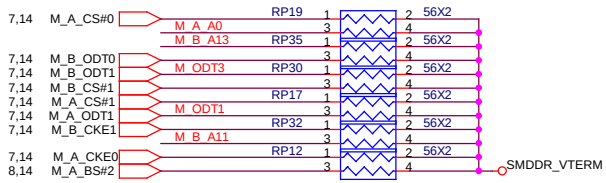


DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM





NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.	
Size B	Document Number DDRII RES.ARRAY	Rev 1A
Date: Monday, March 19, 2007	Sheet 13 of 48	

CGCLK_SMB
CGDAT_SMB
M_A_CKE[0..1]
M_A_CS#[0..1]
M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_CLK0
M_A_CLK0#
M_A_CLK1
M_A_CLK1#
M_A_BS#[0..2]
M_A_ODT[0..1]
M_A_DQM[0..7]
M_A_DQ[0..63]
M_A_DQS[0..7]
M_A_DQS#[0..7]
M_A_A[13..0]
+3V
1.8VSUS
M_B_CKE[0..1]
M_B_CS#[0..1]
M_B_RAS#
M_B_CAS#
M_B_WE#
M_B_CLK0
M_B_CLK0#
M_B_CLK1
M_B_CLK1#
M_B_BS#[0..2]
M_B_ODT[0..1]
M_B_DQM[0..7]
M_B_DQ[0..63]
M_B_DQS[0..7]
M_B_DQS#[0..7]
M_B_A[13..0]

CKEA 0,1

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-M2S-TR
CN26A

CKEB 0,1

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-MAS-TR
CN24A

SMbus address A4

SMbus address A0

SI-1 CHANGE

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-M2S-TR
CN26B

SI-1 CHANGE

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-MAS-TR
CN24B

C771 470P/50V/04
SMDDR_VREF_DIMM
R226 0/06
SMDDR_VREF 7,46
R227
1.8VSUS
R603 *10K/F/06
*10K/F/06

Place these Caps near So-Dimm1.

1.8VSUS
C773 2.2U/6.3V/06
C775 2.2U/6.3V/06
C785 2.2U/6.3V/06
C444 2.2U/6.3V/06
C764 2.2U/6.3V/06
C770 .1U/10V/04
C788 .1U/10V/04
C439 .1U/10V/04
C433 .1U/10V/04
C769 .1U/10V/04
C767 .1U/10V/04
SMDDR_VREF_DIMM
C772 .1U/10V/04
C768 2.2U/6.3V/06
+3V
C317 2.2U/6.3V/06
C316 .1U/10V/04

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.

Place these Caps near So-Dimm2.

1.8VSUS
C774 2.2U/6.3V/06
C786 2.2U/6.3V/06
C784 2.2U/6.3V/06
C759 2.2U/6.3V/06
C760 .1U/10V/04
C776 .1U/10V/04
C789 .1U/10V/04
C787 .1U/10V/04
C443 .1U/10V/04
C765 .1U/10V/04
C766 .1U/10V/04
SMDDR_VREF_DIMM
C371 .1U/10V/04
C373 2.2U/6.3V/06
+3V
C372 2.2U/6.3V/06
C385 .1U/10V/04

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm2

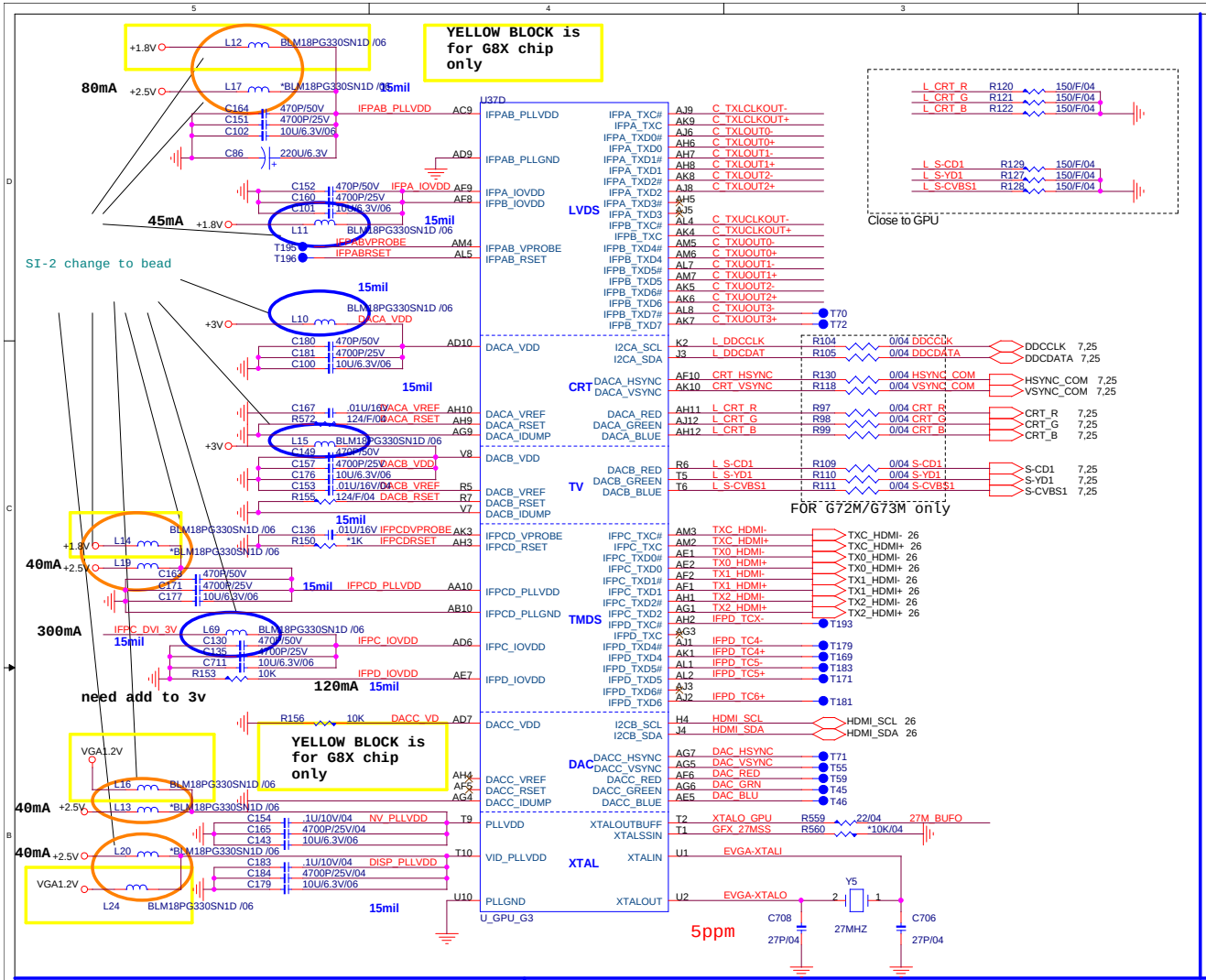
No Vias Between the Trace of PIN to CAP.

NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRII SO-DIMM(200P)	1A

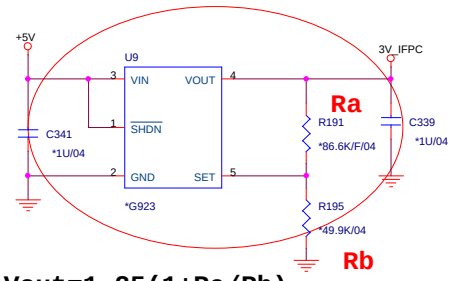
Date: Monday, March 19, 2007 Sheet 14 of 48



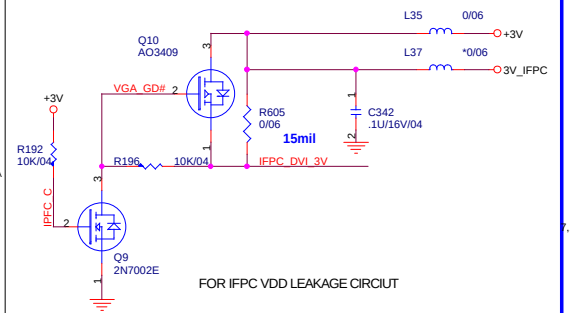
OPTION SIGNAL FROM NB FOR UMA VGA

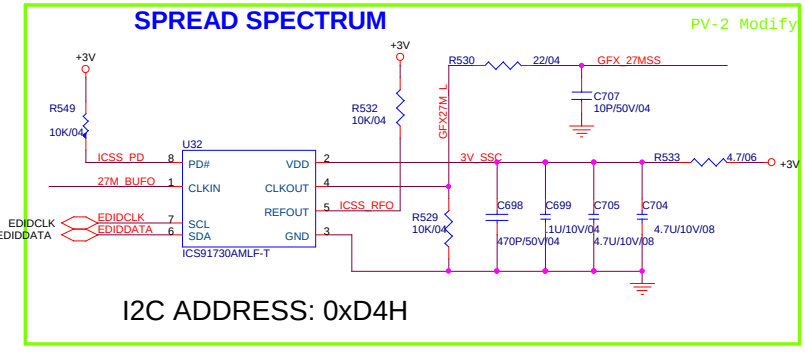
OPTION SIGNAL FROM Nvidia to VGA

C34: PUN issue reserve
U54,C950,c949,R726,R727



Vout=1.25(1+Ra/Rb)





PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NVG73M (LVDS/DVI/CRT/TV)	1A
Date: Monday, March 19, 2007	Sheet 15 of 48	

NB5/RD1/HW2

15mil

U37E

MIOAD

MIOBD

THERMAL GPIO

ROM

U_GPU_G3

GREEN BLOCK can remove if use G8X

MIOBD7 pull down and MIOB_DE pull up from nvidia HANK recommend

SI-2 MODIFIED

YELLOW BLOCK is for G8X chip only

GREEN BLOCK can remove if use G8X

VGACORECTL	NB8P	NB8M
HI	1.15V	1.15V
LO	1.2V	1.15V

GFX_VID0
H : Low Voltage
L : Normal Voltage

ROM_TYPE(0:1) resister can be remove due to from nvidia HANK recommend

need to reserve or cancel

for HDMI function

PCI DEVICE

PCI_DEVICE[3:0]	DESCRIPTION
1000	G72M/G73M
0110	G72M-Z
0111	G72M-V/G73M-V
others	Reserved

PCI_DEVICE[3:0] Default are "0",can remove pull down resister from nvidia HANK recommend

SHARE M/B SYSTEM BIOS, SUB VENDOR ID NEED PULL DOWN .

SI-2 ADD for Nvidia requests

SI-1 MOVE DISP_ON

SI-1 MOVE LVDS_BLON

GPIO1 PULL DOWN strap can be remove from nvidia HANK recommend

G72M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infineon
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

G73M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infineon
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infineon
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix

GPIO12	G8X
HI	AC MODE
LO	BAT MODE

PV-2 MODIFIED

FOR BATTERY MODE throttling FUNCTION

VGA THERMAIL CIRCUIT

Default are "0",can remove pull down resister from nvidia HANK recommend

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NVG73M (ROM/GPIO/STRAP)	1A

NB5/RD1/HW2

Date: Monday, March 19, 2007 Sheet 16 of 48

Channel C is available on G73M only

U37B

VMA_DQ0 N27
VMA_DQ1 M27
VMA_DQ2 N28
VMA_DQ3 L29
VMA_DQ4 K27
VMA_DQ5 K28
VMA_DQ6 J29
VMA_DQ7 J28
VMA_DQ8 P30
VMA_DQ9 N31
VMA_DQ10 N30
VMA_DQ11 N32
VMA_DQ12 L31
VMA_DQ13 L30
VMA_DQ14 J30
VMA_DQ15 L32
VMA_DQ16 H30
VMA_DQ17 K30
VMA_DQ18 H31
VMA_DQ19 F30
VMA_DQ20 H32
VMA_DQ21 E31
VMA_DQ22 D30
VMA_DQ23 E30
VMA_DQ24 H28
VMA_DQ25 H29
VMA_DQ26 E29
VMA_DQ27 J27
VMA_DQ28 F27
VMA_DQ29 E27
VMA_DQ30 E28
VMA_DQ31 E28
VMA_DQ32 AD29
VMA_DQ33 AE29
VMA_DQ34 AD28
VMA_DQ35 AC28
VMA_DQ36 AB29
VMA_DQ37 AA30
VMA_DQ38 Y28
VMA_DQ39 AB30
VMA_DQ40 AM30
VMA_DQ41 AE30
VMA_DQ42 AJ31
VMA_DQ43 AJ30
VMA_DQ44 AJ32
VMA_DQ45 AK29
VMA_DQ46 AM31
VMA_DQ47 AL30
VMA_DQ48 AE32
VMA_DQ49 AE30
VMA_DQ50 AE31
VMA_DQ51 AD30
VMA_DQ52 AC31
VMA_DQ53 AC32
VMA_DQ54 AB32
VMA_DQ55 AB31
VMA_DQ56 AG27
VMA_DQ57 AF28
VMA_DQ58 AH28
VMA_DQ59 AG28
VMA_DQ60 AG29
VMA_DQ61 AD27
VMA_DQ62 AE27
VMA_DQ63 AE28

FBAD0 FBAD1 FBAD2 FBAD3 FBAD4 FBAD5 FBAD6 FBAD7 FBAD8 FBAD9 FBAD10 FBAD11 FBAD12 FBAD13 FBAD14 FBAD15 FBAD16 FBAD17 FBAD18 FBAD19 FBAD20 FBAD21 FBAD22 FBAD23 FBAD24 FBAD25 FBAD26 FBAD27 FBAD28 FBAD29 FBAD30 FBAD31 FBAD32 FBAD33 FBAD34 FBAD35 FBAD36 FBAD37 FBAD38 FBAD39 FBAD40 FBAD41 FBAD42 FBAD43 FBAD44 FBAD45 FBAD46 FBAD47 FBAD48 FBAD49 FBAD50 FBAD51 FBAD52 FBAD53 FBAD54 FBAD55 FBAD56 FBAD57 FBAD58 FBAD59 FBAD60 FBAD61 FBAD62 FBAD63

FBA

VMA_DM0 M29
VMA_DM1 M30
VMA_DM2 G30
VMA_DM3 F29
VMA_DM4 AA29
VMA_DM5 AK30
VMA_DM6 AC30
VMA_DM7 AG30

FBADQM0 FBADQM1 FBADQM2 FBADQM3 FBADQM4 FBADQM5 FBADQM6 FBADQM7

VMA_WDQS0 L28
VMA_WDQS1 K31
VMA_WDQS2 G32
VMA_WDQS3 G28
VMA_WDQS4 AB28
VMA_WDQS5 AL32
VMA_WDQS6 AF32
VMA_WDQS7 AH30

FBADQS_WP0 FBADQS_WP1 FBADQS_WP2 FBADQS_WP3 FBADQS_WP4 FBADQS_WP5 FBADQS_WP6 FBADQS_WP7

VMA_RDQS0 M28
VMA_RDQS1 K32
VMA_RDQS2 G31
VMA_RDQS3 G27
VMA_RDQS4 AA28
VMA_RDQS5 AL31
VMA_RDQS6 AE31
VMA_RDQS7 AH29

FBADQS_RN0 FBADQS_RN1 FBADQS_RN2 FBADQS_RN3 FBADQS_RN4 FBADQS_RN5 FBADQS_RN6 FBADQS_RN7

15mil
+1.8V R604 *1K/04 FB_VREF1 E32
R602 *1K/04
C762 *.1U/10V/04
*U_GPU_G3

G72: Stuff these parts
G73M : NC

VREF = FBVDDQ *
Rbot/(Rtop + Rbot)

FBVDD_0 A12
FBVDD_1 A15
FBVDD_2 A18
FBVDD_3 A21
FBVDD_4 A24
FBVDD_5 A27
FBVDD_6 A3
FBVDD_7 A30
FBVDD_8 A6
FBVDD_9 A9
FBVDD_10 AA32
FBVDD_11 AD32
FBVDD_12 AG32
FBVDD_13 AK32
FBVDD_14 C32
FBVDD_15 F32
FBVDD_16 J32
FBVDD_17 M32
FBVDD_18 R32
FBVDD_19 V32

C309 .1U/10V/04
C306 .1U/10V/04
C104 .1U/10V/04
C144 .1U/10V/04
C283 .47U/10V/06
C291 .47U/10V/06
C175 10U/4V/06
C191 .1U/10V/04
C307 .1U/10V/04
C301 .1U/10V
C197 .1U/10V/04
C216 .47U/10V/06
C268 .47U/10V/06
C289 10U/4V/06
+1.8V
PLACE NEAR GPU

FBVDDQ_0 AA25
FBVDDQ_1 AA26
FBVDDQ_2 AB25
FBVDDQ_3 AB26
FBVDDQ_4 G11
FBVDDQ_5 G12
FBVDDQ_6 G15
FBVDDQ_7 G18
FBVDDQ_8 G21
FBVDDQ_9 G22
FBVDDQ_10 H11
FBVDDQ_11 H12
FBVDDQ_12 H15
FBVDDQ_13 H18
FBVDDQ_14 H21
FBVDDQ_15 H22
FBVDDQ_16 L25
FBVDDQ_17 L26
FBVDDQ_18 M25
FBVDDQ_19 M26
FBVDDQ_20 R25
FBVDDQ_21 R26
FBVDDQ_22 V25
FBVDDQ_23 V26

C763 .1U/10V/04
C314 .1U/10V/04
C274 .1U/10V/04
C310 .1U/10V/04
C285 .47U/10V/06
C279 .47U/10V/06
C282 10U/4V/06
C297 .1U/10V/04
C300 .1U/10V/04
C308 .1U/10V/04
C312 .1U/10V/04
C204 .47U/10V/06
C290 .47U/10V/06
C305 10U/4V/06
+1.8V
PLACE NEAR GPU

C783 +/ 220U

FBA_CMD0 P32
FBA_CMD1 U27
FBA_CMD2 P31
FBA_CMD3 U30
FBA_CMD4 Y31
FBA_CMD5 W32
FBA_CMD6 W31
FBA_CMD7 T32
FBA_CMD8 V27
FBA_CMD9 T28
FBA_CMD10 T31
FBA_CMD11 U32
FBA_CMD12 W29
FBA_CMD13 W30
FBA_CMD14 T27
FBA_CMD15 V28
FBA_CMD16 V30
FBA_CMD17 U31
FBA_CMD18 R27
FBA_CMD19 V29
FBA_CMD20 T30
FBA_CMD21 W28
FBA_CMD22 R29
FBA_CMD23 R30
FBA_CMD24 P29
FBA_CMD25 U28
FBA_CMD26 Y32

VMA_MA3 VMA_MA0 VMA_MA2 VMA_MA1 VMA_MA3H VMA_MA4H VMA_MA5H VMA_BA2 T219
VMA_CS0# VMA_WE# VMA_BA0 VMA_CKE VMA_ODT VMA_MA2H VMA_MA12 VMA_RAS# VMA_MA11 VMA_MA10 VMA_BA1 VMA_MA8 VMA_MA9 VMA_MA6 VMA_MA5 VMA_MA7 VMA_MA4 VMA_CAS# VMA_MA13 T215

VMA_MA3 18 VMA_MA0 18 VMA_MA2 18 VMA_MA1 18 VMA_MA3H 18 VMA_MA4H 18 VMA_MA5H 18
VMA_CS0# 18 VMA_WE# 18 VMA_BA0 18 VMA_CKE 18
VMA_MA2H 18 VMA_MA12 18 VMA_RAS# 18 VMA_MA11 18 VMA_MA10 18 VMA_BA1 18 VMA_MA8 18 VMA_MA9 18 VMA_MA6 18 VMA_MA5 18 VMA_MA7 18 VMA_MA4 18 VMA_CAS# 18 VMA_MA13 18

FBA_CLK0 P28
FBA_CLK0# R28
FBA_CLK1 Y27
FBA_CLK1# AA27

VMA_CLK0 VMA_CLK0# VMA_CLK1 VMA_CLK1#

VMA_CLK0 18 VMA_CLK0# 18 VMA_CLK1 18 VMA_CLK1# 18

RFU2 Y30 FBA_CMD27 T218
RFU3 AC26 G73_AC26 T86
FBA_DEBUG AC27 VMA_DEBUG T87
FBA_REFCLK D32 VMA_REFCK T217
FBA_REFCLK# D31 VMA_REFCK# T216

GREEN BLOCK can remove if use G8X

C313 4.7U/10V/06
C261 .1U/10V
H_PLLVDD
L27 BLM18PG221SN1D/06
VGA1.2V

FBA_PLLVDD G23
FBA_PLLAVDD G25 15mil FBA_PLLAVDD
L33 BLM18PG330SN1D/06 VGA1.2V
FBA_PLLGND G24
C328 4.7U/10V/06
C286 .1U/10V
C315 470P/50V/04
C322 4700P/25V/04
For EMI

YELLOW BLOCK is for G8X chip only

U37C

VMC_DQ0 B7
VMC_DQ1 A7
VMC_DQ2 C7
VMC_DQ3 A2
VMC_DQ4 B2
VMC_DQ5 C4
VMC_DQ6 A5
VMC_DQ7 B5
VMC_DQ8 F9
VMC_DQ9 E10
VMC_DQ10 D12
VMC_DQ11 D9
VMC_DQ12 E12
VMC_DQ13 D11
VMC_DQ14 E8
VMC_DQ15 D8
VMC_DQ16 E7
VMC_DQ17 F7
VMC_DQ18 D6
VMC_DQ19 D5
VMC_DQ20 D3
VMC_DQ21 E4
VMC_DQ22 C3
VMC_DQ23 B4
VMC_DQ24 C10
VMC_DQ25 B10
VMC_DQ26 C8
VMC_DQ27 A10
VMC_DQ28 C11
VMC_DQ29 C12
VMC_DQ30 A11
VMC_DQ31 B11
VMC_DQ32 B28
VMC_DQ33 C27
VMC_DQ34 C26
VMC_DQ35 B26
VMC_DQ36 C30
VMC_DQ37 B31
VMC_DQ38 C29
VMC_DQ39 A31
VMC_DQ40 D28
VMC_DQ41 D27
VMC_DQ42 F26
VMC_DQ43 D24
VMC_DQ44 E23
VMC_DQ45 E26
VMC_DQ46 E24
VMC_DQ47 F23
VMC_DQ48 B23
VMC_DQ49 A23
VMC_DQ50 C25
VMC_DQ51 C23
VMC_DQ52 A22
VMC_DQ53 C22
VMC_DQ54 C21
VMC_DQ55 B22
VMC_DQ56 E22
VMC_DQ57 D22
VMC_DQ58 D21
VMC_DQ59 E21
VMC_DQ60 E18
VMC_DQ61 D19
VMC_DQ62 D18
VMC_DQ63 E19

FBCD0 FBCD1 FBCD2 FBCD3 FBCD4 FBCD5 FBCD6 FBCD7 FBCD8 FBCD9 FBCD10 FBCD11 FBCD12 FBCD13 FBCD14 FBCD15 FBCD16 FBCD17 FBCD18 FBCD19 FBCD20 FBCD21 FBCD22 FBCD23 FBCD24 FBCD25 FBCD26 FBCD27 FBCD28 FBCD29 FBCD30 FBCD31 FBCD32 FBCD33 FBCD34 FBCD35 FBCD36 FBCD37 FBCD38 FBCD39 FBCD40 FBCD41 FBCD42 FBCD43 FBCD44 FBCD45 FBCD46 FBCD47 FBCD48 FBCD49 FBCD50 FBCD51 FBCD52 FBCD53 FBCD54 FBCD55 FBCD56 FBCD57 FBCD58 FBCD59 FBCD60 FBCD61 FBCD62 FBCD63

FBC

VMC_DM0 A4
VMC_DM1 E11
VMC_DM2 E5
VMC_DM3 C9
VMC_DM4 C28
VMC_DM5 F24
VMC_DM6 C24
VMC_DM7 E20

FBCDQM0 FBCDQM1 FBCDQM2 FBCDQM3 FBCDQM4 FBCDQM5 FBCDQM6 FBCDQM7

VMC_WDQS0 C5
VMC_WDQS1 E10
VMC_WDQS2 E5
VMC_WDQS3 B8
VMC_WDQS4 A29
VMC_WDQS5 D25
VMC_WDQS6 B25
VMC_WDQS7 F20

FBCDQS_WP0 FBCDQS_WP1 FBCDQS_WP2 FBCDQS_WP3 FBCDQS_WP4 FBCDQS_WP5 FBCDQS_WP6 FBCDQS_WP7

VMC_RDQS0 C6
VMC_RDQS1 E9
VMC_RDQS2 E6
VMC_RDQS3 A8
VMC_RDQS4 B29
VMC_RDQS5 E25
VMC_RDQS6 A25
VMC_RDQS7 F21

FBCDQS_RN0 FBCDQS_RN1 FBCDQS_RN2 FBCDQS_RN3 FBCDQS_RN4 FBCDQS_RN5 FBCDQS_RN6 FBCDQS_RN7

*U_GPU_G3

FBVTT_0 AA23
FBVTT_1 AB23
FBVTT_2 H16
FBVTT_3 H17
FBVTT_4 J10
FBVTT_5 J23
FBVTT_6 J24
FBVTT_7 J9
FBVTT_8 K11
FBVTT_9 K12
FBVTT_10 K21
FBVTT_11 K22
FBVTT_12 K24
FBVTT_13 K9
FBVTT_14 L23
FBVTT_15 M23
FBVTT_16 T25
FBVTT_17 U25

C287 .1U/10V/04
C198 .1U/10V/04
C294 .1U/10V/04
C311 .1U/10V/04
C227 .47U/10V/06
C241 .47U/10V/06
C193 10U/4V/06
C288 .1U/10V/04
C298 .1U/10V/04
C284 .1U/10V/04
C737 .1U/10V/04
C272 .47U/10V/06
C161 .47U/10V/06
C251 10U/4V/06
+1.8V
PLACE NEAR GPU

18 VMA_DQ[63..0]
18 VMA_DM[7..0]
18 VMA_WDQS[7..0]
18 VMA_RDQS[7..0]

FBC_CMD0 C13 VMC_MA3
FBC_CMD1 A16 VMC_MA0
FBC_CMD2 A13 VMC_MA2
FBC_CMD3 B17 VMC_MA1
FBC_CMD4 B20 VMC_MA3H
FBC_CMD5 A19 VMC_MA4H
FBC_CMD6 B19 VMC_MA5H
FBC_CMD7 B14 VMC_BA2 T83
FBC_CMD8 E16 VMC_CS0#
FBC_CMD9 A14 VMC_WE#
FBC_CMD10 C15 VMC_BA0
FBC_CMD11 B16 VMC_CKE
FBC_CMD12 F17 VMC_ODT
FBC_CMD13 C19 VMC_MA2H
FBC_CMD14 D15 VMC_MA12
FBC_CMD15 C17 VMC_RAS#
FBC_CMD16 A17 VMC_MA11
FBC_CMD17 C16 VMC_MA10
FBC_CMD18 D14 VMC_BA1
FBC_CMD19 F16 VMC_MA8
FBC_CMD20 C14 VMC_MA9
FBC_CMD21 C18 VMC_MA6
FBC_CMD22 E14 VMC_MA5
FBC_CMD23 B13 VMC_MA7
FBC_CMD24 E13 VMC_MA4
FBC_CMD25 F15 VMC_CAS#
FBC_CMD26 A20 VMC_MA13 T212

VMC_MA3 19
VMC_MA0 19
VMC_MA2 19
VMC_MA1 19
VMC_MA3H 19
VMC_MA4H 19
VMC_MA5H 19
VMC_CS0# 19
VMC_WE# 19
VMC_BA0 19
VMC_CKE 19
VMC_MA2H 19
VMC_MA12 19
VMC_RAS# 19
VMC_MA11 19
VMC_MA10 19
VMC_BA1 19
VMC_MA8 19
VMC_MA9 19
VMC_MA6 19
VMC_MA5 19
VMC_MA7 19
VMC_MA4 19
VMC_CAS# 19

19 VMC_DQ[63..0]
19 VMC_DM[7..0]
19 VMC_WDQS[7..0]
19 VMC_RDQS[7..0]

VMA_ODT R832 0/04 VMA_ODT_R VMA_ODT_R 18
VMA_DEBUG R831 *0/04
R598 10K/04
G72M/G73M: STUFF
UMA:NC

VMC_ODT R830 0/04 VMC_ODT_R VMC_ODT_R 19
VMC_DEBUG R829 *0/04
R174 10K/04
G72M/G73M: STUFF
UMA:NC

FBC_CLK0 F13 VMC_CLK0
FBC_CLK0# F13 VMC_CLK0#
FBC_CLK1 F18 VMC_CLK1
FBC_CLK1# E17 VMC_CLK1#

VMC_CLK0 19
VMC_CLK0# 19
VMC_CLK1 19
VMC_CLK1# 19

RFU4 C20 FBC_CMD27 T211
RFU5 D1 G73_D1 T184
FBC_DEBUG F12 VMC_DEBUG

+3V +3V
R131 2.2K/04 R103 2.2K/04

I2C_DAT B1 I2C_DAT R137 0/04 I2CS_SDA
I2C_CLK C1 I2C_CLK R117 0/04 I2CS_SCL

YELLOW BLOCK is for G8X chip only

FBC_PLLVDD G8 G73_G8 T76
FBC_PLLAVDD G10 FBC_PLLAVDD 15mil L23 VGA1.2V
FBC_PLLGND G9
C731 470P/50V/04
C727 4700P/25V/04
C162 BLM18PG330SN1D/06
4.7U/10V/06

FBCAL_PD_VDDQ K26 FBCAL_PD R185 40.2/F/06 +1.8V
FBCAL_PU_GND H26 FBCAL_PU R187 40/F/04
FBCAL_TERM_GND J26 FBCAL_TERM R186 40.2/F/04

FB_VREF2 A28 FB_VREF2 15mil T213

F_VREF2 filter can be remove from nvidia HANK recommend
G70,G71: Stuff these parts
G72M,G73M : NC

+3V
Q51 2N7002E
5,36,37,41,48 MBDATA I2CS_SDA
Q52 2N7002E
5,36,37,41,48 MBCLK I2CS_SCL

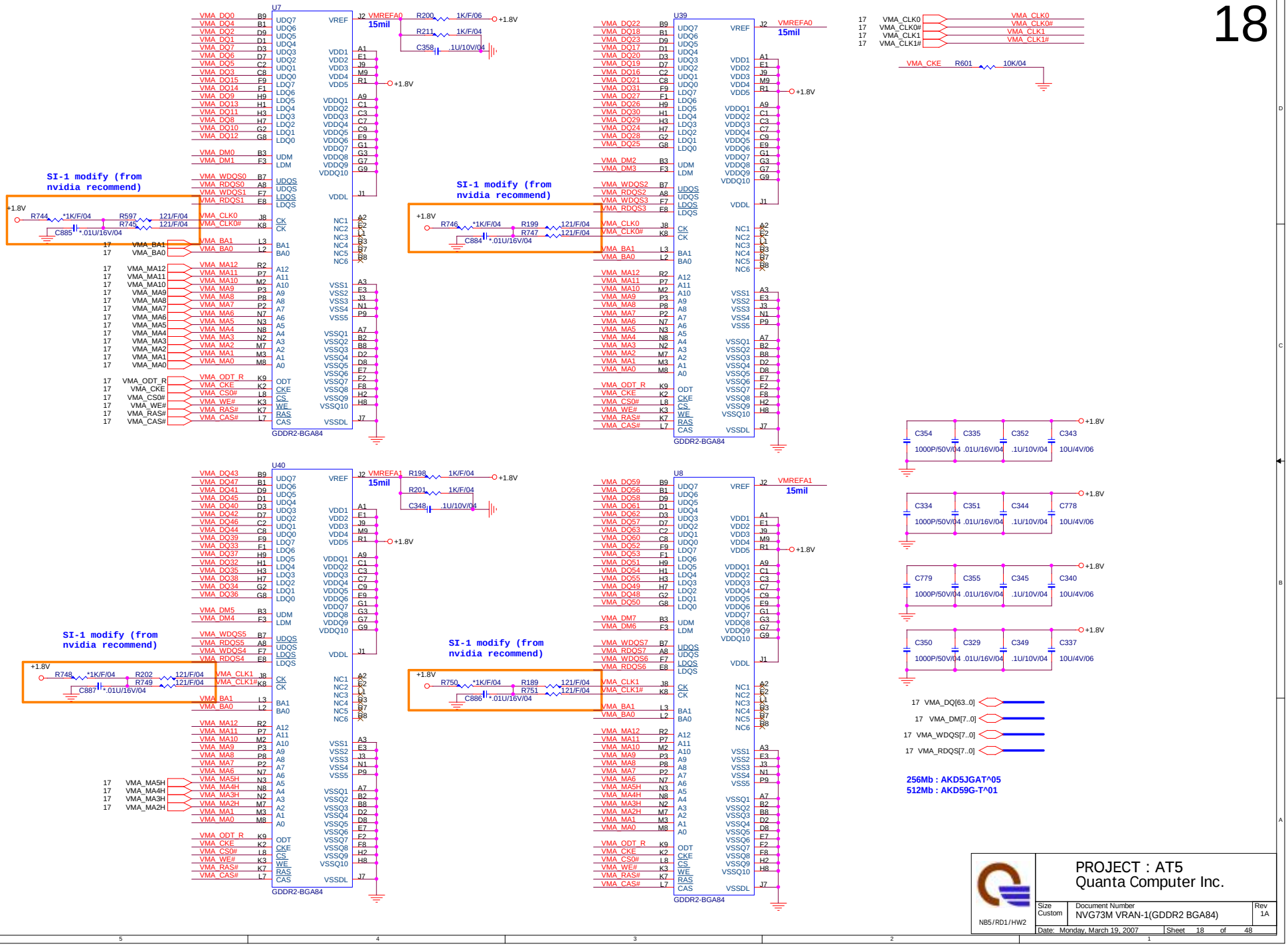
SI-2 modified for G8X thermal sensor

PROJECT : AT5
Quanta Computer Inc.

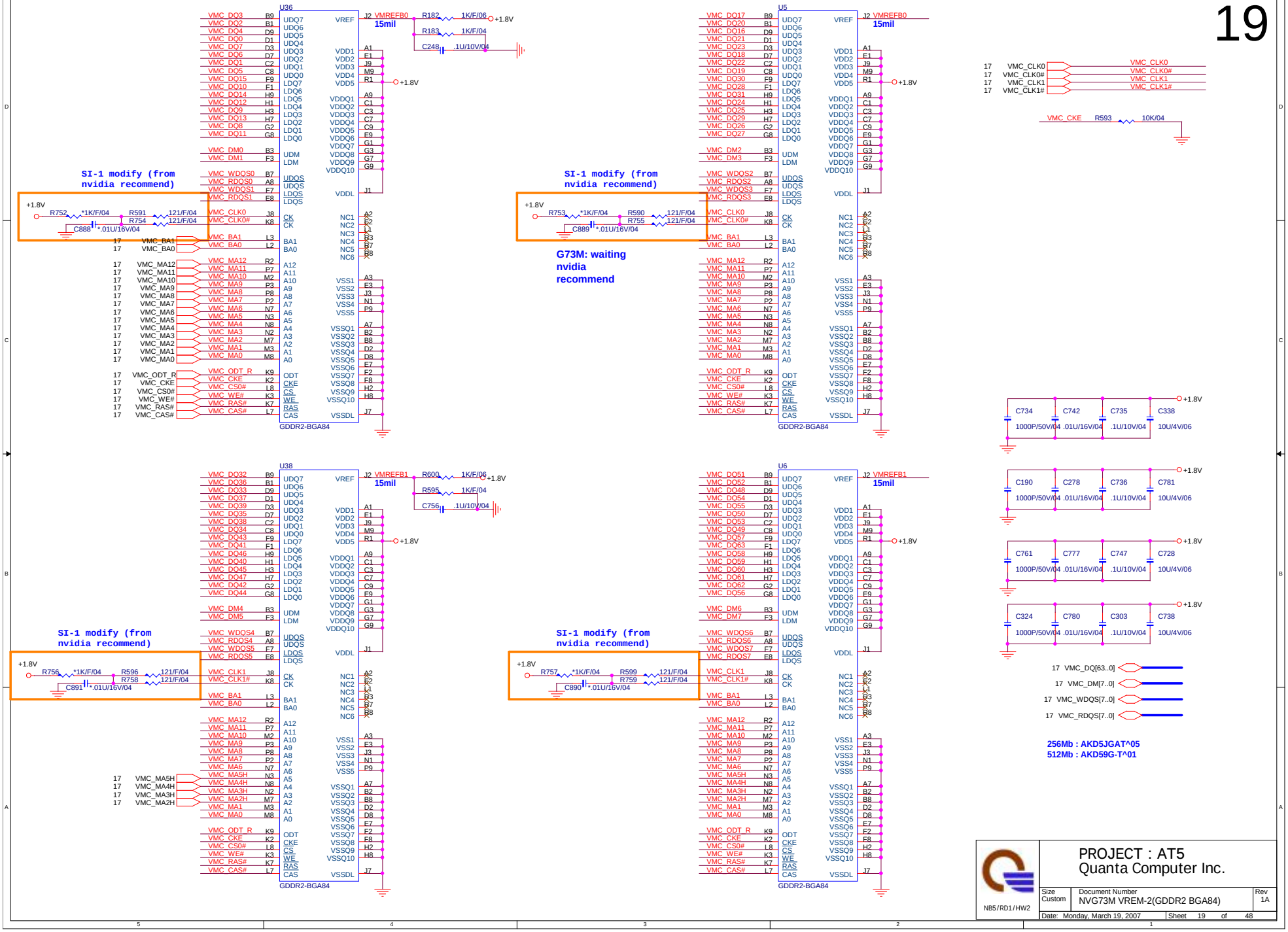
NB5/RD1/HW2

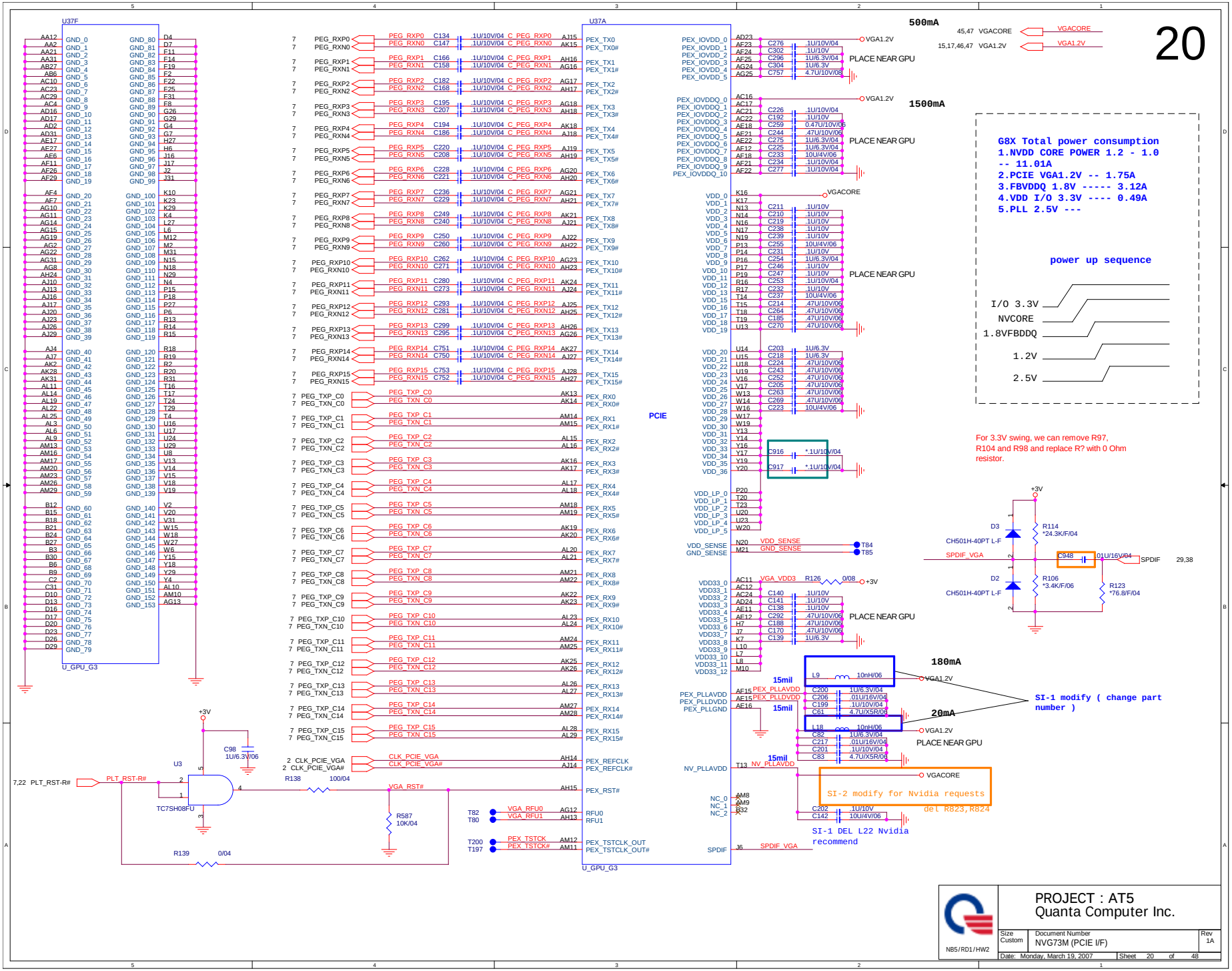
Size	Document Number	Rev
Custom	NVG73M (MEM I/F)	1A

Date: Monday, March 19, 2007 Sheet 17 of 48



PROJECT : AT5	
Quanta Computer Inc.	
NB5/RD1/HW2	
Size: Custom	Document Number: NVG73M VRAN-1(GDDR2 BGA84)
Rev: 1A	
Date: Monday, March 19, 2007	Sheet 18 of 48


U36
U5
U38
U6
GDDR2-BGA84
SI-1 modify (from nvidia recommend)
G73M: waiting nvidia recommend
15mil
VMC_CLK0
VMC_CLK0#
VMC_CLK1
VMC_CLK1#
VMC_CKE R593 10K/04
C734 C742 C735 C338
C190 C278 C736 C781
C761 C777 C747 C728
C324 C780 C303 C738
1000P/50V/04 .01U/16V/04 .1U/10V/04 10U/4V/06
+1.8V
VMC_DQ[63..0]
VMC_DM[7..0]
VMC_WDQS[7..0]
VMC_RDQS[7..0]
256Mb : AKD5JGAT^05
512Mb : AKD59G-T^01
PROJECT : AT5
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number NVG73M VREM-2(GDDR2 BGA84)
Rev 1A
Date: Monday, March 19, 2007
Sheet 19 of 48



PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NVG73M (PCIE I/F)	1A
NB5/RD1/HW2	Date: Monday, March 19, 2007	Sheet 20 of 48

RTC

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF

Place near to Mini-door

VCCRTC
3VPCU
D41 CH500H-40
D42 CH500H-40
C804 1U/16V/06
R638 20K/06
R635 1K/06
R637 1M/F/06
C811 1U/16V/06
G2 *SHORT_PAD1
BT1 BAT_CONN
CN30 *CWY020-B0G1Z
SI-2-1 modified (change to battery con)

C820 15P/50V/04
C817 15P/50V/04
Y6 32.768KHZ
R663 10M/06
CLK_32KX1
CLK_32KX2

5VPCU
20MIL
20MIL
Q42 *MMBT3904
R625 *1.2K/06
R628 *1K/06
R626 *4.7K/06
R629 *15K/06
add RTC Bat rechargeable circuit

U42A

RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS

RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
IDE

SI-1 modified

ICH8M REV 1.0

FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0 DD1 DD2 DD3 DD4 DD5 DD6 DD7 DD8 DD9 DD10 DD11 DD12 DD13 DD14 DD15
DA0 DA1 DA2
DCS1# DCS3#
DIOR# DIOW# DDACK# IDEIRQ IORDY DDREQ

PDD[15:0] 32
PDA[2:0] 32
PDCS1# 32
PDCS3# 32
PDIOR# 32
PDIOW# 32
PDDACK# 32
IRQ14 32
PDIORDY 32
PDDREQ 32

R409 *56/F/06
R449 *56/F/06
R447 10K/06
R648 10K/06
R442 56/F/06
R849 56/04
R439 0/06
R415 0/F/06
R432 0/F/06
R425 0/F/06
R406 24.9/F/06
R334 24.9/F/04
R655 24.9/F/06
R691 10K/06

SI-2 add for fix ESD issue

Should be 2" close ICH7
C560 *SFI0603-050E101NP/06

Place within 500 mils of ICH7
25mils/15mils

SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

R443 332K/F/06 — ICH_INTVRMEN — R417 *0
R444 332K/F/06 — LAN100_SLP — R414 *0
R644 *1K/06 — ACZ_SDOUT — ICH_TP3 23 — R428 *1K

intel check list define to stuff 33ohm

ACZ_SDOUT R654 33/04 ACZ_SDOUT_AUDIO 29 — C814 *10P/50V/04
ACZ_SYNC R649 33/04 ACZ_SYNC_AUDIO 29 — C816 *10P/50V/04
ACZ_BCLK R653 33/04 BIT_CLK_AUDIO 29 — C813 *10P/50V/04
ACZ_RST# R646 33/04 ACZ_RST#_AUDIO 29

ACZ_SDOUT R639 33/04 ACZ_SDOUT_AUDIO_MDC 31 — C807 *10P/50V/04
ACZ_SYNC R640 33/04 ACZ_SYNC_AUDIO_MDC 31 — C809 *10P/50V/04
ACZ_BCLK R643 33/04 BIT_CLK_AUDIO_MDC 31 — C810 *10P/50V/04
ACZ_RST# R645 33/04 ACZ_RST#_AUDIO_MDC 31

PROJECT : AT5
Quanta Computer Inc.

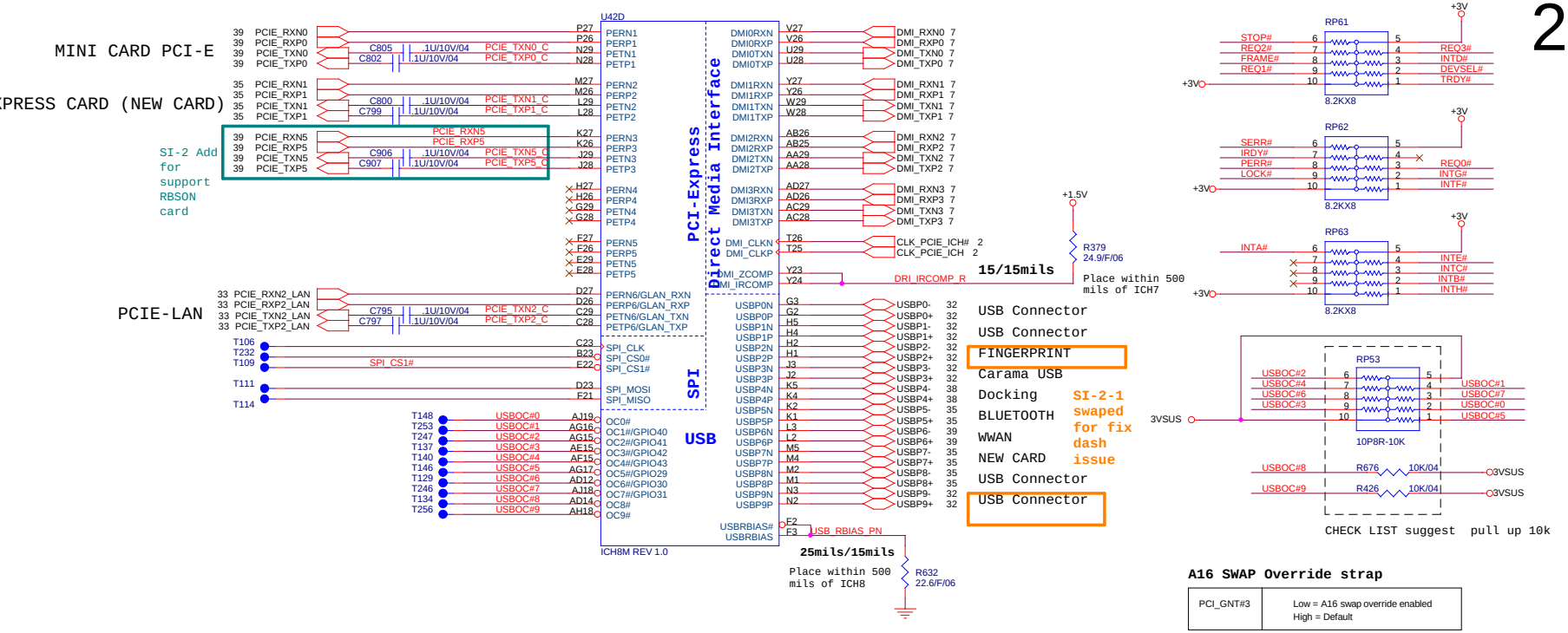
Size	Document Number	Rev
Custom	ICH7-M HOST(1/4)	1A
NB5/RD1/HW2	Date: Monday, March 19, 2007	Sheet 21 of 48

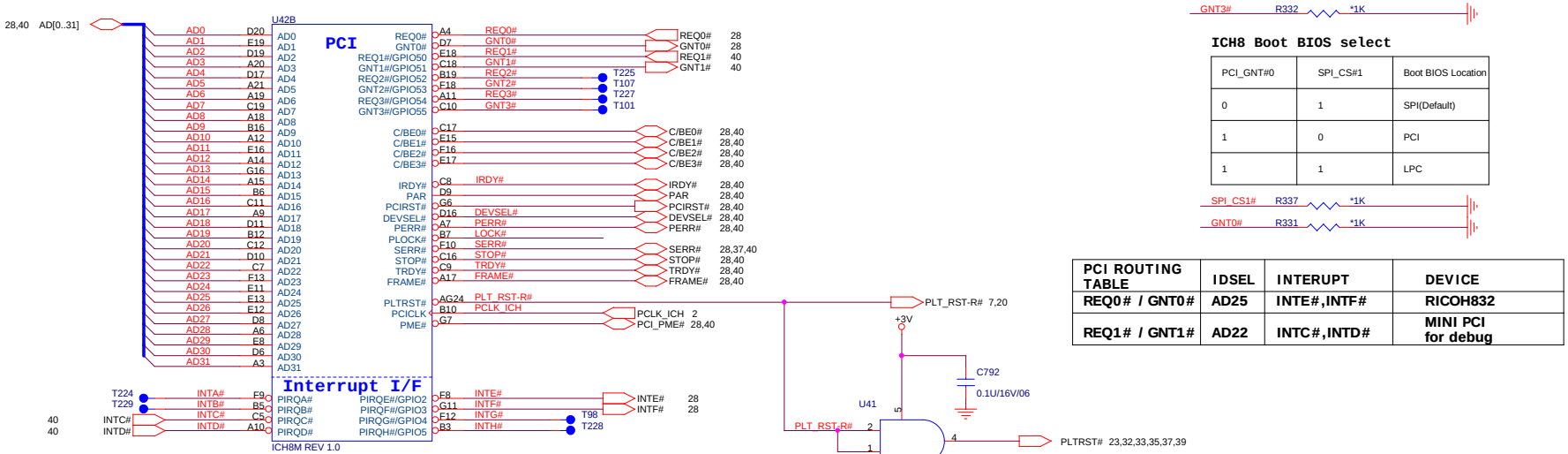
MINI CARD PCI-E

EXPRESS CARD (NEW CARD)

SI-2 Add for support RBSON card

PCIE-LAN





A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

GNT3# R332 *1K

ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R337 *1K

GNT0# R331 *1K

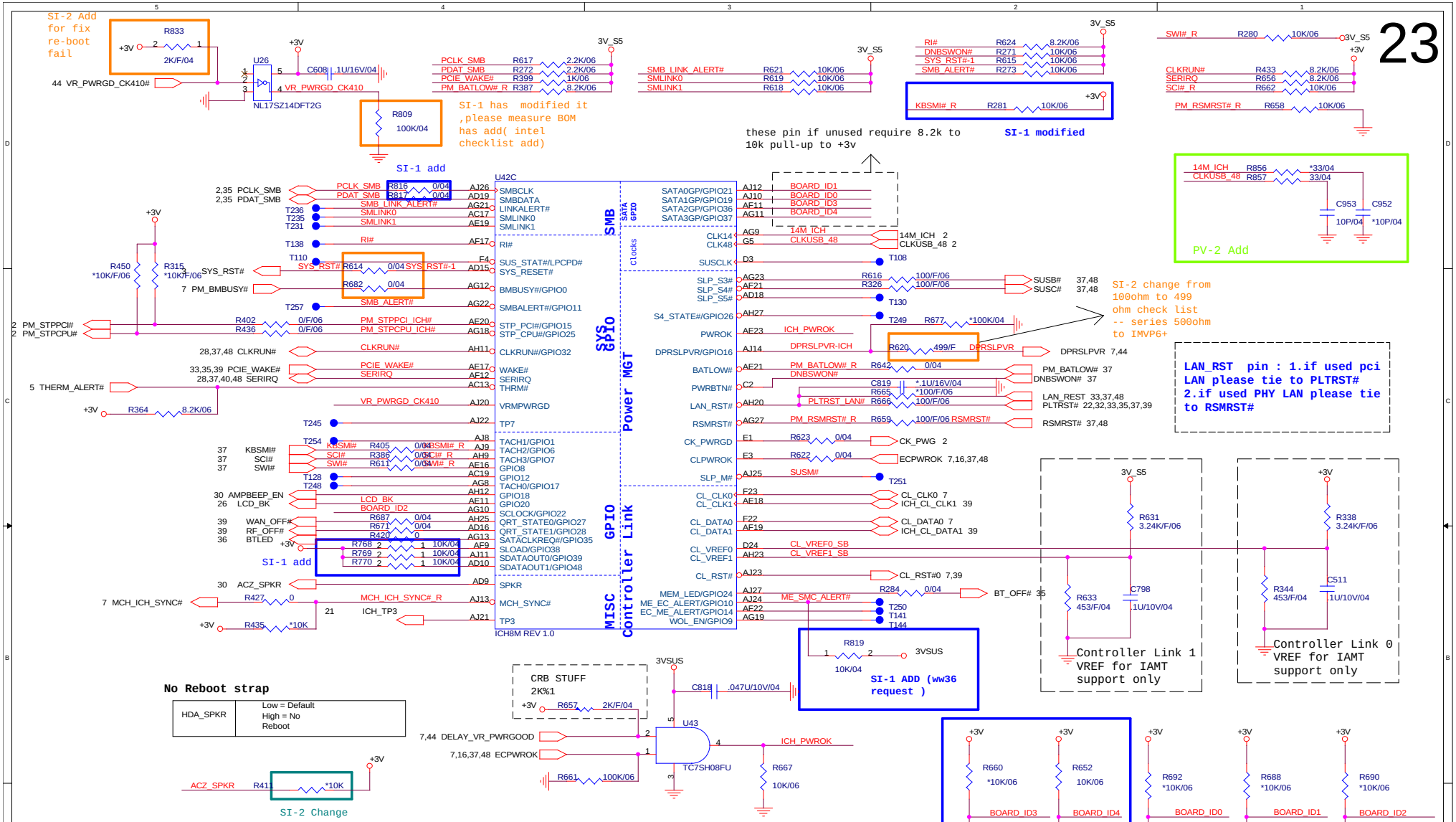
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

PROJECT : AT5
Quanta Computer Inc.

NB5/RD1/HW2

Size	Document Number	Rev
Custom	ICH7-M M PCI E(2/4)	1A

Date: Monday, March 19, 2007 Sheet 22 of 48



Board ID	15 " PAV UMA 965GM (0:0:0)	15" PRE UMA 965GM (0:0:1)	15″PAV Discrete 965PM+G86MV+128M (0:1:0)	17″ PAV Discrete 965PM+G86MV+128M (0:1:1)	17″ PAV Discrete 965PM+G84MV+256M (1:0:0)	17″ PAV UMA 965GM (1:0:1)
ID0	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff
ID1	R448 Stuff	R448 Stuff	R688 Stuff	R688 Stuff	R448 Stuff	R448 Stuff
ID2	R689 Stuff	R689 Stuff	R689 Stuff	R689 Stuff	R690 Stuff	R690 Stuff

PROJECT : AT5
Quanta Computer Inc.

NB5/RD1/HW2

Size	Document Number	Rev
Custom	ICH7-M GPIO(3/4)	1A

Date: Monday, March 19, 2007 Sheet 23 of 48

1.5V_A 1.5A
1.5V_B 675mA
VCC1.05 1.13A

V5REF 1mA
V5REF_SUS 1mA
VCCSATAPLL 47mA
SI-2 modified (remove R374)
VCCUSBPLL 10mA
VCCGLAN3.3 1mA
VCCGLLAN_PLL --23mA
VCCGLAN1.5 80mA
VCCGLAN3.3 18mA
VCCDMIPLL 23mA
VCC_DMI 50mA
VCPU_IO 1mA
VCC3.3 278mA
VCC_SUSHDA 32mA
VCCHDA 32mA
VCC_SUS3.3 177mA
VCCL3.3 18mA - 64mA (S3)

Can be connect to +3V_S5 or +1.5V_S5
Can be connect to +3V or +1.5V

PROJECT : AT5
Quanta Computer Inc.
NB5/RD1/HW2
Size: Custom
Document Number: ICH7-M POWER(4/4)
Rev: 1A
Date: Monday, March 19, 2007
Sheet 24 of 48

CRT PORT

25

SI-1 modified for fix CRT rise time issue

close conn within 600mils

EMI

CRT SWITCH

SI-1 modified for fix CRT rise time issue

U51

74CBT3257

inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

filter for HDTV

SI-1 MODIFY

TV_OUT

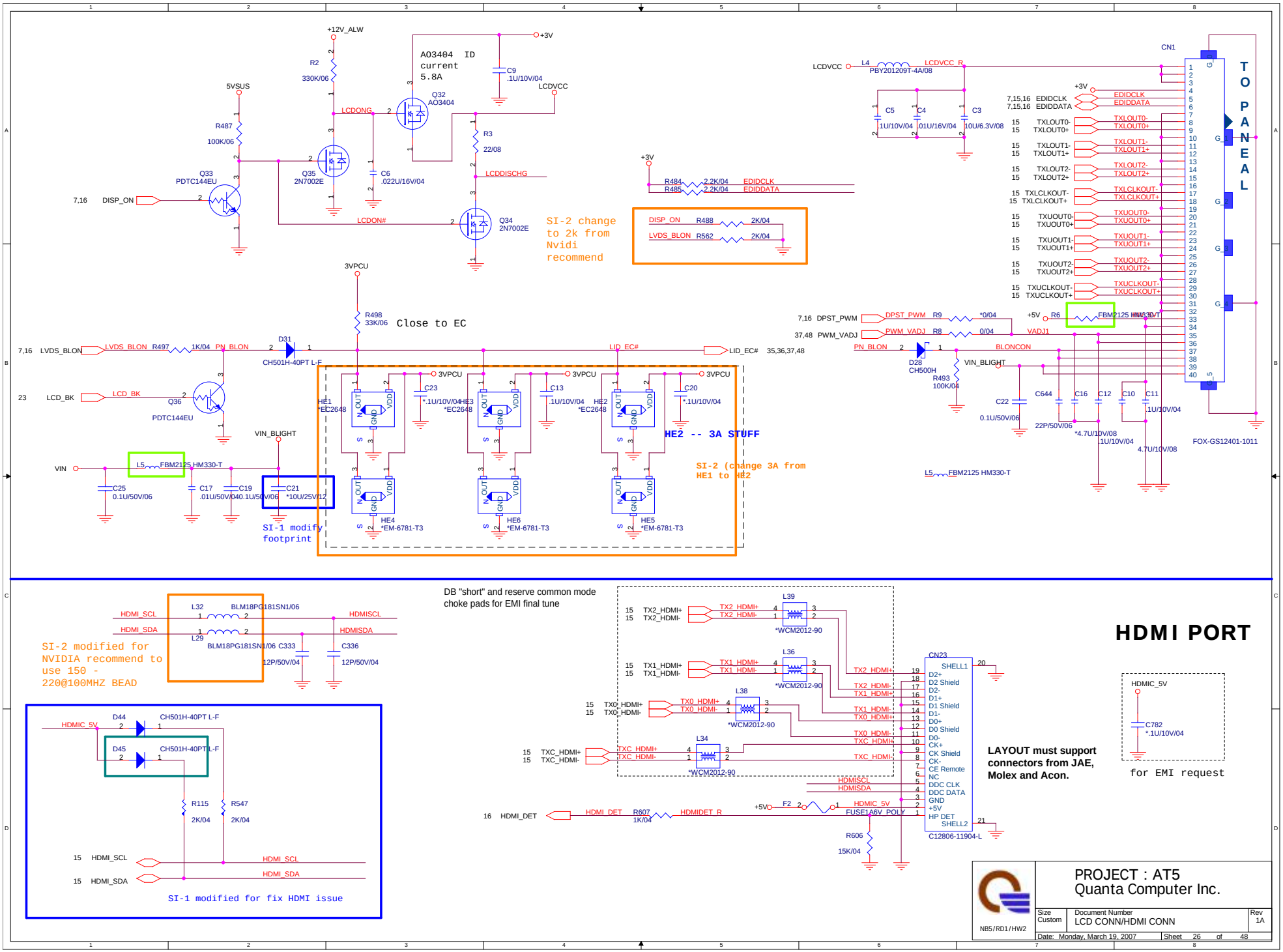
SUY-030005FR007S102FU

PROJECT : AT5
Quanta Computer Inc.

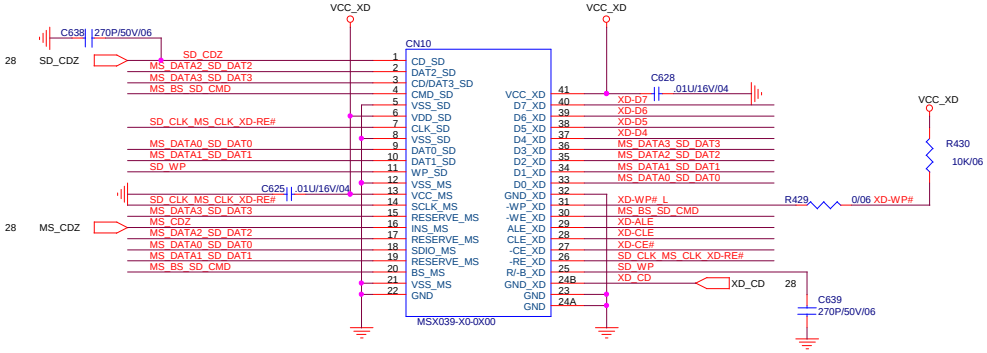
NB5/RD1/HW2

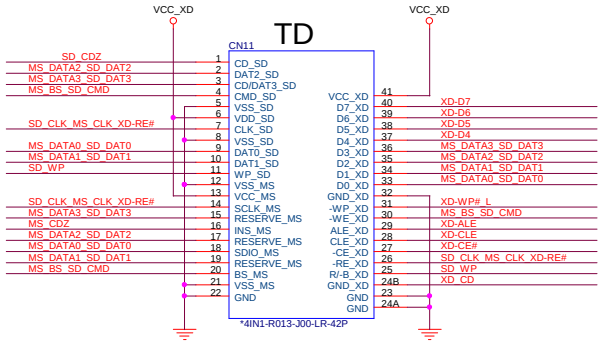
Size: Custom | Document Number: CRT/TV_OUT | Rev: 1A

Date: Monday, March 19, 2007 | Sheet 25 of 48

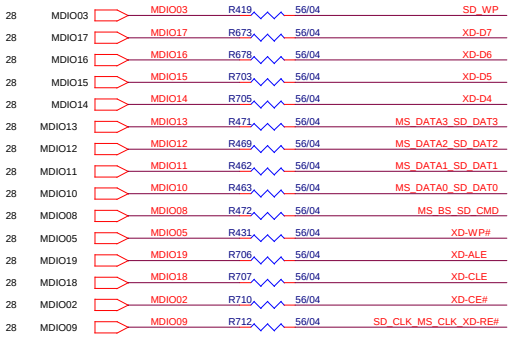

+12V_ALW
R2
330K/06
AO3404 ID current 5.8A
+3V
C9 .1U/10V/04
LCDVCC
5VSUS
Q32 AO3404
LCDONG
R487 100K/06
Q33 PDTC144EU
Q35 2N7002E
C6 .022U/16V/04
R3 22/08
LCDDISCHG
7,16 DISP_ON
LCDON#
Q34 2N7002E
SI-2 change to 2k from Nvidi recommend
R484 2.2K/04 EDIDCLK
R485 2.2K/04 EDIDDATA
DISP_ON R488 2K/04
LVDS_BLON R562 2K/04
LCDVCC L4 PBY201209T-4A/08 LCDVCC_R
C5 1U/10V/04
C4 .01U/16V/04
C3 10U/6.3V/08
CN1
TO PANEL
7,15,16 EDIDCLK
7,15,16 EDIDDATA
15 TXLOUT0-
15 TXLOUT0+
15 TXLOUT1-
15 TXLOUT1+
15 TXLOUT2-
15 TXLOUT2+
15 TXLCLKOUT-
15 TXLCLKOUT+
15 TXUOUT0-
15 TXUOUT0+
15 TXUOUT1-
15 TXUOUT1+
15 TXUOUT2-
15 TXUOUT2+
15 TXUCLKOUT-
15 TXUCLKOUT+
3VPCU
R498 33K/06
Close to EC
7,16 LVDS_BLON
LVDS_BLON R497 1K/04 PN_BLON
D31 CH501H-40PT L-F
LID_EC#
LID_EC# 35,36,37,48
23 LCD_BK
Q36 PDTC144EU
VIN_BLIGHT
VIN
L5 FBM2125 HM330-T
C25 0.1U/50V/06
C17 .01U/50V/04
C19 0.1U/50V/06
C21 *10U/25V/12
C23 *.1U/10V/04
C13 .1U/10V/04
C20 *.1U/10V/04
HE1 *EC2648
HE3 *EC2648
HE2 *EC2648
HE4 *EM-6781-T3
HE6 *EM-6781-T3
HE5 *EM-6781-T3
HE2 -- 3A STUFF
SI-2 (change 3A from HE1 to HE2
SI-1 modify footprint
7,16 DPST_PWM
DPST_PWM R9 *0/04
37,48 PWM_VADJ
PWM_VADJ R8 0/04
+5V R6 FBM2125 HM330-T
VADJ1
PN_BLON
D28 CH500H
BLONCON
R493 100K/04
C22 0.1U/50V/06
C644 22P/50V/06
C16 *4.7U/10V/08
C12 .1U/10V/04
C10
C11 4.7U/10V/08
FOX-GS12401-1011
L5 FBM2125 HM330-T
HDMI_SCL
HDMI_SDA
L32 BLM18PG181SN1/06
L29 BLM18PG181SN1/06
C333 12P/50V/04
C336 12P/50V/04
HDMISCL
HDMISDA
SI-2 modified for NVIDIA recommend to use 150 - 220@100MHZ BEAD
DB "short" and reserve common mode choke pads for EMI final tune
L39
L36
L38
L34
*WCM2012-90
15 TX2_HDMI+
15 TX2_HDMI-
15 TX1_HDMI+
15 TX1_HDMI-
15 TX0_HDMI+
15 TX0_HDMI-
15 TXC_HDMI+
15 TXC_HDMI-
CN23
SHELL1
D2+
D2 Shield
D2-
D1+
D1 Shield
D1-
D0+
D0 Shield
D0-
CK+
CK Shield
CK-
CE Remote
NC
DDC CLK
DDC DATA
GND
+5V
HP DET
SHELL2
C12806-11904-L
LAYOUT must support connectors from JAE, Molex and Acon.
HDMI PORT
HDMIC_5V
C782 *.1U/10V/04
for EMI request
D44 CH501H-40PT L-F
D45 CH501H-40PT L-F
R115 2K/04
R547 2K/04
15 HDMI_SCL
15 HDMI_SDA
SI-1 modified for fix HDMI issue
16 HDMI_DET
HDMI_DET R607 1K/04
HDMIDET_R
F2 FUSE1A6V_POLY
R606 15K/04
PROJECT : AT5
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number LCD CONN/HDMI CONN
Rev 1A
Date: Monday, March 19, 2007
Sheet 26 of 48

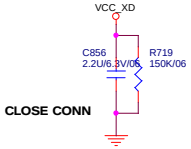
5 IN1 CARD READER
XD,MMC/SD,MS/MSP

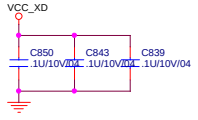


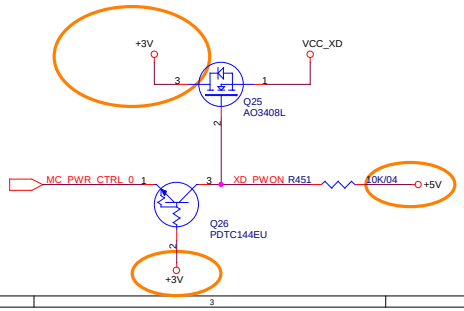


bom create 2'nd source

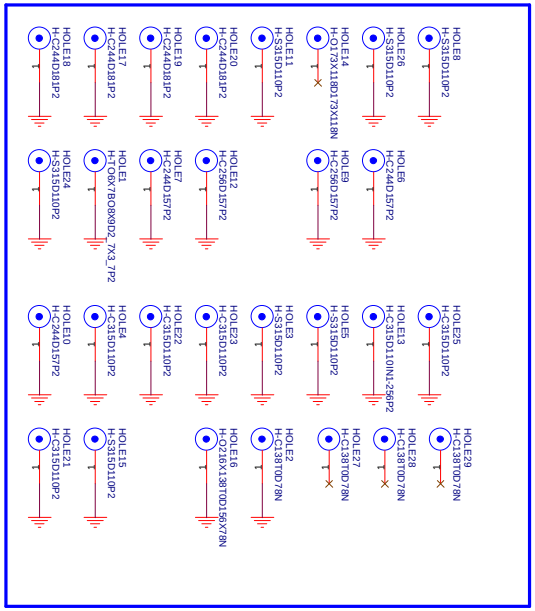




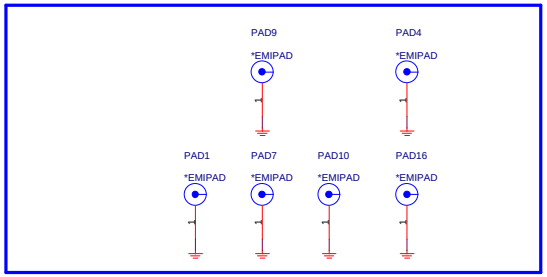


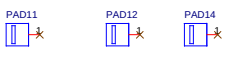


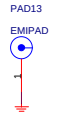
SCREW HOLE



EMI PAD

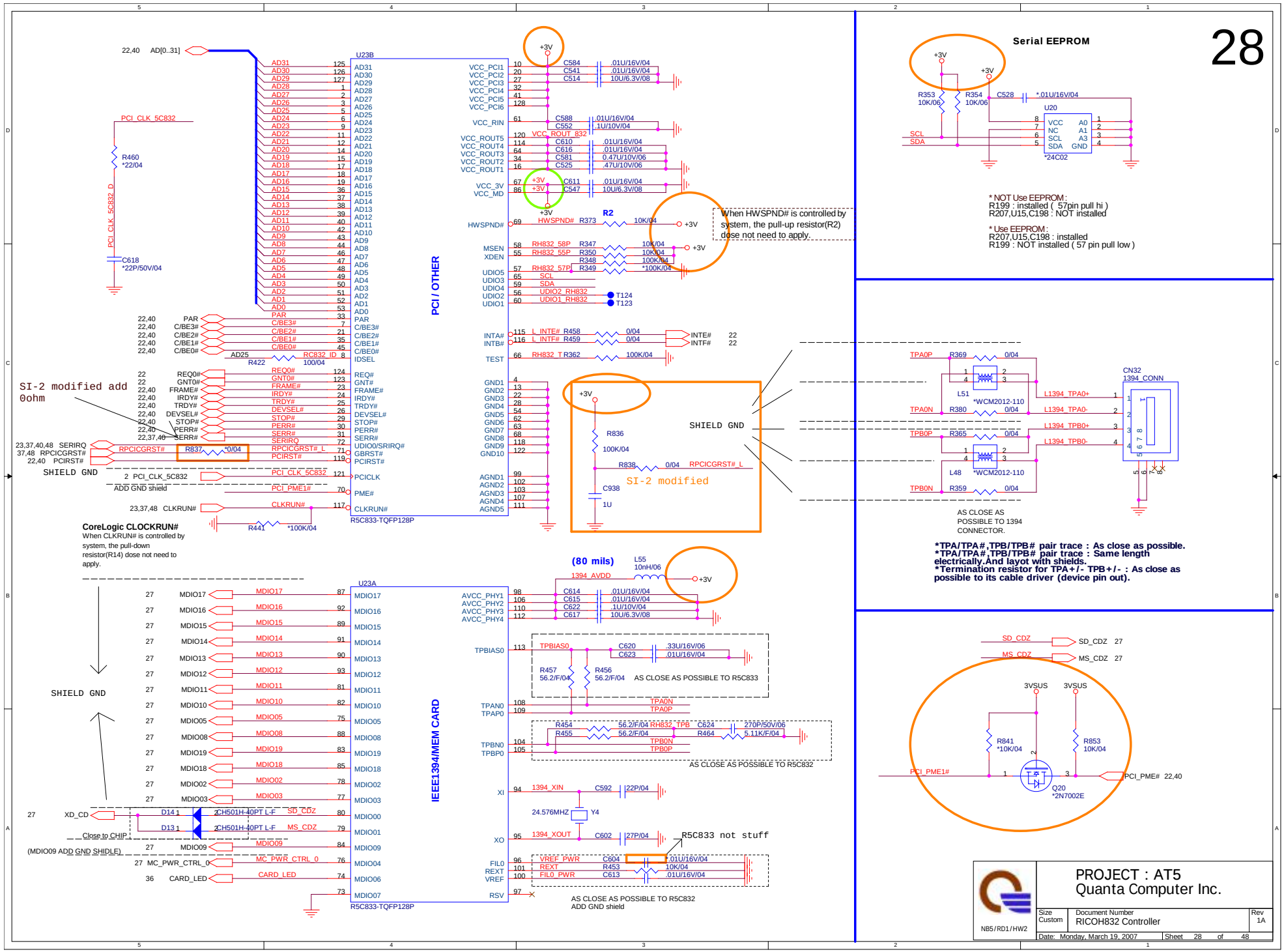


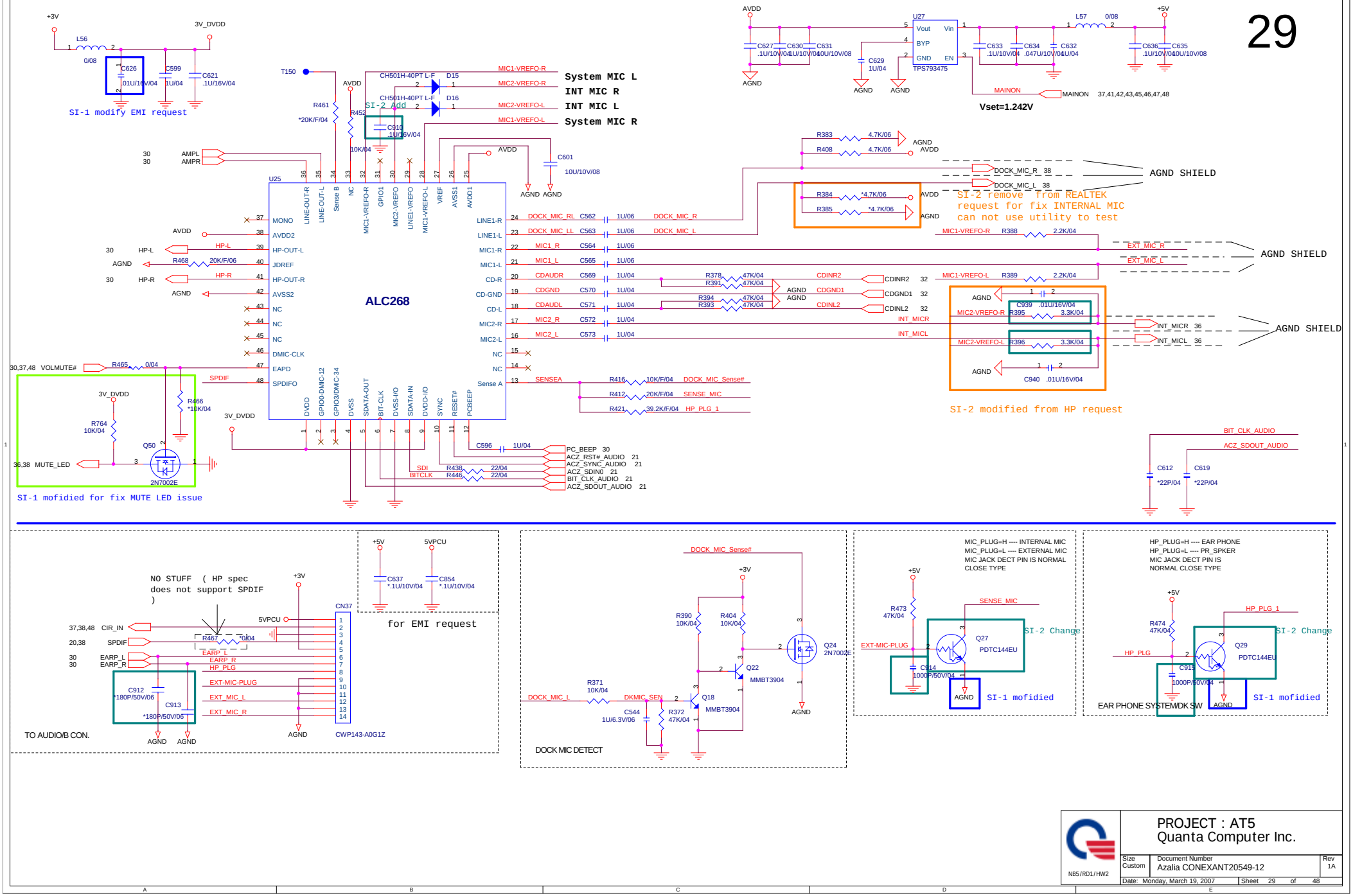




moden cable sprig

NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.		
	Size: Custom	Document Number: CARD READER/HOLE	Rev: 1A
	Date: Monday, March 19, 2007	Sheet 27 of 48	


U23B
PCI / OTHER
R5C833-TQFP128P
U23A
IEEE1394/MEM CARD
R5C833-TQFP128P
SHIELD GND
SI-2 modified add 0ohm
SI-2 modified
CoreLogic CLOCKRUN#
When CLKRUN# is controlled by system, the pull-down resistor(R14) dose not need to apply.
When HWSPND# is controlled by system, the pull-up resistor(R2) dose not need to apply.
(80 mils)
AS CLOSE AS POSSIBLE TO R5C833
AS CLOSE AS POSSIBLE TO R5C832
AS CLOSE AS POSSIBLE TO R5C832
ADD GND shield
R5C833 not stuff
Close to CHIP
(MDIO09 ADD GND SHIDLE)
Serial EEPROM
* NOT Use EEPROM :
R199 : installed (57pin pull hi)
R207,U15,C198 : NOT installed
* Use EEPROM :
R207,U15,C198 : installed
R199 : NOT installed (57 pin pull low)
CN32
1394_CONN
AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.
*TPA/TPA#,TPB/TPB# pair trace : As close as possible.
*TPA/TPA#,TPB/TPB# pair trace : Same length electrically.And layot with shields.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).
PROJECT : AT5
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number RICOH832 Controller
Rev 1A
Date: Monday, March 19, 2007
Sheet 28 of 48



PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia CONEXANT20549-12	1A

NB5/RD1/HW2

Date: Monday, March 19, 2007 Sheet 29 of 48

AUDIO AMPLIFIER

SI-2 remove r739 ,r731 from realtek request for fix BO voice when audio jack unplug

0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	**0**	**0**	**15.6dB**
1	1	0	21.6dB
x	x	1	4.1dB

PV-2 emi requests

SI-1 ADD EMI request

INT. SPEAKER

EMI requests change footprint

SI-1 DEL EMI request

SI-1 ADD EMI request

PCSPK BEEP

TO CODE

TO AMP

SI-1 add R765 and remove * part

SI-1 add R807 and remove *part

(AMP BEEP ENABLE AT SYSTEM BOOT) H=ENABLE L=DISABLE

LINE OUT Amplifier

LINE OUT Amplifier

MAX4411 EP can NOT be connected to GND. Please leave EP pins floating.

SI-2 modified from HP recommend

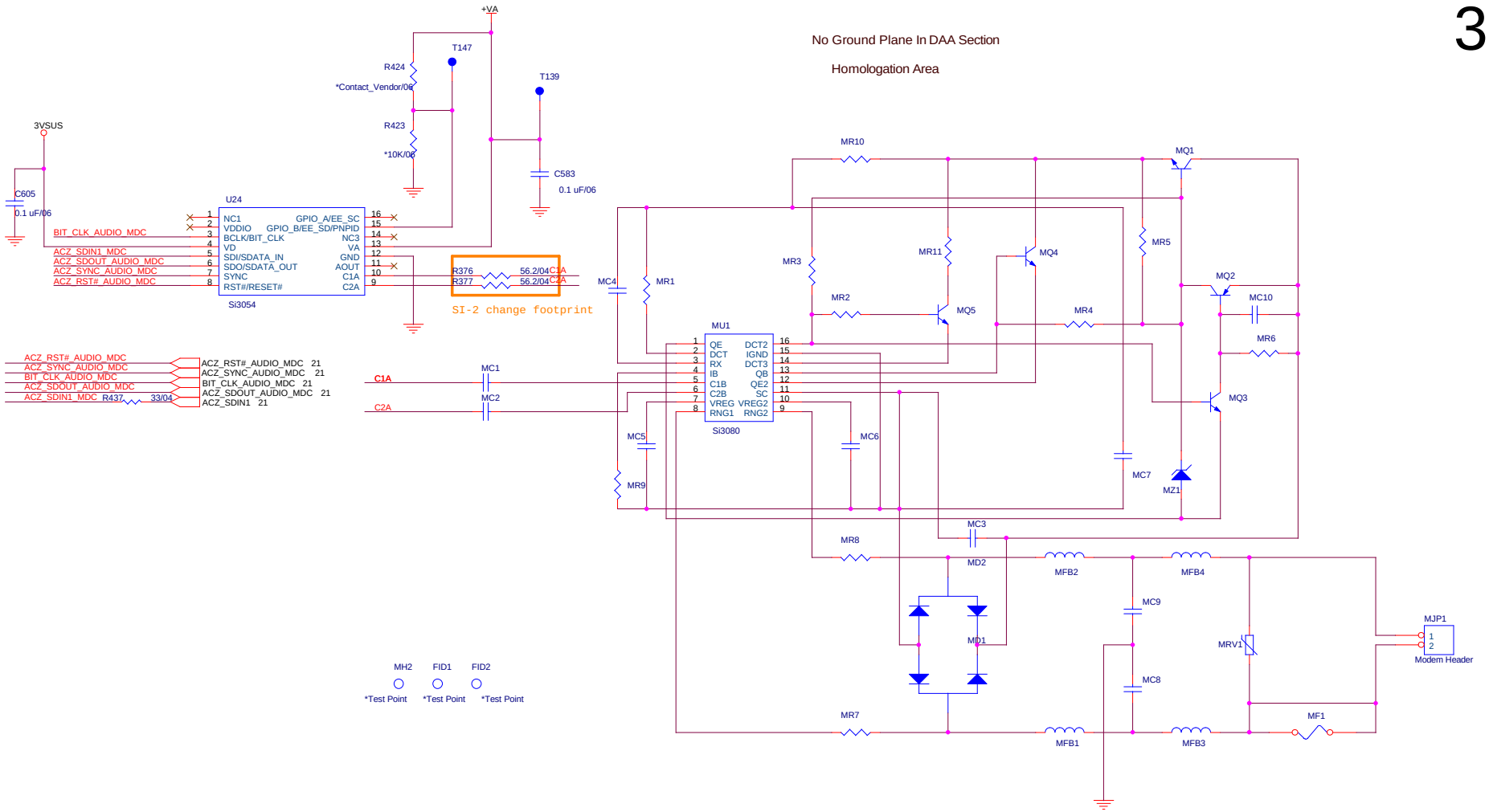
QFN20-4X4-5-25P

PROJECT : AT5
Quanta Computer Inc.

NB5/RD1/HW2

Size	Document Number	Rev
Custom	JACK/AMP_TAP0312	1A

Date: Monday, March 19, 2007 Sheet 30 of 48

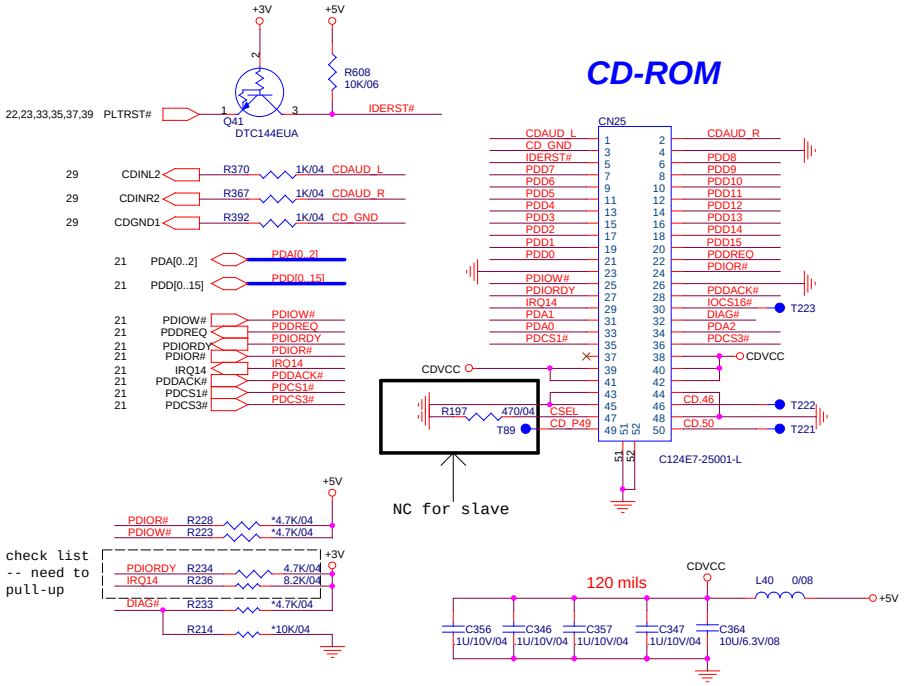


DESIGN SUBJECT TO CHANGE

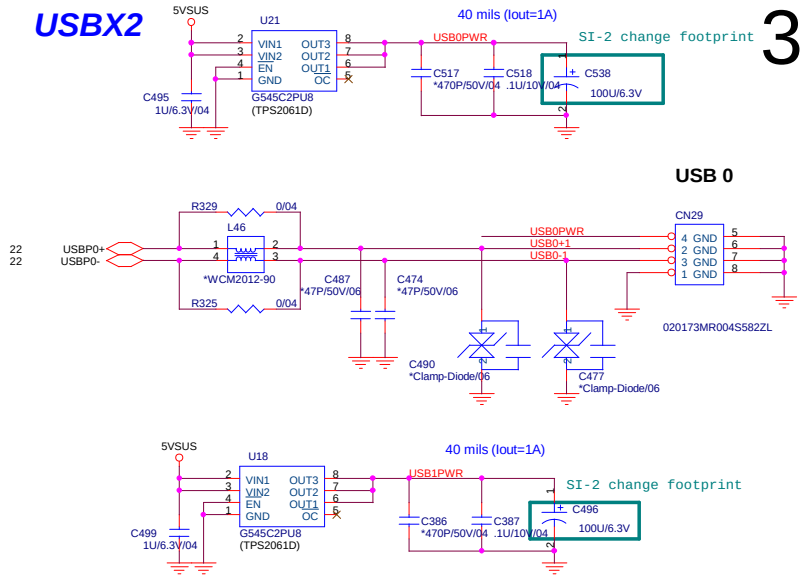
SILICON LABORATORIES CONFIDENTIAL

NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.	
	Size: Custom	Document Number: MODEM(DAA) — Rev: 1A
	Date: Monday, March 19, 2007	Sheet 31 of 48

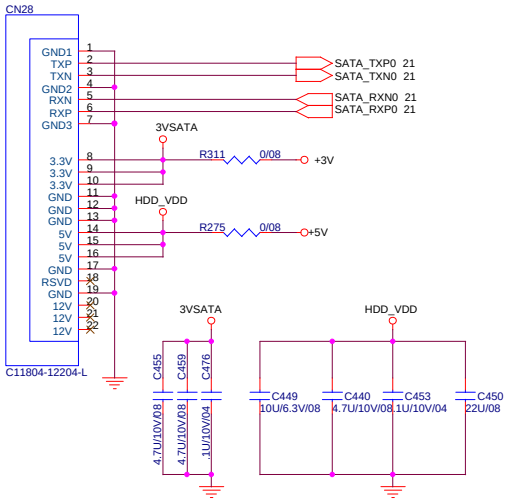
CD-ROM



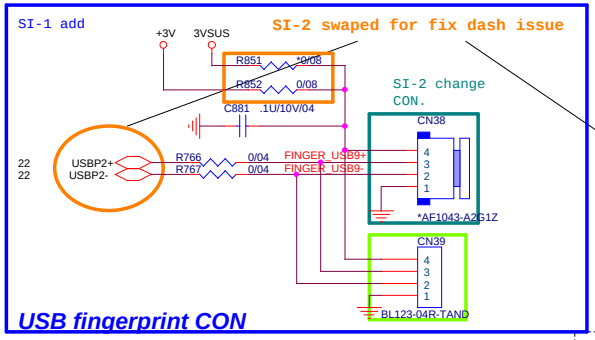
USBX2



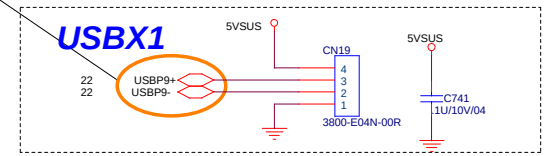
SATA_1 CONNECTOR



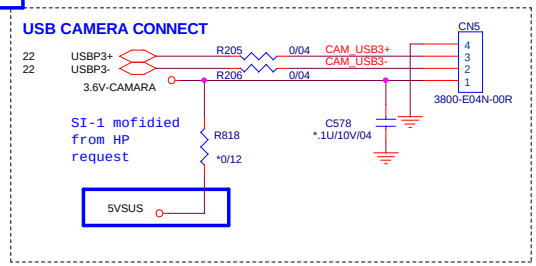
USB fingerprint CON

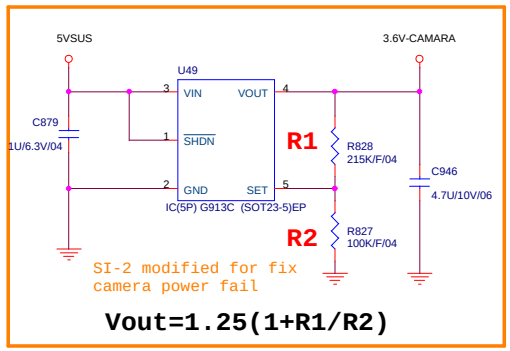


USBX1



USB CAMERA CONNECT





PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/CD-ROM/USBX3	1A

NB5/RD1/HW2

Date: Monday, March 19, 2007 Sheet 32 of 48

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)

giga LAN part number AJ081110006

SI-1 BOM add to fix 10/100 LAN LED issue

R21 value should be 2.49K (1%) for 8111B/8111C application. R21 should be 2.0K(1%) for 8101E application

BLOCK A is only for RTL8101E application.

Block A

for 93C56 used. NC if 93C46 is used.

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

RJ45

SI-1 modified to fix giga LAN LED issue

Remove R70 for 8111B and 8111C

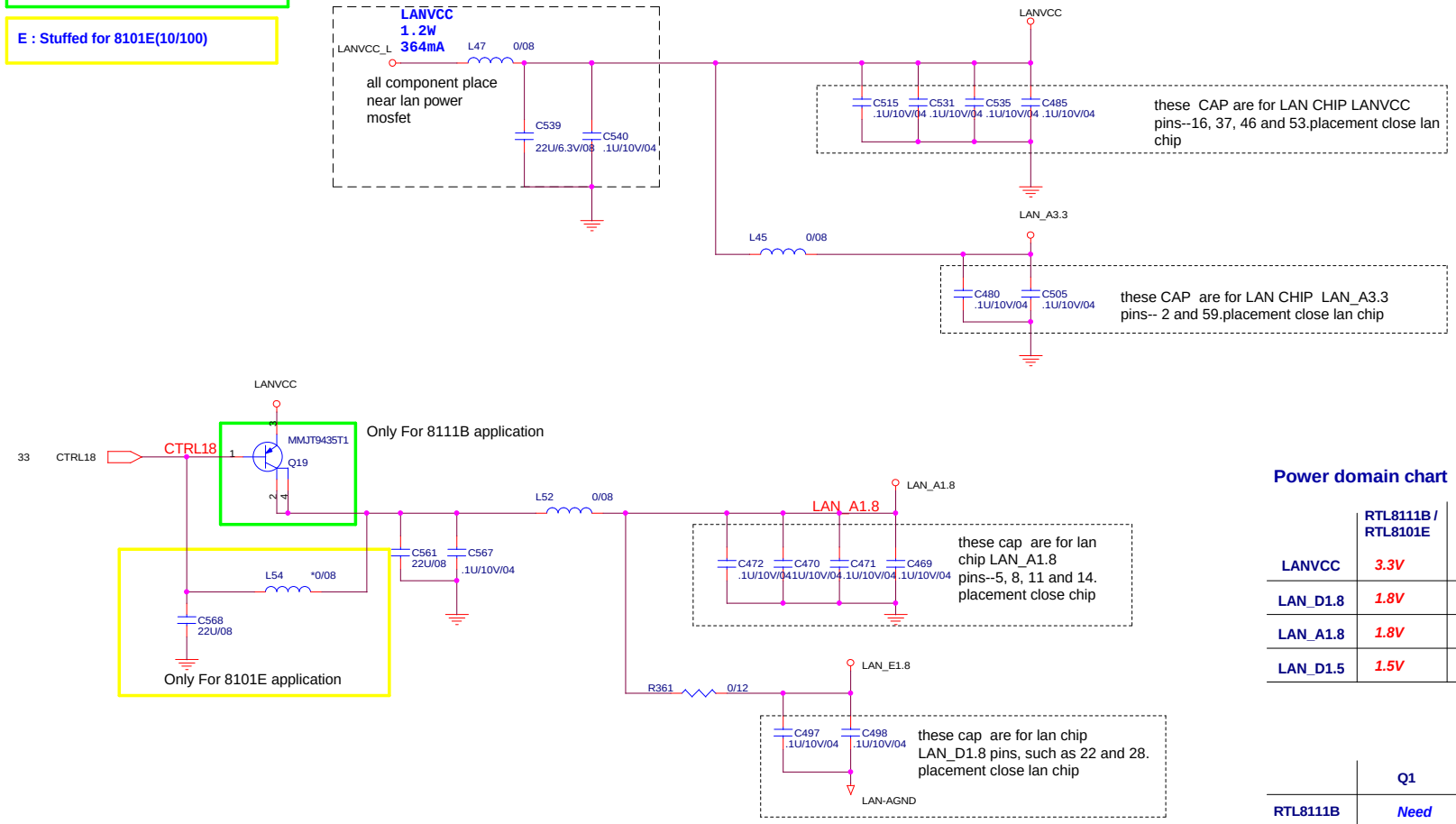
NS892403:GIGABIT
NS892405:10/100

close U6

PROJECT : AT5 Quanta Computer Inc.			
NB5/RD1/HW2	Size: Custom	Document Number: RTL8111B/8111C/8101E	Rev: 1A
	Date: Monday, March 19, 2007	Sheet 33 of 48	

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)



Power domain chart

	RTL8111B / RTL8101E
LANVCC	3.3V
LAN_D1.8	1.8V
LAN_A1.8	1.8V
LAN_D1.5	1.5V

	Q1	Q3
RTL8111B	Need	Need
RTL8101E	N/A	N/A

NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
A3	LAN POWER	1A

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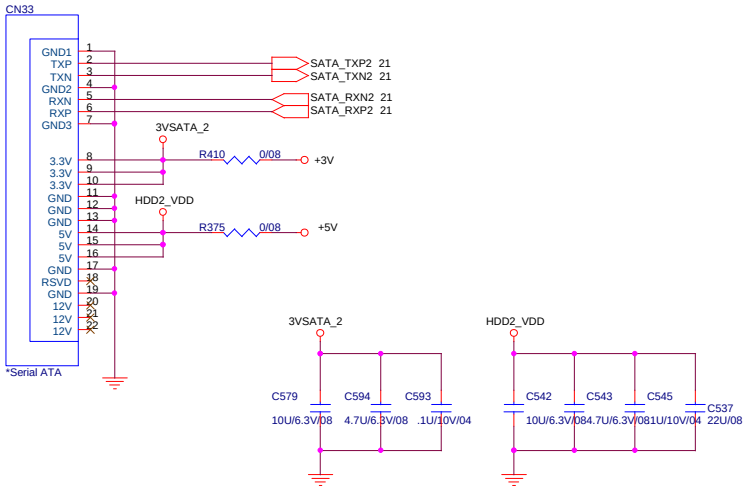
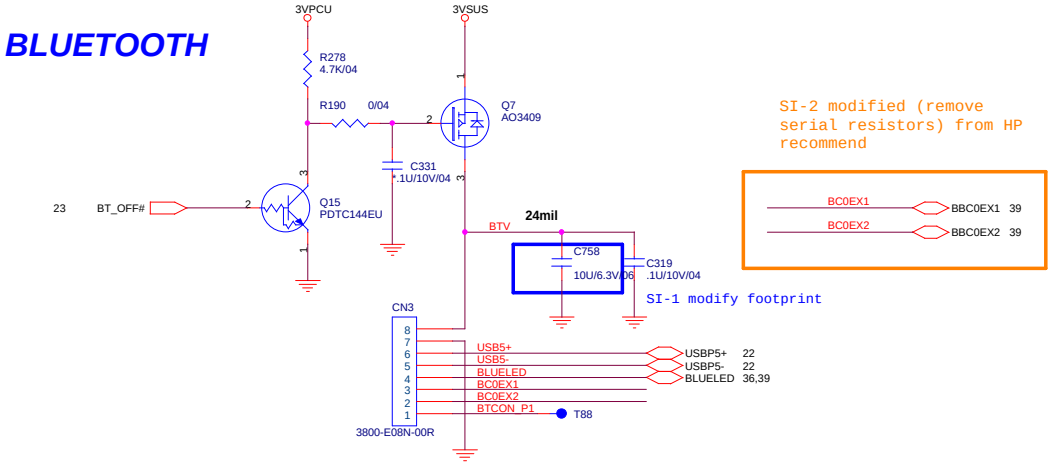
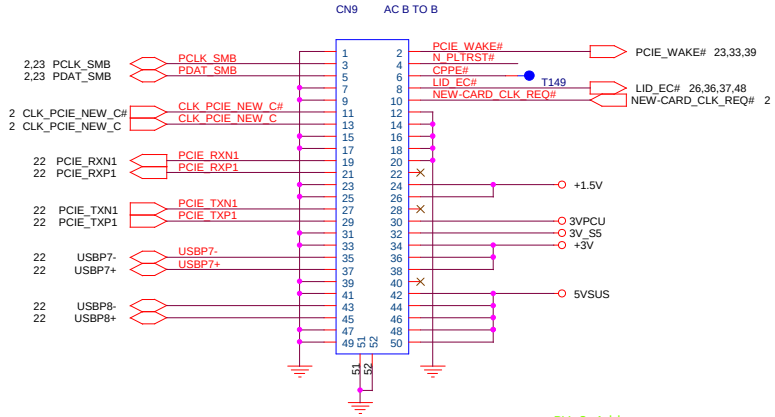
SATA_2 CONNECTOR
For 17"W Second HDD



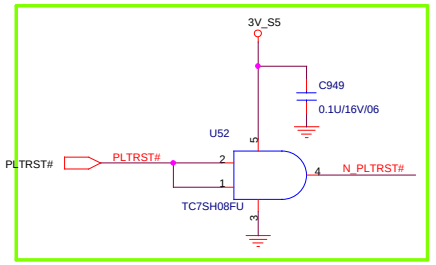
BLUETOOTH

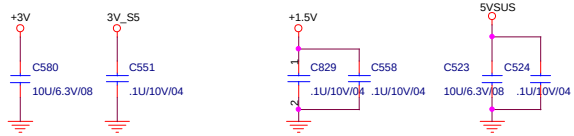


NEWCARD

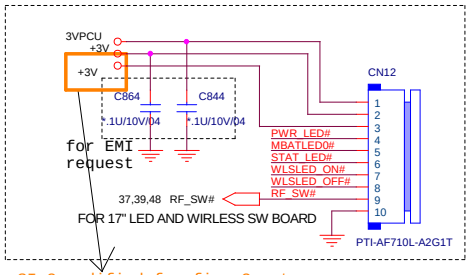


PV-2 Add

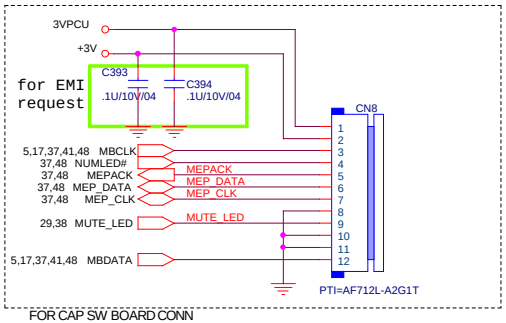


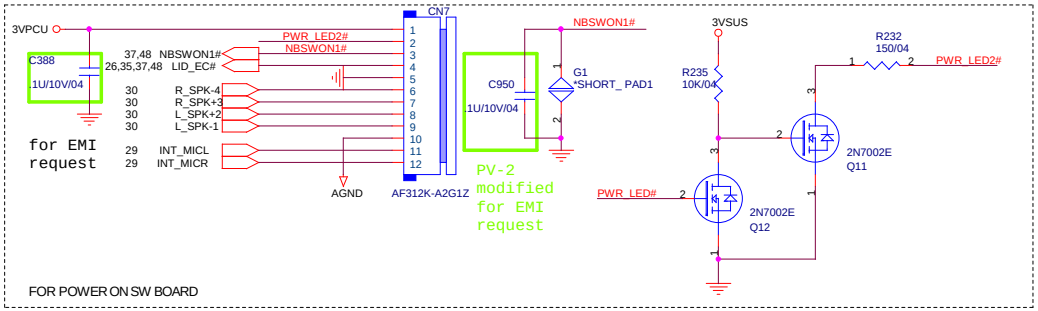


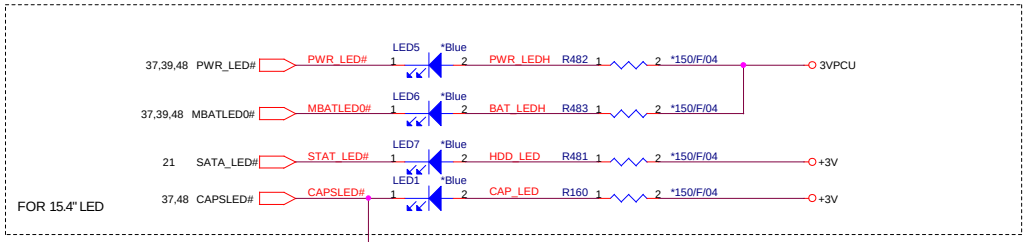
NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.	
Size: Custom	Document Number: NEW CARD/BT	Rev: 1A
Date: Monday, March 19, 2007	Sheet 35 of 48	

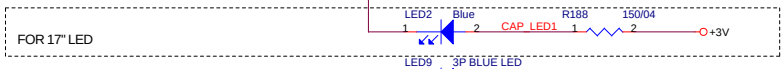


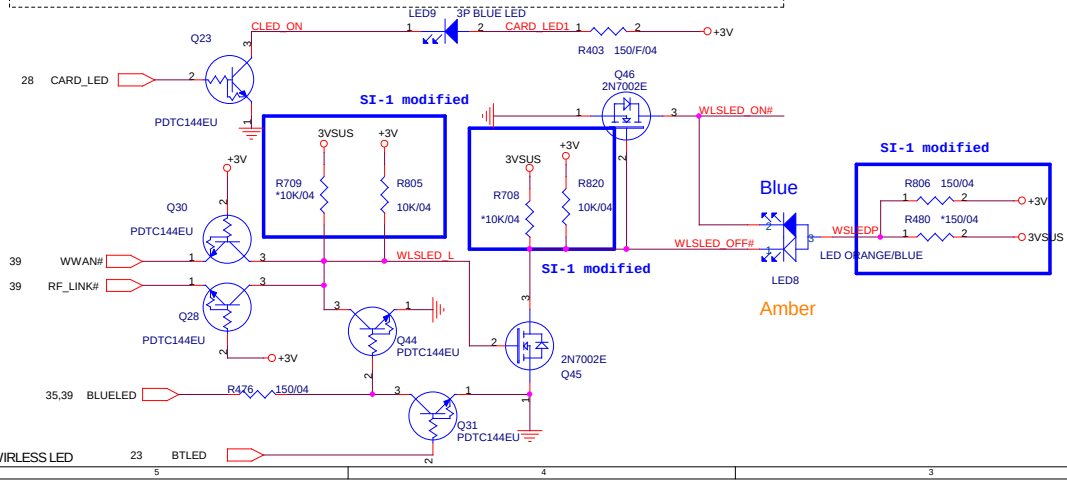
SI-2 modified for fix s3 not support wirless LED

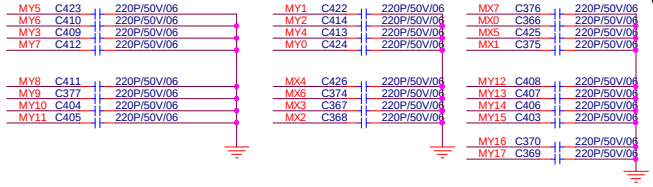




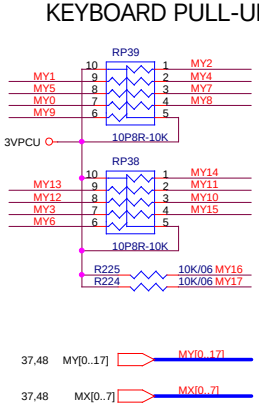


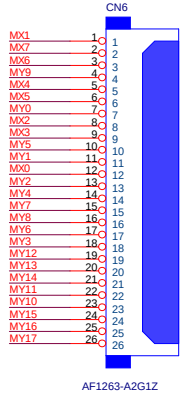


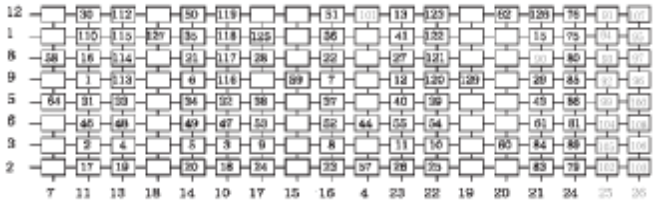




KEYBOARD PULL-UP







PROJECT :	AT5
Quanta Computer Inc.	
NB5/RD1/HW2	
Size: Custom	Document Number: LED/KEYBOARD/SW
Rev: 1A	
Date: Monday, March 19, 2007	Sheet 36 of 48

STRAP PIN

MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode

SI-1 DEL R209,R210,R218,R219,R220

MY2 R208 *10K/04

MY3 R212 *0/04

All hardware straps default internal pull-up, so don't need pull-UP outside. A TEST need try --andrew ????

SELECT KBC TPYE

PIN NAME	USE KBC3920	USE KBC3926
MY2	R208	REMOVE R208
BIOS_A0	REMOVE R808	R808

SI-2 modified remove ISA BIOS

TOUCH PAD CONNECTOR

for EMI request

close conn

SW1 MY7 MY4 *NTC031-AA1G-A160T FOR 15.4"

SW2 MY7 MY4 NTC031-AA1G-A160T FOR 17"

FOR 15.4"

FOR 17"

SI-1 modify (remove R245 and add R241)

SI-1 modify

SI-2 modified remove ISA BIOS

SI-2 modified remove ISA BIOS

SI-1 ADD

PV-2 Add

ICH8 has internal pull-up

1M byte SPI BIOS

PROJECT : AT5
Quanta Computer Inc.

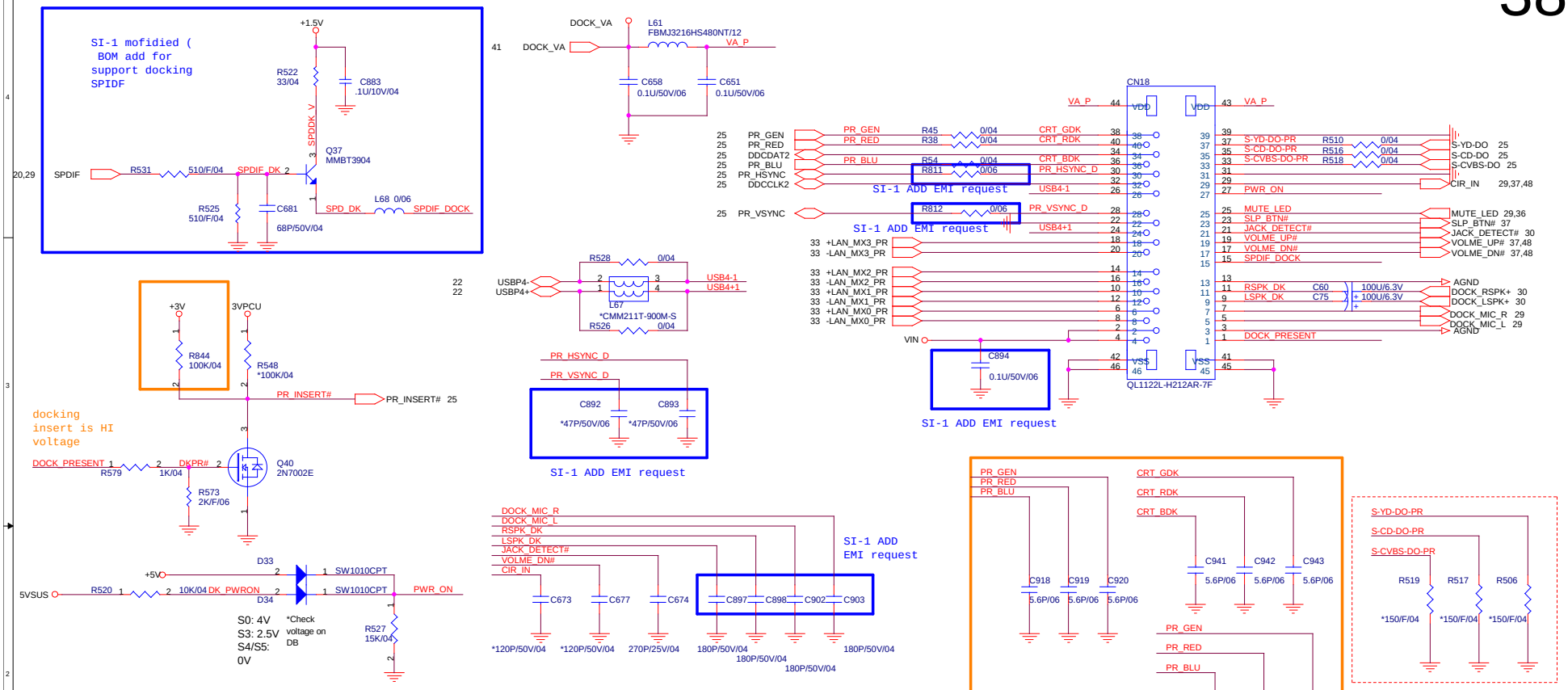
Size: Custom | Document Number: KB3920/ROM/TP | Rev: 1A

Date: Monday, March 19, 2007 | Sheet 37 of 48

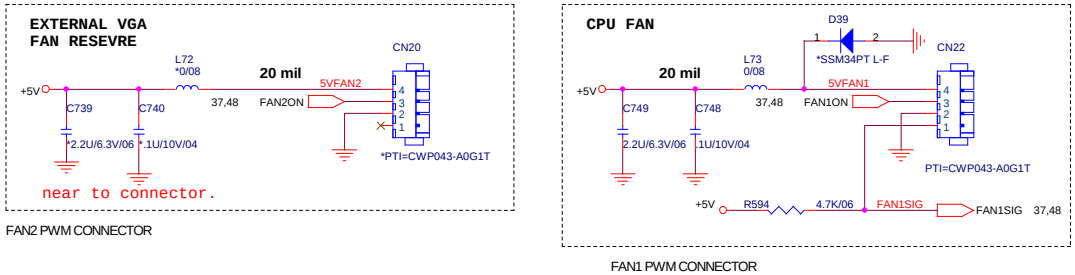
N85/RD1/HW2

CABLE DOCK

support 6A 200mils
CX000480005

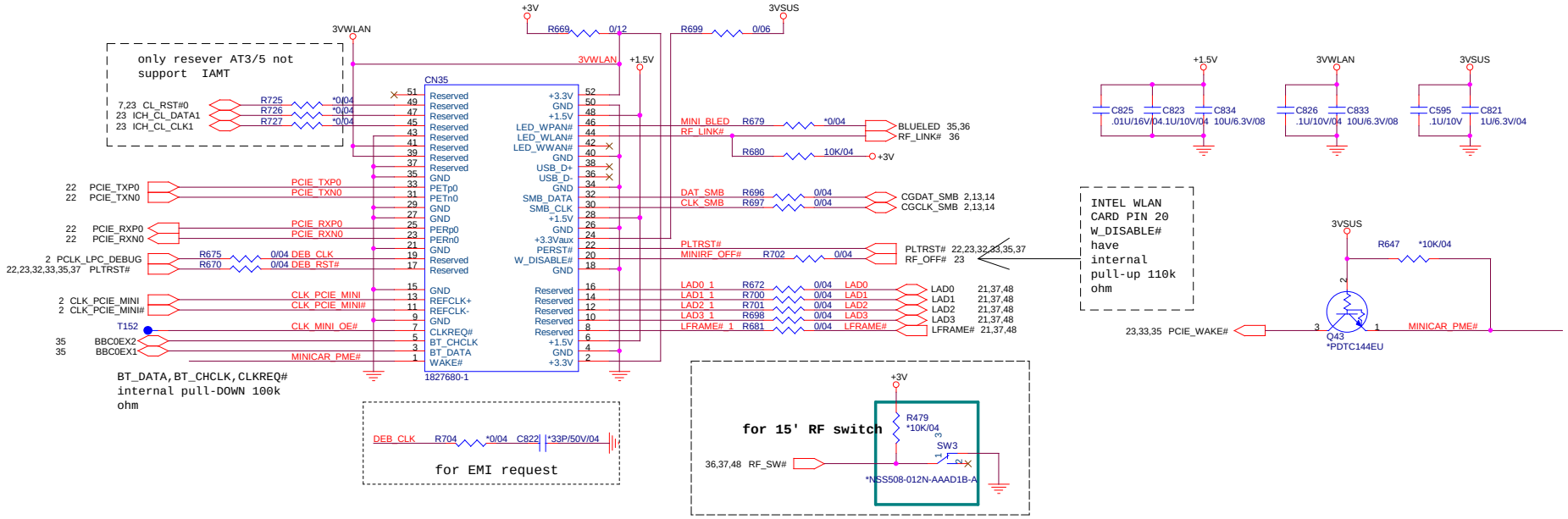


FAN



PROJECT : AT5 Quanta Computer Inc.		
NB5/RD1/HW2	Size: Custom Document Number: CABLE DOCKING/FAN	Rev: 1A
	Date: Monday, March 19, 2007	Sheet 38 of 48

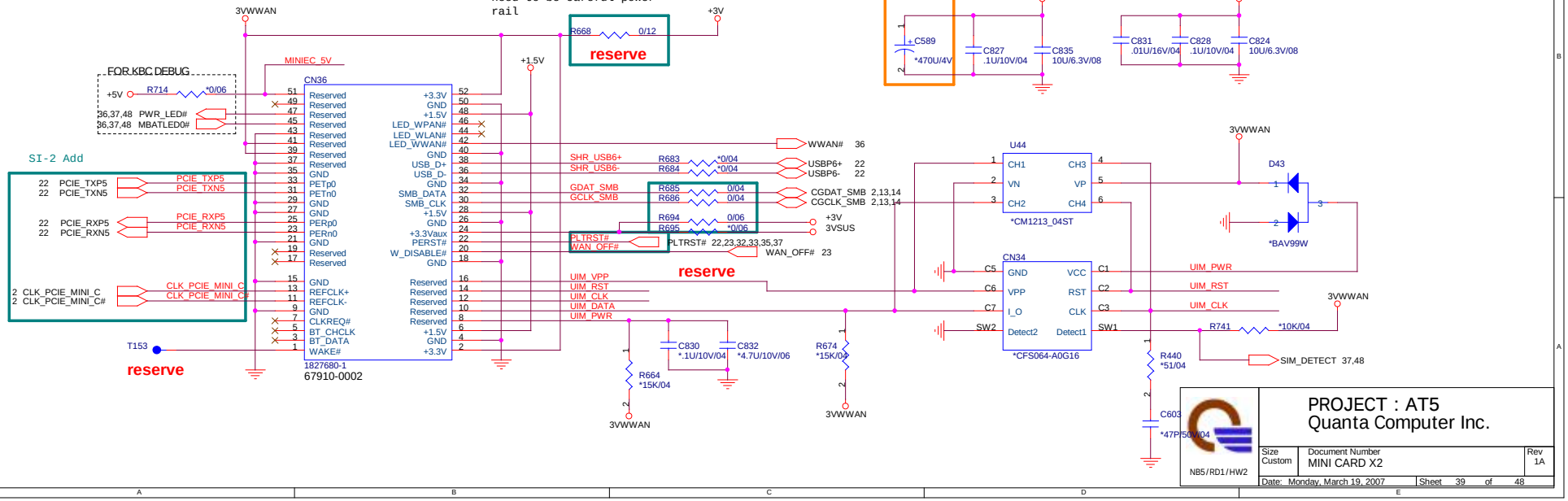
Mini PCI-E Card 1
WLAN



Mini PCI-E Card 2
WWAN(W/SIM)

WWAN -- have 2.8A 7W power consumption
power pin 24.39.41
GND pin 37,43
need to be careful power rail

SI-2 modified (BOM remove C589)

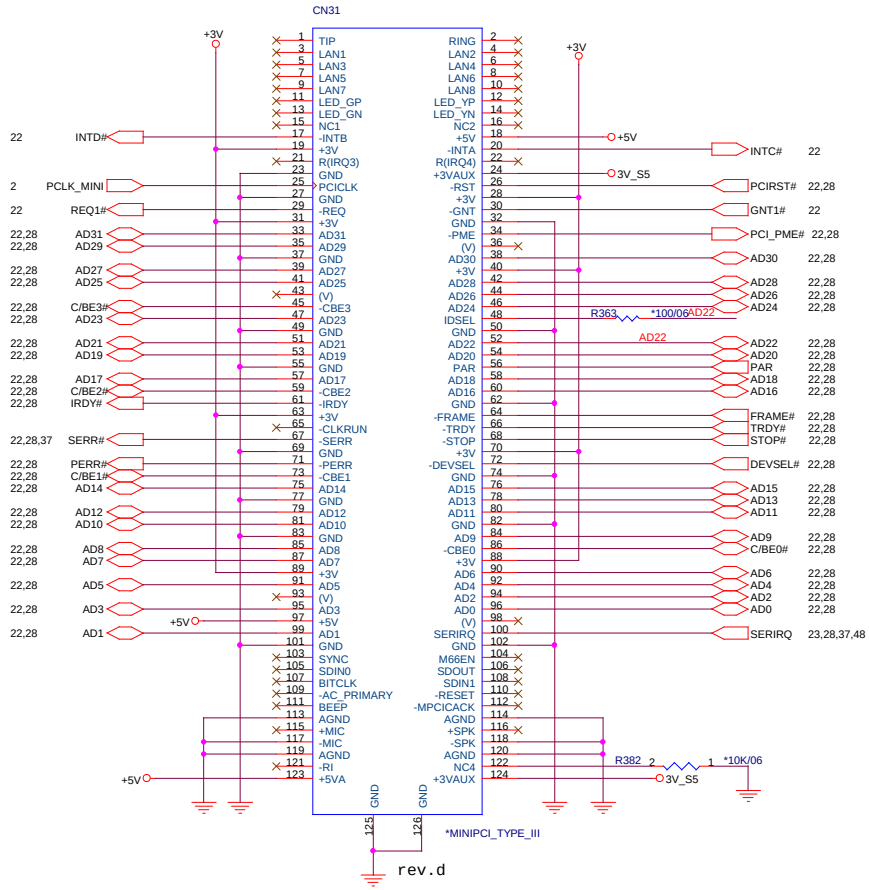


PROJECT : AT5 Quanta Computer Inc.			
Size: Custom	Document Number: MINI CARD X2		Rev: 1A
Date: Monday, March 19, 2007	Sheet 39 of 48		

NB5/RD1/HW2

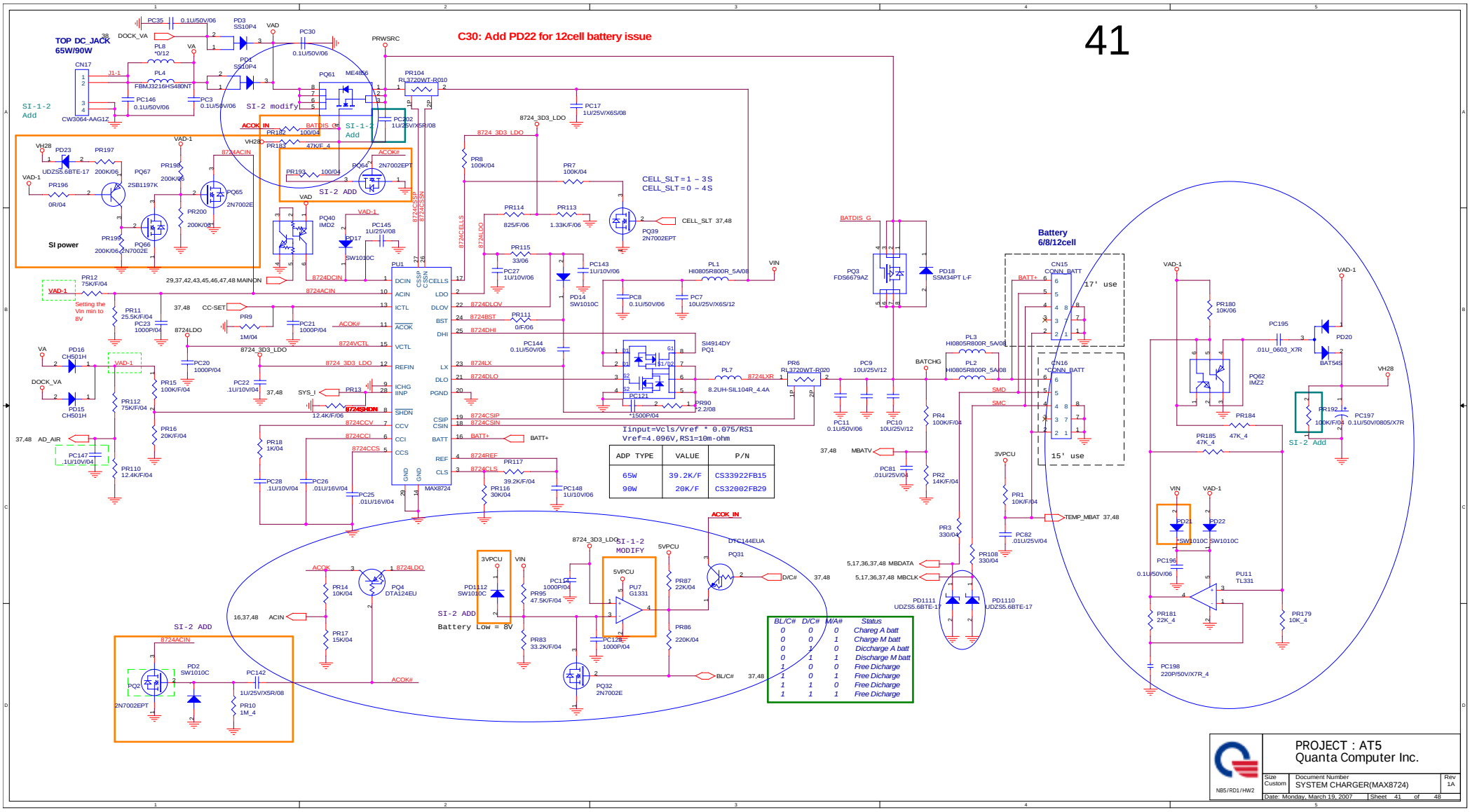
MINI PCI TYPE III SLOT

INTC#, INTD#
REQ1#/GNT1#
D_ID : AD22



PROJECT : AT5 Quanta Computer Inc.		
NB5/RD1/HW2	Size: Custom Document Number: MINI PCI TYPE III SLOT	Rev: 1A
	Date: Monday, March 19, 2007	Sheet 40 of 48

C30: Add PD22 for 12cell battery issue



ADP TYPE	VALUE	P/N
65W	39.2K/F	CS33922FB15
90W	20K/F	CS32002FB29

BL/C#	D/C#	M/A#	Status
0	0	0	Chareg A batt
0	0	1	Charge M batt
0	1	0	Diccharge A batt
0	1	1	Discharge M batt
1	0	0	Free Dicharge
1	0	1	Free Dicharge
1	1	0	Free Dicharge
1	1	1	Free Dicharge

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

5 Volt +/- 5%
Countinue current:8A
Peak current:11A
OCP minimum 13A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

Place these CAPs close to FETs

Place these CAPs close to FETs

Rds(on) 13m ohm

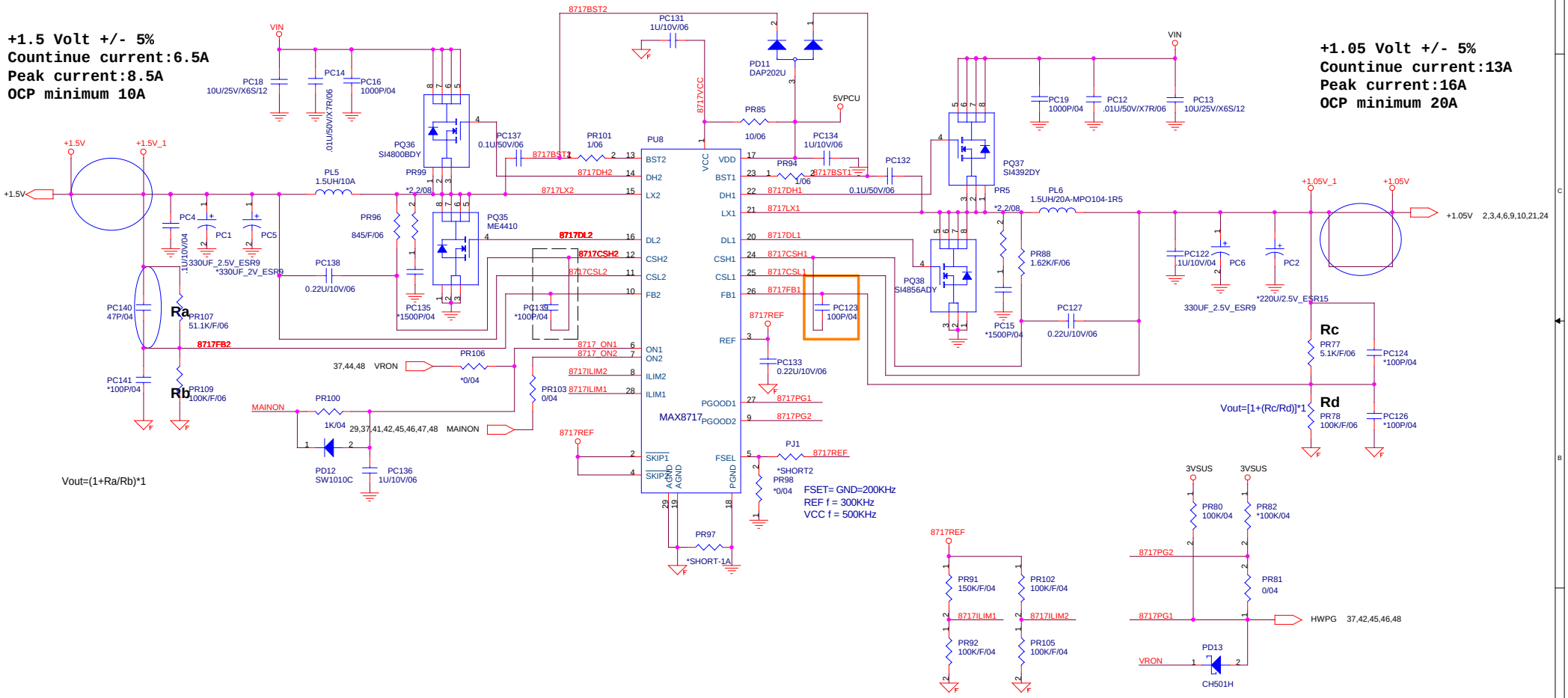
Rds(on) 15m ohm

Max Power Consumption 1.6W

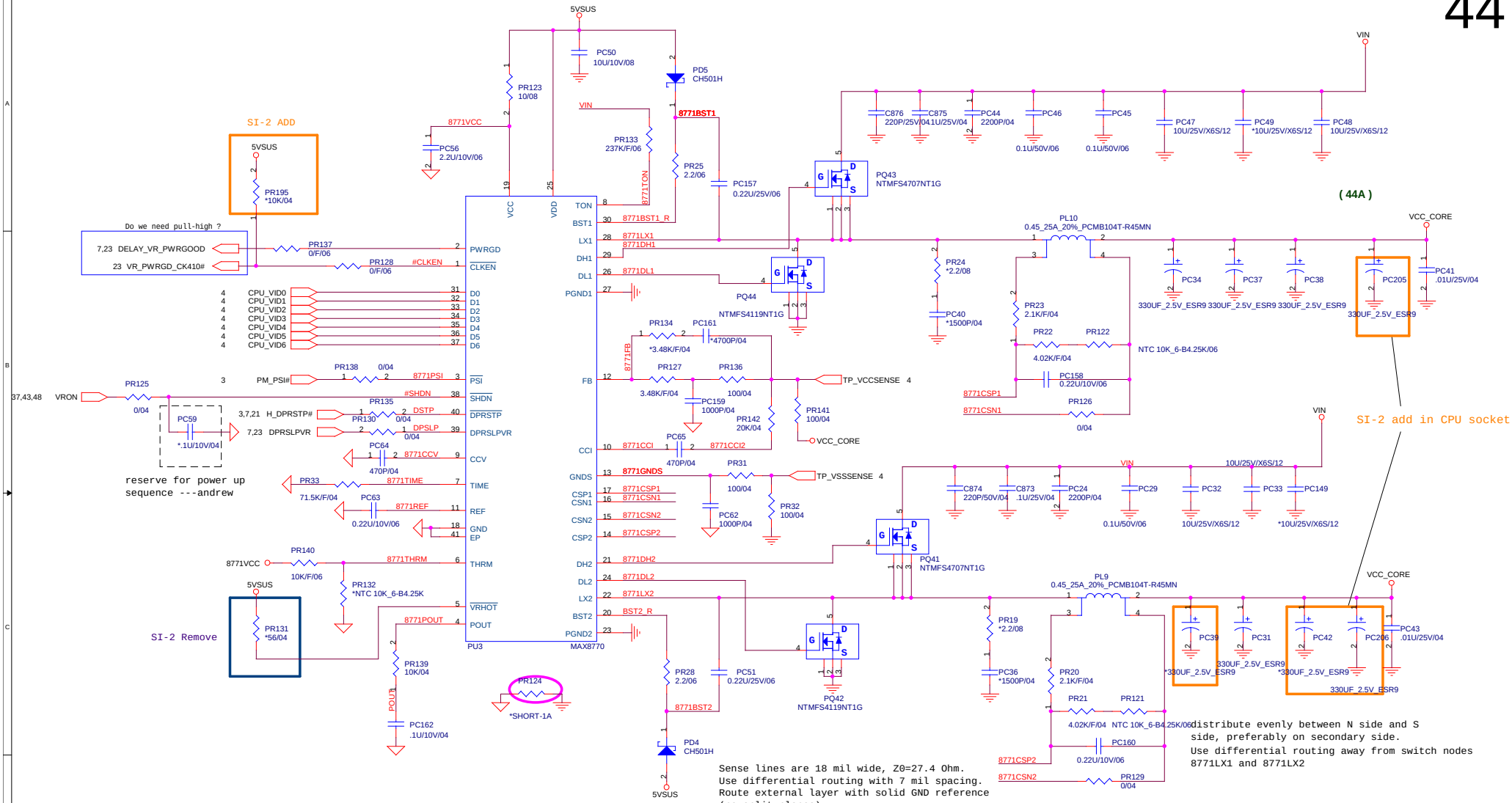
For G73 Only

SI-1 MODIFY

PROJECT : AT5	
Quanta Computer Inc.	
Size: Custom	Document Number: 3v/5v
Rev: 1A	
NB5/RD1/HW2	
Date: Monday, March 19, 2007	Sheet 42 of 48



NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.	
Size: Custom	Document Number: +-1.5V &VCCP+1.05V(MAX8743)	Rev: 1A
Date: Monday, March 19, 2007	Sheet 43 of 48	



PROJECT : AT5
Quanta Computer Inc.

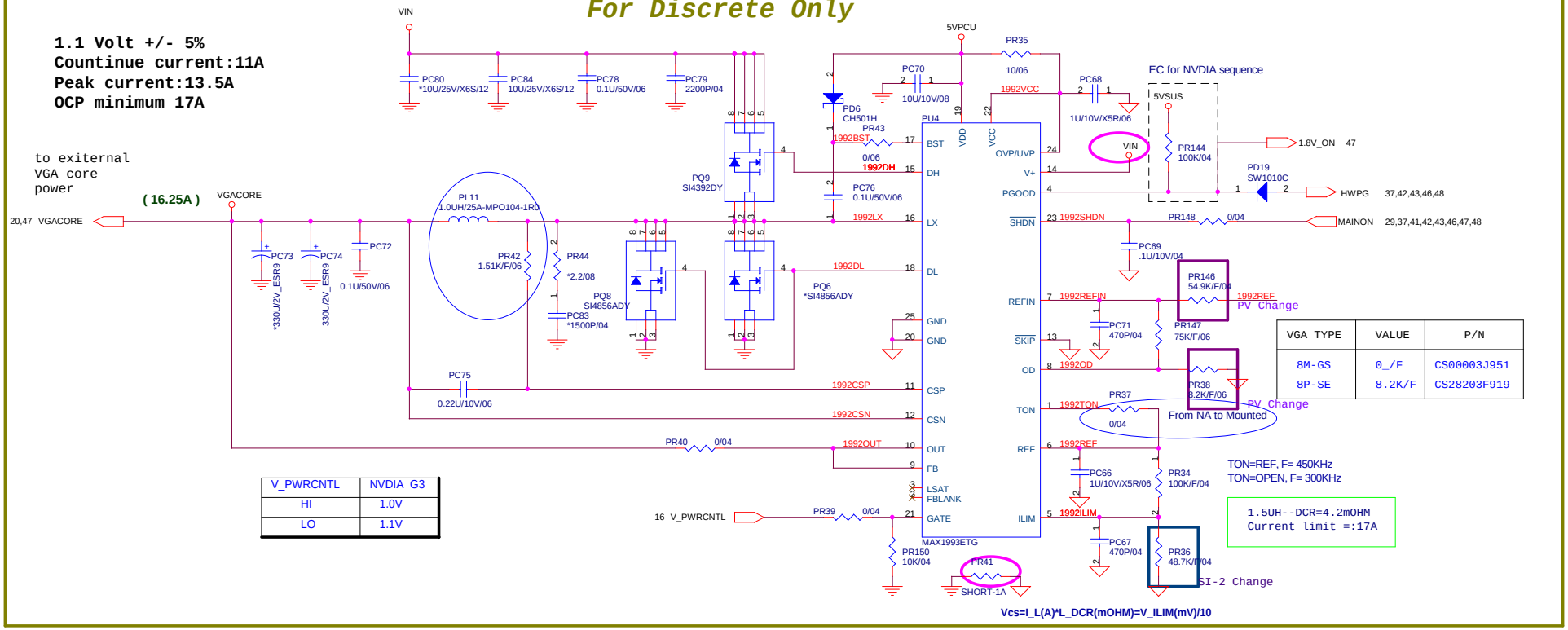
Size	Document Number	Rev
Custom	CPU_CORE(MAX8771)	1A

NB5/RD1/HW2

Date: Monday, March 19, 2007 | Sheet 44 of 48

For Discrete Only

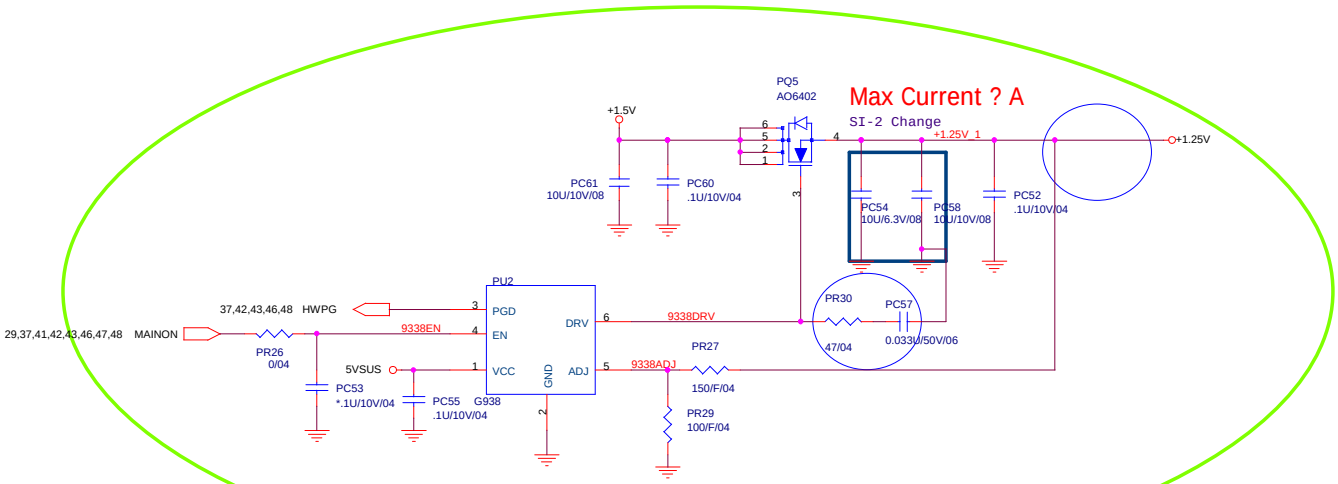
1.1 Volt +/- 5%
Countinue current:11A
Peak current:13.5A
OCP minimum 17A



V_PWRCNTL	NVDIA G3
HI	1.0V
LO	1.1V

VGA TYPE	VALUE	P/N
8M-GS	0_/F	CS00003J951
8P-SE	8.2K/F	CS28203F919

Vcs=I_L(A)*L_DCR(mOHM)=V_ILIM(mV)/10



Vout1=(1+R1/R2)*0.5

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Custom	VGACORE (MAX1993)	1A

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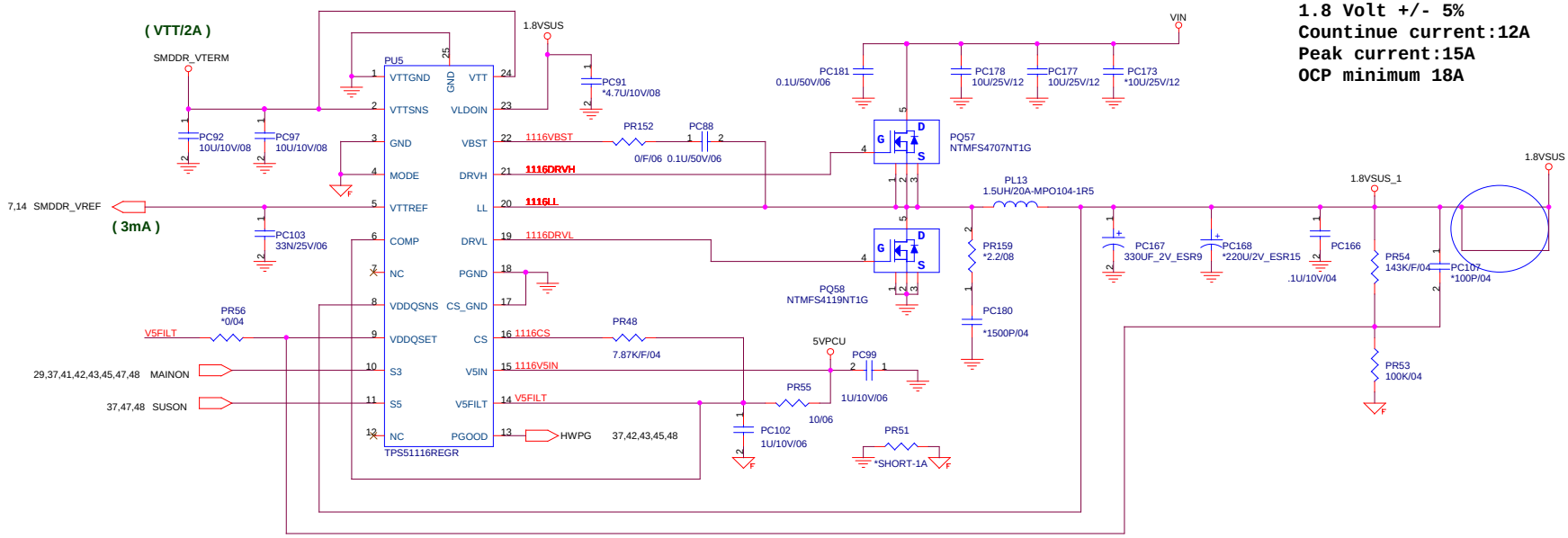
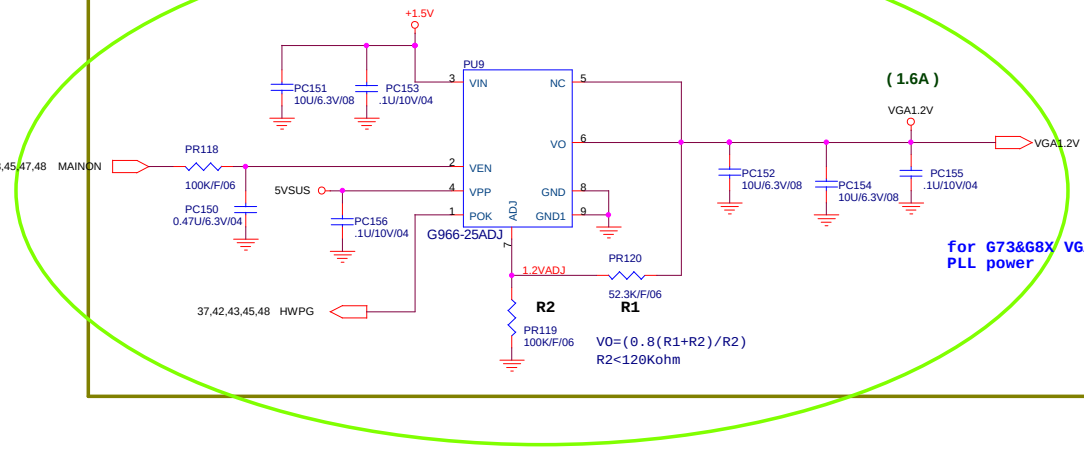
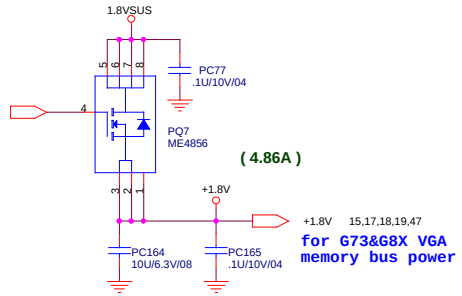


For Discrete Only





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Size: Custom	Document Number: DDRII 1.8VSUS/SMDDR_VTERM	Rev: 1A
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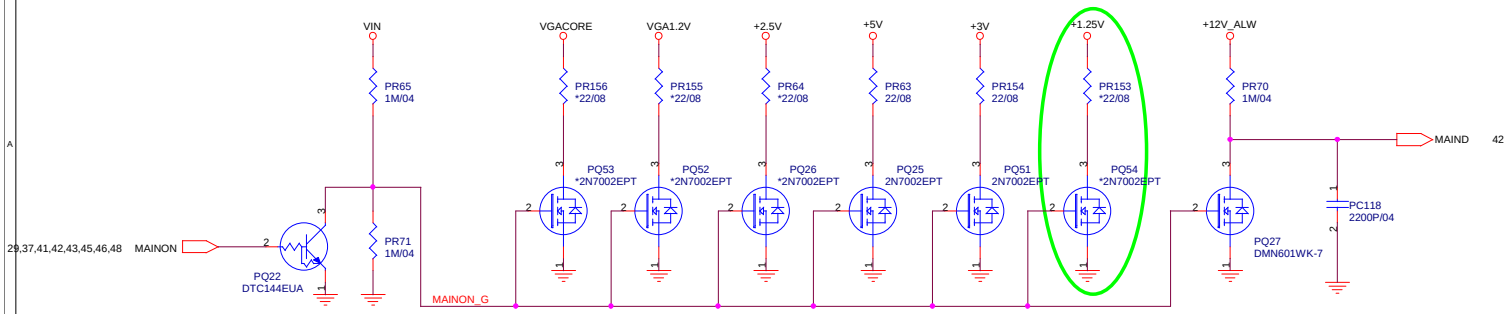
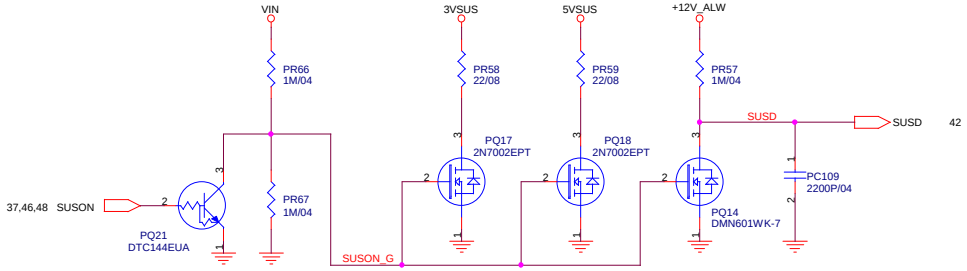
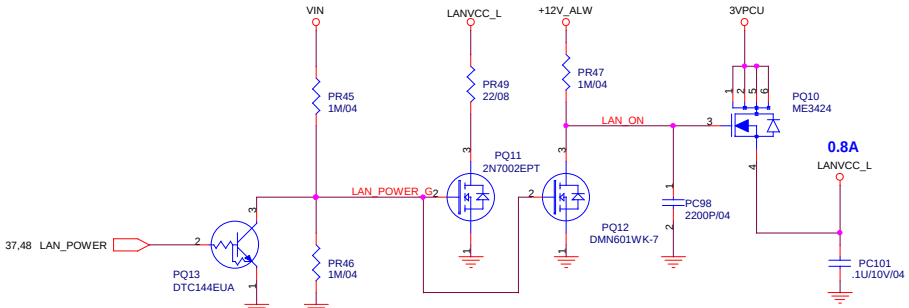
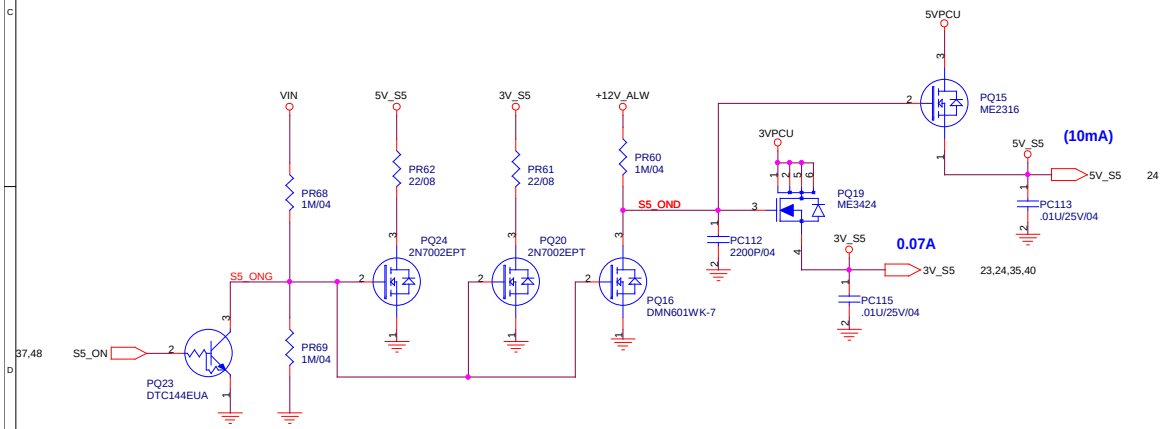
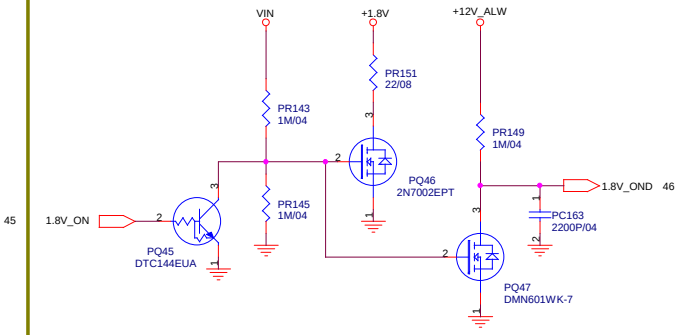








For Discrete Only



NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.	
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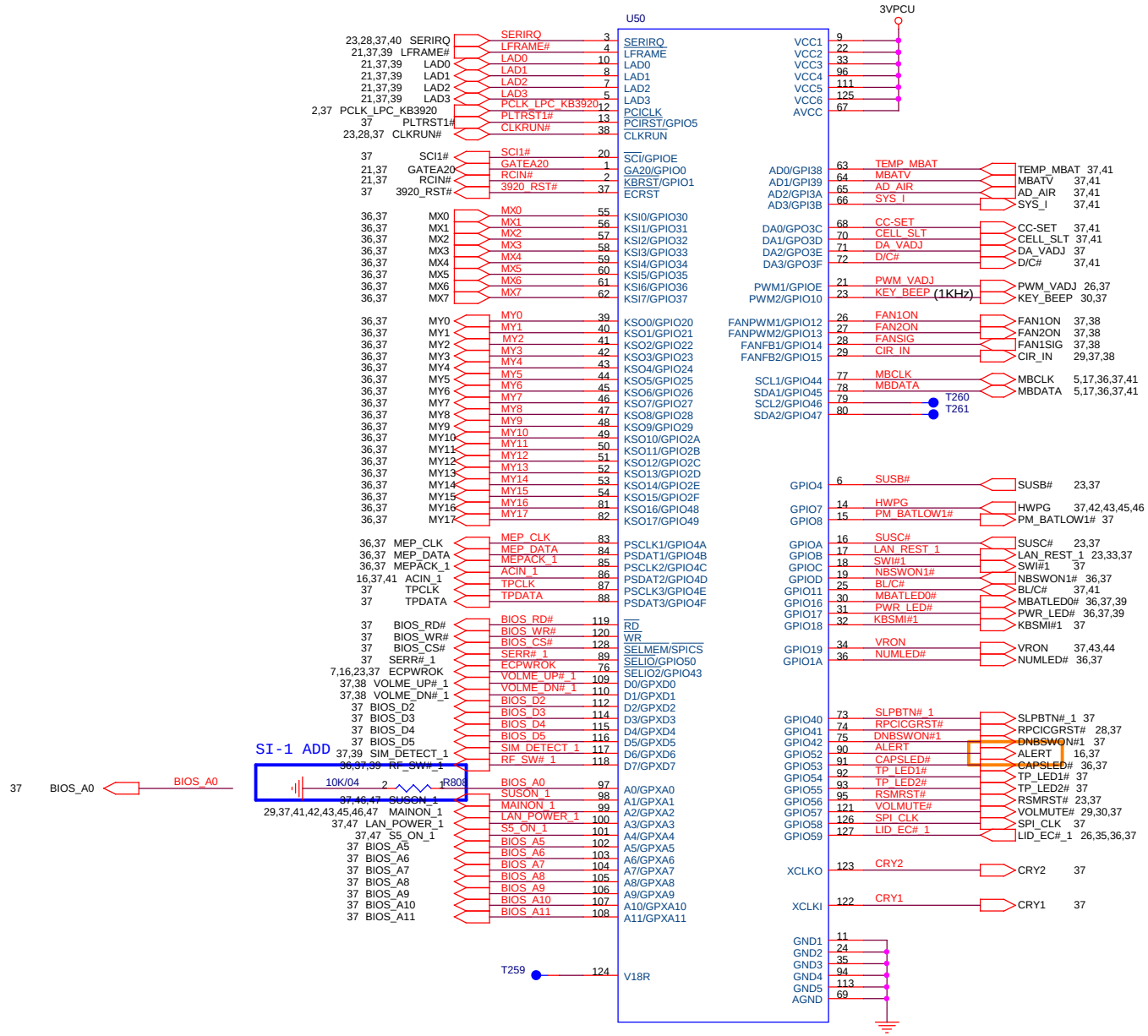
U50
3VPCU
SERIRQ
LFRAME#
LAD0
LAD1
LAD2
LAD3
PCLK_LPC_KB3920
PLTRST1#
CLKRUN#
SCI1#
GATEA20
RCIN#
3920_RST#
MX0
MX1
MX2
MX3
MX4
MX5
MX6
MX7
MY0
MY1
MY2
MY3
MY4
MY5
MY6
MY7
MY8
MY9
MY10
MY11
MY12
MY13
MY14
MY15
MY16
MY17
MEP_CLK
MEP_DATA
MEPACK_1
ACIN_1
TPCLK
TPDATA
BIOS_RD#
BIOS_WR#
BIOS_CS#
SERR#_1
ECPWROK
VOLME_UP#_1
VOLME_DN#_1
BIOS_D2
BIOS_D3
BIOS_D4
BIOS_D5
SIM_DETECT_1
RF_SW#_1
BIOS_A0
SUSON_1
MAINON_1
LAN_POWER_1
S5_ON_1
BIOS_A5
BIOS_A6
BIOS_A7
BIOS_A8
BIOS_A9
BIOS_A10
BIOS_A11
T259
V18R
SERIRQ
LFRAME
LAD0
LAD1
LAD2
LAD3
PCICLK
PCIRST/GPIO5
CLKRUN
SCI/GPIOE
GA20/GPIO0
KBRST/GPIO1
ECRST
KSI0/GPIO30
KSI1/GPIO31
KSI2/GPIO32
KSI3/GPIO33
KSI4/GPIO34
KSI5/GPIO35
KSI6/GPIO36
KSI7/GPIO37
KSO0/GPIO20
KSO1/GPIO21
KSO2/GPIO22
KSO3/GPIO23
KSO4/GPIO24
KSO5/GPIO25
KSO6/GPIO26
KSO7/GPIO27
KSO8/GPIO28
KSO9/GPIO29
KSO10/GPIO2A
KSO11/GPIO2B
KSO12/GPIO2C
KSO13/GPIO2D
KSO14/GPIO2E
KSO15/GPIO2F
KSO16/GPIO48
KSO17/GPIO49
PSCLK1/GPIO4A
PSDAT1/GPIO4B
PSCLK2/GPIO4C
PSDAT2/GPIO4D
PSCLK3/GPIO4E
PSDAT3/GPIO4F
RD
WR
SELMEM/SPICS
SELIO/GPIO50
SELIO2/GPIO43
D0/GPXD0
D1/GPXD1
D2/GPXD2
D3/GPXD3
D4/GPXD4
D5/GPXD5
D6/GPXD6
D7/GPXD7
A0/GPXA0
A1/GPXA1
A2/GPXA2
A3/GPXA3
A4/GPXA4
A5/GPXA5
A6/GPXA6
A7/GPXA7
A8/GPXA8
A9/GPXA9
A10/GPXA10
A11/GPXA11
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
AVCC
AD0/GPI38
AD1/GPI39
AD2/GPI3A
AD3/GPI3B
DA0/GPO3C
DA1/GPO3D
DA2/GPO3E
DA3/GPO3F
PWM1/GPIOE
PWM2/GPIO10
FANPWM1/GPIO12
FANPWM2/GPIO13
FANFB1/GPIO14
FANFB2/GPIO15
SCL1/GPIO44
SDA1/GPIO45
SCL2/GPIO46
SDA2/GPIO47
GPIO4
GPIO7
GPIO8
GPIOA
GPIOB
GPIOC
GPIOD
GPIO11
GPIO16
GPIO17
GPIO18
GPIO19
GPIO1A
GPIO40
GPIO41
GPIO42
GPIO52
GPIO53
GPIO54
GPIO55
GPIO56
GPIO57
GPIO58
GPIO59
XCLKO
XCLKI
GND1
GND2
GND3
GND4
GND5
AGND
TEMP_MBAT
MBATV
AD_AIR
SYS_I
CC-SET
CELL_SLT
DA_VADJ
D/C#
PWM_VADJ
KEY_BEEP (1KHz)
FAN1ON
FAN2ON
FANSIG
CIR_IN
MBCLK
MBDATA
T260
T261
SUSB#
HWPG
PM_BATLOW1#
SUSC#
LAN_REST_1
SWI#1
NBSWON1#
BL/C#
MBATLED0#
PWR_LED#
KBSMI#1
VRON
NUMLED#
SLPBTN#_1
RPCICGRST#
DNBSWON#1
ALERT
CAPSLED#
TP_LED1#
TP_LED2#
RSMRST#
VOLMUTE#
SPI_CLK
LID_EC#_1
CRY2
CRY1
SI-1 ADD
10K/04
R808
KB3926
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Quanta Computer Inc.
NB5/RD1/HW2
Size B
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KB3926
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