UT6 BLOCK DIAGRAM

01

PCB STACK UP

8L

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : SVCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT

Cable Docking PAGE 38
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

- SYSTEM CHARGER ISL6251AHAZ-T PAGE 39
- SYSTEM POWER ISL6237IRZ-T PAGE 40
- DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAGE 44
- VCCP +1.5V AND GMCH 1.05V(RT8204) PAGE 44
- VGACORE(1.025V)Oz8118 PAGE 43
- CPU CORE ISL6266A PAGE 42

CPU Penryn
478P (uPGA)/35W
PAGE 3,4

CPU THERMAL SENSOR PAGE 4

FSB 667/800/1066

14.318MHz

CLOCK GEN
ALPRS355B MLF64PIN
PAGE 2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

NORTH BRIDGE
Cantiga
PM45,GM45
PAGE 5~9

UMA only

PS8101 PAGE 20

27MHz

nVIDIA
NB9P-GS 128 Bit
PAGE 12~18
969p

PCI-Express 16X

Dual Link

HDMI CON PAGE 20

CRT PAGE 20

LCD CONN PAGE 19

DDRII-SODIMM0 PAGE 10,11
DDRII-SODIMM1 PAGE 10,11
DDRIII 667/800 MHz

DMI LINK

32.768KHz

NBSRCCLK, NBSRCCLK#

SOUTH BRIDGE
ICH9-M
PAGE 21,22,23,24

SATA - HDD PAGE 34 — SATA0 150MB
SATA - CD-ROM PAGE 34 — SATA1 150MB
SATA - 2ndHDD PAGE 30 — SATA4 150MB
E-SATA PAGE 31 — SATA5 150MB
Accelerometer LIS302DL PAGE 28 — SMBUS

USB2.0

0,1,8,9 — **USB2.0 Ports X4** PAGE 31
5 — **BlueTooth** PAGE 31
3 — **Webcam** PAGE 31
2 — **Fingerprint** PAGE 31
4,7,10,11 — **Mini PCI-E Card x2**
Express Card x1
Cable Docking x1

PCI-E

24.576Hz

Azalia

Analog
IDT92HD71B7
PAGE 27

X3 — **Mini PCI-e Card** (Wireless LAN) (TV) (ROBSON) PAGE 37

X1 — **LAN** Realtek PCIE-LAN RTL 8111C (GagaLAN) PAGE 32,33

25MHz

X1 — **Express Card** (NEW CARD) PAGE 34

X1 — **JMICRO 380 for Discrete** PAGE 26

IEEE1394 connect for Discrete only PAGE 26

Memory CardReader PAGE 25

LPC

32.768KHz

ENE KBC
KB3926 C0
PAGE 35

Keyboard Touch Pad PAGE 36

Capacitive Sense SW PAGE 36

HDCP SPI for UMA PAGE 22

AUDIO Amplifier TPA6020A2 PAGE 28

AUDIO Amplifier TPA3007D1 PAGE 29

RJ45 PAGE 32

microphone PAGE 27

Audio Jacks (Phone/ MIC) PAGE 27

Jack to Speaker PAGE 28

Jack to Sub-Woofer PAGE 29

GMT G9931P1U
FAN PAGE 38

BIOS SPI PAGE 35

NB5

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	E3A

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[4,6,9,10,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +3V
[3,4,5,6,8,9,21,24,36,41] +1.05V

Delete RP49 for delete ITP conn.

07/09 (PV2) Del RP53, add TP96,TP97 for no support ROBSON card.

7/16 (PV2) Change FP for ICT.
For Vender suggest

07/14 (PV2) Change footprint for PE require.

0=overclocking of CPU and SRC Allowed
1 = overclocking of CPU and SRC not Allowed

0=UMA
1 = External VGA

Enable ITP CLK

05/14 (PV) FOR BOM modify

SI modified
C400,C409 change to 27p

27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

CK505 QFN64

ICS	ICS9LPRS355BKLF	ALPRS355000
Silego	SLG8SP513VTR	AL8SP513000
Realtek	RTM875N-606-VD-GR	AL000875000

For Vender suggest

QT6 modified-0117

CPU Clock select

7/16 (PV2) Change FP for ICT.

1K to NB only when XDP is implement.No XDP can use 0 ohm

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

for EMI

PROJECT : UT6
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Clock Generator	E3A

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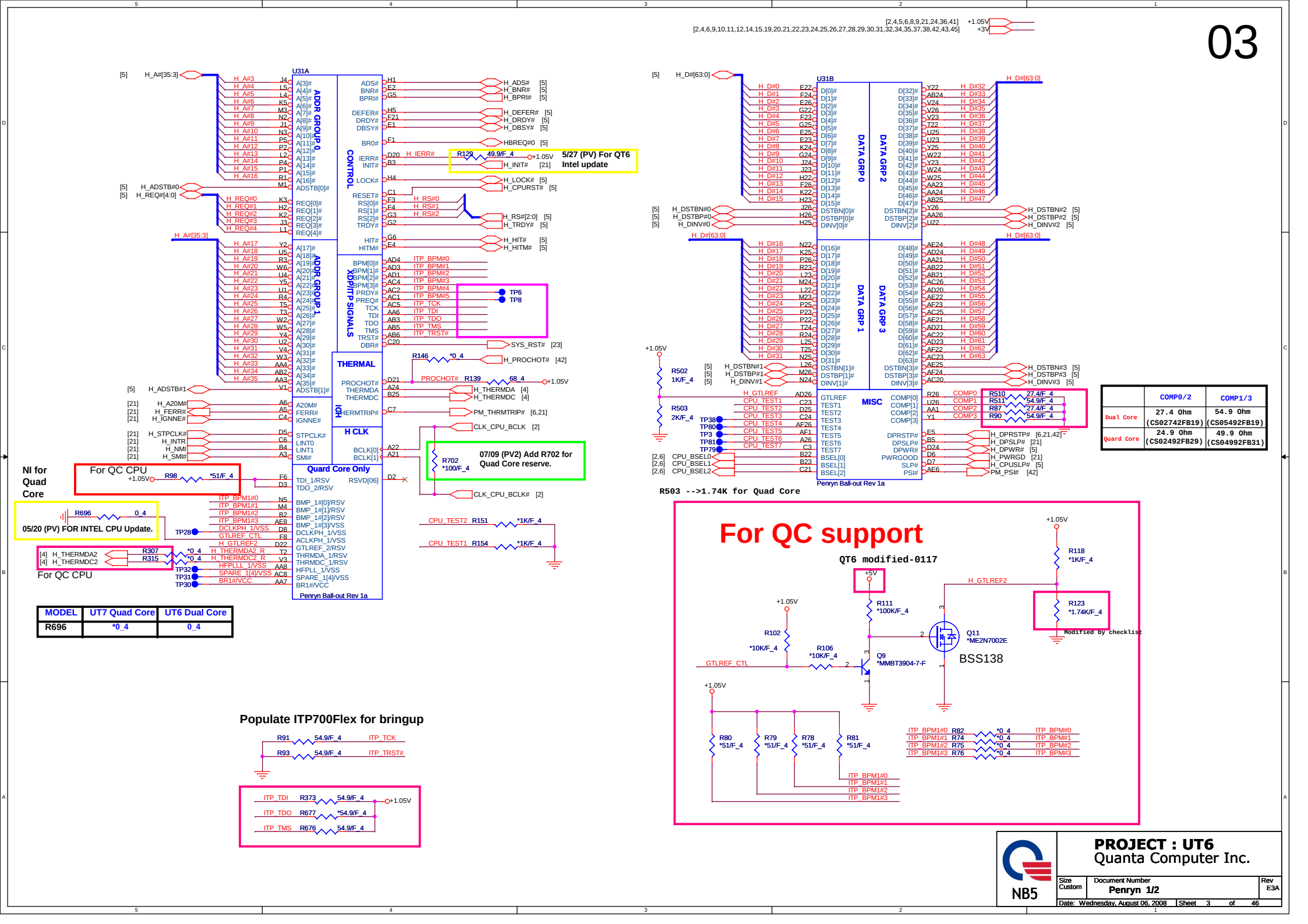


MODEL	UT7 Quad Core	UT6 Dual Core
R696	*0_4	0_4

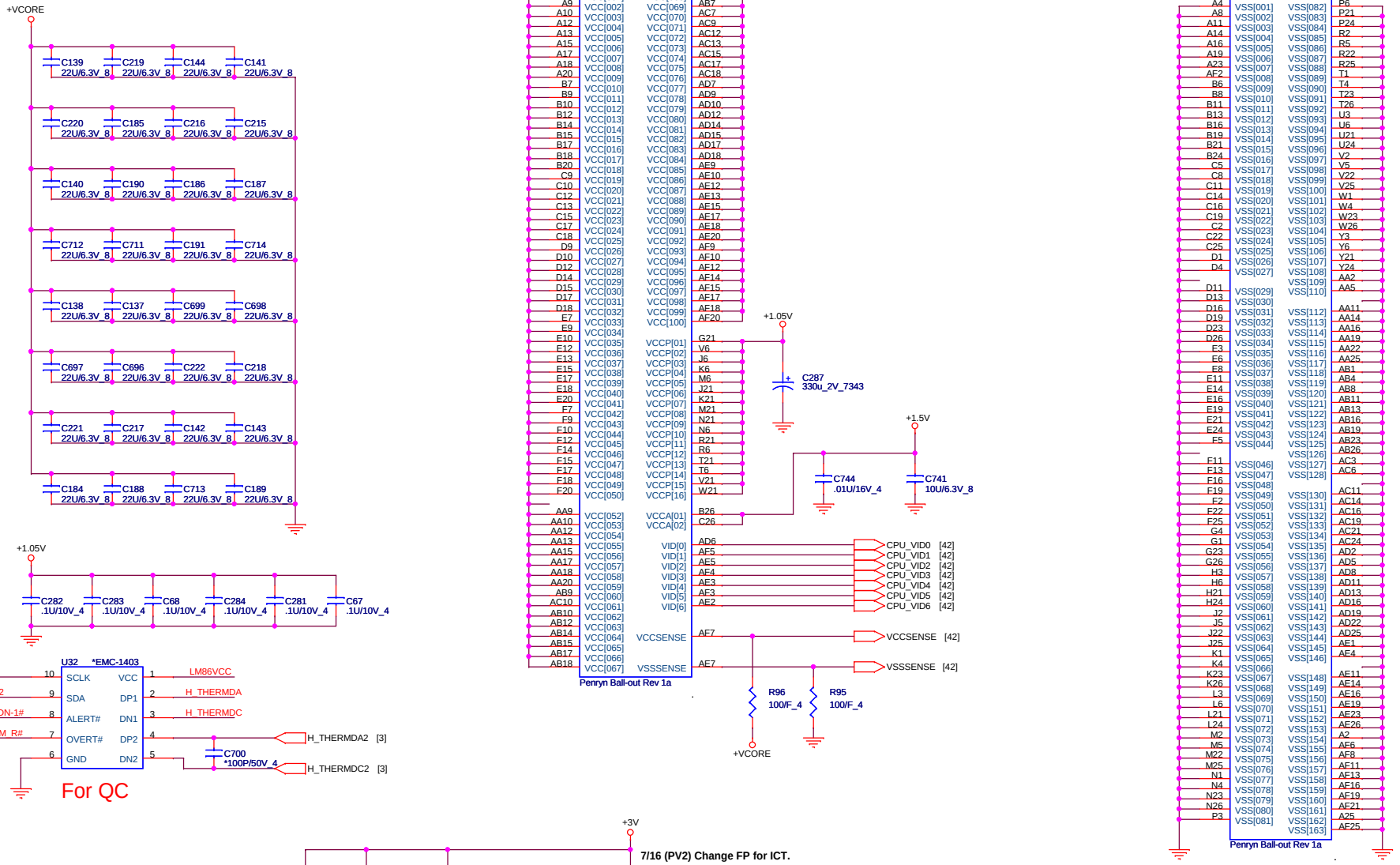
	COMP0/2	COMP1/3
Dual Core	27.4 Ohm (CS02742FB19)	54.9 Ohm (CS05492FB19)
Quard Core	24.9 Ohm (CS02492FB29)	49.9 Ohm (CS04992FB31)

PROJECT : UT6
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Penryn 1/2	E3A

Date: Wednesday, August 06, 2008 Sheet 3 of 46



NB5

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Penryn & TH Monitor 2/2	E3A

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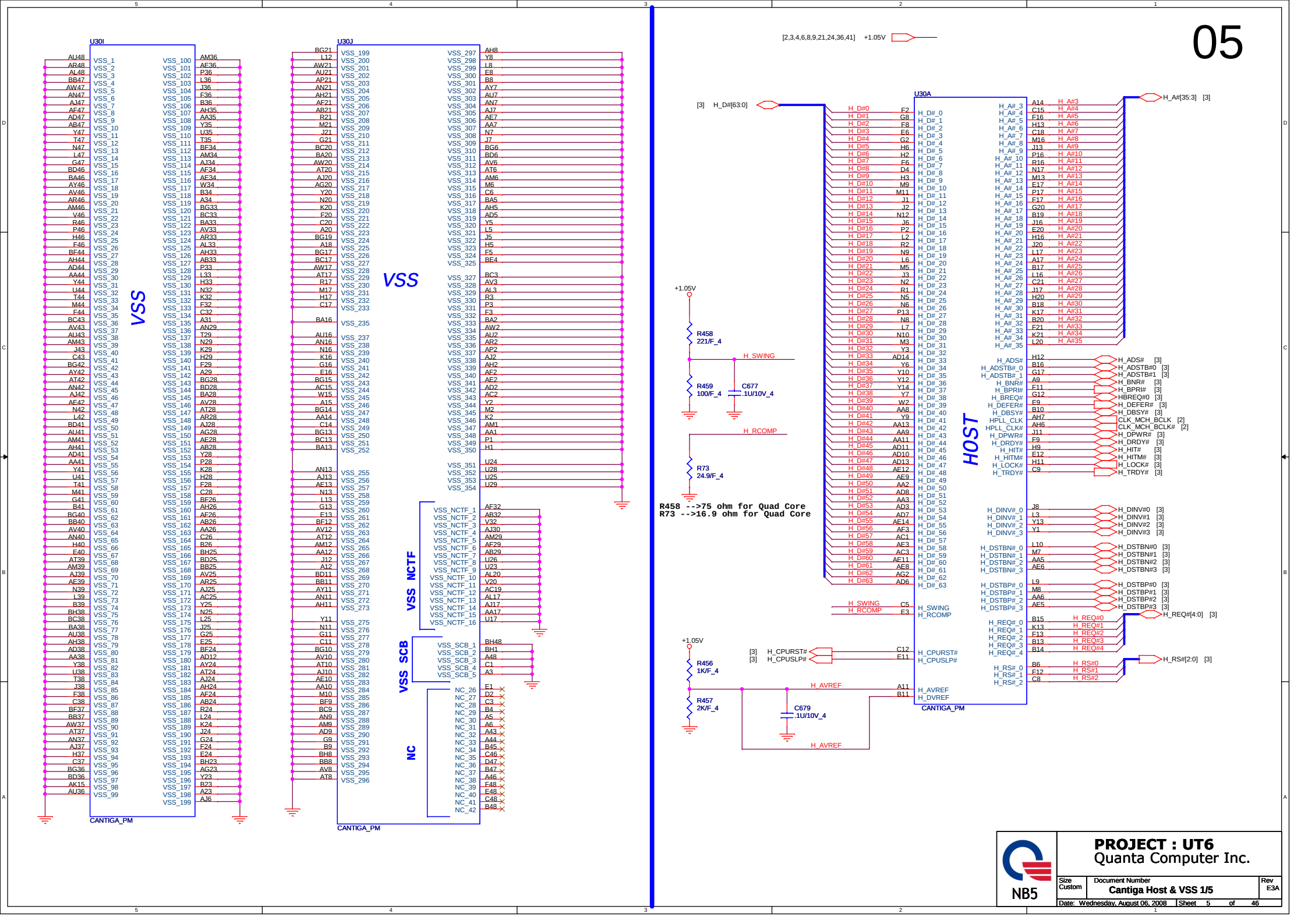
05
U30I
VSS
U30J
VSS
VSS_NCTF
VSS_SCB
NC
U30A
HOST
[2,3,4,6,8,9,21,24,36,41] +1.05V
[3] H_D#[63:0]
H_A#[35:3] [3]
+1.05V
R458
221/F_4
H_SWING
R459
100/F_4
C677
.1U/10V_4
H_RCOMP
R73
24.9/F_4
R458 -->75 ohm for Quad Core
R73 -->16.9 ohm for Quad Core
+1.05V
R456
1K/F_4
R457
2K/F_4
H_AVREF
C679
.1U/10V_4
[3] H_CPURST#
[3] H_CPUSLP#
H_ADS# [3]
H_ADSTB#0 [3]
H_ADSTB#1 [3]
H_BNR# [3]
H_BPRI# [3]
HBREQ#0 [3]
H_DEFER# [3]
H_DBSY# [3]
CLK_MCH_BCLK [2]
CLK_MCH_BCLK# [2]
H_DPWR# [3]
H_DRDY# [3]
H_HIT# [3]
H_HITM# [3]
H_LOCK# [3]
H_TRDY# [3]
H_DINV#0 [3]
H_DINV#1 [3]
H_DINV#2 [3]
H_DINV#3 [3]
H_DSTBN#0 [3]
H_DSTBN#1 [3]
H_DSTBN#2 [3]
H_DSTBN#3 [3]
H_DSTBP#0 [3]
H_DSTBP#1 [3]
H_DSTBP#2 [3]
H_DSTBP#3 [3]
H_REQ#[4:0] [3]
H_RS#[2:0] [3]
CANTIGA_PM
PROJECT : UT6
Quanta Computer Inc.
NB5
Size Custom
Document Number
Cantiga Host & VSS 1/5
Rev E3A
Date: Wednesday, August 06, 2008
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MCH_CFG_5 DMIx2 selection
Low = DMI X2
High = DMI X4 (Default)

MCH_CFG_16 FSB Dynamic ODT
Low = Dynamic ODT disabled
High = Dynamic ODT enabled (default)

MCH_CFG_9 PCI Express Graphic Lane
Low: Reverse Lane
High: Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal
Low = Normal operation (Default)
High = Reverse Lanes

MCH_CFG_6 iTPM Host Interface
Low =The iTPM Host Interface is enabled2
High = The iTPM Host Interface is disabled (default)

MCH_CFG_7 Intel (R) Management Engine Crypto
Low: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable
Low = Enabled3
High: Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13	MCH_CFG_12	Configuration
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

MCH_CFG_20

Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE
Low = Only digital display port (SDVO/DP/iHDMI) or PCIE is operational (default)

High = Digital display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via the PEG port

MCH_CFG2:0

000 = FSB1066
010 = FSB800
011 = FSB667
Others = Reserved

U30B

RSVD: RSVD1 M36, RSVD2 N36, RSVD3 R33, RSVD4 T33, RSVD5 AH9, RSVD6 AH10, RSVD7 AH12, RSVD8 AH13, RSVD9 K12, RSVD14 T24, RSVD15 B31, RSVD16 B2, RSVD17 M1, RSVD20 AY21, RSVD22 BG23, RSVD23 BF23, RSVD24 BH18, RSVD25 BF18

DDR CLK/ CONTROL/COMPENSATION: SA_CK_0 AP24, SA_CK_1 AT21, SB_CK_0 AV24, SB_CK_1 AU20, SA_CK#_0 AR24, SA_CK#_1 AR21, SB_CK#_0 AU24, SB_CK#_1 AV20, SA_CKE_0 BC28, SA_CKE_1 AY28, SB_CKE_0 AY36, SB_CKE_1 BB36, SA_CS#_0 BA17, SA_CS#_1 AY16, SB_CS#_0 AV16, SB_CS#_1 AR13, SA_ODT_0 BD17, SA_ODT_1 AY17, SB_ODT_0 BF15, SB_ODT_1 AY13, SM_RCOMP BG22 R153 80.6/F_4, SM_RCOMP# BH21 R152 80.6/F_4, SM_RCOMP_VOH BF28, SM_RCOMP_VOL BH28, SM_VREF AV42 +0.9VSMVREF_MCH, SM_PWROK AR36 SW_PWROK_NB R112 10K/F_4, SM_REXT BF17 R134 499/F_4, SM_DRAMRST# BC36 TP_SM_DRAMRST# TP37

CLK: DPLL_REF_CLK B38 DREFCLK [2], DPLL_REF_CLK# A38 DREFCLK# [2], DPLL_REF_SSCLK E41 DREFSSCLK [2], DPLL_REF_SSCLK# F41 DREFSSCLK# [2], PEG_CLK F43 CLK_PCIE_3GPLL [2], PEG_CLK# E43 CLK_PCIE_3GPLL# [2]

ME JTAG: TP34 AL34 ME_JTAG_TCK, TP33 AK34 ME_JTAG_TDI, TP36 AN35 ME_JTAG_TDO, TP35 AM35 ME_JTAG_TMS

DMI: DMI_RXN_0 AE41 DMI_TXN0, DMI_RXN_1 AE37 DMI_TXN1, DMI_RXN_2 AE47 DMI_TXN2, DMI_RXN_3 AH39 DMI_TXN3 → DMI_TXN[3:0] [22]; DMI_RXP_0 AE40 DMI_TXP0, DMI_RXP_1 AE38 DMI_TXP1, DMI_RXP_2 AE48 DMI_TXP2, DMI_RXP_3 AH40 DMI_TXP3 → DMI_TXP[3:0] [22]; DMI_TXN_0 AE35 DMI_RXN0, DMI_TXN_1 AE43 DMI_RXN1, DMI_TXN_2 AE46 DMI_RXN2, DMI_TXN_3 AH42 DMI_RXN3 → DMI_RXN[3:0] [22]; DMI_TXP_0 AD35 DMI_RXP0, DMI_TXP_1 AE44 DMI_RXP1, DMI_TXP_2 AF46 DMI_RXP2, DMI_TXP_3 AH43 DMI_RXP3 → DMI_RXP[3:0] [22]

CFG: [2,3] MCH_BSEL0 T25, [2,3] MCH_BSEL1 R25, [2,3] MCH_BSEL2 P25, MCH_CFG_3 P20, MCH_CFG_4 P24, MCH_CFG_5 C25, MCH_CFG_6 N24, MCH_CFG_7 M24, MCH_CFG_8 E21, MCH_CFG_9 C23, MCH_CFG_10 C24, MCH_CFG_11 N21, MCH_CFG_12 P21, MCH_CFG_13 T21, MCH_CFG_14 R20, MCH_CFG_15 M20, MCH_CFG_16 L21, MCH_CFG_17 H21, MCH_CFG_18 P29, MCH_CFG_19 R28, MCH_CFG_20 T28 → CFG_0 … CFG_20

PM: [23] PM_SYNC# B7, [3,21,42] H_DPRSTP# B32, [10,11] PM_EXTTS#0 N33, [11] PM_EXTTS#1 P32, [23,42] DELAY_VR_PWRGOOD AT40, [12,22,26,32,34,35,37] PLT_RST-R# R110 100/F_4 AT11, [3,21] PM_THRMTRIP# T20, [23,42] DPRSLPVR R32 → PM_SYNC#, PM_DPRSTP#, PM_EXT_TS#_0, PM_EXT_TS#_1, PWROK, RSTIN#, THERMTRIP#, DPRSLPVR

GRAPHICS VID: GFX_VID_0 B33 GFXVR_VID_0 TP74, GFX_VID_1 B32 GFXVR_VID_1 TP72, GFX_VID_2 G33 GFXVR_VID_2 TP13, GFX_VID_3 F33 GFXVR_VID_3 TP4, GFX_VID_4 E33 GFXVR_VID_4 TP1; GFX_VR_EN C34 GFXVR_EN TP71

ME: CL_CLK AH37 CL_CLK0 [23], CL_DATA AH36 CL_DATA0 [23], CL_PWROK AN36 ECPWROK [4,23,35], CL_RST# AJ35 CL_RST#0 [23], CL_VREF AH34 MCH_CLVREF 0.35 V; +1.05V → R101 1K/F_4, C126 .1U/10V_4, R104 499/F_4

MISC: DDPC_CTRLCLK N28 DDPC_CTRLCLK TP20, DDPC_CTRLDATA M28 DDPC_CTRLDATA TP10, SDVO_CTRLCLK G36 SDVO_CLK [20], SDVO_CTRLDATA K36 SDVO_DATA [20], CLKREQ# E36 CLK_MCH_OE# [2], ICH_SYNC# H36 MCH_ICH_SYNC# [23], TSATN# B12 MCH_TSATN R455 56.2/F_4 +1.05V

HDA: HDA_BCLK B28 ACZ_BITCLK_MCH [21], HDA_RST# B30 ACZ_RST#_MCH [21], HDA_SDI B29 ACZ_SDIN3_MCH R449 *0_4 ACZ_SDIN3 [21], HDA_SDO C29 ACZ_SDOUT_MCH [21], HDA_SYNC A28 ACZ_SYNC_MCH [21]

07/14 (PV2) BOM reomve R449 for UMA use.

NC: NC_1 … NC_26 BG48, BF48, BD48, BC48, BH47, BG47, BE47, BH46, BF46, BG45, BH44, BH43, BH6, BH5, BG4, BH3, BF3, BH2, BG2, BE2, BG1, BF1, BD1, BC1, F1, A47

CANTIGA_PM

+3V: R55 10K/F_4 PM_EXTTS#0, R48 10K/F_4 PM_EXTTS#1

+1.8VSUS: R125 1K/F_4, C197 .01U/16V_4, C196 2.2U/6.3V_6, R142 3.01K/F_4, SM_RCOMP_VOH; C223 .01U/16V_4, C225 2.2U/6.3V_6, R150 1K/F_4, SM_RCOMP_VOL

C674 *33P/50V_4, R454 *33_4, ACZ_BITCLK_MCH

+0.9VSMVREF_MCH: C201 .1U/10V_4, C206 470P/50V_4, R148 *1K/F_4, R122 *1K/F_4

HP SVTP TEST: +1.8VSUS

R147 *0_4/S short0402 → +0.9VSMVREF [10,44]

7/16 (PV2) Change FP for ICT.

[2,4,9,10,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +3V
[8,9,10,36,41,44] +1.8VSUS
[2,3,4,5,8,9,21,24,36,41] +1.05V
[2,3,4,5,8,9,21,24,36,41] +1.05V_PEG

U30C

LVDS: L_BKLT_CTRL, L_BKLT_EN, L_CTRL_CLK; L_CTRL_DATA, L_DDC_CLK, L_DDC_DATA; L_VDD_EN, LVDS_IBG, LVDS_VBG, LVDS_VREFH, LVDS_VREFL

[15,19] DPST_PWM R44 *0_4 DPST_PWM_INT L32
[15,19] LVDS_BLON R60 *0_4 LVDS_BLON_INT G32
R54 *10K/F_4 L_CTRL_CLK M32
+3V R56 *10K/F_4 L_CTRL_DATA M33
[14,15,19] EDIDCLK R57 *0_4 EDIDCLK_INT K33
[14,15,19] EDIDDATA R58 *0_4 EDIDDATA_INT J33
[15,19] DISP_ON R59 *0_4 DISP_ON_INT M29
R460 *2.37K/F_4 LVDS_IBG C44
LVDS_VBG B43
TP70 E37, E38

LVDSA_CLK#: [19] LA_CLK# C41
LVDSA_CLK: [19] LA_CLK C40
LVDSB_CLK#: [19] LB_CLK# B37
LVDSB_CLK: [19] LB_CLK A37

LVDSA_DATA#_0: [19] LA_DATAN0 H47
LVDSA_DATA#_1: [19] LA_DATAN1 E46
LVDSA_DATA#_2: [19] LA_DATAN2 G40
TP75 LA_DATAN3 A40
LVDSA_DATA_0: [19] LA_DATAP0 H48
LVDSA_DATA_1: [19] LA_DATAP1 D45
LVDSA_DATA_2: [19] LA_DATAP2 F40
TP73 LA_DATAP3 B40
LVDSB_DATA#_0: [19] LB_DATAN0 A41
LVDSB_DATA#_1: [19] LB_DATAN1 H38
LVDSB_DATA#_2: [19] LB_DATAN2 G37
TP19 LB_DATAN3 J37
LVDSB_DATA_0: [19] LB_DATAP0 B42
LVDSB_DATA_1: [19] LB_DATAP1 G38
LVDSB_DATA_2: [19] LB_DATAP2 F37
TP15 LB_DATAP3 K37

TV: TVA_DAC, TVB_DAC, TVC_DAC, TV_RTN, TV_DCONSEL_0, TV_DCONSEL_1

R70 75/F_4 TV_COMP1 F25
R71 75/F_4 TV_Y/G1 H25
R77 75/F_4 TV_C/R1 K25
Change to 75 ohm to GND
H24
R61 *0_4 TV_DCONSEL0 C31
R45 *0_4 TV_DCONSEL1 E32
Change to 0 ohm to GND

VGA: CRT_BLUE, CRT_GREEN, CRT_RED, CRT_IRTN, CRT_DDC_CLK, CRT_DDC_DATA, CRT_HSYNC, CRT_TVO_IREF, CRT_VSYNC

[14,20] CRT_B R126 *0_4 CRT_B_1 E28
R69 *150/F_4
[14,20] CRT_G R127 *0_4 CRT_G_1 G28
R72 *150/F_4
[14,20] CRT_R R128 *0_4 CRT_R_1 J28
R83 *150/F_4
G29
[14,20] DDCCLK R63 *0_4 DDCCLK_INT H32
[14,20] DDCDATA R64 *0_4 DDCDATA_INT J32
R66 *33_4 HSYNC_INT J29
R65 *1.02K/F_4 CRTIREF E29
R67 *33_4 VSYNC_INT L29
[14,20] HSYNC_COM R680 *0_4
[14,20] VSYNC_COM R679 *0_4

CANTIGA_PM

PCI-EXPRESS GRAPHICS

PEG_TX#[15:0] → PEG_TX#[15:0] [12]
PEG_TX[15:0] → PEG_TX[15:0] [12]
PEG_RX#[15:0] → PEG_RX#[15:0] [12]
PEG_RX[15:0] → PEG_RX[15:0] [12]

+1.05V_PEG
PEG_COMPI T37, PEG_COMPO T36, PEG_COMP R86 49.9/F_4

PEG_RX#_0 H44 PEG_RX#0, PEG_RX#_1 J46 PEG_RX#1, PEG_RX#_2 L44 PEG_RX#2, PEG_RX#_3 L40 PEG_RX#3, PEG_RX#_4 N41 PEG_RX#4, PEG_RX#_5 P48 PEG_RX#5, PEG_RX#_6 N44 PEG_RX#6, PEG_RX#_7 T43 PEG_RX#7, PEG_RX#_8 U43 PEG_RX#8, PEG_RX#_9 Y43 PEG_RX#9, PEG_RX#_10 Y48 PEG_RX#10, PEG_RX#_11 Y36 PEG_RX#11, PEG_RX#_12 AA43 PEG_RX#12, PEG_RX#_13 AD37 PEG_RX#13, PEG_RX#_14 AC47 PEG_RX#14, PEG_RX#_15 AD39 PEG_RX#15

PEG_RX_0 H43 PEG_RX0, PEG_RX_1 J44 PEG_RX1, PEG_RX_2 L43 PEG_RX2, PEG_RX_3 L41 PEG_RX3 R68 *0_4 HDMI_HPD#, PEG_RX_4 N40 PEG_RX4, PEG_RX_5 P47 PEG_RX5, PEG_RX_6 N43 PEG_RX6, PEG_RX_7 T42 PEG_RX7, PEG_RX_8 U42 PEG_RX8, PEG_RX_9 Y42 PEG_RX9, PEG_RX_10 W47 PEG_RX10, PEG_RX_11 Y37 PEG_RX11, PEG_RX_12 AA42 PEG_RX12, PEG_RX_13 AD36 PEG_RX13, PEG_RX_14 AC48 PEG_RX14, PEG_RX_15 AD40 PEG_RX15

int

PEG_TX#_0 J41 C_PEG_TX#0 C41 1U/10V_4 PEG_TX#0, PEG_TX#_1 M46 C_PEG_TX#1 C47 1U/10V_4 PEG_TX#1, PEG_TX#_2 M47 C_PEG_TX#2 C55 1U/10V_4 PEG_TX#2, PEG_TX#_3 M40 C_PEG_TX#3 C52 1U/10V_4 PEG_TX#3, PEG_TX#_4 M42 C_PEG_TX#4 C56 1U/10V_4 PEG_TX#4, PEG_TX#_5 R48 C_PEG_TX#5 C65 1U/10V_4 PEG_TX#5, PEG_TX#_6 N38 C_PEG_TX#6 C62 1U/10V_4 PEG_TX#6, PEG_TX#_7 T40 C_PEG_TX#7 C64 1U/10V_4 PEG_TX#7, PEG_TX#_8 U37 C_PEG_TX#8 C74 1U/10V_4 PEG_TX#8, PEG_TX#_9 U40 C_PEG_TX#9 C71 1U/10V_4 PEG_TX#9, PEG_TX#_10 Y40 C_PEG_TX#10 C77 1U/10V_4 PEG_TX#10, PEG_TX#_11 AA46 C_PEG_TX#11 C79 1U/10V_4 PEG_TX#11, PEG_TX#_12 AA37 C_PEG_TX#12 C82 1U/10V_4 PEG_TX#12, PEG_TX#_13 AA40 C_PEG_TX#13 C95 1U/10V_4 PEG_TX#13, PEG_TX#_14 AD43 C_PEG_TX#14 C97 1U/10V_4 PEG_TX#14, PEG_TX#_15 AC46 C_PEG_TX#15 C100 1U/10V_4 PEG_TX#15

PEG_TX_0 J42 C_PEG_TX0 C45 1U/10V_4 PEG_TX0, PEG_TX_1 L46 C_PEG_TX1 C44 1U/10V_4 PEG_TX1, PEG_TX_2 M48 C_PEG_TX2 C53 1U/10V_4 PEG_TX2, PEG_TX_3 M39 C_PEG_TX3 C49 1U/10V_4 PEG_TX3, PEG_TX_4 M43 C_PEG_TX4 C60 1U/10V_4 PEG_TX4, PEG_TX_5 R47 C_PEG_TX5 C66 1U/10V_4 PEG_TX5, PEG_TX_6 N37 C_PEG_TX6 C61 1U/10V_4 PEG_TX6, PEG_TX_7 T39 C_PEG_TX7 C63 1U/10V_4 PEG_TX7, PEG_TX_8 U36 C_PEG_TX8 C72 1U/10V_4 PEG_TX8, PEG_TX_9 U39 C_PEG_TX9 C69 1U/10V_4 PEG_TX9, PEG_TX_10 Y39 C_PEG_TX10 C75 1U/10V_4 PEG_TX10, PEG_TX_11 Y46 C_PEG_TX11 C83 1U/10V_4 PEG_TX11, PEG_TX_12 AA45 C_PEG_TX12 C88 1U/10V_4 PEG_TX12, PEG_TX_13 AA39 C_PEG_TX13 C90 1U/10V_4 PEG_TX13, PEG_TX_14 AD42 C_PEG_TX14 C92 1U/10V_4 PEG_TX14, PEG_TX_15 AD46 C_PEG_TX15 C111 1U/10V_4 PEG_TX15

dis

For UMA HDMI Function

[12] PEG_TX#0_VGA, [12] PEG_TX0_VGA → RP62 *0_4P2R/S short-4p2r-0404 → PEG_TX#0, PEG_TX0 → RP19 *4P2R-S-0 → IN_D2#, IN_D2 [20]
[12] PEG_TX#1_VGA, [12] PEG_TX1_VGA → RP63 *0_4P2R/S short-4p2r-0404 → PEG_TX#1, PEG_TX1 → RP17 *4P2R-S-0 → IN_D1#, IN_D1 [20]
[12] PEG_TX#2_VGA, [12] PEG_TX2_VGA → RP64 *0_4P2R/S short-4p2r-0404 → PEG_TX#2, PEG_TX2 → RP20 *4P2R-S-0 → IN_D0#, IN_D0 [20]
[12] PEG_TX#3_VGA, [12] PEG_TX3_VGA → RP65 *0_4P2R/S short-4p2r-0404 → PEG_TX#3, PEG_TX3 → RP18 *4P2R-S-0 → IN_CLK#, IN_CLK [20]

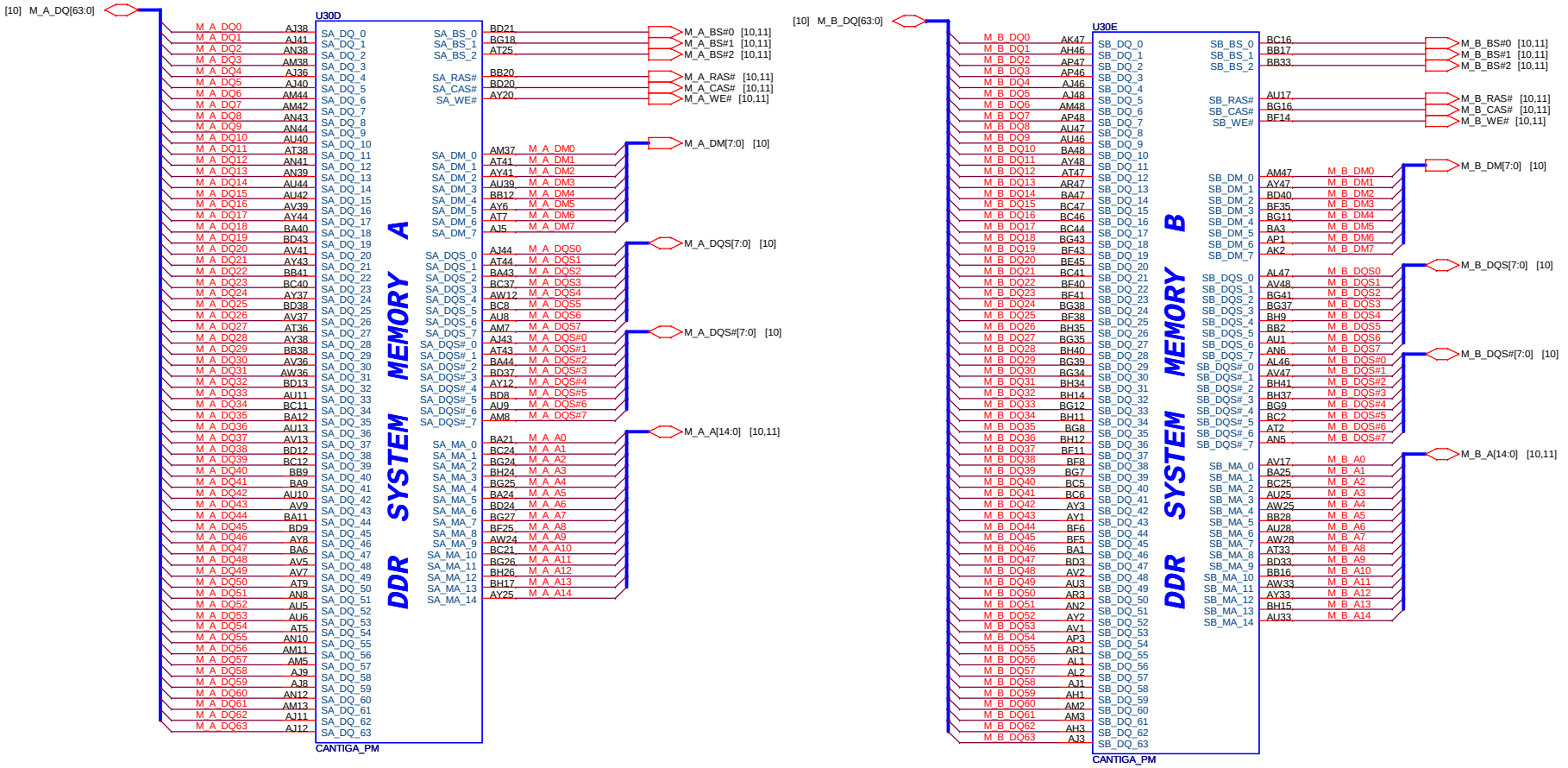
For DIS VGA Function

05/22 (PV) FOR UMA HDMI issue.
07/14 (PV2) Change footprint for PE require.

C416,C423,C440,C431
C419,C418,C430,C424
Need to install for GM

HPD# Inverting Level Shifting Circuit

+3V R39 *20K/F_4 HDMI_HPD#
[20] HDMI_HPD_CON
Q8 *ME2N7002E
R38 *100K/F_4
R43 *7.5K/F_4
Level: 0.9V



NB5

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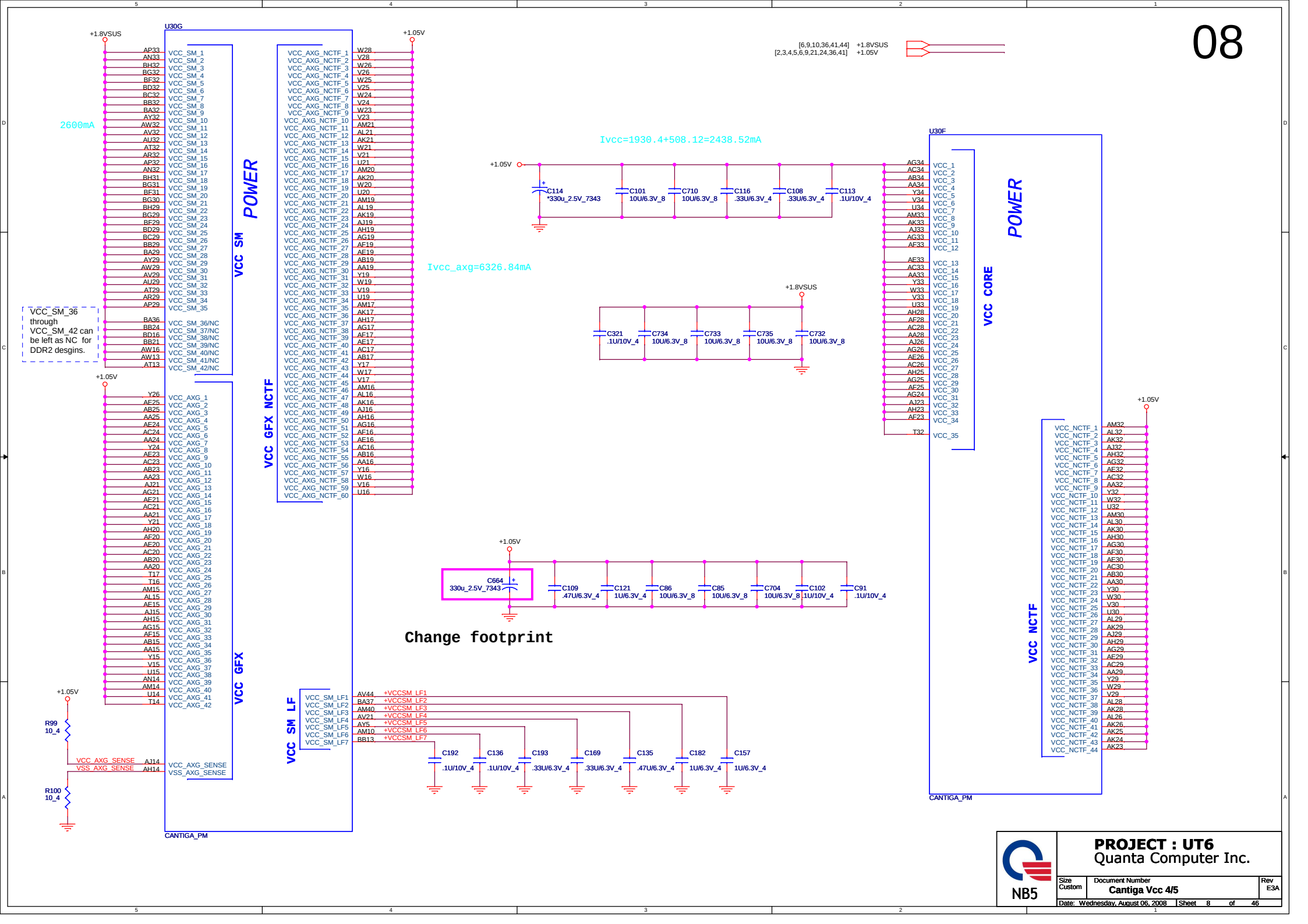

[6,9,10,36,41,44] +1.8VSUS
[2,3,4,5,6,9,21,24,36,41] +1.05V

+1.05V [2,3,4,5,6,8,21,24,36,41]
+3V [2,4,6,10,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45]
+1.5V [4,21,22,24,27,34,37,41]
+1.8VSUS [6,8,10,36,41,44]
+1.05V_PEG [2,3,4,5,6,8,21,24,36,41]

QT6 Modified-0117

Intel Design Guide 1.5

thermal management is enabled on discrete graphics motherboard

Change footprint

Modified

SI-2 Del L11
SI-2 Del R474
SI-2 Del R94
SI-2 Del R108
SI-2 Del R50
SI-2 Del R445
SI-2 Del L12
SI-2 Del L55

05/23 (PV) Del for PE require.

POWER

CANTIGA_PM

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Rev E3A
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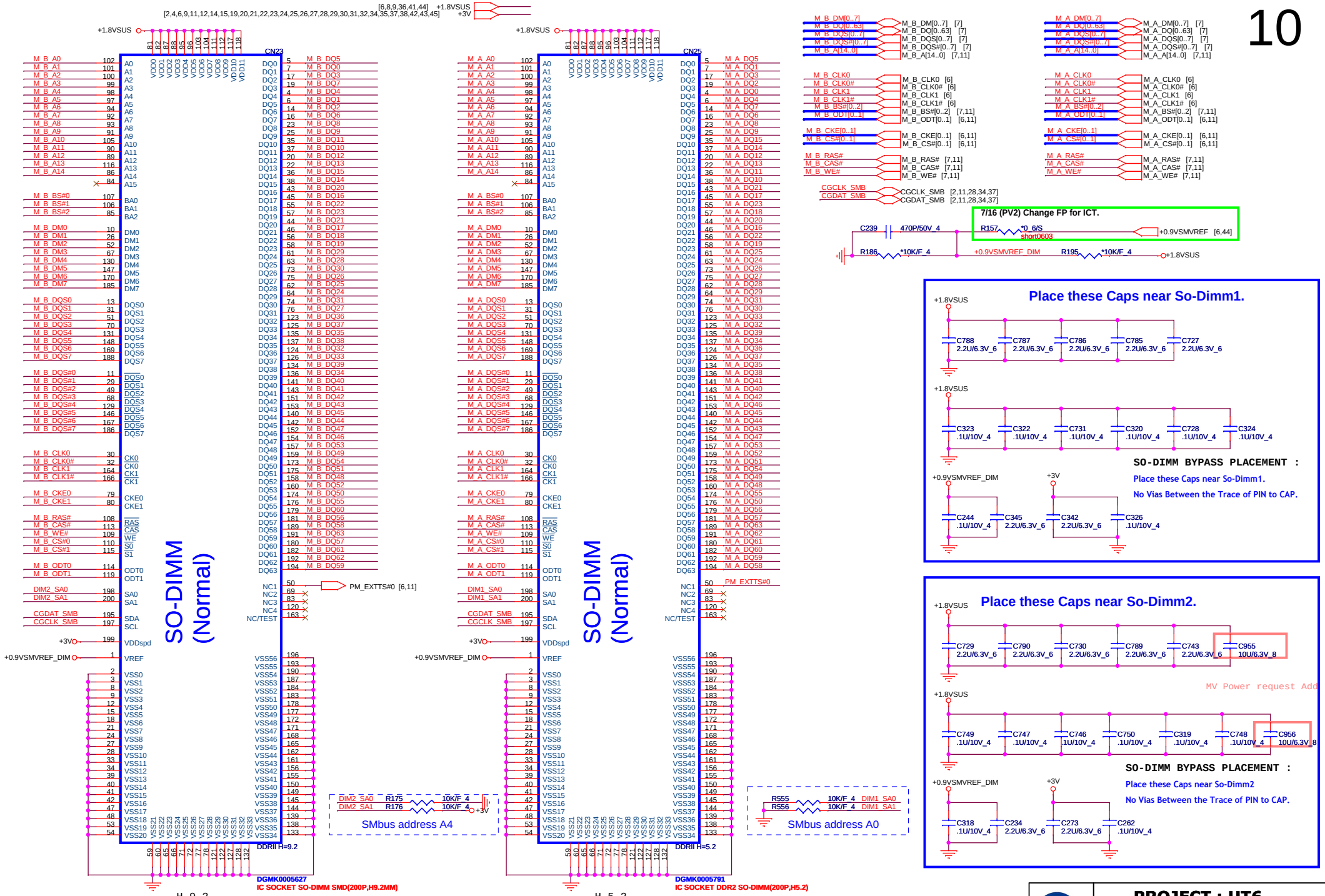
[6,8,9,36,41,44] +1.8VSUS
[2,4,6,9,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +3V
+1.8VSUS
CN23
SO-DIMM (Normal)
M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13 M_B_A14
M_B_BS#0 M_B_BS#1 M_B_BS#2
M_B_DM0 M_B_DM1 M_B_DM2 M_B_DM3 M_B_DM4 M_B_DM5 M_B_DM6 M_B_DM7
M_B_DQS0 M_B_DQS1 M_B_DQS2 M_B_DQS3 M_B_DQS4 M_B_DQS5 M_B_DQS6 M_B_DQS7
M_B_DQS#0 M_B_DQS#1 M_B_DQS#2 M_B_DQS#3 M_B_DQS#4 M_B_DQS#5 M_B_DQS#6 M_B_DQS#7
M_B_CLK0 M_B_CLK0# M_B_CLK1 M_B_CLK1#
M_B_CKE0 M_B_CKE1
M_B_RAS# M_B_CAS# M_B_WE# M_B_CS#0 M_B_CS#1
M_B_ODT0 M_B_ODT1
DIM2_SA0 DIM2_SA1
CGDAT_SMB CGCLK_SMB
+3V +0.9VSMVREF_DIM
M_B_DQ0 M_B_DQ1 M_B_DQ2 M_B_DQ3 M_B_DQ4 M_B_DQ5 M_B_DQ6 M_B_DQ7 M_B_DQ8 M_B_DQ9 M_B_DQ10 M_B_DQ11 M_B_DQ12 M_B_DQ13 M_B_DQ14 M_B_DQ15 M_B_DQ16 M_B_DQ17 M_B_DQ18 M_B_DQ19 M_B_DQ20 M_B_DQ21 M_B_DQ22 M_B_DQ23 M_B_DQ24 M_B_DQ25 M_B_DQ26 M_B_DQ27 M_B_DQ28 M_B_DQ29 M_B_DQ30 M_B_DQ31 M_B_DQ32 M_B_DQ33 M_B_DQ34 M_B_DQ35 M_B_DQ36 M_B_DQ37 M_B_DQ38 M_B_DQ39 M_B_DQ40 M_B_DQ41 M_B_DQ42 M_B_DQ43 M_B_DQ44 M_B_DQ45 M_B_DQ46 M_B_DQ47 M_B_DQ48 M_B_DQ49 M_B_DQ50 M_B_DQ51 M_B_DQ52 M_B_DQ53 M_B_DQ54 M_B_DQ55 M_B_DQ56 M_B_DQ57 M_B_DQ58 M_B_DQ59 M_B_DQ60 M_B_DQ61 M_B_DQ62 M_B_DQ63
NC1 NC2 NC3 NC4 NC/TEST
PM_EXTTS#0 [6,11]
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56
DIM2_SA0 R175 10K/F_4
DIM2_SA1 R176 10K/F_4 +3V
SMbus address A4
DDRII H=9.2
DGMK0005627
IC SOCKET SO-DIMM SMD(200P,H9.2MM)
H 9.2
SI modified
Footprint: "ddr-1-1775859-1-200p-ldv
+1.8VSUS
CN25
SO-DIMM (Normal)
M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14
M_A_BS#0 M_A_BS#1 M_A_BS#2
M_A_DM0 M_A_DM1 M_A_DM2 M_A_DM3 M_A_DM4 M_A_DM5 M_A_DM6 M_A_DM7
M_A_DQS0 M_A_DQS1 M_A_DQS2 M_A_DQS3 M_A_DQS4 M_A_DQS5 M_A_DQS6 M_A_DQS7
M_A_DQS#0 M_A_DQS#1 M_A_DQS#2 M_A_DQS#3 M_A_DQS#4 M_A_DQS#5 M_A_DQS#6 M_A_DQS#7
M_A_CLK0 M_A_CLK0# M_A_CLK1 M_A_CLK1#
M_A_CKE0 M_A_CKE1
M_A_RAS# M_A_CAS# M_A_WE# M_A_CS#0 M_A_CS#1
M_A_ODT0 M_A_ODT1
DIM1_SA0 DIM1_SA1
CGDAT_SMB CGCLK_SMB
+3V +0.9VSMVREF_DIM
M_A_DQ0 M_A_DQ1 M_A_DQ2 M_A_DQ3 M_A_DQ4 M_A_DQ5 M_A_DQ6 M_A_DQ7 M_A_DQ8 M_A_DQ9 M_A_DQ10 M_A_DQ11 M_A_DQ12 M_A_DQ13 M_A_DQ14 M_A_DQ15 M_A_DQ16 M_A_DQ17 M_A_DQ18 M_A_DQ19 M_A_DQ20 M_A_DQ21 M_A_DQ22 M_A_DQ23 M_A_DQ24 M_A_DQ25 M_A_DQ26 M_A_DQ27 M_A_DQ28 M_A_DQ29 M_A_DQ30 M_A_DQ31 M_A_DQ32 M_A_DQ33 M_A_DQ34 M_A_DQ35 M_A_DQ36 M_A_DQ37 M_A_DQ38 M_A_DQ39 M_A_DQ40 M_A_DQ41 M_A_DQ42 M_A_DQ43 M_A_DQ44 M_A_DQ45 M_A_DQ46 M_A_DQ47 M_A_DQ48 M_A_DQ49 M_A_DQ50 M_A_DQ51 M_A_DQ52 M_A_DQ53 M_A_DQ54 M_A_DQ55 M_A_DQ56 M_A_DQ57 M_A_DQ58 M_A_DQ59 M_A_DQ60 M_A_DQ61 M_A_DQ62 M_A_DQ63
NC1 NC2 NC3 NC4 NC/TEST
PM_EXTTS#0
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56
R555 10K/F_4 DIM1_SA0
R556 10K/F_4 DIM1_SA1
SMbus address A0
DDRII H=5.2
DGMK0005791
IC SOCKET DDR2 SO-DIMM(200P,H5.2)
H 5.2
SI modified
Footprint: "DDR-1-1734075-1-200P
M_B_DM[0..7] M_B_DQ[0..63] M_B_DQS[0..7] M_B_DQS#[0..7] M_B_A[14..0]
M_B_DM[0..7] [7]
M_B_DQ[0..63] [7]
M_B_DQS[0..7] [7]
M_B_DQS#[0..7] [7]
M_B_A[14..0] [7,11]
M_B_CLK0 M_B_CLK0# M_B_CLK1 M_B_CLK1# M_B_BS#[0..2] M_B_ODT[0..1]
M_B_CLK0 [6]
M_B_CLK0# [6]
M_B_CLK1 [6]
M_B_CLK1# [6]
M_B_BS#[0..2] [7,11]
M_B_ODT[0..1] [6,11]
M_B_CKE[0..1] M_B_CS#[0..1]
M_B_CKE[0..1] [6,11]
M_B_CS#[0..1] [6,11]
M_B_RAS# M_B_CAS# M_B_WE#
M_B_RAS# [7,11]
M_B_CAS# [7,11]
M_B_WE# [7,11]
CGCLK_SMB CGDAT_SMB
CGCLK_SMB [2,11,28,34,37]
CGDAT_SMB [2,11,28,34,37]
M_A_DM[0..7] M_A_DQ[0..63] M_A_DQS[0..7] M_A_DQS#[0..7] M_A_A[14..0]
M_A_DM[0..7] [7]
M_A_DQ[0..63] [7]
M_A_DQS[0..7] [7]
M_A_DQS#[0..7] [7]
M_A_A[14..0] [7,11]
M_A_CLK0 M_A_CLK0# M_A_CLK1 M_A_CLK1# M_A_BS#[0..2] M_A_ODT[0..1]
M_A_CLK0 [6]
M_A_CLK0# [6]
M_A_CLK1 [6]
M_A_CLK1# [6]
M_A_BS#[0..2] [7,11]
M_A_ODT[0..1] [6,11]
M_A_CKE[0..1] M_A_CS#[0..1]
M_A_CKE[0..1] [6,11]
M_A_CS#[0..1] [6,11]
M_A_RAS# M_A_CAS# M_A_WE#
M_A_RAS# [7,11]
M_A_CAS# [7,11]
M_A_WE# [7,11]
7/16 (PV2) Change FP for ICT.
C239 470P/50V_4
R157 *0_6/S
short0603
+0.9VSMVREF [6,44]
R186 *10K/F_4
+0.9VSMVREF_DIM
R195 *10K/F_4
+1.8VSUS
Place these Caps near So-Dimm1.
+1.8VSUS
C788 2.2U/6.3V_6
C787 2.2U/6.3V_6
C786 2.2U/6.3V_6
C785 2.2U/6.3V_6
C727 2.2U/6.3V_6
+1.8VSUS
C323 .1U/10V_4
C322 .1U/10V_4
C731 .1U/10V_4
C320 .1U/10V_4
C728 .1U/10V_4
C324 .1U/10V_4
SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.
+0.9VSMVREF_DIM
C244 .1U/10V_4
C345 2.2U/6.3V_6
+3V
C342 2.2U/6.3V_6
C326 .1U/10V_4
Place these Caps near So-Dimm2.
+1.8VSUS
C729 2.2U/6.3V_6
C790 2.2U/6.3V_6
C730 2.2U/6.3V_6
C789 2.2U/6.3V_6
C743 2.2U/6.3V_6
C955 10U/6.3V_8
MV Power request Add
+1.8VSUS
C749 .1U/10V_4
C747 .1U/10V_4
C746 .1U/10V_4
C750 .1U/10V_4
C319 .1U/10V_4
C748 .1U/10V_4
C956 10U/6.3V_8
SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm2
No Vias Between the Trace of PIN to CAP.
+0.9VSMVREF_DIM
C318 .1U/10V_4
C234 2.2U/6.3V_6
+3V
C273 2.2U/6.3V_6
C262 .1U/10V_4
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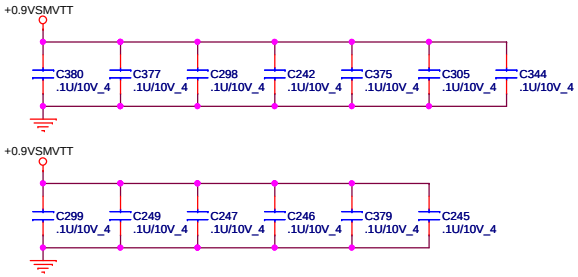
+0.9VSMVTT [44]

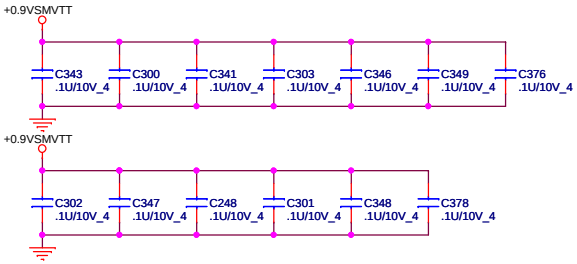
+3V [2,4,6,9,10,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45]

DDRII DUAL CHANNEL A,B.

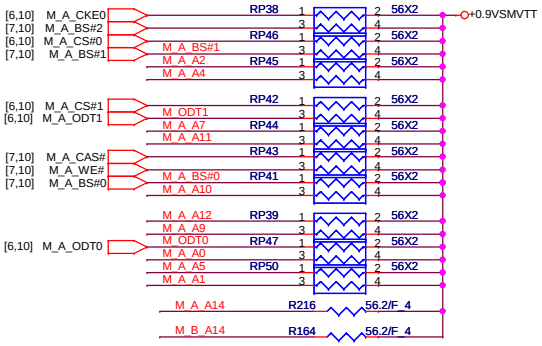
DDRII A CHANNEL

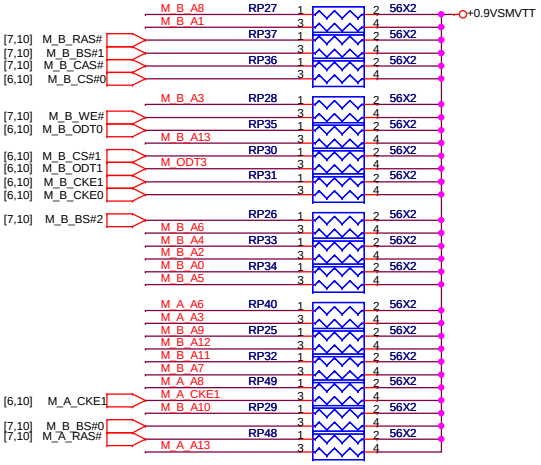


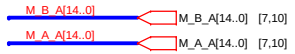
DDRII B CHANNEL

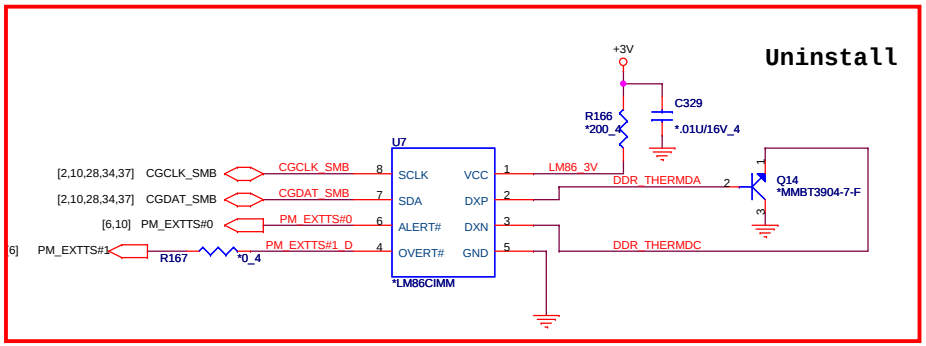


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM









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[2,4,6,9,10,11,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +3V
[13,14,44] +VGA1.1V

U35A
BGA969-NVIDIA-NB9P-GS
COMMON

PCI EXPRESS

+VGA1.1V
C238 22U/6.3V_8
C237 4.7U/6.3V_6
C253 1U/6.3V_4
C243 1U/6.3V_4
C716 .1U/10V_4
C709 .1U/10V_4
C706 .47U/6.3V_4
~ 500mA

+VGA1.1V
C707 22U/6.3V_8
C205 4.7U/6.3V_6
C254 1U/6.3V_4
C204 .47U/6.3V_4
C723 .47U/6.3V_4
C718 .1U/10V_4
1600mA

Near BGA

+3V
C292 1U/6.3V_4
C310 .1U/10V_4
C339 .1U/10V_4

[43] VGA_SENSE
SI-2 4/10 For Nvidia recommend.

+VGA1.1V
L22 10nH_6
+PEX_PLLVDD
C236 4.7U/6.3V_6
C720 4.7U/6.3V_6
C726 1U/6.3V_4
C251 .1U/10V_4
C724 .01U/16V_4
100mA
12~16 mils width

AK16 PEX_IOVDD_1
AK17 PEX_IOVDD_2
AK21 PEX_IOVDD_3
AK24 PEX_IOVDD_4
AK27 PEX_IOVDD_5

AG11 PEX_IOVDDQ_1
AG12 PEX_IOVDDQ_2
AG13 PEX_IOVDDQ_3
AG15 PEX_IOVDDQ_4
AG16 PEX_IOVDDQ_5
AG17 PEX_IOVDDQ_6
AG18 PEX_IOVDDQ_7
AG22 PEX_IOVDDQ_8
AG23 PEX_IOVDDQ_9
AG24 PEX_IOVDDQ_10
AG25 PEX_IOVDDQ_11
AG26 PEX_IOVDDQ_12
AJ14 PEX_IOVDDQ_13
AJ15 PEX_IOVDDQ_14
AJ19 PEX_IOVDDQ_15
AJ21 PEX_IOVDDQ_16
AJ22 PEX_IOVDDQ_17
AJ24 PEX_IOVDDQ_18
AJ25 PEX_IOVDDQ_19
AJ27 PEX_IOVDDQ_20
AK18 PEX_IOVDDQ_21
AK20 PEX_IOVDDQ_22
AK23 PEX_IOVDDQ_23
AK26 PEX_IOVDDQ_24
AL16 PEX_IOVDDQ_25

J10 VDD33_1
J11 VDD33_2
J12 VDD33_3
J13 VDD33_4
J9 VDD33_5

AD20 VDD_SENSE
AD19 GND_SENSE
AG14 PEX_PLLVDD
AG19 PEX_CAL_PD_VDDQ
AG20 PEX_CAL_PU_GND

A2 NC_1
AB7 NC_2
AD6 NC_3
AE6 NC_4
AG6 NC_5
AJ5 NC_6
AK15 NC_7
AL7 NC_8
D35 NC_9
E35 NC_10
E7 NC_11
F7 NC_12
H32 NC_13
M7 NC_14
P6 NC_15
P7 NC_16
R7 NC_17
U7 NC_18
V6 NC_19

PEX_RX0 AP17 PEG_TX0_VGA
PEX_RX0* AN17 PEG_TX#0_VGA
PEX_RX1 AN19 PEG_TX1_VGA
PEX_RX1* AP19 PEG_TX#1_VGA
PEX_RX2 AR19 PEG_TX2_VGA
PEX_RX2* AR20 PEG_TX#2_VGA
PEX_RX3 AP20 PEG_TX3_VGA
PEX_RX3* AN20 PEG_TX#3_VGA
PEX_RX4 AN22 PEG_TX4
PEX_RX4* AP22 PEG_TX#4
PEX_RX5 AR22 PEG_TX5
PEX_RX5* AR23 PEG_TX#5
PEX_RX6 AP23 PEG_TX6
PEX_RX6* AN23 PEG_TX#6
PEX_RX7 AN25 PEG_TX7
PEX_RX7* AP25 PEG_TX#7
PEX_RX8 AR25 PEG_TX8
PEX_RX8* AR26 PEG_TX#8
PEX_RX9 AP26 PEG_TX9
PEX_RX9* AN26 PEG_TX#9
PEX_RX10 AN28 PEG_TX10
PEX_RX10* AP28 PEG_TX#10
PEX_RX11 AR28 PEG_TX11
PEX_RX11* AR29 PEG_TX#11
PEX_RX12 AP29 PEG_TX12
PEX_RX12* AN29 PEG_TX#12
PEX_RX13 AN31 PEG_TX13
PEX_RX13* AP31 PEG_TX#13
PEX_RX14 AR31 PEG_TX14
PEX_RX14* AR32 PEG_TX#14
PEX_RX15 AR34 PEG_TX15
PEX_RX15* AP34 PEG_TX#15

PEG_TX0_VGA [6]
PEG_TX#0_VGA [6]
PEG_TX1_VGA [6]
PEG_TX#1_VGA [6]
PEG_TX2_VGA [6]
PEG_TX#2_VGA [6]
PEG_TX3_VGA [6]
PEG_TX#3_VGA [6]

05/22 (PV) FOR UMA HDMI.

PEG_TX4 [6]
PEG_TX#4 [6]
PEG_TX5 [6]
PEG_TX#5 [6]
PEG_TX6 [6]
PEG_TX#6 [6]
PEG_TX7 [6]
PEG_TX#7 [6]
PEG_TX8 [6]
PEG_TX#8 [6]
PEG_TX9 [6]
PEG_TX#9 [6]
PEG_TX10 [6]
PEG_TX#10 [6]
PEG_TX11 [6]
PEG_TX#11 [6]
PEG_TX12 [6]
PEG_TX#12 [6]
PEG_TX13 [6]
PEG_TX#13 [6]
PEG_TX14 [6]
PEG_TX#14 [6]
PEG_TX15 [6]
PEG_TX#15 [6]

PEX_TX0 AL17 C_PEG_RX0 C171 .1U/10V_4
PEX_TX0* AM17 C_PEG_RX#0 C170 .1U/10V_4
PEX_TX1 AM18 C_PEG_RX1 C209 .1U/10V_4
PEX_TX1* AM19 C_PEG_RX#1 C210 .1U/10V_4
PEX_TX2 AL19 C_PEG_RX2 C172 .1U/10V_4
PEX_TX2* AK19 C_PEG_RX#2 C173 .1U/10V_4
PEX_TX3 AL20 C_PEG_RX3 C145 .1U/10V_4
PEX_TX3* AM20 C_PEG_RX#3 C146 .1U/10V_4
PEX_TX4 AM21 C_PEG_RX4 C211 .1U/10V_4
PEX_TX4* AM22 C_PEG_RX#4 C212 .1U/10V_4
PEX_TX5 AL22 C_PEG_RX5 C213 .1U/10V_4
PEX_TX5* AK22 C_PEG_RX#5 C214 .1U/10V_4
PEX_TX6 AL23 C_PEG_RX6 C147 .1U/10V_4
PEX_TX6* AM23 C_PEG_RX#6 C148 .1U/10V_4
PEX_TX7 AM24 C_PEG_RX7 C174 .1U/10V_4
PEX_TX7* AM25 C_PEG_RX#7 C175 .1U/10V_4
PEX_TX8 AL25 C_PEG_RX8 C149 .1U/10V_4
PEX_TX8* AK25 C_PEG_RX#8 C150 .1U/10V_4
PEX_TX9 AL26 C_PEG_RX9 C176 .1U/10V_4
PEX_TX9* AM26 C_PEG_RX#9 C177 .1U/10V_4
PEX_TX10 AM27 C_PEG_RX10 C151 .1U/10V_4
PEX_TX10* AM28 C_PEG_RX#10 C152 .1U/10V_4
PEX_TX11 AL28 C_PEG_RX11 C199 .1U/10V_4
PEX_TX11* AK28 C_PEG_RX#11 C200 .1U/10V_4
PEX_TX12 AK29 C_PEG_RX12 C178 .1U/10V_4
PEX_TX12* AL29 C_PEG_RX#12 C179 .1U/10V_4
PEX_TX13 AM29 C_PEG_RX13 C162 .1U/10V_4
PEX_TX13* AM30 C_PEG_RX#13 C163 .1U/10V_4
PEX_TX14 AM31 C_PEG_RX14 C155 .1U/10V_4
PEX_TX14* AM32 C_PEG_RX#14 C156 .1U/10V_4
PEX_TX15 AN32 C_PEG_RX15 C180 .1U/10V_4
PEX_TX15* AP32 C_PEG_RX#15 C181 .1U/10V_4

PEG_RX0 [6]
PEG_RX#0 [6]
PEG_RX1 [6]
PEG_RX#1 [6]
PEG_RX2 [6]
PEG_RX#2 [6]
PEG_RX3 [6]
PEG_RX#3 [6]
PEG_RX4 [6]
PEG_RX#4 [6]
PEG_RX5 [6]
PEG_RX#5 [6]
PEG_RX6 [6]
PEG_RX#6 [6]
PEG_RX7 [6]
PEG_RX#7 [6]
PEG_RX8 [6]
PEG_RX#8 [6]
PEG_RX9 [6]
PEG_RX#9 [6]
PEG_RX10 [6]
PEG_RX#10 [6]
PEG_RX11 [6]
PEG_RX#11 [6]
PEG_RX12 [6]
PEG_RX#12 [6]
PEG_RX13 [6]
PEG_RX#13 [6]
PEG_RX14 [6]
PEG_RX#14 [6]
PEG_RX15 [6]
PEG_RX#15 [6]

PEX_REFCLK AR16 CLK_PCIE_VGA
PEX_REFCLK* AR17 CLK_PCIE_VGA#

CLK_PCIE_VGA [2]
CLK_PCIE_VGA# [2]

PEX_TSTCLK_OUT AJ17 R161 *200_4
PEX_TSTCLK_OUT* AJ18

PEX_RST* AM16 VGA_RST# R491 100/F_4
PEX_CLKREQ* AR13 PEX_CLKREQ# T5
PEX_TERMP AG21 PEX_TERMP R165 2.49K/F_4
TESTMODE AP35 TESTMODE R486 10K/F_4

PLT_RST-R#-1
D28 *RB501V-40
PLT_RST-R#
PLT_RST-R# [6,22,26,32,34,35,37]
R490 *100K/F_4
R487 *0_4/S short0402

07/14 (PV2) Change footprint for PE require.

PROJECT : UT6
Quanta Computer Inc.
NB5
Size Custom
Document Number NV9X (PCIE I/F) 1/5
Rev E3A
Date: Wednesday, August 06, 2008 Sheet 12 of 46

U35B
BGA969-NVIDIA-NB9P-GS
COMMON

MEMORY I/F A

U35C
BGA969-NVIDIA-NB9P-GS
COMMON

MEMORY I/F B

SI-II Add

SI-II Add

R505 10K/F_4 VMA_ODT

R159 10K/F_4 VMA_CKE

for DDR2 need use CMD11(CKE) and CMD12(ODT)

R299 10K/F_4 VMC_ODT

R298 10K/F_4 VMC_CKE

R190 *1K/F_4

R189 *1K/F_4

15mils width

use internal Vref, ext divider no stuff

C355 .1U/10V_4

For Debug only

R177 *60.4/F_4

15mils width

L20 HCB1608KF-181T15_6

C333 .1U/10V_4 C352 .1U/10V_4 C235 10U/6.3V_4 C921 4.7U/6.3V_6

For Nvidia request

G96 only

R191 30.1/F_4

R183 30.1/F_4

R184 *30.1/F_4

R192 Install for DDR3

R196 *60.4/F_4

R178 no stuff

C361 .1U/10V_4 C252 .1U/10V_4

For NB9P-GS only

C415 4.7U/6.3V_6 C405 .47U/6.3V_4 C482 .47U/6.3V_4 C293 .1U/10V_4 C390 4.7U/6.3V_6 C263 .47U/6.3V_4 C335 .47U/6.3V_4 C358 .1U/10V_4 C835 .1U/10V_4 C325 .1U/10V_4 C294 .1U/10V_4 C360 .1U/10V_4 C805 .1U/10V_4 C350 .1U/10V_4

C486 4.7U/6.3V_6 C477 .47U/6.3V_4 C818 .47U/6.3V_4 C330 .1U/10V_4 C485 4.7U/6.3V_6 C481 .47U/6.3V_4 C337 .47U/6.3V_4 C338 .1U/10V_4 C331 .1U/10V_4 C285 .1U/10V_4 C359 .1U/10V_4 C309 .1U/10V_4 C272 .1U/10V_4 C362 .1U/10V_4

NB5

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV9X (MEMORY I/F) 2/5	E3A
Date: Wednesday, August 06, 2008	Sheet 13 of 46	

U35D
BGA969-NVIDIA-N89P-GS
COMMON

IFPAB(LVDS)
IFPCD
IFPC
IFPD
IFPEF
DACA(CRT)
DACC(CRT2)
DACB(TV)
XTAL_PLL

TMDS channel two

Display port output

07/14 (PV2) Change footprint for PE require.

MV modify short pad

SI modified
Nvidia request

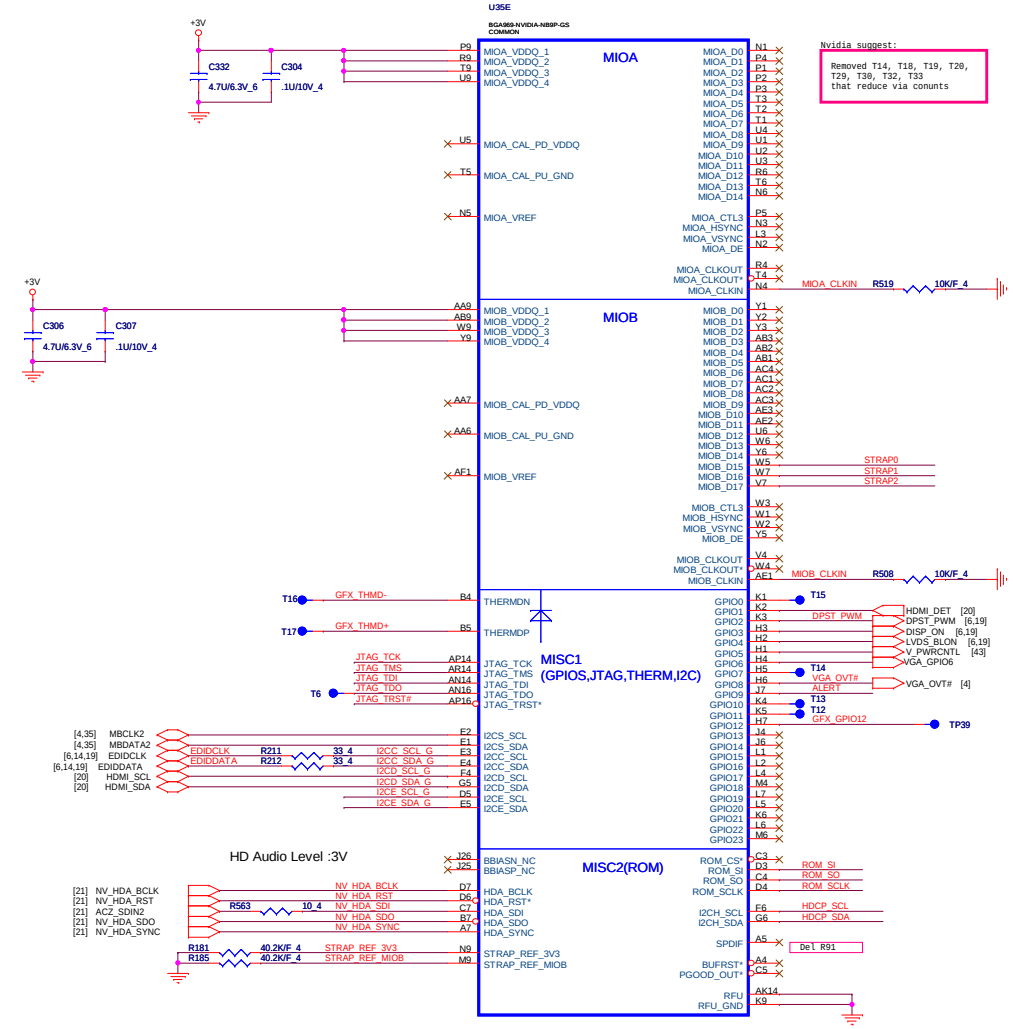
SPREAD SPECTRUM

I2C ADDRESS: 0xD4H

NVidia suggest:
10 kΩ pull-down only if no spread chip used.

05/12 (PV) FOR EMI Solution

PROJECT	UT6
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: NV9X (DISPLAY) 3/5
Rev	E3A
Date: Wednesday, August 06, 2008	Sheet 14 of 46



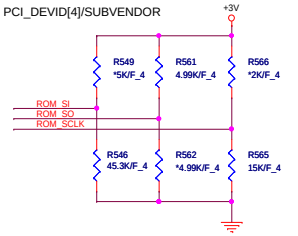
[2,4,6,9,10,11,12,14,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45]

+3V

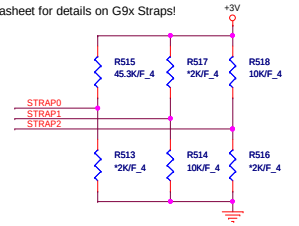
NB9P-GS (G96) Straps
NB9M-GE (G98) Straps
GPIO ASSIGNMENTS

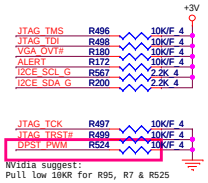
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

PCI_DEVID[4]/SUBVENDOR



SEE Datasheet for details on G9x Straps!





Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_277	TVMODE2]	TVMODE[1]	TVMODE[0]	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

Delete VGA thermal circuit

PCI_DEVID: STRAP2

NB9M-GE	**0x06E**	**8**	**1000 default**
NB9M-GS	0x06E	9	1001
NB9P-GE2	0x064	8	1000
NB9P-GS	**0x064**	**9**	**1001 default**

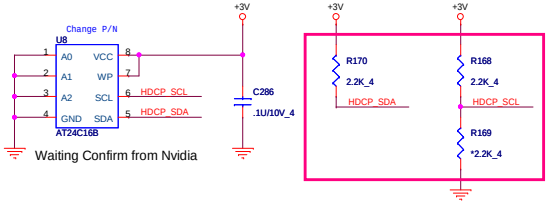
CS33572FB13 RES CHIP 35.7K 1/16W +-1%(0402)

NB9X VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix HY5PS121621CFP-25
0110	DDR2 32Mx16x8, 128bit, 512MB	Qimonda HYB18T512161B2F-25
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung K4N51163QE-ZC25
0100	DDR2 32Mx16x8, 128bit, 512MB	Nanya/Elpida
0000	DDR2 64Mx16x8, 128bit, 1GB	Hynix
0001	DDR2 64Mx16x8, 128bit, 1GB	Samsung
0010	DDR2 64Mx16x8, 128bit, 1GB	Qimonda

HDCP ROM

DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM



NVVDD Decoupling

[43] +VGACORE

+VGACORE

+VGACORE

U35F

BGA969-NVIDIA-NB9P-GS
COMMON

NVVDD

AB11	VDD_001	VDD_057	P21
AB13	VDD_002	VDD_058	P23
AB15	VDD_003	VDD_059	P25
AB17	VDD_004	VDD_060	R11
AB19	VDD_005	VDD_061	R12
AB21	VDD_006	VDD_062	R13
AB23	VDD_007	VDD_063	R14
AB25	VDD_008	VDD_064	R15
AC11	VDD_009	VDD_065	R16
AC12	VDD_010	VDD_066	R17
AC13	VDD_011	VDD_067	R18
AC14	VDD_012	VDD_068	R19
AC15	VDD_013	VDD_069	R20
AC16	VDD_014	VDD_070	R21
AC17	VDD_015	VDD_071	R22
AC18	VDD_016	VDD_072	R23
AC19	VDD_017	VDD_073	R24
AC20	VDD_018	VDD_074	R25
AC21	VDD_019	VDD_075	T12
AC22	VDD_020	VDD_076	T14
AC23	VDD_021	VDD_077	T16
AC24	VDD_022	VDD_078	T18
AC25	VDD_023	VDD_079	T20
AD12	VDD_024	VDD_080	T22
AD14	VDD_025	VDD_081	T24
AD16	VDD_026	VDD_082	V11
AD18	VDD_027	VDD_083	V13
AD22	VDD_028	VDD_084	V15
AD24	VDD_029	VDD_085	V17
L11	VDD_030	VDD_086	V19
L12	VDD_031	VDD_087	V21
L13	VDD_032	VDD_088	V23
L14	VDD_033	VDD_089	V25
L15	VDD_034	VDD_090	W11
L16	VDD_035	VDD_091	W12
L17	VDD_036	VDD_092	W13
L18	VDD_037	VDD_093	W14
L19	VDD_038	VDD_094	W15
L20	VDD_039	VDD_095	W16
L21	VDD_040	VDD_096	W17
L22	VDD_041	VDD_097	W18
L23	VDD_042	VDD_098	W19
L24	VDD_043	VDD_099	W20
L25	VDD_044	VDD_100	W21
M12	VDD_045	VDD_101	W22
M14	VDD_046	VDD_102	W23
M16	VDD_047	VDD_103	W24
M18	VDD_048	VDD_104	W25
M20	VDD_049	VDD_105	Y12
M22	VDD_050	VDD_106	Y14
M24	VDD_051	VDD_107	Y16
P11	VDD_052	VDD_108	Y18
P13	VDD_053	VDD_109	Y20
P15	VDD_054	VDD_110	Y22
P17	VDD_055	VDD_111	Y24
P19	VDD_056		

PLACE NEAR BALLS

NEAR BGA

+VGACORE

C311 .47U/6.3V_4	C268 .47U/6.3V_4	C270 .47U/6.3V_4	C259 .47U/6.3V_4	C269 .47U/6.3V_4	C297 4.7U/6.3V_6
C278 .47U/6.3V_4	C291 .47U/6.3V_4	C288 .47U/6.3V_4	C312 .47U/6.3V_4	C314 .47U/6.3V_4	C316 4.7U/6.3V_6
C274 .1U/10V_4	C313 .1U/10V_4	C290 .1U/10V_4	C315 .1U/10V_4	C295 .1U/10V_4	C266 4.7U/6.3V_6
C289 .1U/10V_4	C279 .1U/10V_4	C296 .1U/10V_4	C271 .1U/10V_4	C267 .1U/10V_4	

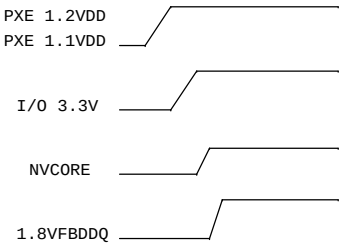
C924 330U/2.5V_6032

SI modified

Follow Design Guide DG-03276-001 4.7uFx3
and 0.47x10 uF instead of 0.1uF x10

NB9M: VGACORE +0.90V (Normal) , +1.09V

power up sequence



U35G

BGA969-NVIDIA-NB9P-GS
COMMON

GROUND

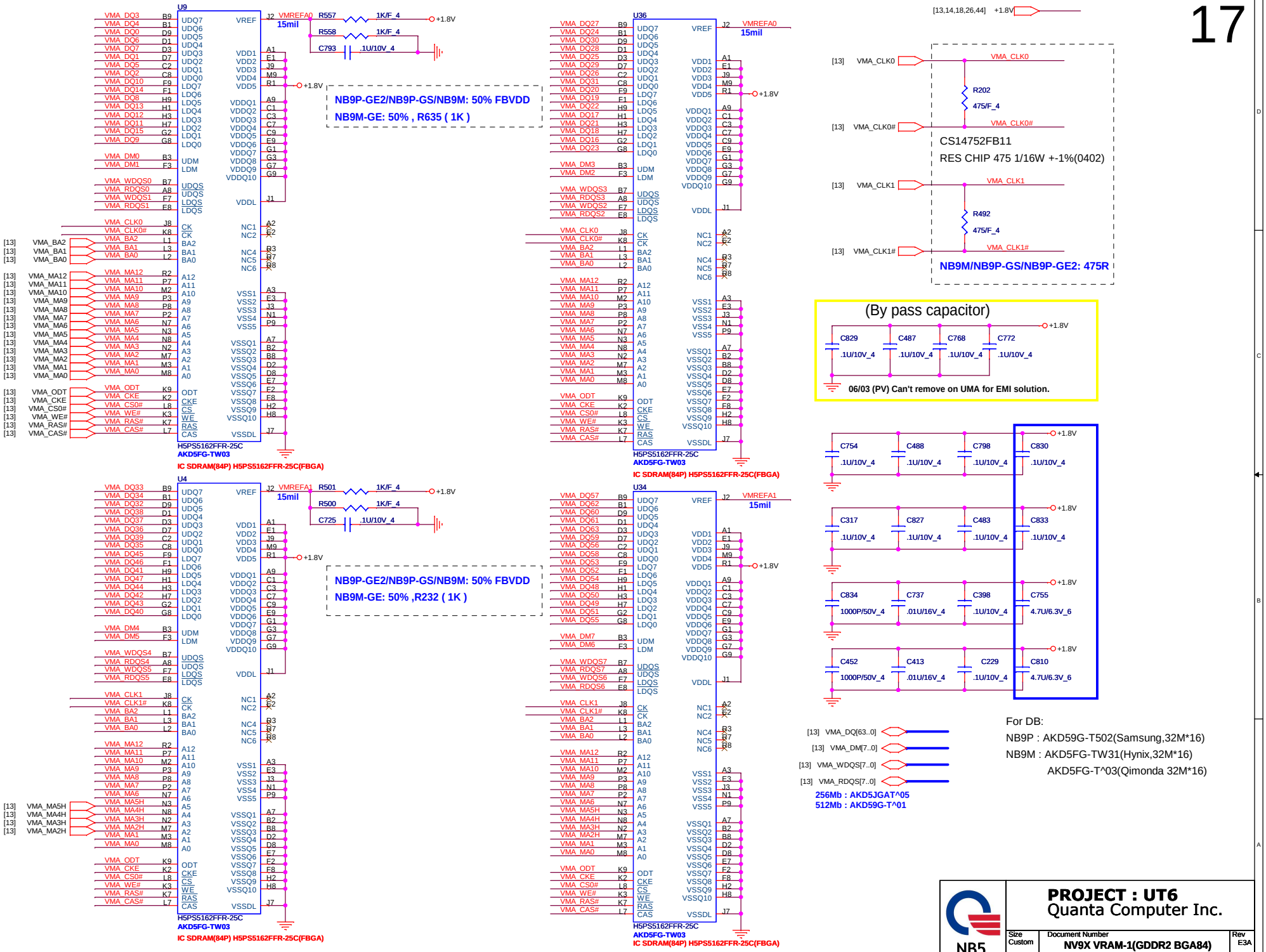
AA11	GND_1	GND_096	E15
AA12	GND_2	GND_097	E18
AA13	GND_3	GND_098	E24
AA14	GND_4	GND_099	E27
AA15	GND_5	GND_100	E30
AA16	GND_6	GND_101	E6
AA17	GND_7	GND_102	E9
AA18	GND_8	GND_103	F2
AA19	GND_9	GND_104	F31
AA2	GND_10	GND_105	F34
AA20	GND_11	GND_106	F5
AA21	GND_12	GND_107	J2
AA22	GND_13	GND_108	J31
AA23	GND_14	GND_109	J34
AA24	GND_15	GND_110	J5
AA25	GND_16	GND_111	L9
AA34	GND_17	GND_112	M11
AA5	GND_18	GND_113	M13
AB12	GND_19	GND_114	M15
AB14	GND_20	GND_115	M17
AB16	GND_21	GND_116	M19
AB18	GND_22	GND_117	M2
AB20	GND_23	GND_118	M21
AB22	GND_24	GND_119	M23
AB24	GND_25	GND_120	M25
AC9	GND_26	GND_121	M31
AD11	GND_27	GND_122	M34
AD13	GND_28	GND_123	M5
AD15	GND_29	GND_124	N11
AD17	GND_30	GND_125	N12
AD2	GND_31	GND_126	N13
AD21	GND_32	GND_127	N14
AD23	GND_33	GND_128	N15
AD25	GND_34	GND_129	N16
AD31	GND_35	GND_130	N17
AD34	GND_36	GND_131	N18
AD5	GND_37	GND_132	N19
AE11	GND_38	GND_133	N20
AE12	GND_39	GND_134	N21
AE13	GND_40	GND_135	N22
AE14	GND_41	GND_136	N23
AE15	GND_42	GND_137	N24
AE16	GND_43	GND_138	N25
AE17	GND_44	GND_139	P12
AE18	GND_45	GND_140	P14
AE19	GND_46	GND_141	P16
AE20	GND_47	GND_142	P18
AE21	GND_48	GND_143	P20
AE22	GND_49	GND_144	P22
AE23	GND_50	GND_145	P24
AE24	GND_51	GND_146	P2
AE25	GND_52	GND_147	R31
AG2	GND_53	GND_148	R34
AG31	GND_54	GND_149	R5
AG34	GND_55	GND_150	T11
AG5	GND_56	GND_151	T13
AK2	GND_57	GND_152	T15
AK31	GND_58	GND_153	T17
AK34	GND_59	GND_154	T19
AK5	GND_60	GND_155	T21
AL12	GND_61	GND_156	T23
AL15	GND_62	GND_157	T25
AL18	GND_63	GND_158	U11
AL21	GND_64	GND_159	U12
AL24	GND_65	GND_160	U13
AL27	GND_66	GND_161	U14
AL30	GND_67	GND_162	U15
AL6	GND_68	GND_163	U16
AL9	GND_69	GND_164	U17
AN2	GND_70	GND_165	U18
AN34	GND_71	GND_166	U19
AP12	GND_72	GND_167	U20
AP15	GND_73	GND_168	U21
AP18	GND_74	GND_169	U22
AP21	GND_75	GND_170	U23
AP24	GND_76	GND_171	U24
AP27	GND_77	GND_172	U25
AP3	GND_78	GND_173	V12
AP30	GND_79	GND_174	V14
AP33	GND_80	GND_175	V16
AP6	GND_081	GND_176	V18
AP9	GND_082	GND_177	V2
B12	GND_083	GND_178	V20
B15	GND_084	GND_179	V22
B21	GND_085	GND_180	V24
B24	GND_086	GND_181	V31
B27	GND_087	GND_182	V5
B3	GND_088	GND_183	V9
B30	GND_089	GND_184	Y11
B33	GND_090	GND_185	Y13
B6	GND_091	GND_186	Y15
B9	GND_092	GND_187	Y17
C2	GND_093	GND_188	Y19
C34	GND_094	GND_189	Y21
E12	GND_095	GND_190	Y23
		GND_191	Y25

NB5

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV9X (POWER & GND) 5/5	E3A

Date: Wednesday, August 06, 2008 Sheet 16 of 46



PROJECT : UT6
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	NV9X VRAM-1(GDDR2 BGA84)	E3A

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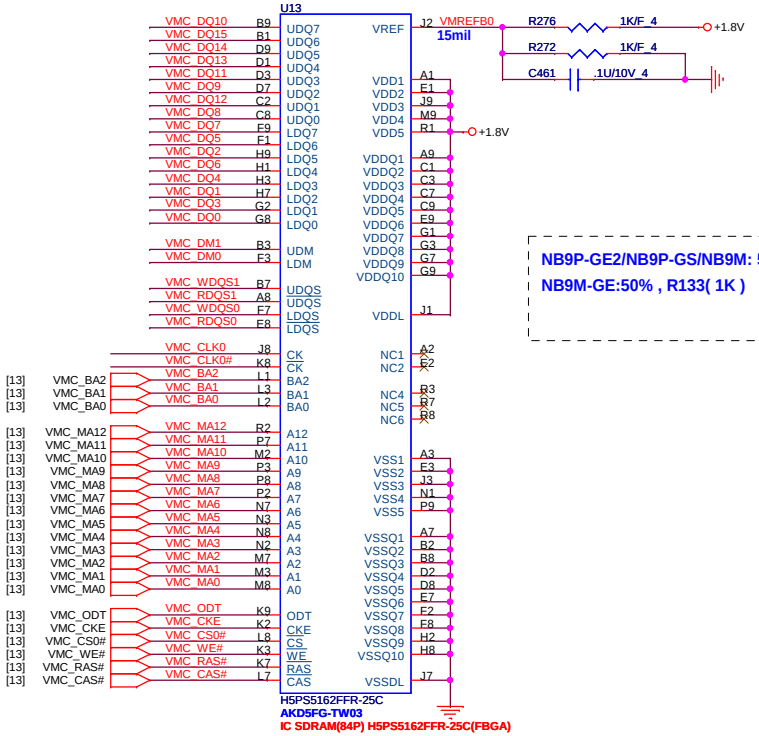
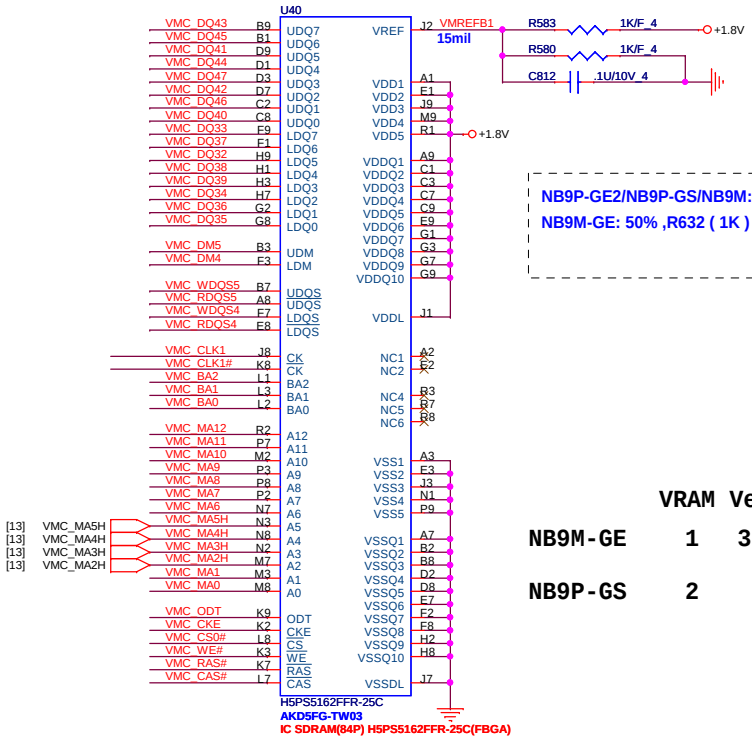
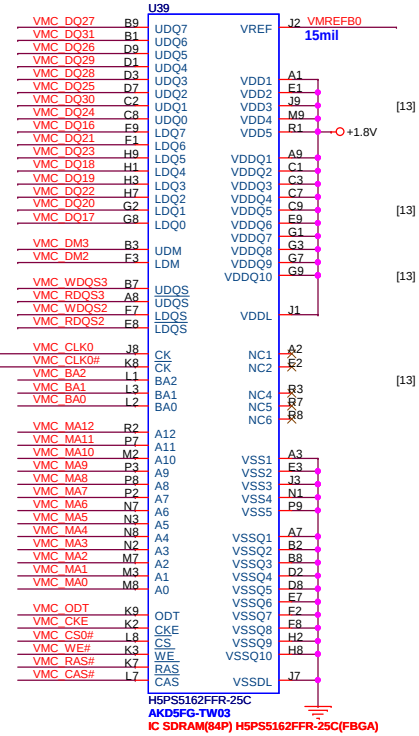
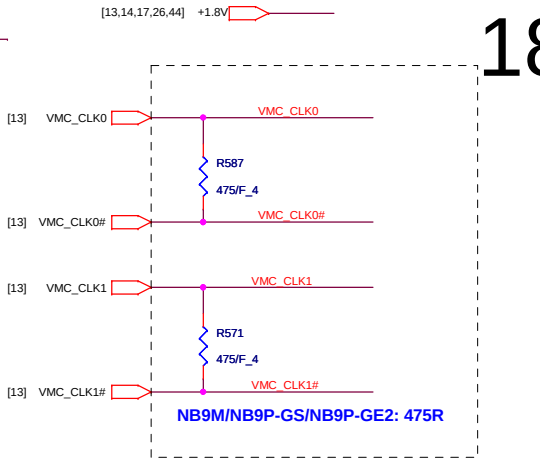
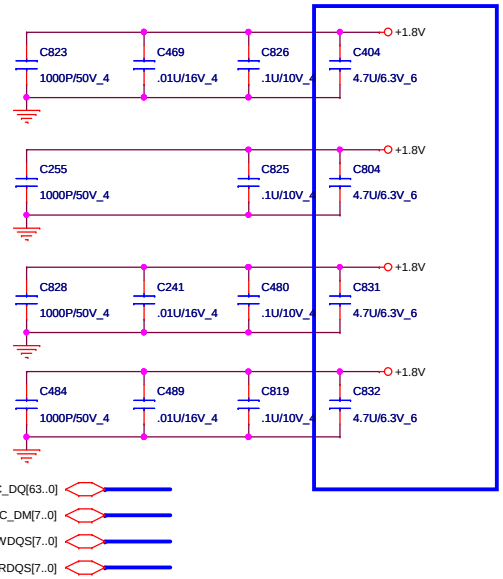


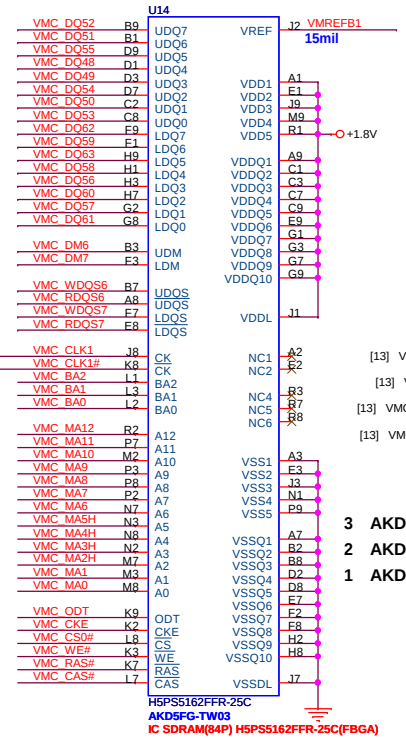






CS14752FB11 RES CHIP 475 1/16W +-1%(0402)





VRAM Vendor		
NB9M-GE	1	3
NB9P-GS	2	

3	AKD5FG-T501	IC SDRAM(84P) K4N51163QG-HC25(FBGA)	Samsung
2	AKD5FG-T^03	IC SDRAM(84P)HYB18T512161B2F-25(TFBGA)	Qimonda
1	AKD5FG-TW31	IC SDRAM(84P) HY5PS121621CFP-25(FBGA)	Hynix

NB5

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV9X VRAM-2(GDDR2 BGA84)	E3A

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1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB FOR UMA VGA

[6]	LA_CLK	RP6	*4P2R-S-0	TXLCLKOUT+	
[6]	LA_CLK#			TXLCLKOUT-	
[6]	LA_DATAP0	RP5	*4P2R-S-0	TXLOUT0+	
[6]	LA_DATAN0			TXLOUT0-	
[6]	LA_DATAP1	RP8	*4P2R-S-0	TXLOUT1+	
[6]	LA_DATAN1			TXLOUT1-	
[6]	LA_DATAP2	RP7	*4P2R-S-0	TXLOUT2+	
[6]	LA_DATAN2			TXLOUT2-	
[6]	LB_CLK#	RP1	*4P2R-S-0	TXUCLKOUT-	
[6]	LB_CLK			TXUCLKOUT+	
[6]	LB_DATAP0	RP4	*4P2R-S-0	TXUOUT0+	
[6]	LB_DATAN0			TXUOUT0-	
[6]	LB_DATAP1	RP3	*4P2R-S-0	TXUOUT1+	
[6]	LB_DATAN1			TXUOUT1-	
[6]	LB_DATAN2	RP2	*4P2R-S-0	TXUOUT2-	
[6]	LB_DATAP2			TXUOUT2+	

OPTION SIGNAL FROM Nvidia to VGA

[14]	EXT_TXLCLKOUT+	RP14	*0_4P2R/S	TXLCLKOUT+	
[14]	EXT_TXLCLKOUT-		short-4p2r-0404	TXLCLKOUT-	
[14]	EXT_TXLOUT0-	RP13	*0_4P2R/S	TXLOUT0-	
[14]	EXT_TXLOUT0+		short-4p2r-0404	TXLOUT0+	
[14]	EXT_TXLOUT1+	RP16	*0_4P2R/S	TXLOUT1+	
[14]	EXT_TXLOUT1-		short-4p2r-0404	TXLOUT1-	
[14]	EXT_TXLOUT2+	RP15	*0_4P2R/S	TXLOUT2+	
[14]	EXT_TXLOUT2-		short-4p2r-0404	TXLOUT2-	
[14]	EXT_TXUCLKOUT+	RP9	*0_4P2R/S	TXUCLKOUT+	
[14]	EXT_TXUCLKOUT-		short-4p2r-0404	TXUCLKOUT-	
[14]	EXT_TXUOUT0+	RP12	*0_4P2R/S	TXUOUT0+	
[14]	EXT_TXUOUT0-		short-4p2r-0404	TXUOUT0-	
[14]	EXT_TXUOUT1-	RP11	*0_4P2R/S	TXUOUT1-	
[14]	EXT_TXUOUT1+		short-4p2r-0404	TXUOUT1+	
[14]	EXT_TXUOUT2-	RP10	*0_4P2R/S	TXUOUT2-	
[14]	EXT_TXUOUT2+		short-4p2r-0404	TXUOUT2+	

07/14 (PV2) Change footprint for PE require.

[2,4,6,9,10,11,12,14,15,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +3V
[3,20,24,25,27,28,30,31,34,36,38,45] +5V
[29,38,39,40,41,42,43,44,45] +VIN
[21,30,31,35,36,38,39,40,45] +3VPCU
[27,30,36,40,45] +12VALW

SI modified Change part: " DFWF40MS000

+VIN_BLIGHT

+VIN — L2 FBM2125 HM330-T — +VIN_BLIGHT
C19 .1U/50V_6
C9 .01U/50V_4
C12 .1U/50V_6
C14 *10U/25V_12

SI-2 Del R9

+3VLCD_CON
+3V
[6,14,15] EDIDDATA
+LOGO_PWR
C7 1000P/50V_4
C10 1000P/50V_4
BLON_CON

CN1

		+VIN_BLIGHT	+VIN_BLIGHT
			+3VLCD_CON
		VADJ1	EDIDCLK [6,14,15]
		TXLCLKOUT+	TXUCLKOUT+
		TXLCLKOUT-	TXUCLKOUT-
		TXLOUT0+	TXUOUT0+
		TXLOUT0-	TXUOUT0-
		TXLOUT1+	TXUOUT1+
		TXLOUT1-	TXUOUT1-
		TXLOUT2+	TXUOUT2+
		TXLOUT2-	TXUOUT2-

LCD CONN
DFWF40MS003
CONN SMD WAFER 40P 2R MS(P1.0,H4.68)

SI modified

Del CN7,R88,C115
Remove Logo light2

+5V — R11 75R/F_6 — +LOGO_PWR

0090 use 100 ohm and must change back to 75ohm

[6,15] DPST_PWM — DPST_PWM — R16 *0_4

7/16 (PV2) Change FP for ICT.

[35] PWM_VADJ — PWM_VADJ — R15 *0_4/S short0402 — VADJ1

C16 *4.7U/6.3V_6
C15 .1U/10V_4

+3V — R12 2.2K_4 — EDIDCLK
R10 2.2K_4 — EDIDDATA

+12VALW
AO3404 ID current 5.8A
R23 330K_6
Q4 AO3404
+3V
C18 .1U/10V_4

+5VSUS
R26 100K/F_4
LCDONG
Q6 DTC144EUA
Q7 ME2N7002E
C22 .022U/16V_4
[6,15] DISP_ON
LCDON#
Q5 ME2N7002E

+3VLCD
L1 PBY201209T-4A/08
R18 22_8
LCDDISCHG
C8 .01U/16V_4
C11 .1U/10V_4
C13 10U/6.3V_8
+3VLCD_CON

+3VPCU
R21 33K_6
Close to EC
[6,15] LVDS_BLON — R14 1K/F_4 — PN_BLON — D7 RB501V-40 — LID_EC# [35,36]
D6 RB501V-40 — BLON_CON
[23] LCD_BK — Q3 DTC144EUA
R17 100K/F_4
C17 22P/50V_4

Nvidia suggest:
Pull low 10KR for R95, R7 & R525

DISP_ON R25 10K/F_4
LVDS_BLON R13 10K/F_4

PROJECT : UT6
Quanta Computer Inc.

NB5

Size	Document Number	Rev
B	LCD CONN/Lid function	E3A

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CRT PORT

QT6 modified

SI modified

DSUB-070546FR015SX68ZR-15P-H

40 mils

40 MIL

06/03 (PV) BOM modify for EMI solution.

SSM14 spec is 40V 1A

FUSE1A6V_POLY

EMI

CRT CONN CN16

07/14 (PV2) Change footprint for PE require.

06/03 (PV) For EMI solution.

SI modified

Change ESD protection to +5V

CRT SWITCH

U1

74CBT3257

05/23 (PV) Del for PE require.

inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

For UMA HDMI function

SI-2 change contact signal

U2

POWER

CONTROL

GND

*PI3VDP411LSZDE

EQUALIZATION SETTING

PC1:PC0=0:0	8dB
PC1:PC0=0:1	4dB Recommanded
PC1:PC0=1:0	12dB
PC1:PC0=1:1	0dB

SCL/SDAZ Low-level input/output Voltage

CFG1:CFG0=0:0	VIL:<0.4V VOL:0.6V (Default)
CFG1:CGF0=0:1	VIL:<0.36V VOL:0.55V
CFG1:CGF0=1:0	VIL:<0.44V VOL:0.65V
CFG1:CGF0=1:1	VIL:<0.36V VOL:0.6V

Only for NVIDIA

For EXT VGA

UMA : NC

NB9M-GE/NB9P-GS: 0.1uF

05/23 (PV) Short for PE require.

7/16 (PV2) Change FP for ICT.

SI modified

07/14 (PV2) Change footprint for PE require.

05/23 (PV) For UMA HDMI detect issue

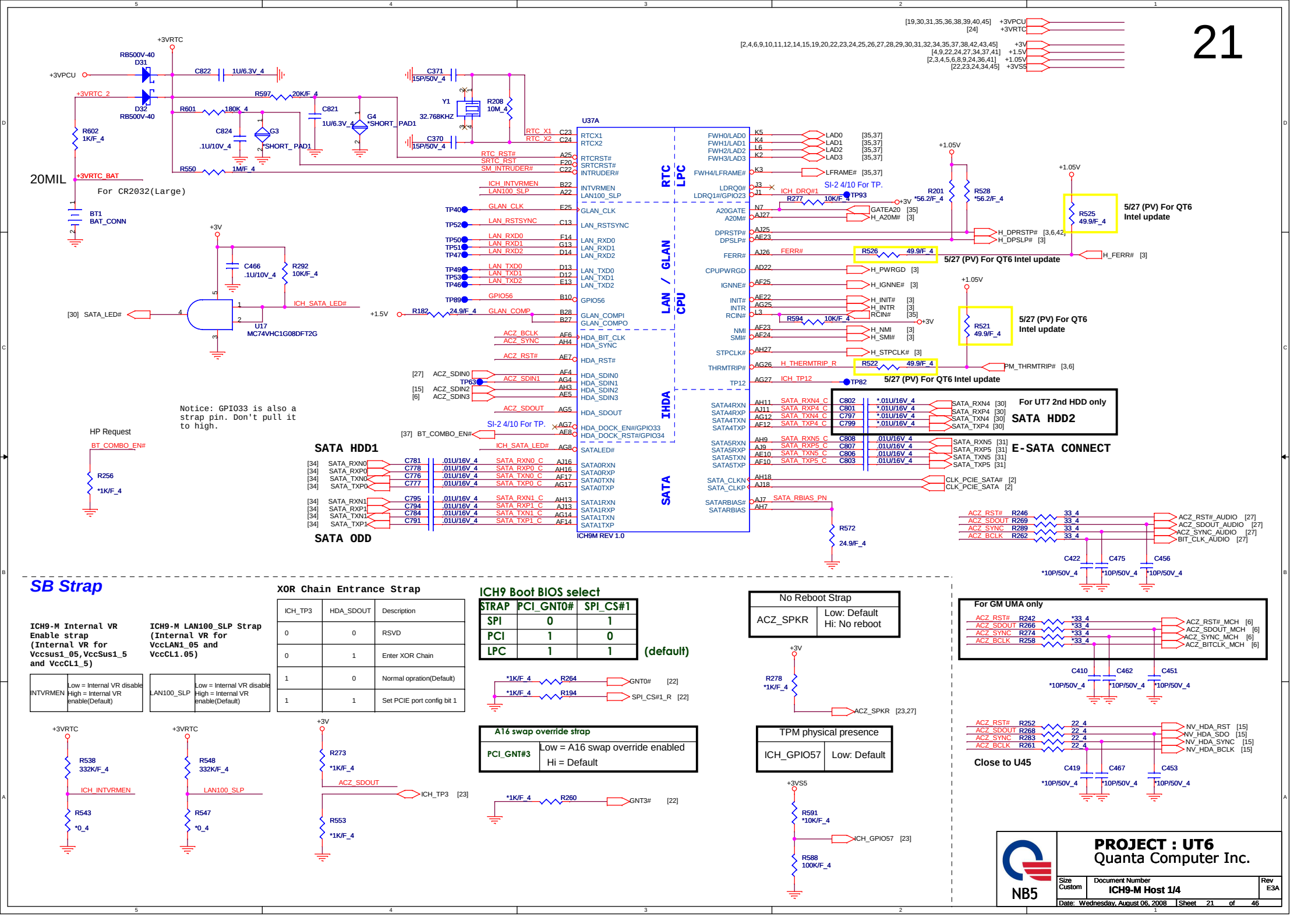
MODEL	DIS	UMA
C233	220P/50V_4	.01U/16V_4

HDMI PORT

HDMI CONN

for EMI request

SI modified



SB Strap

ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

TPM physical presence	
ICH_GPIO57	Low: Default

For GM UMA only

Close to U45

PROJECT : UT6
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	ICH9-M Host 1/4	E3A

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SWAP PCIE PORT6 to PORT2 (Lan and New card swap) -->Rename the port name by function and port

MINI CARD PCI-E(WLAN)

PCIE-LAN

MINI CARD PCI-E (ROBSAN)

TV CARD PCI-E

FireWire PCI-E

EXPRESS CARD (NEW CARD)

07/09 (PV2) Del C761,C762, add TP98, TP99 for no support ROBSON card.

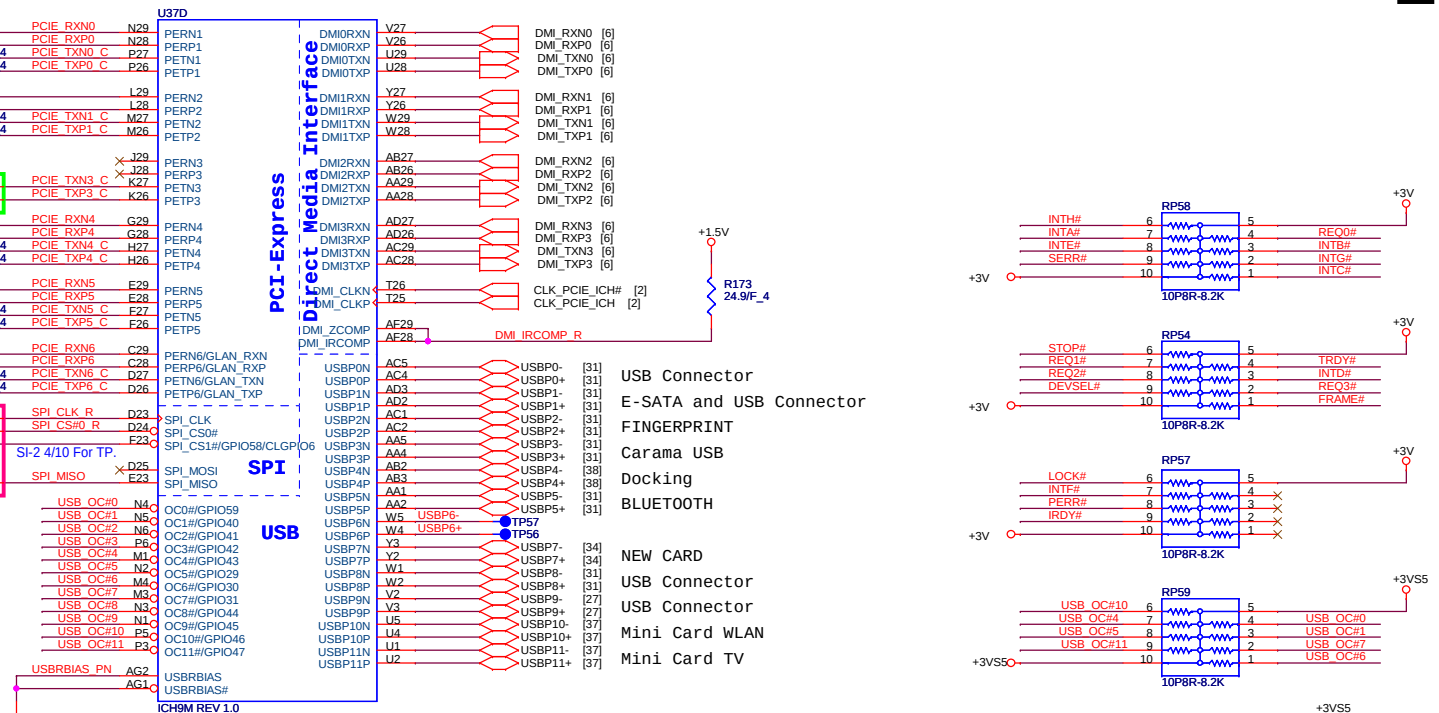
SI modified

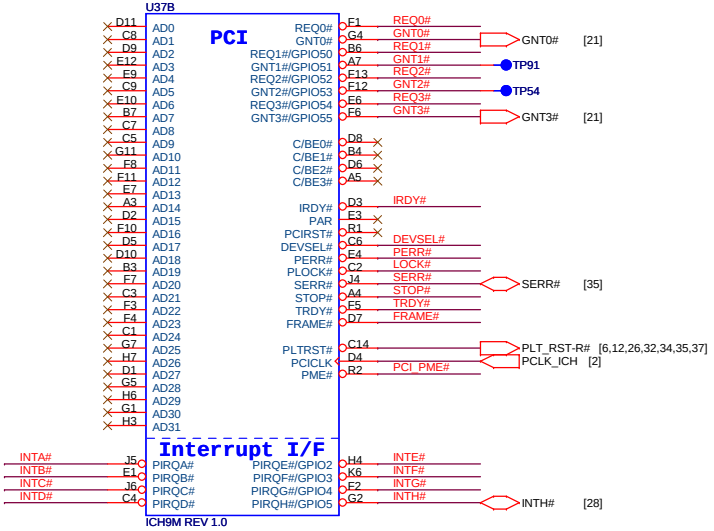
Del GM HDCP circuit

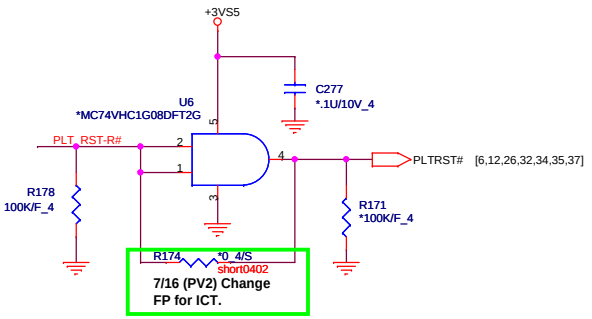
Del U16,R297,R285,R275, R291,R286,C476C478,R294

512K byte SPI ROM
For HDCP only

For GM HDCP







NB5	**PROJECT : UT6** Quanta Computer Inc.
Size: Custom	Document Number: ICH9-M PCIE 2/4
Rev: E3A	
Date: Wednesday, August 06, 2008	Sheet 22 of 46

[2,4,6,9,10,11,12,14,15,19,20,21,22,24,25,26,27,28,29,30,31,32,34,35,37,38,42,43,45] +3V
[21,22,24,34,45] +3VS5
[31,37,41,42,43,45] +3VSUS

U37C

SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M REV 1.0

SI modified
Del T18,TP84,TP86

07/09 (PV2) Add TP95 for no support ROBSON card.

SI-2 Build
Delete R574,G2 as Bios_Rec can be cover by Bios

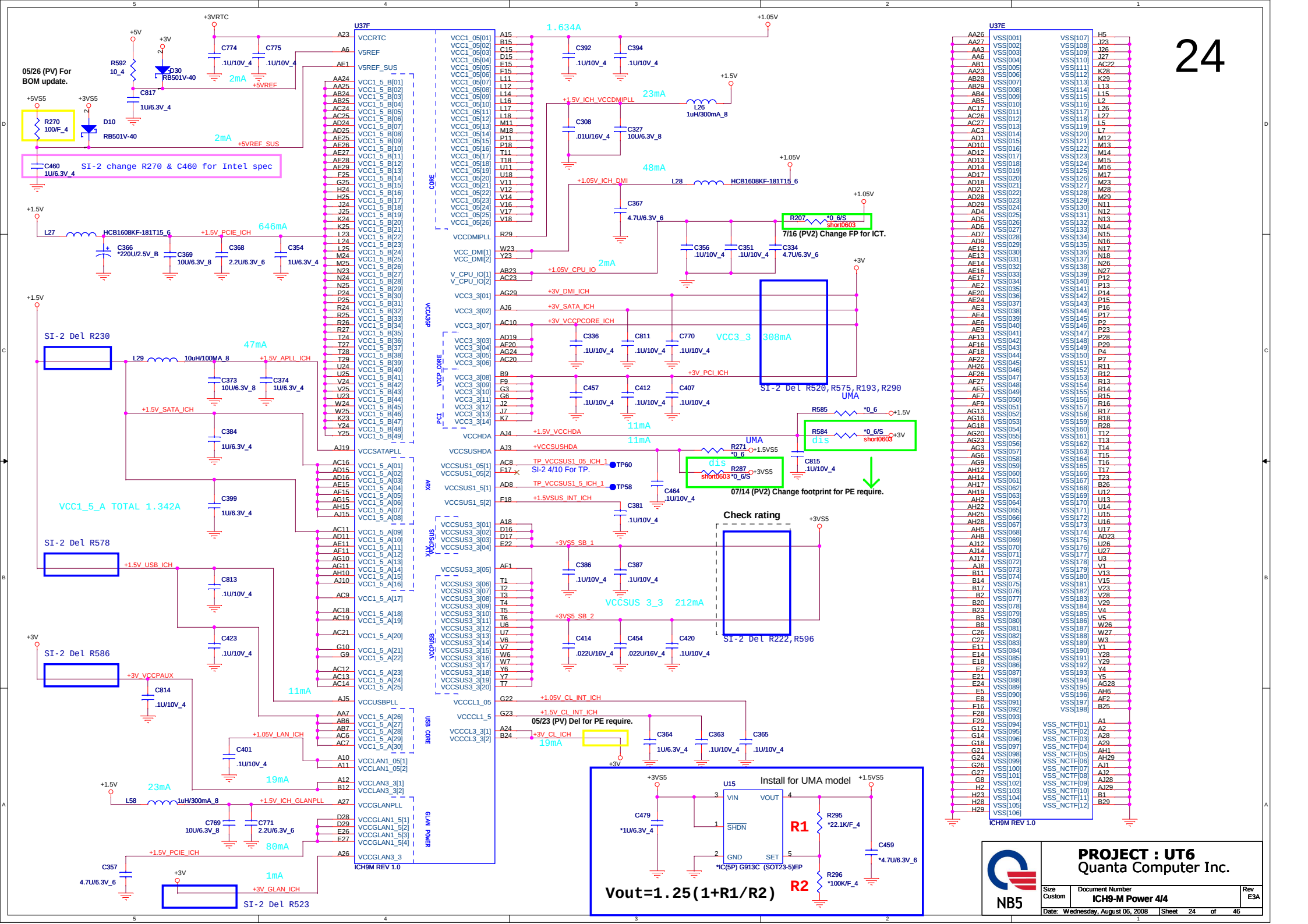
05/28 (PV) For EA measure.

Discrete / UMA

Board ID 0: 1-->Discrete , 0-->UMA
Board ID 1: 1- - >18.4" , 0- - >16.0"
Board ID 2: 1-- >MXM, 0-- >non-MXM
Board ID 3: 1-- >HDX, 0-- > non-HDX
Board ID 4
Board ID 5

7/16 (PV2) Change FP for ICT.

PROJECT : UT6
Quanta Computer Inc.
NB5
Size Custom | Document Number ICH9-M GPIO 3/4 | Rev E3A
Date: Wednesday, August 06, 2008 | Sheet 23 of 46


05/26 (PV) For BOM update.
SI-2 change R270 & C460 for Intel spec
SI-2 Del R230
SI-2 Del R578
SI-2 Del R586
SI-2 Del R523
SI-2 Del R520,R575,R193,R290
SI-2 Del R222,R596
VCC1_5_A TOTAL 1.342A
VCC3_3 308mA
VCCSUS 3_3 212mA
UMA
dis
Check rating
07/14 (PV2) Change footprint for PE require.
7/16 (PV2) Change FP for ICT.
05/23 (PV) Del for PE require.
Install for UMA model
Vout=1.25(1+R1/R2)
*IC(5P) G913C (SOT23-5)EP
U37F
U37E
ICH9M REV 1.0
PROJECT : UT6
Quanta Computer Inc.
NB5
ICH9-M Power 4/4
Size Custom
Document Number
Rev E3A
Date: Wednesday, August 06, 2008
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MV modify short pad

JMB_SD/MS_CLK — R638 *0_4/S short0402 — SD_MS_CLK

Delete JMB 385

D40 RB501V-40 — MS_CD# — MS_CD# [26]

D38 RB501V-40 — SD_CD# — SD_CD# [26]

XD_CD# — C864 270P/50V_4

Close to CN34

+3VCARD — CLOSE CONN — +3VCARD

C862 4.7U/6.3V_6 — R631 150K/F_4 — C867 .1U/10V_4 — C866 .1U/10V_4 — C863 .1U/10V_4

	SD/MMC	MS	XD
MDID0	SD_DAT0	MS_D0	XD_D0
MDID1	SD_DAT1	MS_D1	XD_D1
MDID2	SD_DAT2	MS_D2	XD_D2
MDID3	SD_DAT3	MS_D3	XD_D3
MDID4	SD_CMD	MS_BS	XD_WE#
MDID5	SD_CLK	MS_SCLK	XD_CE#
MDID6	SD_WP		XD_WP#
MDID7			XD_CLE
MDID8	SD_DAT4		XD_D4
MDID9	SD_DAT5		XD_D5
MDID10	SD_DAT6		XD_D6
MDID11	SD_DAT7		XD_D7
MDID12			XD_RE#
MDID13			XD_R/B#
MDID14			XD_ALE
CR1_LEDN	SD1_LED#	MS1_LED#	XD_LED#
CR1_PCTLN	SD1_PCTL#	MS1_PCTL#	XD1_PCTL#
CR1_CD0	SD1_CD#		XD_CV#
CR1_CD1		MS1_CD#	XD_CD#

5 IN1 CARD READER
XD,MMC/SD,MS/MSP

C874 *270P/25V_4 — MV modify short pad — +3VCARD — R632 *10K/F_4 — XD-WP# — R633 *0_6/S short0603 — XD-WP# L

CN32 — *5IN1 CARD READER SOCKET

1	XD-R/B	GND	37
2	XD-RE	GND	38
3	XD-CE	GND	40
4	XD-CLE	GND	42
5	XD-ALE	GND	43
6	XD-WE		
7	XD-WP	SD-C/D	39
8	XD-DATA0	SD-CD-SW	36
9	XD-DATA1	SD-W/P	41
10	SD-DATA2	SD-WP-SW	35
11	SD-DAT3	XD-CD	34
12	SD-CMD	XD-VCC	33
13	GND	XD-DATA7	32
14	MS-VCC	XD-DATA6	31
15	MS-SDLK	XD-DATA5	30
16	MS-DATA3	XD-DATA1	29
17	MS-INS	XD-DATA4	28
18	MS-DATA2	XD-DATA3	27
19	MS-DATA0	XD-DATA2	26
20	MS-DATA1	SD-DATA0	25
21	MS-BS	SD-CLK	24
22	GND	SD-VCC	23

XD-RB# XD-RE# XD-CE# XD-CLE XD-ALE XD_WE XD-WP# L XD-D0 XD-D1 SD_DAT2 SD_DAT3 SD_CMD

SD_MS_CLK MS_DATA3 MS_CD# MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 MS_DATA1 MS_BS

SD_CD# SD_CD# SD_WP SD_WP XD_CD# XD-D7 XD-D6 XD-D5 SD_DAT1 XD-D4 XD-D3 MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 SD_MS_CLK

C865 *270P/25V_4

SI modified Footprint: "4in1-72700327123-43p-l"

7/16 (PV2) Delete net for ICT.

7/16 (PV2) Change FP for ICT.

[26]	MDIO00	R404 *0_4/S short0402	R386 *0_4/S short0402	MS_DATA0_SD_DAT0 / XD-D0
[26]	MDIO01	R399 *0_4/S short0402	R403 *0_4/S short0402 / R392 *0_4/S short0402	SD_DAT1 / MS_DATA1 / XD-D1
[26]	MDIO02	R405 *0_4/S short0402	R409 *0_4/S short0402	MS_DATA2_XD_D2 / SD_DAT2
[26]	MDIO03	R406 *0_4/S short0402	R408 *0_4/S short0402 / R401 *0_4/S short0402	MS_DATA3 / SD_DAT3 / XD-D3
[26]	MDIO04	R407 *0_4/S short0402	R402 *0_4/S short0402 / R377 *0_4/S short0402	SD_CMD / MS_BS / XD_WE
[26]	MDIO05	R358 22_4	R367 22_4	JMB_SD/MS_CLK / XD-CE#
[26]	MDIO06	R395 *0_4/S short0402	R382 *0_4/S short0402	SD_WP / XD-WP#
[26]	MDIO07	R370 *0_4/S short0402		XD-CLE
[26]	MDIO08	R400 *0_4/S short0402		XD-D4
[26]	MDIO09	R398 *0_4/S short0402		XD-D5
[26]	MDIO10	R397 *0_4/S short0402		XD-D6
[26]	MDIO11	R396 *0_4/S short0402		XD-D7
[26]	MDIO12	R350 *0_4/S short0402		XD-RE#
[26]	MDIO13	R347 *0_4/S short0402		XD-RB#
[26]	MDIO14	R375 *0_4/S short0402		XD-ALE

2ND SOURCE

+3VCARD — CN33 — TAI TWUM 5IN1 CARD READER SOCKET — +3VCARD

1	xD-R/B	GND	37
2	xD-RE	GND	38
3	xD-CE	GND	41
4	xD-CLE	GND	42
5	xD-ALE		
6	xD-WE	NC	40
7	xD-WP	NC	39
8	xD-D0		
9	xD-D1		
10	SD-DAT2	SD-CD	36
11	SD-DAT3	SD-WP	35
12	SD-CMD	xD-CD	34
13	GND	xD-VCC	33
14	MS-VCC	xD-D7	32
15	MS-SDLK	xD-D6	31
16	MS-DATA3	xD-D5	30
17	MS-INS	SD-DAT1	29
18	MS-DATA2	xD-D4	28
19	MS-DATA0	xD-D3	27
20	MS-DATA1	xD-D2	26
21	MS-BS	SD-DAT0	25
22	GND	SD-CLK	24
		SD-VCC	23

XD-RB# XD-RE# XD-CE# XD-CLE XD-ALE XD_WE XD-WP# L XD-D0 XD-D1 SD_DAT2 SD_DAT3 SD_CMD

SD_MS_CLK MS_DATA3 MS_CD# MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 MS_DATA1 MS_BS

SD_CD# SD_WP XD_CD# XD-D7 XD-D6 XD-D5 SD_DAT1 XD-D4 XD-D3 MS_DATA2_XD_D2 MS_DATA0_SD_DAT0 SD_MS_CLK

SI modified Footprint: "7IN1-R015-B11-LM-42P-L"

+3V — Q34 *ME2307 — +3VCARD

[26] MC_PWR_CTRL_0# — R629 *10K/F_4 — +5V

20mils — R630 *0_8/S short0805 — +3VCARD — 30mils

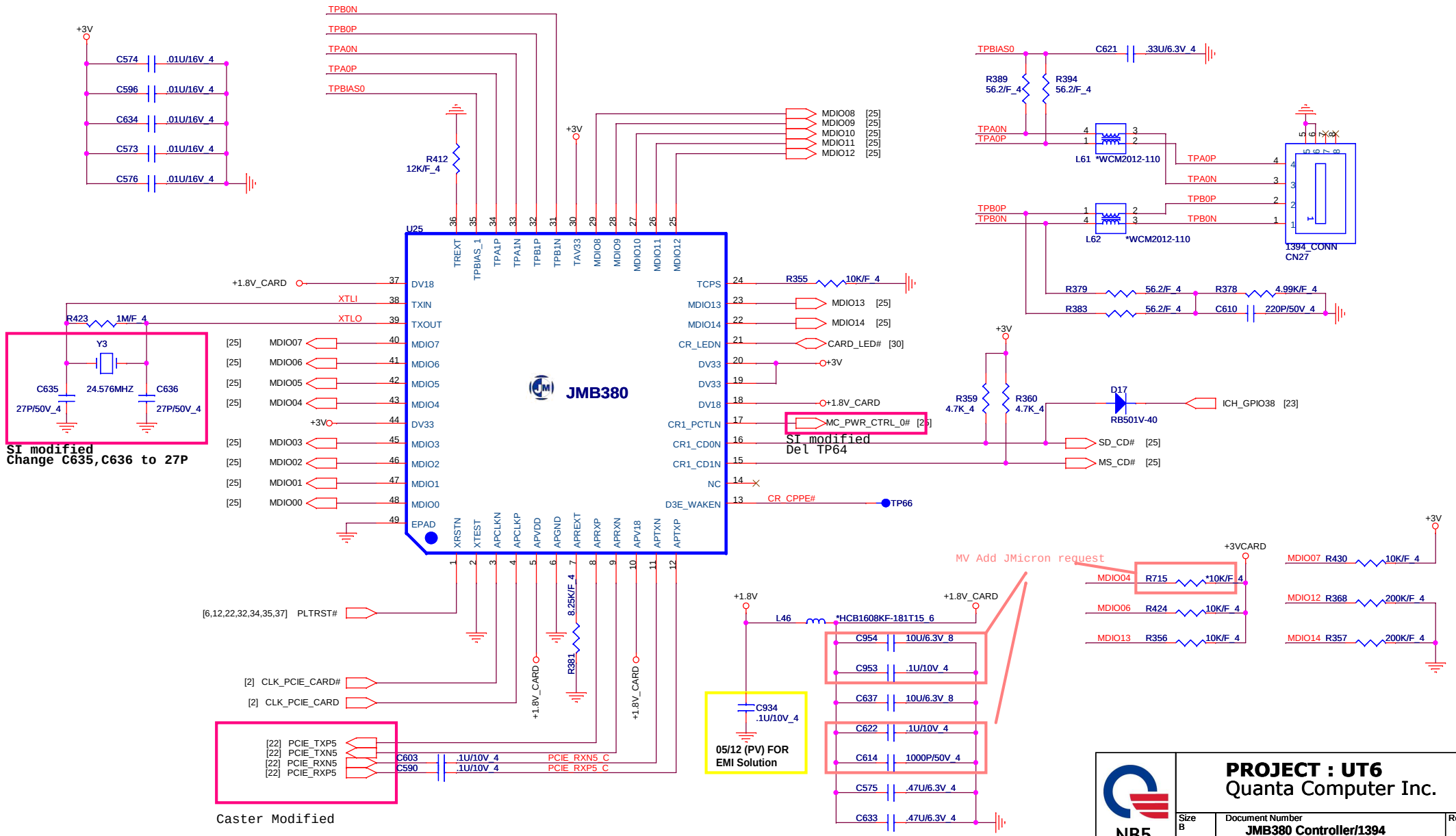
07/14 (PV2) Change footprint for PE require.

NB5

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CardReader SOCKET	E3A

Date: Wednesday, August 06, 2008 | Sheet 25 of 46



NB5

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
B	JMB380 Controller/1394	E3A
Date: Thursday, August 07, 2008	Sheet 26 of 46	

05/23 (PV) For IDT Dolby functionality.
07/14 (PV2) R697 change footprint for PE require.

06/03 (PV) For EMI solution.

QT6 Modified-0117
C762,C763 10P

UMA

07/14 (PV2) Change footprint for PE require.

Close to Pin1

Close to Pin38

Close to Pin9

IDT

92HP61B7X5NLGXA1X

TO Headphone jack

TO Audio Jack Sub Woofer

TO Internal Speakers

SI-2 Del R363,R369,R372

TO Audio Jack MIC

TO DOCKING MIC

Relying directly on ground closure at the jack can introduce errors due to differences in ground potential between CODEC and Dock as well as and noise pickup.

PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	Docking MIC
PORT F	X
DM	DIGITAL MIC

07/14 (PV2) Add R713 for Audio power timing.

SI-2 Del L44

Vset=1.242V

SI modified

TO AUDIO/B CON.

05/12 (PV) FOR EMI Solution

SI modified

SI-2 Del L45

IDT modified

QT6 Modified-0117
R485,R499 Reserve

07/14 (PV2) Change footprint for PE require.

SI-2 EMI requests Add

05/20 (PV) FOR Audio noise.

05/20 (PV) FOR HP recommend.

SI-II Add solve docking noise

TO DOCK Headphone

DOCK MIC DETECT

SA_A# -->EXT HP
SA_B# -->EXT MIC
SB_E#--> DOCK MIC
Audio JACK: Normal Open

PROJECT : UT6
Quanta Computer Inc.

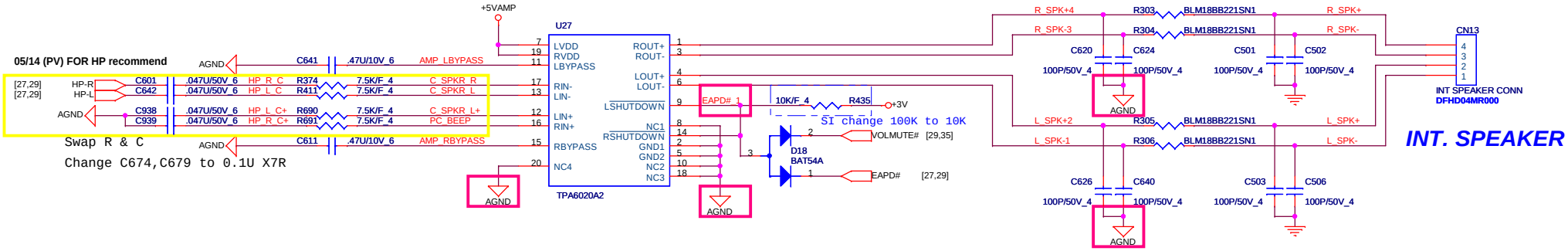
NB5

Size	Document Number	Rev
Custom	Azalia IDT92HD71B7	E3A
Date: Wednesday, August 06, 2008	Sheet 27 of 46	

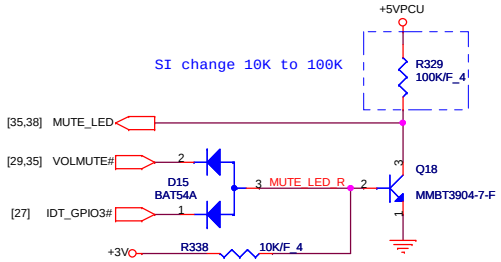
AUDIO AMPLIFIER

+3V [2,4,6,9,10,11,12,14,15,19,20,21,22,23,24,25,26,27,29,30,31,32,34,35,37,38,42,43,45]
+5V [3,19,20,24,25,27,30,31,34,36,38,45]
+5VPCU [27,35,40,41,42,43,44,45]
+5VAMP [29]

CONN SMD HEADER 4P 1R MR(P1.25,H1.95)

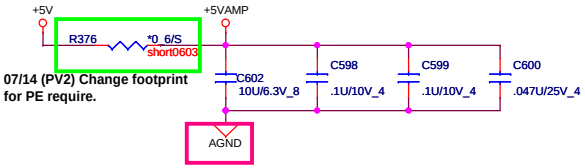


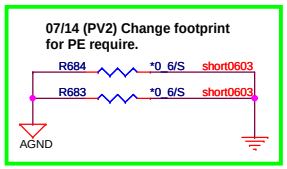
INT. SPEAKER



07/09 (PV2) Delete for 2ND FAN function.

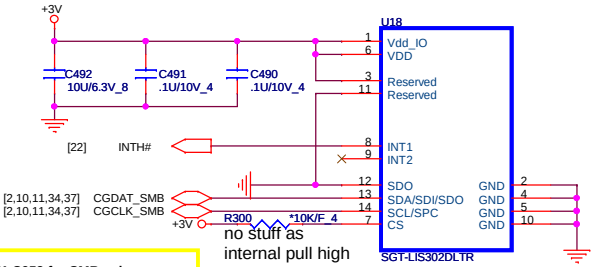
Delete Gain set



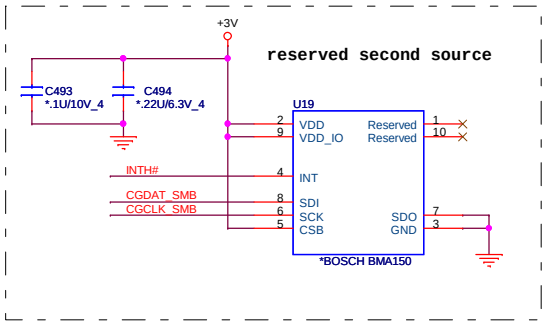


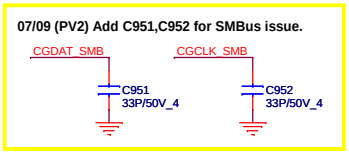
Del R373,R677,R676
Del AMP_GND to AGND

Accelerometer Sensor



Modified footprint to "SENSOR-3-8-14P-QT8"
SI modified





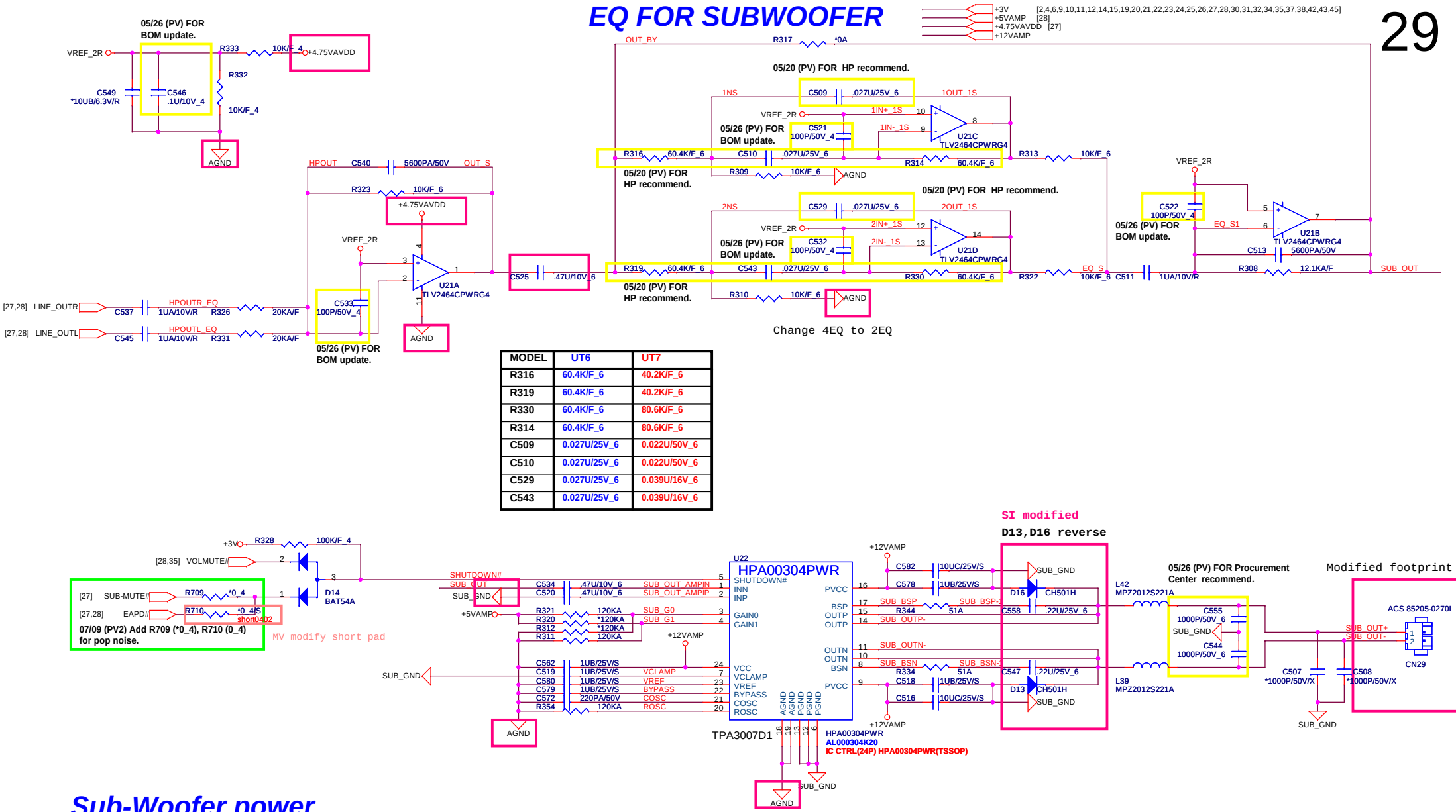
NB5

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA6017/Accelerometer	E3A

Date: Wednesday, August 06, 2008 | Sheet 28 of 46

EQ FOR SUBWOOFER



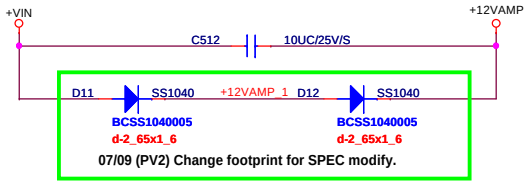
Change 4EQ to 2EQ

MODEL	UT6	UT7
R316	60.4K/F_6	40.2K/F_6
R319	60.4K/F_6	40.2K/F_6
R330	60.4K/F_6	80.6K/F_6
R314	60.4K/F_6	80.6K/F_6
C509	0.027U/25V_6	0.022U/50V_6
C510	0.027U/25V_6	0.022U/50V_6
C529	0.027U/25V_6	0.039U/16V_6
C543	0.027U/25V_6	0.039U/16V_6

SI modified

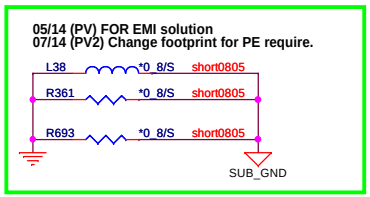
D13,D16 reverse

Sub-Woofer power



Del HP_GND to GND
Del R307,R315

Delete L1003



PROJECT : UT6
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	SUBWOOFER(EQ & AMP.)	E3A

Date: Wednesday, August 06, 2008 Sheet 29 of 46

SATA_2 CONNECTOR

DC Current rating: 0.5 A

CN34 *SATA HDD(1ST)

Main HDD

+5V: 2 A(4 Pin)
+3V: 2 A(4 Pin)
Gnd : (5 Pin)

+5V_HDD2 +5V
SI-2 Del R345

+3V_HDD2 +3V
R673 *0_8

SATA_TXP4 [21]
SATA_TXN4 [21]
SATA_RXN4 [21]
SATA_RXP4 [21]

+3V_HDD2
+5V_HDD2

FOR UT7 2ND HDD ONLY.

+5V_HDD2
C566 *10U/6.3V_8
C591 *4.7U/6.3V_6
C586 *.1U/10V_4
C581 *10U/6.3V_8

+3V_HDD2
C914 *10U/6.3V_8
C917 *.1U/10V_4

+3VPCU_LED [36]
+3V_LED [35]
+5V [3,19,20,24,25,27,28,31,34,36,38,45]
+3V [2,4,6,9,10,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,31,32,34,35,37,38,42,43,45]
+12VALW [19,27,36,40,45]

M/B Screw Hole

H1 H9 H14 H10 H19 H22 H21 H23 H15 H7 H4 — *H-S315D110P2
H13 H12 H11 H6 H8 H5 — *H-C256D165P2
H24 H25 — *H-r015x134d114x94p2 / *H-c986f59p2
PAD2 EMI
H26 — *H-r015x134d114x94p2
H18 H20 — *H-C256D150P2 / *H-C283D150P2
H2 H3 — *H-C256D110P2 / *H-C236D110P2

SI modified
MV Add for EMI Request
SI Add for UT7 odd NUT

delete all PAD & change screw footprint

07/14 (PV2) Delete H16,H17 for no support ROBSON card.

PAD1 *pad-re236x394np
05/19 (PV) FOR EMI solution

05/19 (PV) FOR M/E recommend for UT7 BAT NUT

SI modified
LED5 change type 朝上 4 pin
MV LED5 change type 朝前 3 pin

[23] ACCLED_EN
Q30 DTC144EUA
+3V [21] SATA_LED#
R425 *10K/F_4
Q24
[35] LEDVCC_EN#
*DTC144EUA
Q23 *DTC144EUA
200/F_6 R685 SATA_R_LED2
0_6 R426 SATA_R_LED1
朝前 (Amber)
LED 3P WHITE/AMBER LED5
R714 39_6 +3V
(White) MV modify

SI modified
LED3,4,6 change type 朝上 2 pin

[35,36] PWR_LED#
[35] MBATLED0#
[26] CARD_LED#
[35] CAPSLED#
朝前 LED3 3P WHITE LED PWR_R_LED1 R432 39_6 +3VPCU_LED
朝前 LED4 3P WHITE LED MBAT_R_LED1 R433 39_6 +3VPCU_LED
MV modify
朝上 LED6 2P WHITE CARD_LED1 R678 39_6 +3V
朝上 LED2 2P WHITE CAP_LED R158 39_6 +3V_LED
for U6 CAPS LOCK led
朝上 LED1 *2P WHITE CAP_LED R140 *39_6 +3V_LED
for UT7 CAPS LOCK led

07/09 (PV2) Add R703,R704,R705, remove Q21,Q22,Q25,Q26, R391,R393, C627,C639 for HP LED SPEC change.

+12VALW
R391 *100K/F_4
R704 *0_8/S short0805
+3V
Q26 *ME2N7002E
+3V_LED
20~40mils
R393 *1M/F_4 LED_CTL
[35] LEDVCC_EN#
Q22 *ME2N7002E
C627 *.22U/25V_6
C639 *1U/25V_8
C630 *.22U/25V_6
C638 10U/6.3V_8
C647 .1U/10V_4

LED PWR CONTROL

R705 *0_8/S short0805
+3VPCU
Q21 *ME2N7002E
LED_CTL
+3VPCU_LED
20~40mils
C625 10U/6.3V_8
C628 .1U/10V_4

R703 *0_8/S short0805
+5V
Q25 *AO3404
LED_CTL
+5V_LED
20~40mils
C629 .1U/10V_4
Change Q25 to AO3404 as LED current limited

NB5

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED & 2nd HDD & Hole	E3A

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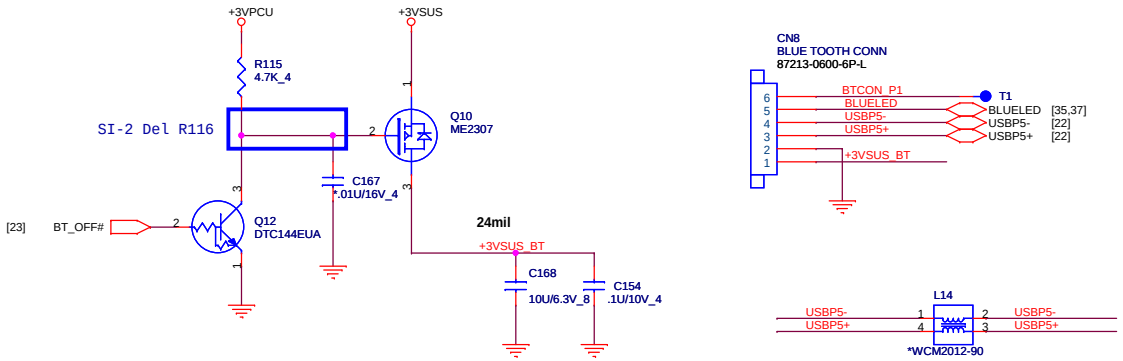
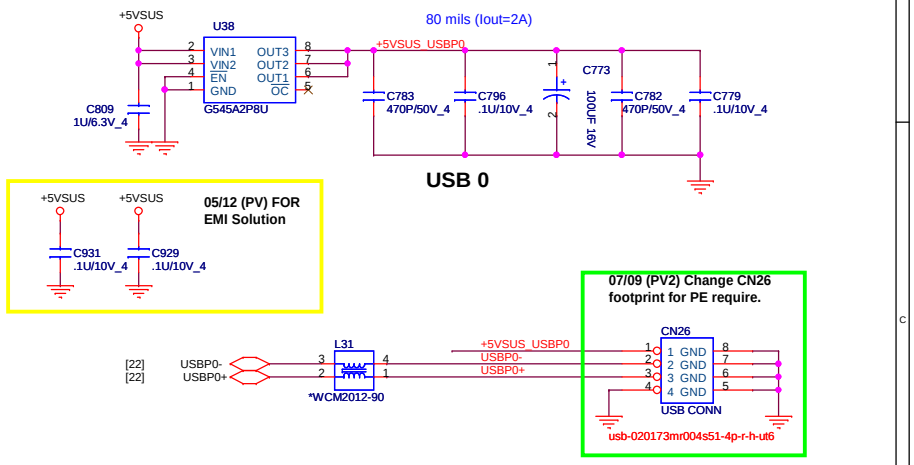
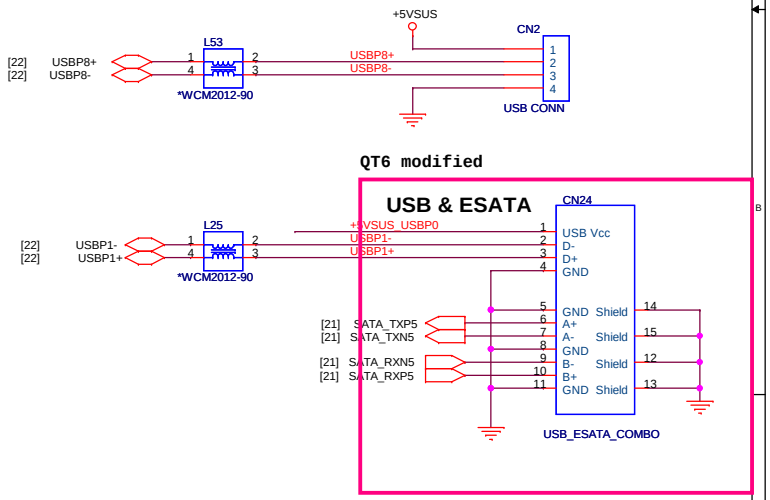
BLUETOOTH

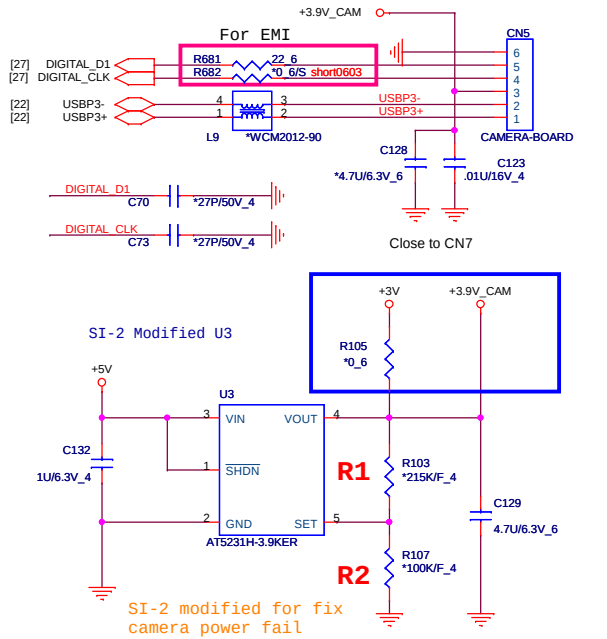


USBX1 and E-SATA

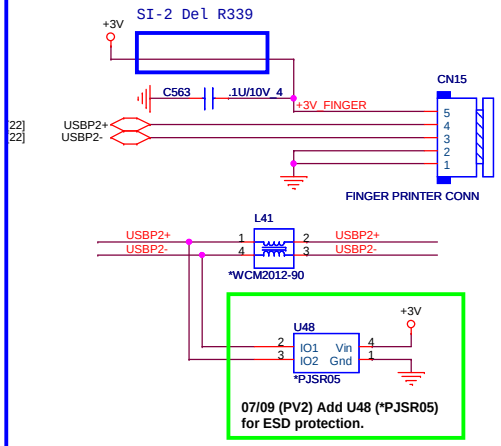




USB CAMERA /DIGITAL MIC CONNECT



USB fingerprint CON



1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/WC/FT/TS/ESATA/USB	E3A

NB5

Date: Wednesday, August 06, 2008 Sheet 31 of 46

T : Stuffed for RTL8111C(10/100/1000)

+3V +LAN_E1.8 [2,4,6,9,10,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,34,35,37,38,42,43,45] [33]

+LAN_D1.5 +LAN_D1.5_SRVDD
05/23 (PV) Del for PE require.
T26 +LAN_D1.5_CLKREQ
Stuffed for 8102E/RTL8111C

+3VLANVCC +3V_GVDD
[33] +FB12 +LAN_A1.8_FB12
05/23 (PV) Del for PE require.
05/23 (PV) Del for PE require.
Power trace Layout 寬度> 40mil
C905 10U/6.3V_8 C906 10U/6.3V_8 C898 .1U/10V_4
Stuffed for RTL8111C(10/100/1000)

7/16 (PV2) Change FP for ICT.
R653 *0_4/S short0402

for 93C56 used. NC if 93C46 is used.

Y6 25MHZ C913 33P/50V_4 C912 33P/50V_4
SI modified
Change C913,C912 to 33P

7/16 (PV2) Delete C899 for LAN Power placement.

U18#63 wider than 40 mils
U18#1 wider than 60 mils

U43 RTL8111C-VB-GR Pin 65

Isolate pull low:
1.Can only disable RTL8111C.
2.RTL8101E can't disable

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

R640 *1K/F_4 05/16 (PV) BOM modify for Power saving.
R643 100/F_4
D43 *RB501V-40 SI modified
R648 15K/F_4

SI-2 Del R647
SI-2 Del R649

U46 *M93C46-WMN6TP
R657 *10K/F_4
R658 3.65K/F_4
C897 *.1U/10V_4

07/14 (PV2) Change footprint for PE require.
07/16 (PV2) Delete R637 for ICT.
R636 *0_4/S short0402

C890 .1U/10V_4

T24 T25

R634 *0_4
R635 *0_4/S short0402
7/16 (PV2) Change FP for ICT.

AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)

Caster Modified

U41 NS892402
C857 C856 C855 C854 .01U/16V_4 V_DAC
C845 C842 C844 C843 .01U/100V_6
R606 R605 R608 R607 75/F_4
C841 1000P/3KV_1808

NS892402:GIGABIT

DB0AT9LAN05

SI modified FOR EMI
RJ45
CN20
C134 .1U/10V_4
R109 R97 330/F_4
SI Build
FOR EMI
C120 .1U/10V_4 SI modified
RJ45_CONN
DFTJ12FR038
rj45-jm3611a-n3423-7f-8p-rdv-v
05/16 (PV) Change footprint for SMT line & M/E recommend

D42 BAT54A
D41 RB501V-40
R84 *0_4/S short0402
07/14 (PV2) Change footprint for PE require.
C918 C81 *.01U/16V_4
Link

NB5

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8111C & RJ45	E3A

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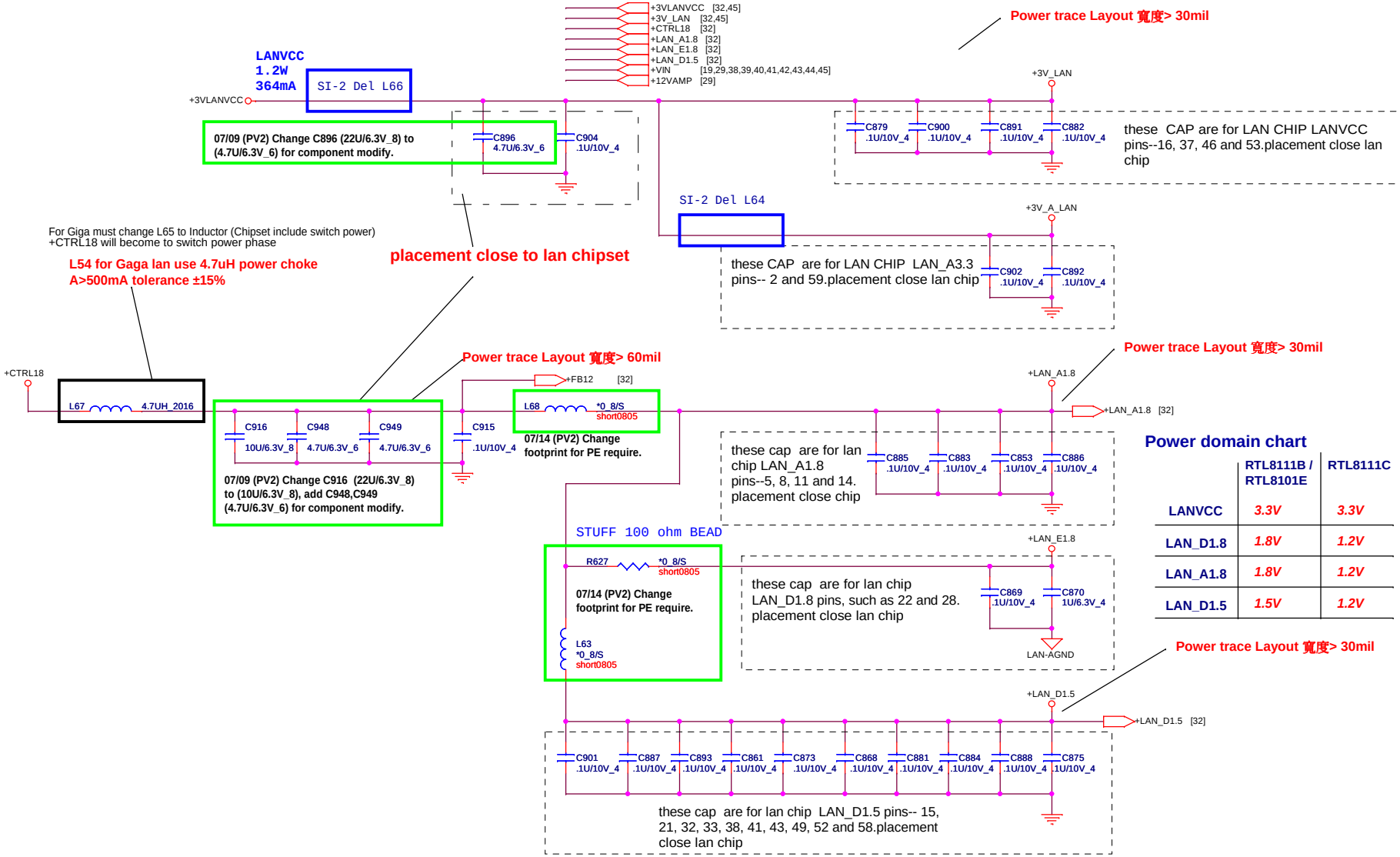

Power domain chart

	RTL8111B / RTL8101E	RTL8111C
LANVCC	3.3V	3.3V
LAN_D1.8	1.8V	1.2V
LAN_A1.8	1.8V	1.2V
LAN_D1.5	1.5V	1.2V

NB5

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
A3	LAN Power	E3A

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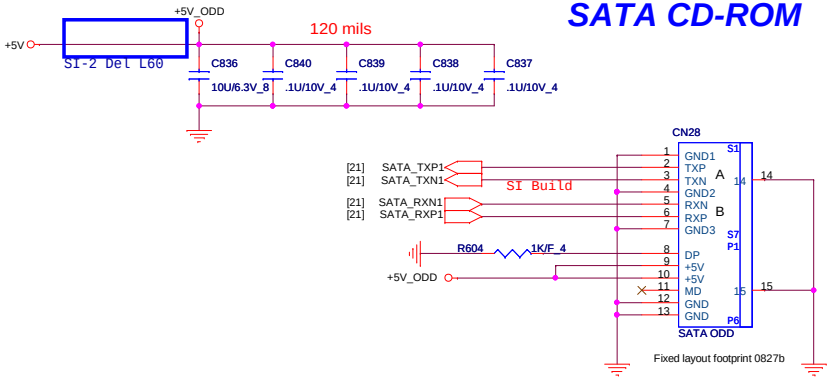
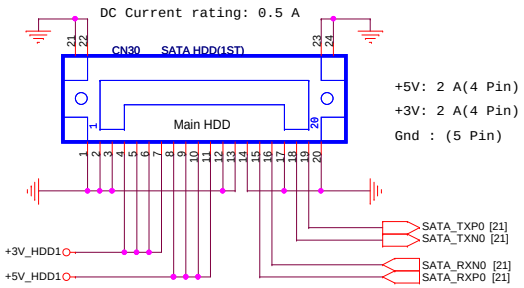
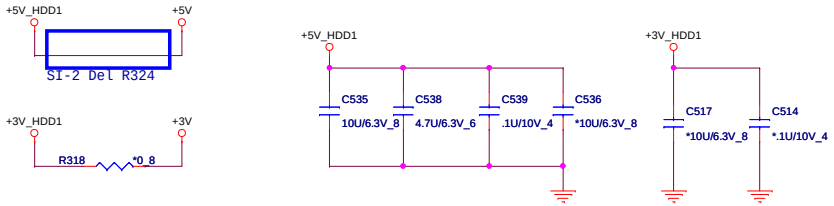
SATA CD-ROM



SATA_1 CONNECTOR

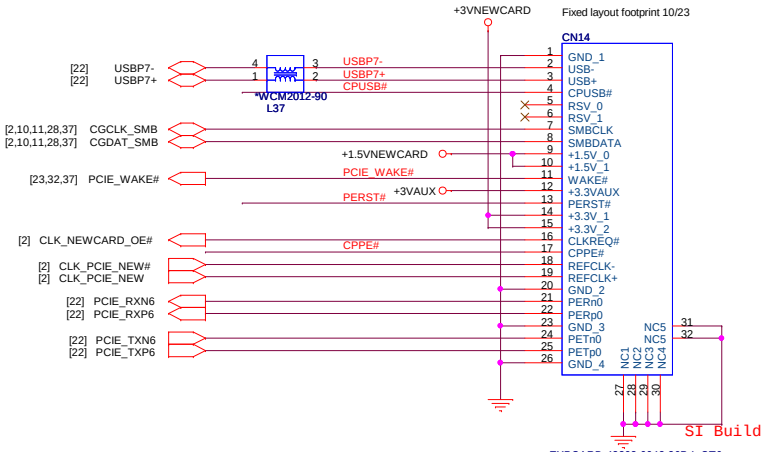


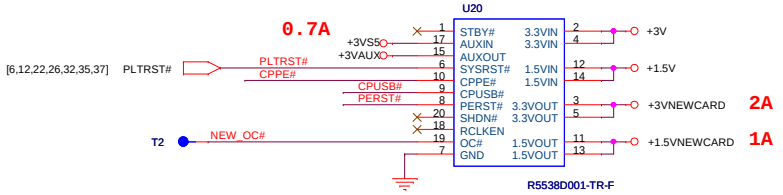


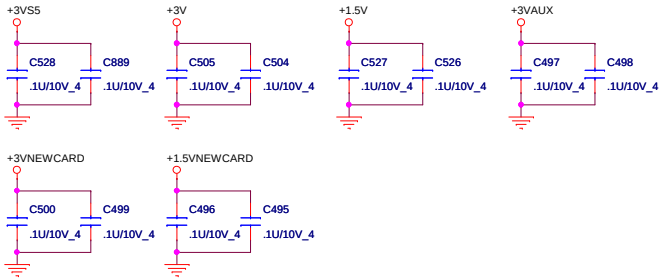
NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)

34







NB5

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ODD/HDD/NEW CARD	E3A

Date: Wednesday, August 06, 2008 Sheet 34 of 46

TOUCH PAD CONNECTOR

Spec. Change

SI modified
Swap pin define

25 mils

SI-2 Del L36

close conn

05/12 (PV) FOR EMI Solution

SI modified Change CN6 to BL123-06R-6P-L-QT6-A

TOUCH PAD ON/OFF

SI-2 Del L30

07/09 (PV2) FOR 2ND FAN function.

05/15 (PV) FOR HP recommend

07/09 (PV2) FOR 2ND FAN function.

05/12 (PV) FOR EMI Solution

07/09 (PV2) Delete for EMI solution.

SI-2 Del R612,R610

MODEL	UT7 120W (H)	UT6 90W (L)	UT6 65W (0.5V)
R694	8.25K/F_4	N/A	45.3K/F_4
R695	N/A	8.25K/F_4	8.25K/F_4

05/15 (PV) FOR HP recommend

SI modified

Delete Q18 and tied to U20#116 direction

SI-2 change 10K to 100K

07/09 (PV2) For HP LED SPEC change and Power recommend.

SI modified
Change C877,C878 to 27P

07/14 (PV2) Delete R688,R689 for EMI solution.

SI-2 Del R641,R659

SI-2 Del R618

MV modify short pad

SI Change

64.9K -->65W
33.7K -->90W

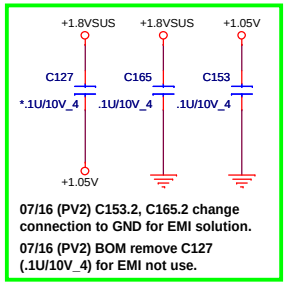
Socket: DG008000031
MXIC: AKE5GFK0Z09
AIT: AKE3GZP0801

CS36492FB17 RES CHIP 64.9K 1/16W +-1%(0402)
CS33322FB13 RES CHIP 33.2K 1/16W +-1% (0402)

PROJECT : UT6
Quanta Computer Inc.

NB5

Size: Custom | Document Number: KB3926/ROM/TP | Rev: E3A
Date: Wednesday, August 06, 2008 | Sheet 35 of 46

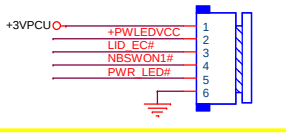


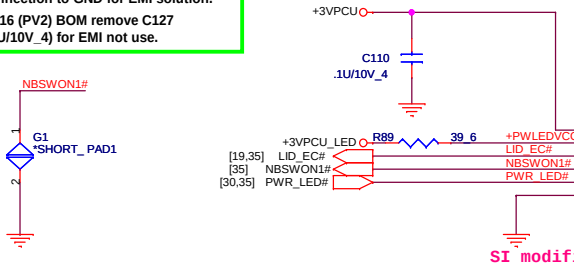
07/16 (PV2) C153.2, C165.2 change connection to GND for EMI solution.

07/16 (PV2) BOM remove C127 (.1U/10V_4) for EMI not use.

05/12 (PV) FOR M/E recommend

FOR UT7





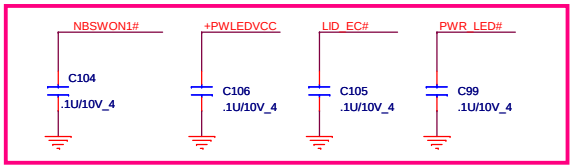
FOR UT6

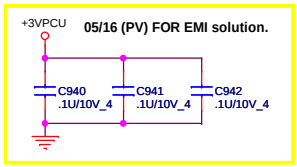
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

SI modified Change CN6 to BL123-06R-6P-L-QT6-A

POWER BOTTON CONNECT

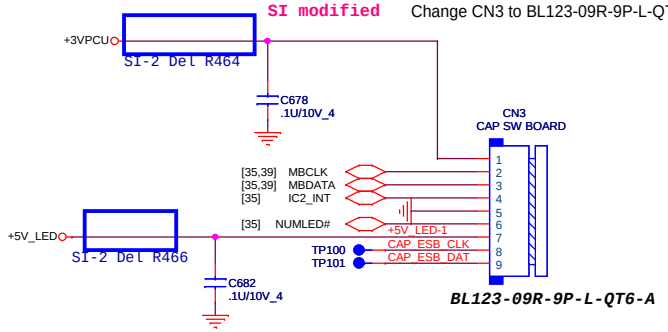
SI modified For EMI





CAP SW CONNECT

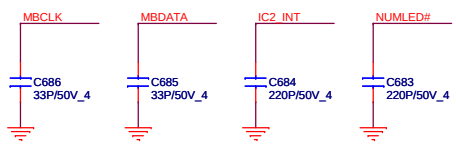
SI modified Change CN3 to BL123-09R-9P-L-QT6-A

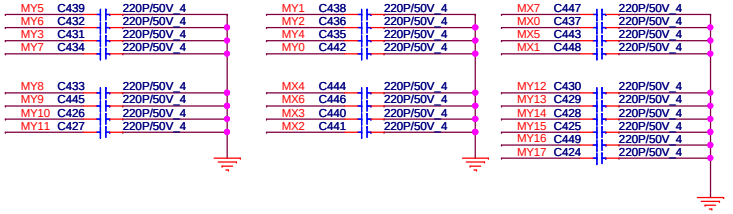


1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V_LED
8. ESB_CLK
9. ESB_DAT

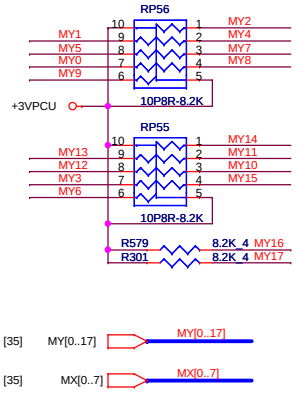
07/14 (PV2) Delete L69,L70,C922,C923 for EMI solution.

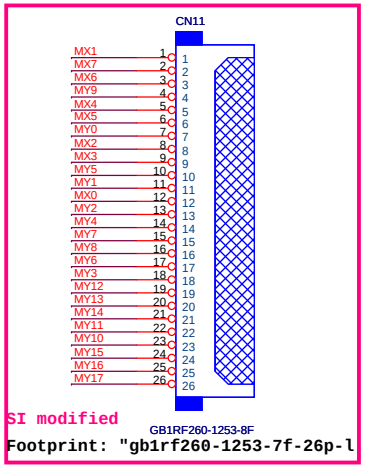
06/03 (PV) FOR EMI solution.





KEYBOARD PULL-UP

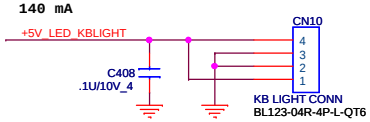




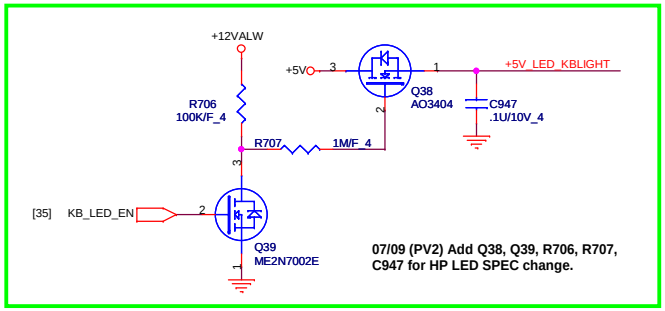
SI modified

Footprint: "gb1rf260-1253-7f-26p-l

140 mA



1. LEDVCC
2. GND
3. GND
4. LEDVCC



07/09 (PV2) Add Q38, Q39, R706, R707, C947 for HP LED SPEC change.

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Quanta Computer Inc.

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Custom	KB/CAP/POWER CONN	E3A

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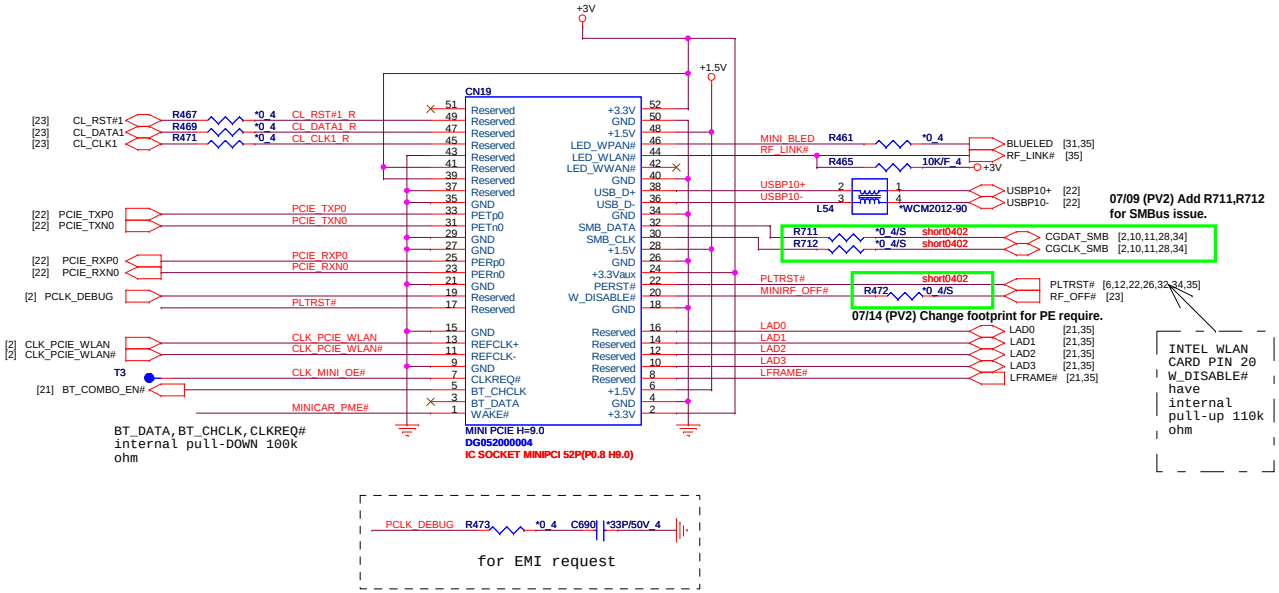
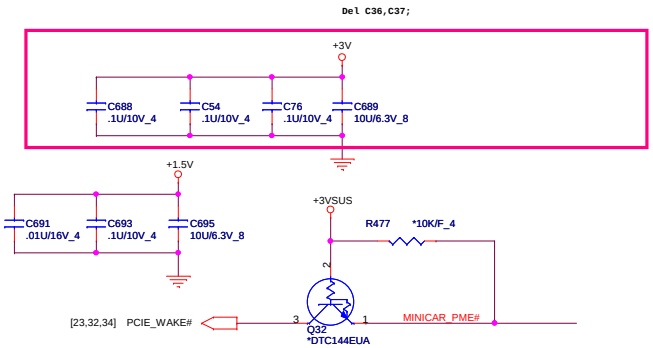
NB5

Mini PCI-E Card 1
WLAN

Delete R110,R78

+3V must have a 120mil plane
Each pin 25mil

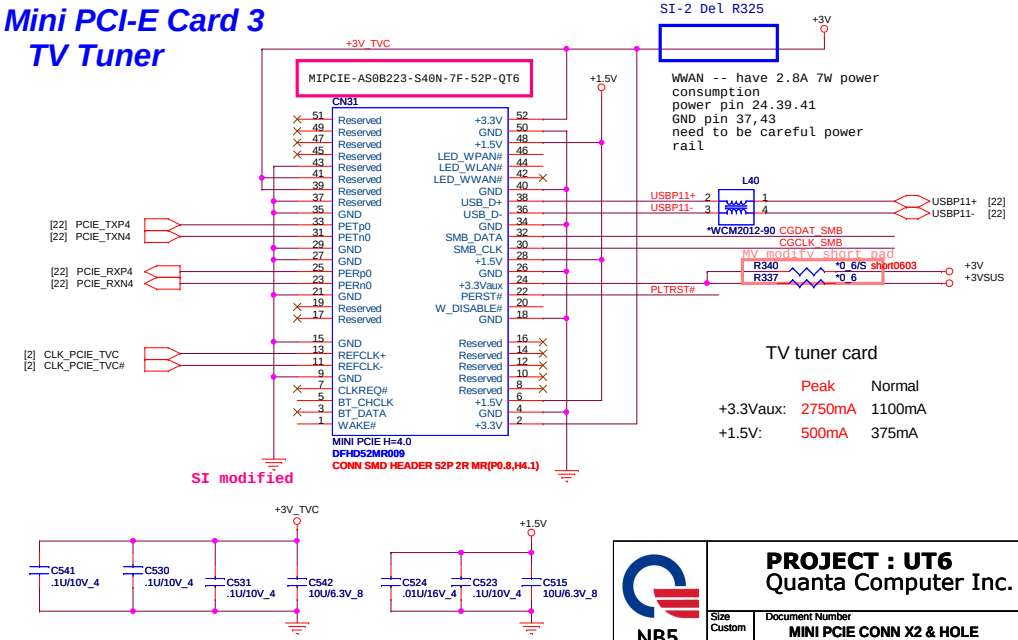




Mini PCI-E Card 2
ROBSON

07/09 (PV2) Delete for no support ROBSON card.

Mini PCI-E Card 3
TV Tuner



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Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	MINI PCIE CONN X2 & HOLE	E3A

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CABLE DOCK

support 6A 200mils
CX000480005

SPDIF R442 221/F_4 C660 .1U/50V_6 SPDIF_DOCK
R441 100/F_4
C659 220P/50V_4

+DOCK_VA L51 MLB-321611-0048P-N1A_12 +VA_DOCKIN
C654 .1U/50V_6
C655 .1U/50V_6

+3V R468 100K/F_4
+3VPCU R470 *100K/F_4
PR_INSERT# PR_INSERT# [20,35]
DOCK_PRESENT R462 1K/F_4 DKPR# Q31 MMBT3904-7-F
R463 2K/F_4

USBP4- USBP4+ L3 *CMM211T-900M-S

05/23 (PV) For IDT Dolby functionality.
07/14 (PV2) Change footprint for PE require.
PR_INSERT#_IDT R699 *0_4/S short0402 PR_INSERT#

07/14 (PV2) Change footprint for PE require.
DDCDAT2 PR_HSYNC DDCCLK2 PR_VSYNC
R31 *0_6/S short0603
R32 *0_6/S short0603
CRT_GDK CRT_RDK CRT_BDK PR_HSYNC_D PR_VSYNC_D USBP4- USBP4+
LAN_MX3+ LAN_MX3- LAN_MX2+ LAN_MX2- LAN_MX1+ LAN_MX1- LAN_MX0+ LAN_MX0-
+VIN C40 .1U/50V_6

CN17 DOCKING CONN
+VA_DOCKIN VDD VSS
TP68 TP69 TP67
CIR_IN PWR_ON MUTE_LED SLP_BTN# JACK_SEN# VOLME_UP# VOLME_DN# SPDIF_DOCK
AGND RSPK_DK LSPK_DK DOCK_MIC_R3 DOCK_MIC_L3 AGND DOCK_PRESENT

SI-2 Modified
Change to RB500 as Current loss
+5V D23 RB500-40
+5VSUS R440 10K/F_4 DK_PWRON D22 RB500-40 PWR_ON
R439 15K/F_4
S0: 4V
S3: 2.5V
S4/S5: 0V
*Check voltage on DB

MV modify short pad
DOCK_RSPK+ R443 *0_4/S short0402 RSPK_DK
DOCK_LSPK+ R444 *0_4/S short0402 LSPK_DK
C662 100P/50V_4
C661 100P/50V_4

DOCK_MIC_R R450 *0_6/S short0603 DOCK_MIC_R3
DOCK_MIC_L R453 *0_6/S short0603 DOCK_MIC_L3
07/14 (PV2) Change footprint for PE require.
C669 220P/50V_4
C665 220P/50V_4
SI modified

CPU FAN

QT6 Modified-0117
Del R57
+5V C232 1U/6.3V_4
FANPWR = 1.6*VSET
30 MIL
U5 G995 AL005606000 IC OTHER(8P) APL5606KI-TRL(SOP-8)
VIN VO /FON GND VSET GND
+5V_FAN
R156 10K/F_4 THERM_OVER#
VFAN
+3V R155 4.7K_4
FAN1SIG
CN22 FAN CONN
C230 2.2U/6.3V_6
C231 .1U/10V_4

2ND FAN

07/09 (PV2) Add for 2ND FAN function.
+5V C944 1U/6.3V_4
FANPWR = 1.6*VSET
30 MIL
U47 G995 AL005606000 IC OTHER(8P) APL5606KI-TRL(SOP-8)
VIN VO /FON GND VSET GND
+5V_FAN_2ND
R701 10K/F_4 THERM_OVER#_2ND
VFAN_2ND
+3V R700 4.7K_4
FAN2SIG
CN38 FAN CONN
C945 2.2U/6.3V_6
C946 .1U/10V_4

QT6 modified-0117
PR_GEN PR_RED PR_BLU
R30 150/F_4
R22 150/F_4
R28 150/F_4

06/03 (PV) BOM modify for EMI solution.
R27 BK1608LL680-T CRT_GDK
R24 BK1608LL680-T CRT_RDK
R29 BK1608LL680-T CRT_BDK
C27 10P/50V_4
C21 10P/50V_4
C24 10P/50V_4
06/03 (PV) BOM modify for EMI solution.
C26 *6.8P/50V_4
C23 *6.8P/50V_4
C25 *6.8P/50V_4

PR_HSYNC_D PR_VSYNC_D JACK_SEN# VOLME_DN# CIR_IN
C656 120P/50V_4
C657 120P/50V_4
C658 270P/25V_4
C32 47P/50V_6
C28 47P/50V_6
SI modified

NB5
PROJECT : UT6
Quanta Computer Inc.
Size Custom
Document Number CABLE DOCKING/FAN
Rev E3A
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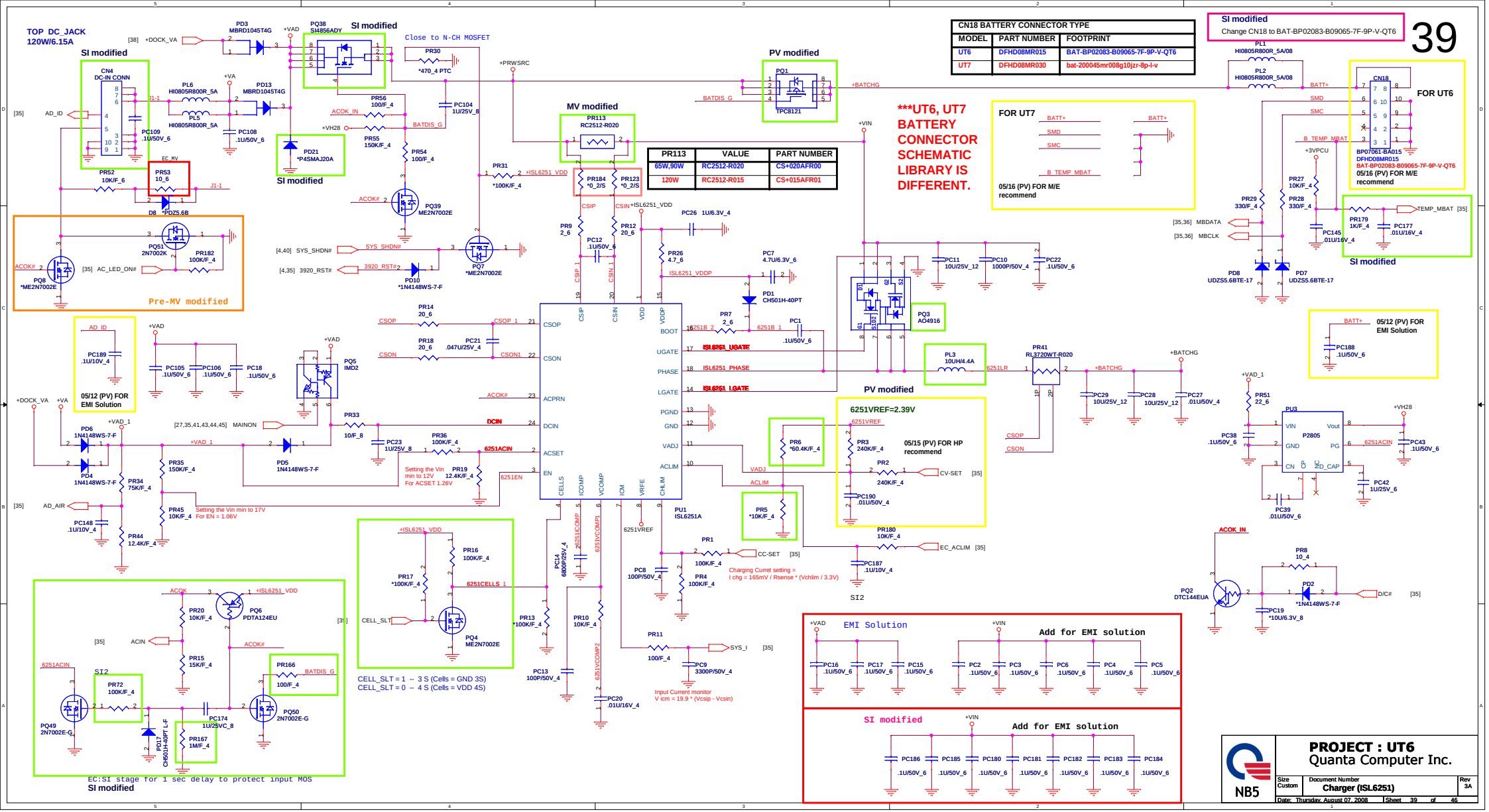

CN18 BATTERY CONNECTOR TYPE		
MODEL	PART NUMBER	FOOTPRINT
UT6	DFHD08MR015	BAT-BP02083-B09065-7F-9P-V-QT6
UT7	DFHD08MR030	bat-200045mr008g10jzr-8p-l-v

PR113	VALUE	PART NUMBER
65W,90W	RC2512-R020	CS+020AFR00
120W	RC2512-R015	CS+015AFR01

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

Place these CAPs close to FETs

Pre-MV modified

PR183 *0_4 — PD22 PDZ5.6B — PR133 1K_4 — PR129 150K/F_4

+VIN

PC93 10U/25V_12 — PC87 1000P/50V_4 — PC88 .1U/50V_6

DEL PR78 0_6

+5VALW

PC66 4.7U/25V_8

DEL PR72 (47ohm_6)

+5V_VCC1

PC127 .1U/50V_6 — PC65 1U/6.3V_4 — PC126 .1U/10V_4 — PC122 1U/6.3V_4

DEL PR76,PR80,PR134

Place these CAPs close to FETs

PC79 .1U/50V_6 — PC76 1000P/50V_4 — PC83 10U/25V_12

5 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 9A

+5VPCU — +5V_ALWP — PC135 .1U/10V_4 — PC136 330U/6.3V_6X5.8 — PR83 *0_4 — PR84 *0_4/S

PL10 2.5uH/7.5A

PQ20 FDS8884 — PQ24 SI4686DY-T1-E3

PR149 *2.2_8 — PC137 *1500P/50V_4

5V_LX — 5V_DH — 5V_DL

Rds(on) 20m ohm

PR136 232K/F_4

PU4 ISL6237IRZ-T

BYP, OUT1, FB1, ILIM1, PGOOD1, ON1, DH1, LX1, PAD, BST1, DL1, VDD, N.C, AGND, PGND, DL2, BST2, PAD, PAD, REFIN2, ILIM2, OUT2, SKIP, PGOOD2, ON2, DH2, LX2

DOREFIN, LDO, IN, N.C, ONLDO, VCC, TON, REF

PGOOD1 — PGOOD2

PR137 309K/F_4

PC80 .1U/50V_6 — PR96 4.7_6 — PC72 .1U/50V_6 — PR143 4.7_6

3V_DH — 3V_DL

PQ16 FDS8884 — PQ19 FDS4410A

3V_LX — PL9 2.5uH/7.5A — +3.3V_ALWP — +3VPCU

PR148 *2.2_8 — PC132 *1500P/50V_4

PR85 *0_4/S — PR87 *0_4 — PC133 .1U/10V_4 — PC134 330U/6.3V_6X5.8

Rds(on) 20m ohm

PD11 — BAT54SPT — PD12 — BAT54SPT

PC77 .01U/50V_6 — PC78 .01U/50V_6 — PC82 .1U/25V_8

PC81 1U/6.3V_4

PR144 *SHORT-1A

PR93 100K/F_4

+12VALW

PC85 2.2U/50V_8

[4,39] SYS_SHDN#

PGOOD2 — PGOOD1 — PR91 *0_4/S — HWPG [35,41,43,44]

NB5

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
B	+5V/+3V (ISL6237)	3A

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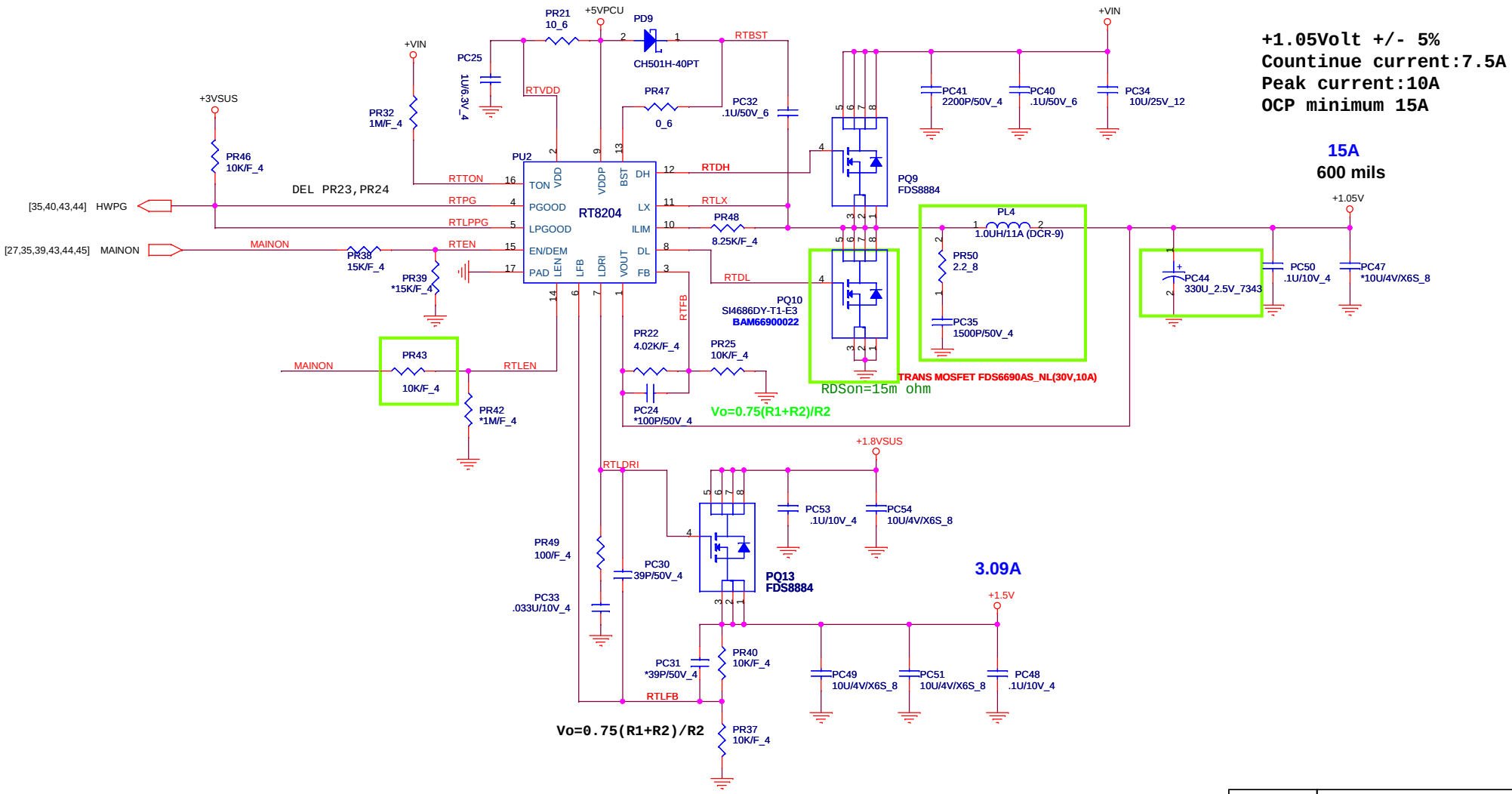
VCCP1.05V & +1.5V



NB5

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.05V/+1.5V (RT8204)	3A

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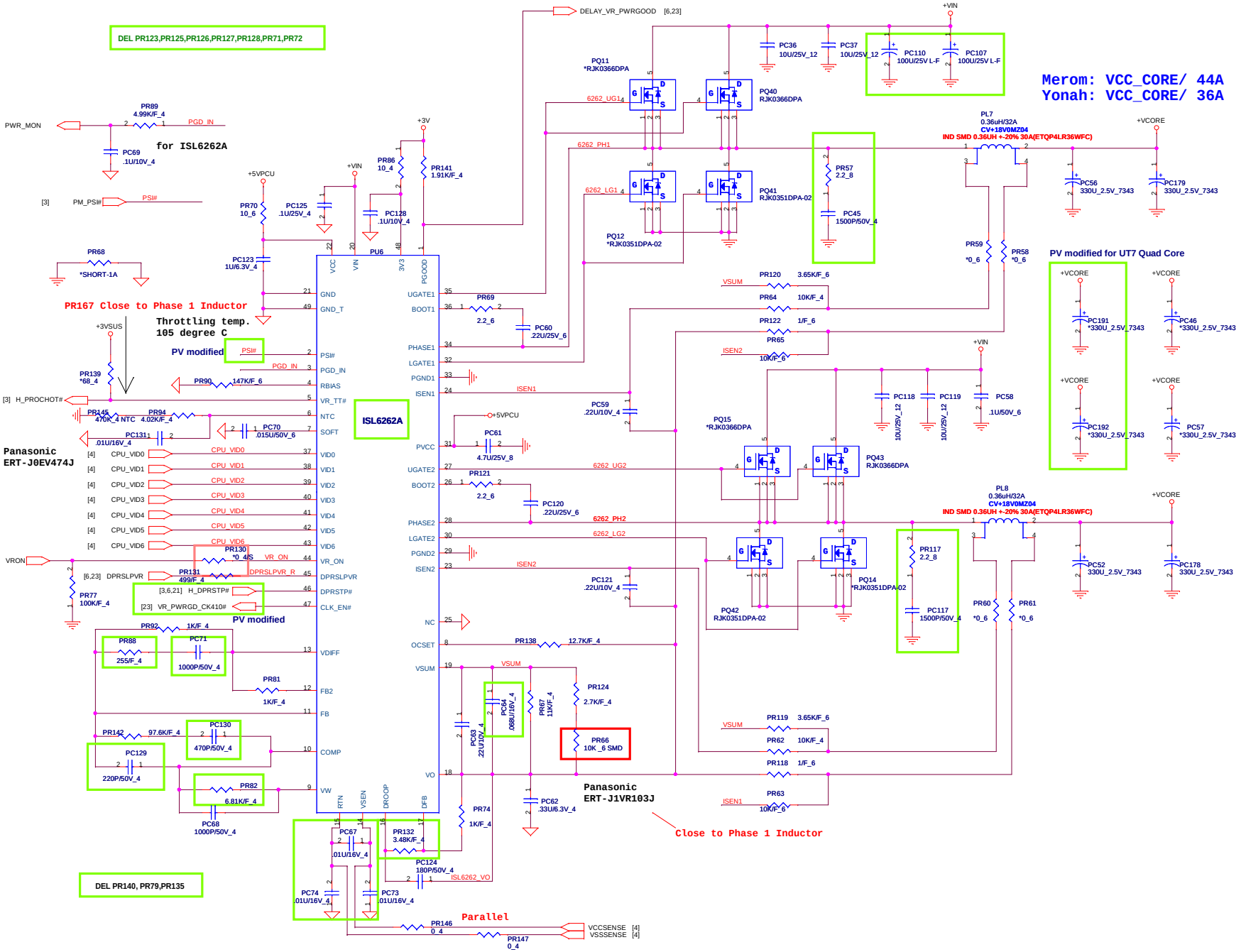

NB5	PROJECT : UT6 Quanta Computer Inc.	
	Size: Custom Document Number: CPU Core (ISL6266A)	Rev: 3A
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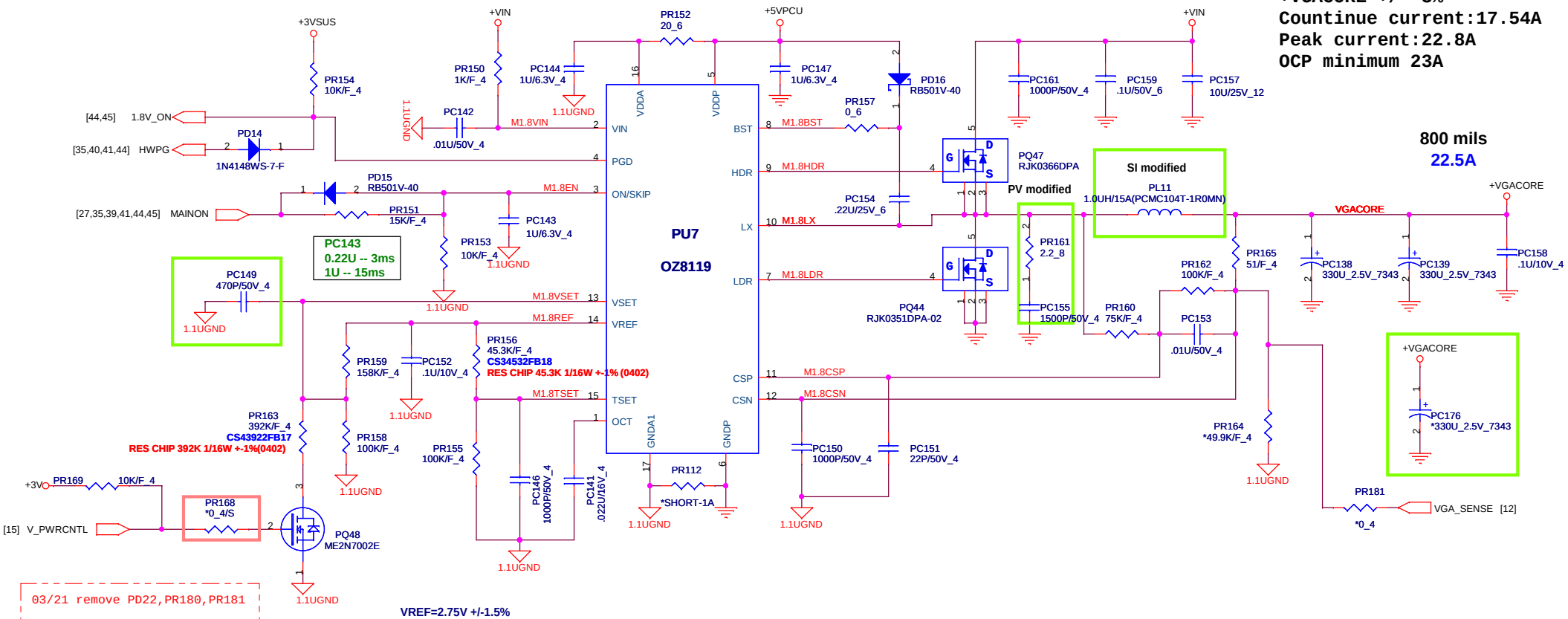
VGA Core & VCC1.1



V_PWRCNTL GPIO5	NB9P-GS
Low	1.05V
High	0.9V

VGA_GPIO6 GPIO6	V_PWRCNTL GPIO5		NB9P-GS	NB9M-GE
Low	Low	MAX BAT	0.9V	0.9V
Low	High	SD DVD	0.9V	0.9V
High	Low	HD DVD	0.9V	0.9V
High	High	MAX PERF	1.05V	1.09V

NB5

PROJECT : UT6
Quanta Computer Inc.

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B	VGA CORE OZ8118	3A

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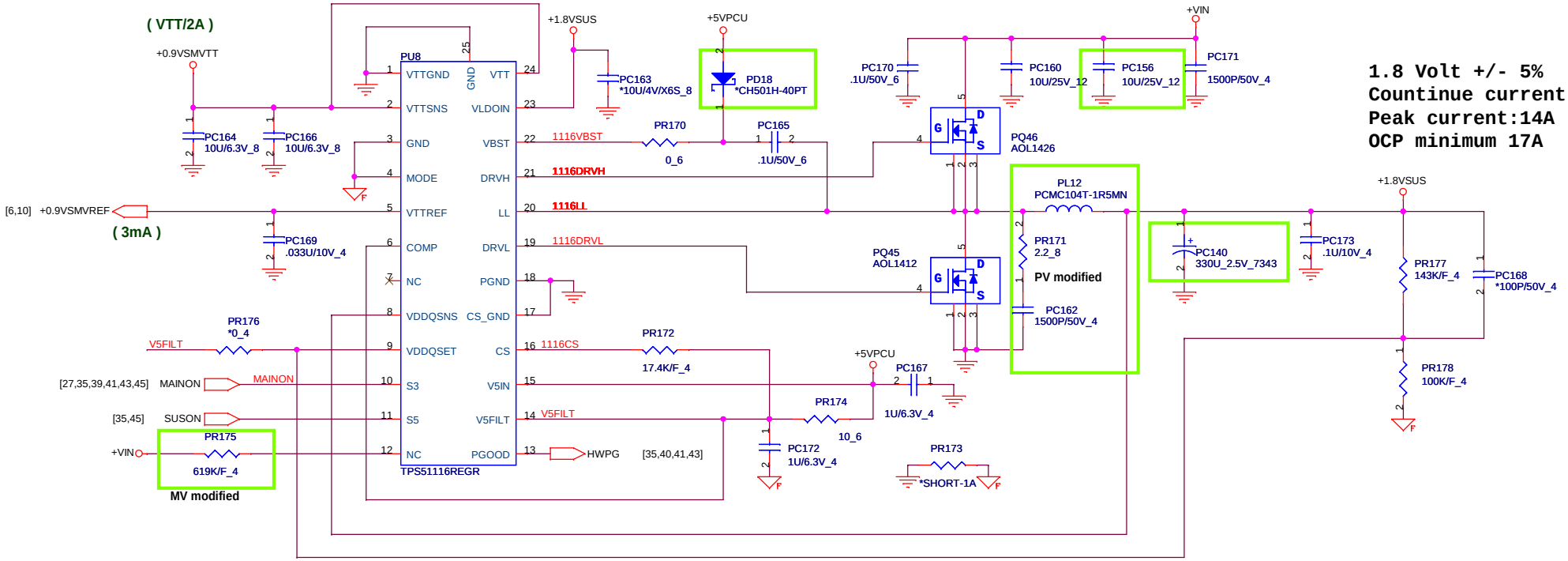
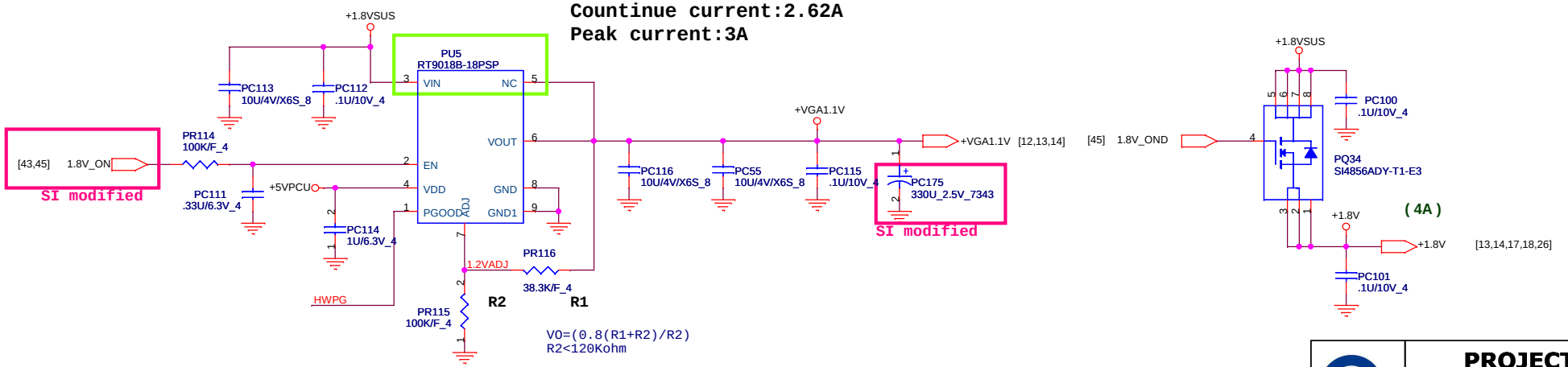
(VTT/2A)

1.8 Volt +/- 5%
Countinue current:6A
Peak current:14A
OCP minimum 17A



1.1 Volt +/- 5%
Countinue current:2.62A
Peak current:3A



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Quanta Computer Inc.

NB5

Size	Document Number	Rev
B	1.8V/DDR_VTER/+1.8v/+1.1V	3A

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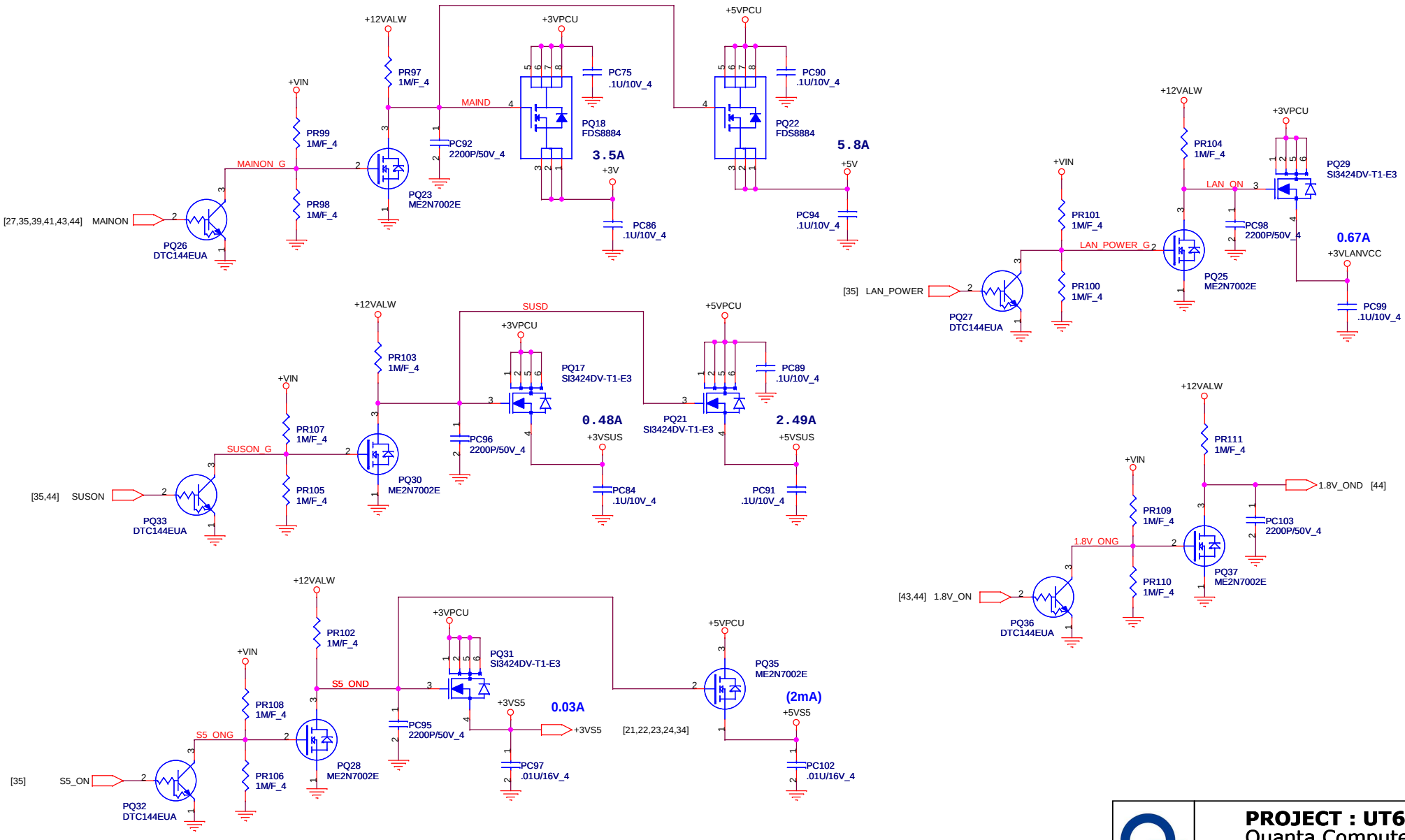

NB5

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
B	DISCHARGE/3VS5/5VS5/LAN	3A

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		AC MODE				DC MODE			
	Voltage level	S0	S3	S4	S5	S0	S3	S4	S5
+3VPCU	3.3V +/- 5%	V	V	V	V	V	V	V	V
+5VPCU	5V +/- 5%	V	V	V	V	V	V	V	V
+3VRTC	3.3V +/- 5%	V	V	V	V	V	V	V	V
+3VS5	3.3V +/- 5%	V	V	V	V	V	V		
+5VS5	5V +/- 5%	V	V	V	V	V	V		
+3VSUS	3.3V +/- 5%	V	V			V	V		
+5VSUS	5V +/- 5%	V	V			V	V		
+1.8VSUS	1.8V +/- 5%	V	V			V	V		
+0.9VSMVTT	0.9V +/- 5%	V	V			V	V		
+1.5V	1.5V +/- 5%	V				V			
+1.05V	1.05V +/- 5%	V				V			
+VCORE	0.9~1.15V	V				V			
+VGA_CORE	0.9~1.2V	V				V			
+VGA1.1V	1.1V +/- 5%	V				V			
+1.8V	1.8V +/- 5%	V				V			
+3VLANVCC	3.3V +/- 5%	V				V			

NB5

PROJECT : UT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**Voltage**	E3A

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