

Annika 1.1 Block Diagram

01

PCB STACK UP

6L

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

10.1" LCD Panel
Page 16

CRT
Page 12

Intel Pineview-M
Micro-FCBGA8
22 x 22 mm
TDP~5.5W
Page 3~5

DDR3 667MT/s
Single Channel

DDR3 SO-DIMM
2GB Max.
Page 11

XDP
Page 31

CLOCK GEN
9LRS3165
Page 2

SATA

2.5"HDD/SSD
Page 19

Intel
Tigerpoint
17 x 17 mm
MMAP 360 Balls
TDP~1.5W
Page 6~10

USB 2.0

0, 1, 2
USB2.0
Port x3
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Card
Reader
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Card Reader
Socket
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5
Bluetooth
/WLAN
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Touch Screen
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7
WWAN
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SIM Card Socket
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8
Webcam
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PCI-Express

X1
WWAN
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SIM Card
Page 20

X1
LAN
Realtek
RTL8103EL-VB
10/100
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RJ 45
Page 15

X1
WLAN
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X1
HD Decoder
Page 18
DDRII
64MByte
Page 18

SYSTEM POWER
+3VPCU/+5VPCU(RT8206)
PAGE 24

DDR 3 SMDDR_VTERM
+0.75VSMVREF/+1.5VSUS(RT8207)
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CPU CORE RT8152D
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SYSTEM CHARGER ISL6251AHAZ-T
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GFX CORE(RT9025)
+1.2V(RT9025)
+1.5V(RT9025)
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VCCP 1.05V(RT8209A)
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Touch Pad
Keyboard
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Power SW
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32.768KHz
LPC

ENC KBC
KB3926D2
Page 23

BIOS
SPI Flash
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FAN
G991
Page 22

HDA

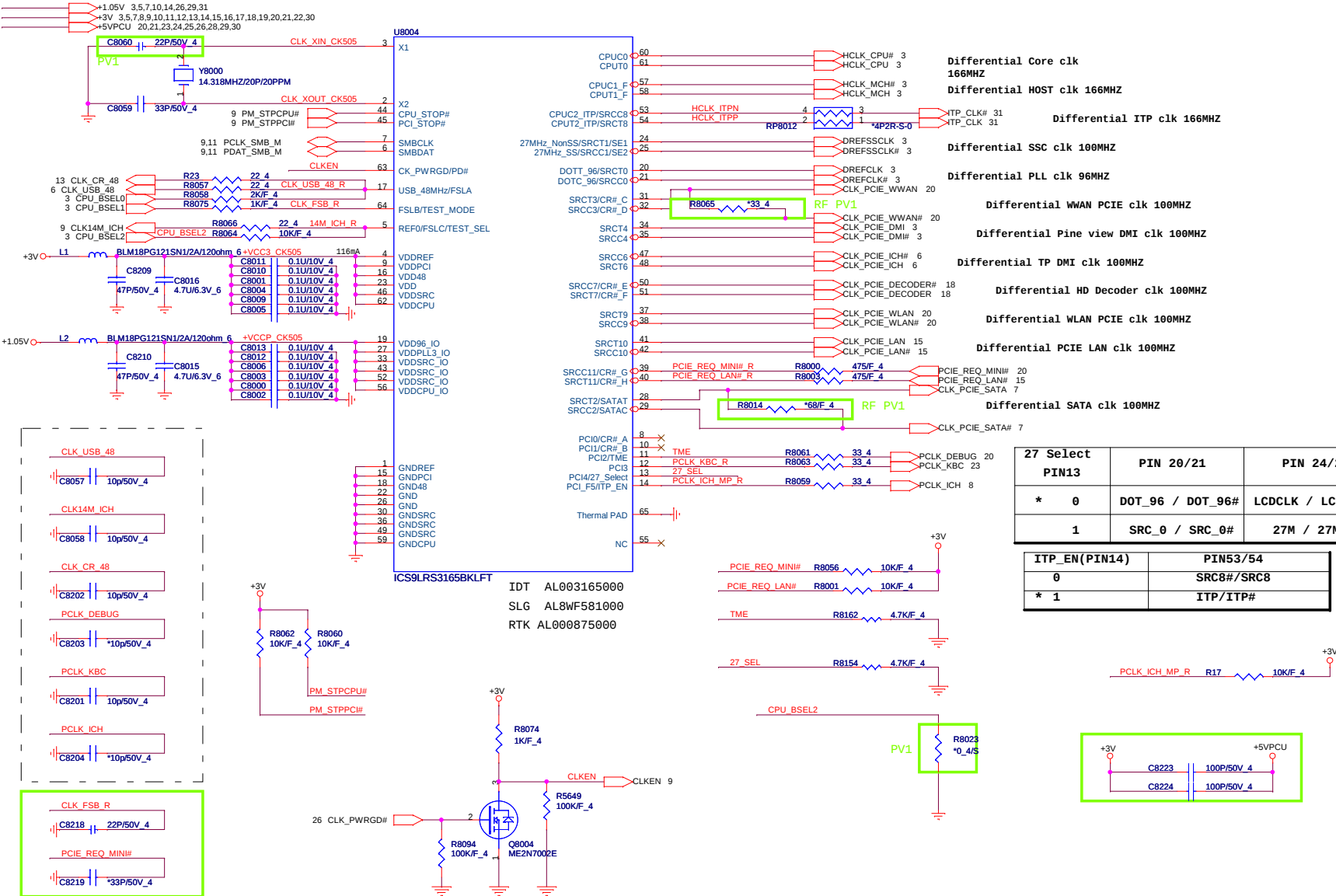
AUDIO CODEC
92HD80BX
Page 17

Int SPK
Page 17

Digital MIC
Page 17

HP/MIC
COMBO JACK
Page 17

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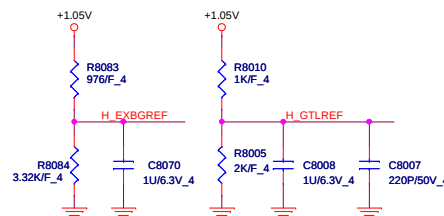
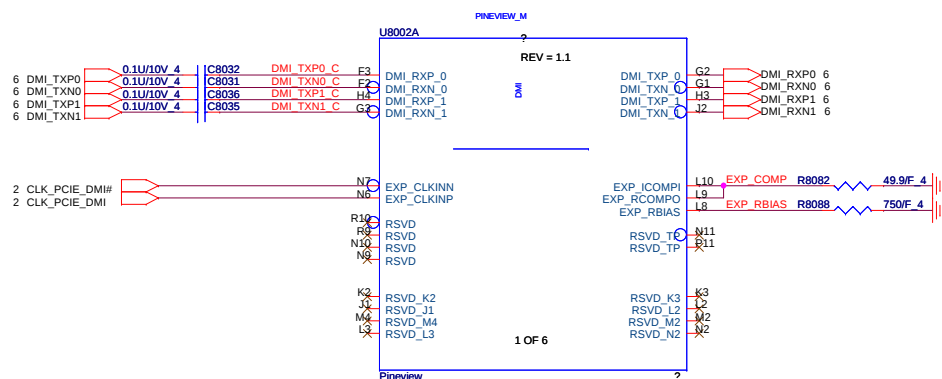
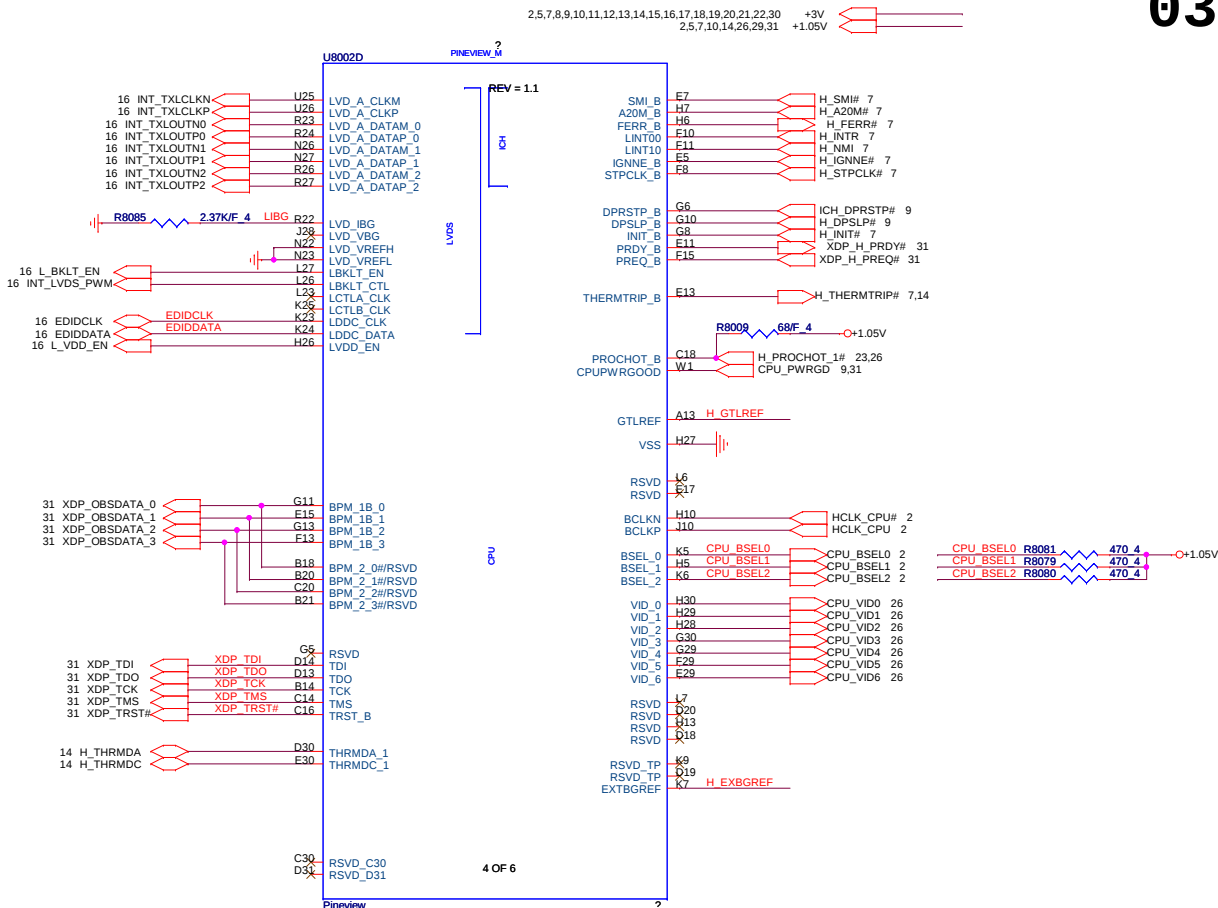
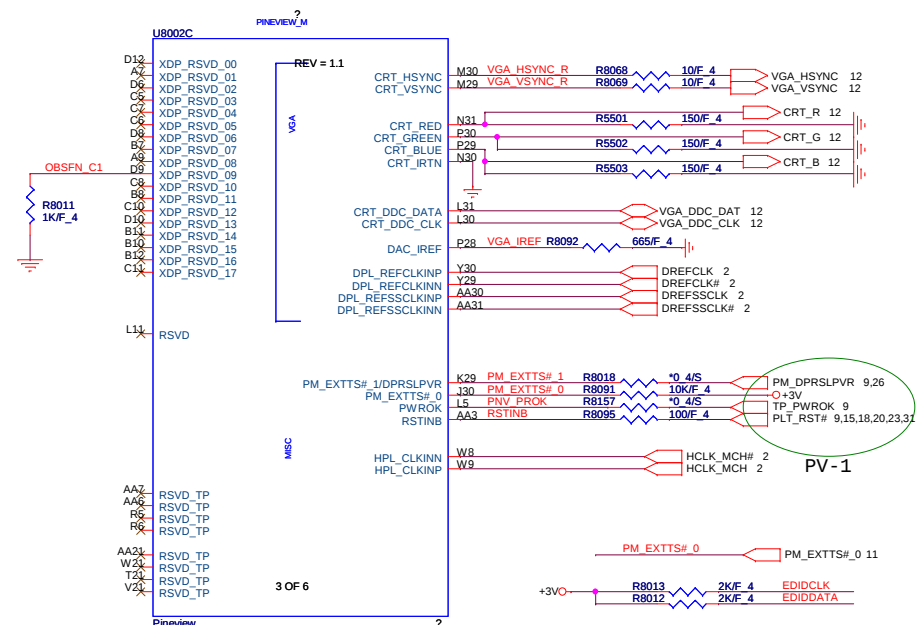


- Differential Core clk 166MHZ
- Differential HOST clk 166MHZ
- Differential ITP clk 166MHZ
- Differential SSC clk 100MHZ
- Differential PLL clk 96MHZ
- Differential WWAN PCIE clk 100MHZ
- Differential Pine view DMI clk 100MHZ
- Differential TP DMI clk 100MHZ
- Differential HD Decoder clk 100MHZ
- Differential WLAN PCIE clk 100MHZ
- Differential PCIE LAN clk 100MHZ
- Differential SATA clk 100MHZ

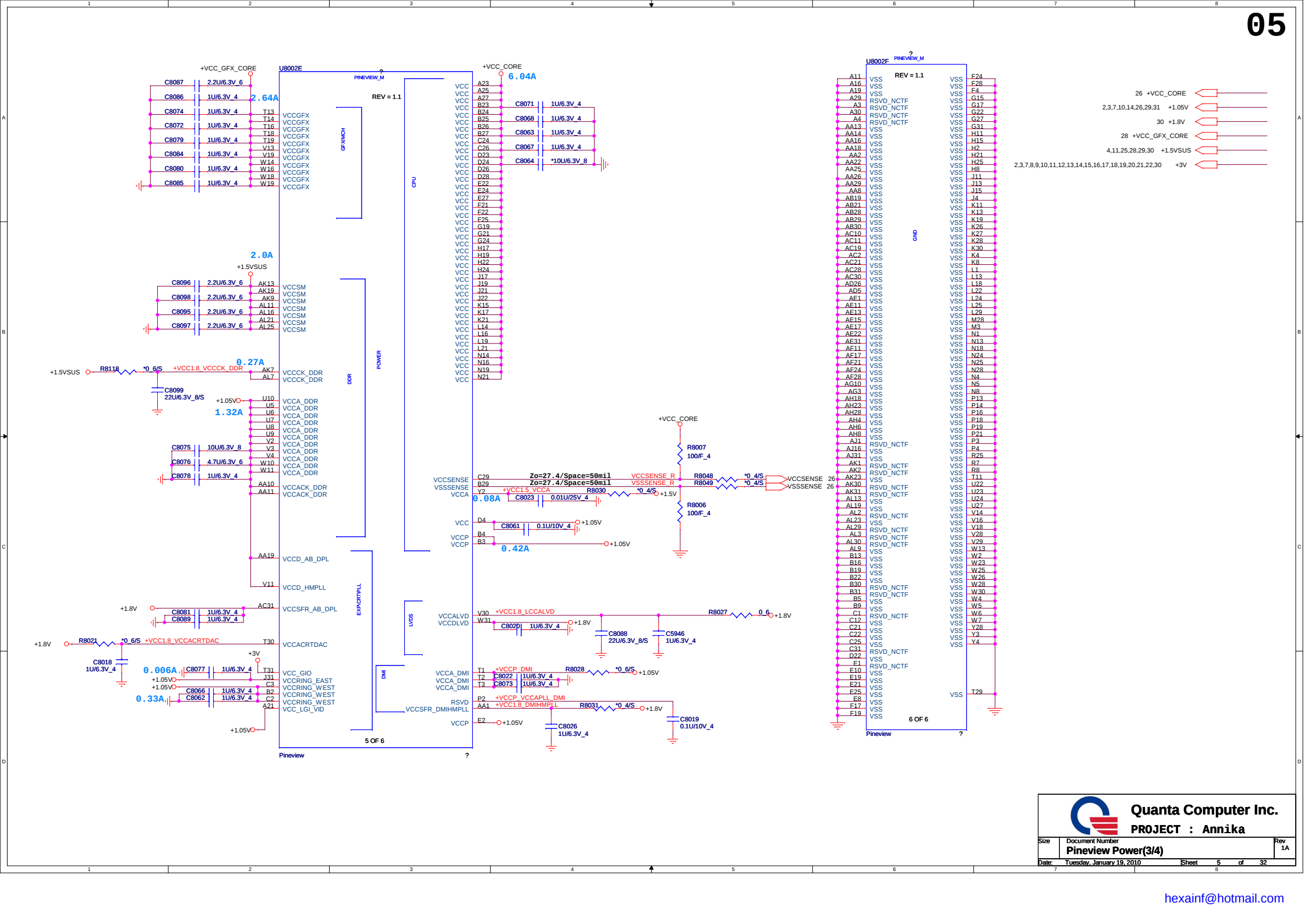
27 Select PIN13	PIN 20/21	PIN 24/25
* 0	DOT_96 / DOT_96#	LCDCLK / LCDCLK#
1	SRC_0 / SRC_0#	27M / 27M_SS

ITP_EN(PIN14)	PIN53/54
0	SRC8#/SRC8
* 1	ITP/ITP#

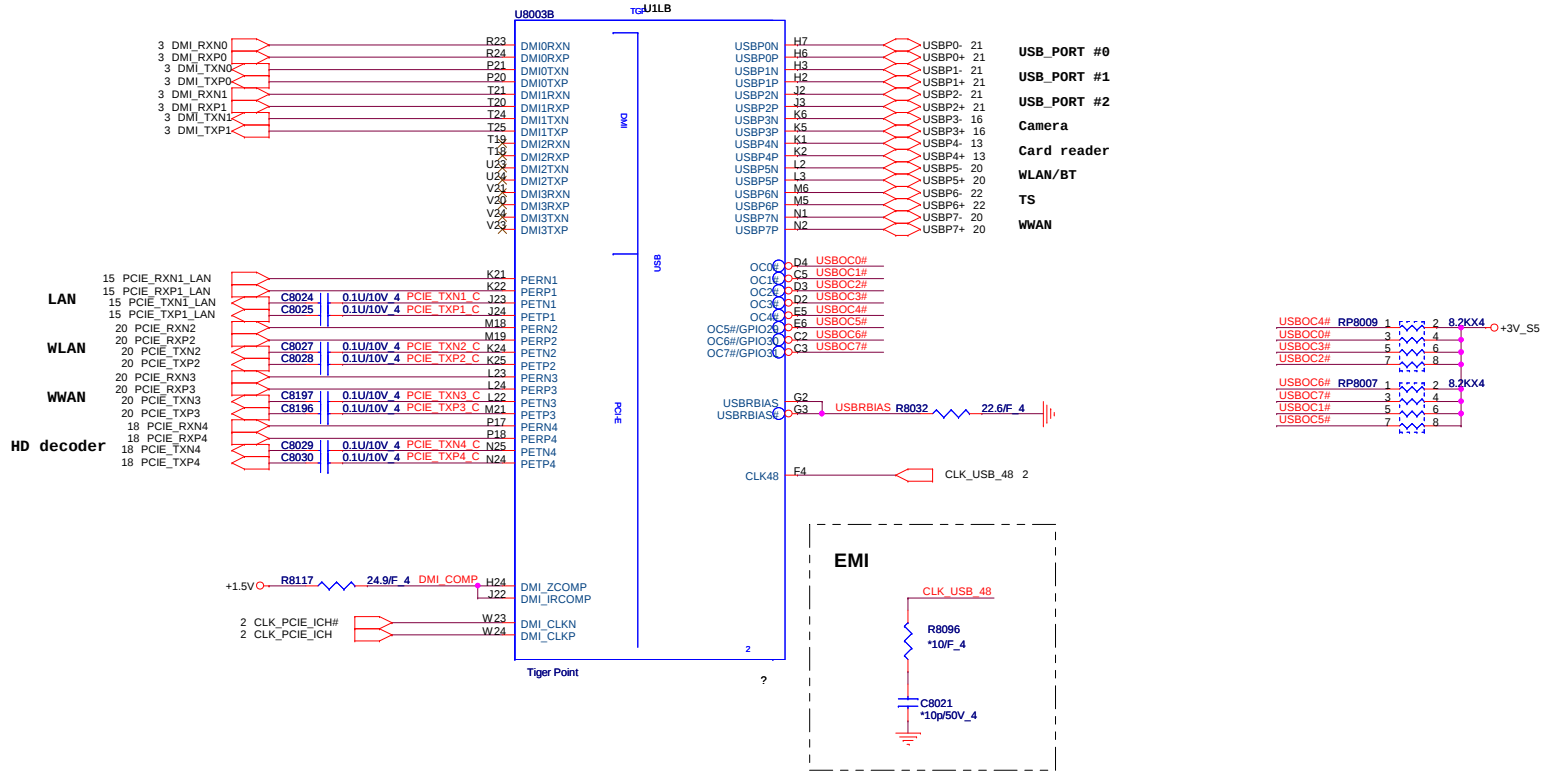
FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
0	1	0	200.00	100	33.33	14.318	48	96	0.5 Down
0	1	1	166.66	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	RESERVED						



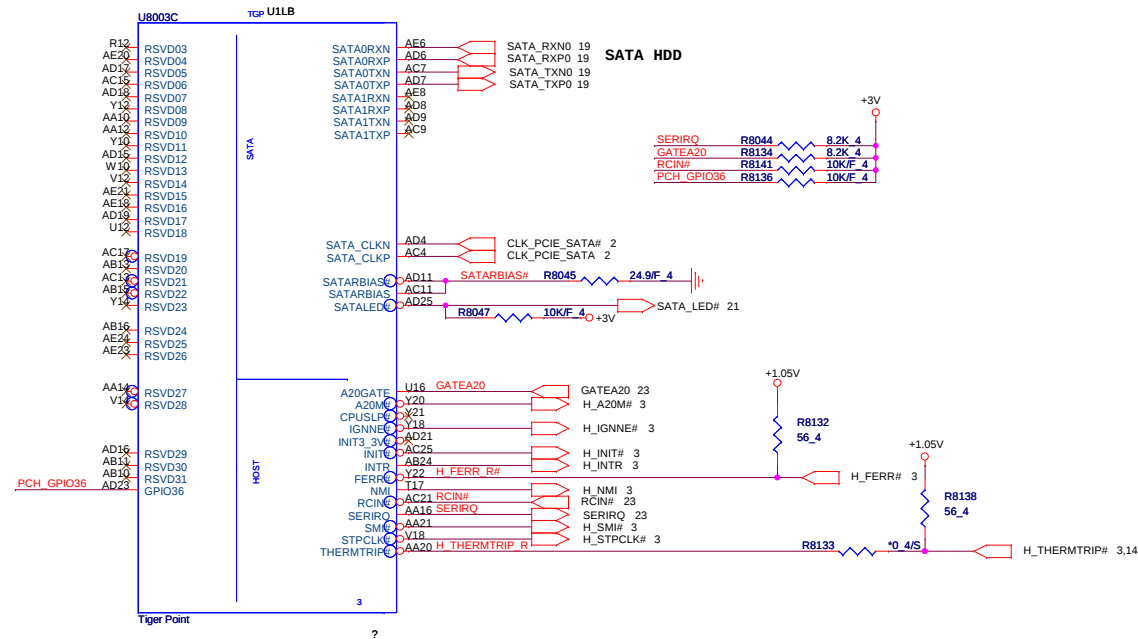




5,10,18,20,30 +1.5V
9,10,30 +3V_S5



 +3V 2,3,5,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,30
 +1.05V 2,3,5,10,14,26,29,31





ICH Boot BIOS select

PCH_GPIO17 (INT PU)	PCH_GPIO48 (INT PU)	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (Default)

A16 SWAP Override blue

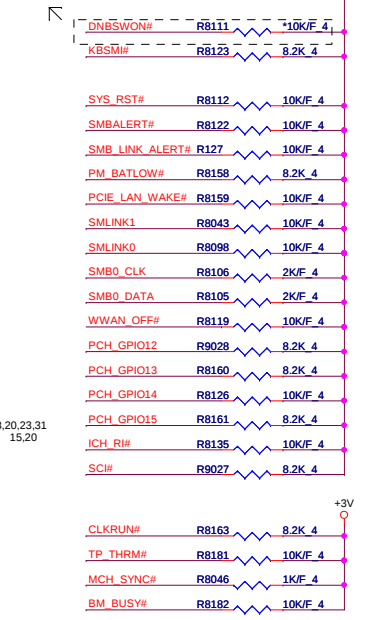
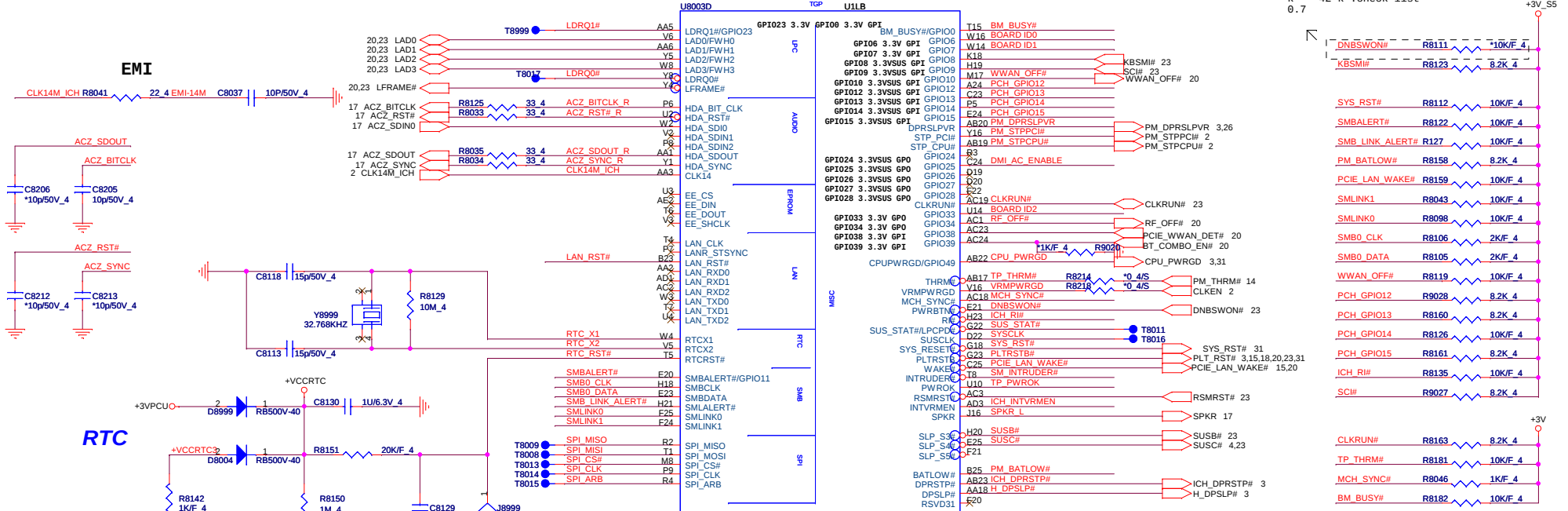
PCH_A16WP (INT PU)	Low = A16 swap override enabled High = Default
-----------------------	---

IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UHCI Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2

PCI_GNT#2	Internal PU Should not be PD
-----------	---------------------------------

14,16,20,21,22,23,24,26,27,30 +3VPCU
2,3,5,7,8,10,11,12,13,14,15,16,17,18,19,20,21,22,30 +3V
6,10,30 +3V_S5

integrated pull-up of 18 k - 42 k .check list 0.7

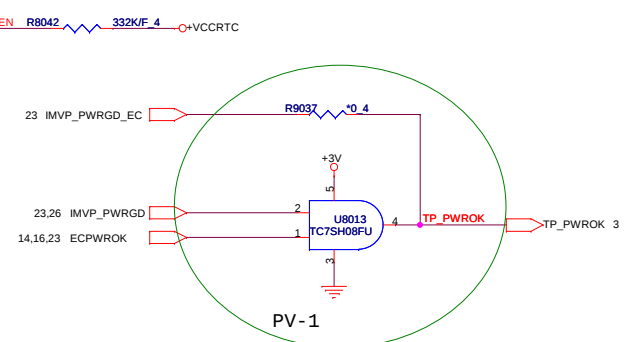


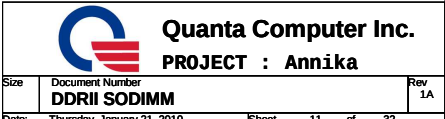
INTVRMEN	
Enable (default)	1
Disable	0

Board ID	ID0	ID1	ID2
Annika 1.0 WO SIM	0	0	0
Annika 1.0 W/ SIM	1	0	0
Annika 1.1 WO SIM	0	1	0
Annika 1.1 W/ SIM	1	1	0

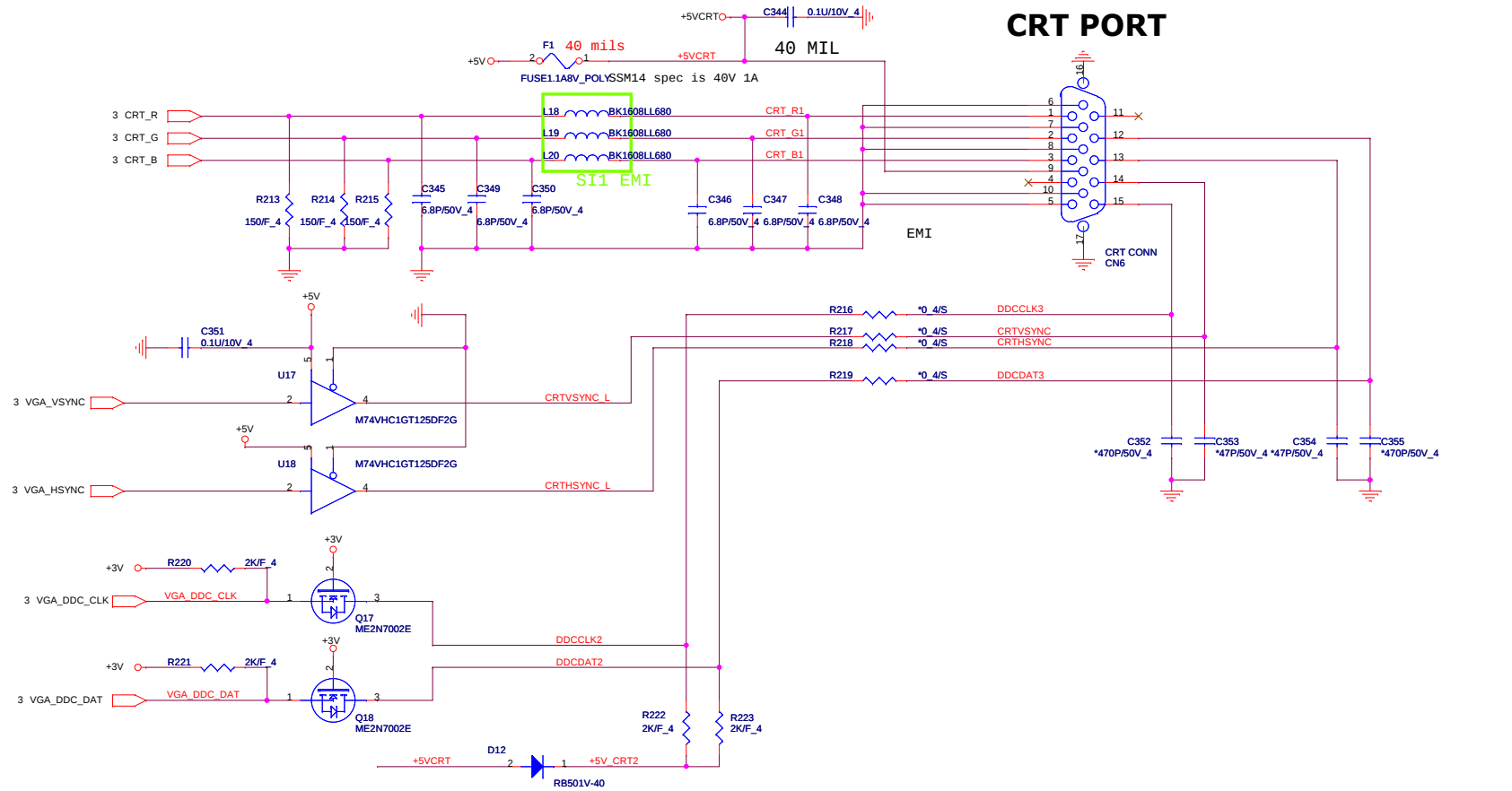
ACZ_SDOUIT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0	* 4 x 1s
1	0	Reserved
0	1	Reserved
1	1	1 x 4s(1 port/4 lanes)

GPIO25 This signal has a weak internal pull-up. If the signal is sampled high, the DMI interface is strapped to operate in DC coupled mode (No coupling capacitors are required on DMI differential pairs). If the signal is sampled low, the DMI interface is strapped to operate in AC coupled mode (Coupling capacitors are required on DMI differential pairs). NOTE: Board designer must ensure that DMI implementation matches the strap selection.



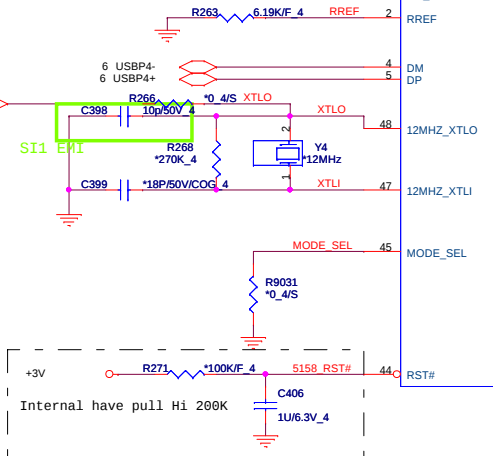
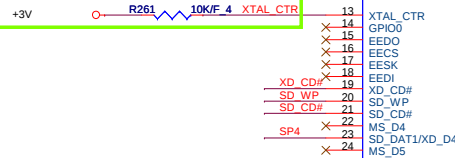


2,3,5,7,8,9,10,11,13,14,15,16,17,18,19,20,21,22,30 +3V
2,3,5,7,10,14,26,29,31 +1.05V

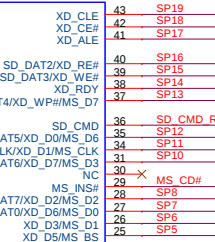


SD/MMC	MS	XD
SP0		XD_CD#
SP1	SD_WP	
SP2	SD_CD#	
SP3	SD_DAT1	XD_D4
SP4	MS_BS	XD_D5
SP5	MS_D1	XD_D3
SP6	SD_DAT0	MS_D0
SP7	SD_DAT7	MS_D2
SP8	MS_INS#	XD_D2
SP9	SD_DAT6	MS_D3
SP10	SD_CLK	MS_SCLK
SP11	SD_CMD	XD_D0
SP12	SD_DAT5	XD_WP#
SP13	SD_DAT4	XD_R/#
SP14	SD_DAT3	XD_WE#
SP15	SD_DAT2	XD_RE#
SP16	XD_ALE	
SP17	XD_CE#	
SP18	XD_CLE	
SP19		

PU for internal CLK input
Unstuff for external XTAL(12MHZ)

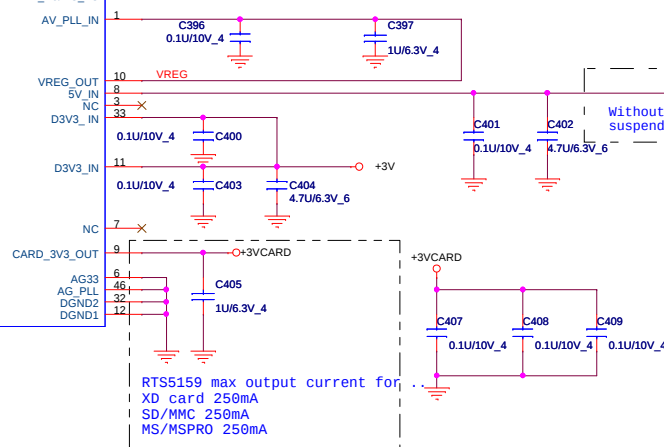
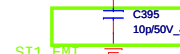


Realtek RTS5159

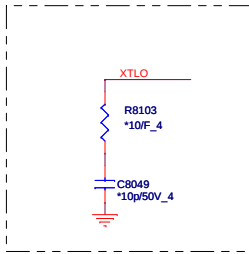


Close to Chipset

SD CLK MS CLK



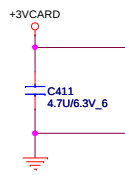
RTS5159 max output current for...
XD card 250mA
SD/MMC 250mA
MS/MSPRO 250mA



5 IN1 CARD-READER (PUSH-PUSH)

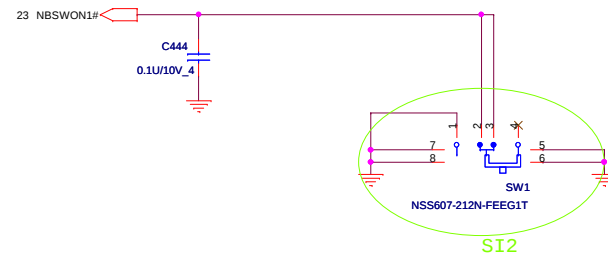
Support SD/SD PRO/MMC/MS/MS PRO/xD Cards

CLOSE to CONN

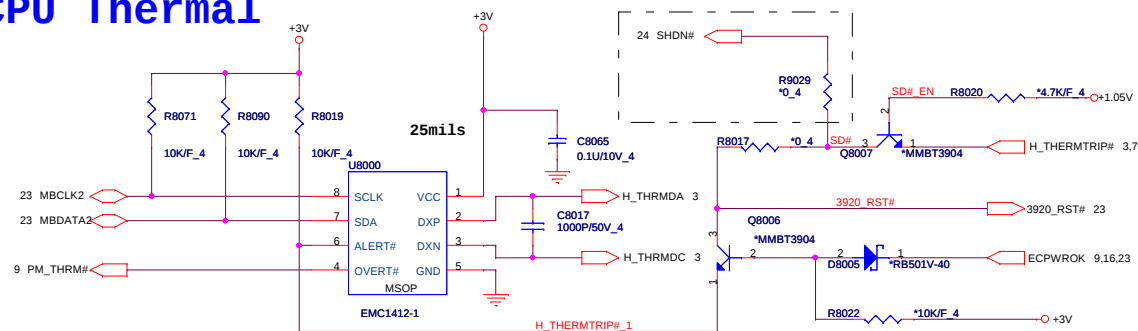


To Cardreader Connector





CPU Thermal

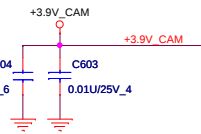
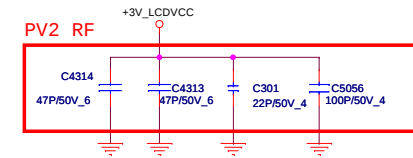


2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

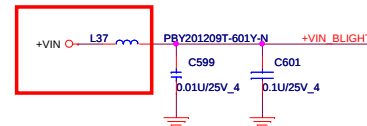
2,3,5,7,8,9,10,11,12,13,14,15,17,18,19,20,21,22,30	+3V
9,14,20,21,22,23,24,26,27,30	+3VPCU
10,12,17,19,20,22,30	+5V
24,25,26,27,29,30	+VIN

LED Panel(LDS)

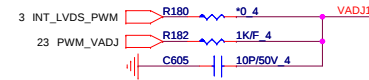
Request by HP RF(47Px2)



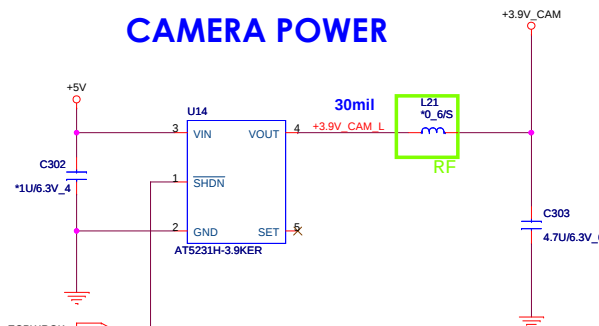
PV2 RF



Close to LCD Connector

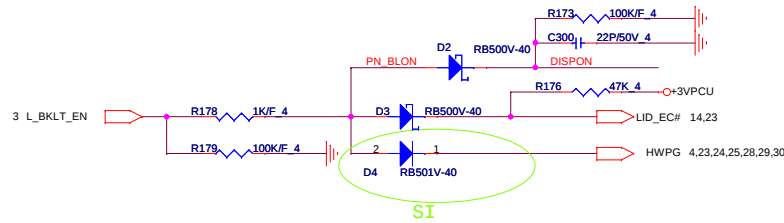


CAMERA POWER

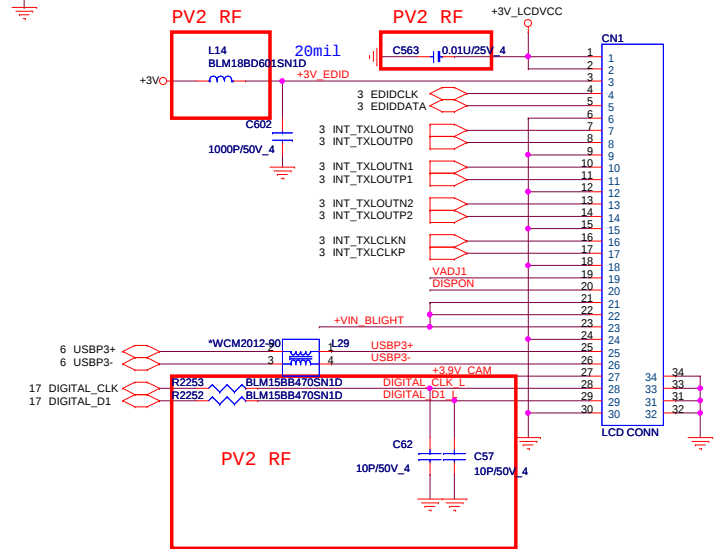
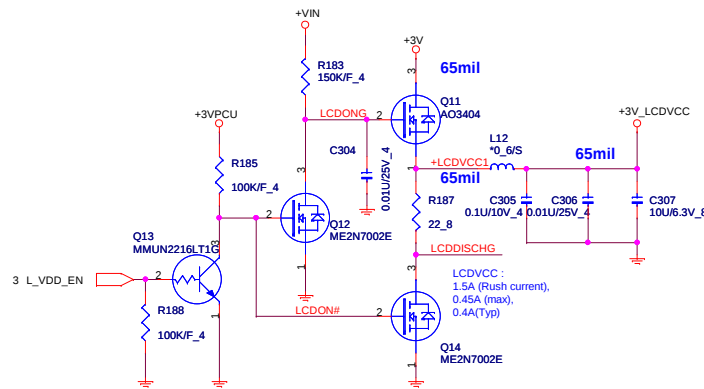


$$V_{out} = 1.25(1 + R1/R2)$$

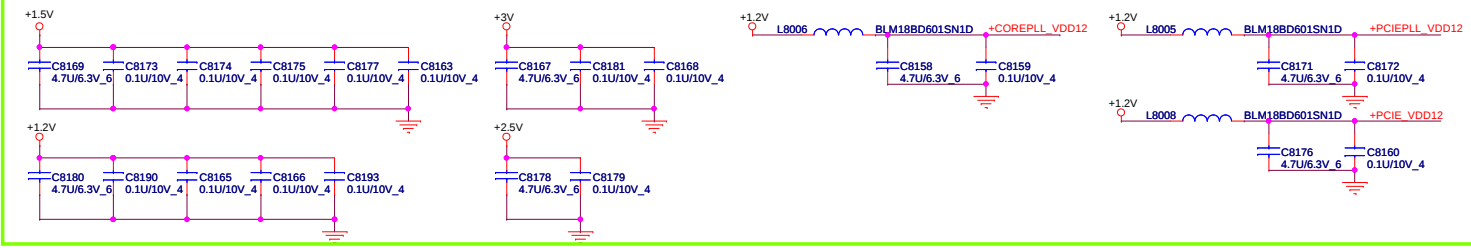
Backlight Control(LDS)



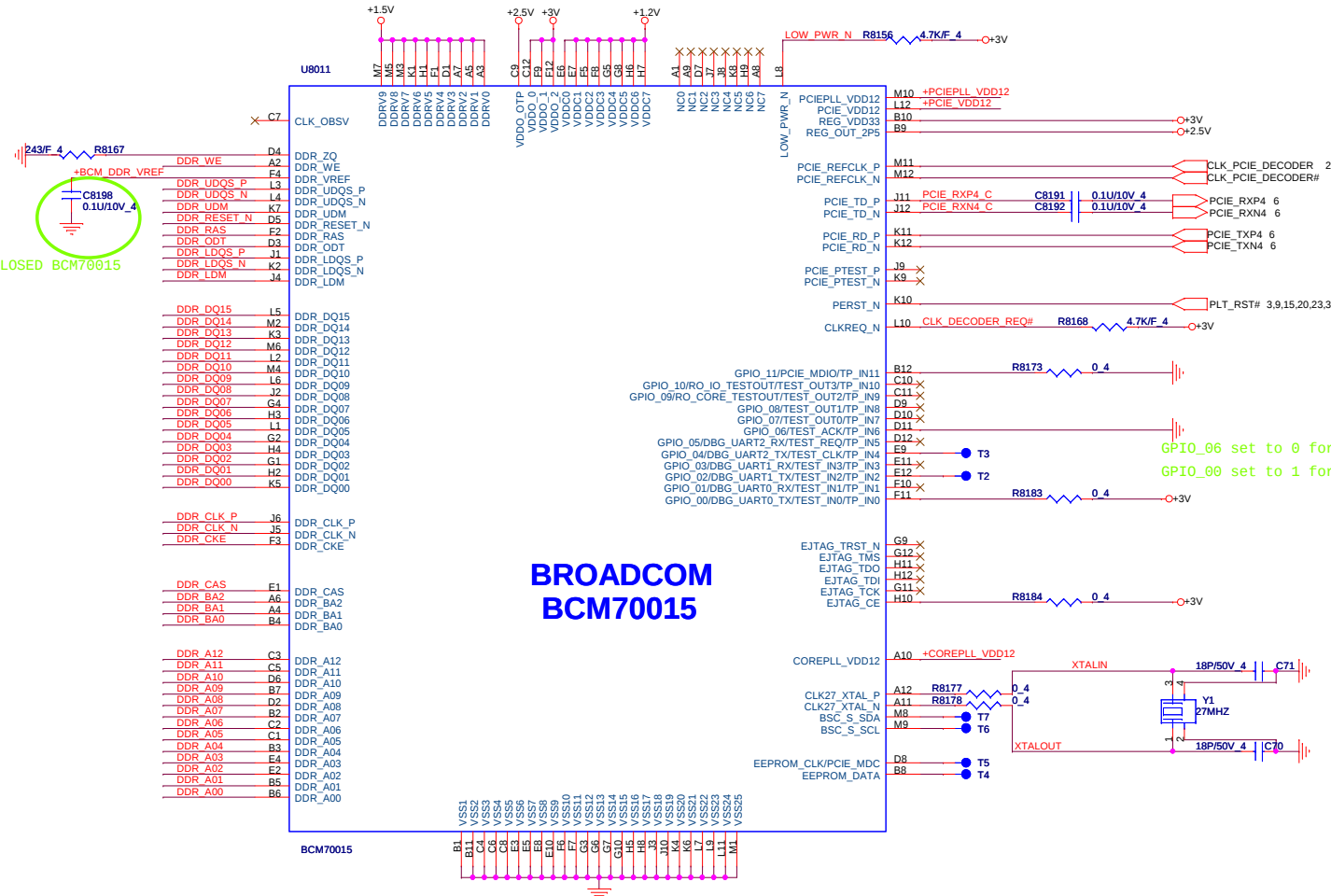
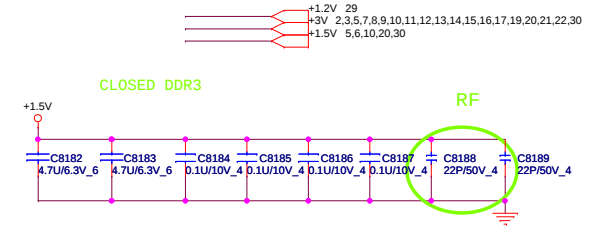
LCD POWER SWITCH







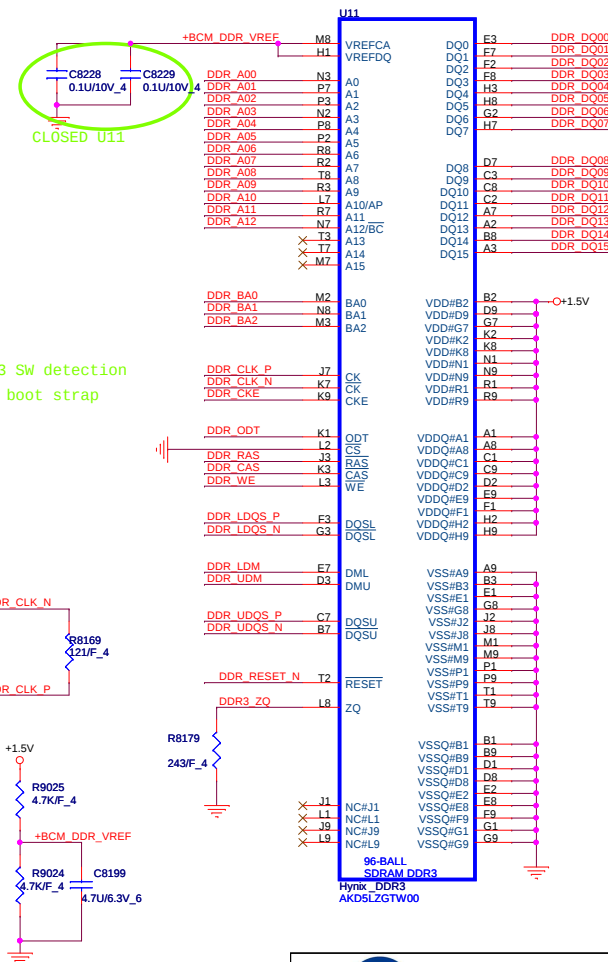
CLOSED BCM70015



BROADCOM BCM70015

DDR3 RAM Configuration Table

DESCRIPTION	Vendor	Vendor P/N	QCI P/N
DDR3 64Mx16, 128bit	800MHZ	HYNIX H5TQ1G63BFR-12C	AKD5LZGTW00
DDR3 64Mx16, 128bit	800MHZ	SAMSUNG K4W1G1646E-HC12	AKD5LGGT502

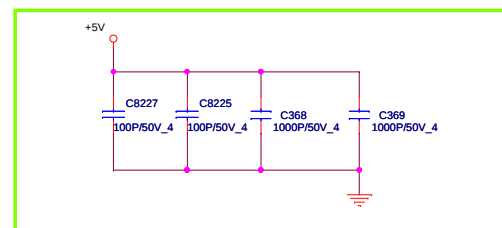
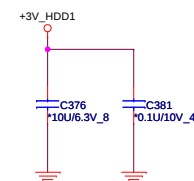
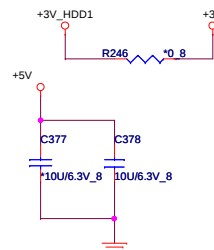
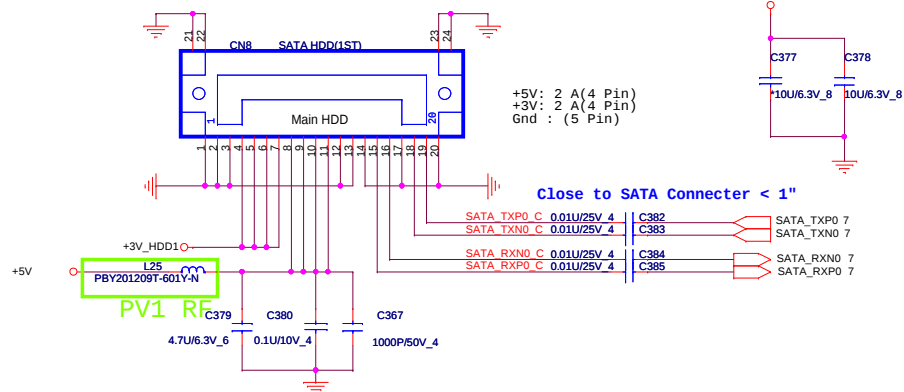


Quanta Computer Inc.

PROJECT : Annika

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DC Current rating: 0.5 A



PV1 RF

CPU SOCKET

H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H11 H12

H1-C31SD91P2 H2-B2X31S091P2 H3-B2X31S091P2 H4-C31SD91P2 H5-B2X31S091P2 H6-C31SD91P2 H7-B2X31S091P2 H8-C31SD91P2-NM6 H9-C31SD91P2 H10-C31SD91P2 H11-C31SD91P2 H12-AGND

mini card

H13 H14 H15 H16 H17 H18

H13-B2X31S091P2 H14-C217D10P2 H15-C217D10P2 H16-C217D10P2 H17-C217D10P2 H18-C217D10P2

FA

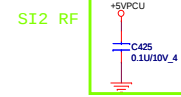
H19 H20

H19-C217D10P2 H20-B2X31S091P2

H13/17/18/19 要上件

FAN固定螺絲
H16要上件

 PAD1
 *spad-re236x591np
 PAD2
 *spad-re472x236np
 PAD3
 *spad-s236np

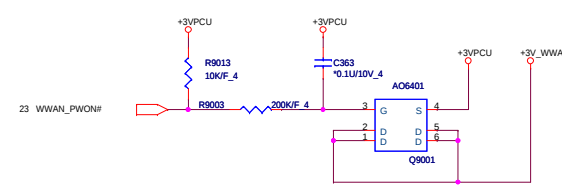


The value of the capacitor is suggest by Siemens HQ expert.
For against 900MHz RF interference. The value of capacitor is 27pF.
For against 1800MHz RF interference. The value of capacitor is 10pF.
1nF/10nF value capacitor use for against ESD purpose.

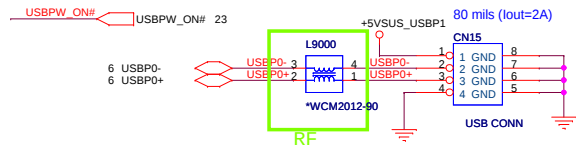
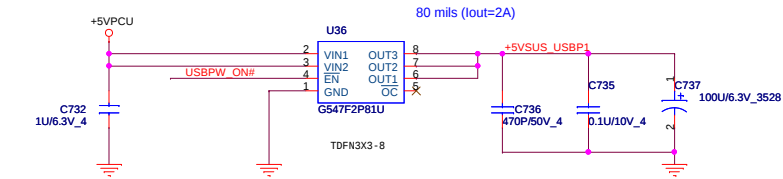


SI2 RF

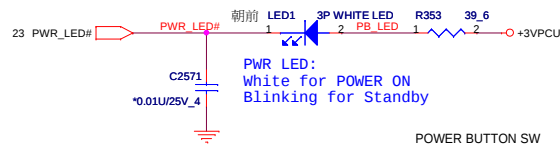
The diagram shows a green rectangular area representing a PCB layout. Inside, a red wire connects a red circle labeled '+5VPCU' to a blue capacitor symbol labeled 'C426'. Below the capacitor is the text '0.1U/10V_4'. A red wire connects the bottom of the capacitor to a ground symbol (three horizontal lines of decreasing width).



1x Left side USB port supports Keyed USB.



PWR Button/LED

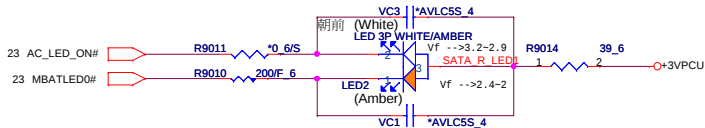


POWER BUTTON SW

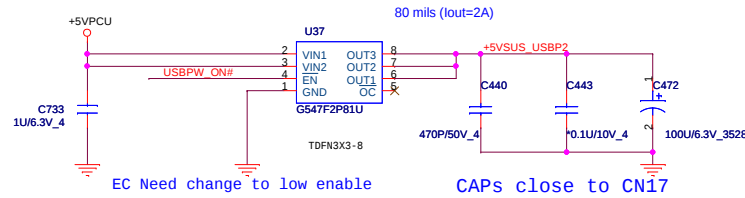
SATA/LED



Charging & Discharging/LED

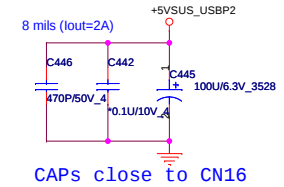


For Right 2xUSB Ports PWR

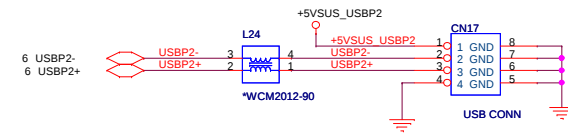
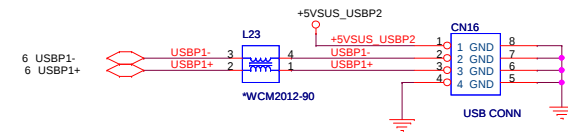


EC Need change to low enable

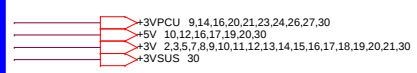
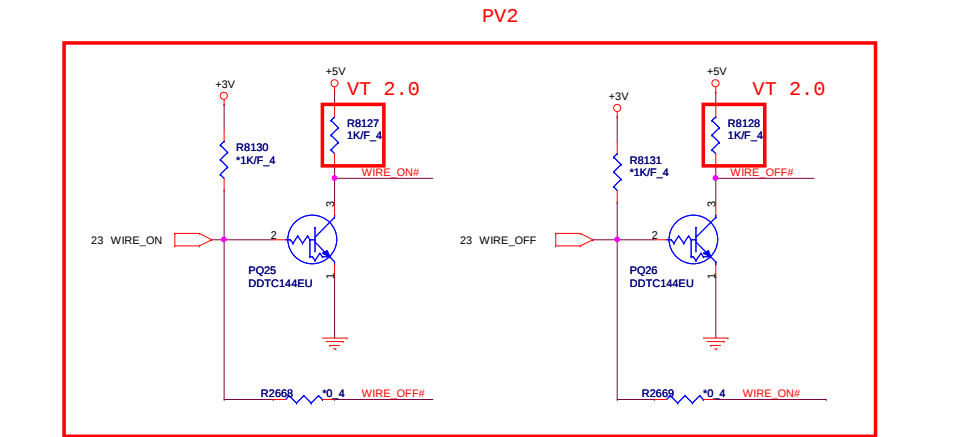
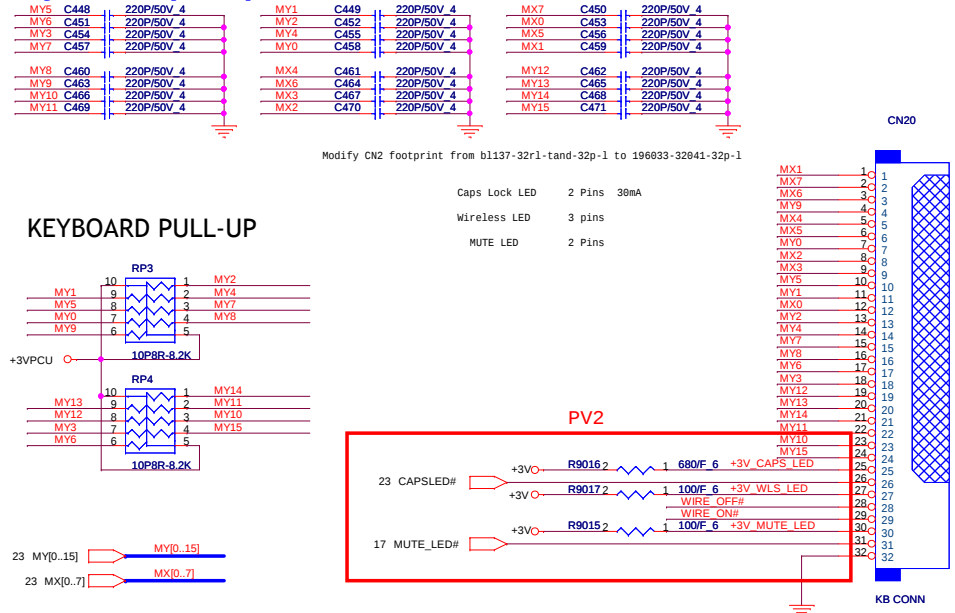
CAPS close to CN17



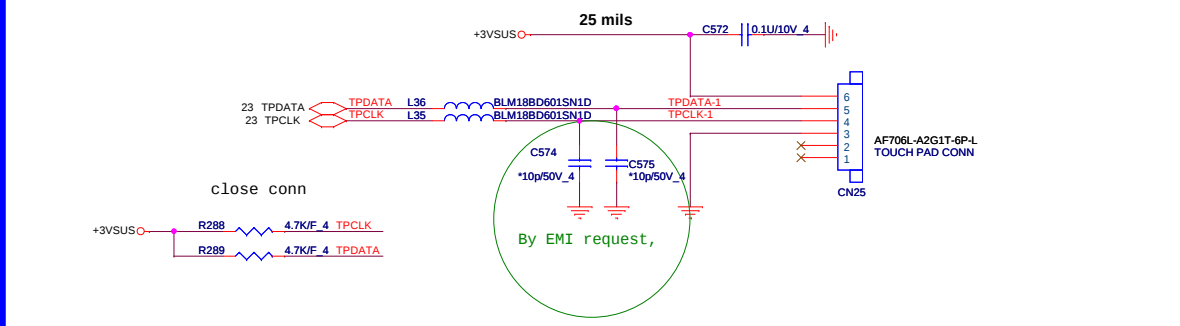
CAPS close to CN16



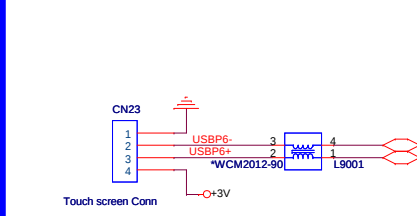
Keyboard (KBC)



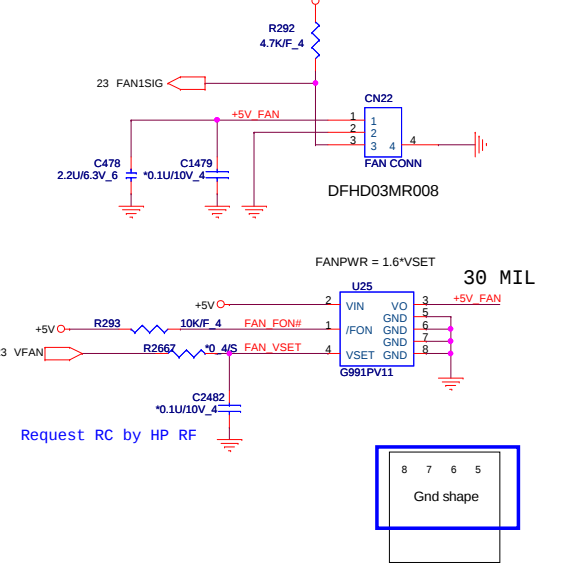
TOUCH PAD CONNECTOR



TOUCH SCREEN

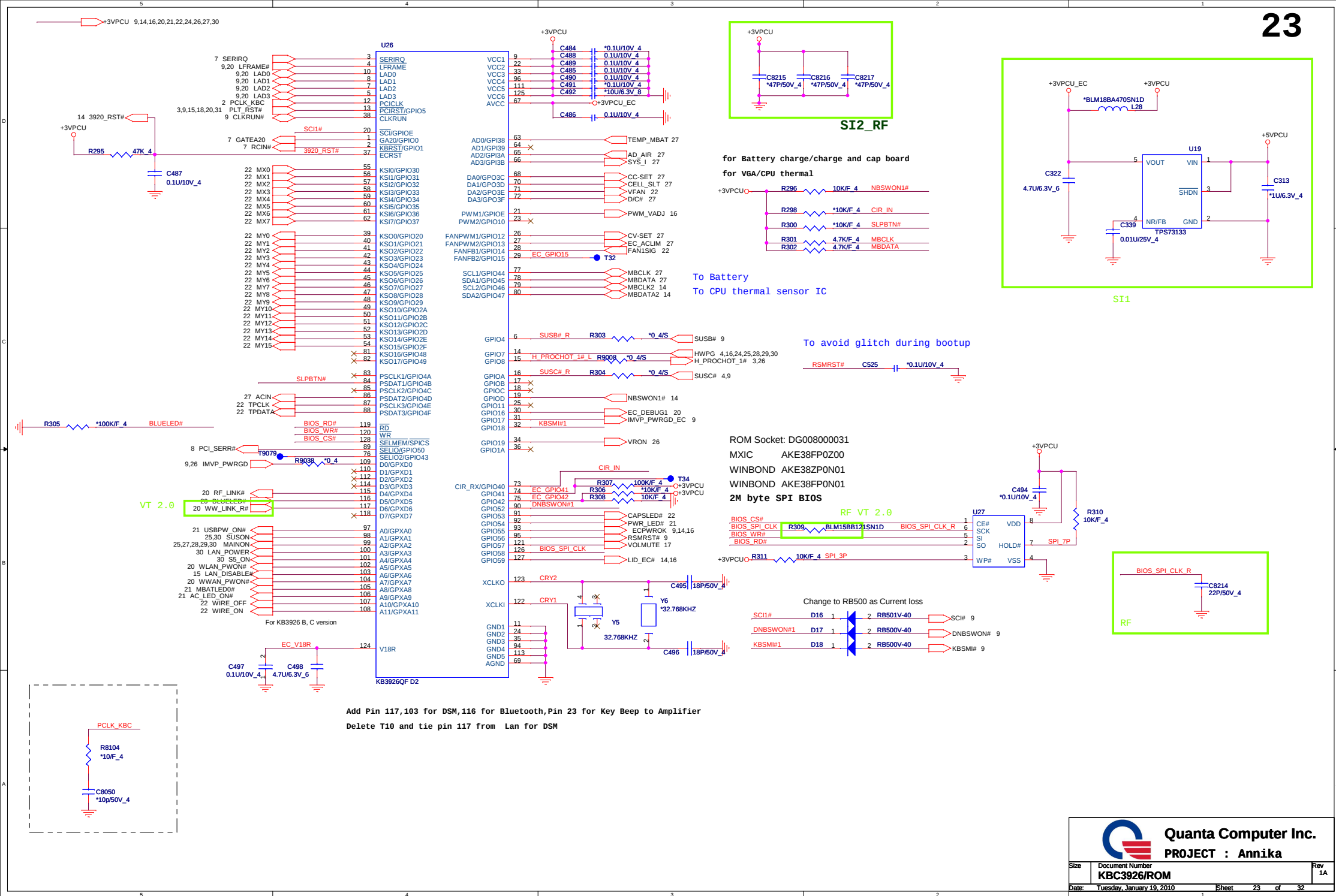


CPU FAN



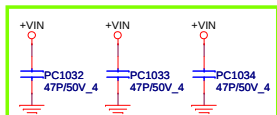
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	KB/TP/BI/CPU FAN/TP SCREEN	1A
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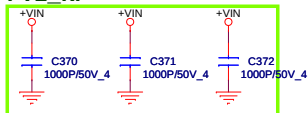


DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

SI2_RF

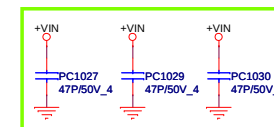


PV1_RF

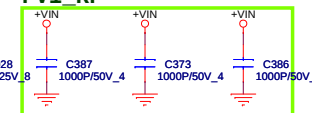


+5VPCU Volt +/- 5%
Countinue current:4A
Peak current:5.5A
OCp minimum 6A

SI2_RF

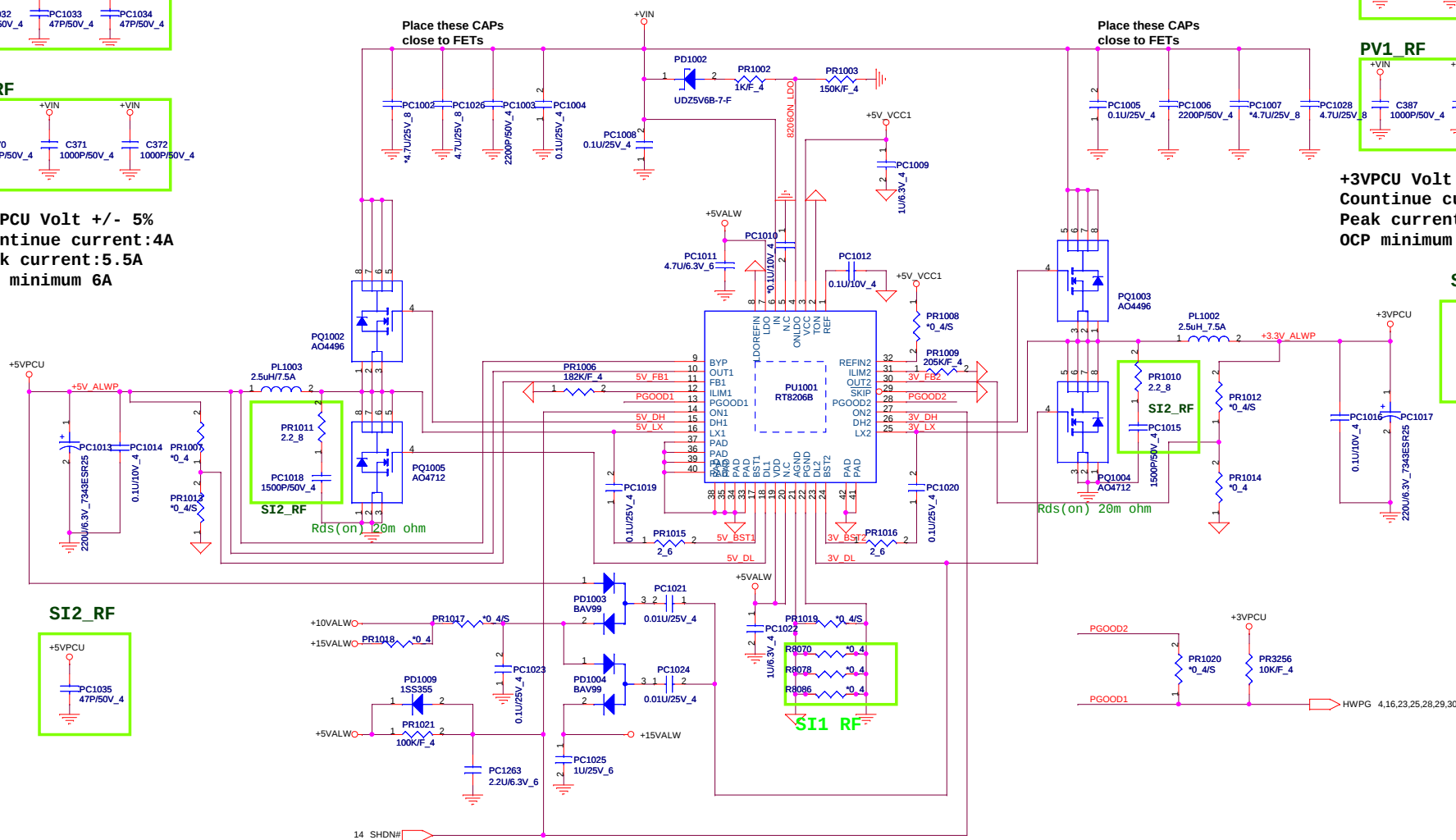
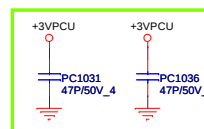


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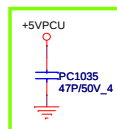


+3VPCU Volt +/- 5%
Countinue current:4A
Peak current:5.5A
OCp minimum 6A

SI2_RF



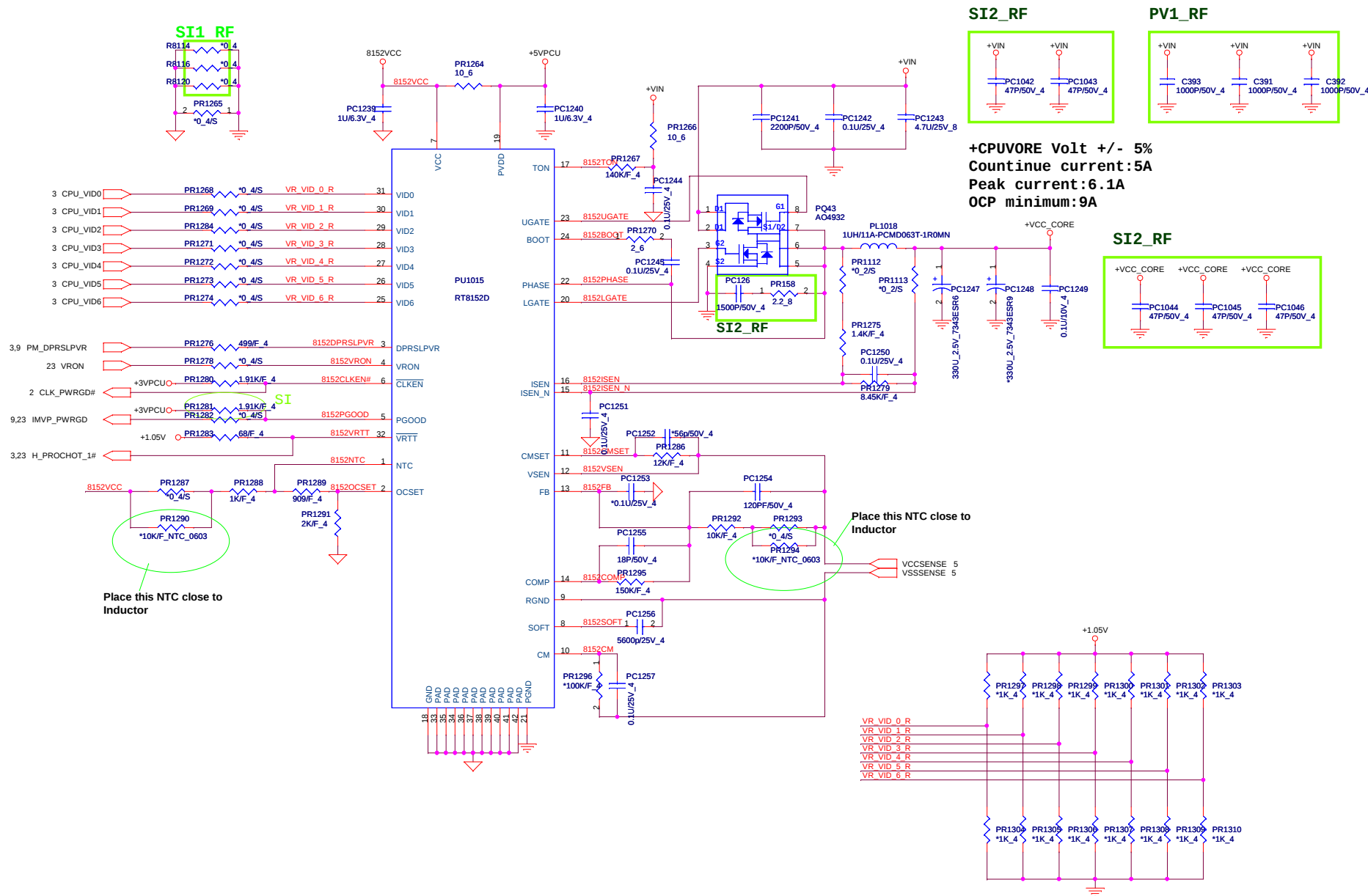
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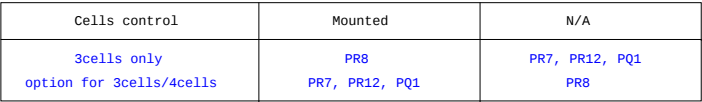


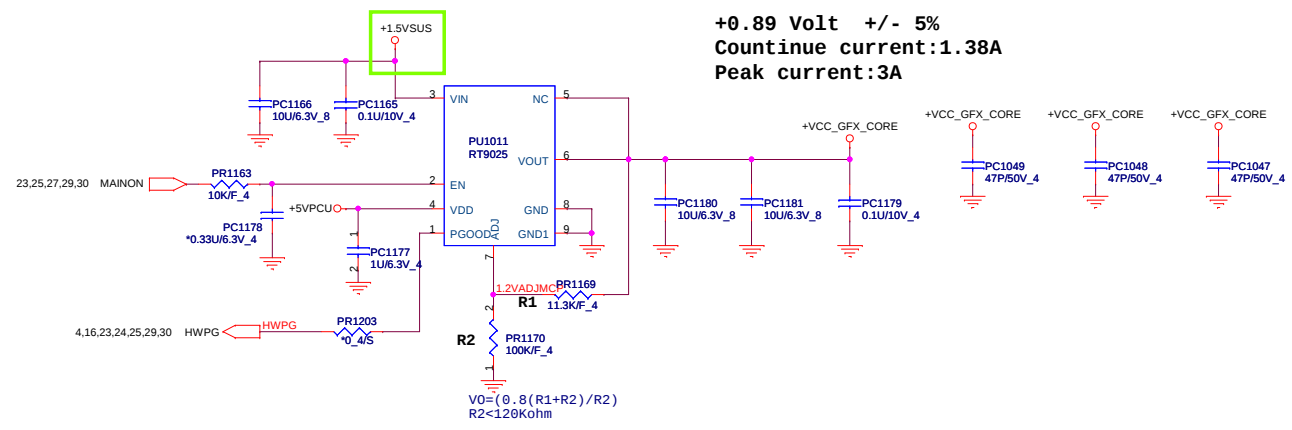
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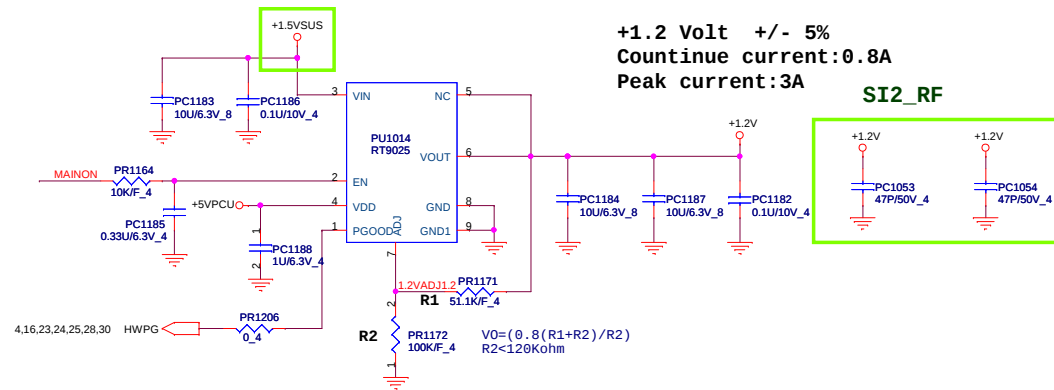
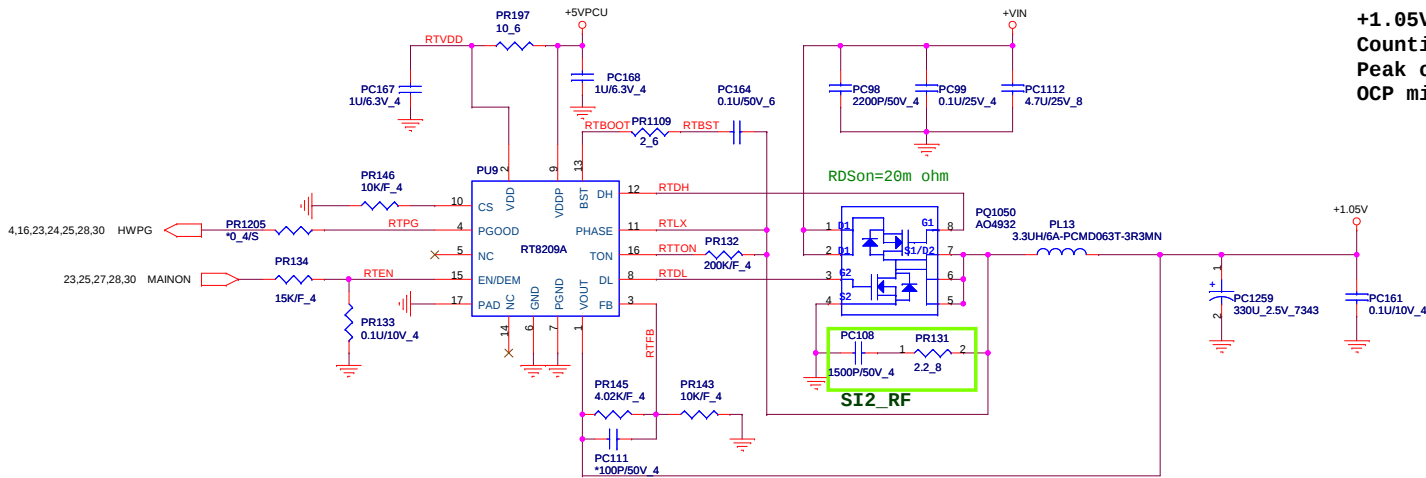








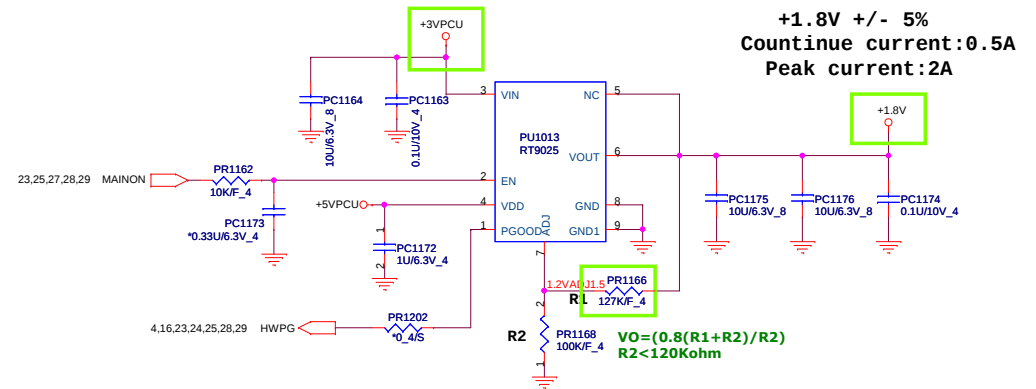
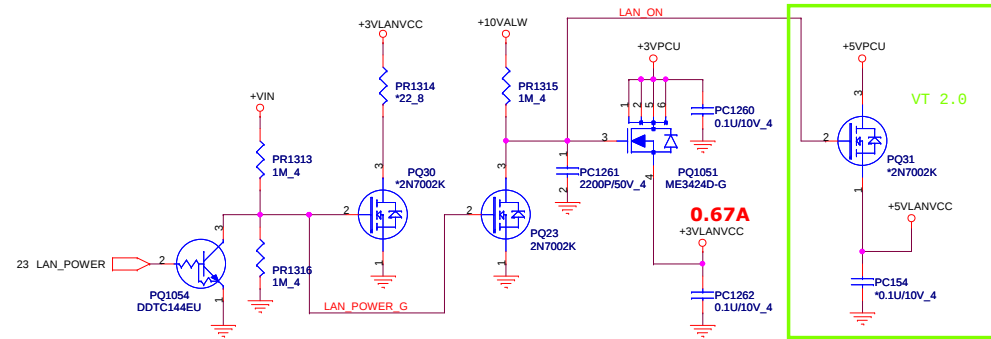
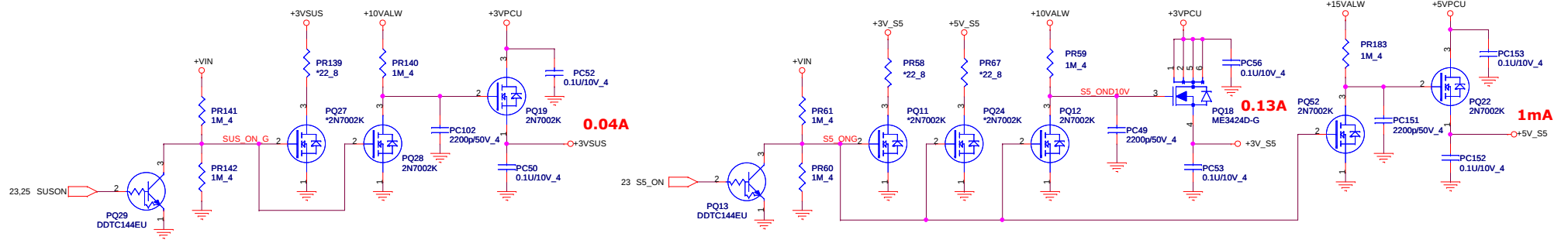
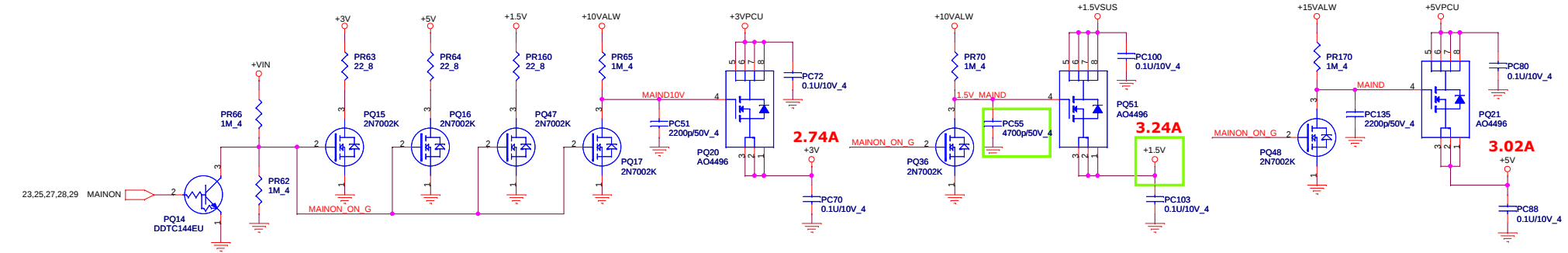




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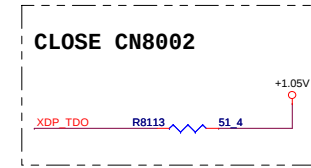
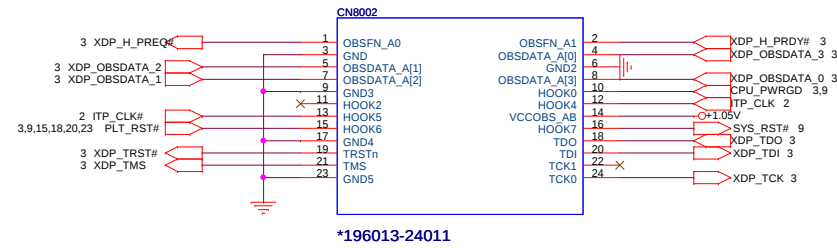
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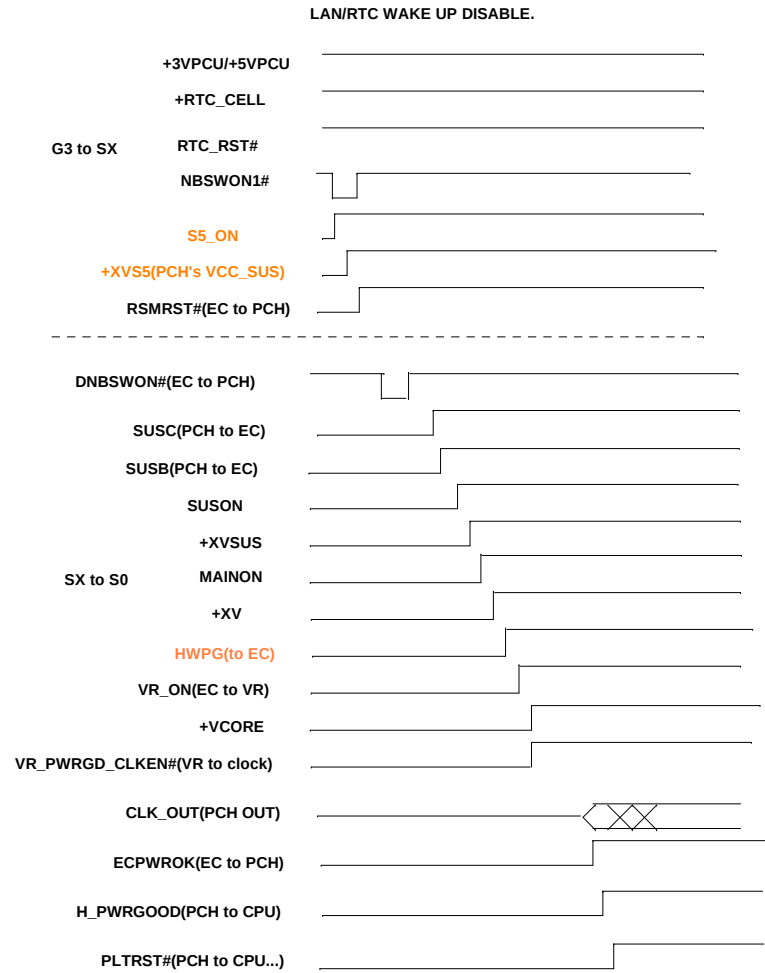
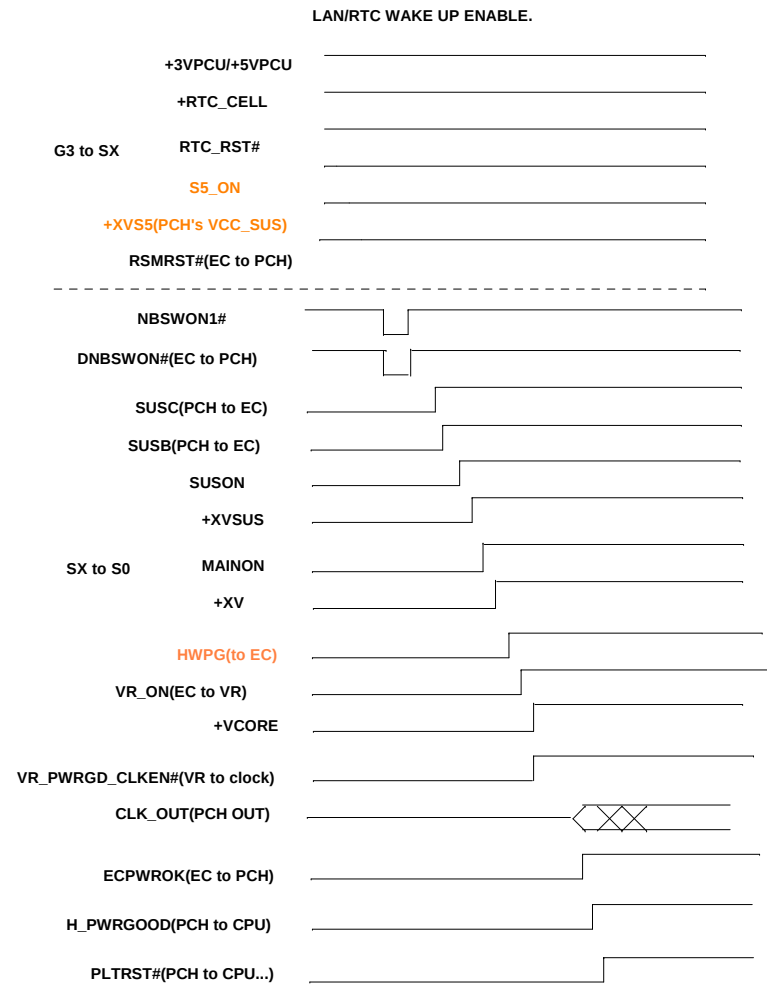
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CPU XDP



Power up sequence



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