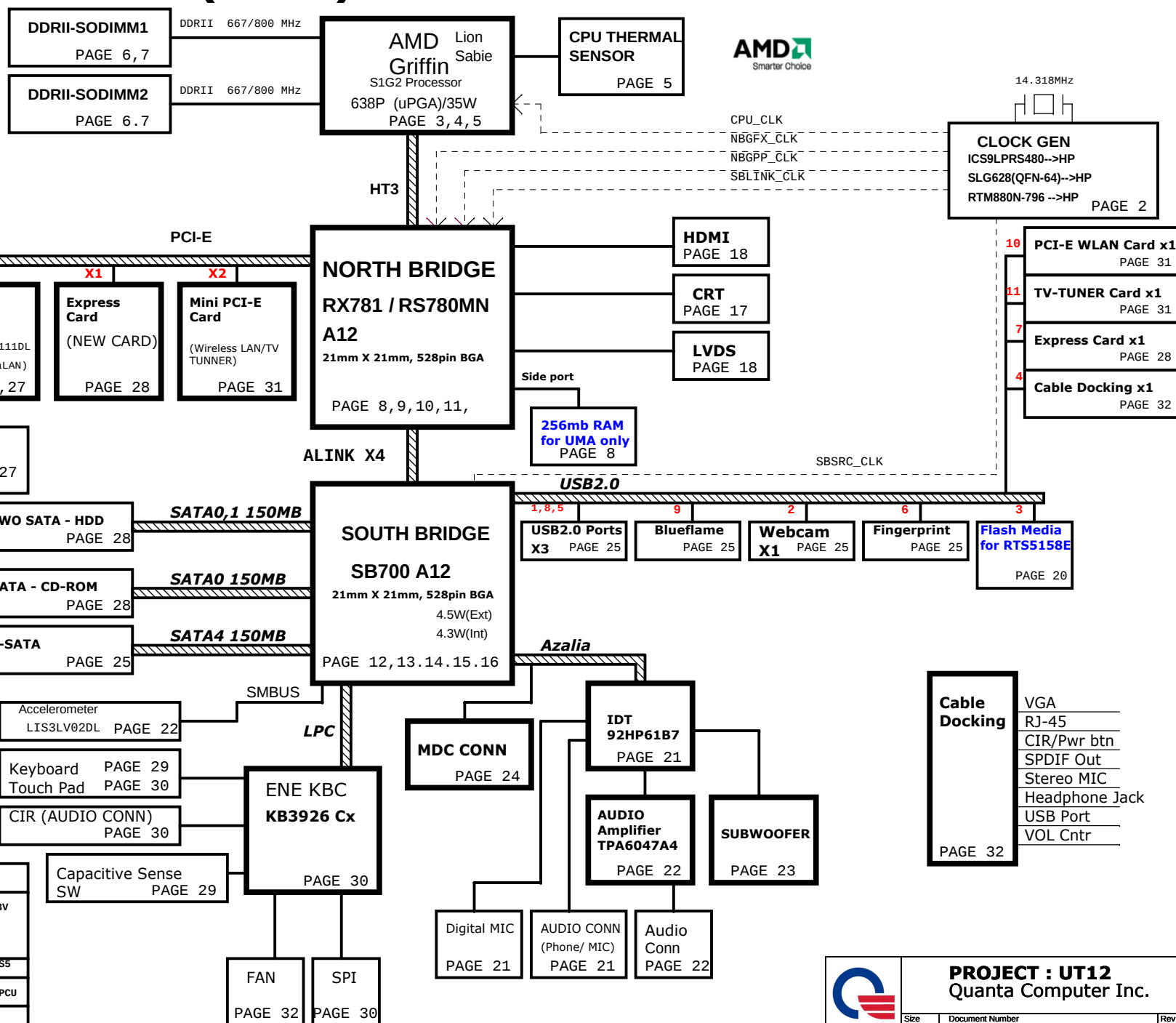


UT12(UMA) SYSTEM DIAGRAM

01

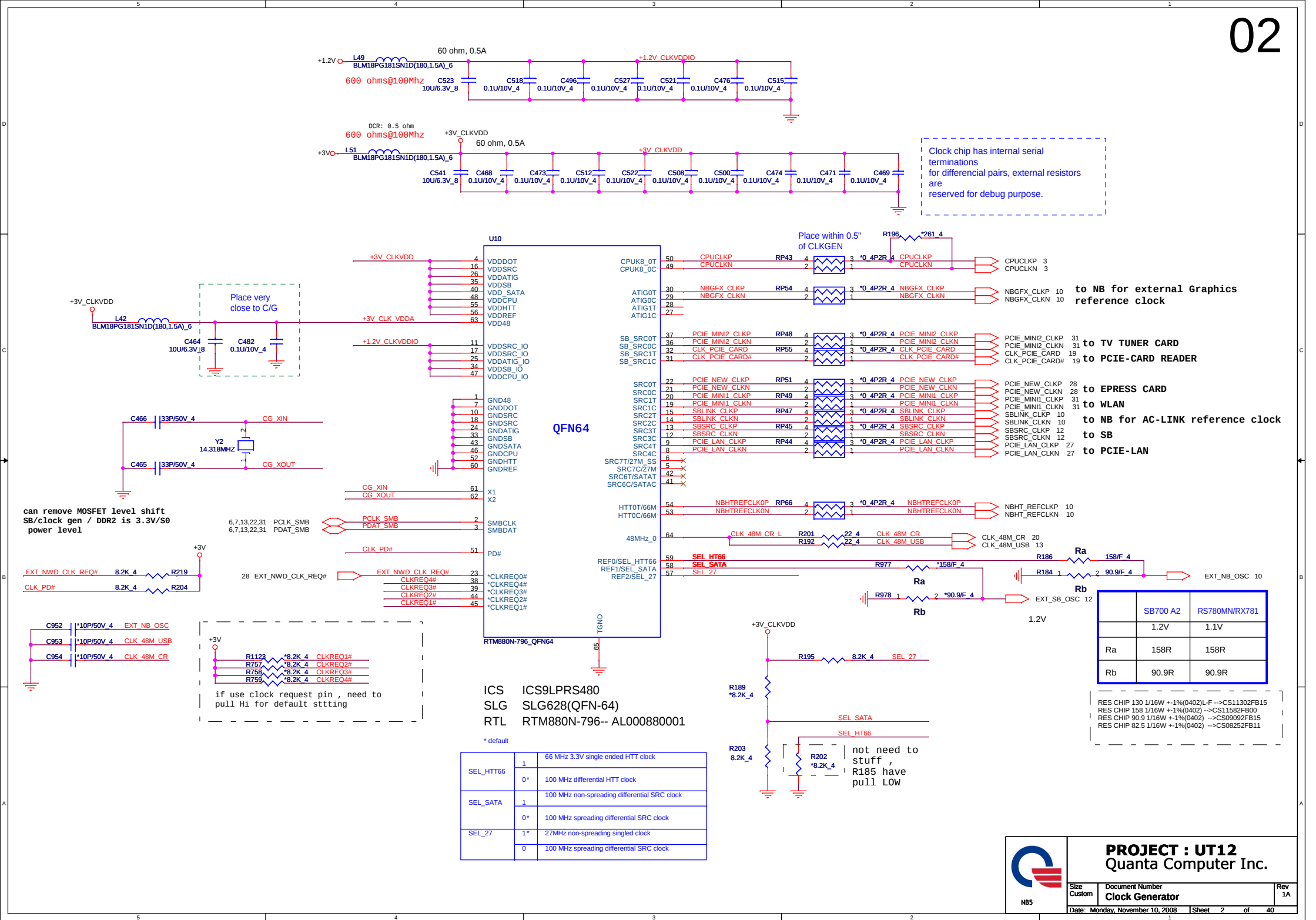
PCB STACK UP

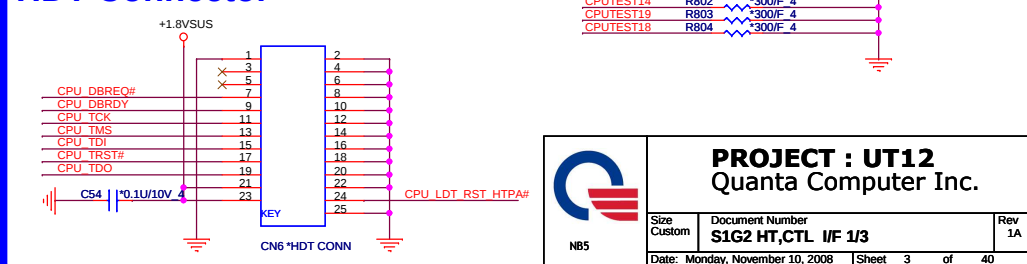
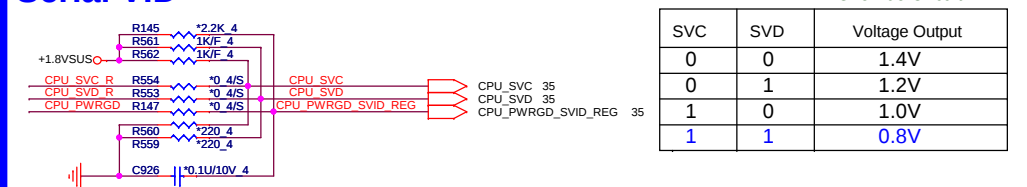
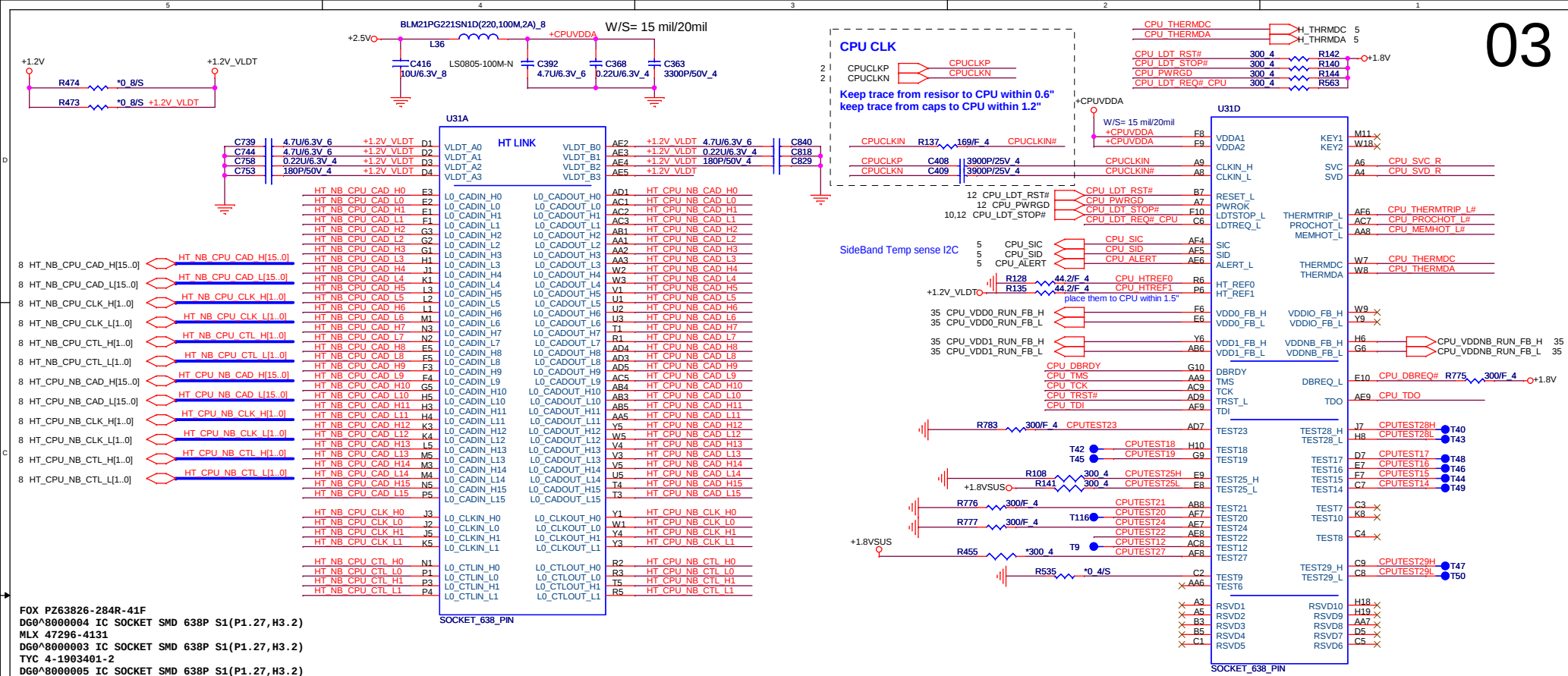
LAYER 1 : TOP
LAYER 2 : IN1
LAYER 3 : IN2
LAYER 4 : VCC
LAYER 5 : IN3
LAYER 6 : BOT



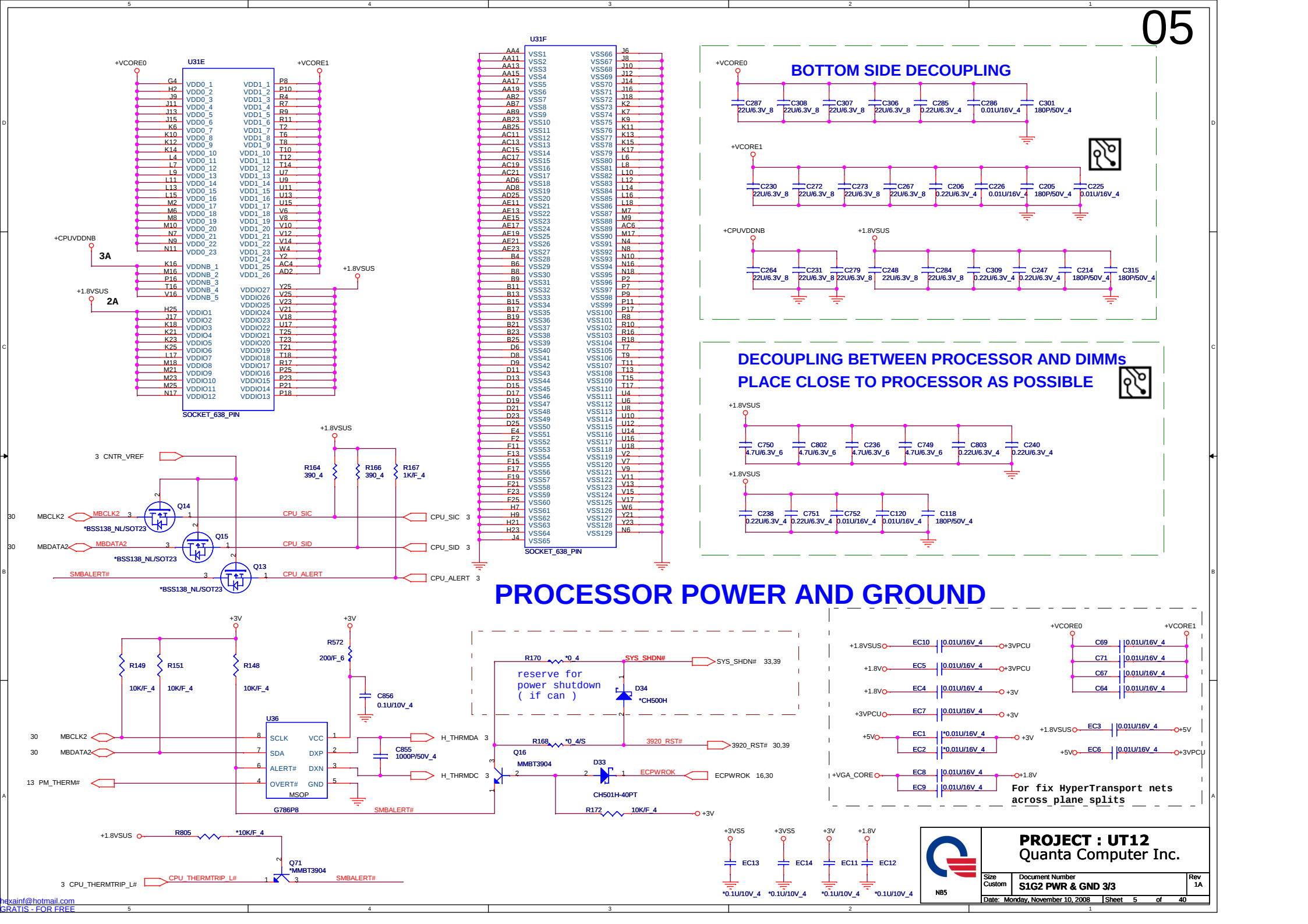
PROJECT : UT12
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A
Date: Monday, November 10, 2008	Sheet 1 of 40	









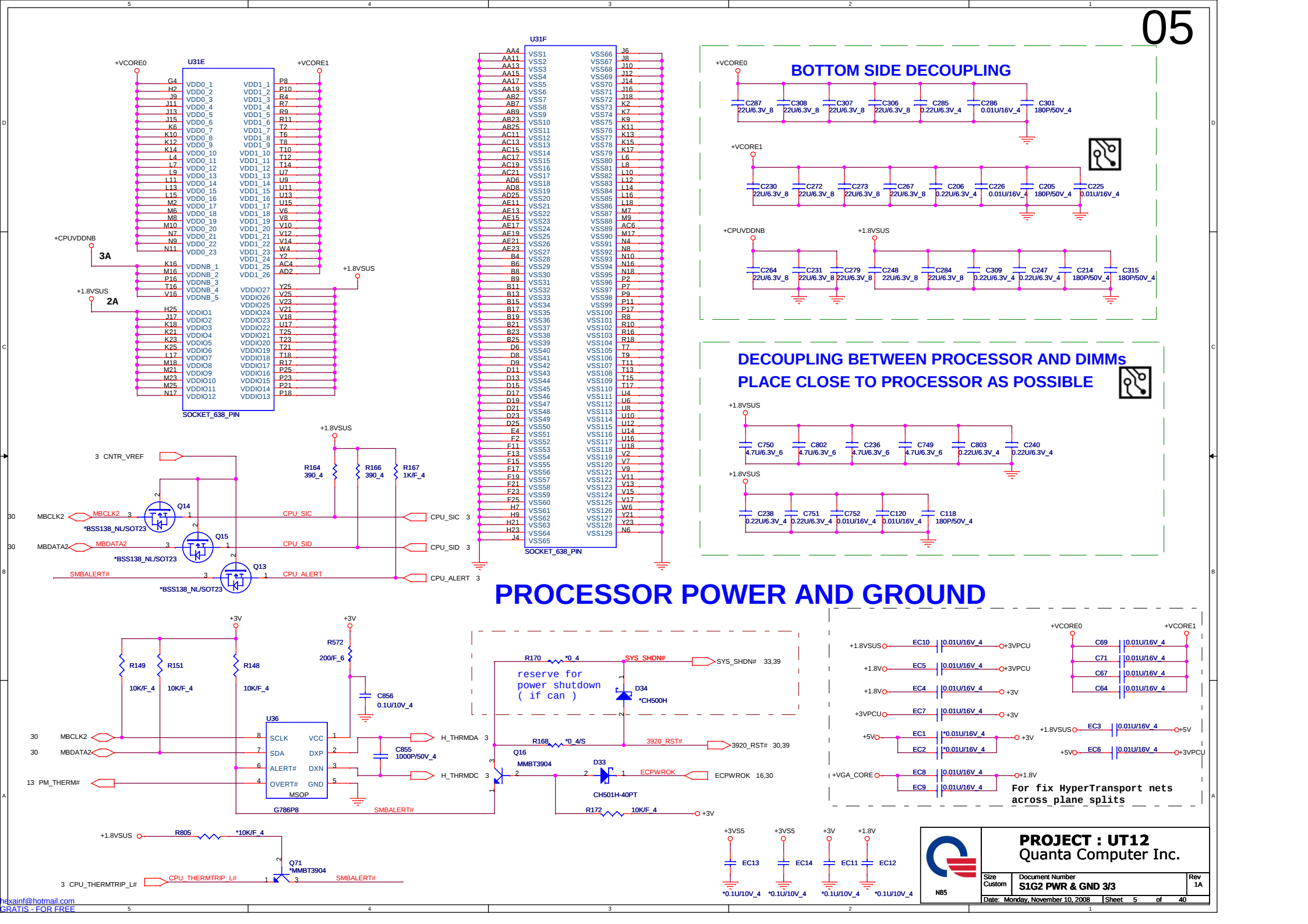
PROCESSOR POWER AND GROUND

BOTTOM SIDE DECOUPLING

DECOUPLING BETWEEN PROCESSOR AND DIMMS
PLACE CLOSE TO PROCESSOR AS POSSIBLE

PROJECT : UT12
Quanta Computer Inc.

Size Custom Document Number S1G2 PWR & GND 3/3 Rev 1A
Date: Monday, November 10, 2008 Sheet 5 of 40



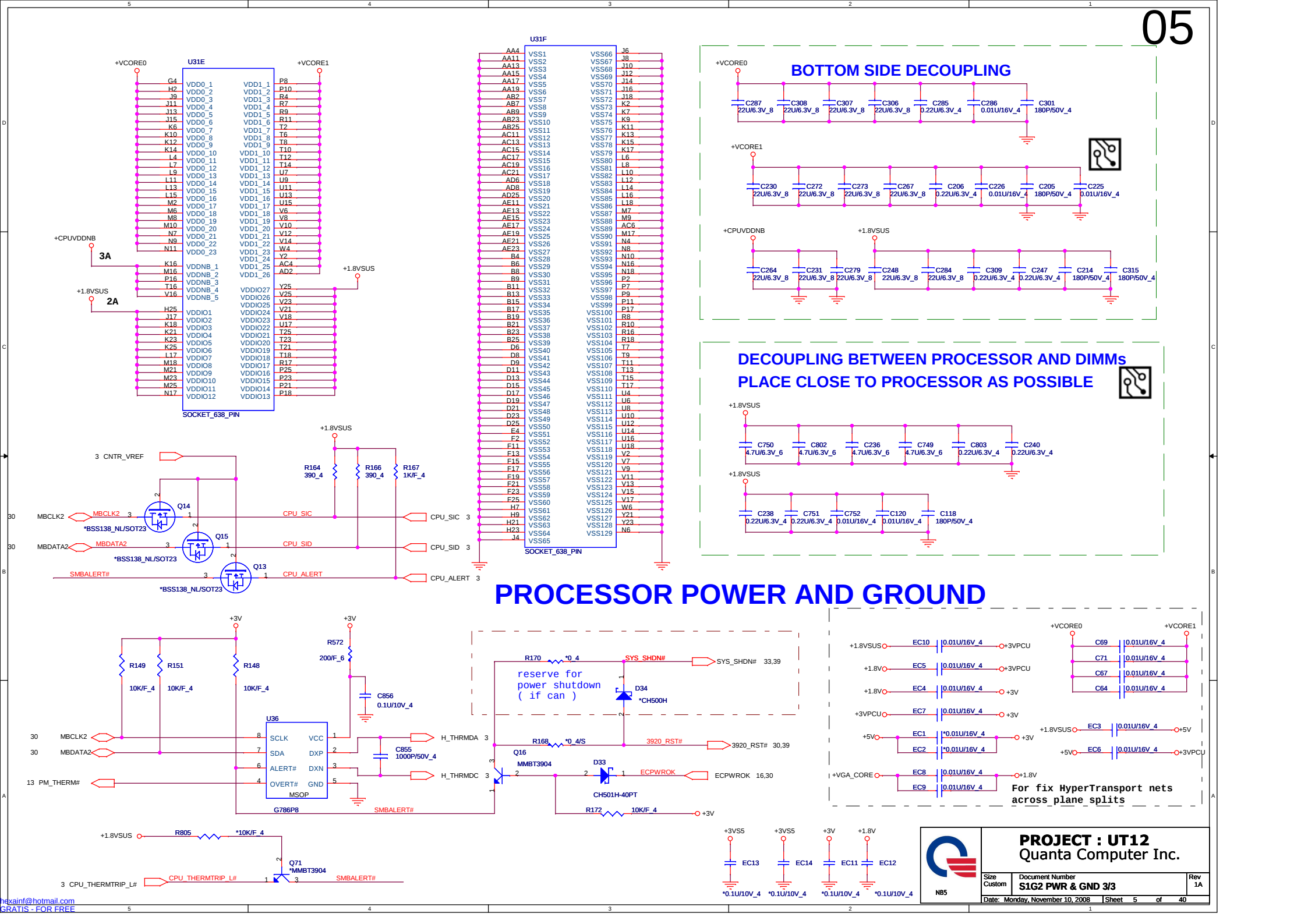
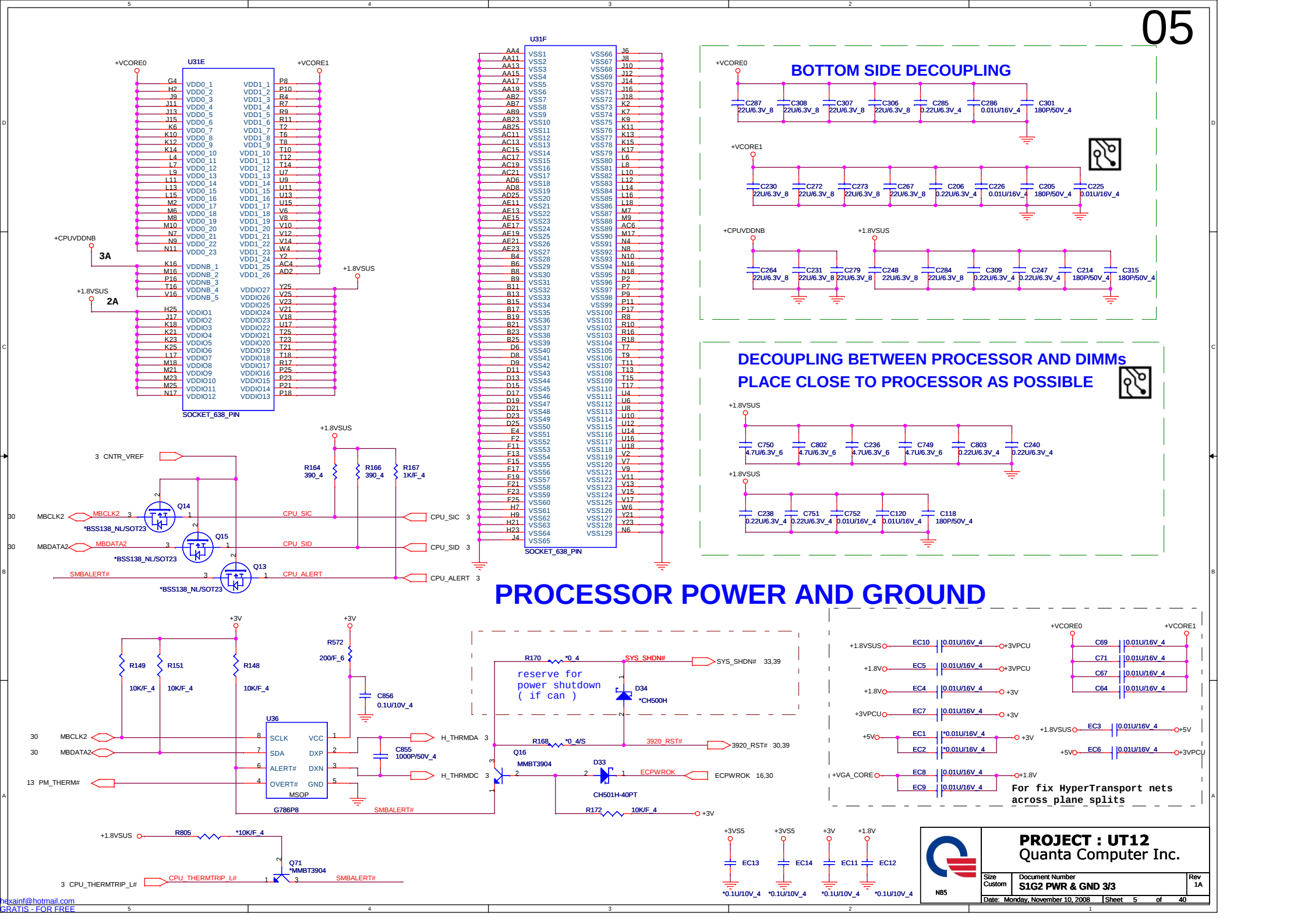
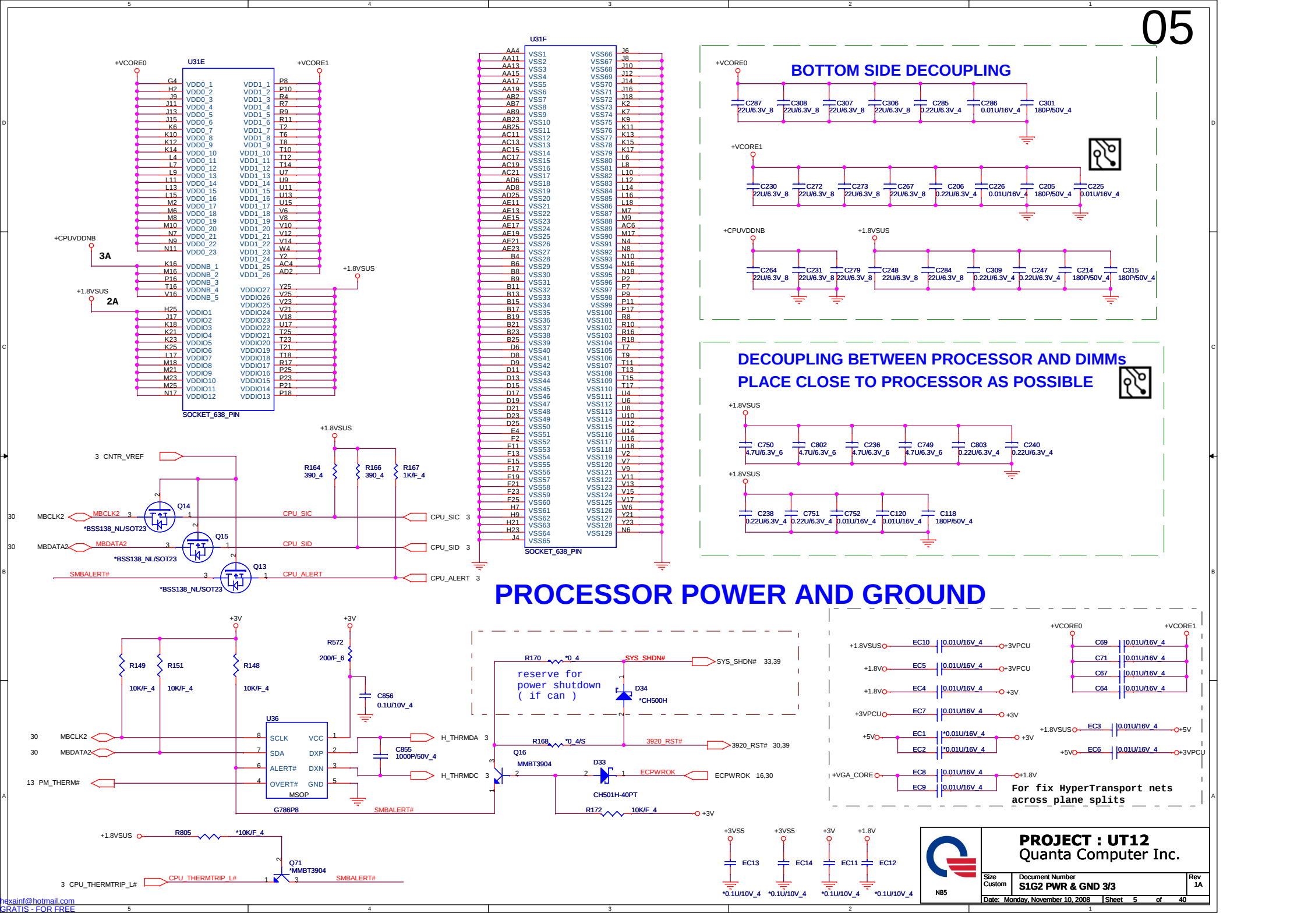
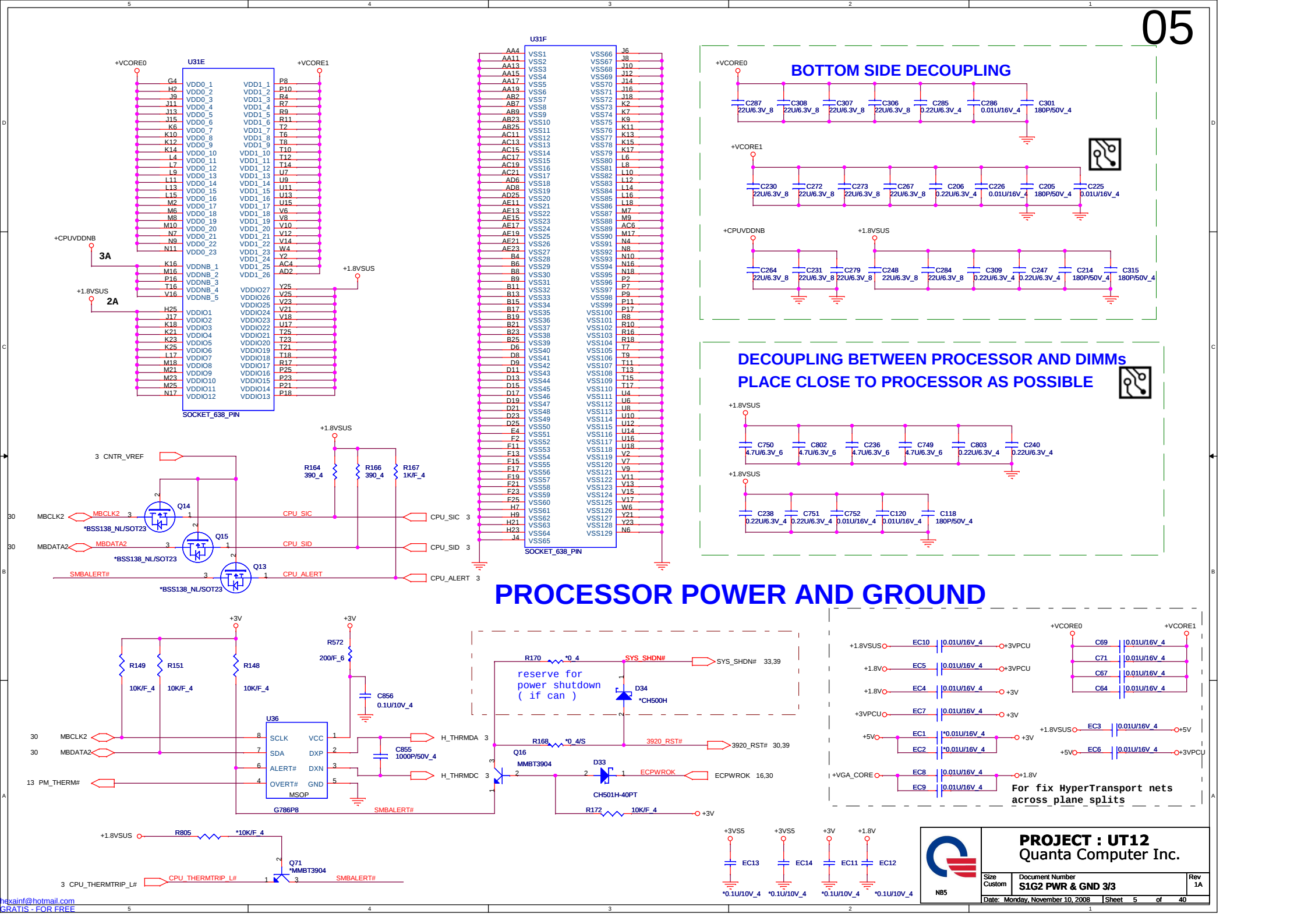
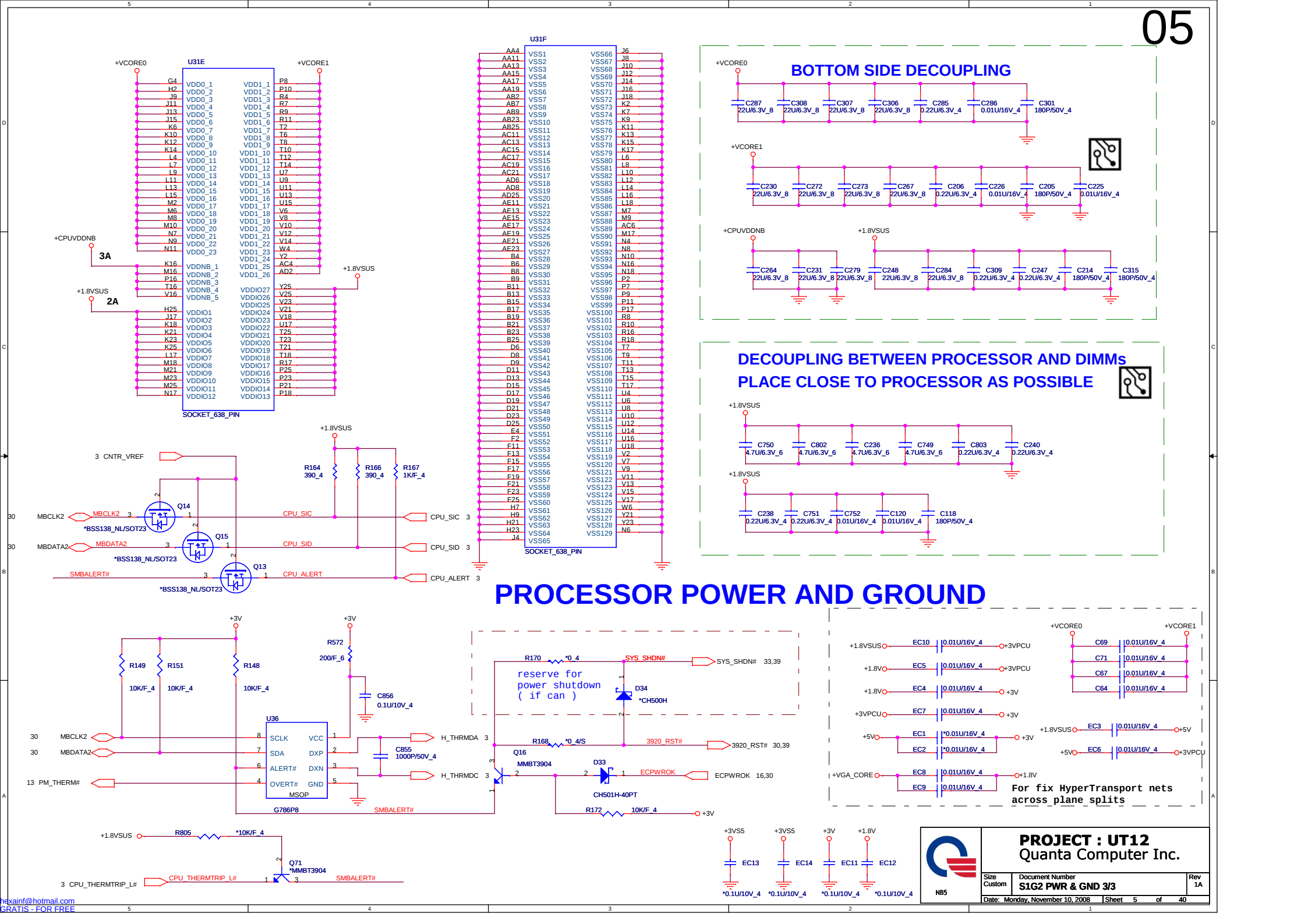
PROCESSOR POWER AND GROUND

BOTTOM SIDE DECOUPLING

DECOUPLING BETWEEN PROCESSOR AND DIMMS
PLACE CLOSE TO PROCESSOR AS POSSIBLE

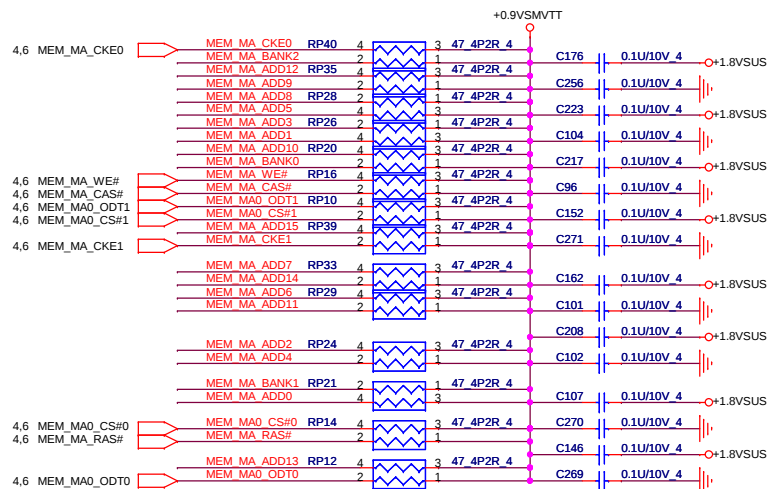
PROJECT : UT12
Quanta Computer Inc.

Size Custom Document Number S1G2 PWR & GND 3/3 Rev 1A
Date: Monday, November 10, 2008 Sheet 5 of 40

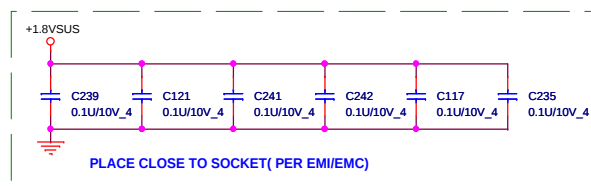




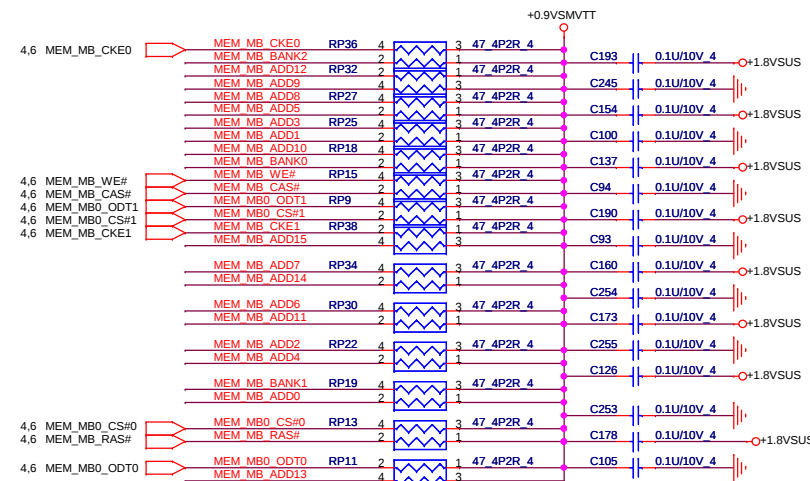
4,6 MEM_MA_ADD[0..15]  MEM_MA_ADD[0..15]
4,6 MEM_MA_BANK[0..2]  MEM_MA_BANK[0..2]



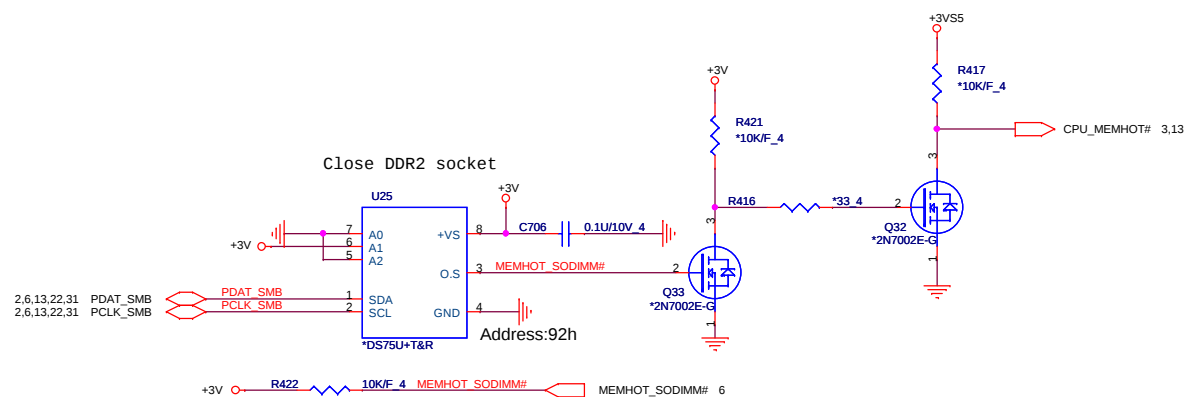
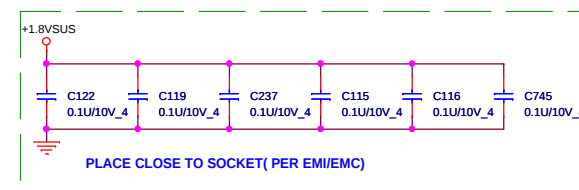
PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



4,6 MEM_MB_ADD[0..15]  MEM_MB_ADD[0..15]
4,6 MEM_MB_BANK[0..2]  MEM_MB_BANK[0..2]

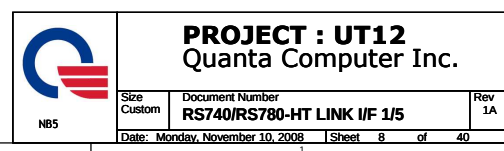
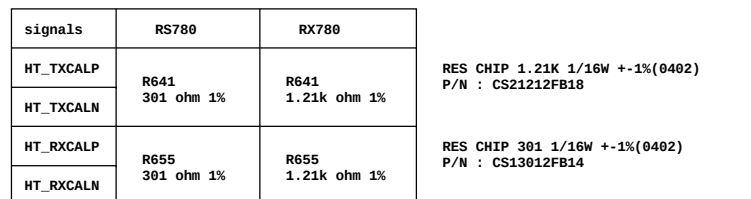


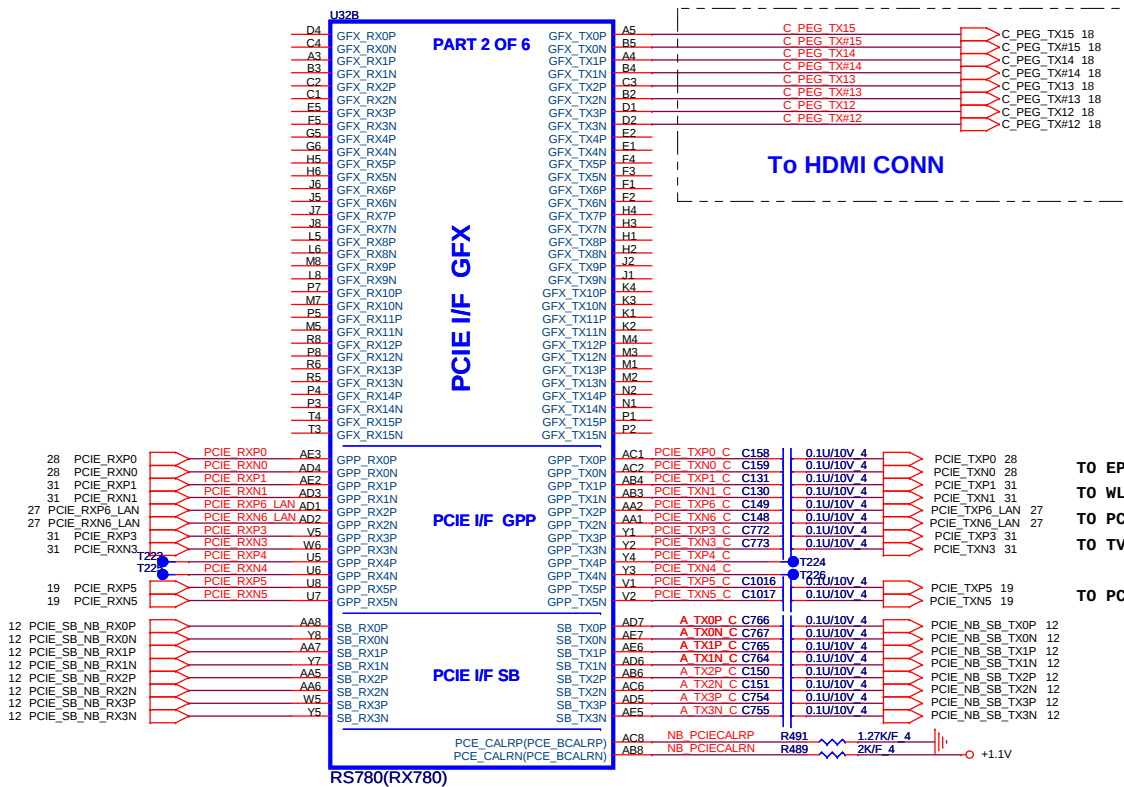
PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



PROJECT : UT12
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
DDR2 SODIMMS TERMINATIONS		
Date: Monday, November 10, 2008	Sheet 7 of 40	





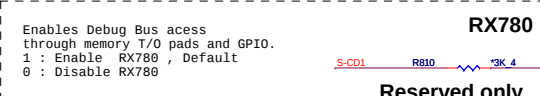
TO EPRESS CARD
TO WLAN
TO PCIE-LAN
TO TV TUNNER
TO PCIE CARD READER

RX780/RS740/RS780 difference table (PCIE LINK)

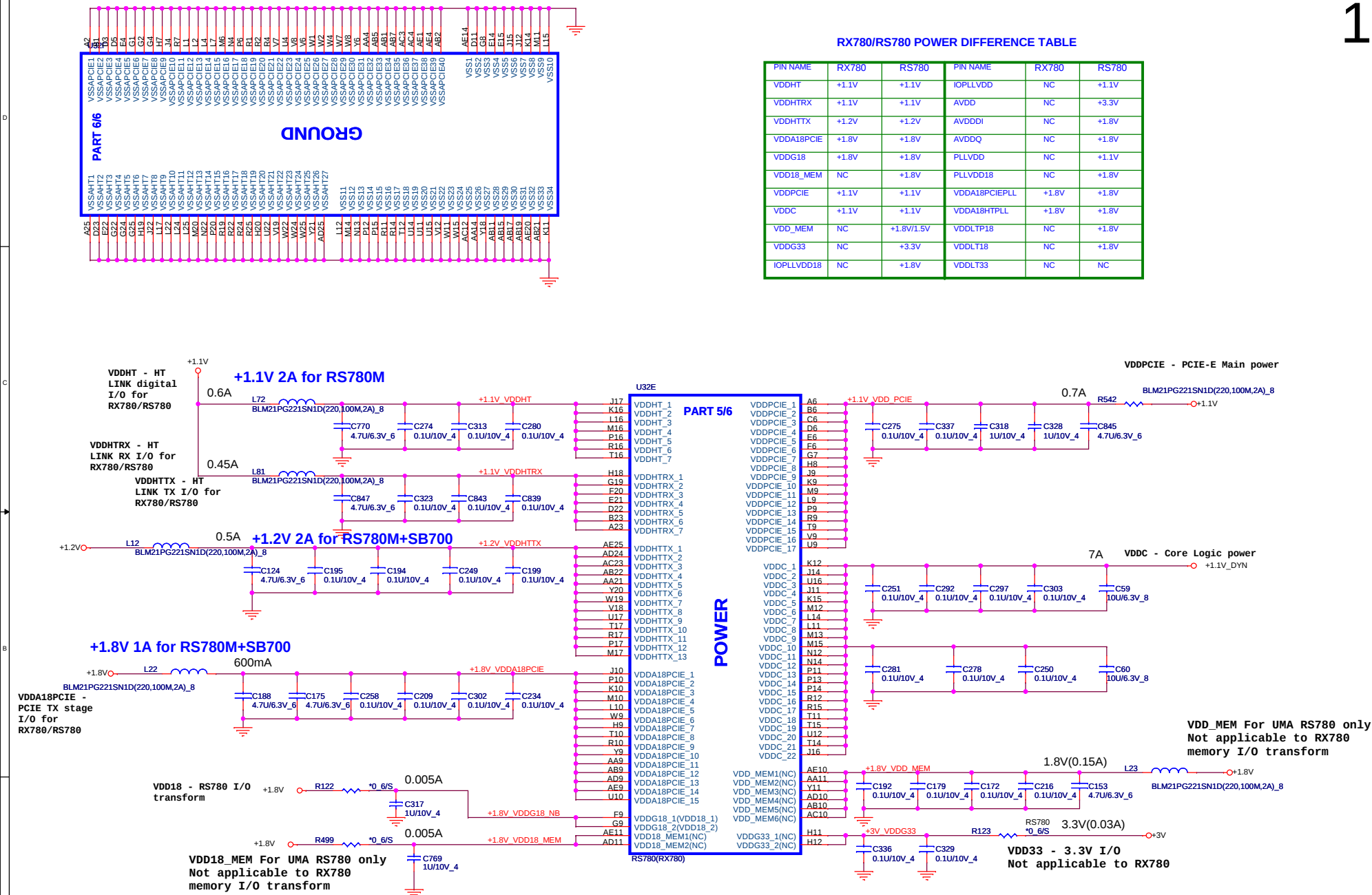
	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1



PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTPI8	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDLT33	NC	NC





Size Custom	Document Number SB700-PCIE/PCI/CPU/LPC 1/4	Rev 1/
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Size Custom	Document Number SB700-PWR/DECOUPLING 4/4	Rev 1A
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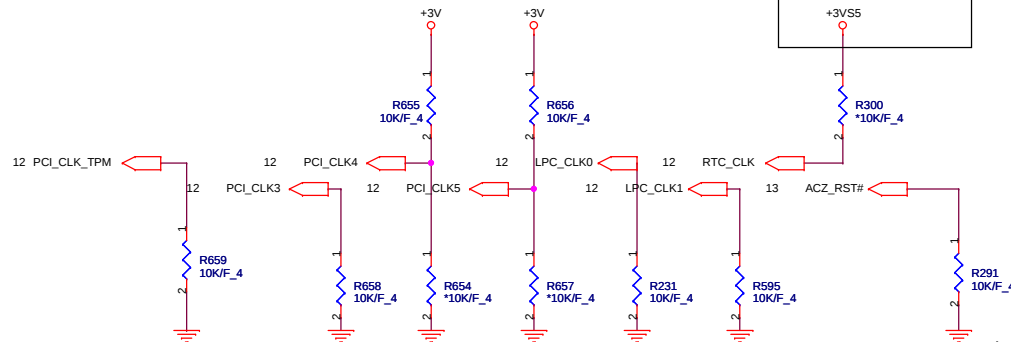


OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OF RESISTORS.

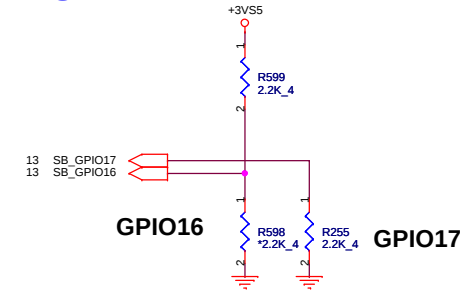
16

It must ready
before RSMRST#

REQUIRED STRAPS



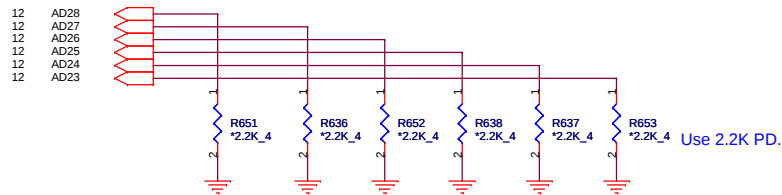
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

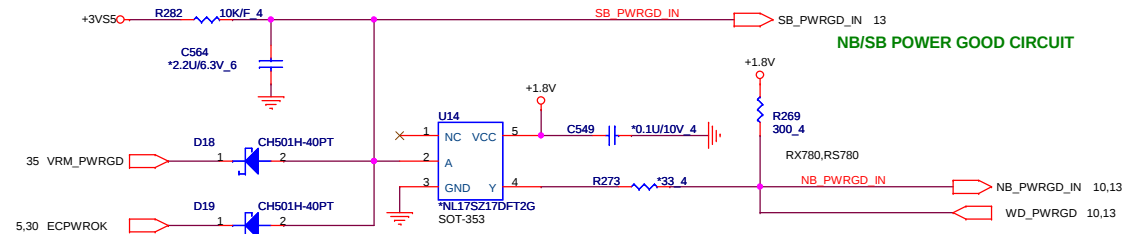
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



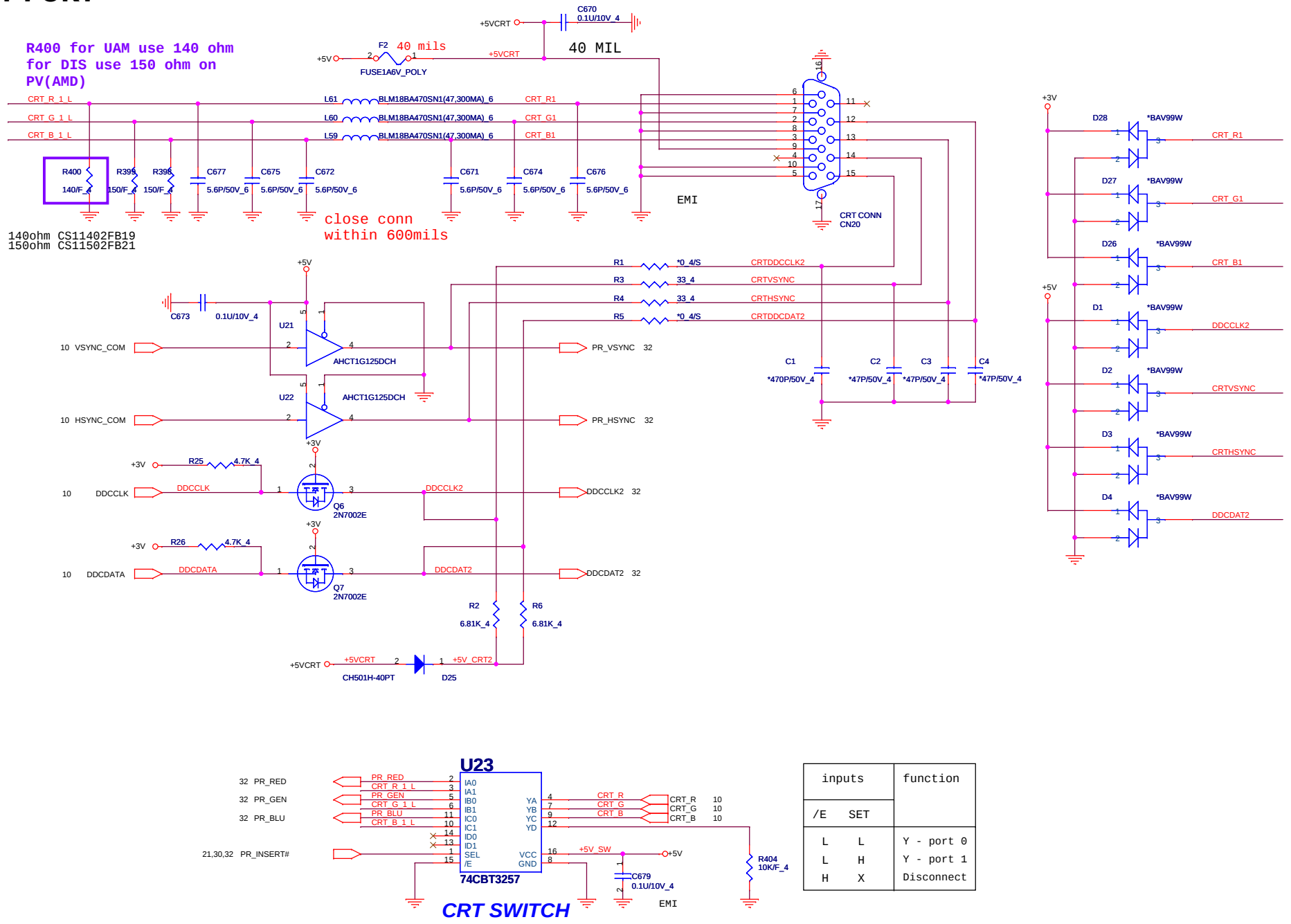
AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5



PROJECT : UT12
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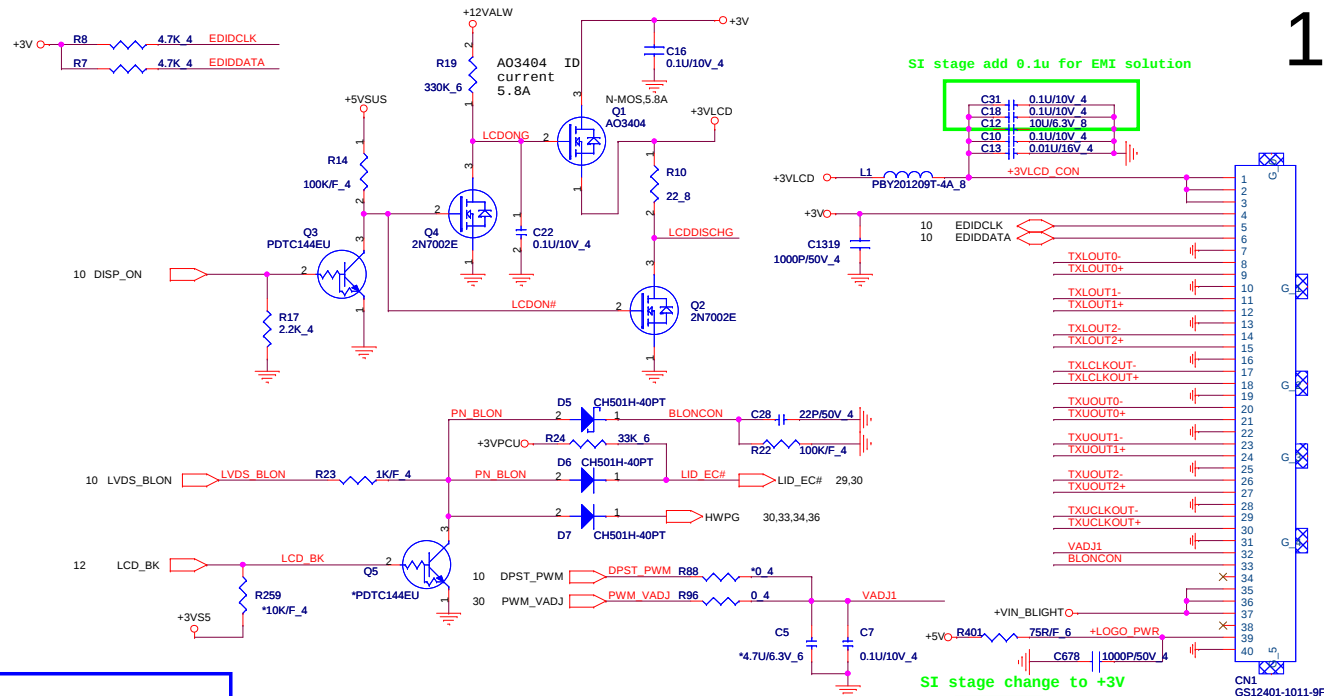
CRT PORT



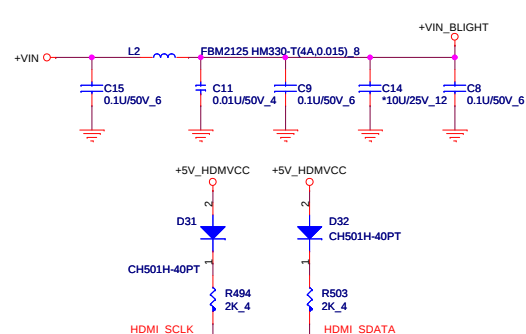
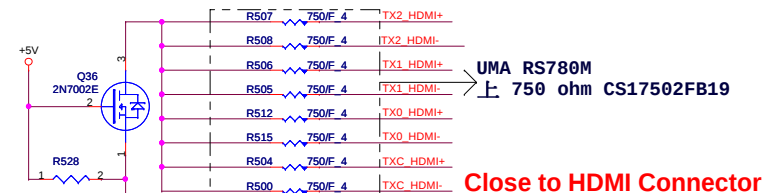
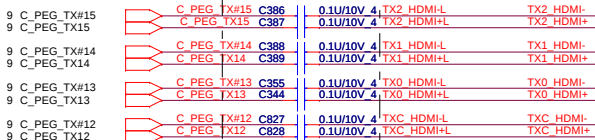
PROJECT : UT12
Quanta Computer Inc.

Size Custom	Document Number CRT	Rev 1A
Date: Monday, November 10, 2008	Sheet 17 of 40	

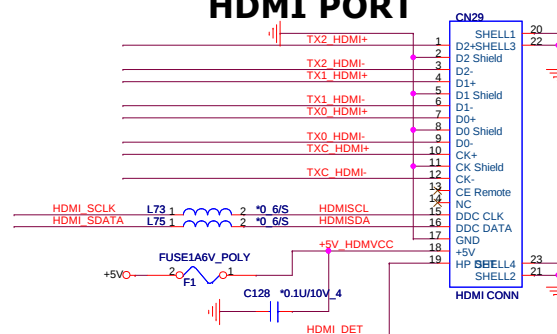
10	LA_CLK	LA_CLK	TXCLKOUT+
10	LA_CLK#	LA_CLK#	TXCLKOUT-
10	LA_DATA0	LA_DATA0	TXU0T0+
10	LA_DATA0	LA_DATA0	TXU0T0-
10	LA_DATA1	LA_DATA1	TXU0T1+
10	LA_DATA1	LA_DATA1	TXU0T1-
10	LA_DATA2	LA_DATA2	TXU0T2+
10	LA_DATA2	LA_DATA2	TXU0T2-
10	LB_CLK	LB_CLK	TXCLKOUT+
10	LB_CLK#	LB_CLK#	TXCLKOUT-
10	LB_DATA0	LB_DATA0	TXU0T0+
10	LB_DATA0	LB_DATA0	TXU0T0-
10	LB_DATA1	LB_DATA1	TXU0T1+
10	LB_DATA1	LB_DATA1	TXU0T1-
10	LB_DATA2	LB_DATA2	TXU0T2+
10	LB_DATA2	LB_DATA2	TXU0T2-



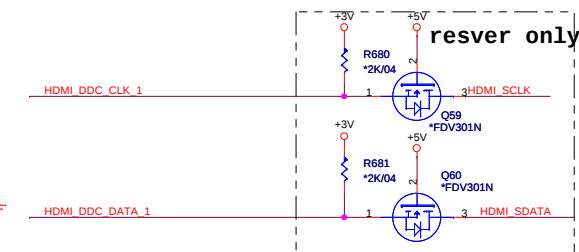
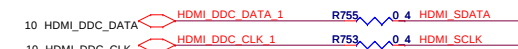
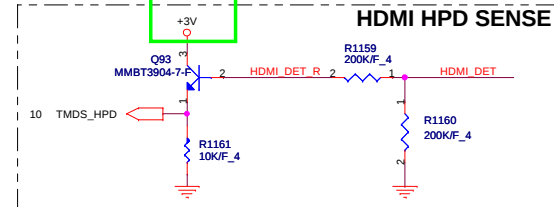
for Layout -
concern
, placement close
north bridge

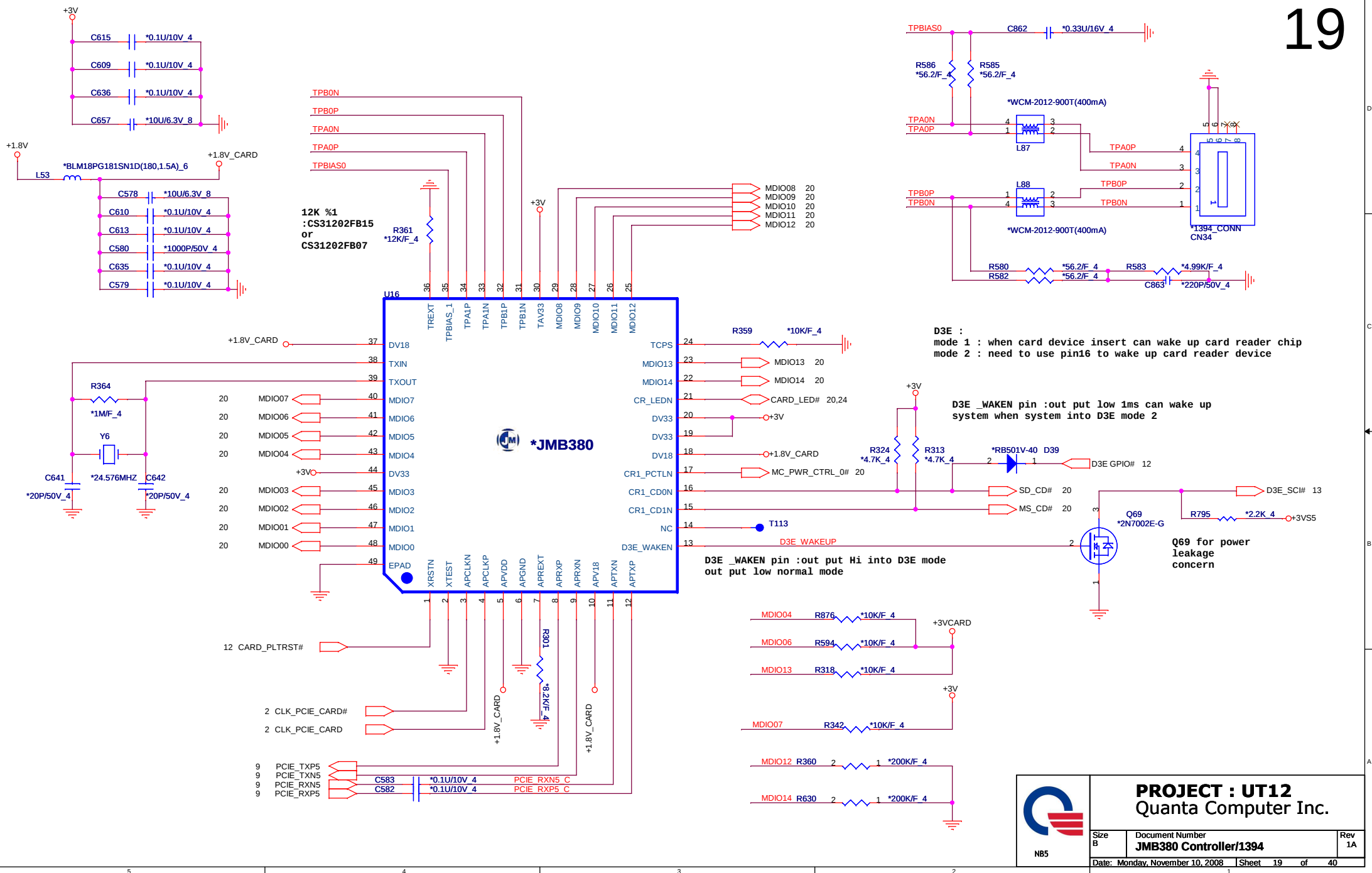


HDMI PORT



HDMI HPD SENSE

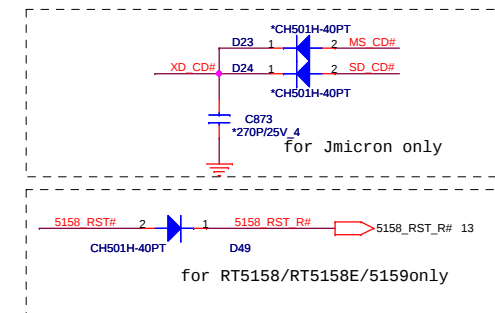
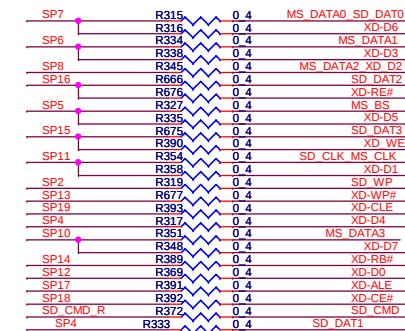
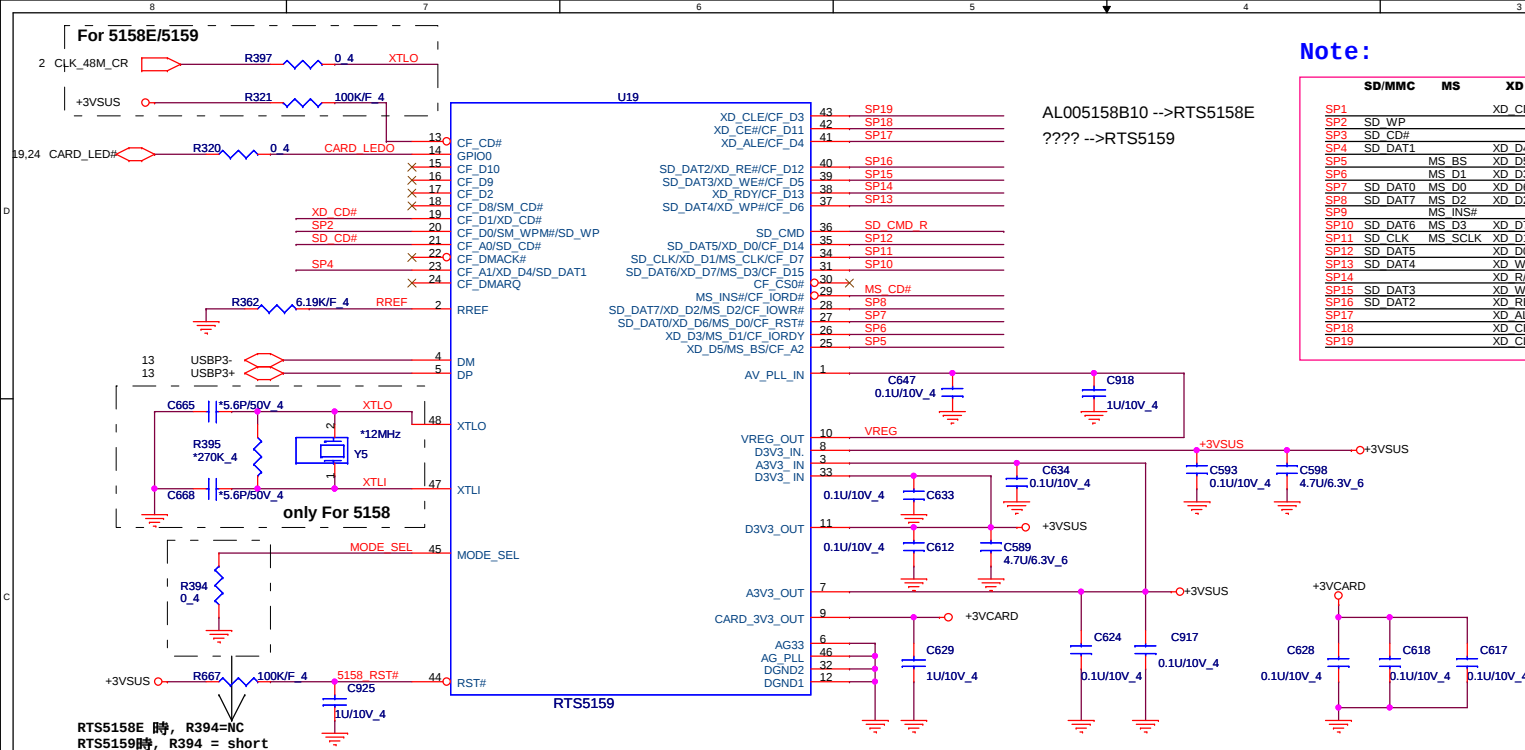




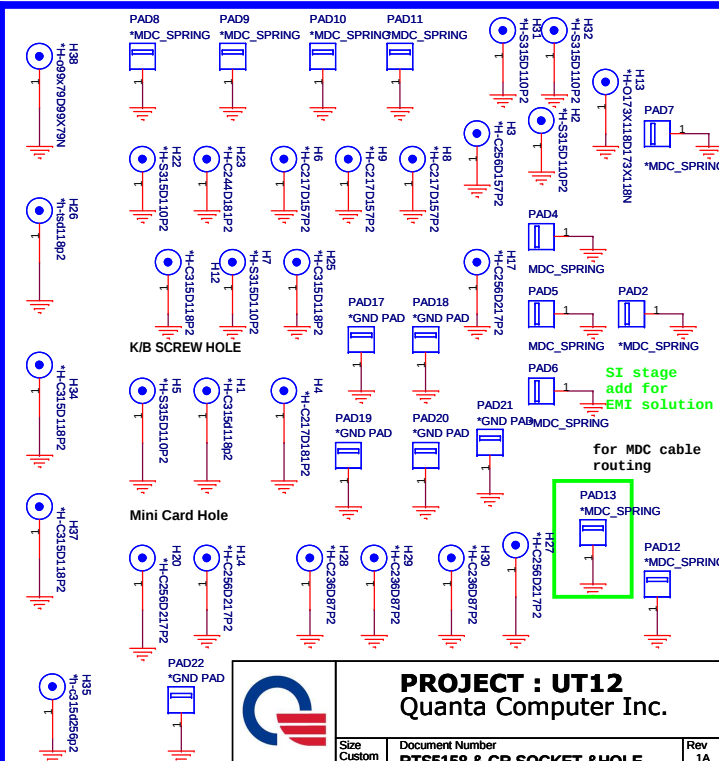
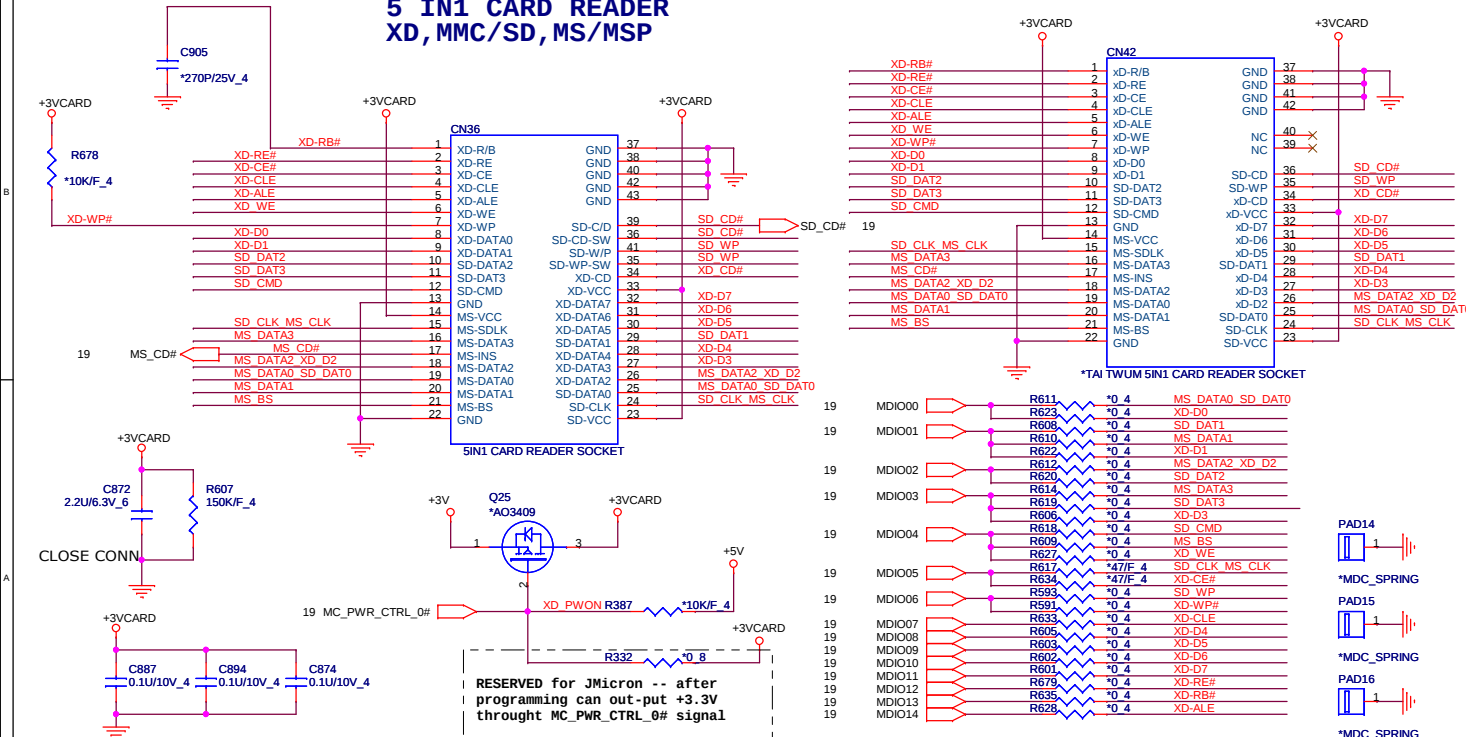
PROJECT : UT12
Quanta Computer Inc.

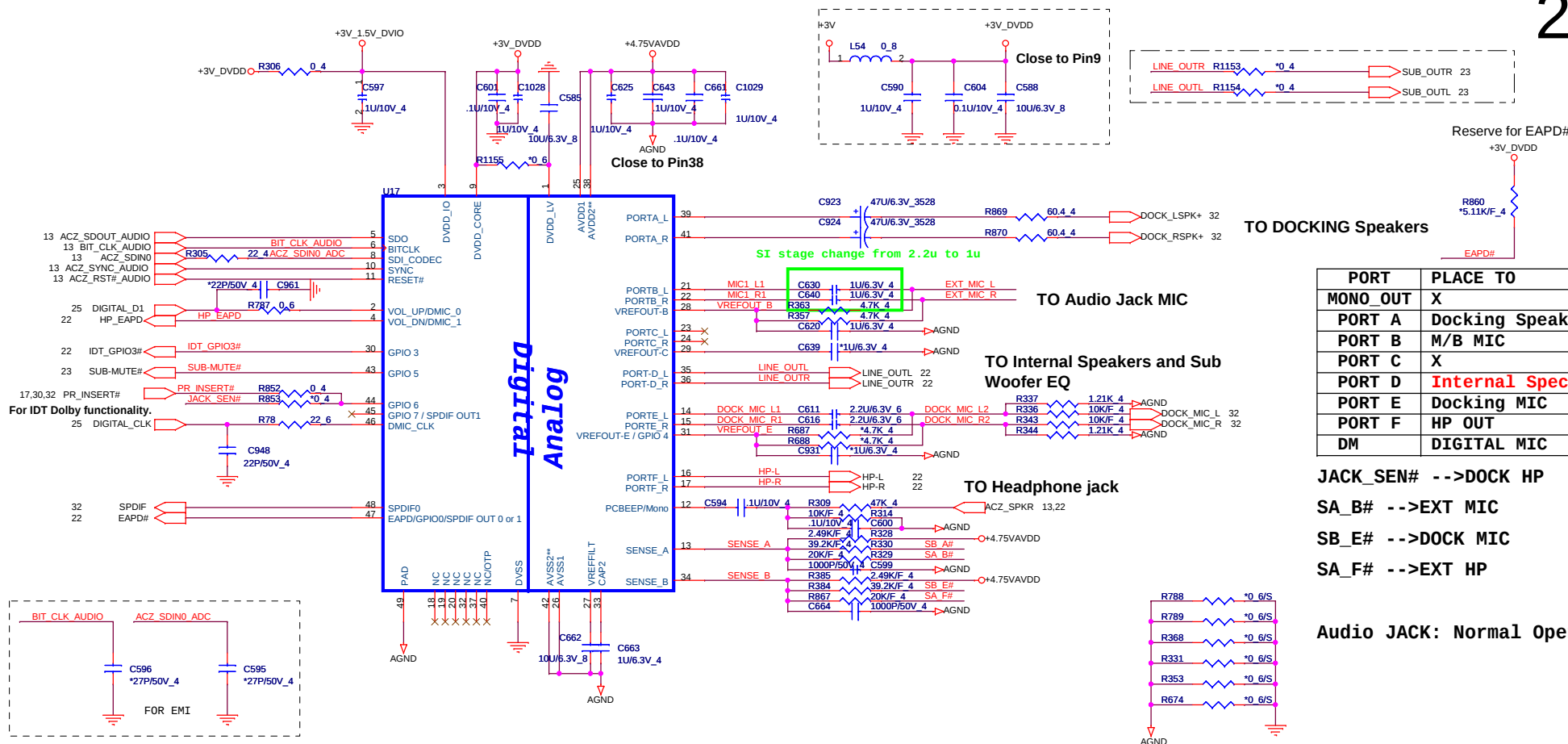
Size B	Document Number	Rev 1A
	JMB380 Controller/1394	
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Note:



5 IN1 CARD READER
XD, MMC/SD, MS/MSP





TO DOCKING Speakers

TO Audio Jack MIC

TO Internal Speakers and Sub Woofer EQ

TO Headphone jack

PORT	PLACE TO
MONO_OUT	X
PORT A	Docking Speakers
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	Docking MIC
PORT F	HP OUT
DM	DIGITAL MIC

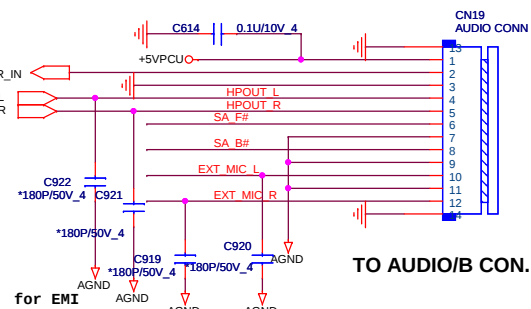
JACK_SEN# -->DOCK HP

SA_B# -->EXT MIC

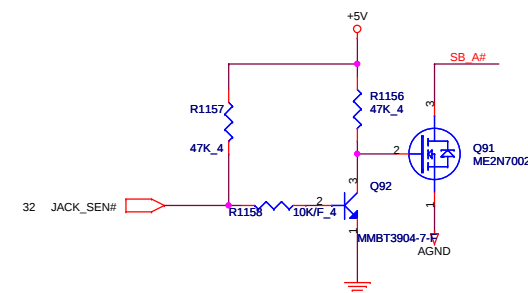
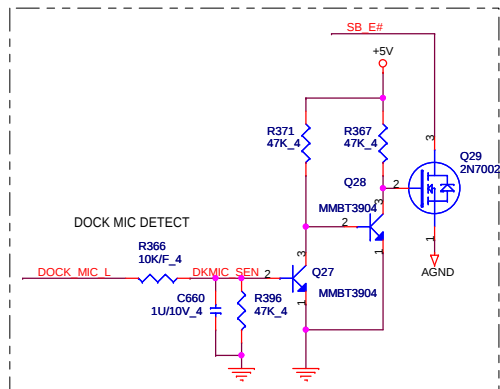
SB_E# -->DOCK MIC

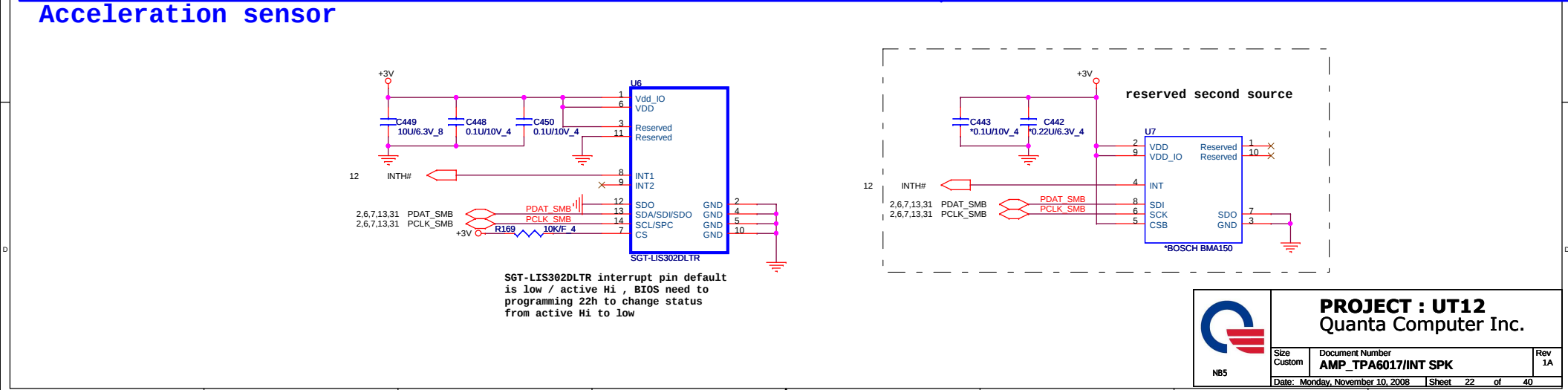
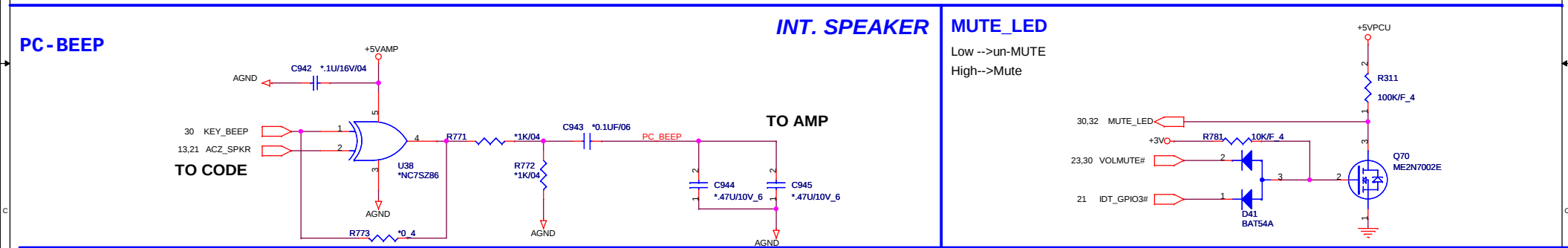
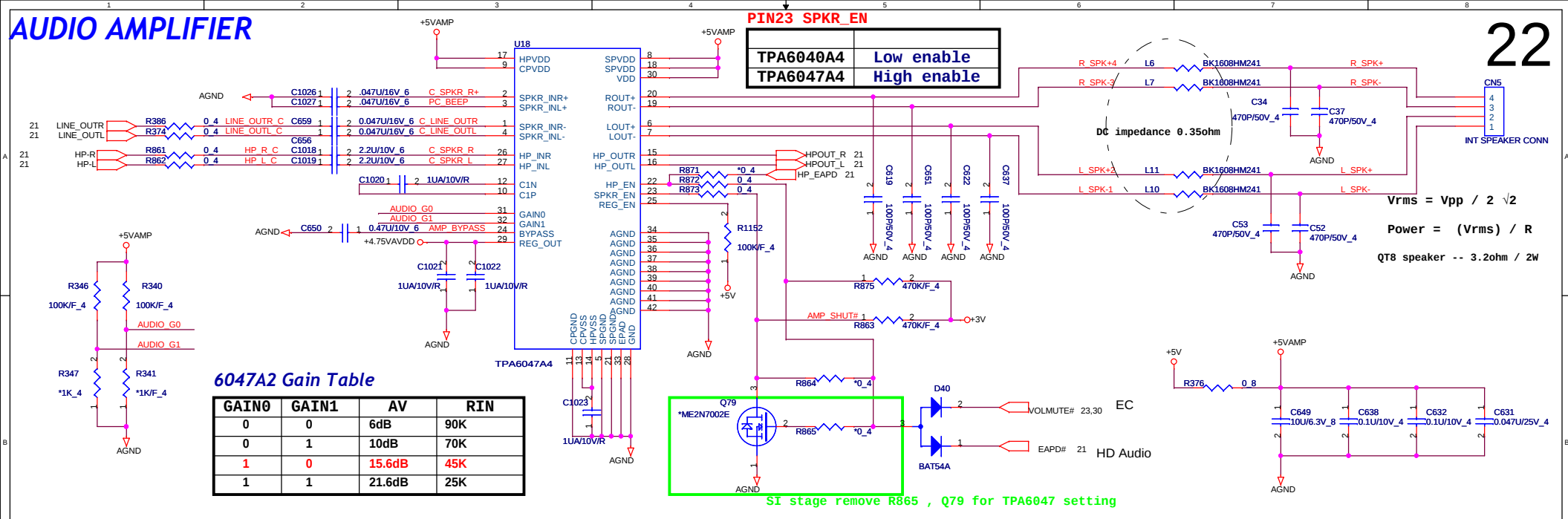
SA_F# -->EXT HP

Audio JACK: Normal Open



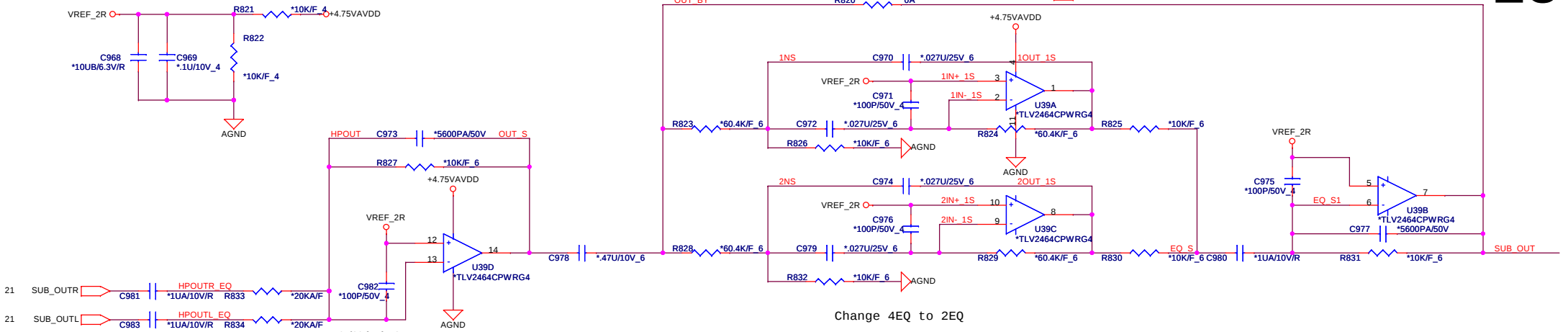
TO AUDIO/B CON.



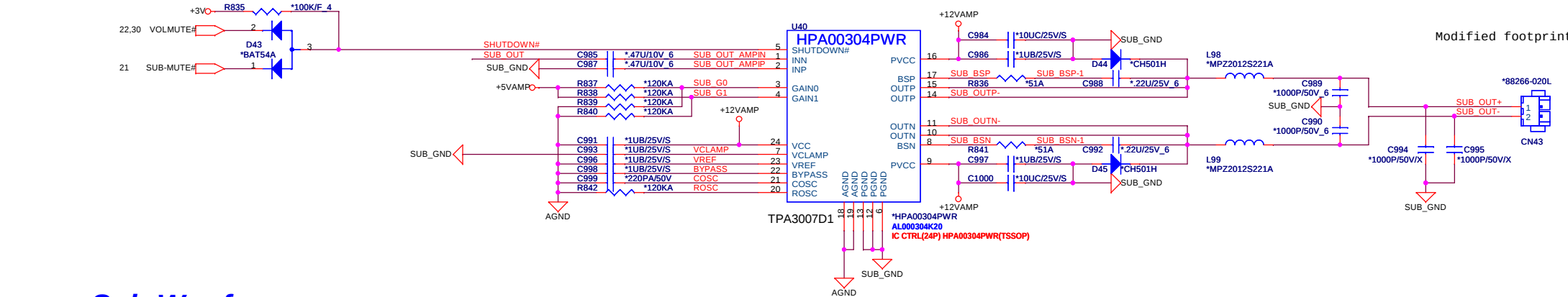


EQ FOR SUBWOOFER

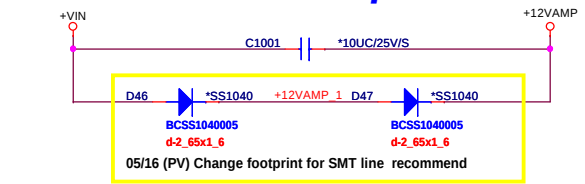
23



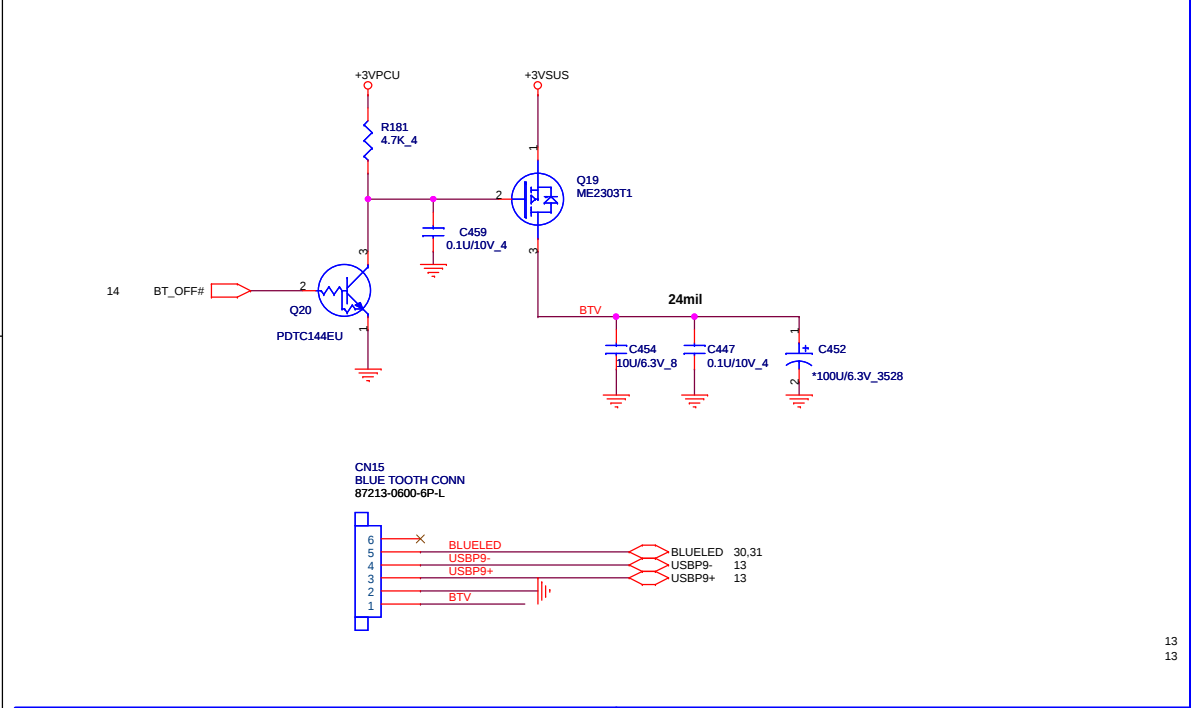
MODEL	UT1	UT2
R823	60.4K/F_6	40.2K/F_6
R824	60.4K/F_6	40.2K/F_6
R828	60.4K/F_6	80.6K/F_6
R829	60.4K/F_6	80.6K/F_6
C970	0.027U/25V_6	0.022U/50V_6
C972	0.027U/25V_6	0.022U/50V_6
C974	0.027U/25V_6	0.039U/16V_6
C976	0.027U/25V_6	0.039U/16V_6



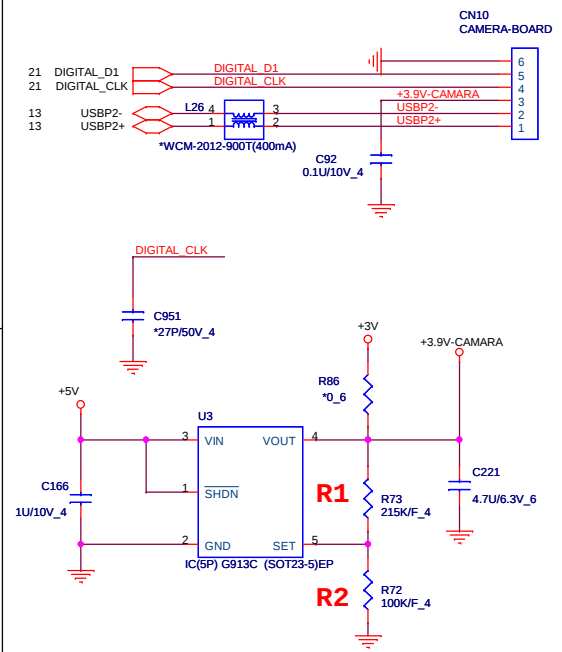
Sub-Woofer power



BLUETOOTH

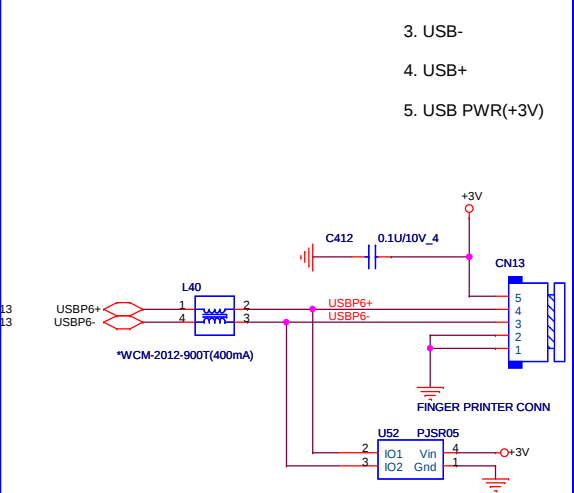


USB CAMERA CONNECT

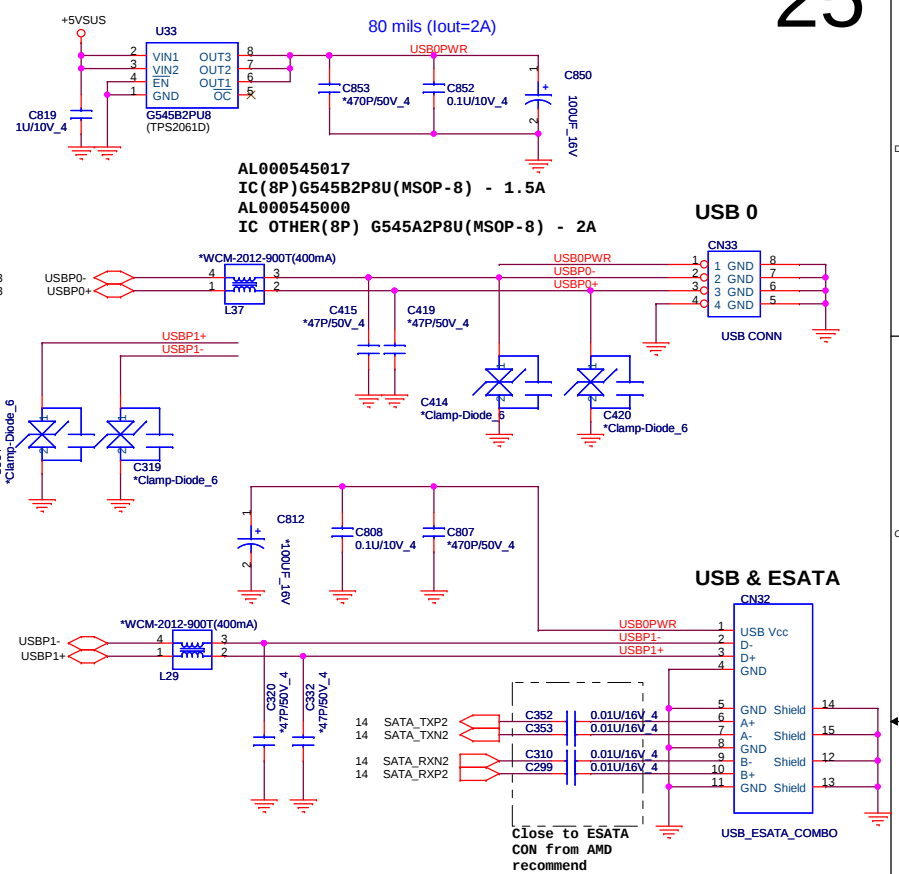


$$V_{out} = 1.25(1 + R1/R2)$$

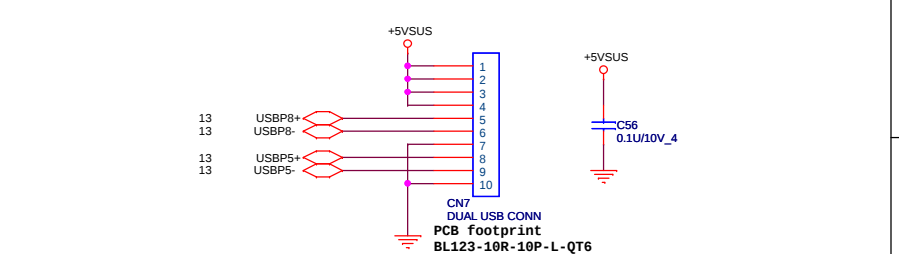
USB Fingerprint CON



LEFT SIDE USBX1 and E-SATA/USB COMBO



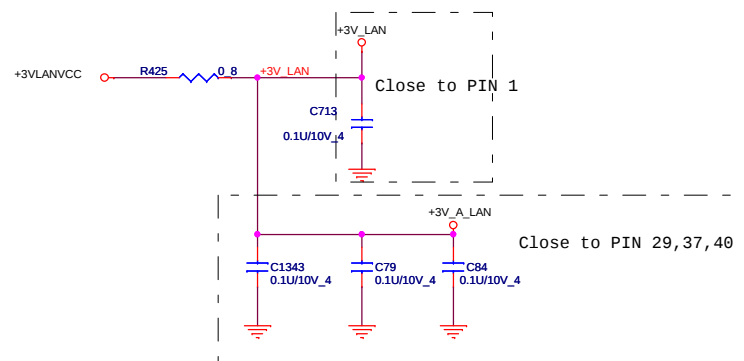
RIGHT SIDE USBX2



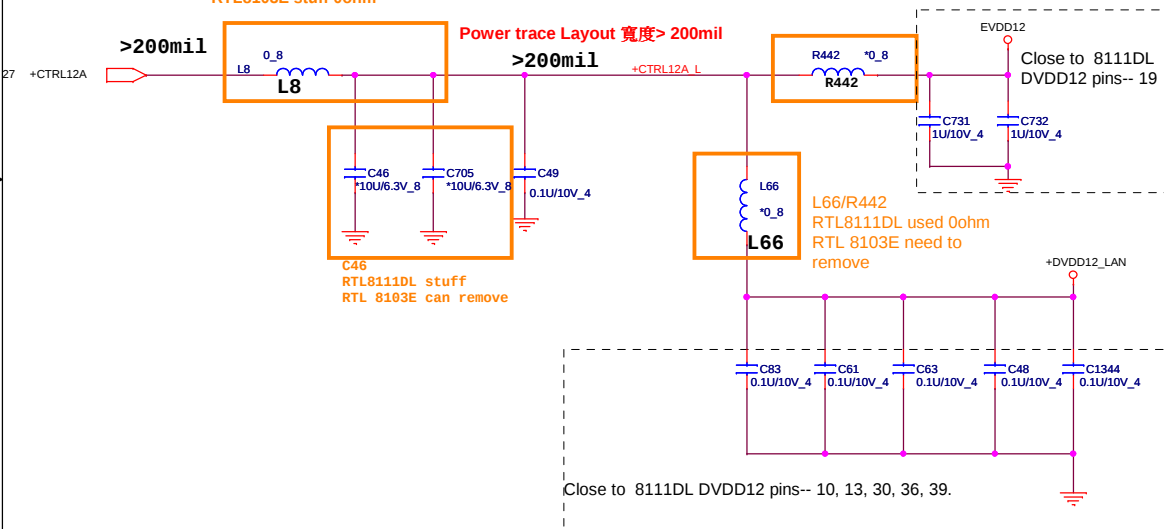


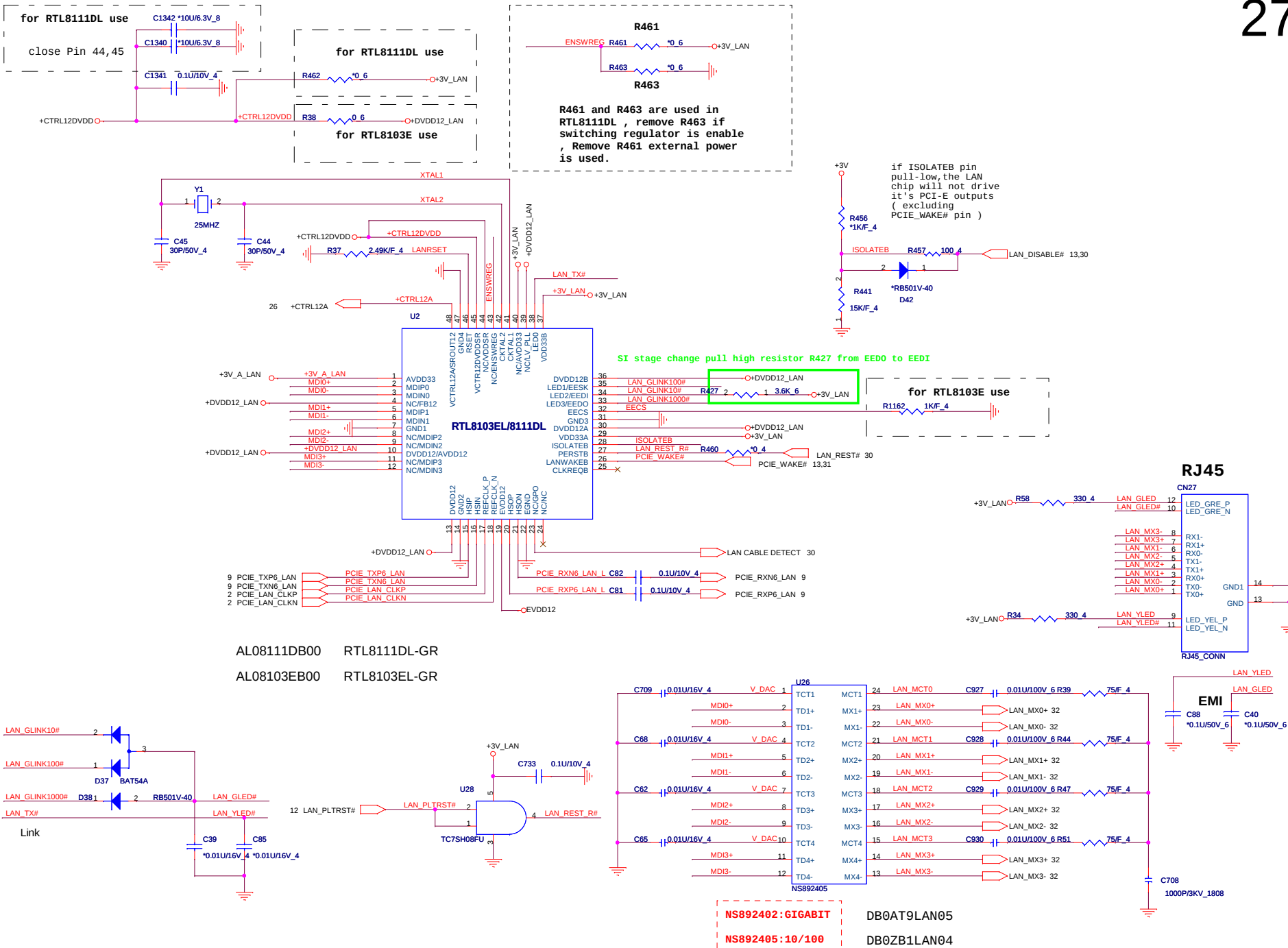
PROJECT : UT12
Quanta Computer Inc.

Size Custom	Document Number BT/WEBCAM/FT/USBX4/ESATA	Rev 1A
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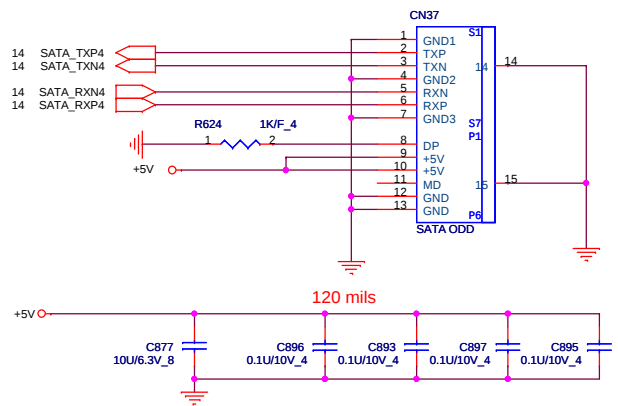
L8
RTL8111DL (Giga lan) use 4.7uH
power choke A>600mA tolerance
±15%
RTL8103E stuff 0ohm



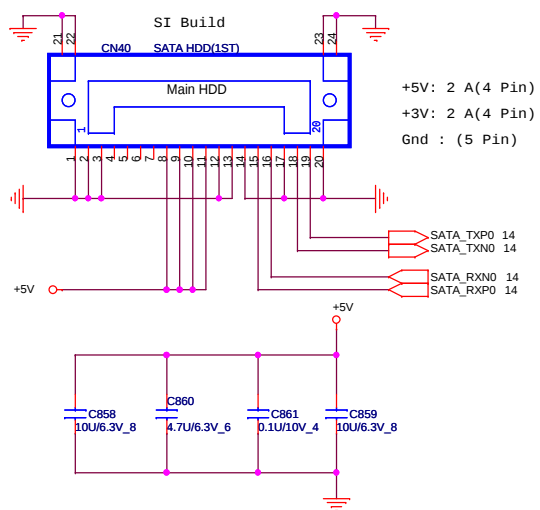


SATA CD-ROM

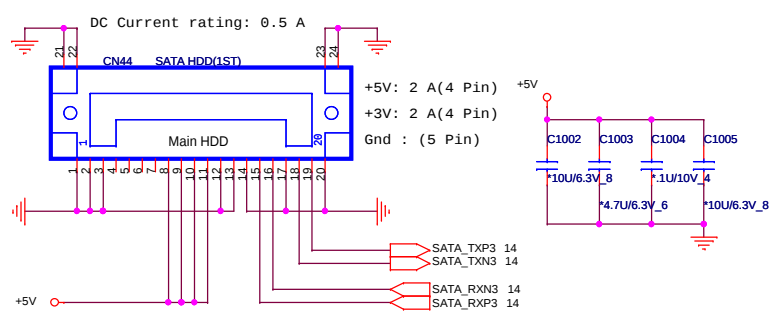
17.3 ODD P/N : DFHS13FR030 or DFHS13FR040
16.3 ODD P/N : DFHD13MR006 , DFHD13MR009 , DFHD13MR008



SATA_1 HDD CONNECTOR



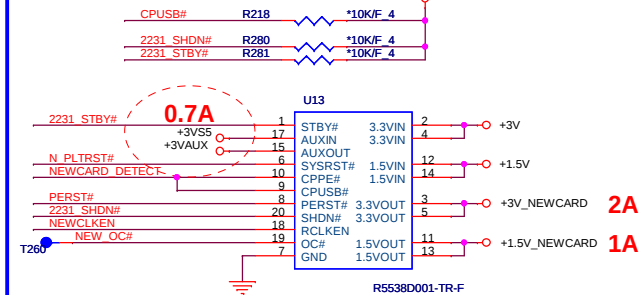
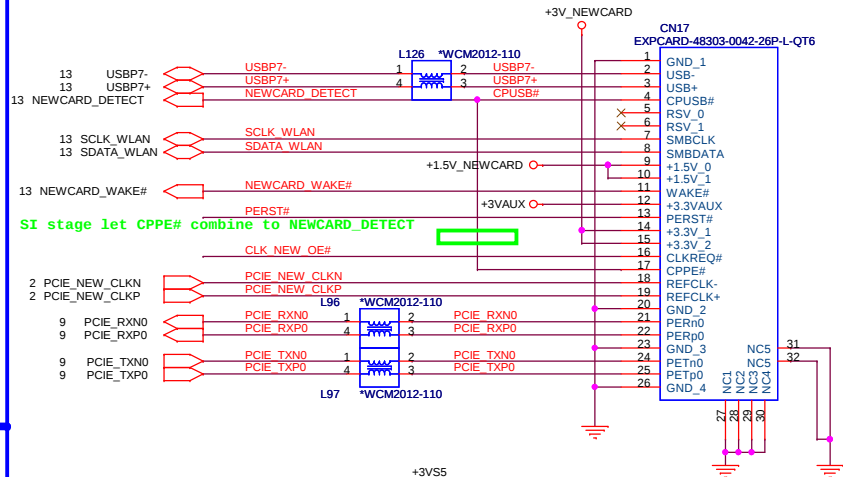
SATA_2 CONNECTOR



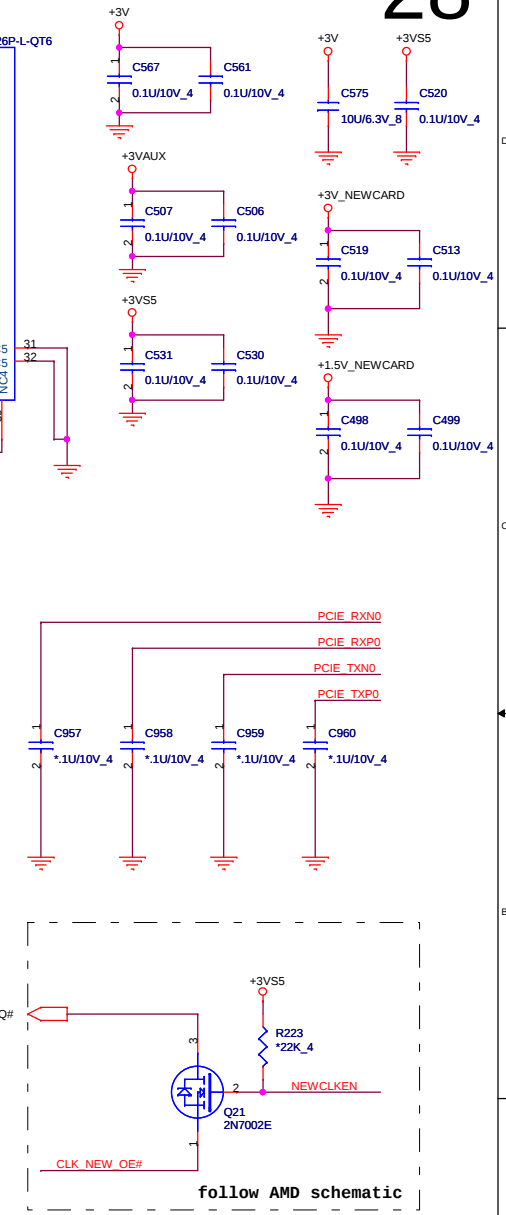
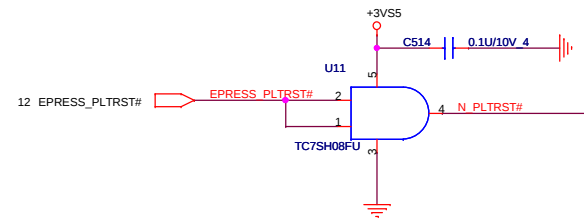
NEWCARD

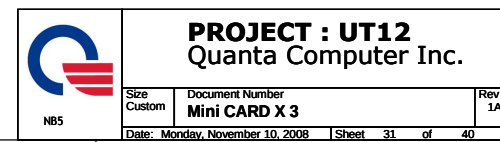
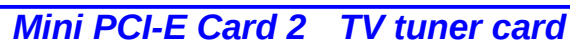
NEWCARD (PCIEXPRESS*1 + USB*1)

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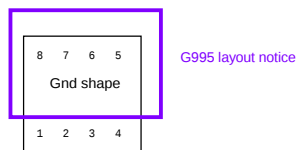
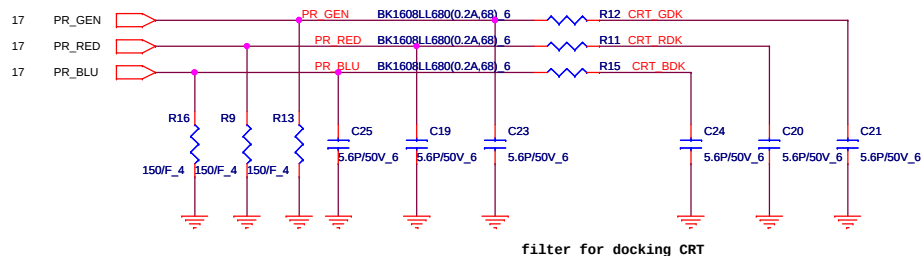


R5538 NEW CARD POWER SWITCH	
pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN





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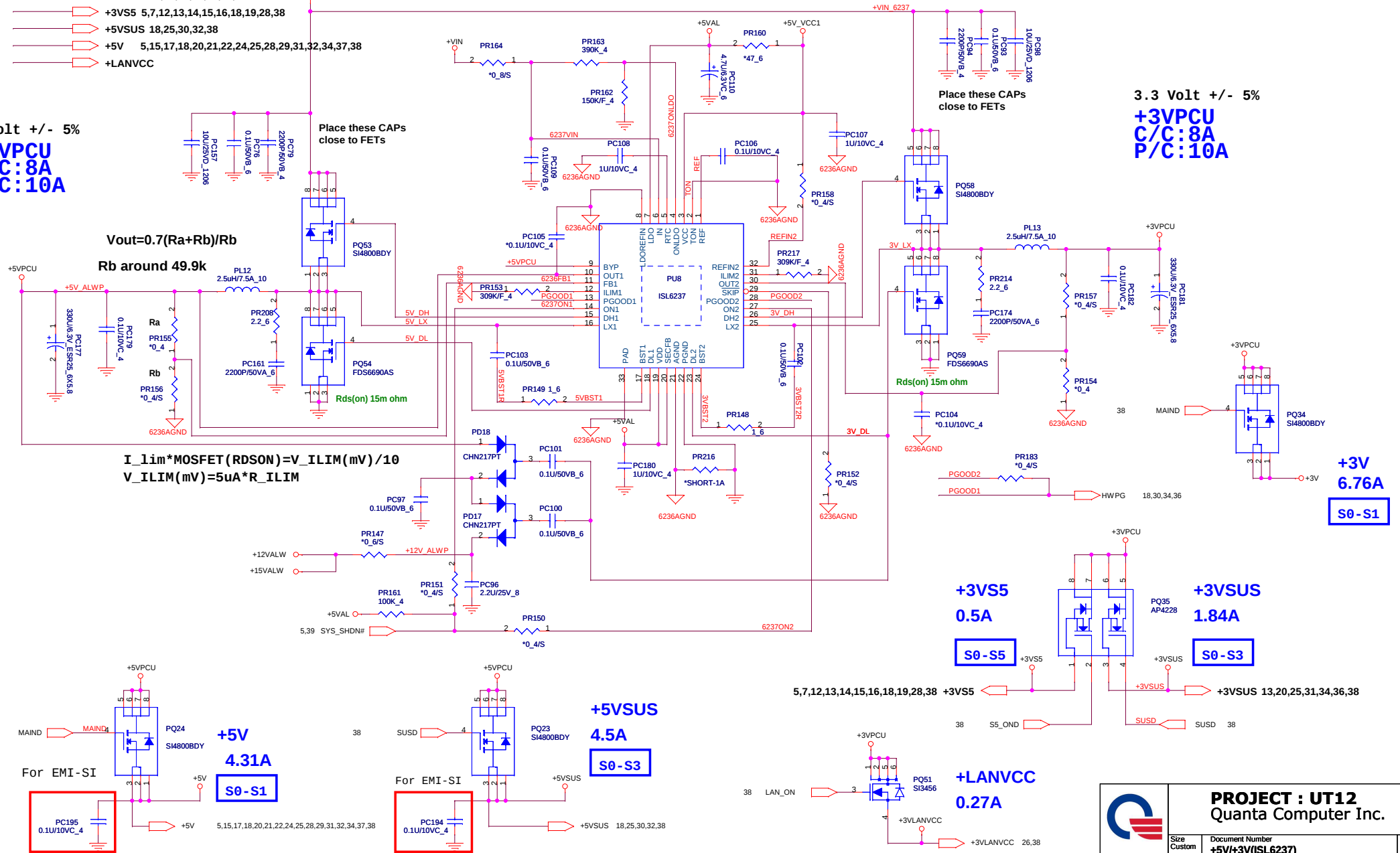


DC/DC +3VPCU/+ 5VPCU/ +12VALW

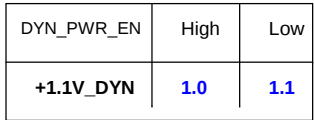
- +5VPCU 21,22,29,30,34,35,36,37
- +3VPCU 5,12,18,24,25,29,30,32,35,36,37,39
- +3VSUS 13,20,25,31,34,36,38
- +3VS5 5,7,12,13,14,15,16,18,19,28,38
- +5VSUS 18,25,30,32,38
- +5V 5,15,17,18,20,21,22,24,25,28,29,31,32,34,37,38
- +LANVCC

5 Volt +/- 5%

+5VPCU
C/C:8A
P/C:10A



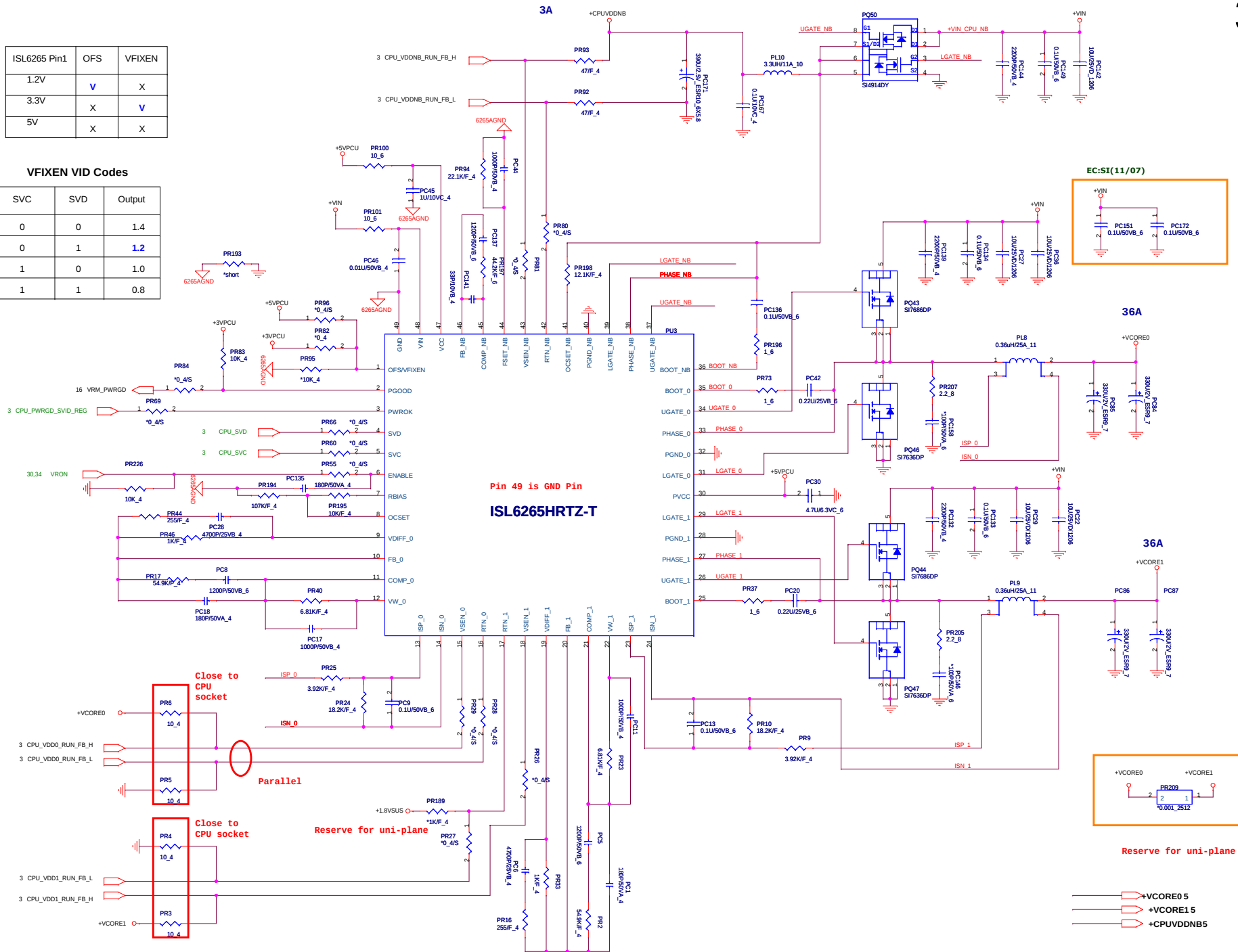
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ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

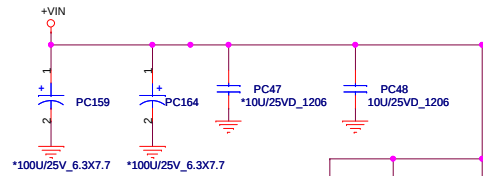
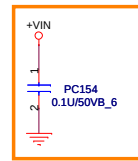
VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

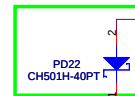


 +2.5V 3
 +1.8VSUS 3,4,5,6,7,35,37

EC:SI(11/07)

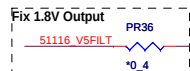
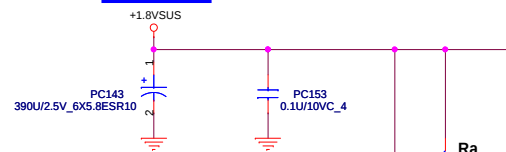


EC:SI(11/07)

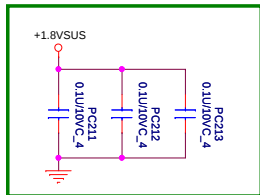


$I_{lim(Valley)} = 10\mu A \cdot R_{ILIM} / R_{DS_ON}$
 For OCP set.

23.65A
S0~S3



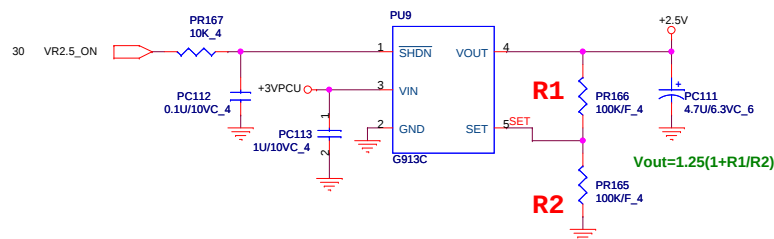
Add 0.1u CAP PC211, PC212, PC213 for EMI



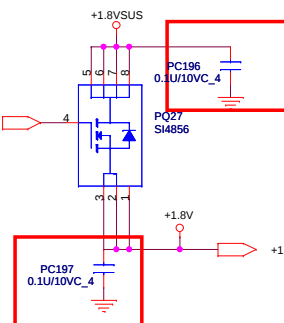
$R_a = (V_{out} - 0.75) / (0.75 \cdot R_b)$
 Rb value from 100K to 300K ohm

+2.5V
0.25A
S0~S1

S0~S1

Close to CPU
SI power
 $V_{out} = 1.25(1 + R1/R2)$

For EMI-SI



Discrete:SI4856
UMA:SI4800

For EMI-SI

+1.8V
10.4A
S0~S1

S0~S1

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

$$V_{TRIP}(mV) = R_{TRIP}(Kohm) \cdot 10(\mu A)$$

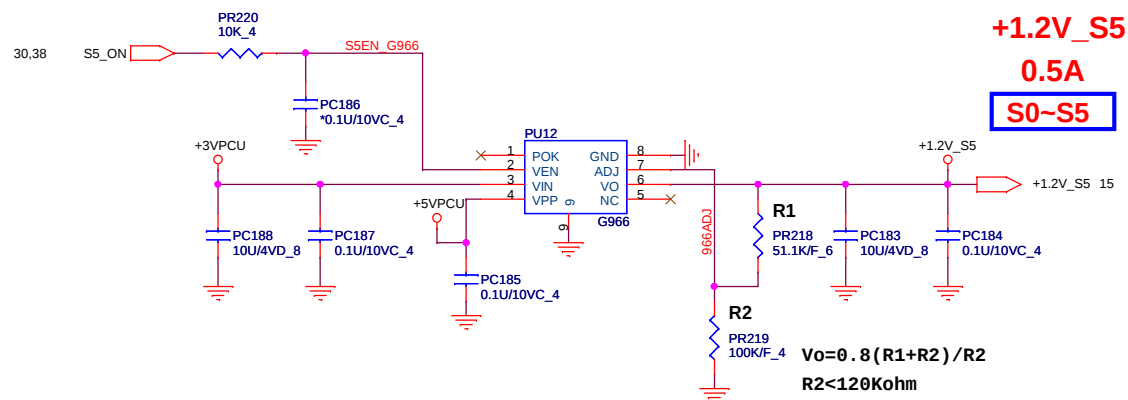
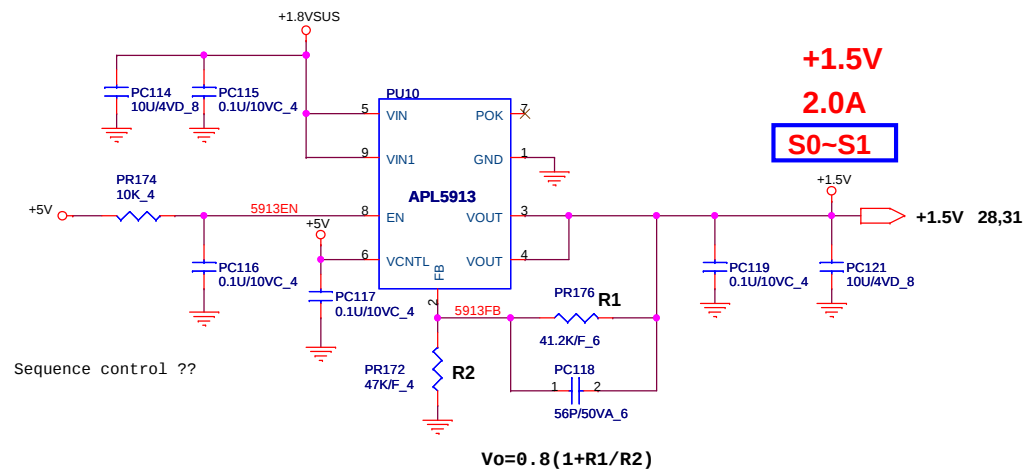
$$I_{OCP} = V_{trip} / R_{ds_on} + I_{Ripple} / 2$$

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	$V_{_vddqsns} / 2$	DDR
V5IN	1.8	$V_{_vddqsns} / 2$	DDR2
FB	adjustable	$V_{_VDDQSNS} / 2$	$1.5V < VDDQ < 3V$



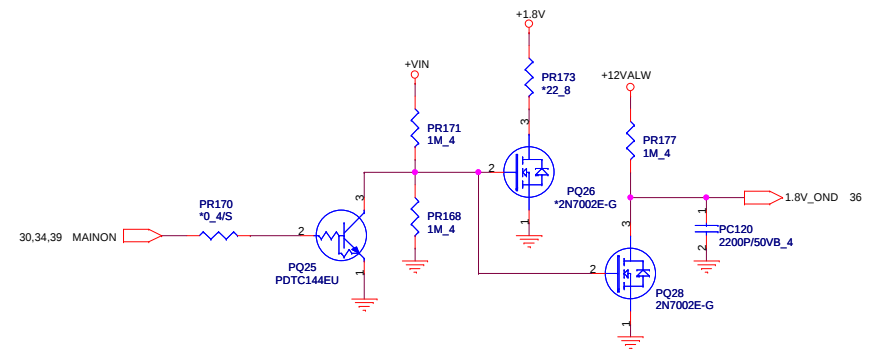
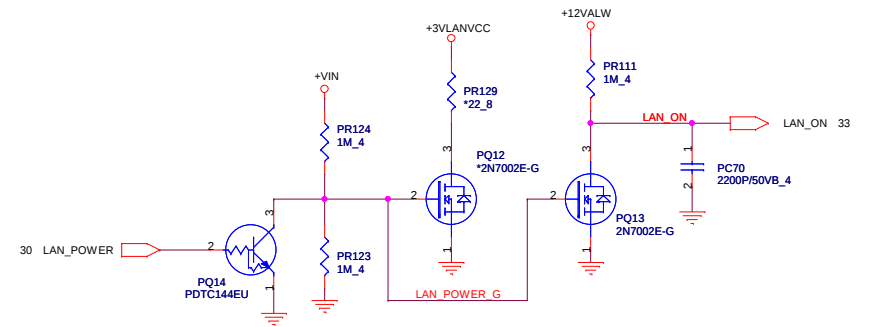
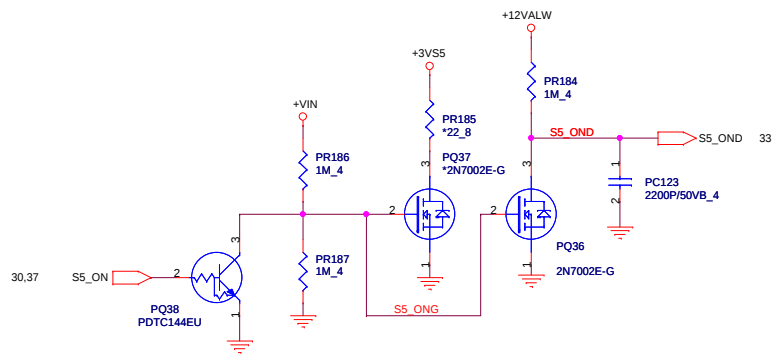
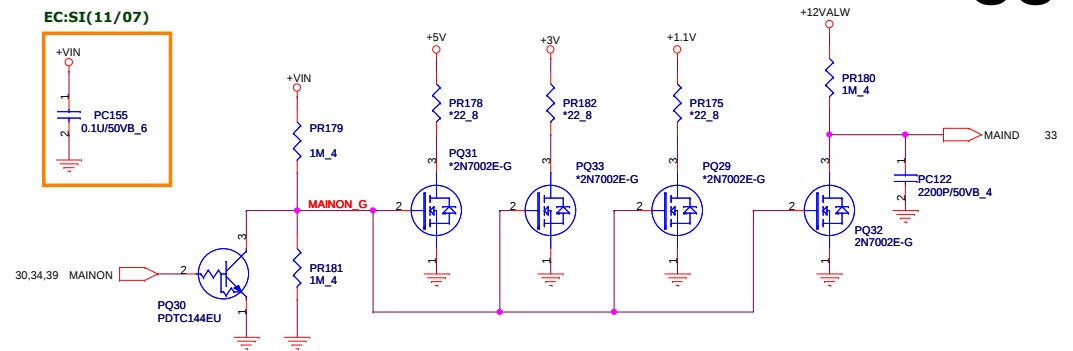
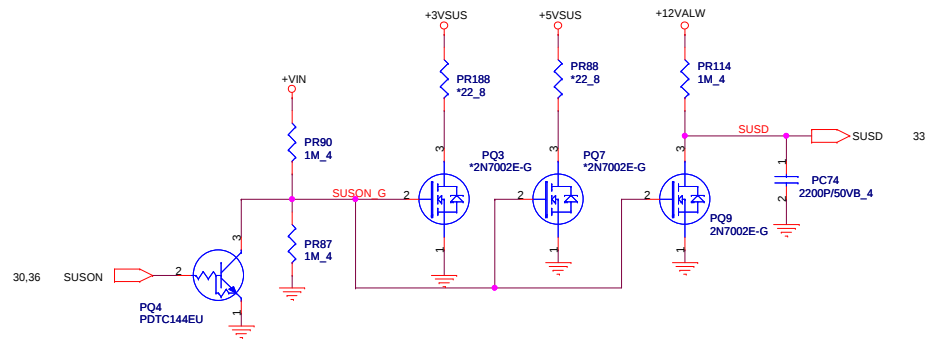
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Quanta Computer Inc.

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Quanta Computer Inc.

Size B	Document Number VGA PWR OZ8118/1.2V_S5/+1.5	Rev 1A
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Quanta Computer Inc.

Size Custom	Document Number DISCHARGE	Rev 1A
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