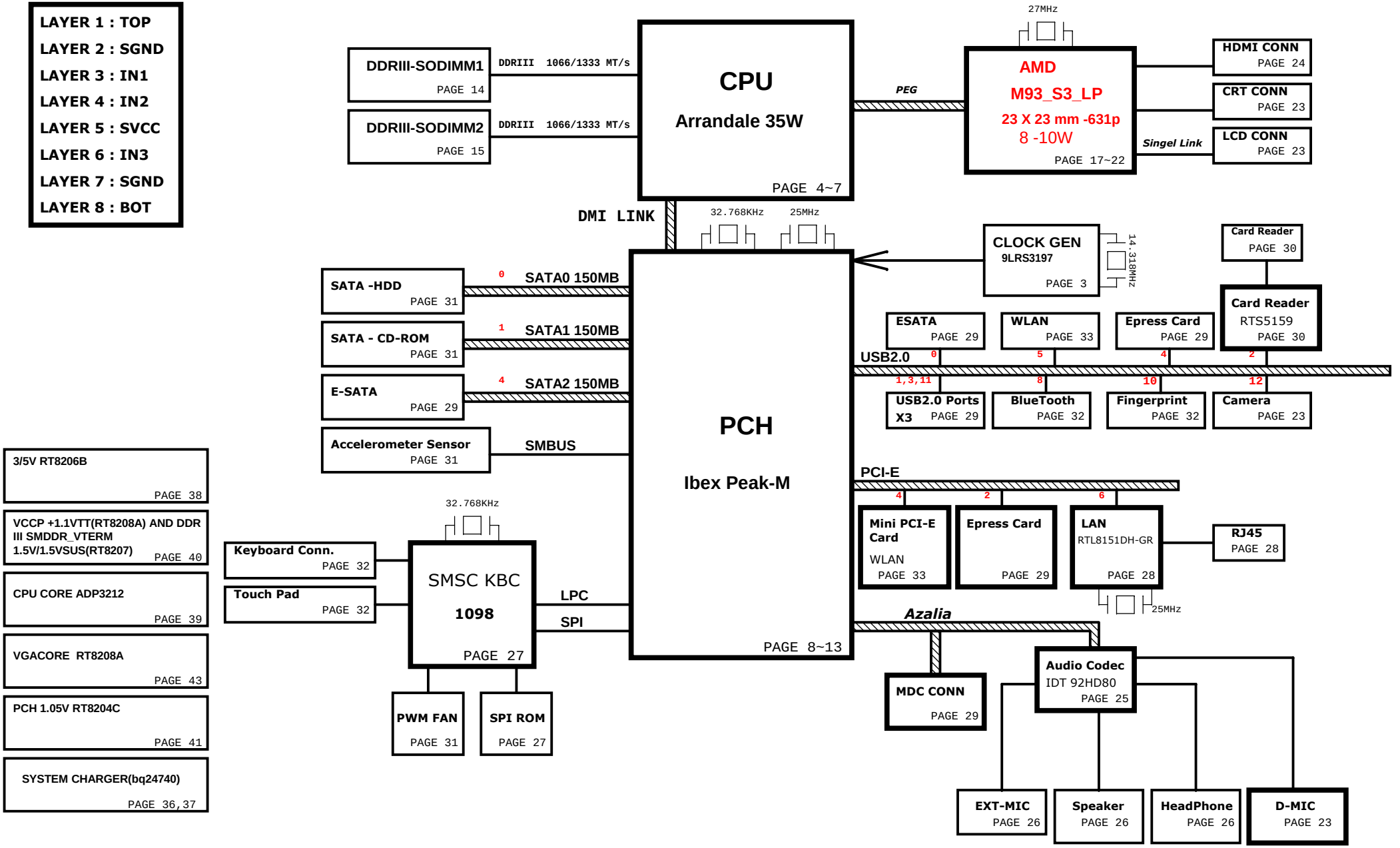
Hamilton 1.0 (SX6-DIS) BLOCK DIAGRAM

01

PCB STACK UP
8L Dis.

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : SGND
LAYER 8 : BOT



PROJECT : SX6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	2B

NB5

Date: Tuesday, December 15, 2009 | Sheet 1 of 43

power / State	+RTC_CELL	+VIN +3VPCU	+3VS5 +5VS5	+5VSUS +1.5VSUS	+5V +3V +1.8V_GFX +1.8V +1.5V +1.5V_CPU +1.1V_VTT +1.05V +1.0V_GFX +VGA_CORE +VCORE
S0	ON	ON	ON	ON	ON
S1	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4/S5 AC	ON	ON	ON	OFF	OFF
S4/S5 DC Only	ON	ON	OFF	OFF	OFF
AC/DC No Exist	ON	OFF	OFF	OFF	OFF

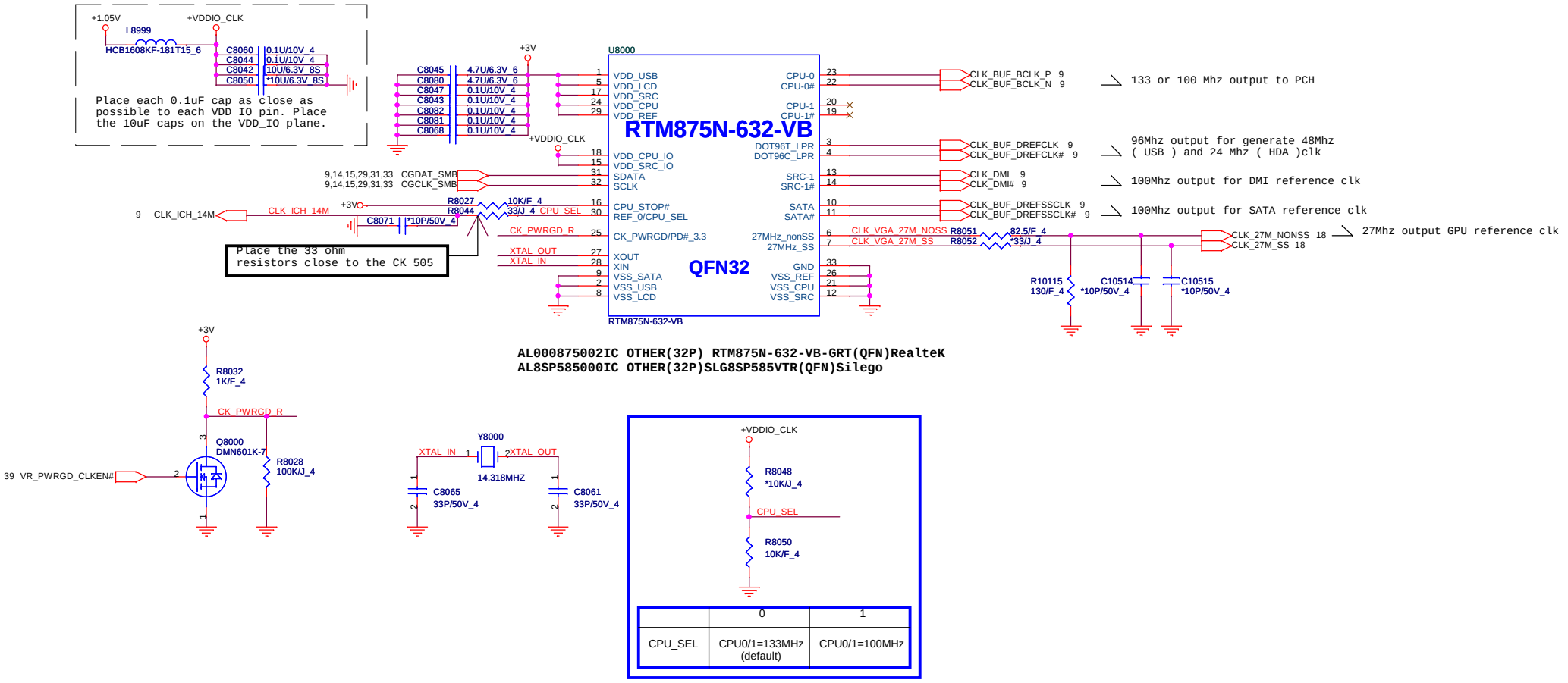
	SOURCE	BATTERY 0x16	CLK GEN 0xD2	Thermal IC 0x98(Write) / 0x99(Read)	G-SENSOR 0x3A(Write) /0x3B(Read)	WLAN	SO-DIMM DIMM0: 0xA0 DIMM1: 0xA2	SMSC 1098	GPU thermal sensor
SMBCLK SMBDATA	PCH	X	Y	Y	Y	Y	Y	X	X
SMB_CLK_ME1 SMB_DAT_ME1	PCH	X	X	X	X	X	X	Y	Y
AB1A_CLK AB1A_DATA	SMSC 1098	Y	X	X	X	X	X	X	X

NB5

PROJECT : SX6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	power rails	2B

Date: Tuesday, December 15, 2009 | Sheet 2 of 43



AL000875002IC OTHER(32P) RTM875N-632-VB-GRT(QFN)RealteK
AL8SP585000IC OTHER(32P)SLG8SP585VTR(QFN)Silego

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

4,8,9,10,11,12,14,15,16,20,23,25,27,28,29,30,31,32,33,34,35,37,39,42 +3V

PROJECT : SX6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GEN (9LRS3197)	2B
Date: Tuesday, December 15, 2009	Sheet 3 of 43	

NB5

U8009A

DMI_TXN0 10 — A24 DMI_RX#[0]
DMI_TXN1 10 — C23 DMI_RX#[1]
DMI_TXN2 10 — B22 DMI_RX#[2]
DMI_TXN3 10 — A21 DMI_RX#[3]

DMI_TXP0 10 — B24 DMI_RX[0]
DMI_TXP1 10 — D23 DMI_RX[1]
DMI_TXP2 10 — B23 DMI_RX[2]
DMI_TXP3 10 — A22 DMI_RX[3]

DMI_RXN0 10 — D24 DMI_TX#[0]
DMI_RXN1 10 — G24 DMI_TX#[1]
DMI_RXN2 10 — F23 DMI_TX#[2]
DMI_RXN3 10 — H23 DMI_TX#[3]

DMI_RXP0 10 — D25 DMI_TX[0]
DMI_RXP1 10 — F24 DMI_TX[1]
DMI_RXP2 10 — E23 DMI_TX[2]
DMI_RXP3 10 — G23 DMI_TX[3]

DMI

E22 FDI_TX#[0]
D21 FDI_TX#[1]
D19 FDI_TX#[2]
D18 FDI_TX#[3]
G21 FDI_TX#[4]
E19 FDI_TX#[5]
F21 FDI_TX#[6]
G18 FDI_TX#[7]

D22 FDI_TX[0]
C21 FDI_TX[1]
D20 FDI_TX[2]
C18 FDI_TX[3]
G22 FDI_TX[4]
E20 FDI_TX[5]
F20 FDI_TX[6]
G19 FDI_TX[7]

C_FDI_SYNC F17 FDI_FSYNC[0]
C_FDI_SYNC E17 FDI_FSYNC[1]
R8015 1K/F_4 C_FDI_INT C17 FDI_INT
C_FDI_SYNC F18
R8012 1K/F_4 C_FDI_SYNC D17 FDI_LSYNC[0]
FDI_LSYNC[1]

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI
PEG_ICOMPO
PEG_RCOMPO
PEG_RBIAS
B26 PEG_COMP R8186 49.9/F_4
A26
B27
A25 PEG_RBIAS R8187 750/F_4

PEG_RX#[0..15] 17

K35 PEG_RX#0 — PEG_RX#[0]
J34 PEG_RX#1 — PEG_RX#[1]
J33 PEG_RX#2 — PEG_RX#[2]
G35 PEG_RX#3 — PEG_RX#[3]
G32 PEG_RX#4 — PEG_RX#[4]
F34 PEG_RX#5 — PEG_RX#[5]
F31 PEG_RX#6 — PEG_RX#[6]
D35 PEG_RX#7 — PEG_RX#[7]
E33 PEG_RX#8 — PEG_RX#[8]
C33 PEG_RX#9 — PEG_RX#[9]
D32 PEG_RX#10 — PEG_RX#[10]
B32 PEG_RX#11 — PEG_RX#[11]
C31 PEG_RX#12 — PEG_RX#[12]
B28 PEG_RX#13 — PEG_RX#[13]
B30 PEG_RX#14 — PEG_RX#[14]
A31 PEG_RX#15 — PEG_RX#[15]

J35 PEG_RX0 — PEG_RX[0]
H34 PEG_RX1 — PEG_RX[1]
H33 PEG_RX2 — PEG_RX[2]
E35 PEG_RX3 — PEG_RX[3]
G33 PEG_RX4 — PEG_RX[4]
E34 PEG_RX5 — PEG_RX[5]
F32 PEG_RX6 — PEG_RX[6]
D34 PEG_RX7 — PEG_RX[7]
F33 PEG_RX8 — PEG_RX[8]
B33 PEG_RX9 — PEG_RX[9]
D31 PEG_RX10 — PEG_RX[10]
A32 PEG_RX11 — PEG_RX[11]
C30 PEG_RX12 — PEG_RX[12]
A28 PEG_RX13 — PEG_RX[13]
B29 PEG_RX14 — PEG_RX[14]
A30 PEG_RX15 — PEG_RX[15]

10 PM_DRAM_PWRGD — PM_DRAM_PWRGD R10153 0/J_4 DRAM_PWRGD_CPU AK13
PEG_RX[0..15] 17

L33 C_PEG_TX#0 C8225 0.1U/10V_4 PEG_TX#0 — PEG_TX#[0]
M35 C_PEG_TX#1 C8222 0.1U/10V_4 PEG_TX#1 — PEG_TX#[1]
M33 C_PEG_TX#2 C8218 0.1U/10V_4 PEG_TX#2 — PEG_TX#[2]
M30 C_PEG_TX#3 C8219 0.1U/10V_4 PEG_TX#3 — PEG_TX#[3]
L31 C_PEG_TX#4 C8203 0.1U/10V_4 PEG_TX#4 — PEG_TX#[4]
K32 C_PEG_TX#5 C8208 0.1U/10V_4 PEG_TX#5 — PEG_TX#[5]
M29 C_PEG_TX#6 C8201 0.1U/10V_4 PEG_TX#6 — PEG_TX#[6]
J31 C_PEG_TX#7 C8202 0.1U/10V_4 PEG_TX#7 — PEG_TX#[7]
K29 C_PEG_TX#8 C8197 0.1U/10V_4 PEG_TX#8 — PEG_TX#[8]
H30 C_PEG_TX#9 C8196 0.1U/10V_4 PEG_TX#9 — PEG_TX#[9]
H29 C_PEG_TX#10 C8192 0.1U/10V_4 PEG_TX#10 — PEG_TX#[10]
F29 C_PEG_TX#11 C8189 0.1U/10V_4 PEG_TX#11 — PEG_TX#[11]
E28 C_PEG_TX#12 C8193 0.1U/10V_4 PEG_TX#12 — PEG_TX#[12]
D29 C_PEG_TX#13 C8188 0.1U/10V_4 PEG_TX#13 — PEG_TX#[13]
D27 C_PEG_TX#14 C8181 0.1U/10V_4 PEG_TX#14 — PEG_TX#[14]
C26 C_PEG_TX#15 C8183 0.1U/10V_4 PEG_TX#15 — PEG_TX#[15]

PEG_TX#[0..15] 17

L34 C_PEG_TX0 C8223 0.1U/10V_4 PEG_TX0 — PEG_TX[0]
M34 C_PEG_TX1 C8220 0.1U/10V_4 PEG_TX1 — PEG_TX[1]
M32 C_PEG_TX2 C8209 0.1U/10V_4 PEG_TX2 — PEG_TX[2]
L30 C_PEG_TX3 C8217 0.1U/10V_4 PEG_TX3 — PEG_TX[3]
M31 C_PEG_TX4 C8206 0.1U/10V_4 PEG_TX4 — PEG_TX[4]
K31 C_PEG_TX5 C8205 0.1U/10V_4 PEG_TX5 — PEG_TX[5]
M28 C_PEG_TX6 C8198 0.1U/10V_4 PEG_TX6 — PEG_TX[6]
H31 C_PEG_TX7 C8200 0.1U/10V_4 PEG_TX7 — PEG_TX[7]
K28 C_PEG_TX8 C8195 0.1U/10V_4 PEG_TX8 — PEG_TX[8]
G30 C_PEG_TX9 C8194 0.1U/10V_4 PEG_TX9 — PEG_TX[9]
G29 C_PEG_TX10 C8190 0.1U/10V_4 PEG_TX10 — PEG_TX[10]
F28 C_PEG_TX11 C8185 0.1U/10V_4 PEG_TX11 — PEG_TX[11]
E27 C_PEG_TX12 C8191 0.1U/10V_4 PEG_TX12 — PEG_TX[12]
D28 C_PEG_TX13 C8184 0.1U/10V_4 PEG_TX13 — PEG_TX[13]
C27 C_PEG_TX14 C8179 0.1U/10V_4 PEG_TX14 — PEG_TX[14]
C25 C_PEG_TX15 C8180 0.1U/10V_4 PEG_TX15 — PEG_TX[15]

IC,AUB_CFD_rPGA,R1P0

U8009B

R8150 20/F_4 H_COMP3 AT23 COMP3
R8148 20/F_4 H_COMP2 AT24 COMP2
R8011 49.9/F_4 H_COMP1 G16 COMP1
R8149 49.9/F_4 H_COMP0 AT26 COMP0
AH24 SKTOCC#

MISC

H_CATERR# AK14 CATERR#
11 H_PECI AT15 PECI
31,39 H_PROCHOT# AN26 PROCHOT#
11,31 PM_THRMTRIP# AK15 THERMTRIP#

THERMAL

34 H_CPURST# AP26 RESET_OBS#
10 PM_SYNC AL15 PM_SYNC
11,34 H_PWRGOOD AN14 VCCPWRGOOD_1
AN27 VCCPWRGOOD_0
SM_DRAMPWROK

34 H_PWRGD_XDP AM26 TAPPWRGOOD
H_VTTPWRGD AM15 VTTPWRGOOD
9,16,17,27,28,29,33,34 PLTRST# R8137 1.5K/F_4 CPU_PLTRST# AL14 RSTIN#
R8138 750/F_4

PWR MANAGEMENT

34 XDP_OBS[0:7]
XDP_OBS0 AJ22 BPM#[0]
XDP_OBS1 AK22 BPM#[1]
XDP_OBS2 AK24 BPM#[2]
XDP_OBS3 AJ24 BPM#[3]
XDP_OBS4 AJ25 BPM#[4]
XDP_OBS5 AH22 BPM#[5]
XDP_OBS6 AK23 BPM#[6]
XDP_OBS7 AH23 BPM#[7]

JTAG & BPM

IC,AUB_CFD_rPGA,R1P0

BCLK A16 CLK_CPU_BCLK 11
BCLK# B16 CLK_CPU_BCLK# 11
BCLK_ITP AR30 BCLK_ITP_P 34
BCLK_ITP# AT30 BCLK_ITP_N 34 For ITP CLK

CLOCKS

PEG_CLK E16 CLK_PCIE_3GPLL 9
PEG_CLK# D16 CLK_PCIE_3GPLL# 9
DPLL_REF_SSCLK A18
DPLL_REF_SSCLK# A17

SM_DRAMRST# F6 CPU_DRAMRST#

DDR3 MISC

SM_RCOMP[0] AL1 SM_RCOMP_0 R8124 100/F_4
SM_RCOMP[1] AM1 SM_RCOMP_1 R8127 24.9/F_4
SM_RCOMP[2] AN1 SM_RCOMP_2 R8218 130/F_4
R8155 10K/F_4
PM_EXT_TS#[0] AN15 PM_EXT_TS#0 R8156 *0/short_4 +1.1V_VTT
PM_EXT_TS#[1] AP15 PM_EXT_TS#1 R8147 *0/short_4 PM_EXTTS#0 14
R8154 10K/F_4 PM_EXTTS#1 15 +1.1V_VTT

PRDY# AT28 XDP_PRDY# 34
PREQ# AP27 XDP_PREQ# 34
TCK AN28 XDP_TCLK 34 T8999
TMS AP28 XDP_TMS 34 T8003
TRST# AT27 XDP_TRST# 34 T8008
TDI AT29 XDP_TDI_R T8007
TDO AR27 XDP_TDO_R T8005
TDI_M AR29 XDP_TDI_M T8006
TDO_M AP29 XDP_TDO_M T8004
DBR# AN25 XDP_DBRESET# 10,34

+1.1V_VTT

XDP_TDO R8173 51/J_4
H_CATERR# R8109 49.9/F_4
H_PROCHOT# R8153 68/J_4
CPU_PLTRST# R8140 *68/J_4
XDP_TMS R8165 *51/J_4
XDP_TDI_R R8175 *51/J_4
XDP_PREQ# R8167 *51/J_4
XDP_TCLK R8159 *51/J_4

+3V

U8006
MC74VHC1G08DFT2G
23,27,34,35,39 PWRGD
R8146 2K/F_4 H_VTTPWRGD
R8145 1K/F_4

JTAG MAPPING

XDP_TDI_R R8170 0/J_4
XDP_TDI_M R8164 *0/J_4
XDP_TDI 34
R8162 0/J_4
XDP_TDO_M R8161 *0/J_4
XDP_TDO_R R8166 0/J_4
XDP_TDO 34
XDP_TRST# R8174 51/J_4

Scan Chain (Default)	STUFF -> R97, R89, R90 NO STUFF -> R84, R512
CPU Only	STUFF -> R97, R84 NO STUFF -> R89, R512, R90
GMCH Only	STUFF -> R512, R90 NO STUFF -> R97, R84, R89

For S3 leakage issue

+1.5VSUS
R10130 1K/F_4
DDR3_DRAMRST# 14,15
Q9087 DMN601K-7
11 DDR3_RST — DDR3_RST
R10157 *0/J_4
35,40 +1.1V_VTT_PDK
MV modified for Intel comment
C10627 0.047U/25V_6
CPU_DRAMRST#
R10131 100K/F_4

+3VS5
R10155 10K/F_4
R10154 8.25K/F_4
U9059 MC74VHC1G08DFT2G
+1.5V_CPU
R8136 *1.1K/F_4
R10156 1.5K/F_4 DRAM_PWRGD_CPU
R8130 750/F_4

6,11,12,31,34,39,40 +1.1V_VTT
14,15,40,42,43 +1.5VSUS
3,8,9,10,11,12,14,15,16,20,23,25,27,28,29,30,31,32,33,34,35,37,39,42 +3V

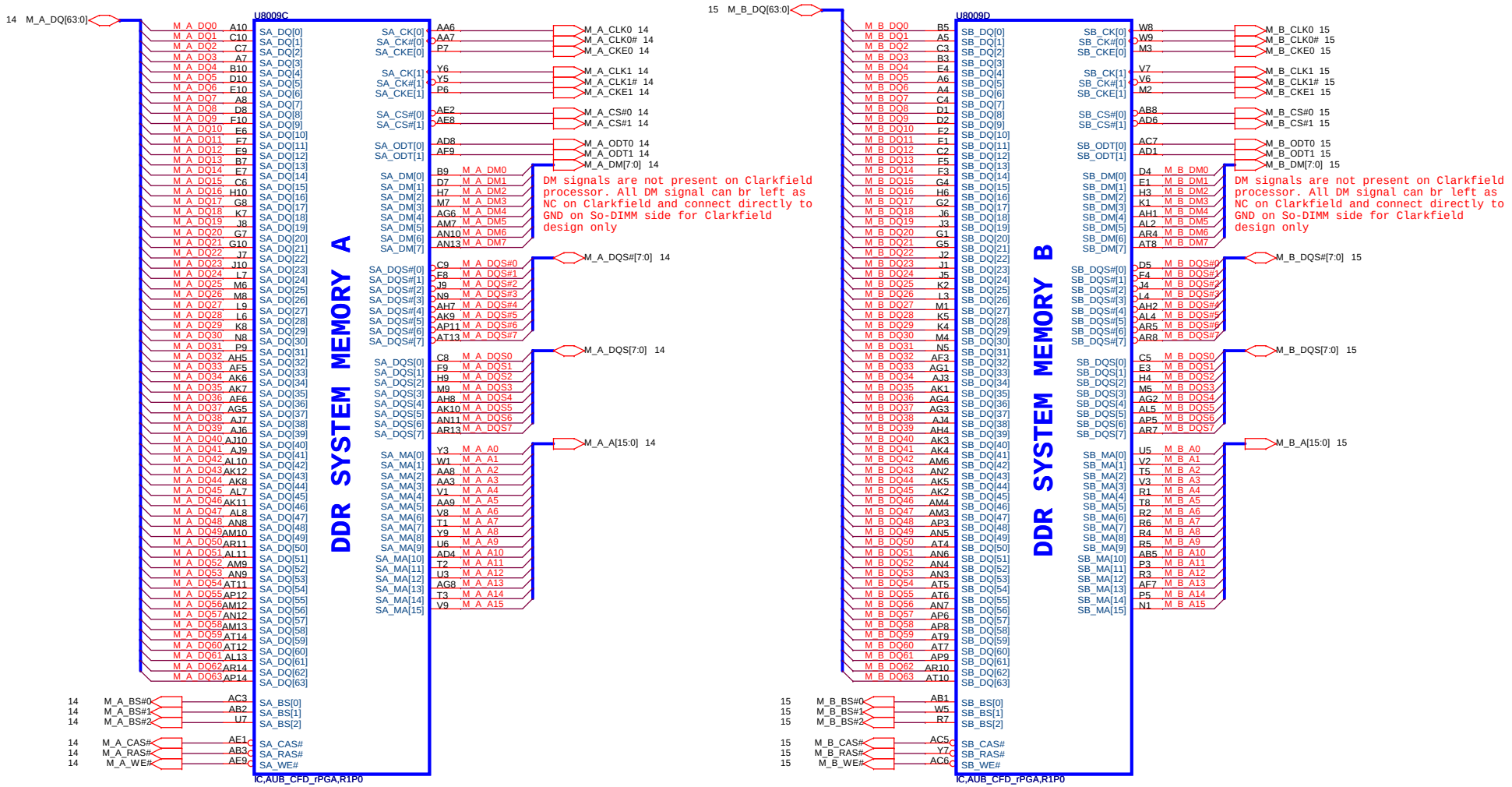
NB5

PROJECT : SX6
Quanta Computer Inc.

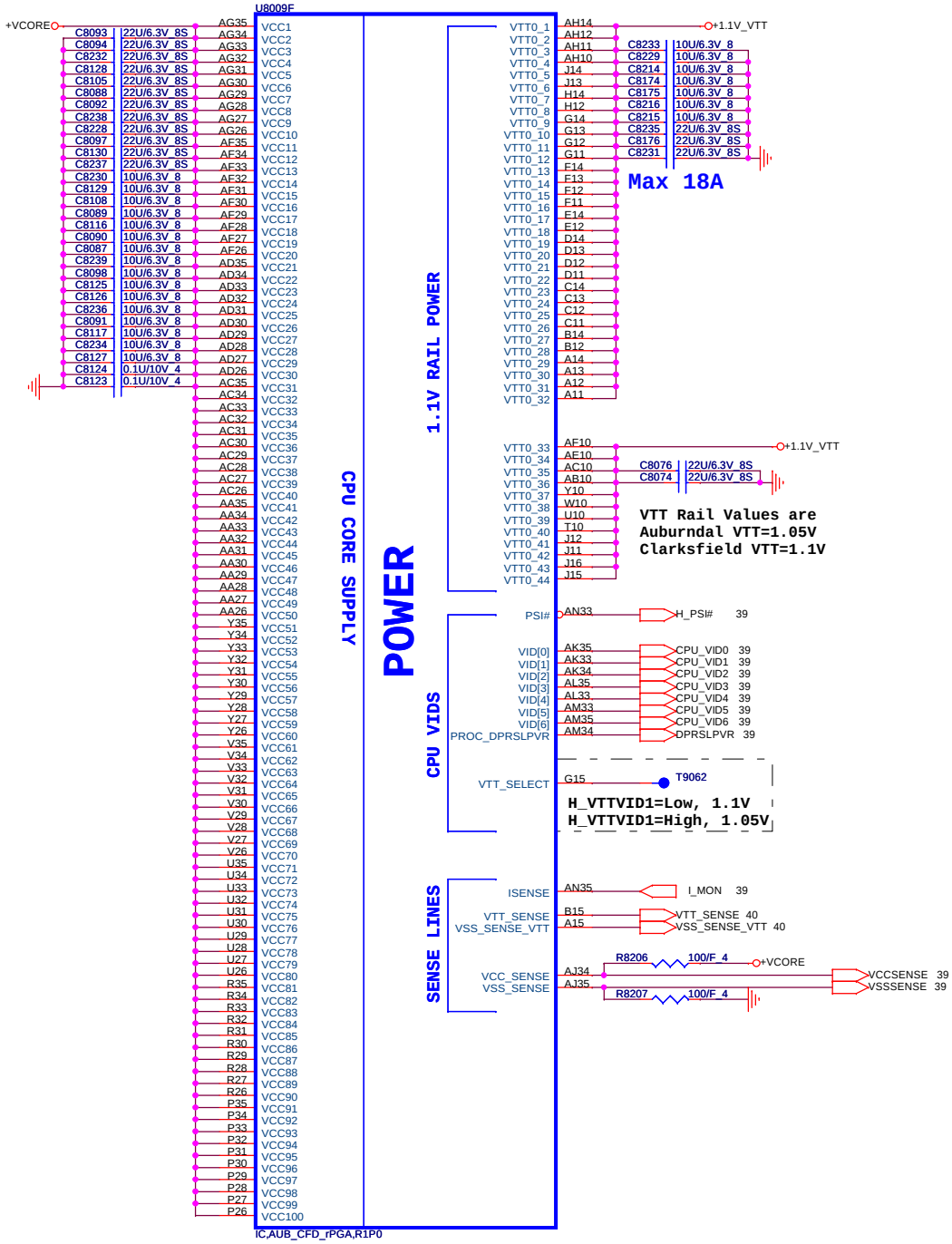
Size	Document Number	Rev
Custom	PROCESSER 1/4(HOST&PEX)	2B

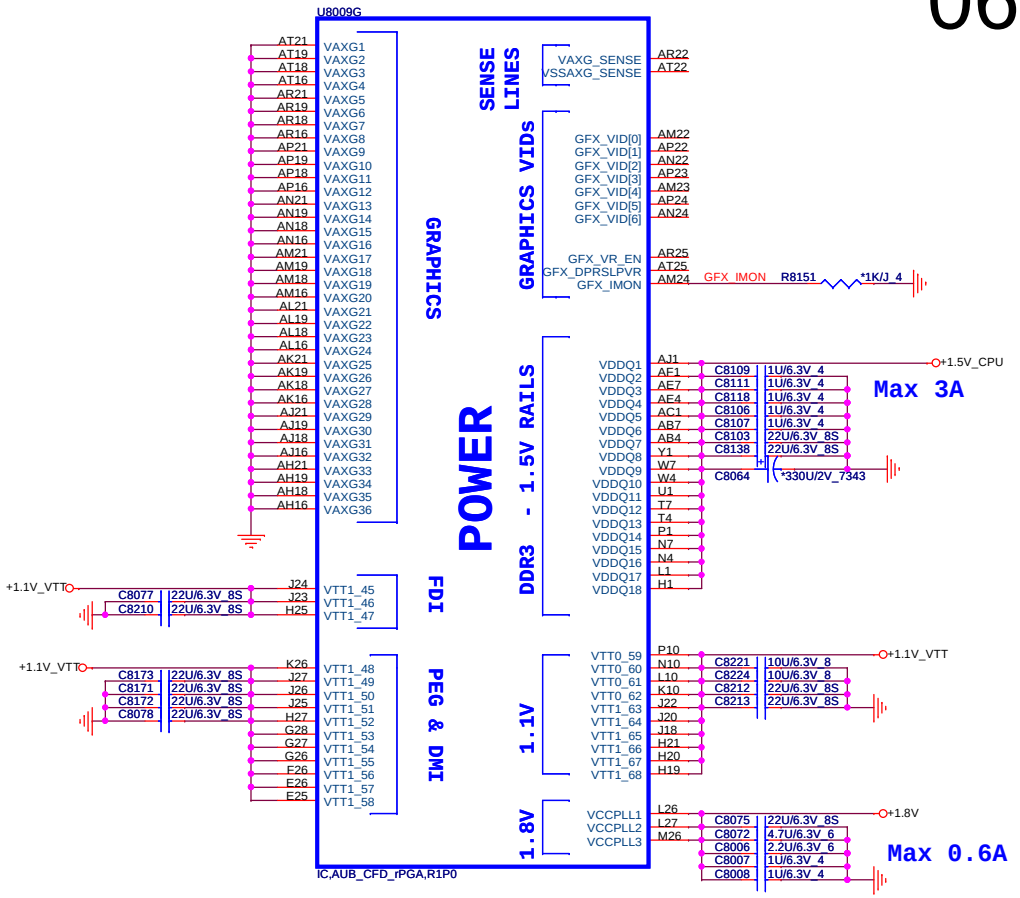
Date: Tuesday, December 22, 2009 Sheet 4 of 43

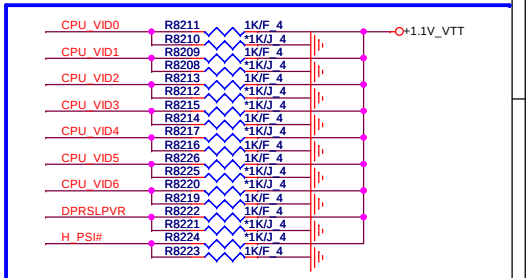
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



NB5	PROJECT : SX6 Quanta Computer Inc.	
Size: Custom	Document Number: PROCESSER 2/4(DDR)	Rev: 2B
Date: Tuesday, December 15, 2009	Sheet 5 of 43	







39 +VCORE
4,11,12,31,34,39,40 +1.1V_VTT
4,14,15,40,42,43 +1.5VSUS
11,12,41,42 +1.8V

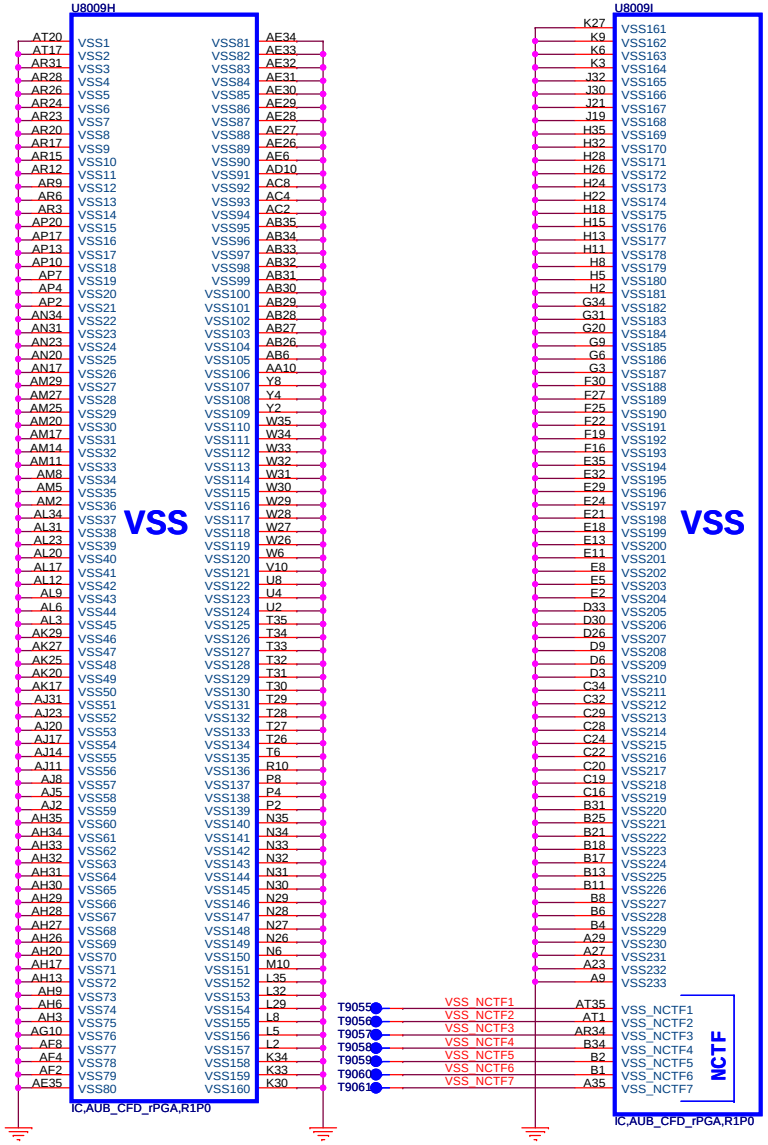
NB5

PROJECT : SX6
Quanta Computer Inc.

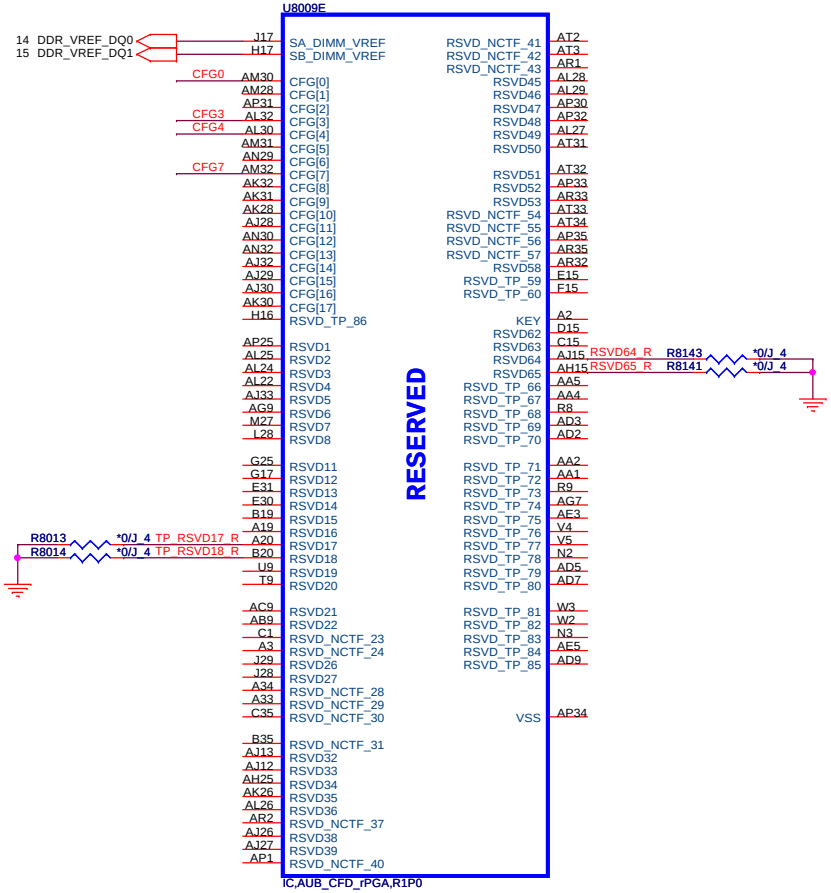
Size	Document Number	Rev
Custom	PROCESSER 3/4(POWER)	2B

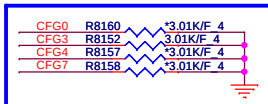
Date: Wednesday, December 16, 2009 Sheet 6 of 43

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)





CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

NB5

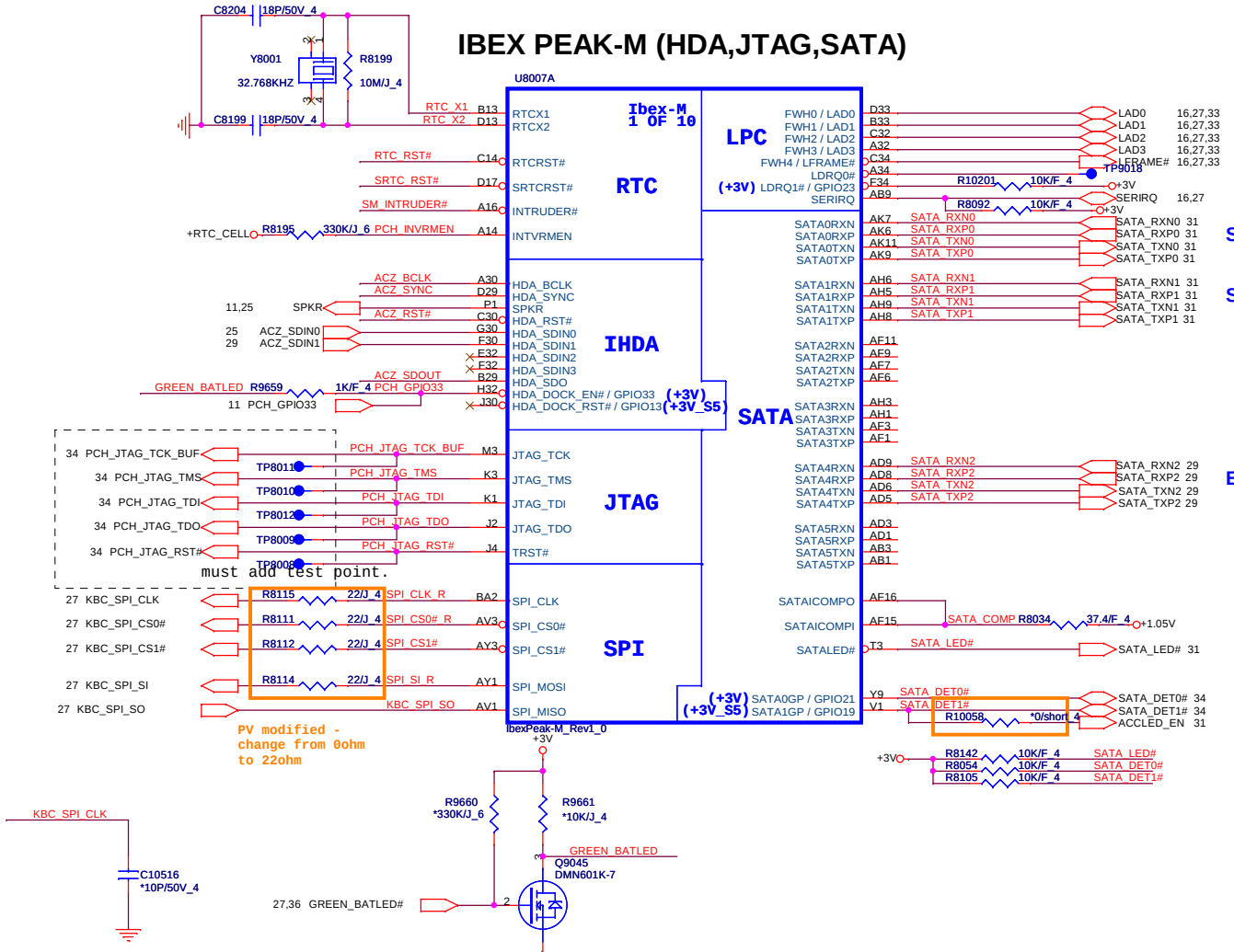
PROJECT : SX6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 4/4(GND)	2B

Date: Tuesday, December 15, 2009 Sheet 7 of 43

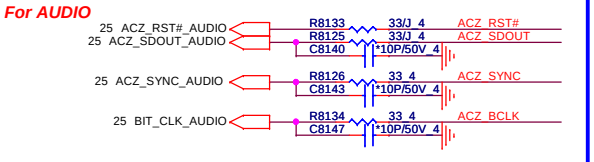
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

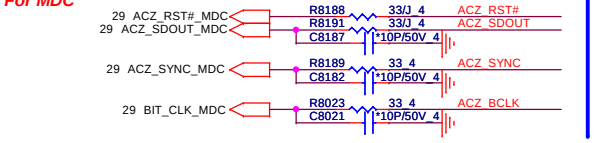


IBEX PEAK-M (LVDS,DDI)

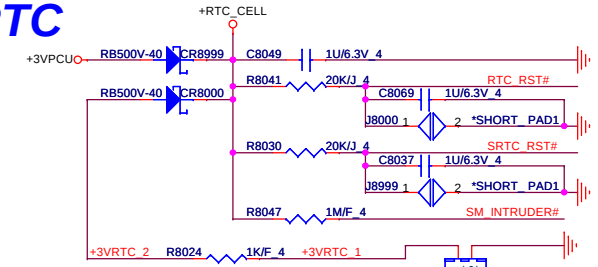
For AUDIO



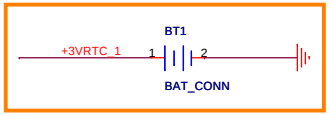
For MDC



RTC



PV modified -



CN7042
DFWF02MS022
SI change p/n
*85205-0200L

3,9,10,12,34,39,41 +1.05V
3,4,9,10,11,12,14,15,16,20,23,25,27,28,29,30,31,32,33,34,35,37,39,42 +3V
10,23,25,27,31,32,36,37,38 +3VPCU

NB5	PROJECT : SX6 Quanta Computer Inc.	
Size: Custom	Document Number: PCH 2/6 (SATA,HDA,LPC)	Rev: 2B
Date: Tuesday, December 15, 2009	Sheet 8 of 43	

IBEX PEAK-M (PCI-E,SMBUS,CLK)

09

U8007B

Ibex-M
2 OF 10

PCI-E*

SMBus

Controller Link

PEG

From CLK BUFFER

Clock Flex

[Epress Card]

[WLAN]

[PCIE_LAN]

New Card

WLAN

PCIE_RXN2 PCIE_RXP2 PCIE_TXN2 PCIE_TXP2 — C8010 0.1U/10V_4 PCIE_TXN2_C, C8016 0.1U/10V_4 PCIE_TXP2_C

PCIE_RXN4 PCIE_RXP4 PCIE_TXN4 PCIE_TXP4 — C8041 0.1U/10V_4 PCIE_TXN4_C, C8034 0.1U/10V_4 PCIE_TXP4_C

PCIE_RXN6 PCIE_RXP6 PCIE_TXN6 PCIE_TXP6 — C8004 0.1U/10V_4 PCIE_TXN6_C, C8009 0.1U/10V_4 PCIE_TXP6_C

CLK1_OE# → R8083 *0/short_4 → CLK2_OE#

PCIE_CLK_REQ0# PCIE_CLK_REQ3# PCIE_CLK_REQ4# PCIE_CLK_REQB# PCIE_CLK_REQ5#

CLK_PCIE_WLAN# CLK_PCIE_WLAN

R10132 100K/J_4 +3VS5

D9022 *SDMK0340L-7-F LID_SW# 23,27,31

SMBALERT# SMBCLK SMBDATA SMBL0ALERT# SMB_CLK_ME0 SMB_DATA_ME0 SMBL1ALERT# SMB_CLK_ME1 SMB_DATA_ME1

PEG_CLKREQ#

CL_CLK1 CL_DATA1 CL_RST1# → T9048 T9049 T9050

MBCLK2 MBDATA2 — Q8004 Q8005 DMN601K-7 SMB_CLK_ME1 SMB_DATA_ME1

CLK_PCIE_VGA# CLK_PCIE_VGA CLK_PCIE_3GPLL# CLK_PCIE_3GPLL

CLKOUT_DP_N / CLKOUT_BCLK1_N CLKOUT_DP_P / CLKOUT_BCLK1_P

CLKIN_DMI_N CLKIN_DMI_P → CLK_DMI# CLK_DMI

CLKIN_BCLK_N CLKIN_BCLK_P → CLK_BUF_BCLK_N CLK_BUF_BCLK_P

CLKIN_DOT_96N CLKIN_DOT_96P → CLK_BUF_DREFCLK# CLK_BUF_DREFCLK

CLKIN_SATA_N / CKSSCD_N CLKIN_SATA_P / CKSSCD_P → CLK_BUF_DREFSSCLK# CLK_BUF_DREFSSCLK

REFCLK14IN → CLK_ICH_14M

CLKIN_PCILOOPBACK → CLK_PCI_FB

XTAL25_IN XTAL25_OUT

XCLK_RCOMP → R8010 90.9/F_4 +1.05V

CLKOUTFLEX0 / GPIO64 → T8000
CLKOUTFLEX1 / GPIO65 → T8002
CLKOUTFLEX2 / GPIO66 → T9051
CLKOUTFLEX3 / GPIO67 → R9663 33_4 → CLK_48M_CR

CLK_48M_CR → C10517 *10P/50V_4

U8003 *MC74VHC1G08DFT2G — C8139 *0.1U/10V_4

PLT_RST-R# → PLTRST# 4,16,17,27,28,29,33,34

R8108 100K/F_4 R8121 *100K/F_4 R8122 *0/short_4

PV modified - change from 0ohm to short pad

Q8003 Q8001 DMN601K-7 — SMBDATA SMBCLK → CGDAT_SMB CGCLK_SMB 3,14,15,29,31,33

R8120 4.7K/F_4 R8107 4.7K/F_4 +3VO

Intel suggest 25MHz X'tal can be removed in POR 3/16

XTAL25_IN XTAL25_OUT — C8168 *18P/50V_4 C8167 *18P/50V_4 R8183 *1M/F_4 Y8999 *25MHZ

3,8,10,12,34,39,41 +1.05V
3,4,8,10,11,12,14,15,16,20,23,25,27,28,29,30,31,32,33,34,35,37,39,42 +3V

IbexPeak-M_Rev1_0

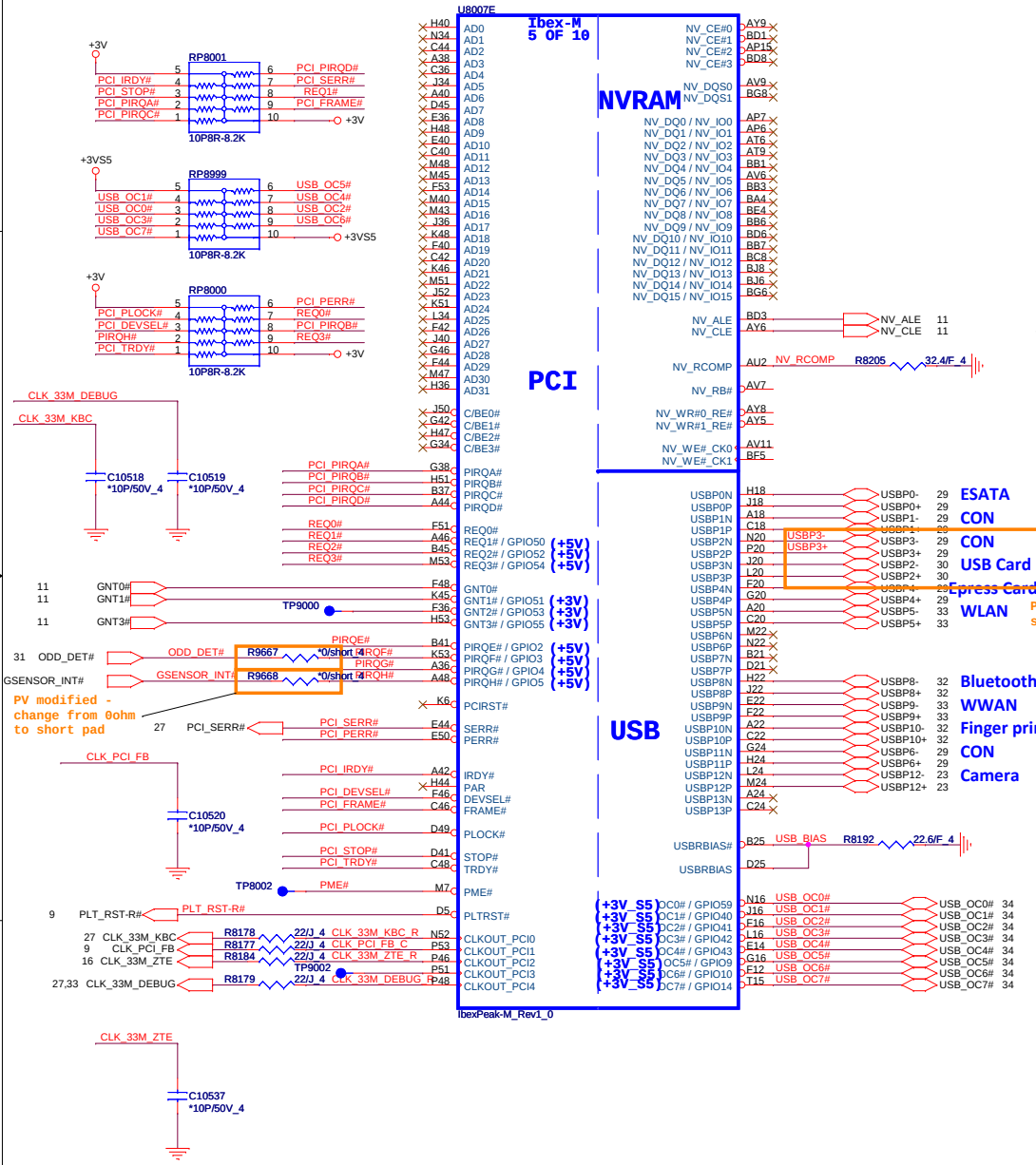
NB5

PROJECT : SX6
Quanta Computer Inc.

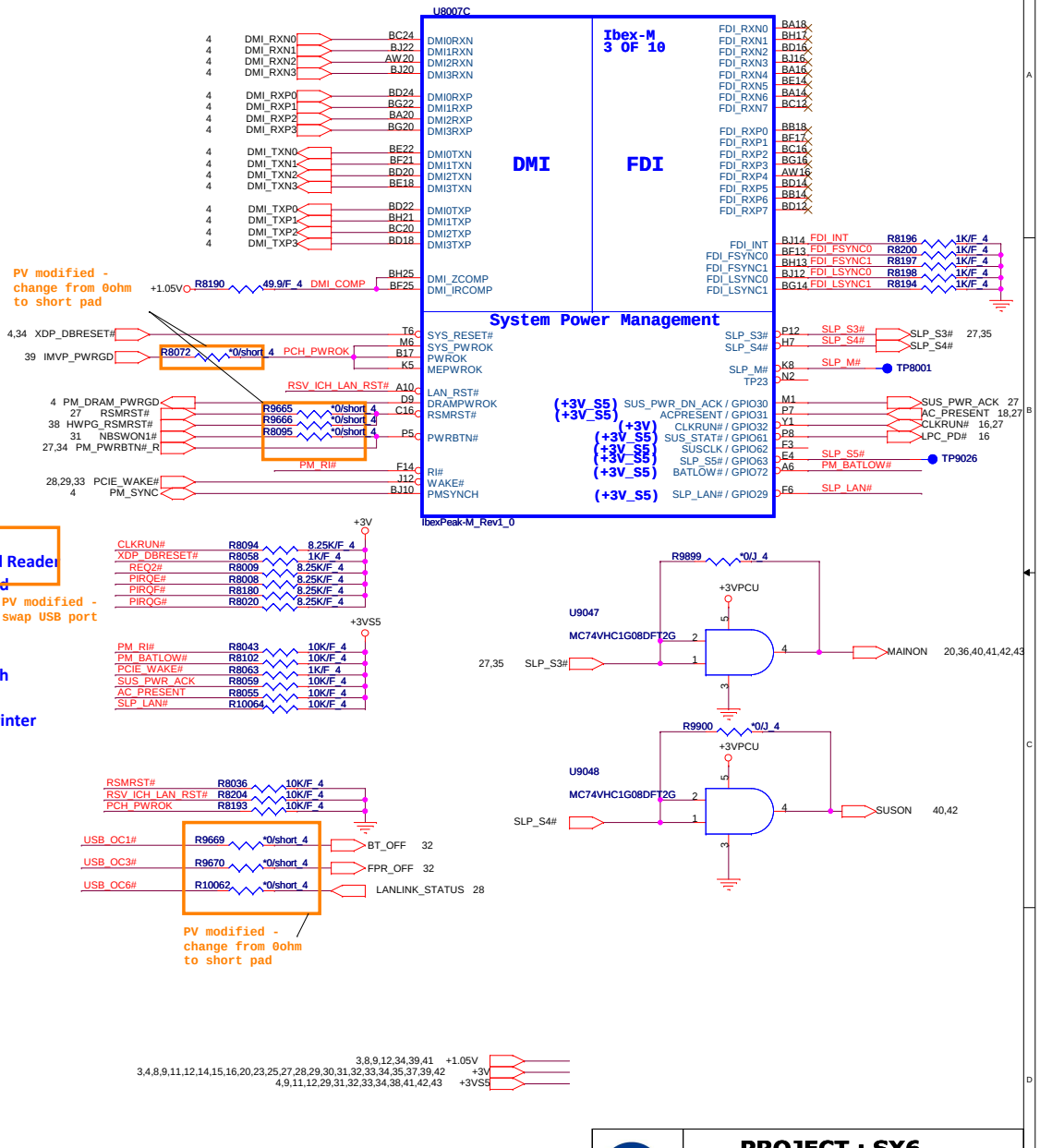
Size	Document Number	Rev
Custom	PCH 3/6 (PCI,ONFI,USB,CK)	2B

Date: Tuesday, December 15, 2009 Sheet 9 of 43

IBEX PEAK-M (PCI,USB,NVRAM)



IBEX PEAK-M (DMI,FDI,GPIO)



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

U8007F

Ibex-M
6 OF 10

GPIO MISC

34 BMBUSY#	Y3	BMBUSY# / GPIO0 (+3V)
37 OCP#	C38	TACH1 / GPIO1 (+3V)
27 SIO_EXT_SCI#	D37	TACH2 / GPIO6 (+3V)
31 THERM_SCI#	J32	TACH3 / GPIO7 (+3V)
4 DDR3_RST	F10	GPIO8 (+3V_S5)
28 CB_IN# R8075 *0_4 LAN_CABLE_DET#	K9	LAN_PHY_PWR_CTRL / GPIO12 (+3V_S5)
PCH_GPIO15	T7	GPIO15 (+3V_S5)
34 SATA4GP	AA2	SATA4GP / GPIO16 (+3V)
PCH_GPIO17	F38	TACH0 / GPIO17 (+3V)
33 WWAN_DET#	Y7	SCLOCK / GPIO22 (+3V)
33 WWAN_OFF#	AB12	GPIO27 (+3V_S5)
28,34 LAN_DIS#	V13	GPIO28 (+3V_S5)
34 SATA2GP	AB7	SATA2GP / GPIO36 (+3V)
23,34 SATA3GP	AB13	SATA3GP / GPIO37 (+3V)
23,34 WEBCAM_OFF	P3	SDATAOUT0 / GPIO39 (+3V)
GPIO46	F1	PCIECLKRQ7# / GPIO46 (+3V_S5)
SV_SET_UP	AB6	SDATAOUT1 / GPIO48 (+3V)
34 SATA5GP	AA4	SATA5GP / GPIO49 (+3V)
GPIO24	H10	GPIO24 (+3V_S5)
28 PCIE_LAN_CLK_REQ#	H3	PCIECLKRQ6# / GPIO45 (+3V_S5)
33 WLAN_OFF#	F8	GPIO57 (+3V_S5)
STP_PCI#	M11	STP_PCI# / GPIO34 (+3V)
SATACLKREQ#	V6	SATACLKREQ# / GPIO35 (+3V)
DOCK_ID0	V3	SLOAD / GPIO38 (+3V)

CPU

CLKOUT_PCIE6N	AH45	CLK_PCIE_LAN# 28
CLKOUT_PCIE6P	AH46	CLK_PCIE_LAN 28
CLKOUT_PCIE7N	AF48	
CLKOUT_PCIE7P	AF47	
A20GATE	U2	GATEA20 27
CLKOUT_BCLK0_N/CLKOUT_PCIE8N	AM3	CLK_CPU_BCLK# 4
CLKOUT_BCLK0_P/CLKOUT_PCIE8P	AM1	CLK_CPU_BCLK 4
PECI	BG10	PCH_PECI_R R8201 *0/short_4 H_PECI 4
RCIN#	T1	KB_RST# 27
PROCPWRGD	BE10	H_PWRGOOD 4,34
THRMTRIP#	BD10	PCH_THRMTRIP# R8037 56.2/F_4 PM_THRMTRIP# 4,31
+1.1V_VTT		R8038 56.2/F_4

RSVD

TP1 BA22, TP2 AW22, TP3 BB22, TP4 AY45, TP5 AY46, TP6 AV43, TP7 AV45, TP8 AF13, TP9 M18, TP10 N18, TP11 AJ24, TP12 AK41, TP13 AK42, TP14 M32, TP15 N32, TP16 M30, TP17 N30, TP18 H12, TP19 AA23, NC_1 AB45, NC_2 AB38, NC_3 AB42, NC_4 AB41, NC_5 T39, INIT3_3V# P6, TP24 C10

NCTF

PCH_NCTF6	A4	VSS_NCTF_1	BH2
PCH_NCTF7	A49	VSS_NCTF_2	BH52
	A5	VSS_NCTF_3	BH53
	A50	VSS_NCTF_4	BJ1 PCH_NCTF19
	A52	VSS_NCTF_5	BJ2
	A53	VSS_NCTF_6	BJ4
	B2	VSS_NCTF_7	BJ49
	B4	VSS_NCTF_8	BJ5
	B52	VSS_NCTF_9	BJ50
	B53	VSS_NCTF_10	BJ52
	BE1	VSS_NCTF_11	BJ53 PCH_NCTF26
	BE53	VSS_NCTF_12	D1
	BF1	VSS_NCTF_13	D2
	BF53	VSS_NCTF_14	D53
	BH1	VSS_NCTF_15	E1
		VSS_NCTF_16	E53

IbexPeak-M_Rev1_0

PV modified - change from 0ohm to short pad

SATA2GP R9674 *0/short_4 NPCI_RST# 27

LAN

+3V

R9671 100K/F_4 Q9046 DMN601K-7 CRACK_BGA 19,27 PCH_NCTF6

R9672 100K/F_4 Q9047 DMN601K-7 CRACK_BGA 19,27 PCH_NCTF7

R9673 100K/F_4 Q9048 DMN601K-7 CRACK_BGA 19,27 PCH_NCTF19

R9675 100K/F_4 Q9049 DMN601K-7 CRACK_BGA 19,27 PCH_NCTF26

+3VS5

DDR3_RST	R8065	10K/F_4
PCH_GPIO15	R8026	1K/F_4
LAN_CABLE_DET#	R10147	10K/F_4
WWAN_OFF#	R9676	10K/F_4
GPIO24	R8085	10K/F_4
WLAN_OFF#	R8066	10K/F_4
GPIO46	R9677	10K/F_4
PCIE_LAN_CLK_REQ#	R8098	10K/F_4
LAN_DIS#	R8033	10K/F_4

+3V

KB_RST#	R8106	10K/F_4
GATEA20	R8080	10K/F_4
SATA2GP	R8053	10K/F_4
SATA3GP	R8040	10K/F_4
SATA4GP	R8104	10K/F_4
SATA5GP	R8093	10K/F_4
BMBUSY#	R8096	10K/F_4
SIO_EXT_SCI#	R8018	10K/F_4
THERM_SCI#	R8021	10K/F_4
PCH_GPIO17	R8017	10K/F_4
WWAN_DET#	R8069	10K/F_4
STP_PCI#	R8056	10K/F_4
SATACLKREQ#	R8067	10K/F_4
DOCK_ID0	R8068	10K/F_4
DOCK_ID1	R8078	10K/F_4

4,6,12,31,34,39,40 +1.1V_VTT
6,12,41,42 +1.8V
3,4,8,9,10,12,14,15,16,20,23,25,27,28,29,30,31,32,33,34,35,37,39,42 +3V
4,9,10,12,29,31,32,33,34,38,41,42,43 +3VS5

10 GNT3# R8182 *10K/J_4

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP R8076 10K/F_4 +3V

SV_SET_UP	1-X High = Strong (Default)

10 GNT0# R8005 *1K/J_4
10 GNT1# R8181 *1K/J_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

10 NV_ALE R8202 *1K/J_4
10 NV_CLE R8203 *1K/J_4 +1.8V

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

No Reboot Strap

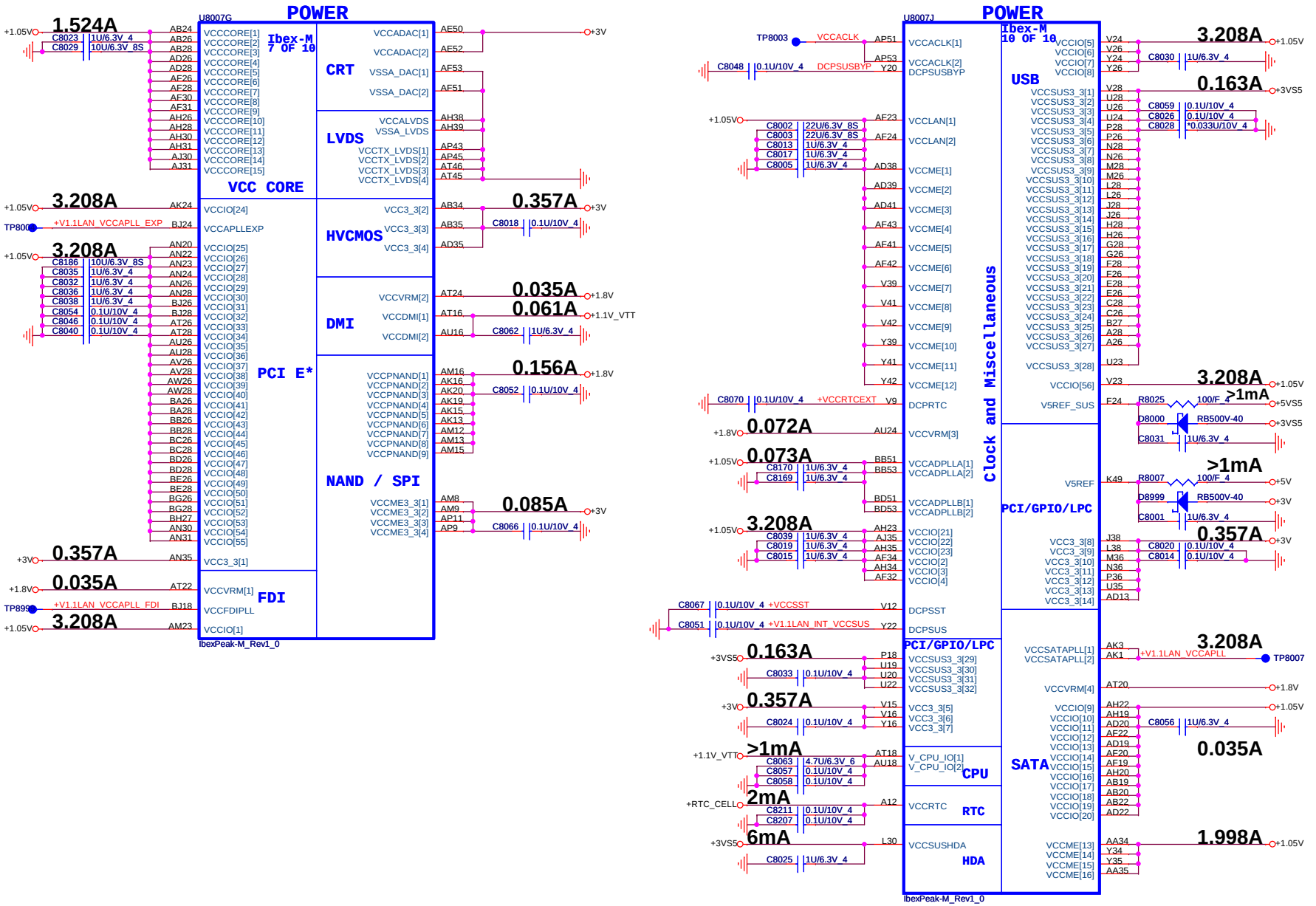
8,25 SPKR SPKR R8132 *1K/J_4 +3V

8 PCH_GPIO33 R8022 *100K/J_4

NB5

PROJECT : SX6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO & Strap)	2B
Date: Tuesday, December 15, 2009	Sheet 11 of 43	



3,8,9,10,34,39,41 +1.05V
4,6,11,31,34,39,40 +1.1V_VTT
6,11,41,42 +1.8V
3,4,8,9,10,11,14,15,16,20,23,25,27,28,29,30,31,32,33,34,35,37,39,42 +3V
4,9,10,11,29,31,32,33,34,38,41,42,43 +3VS5
20,23,24,25,31,32,35,37,42 +5V
23,35,36,37,38,40,42 +5VS5

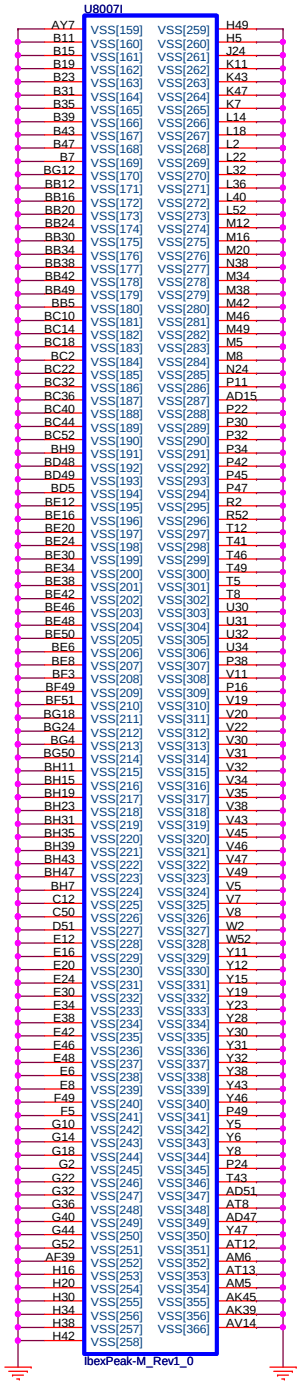
PROJECT : SX6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	2B

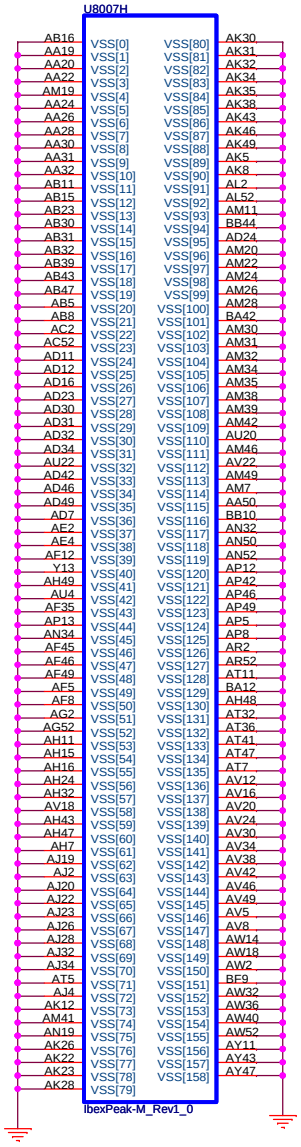
NB5

Date: Tuesday, December 15, 2009 | Sheet 12 of 43

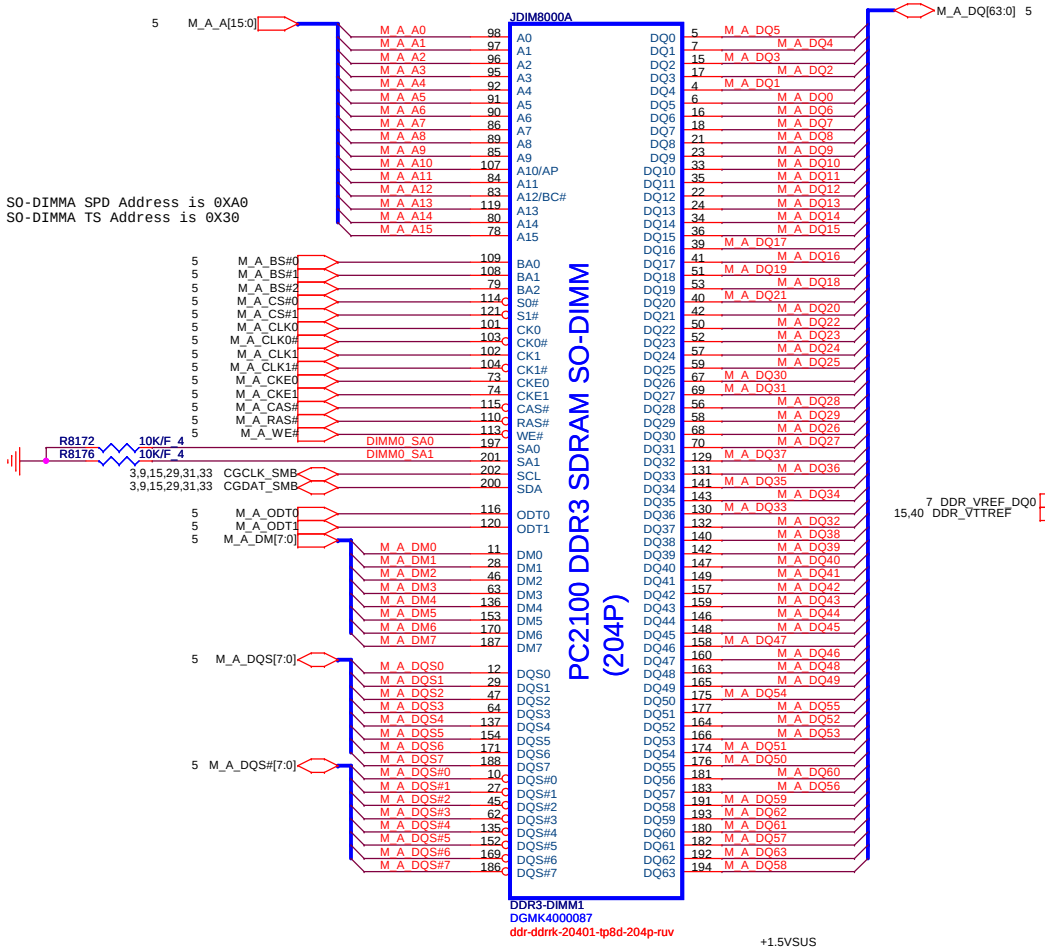
IBEX PEAK-M (GND)

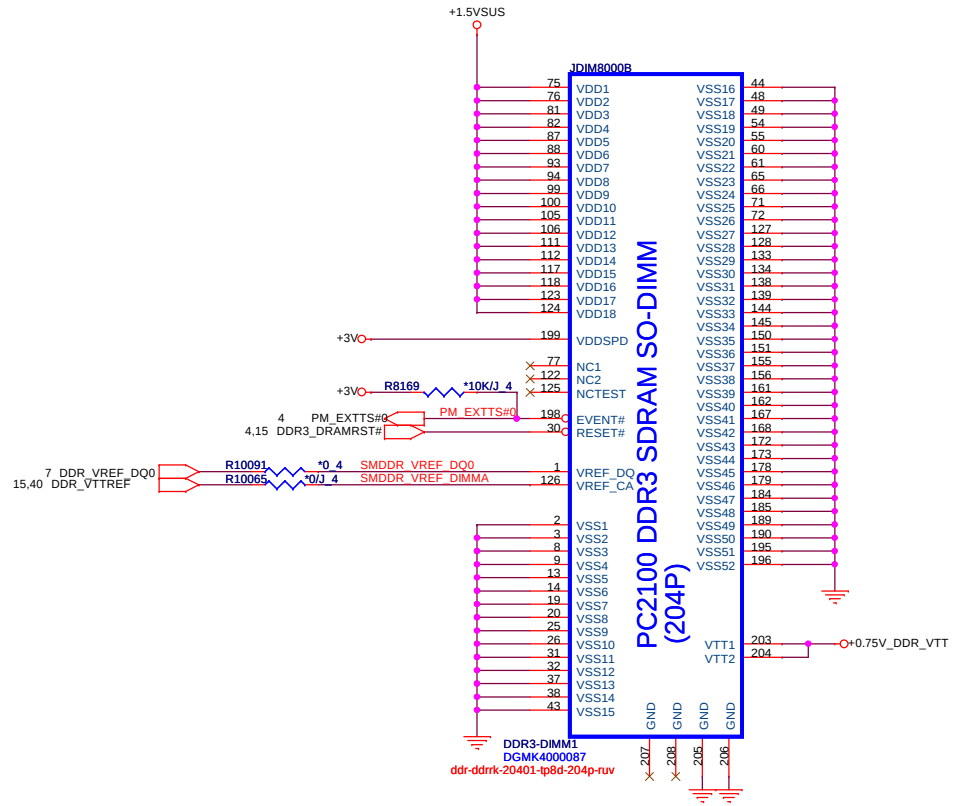


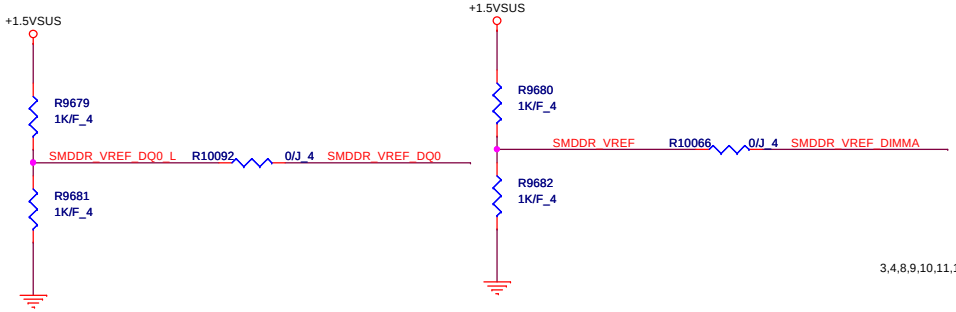
IBEX PEAK-M (GND)

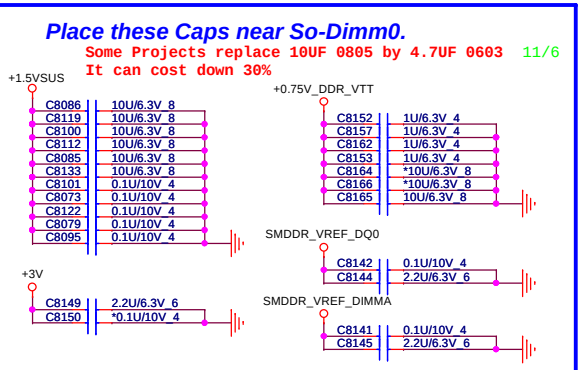


NB5	PROJECT : SX6 Quanta Computer Inc.	
Size: Custom	Document Number: PCH 6/6 (GND)	Rev: 2B
Date: Tuesday, December 15, 2009	Sheet 13 of 43	









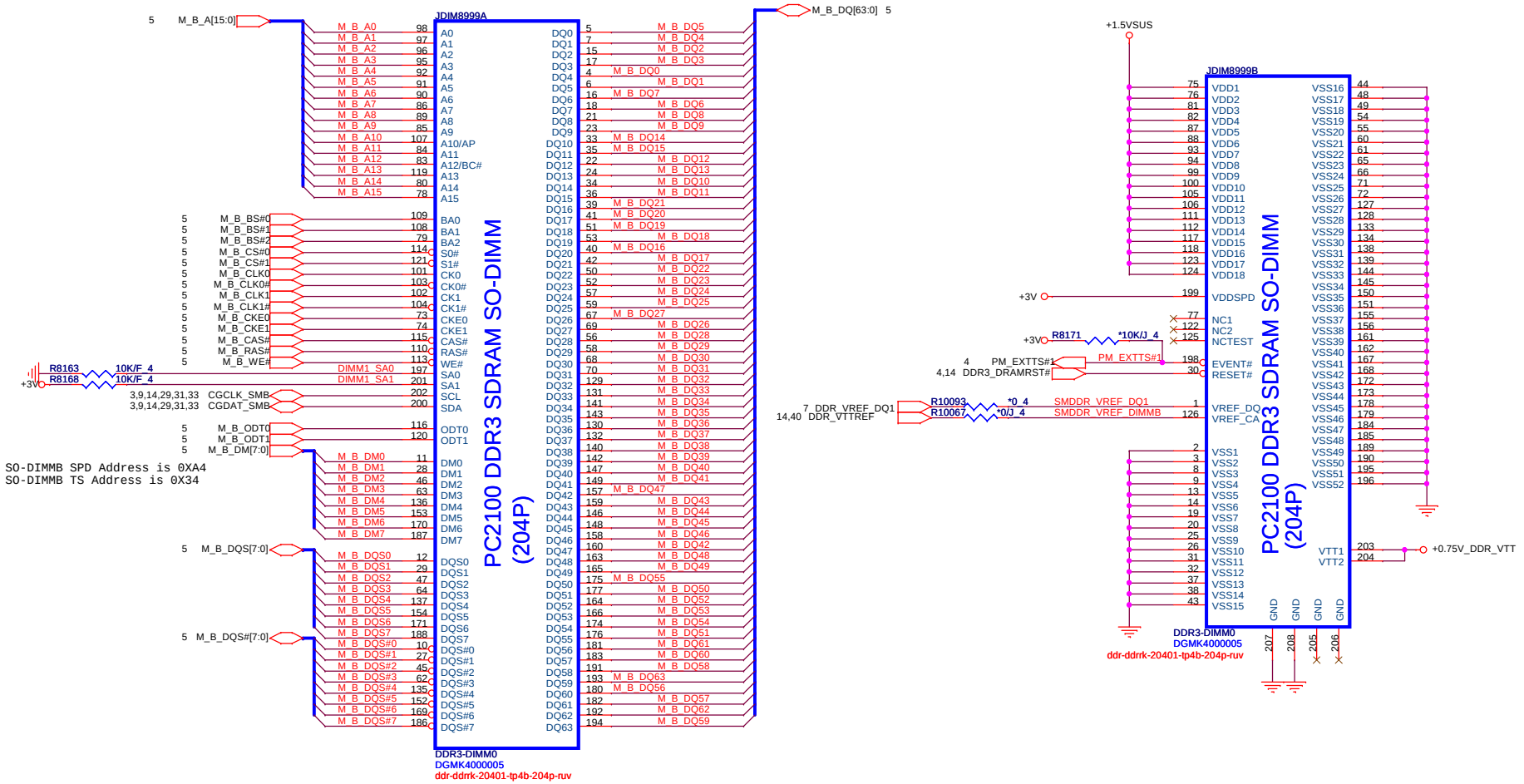
15,40,42 +0.75V_DDR_VTT
4,15,40,42,43 +1.5VSUS
3,4,8,9,10,11,12,15,16,20,23,25,27,28,29,30,31,32,33,34,35,37,39,42 +3V
8,10,23,25,27,31,32,36,37,38 +3VPCU
+5VPCU

NB5

PROJECT : SX6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-0	2B

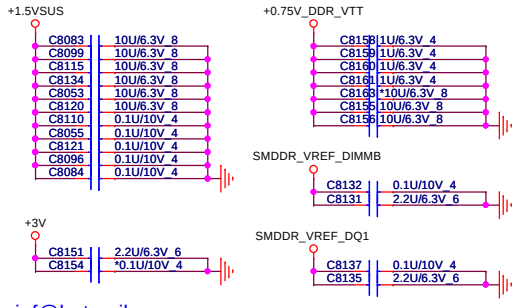
Date: Tuesday, December 15, 2009 | Sheet 14 of 43

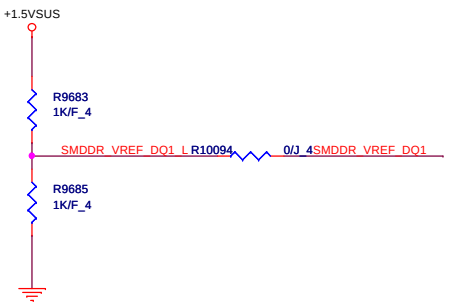


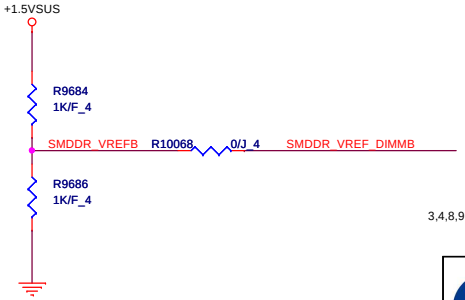
Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603

It can cost down 30%







14,40,42 +0.75V_DDR_VTT
4,14,40,42,43 +1.5VSUS
3,4,8,9,10,11,12,14,16,20,23,25,27,28,29,30,31,32,33,34,35,37,39,42 +3V
8,10,23,25,27,31,32,36,37,38 +3VPCU
+5VPCU

NB5

PROJECT : SX6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1	2B

Date: Tuesday, December 15, 2009 Sheet 15 of 43

H1 *H-C354D118P2
H2 *H-C354D118P2
H3 *H-C394D276P2
H4 *H-C394D276P2
H5 *H-C197D181P2
H6 *H-C197D181P2
VGA HOLE
H7 *H-TC374197BC197D181P2
H8 *H-TC374197BC197D181P2
H9 *H-TC374197BC197D181P2
H10 *H-TC374197BC197D181P2
CPU HOLE
H11 *H-TC2768C236D91P2
H12 *H-TC2768C236D91P2
H13 *H-TC2768C236D91P2
H14 *H-TC2768C236D91P2
Epress card screw HOLE
PAD1
PAD2
PAD3
PAD4
PAD5
PAD7
GND PAD
PAD6
PAD8
PAD9
H15 *H-C354D276P2
H16 *H-C354D276P2
H20 *H-TC3548C276D118P2
H22 *H-TC3548C276D118P2
H27 *H-TC394BC354D276P2
H29 *H-TC236BC276D118P2
H30 *H-C433D394P2
H31 *H-C315D276P2
H23 *H-C197D91P2
H24 *H-C197D91P2
HDD screw HOLE
H25 *H-C197D91P2
H26 *H-C197D91P2
ODD screw HOLE
MBAT8002019
H32 *MBAT8002019
WLAN CARD NUT
MBAT8002019
H19 *MBAT8002019
WWAN CARD NUT
H17 MBZR1002015
H18 MBZR1002015
MDC NUT
MBZR1002015

BADD1	BADD0	
0	0	EE/EF
0	1	7E/7F
1	0	2E/2F
1	1	4E/4F(Defult)

U9066
ZTEIC
*SSX44-B-H-Q
LAD0 LAD1 LAD2 LAD3 LFRAME#
PLTRST# CLK_33M_ZTE LPC_PD# CLKRUN# SERIRQ
NC_P
GPIO3 GPIO15 GPIO16
PP BADD0 BADD1
GND EPAD
VCC3
+3V
8,27,33 LAD0
8,27,33 LAD1
8,27,33 LAD2
8,27,33 LAD3
8,27,33 LFRAME#
4,9,17,27,28,29,33,34 PLTRST#
10 CLK_33M_ZTE
10 LPC_PD#
10,27 CLKRUN#
8,27 SERIRQ
LPC_PP
BADD0
BADD1
R9690 *10K/F_4
R9662 *10K/F_4
R9678 *10K/F_4
Not Stuff
Not Stuff
CLK_33M_ZTE
R9709 *33
C9981 *10P
Close to U9066
C9982 *0.1U/16V_4
C9983 *0.1U/16V_4
C9984 *0.1U/16V_4
C10464 *1U/6.3V_4

NB5

PROJECT : SX6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hole, Nuts,TCM	2B

Date: Tuesday, December 15, 2009 Sheet 16 of 43

POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=0.9~1.2V

POWER
for M9x-S3 DPx_VDD10=1.1V
for Park-S3 DPx_VDD10=1.0V

2.5GT/s bit rate

U9050A

PCI EXPRESS INTERFACE

M93-S3_LP

100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing

VGA Core BPP
VGA Core VDDC

+1.8V PCIE_VDDR
+1.8V PCIE_PVDD
+1.8V VDDR1

3.3V_Delay VDDR3

20ms 20ms

U9050G

M9x-S3:TMDS 1.1V@170mA LVDS 1.1V@100mA
Park-S3:TMDS 1.0V@110mA LVDS 1.0V@120mA

M9x-S3:1.1V@200mA Park-S3:1.0V@110mA

M93-S3_LP

PROJECT : SX6
Quanta Computer Inc.

NB5/RD2

Size Custom | Document Number Park_PCIE_Interface | Rev 2B

Date: Tuesday, December 15, 2009 | Sheet 17 of 43

R9917 10K/F_4 GPIO22

GPIO22(ROMCS#)
PD without external VBIOS ROM

MEM_ID[3:0]	Vendor	Type	Vendor P/N	Quanta P/N
0000 0100	Samsung E-die Hynix Orion-die	64*16-800MHZ 64*16-800MHZ	K4W1G1646E-HC12 H5TQ1G63BFR-12C	AKD5LGGT503 AKD5LZGTW01

I.MEMID_0: ODM, 0'Quanta 1'Wistron
II.MEMID_1: Vram size, 0'512MB, 1'1GB
III.MEMID_2: Vram vender, 0'sunsumg, 1'hyniex.

Hynix 512M 0100	上件	不上件
	R9919	R9921,R9920,R9918

Samsung 512M 0000	上件	不上件
	NA	R9921,R9920,r9919,R9918

Hynix 1G 0110	上件	不上件
	R9919,R9920	R9921,R9918

Samsung 1G 0010	上件	不上件
	R9920	R9921,R9919,R9918

	PWRCNTL1	PWRCNTL0	V-CORE
	1	1	0.9V
	1	0	0.95V
	0	1	1.05V
	0	0	1.1V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V

for Park-S3 only

No need "CLK_27M_SS" connect to GPIO_16, since M9x chip support memory SS function in VBIOS

M93-S3/ Park-S3:Use 150R Pull down
Park-S3:NC

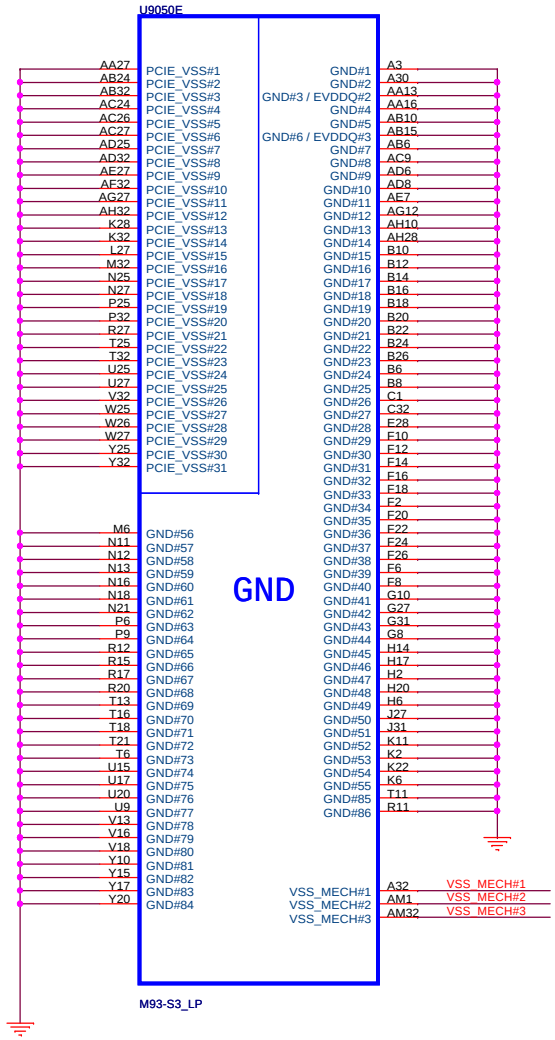
PV modified - change R9929 from 0ohm to short pad

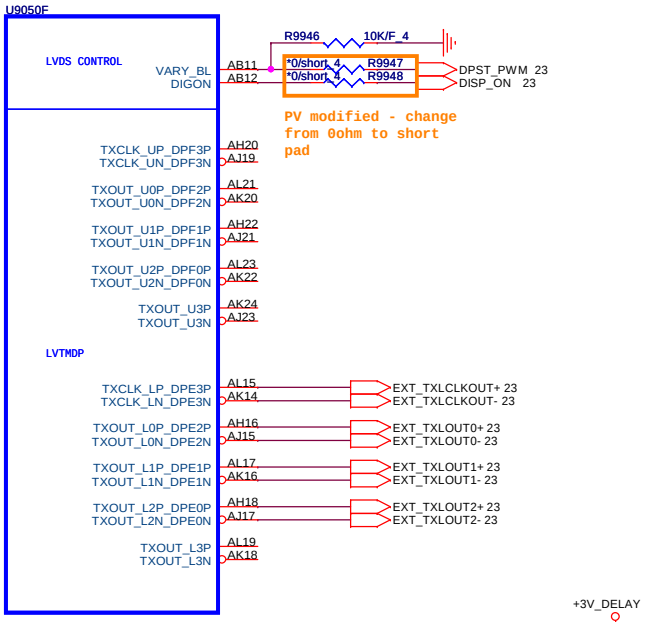
PV modified - change R9924,R9926,R9928 from 0ohm to short pad

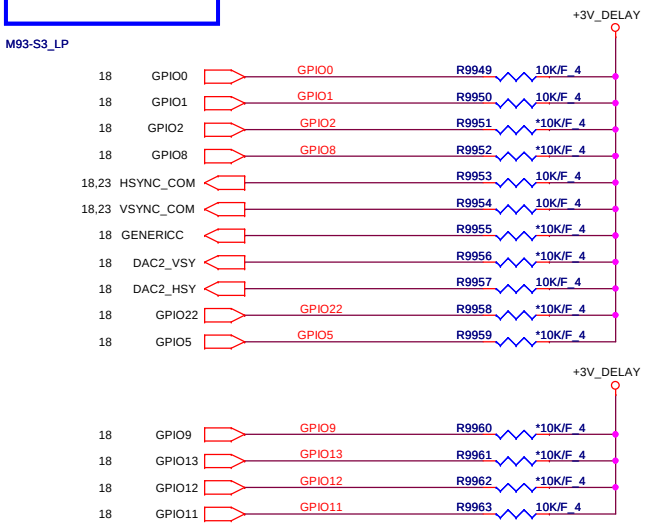
PV modified - change Q9078 and Q9079 pin connection for fix leakage issue

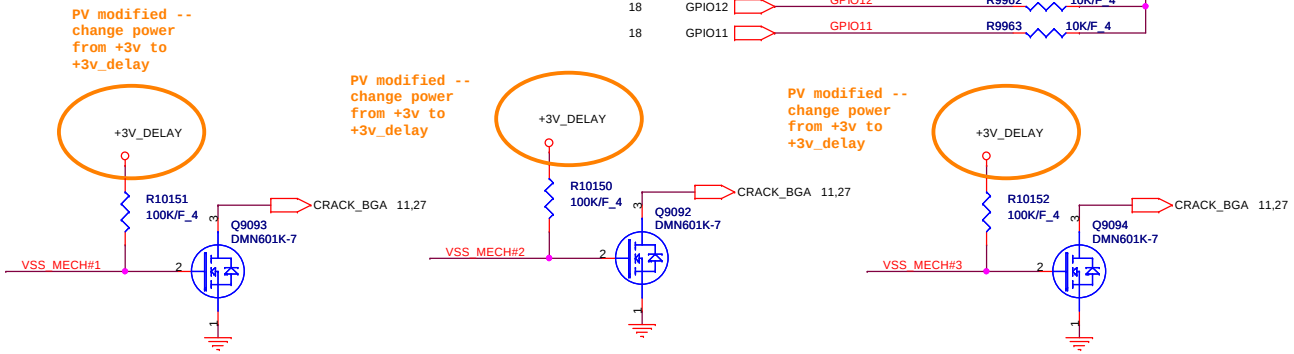
PROJECT :	SX6
Quanta Computer Inc.	
Size: Custom	Document Number: Park_Main
Rev: 2B	
Date: Tuesday, December 15, 2009	Sheet 18 of 43

NB5/RD2









Pin Straps description

Strap Name			Default Value
TX_PWRS_ENB	GPIO0	PCI Express Full TX Output Swing 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0 0 0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	1
AUD[0] AUD(1)	VSYNC HSYNC	AUD[1] AUD[0] 00 No Audio function 01 Audio for DisplayPort and HDMI if dongle is detected 10 Audio for DisplayPort only 11 Audio for both DisplayPort and HDMI	1 1
VIP_DEVICE_STRAP_ENA	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
RSVD	GENERICC		0

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

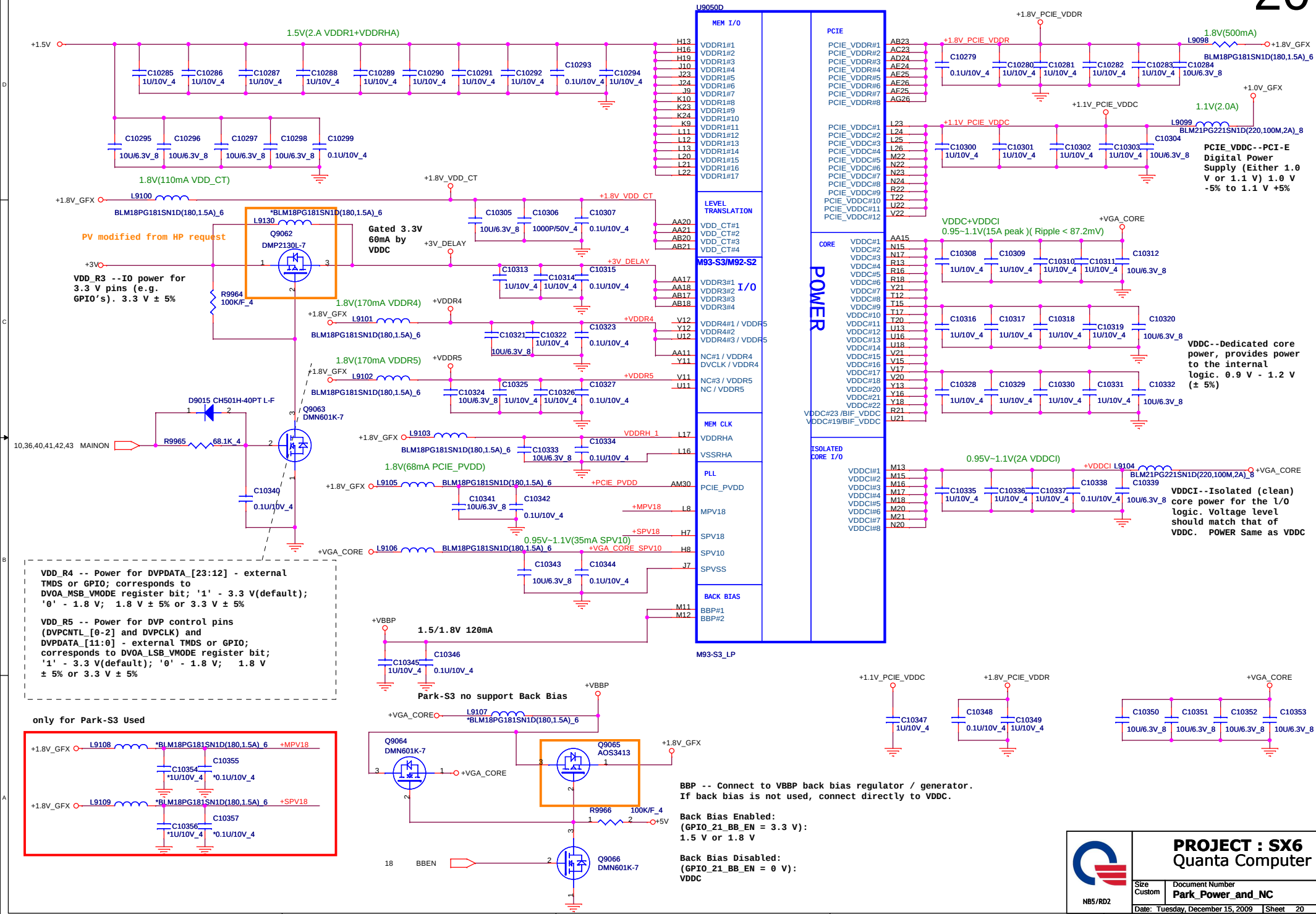
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

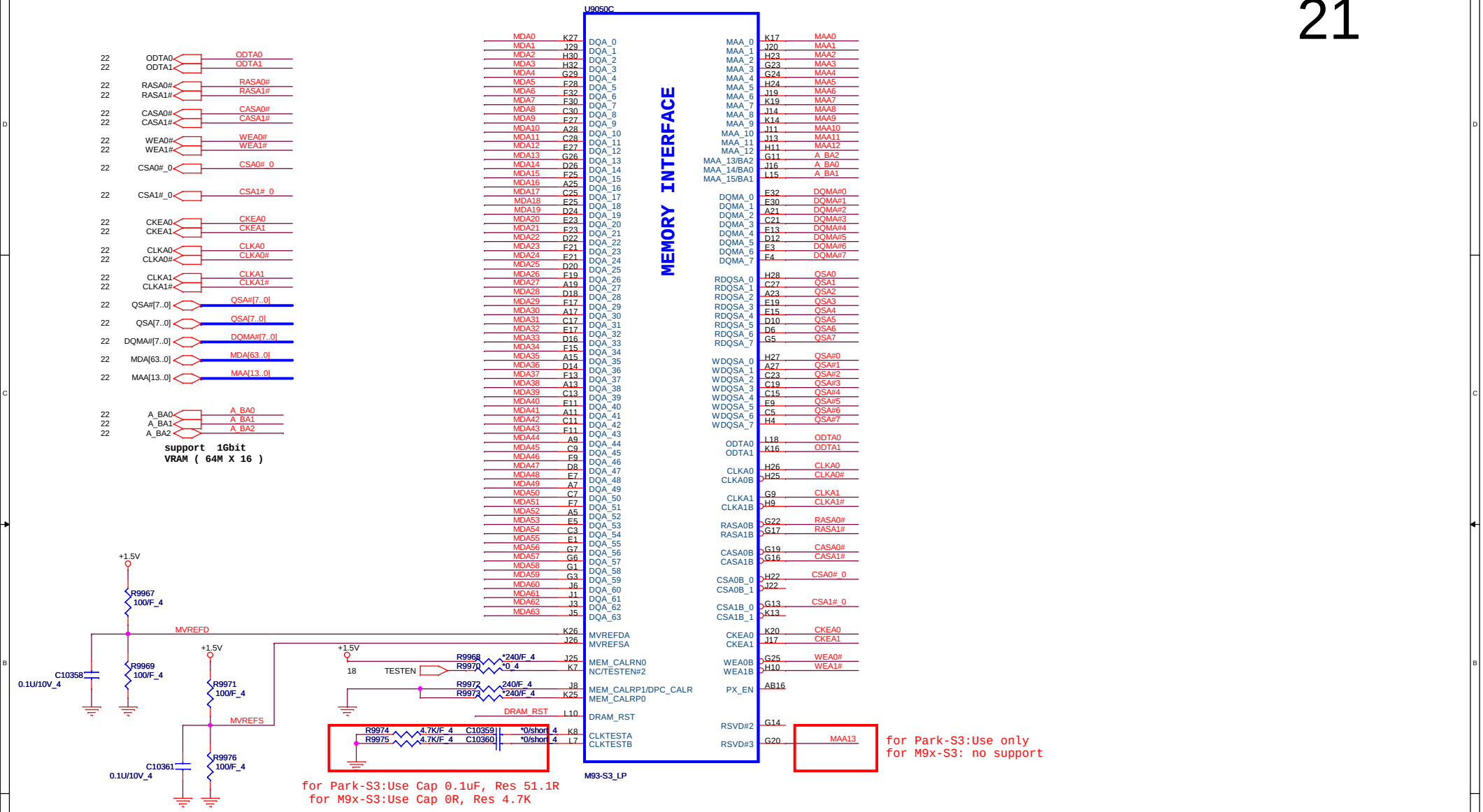
PROJECT : SX6
Quanta Computer Inc.

NB5/RD2

Size	Document Number	Rev
Custom	Park_GND / LVDS/ Straps	2B
Date: Tuesday, December 15, 2009	Sheet 19 of 43	

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%



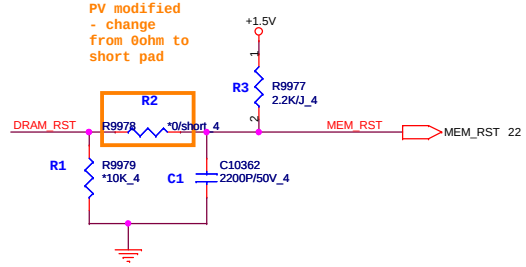


	M9x-S2/S3	Park-S3
MEM_CALRN0(J25) MEM_CALRP0(K25)	NC	240R
MEM_CALRP1(J8)	240R	150R
TESTEN2#2(K7)	NC	0R
R1	NC	10K
R2	0R	680R
R3	2.2K	NC
C1	2.2nF	68pF

240R:CS12402FB03
150R:CS11502FB21

0R:CS00002JB38
680R:CS16802JB27

2.2nF:CH22206KB16
68pF:CH06806JB01



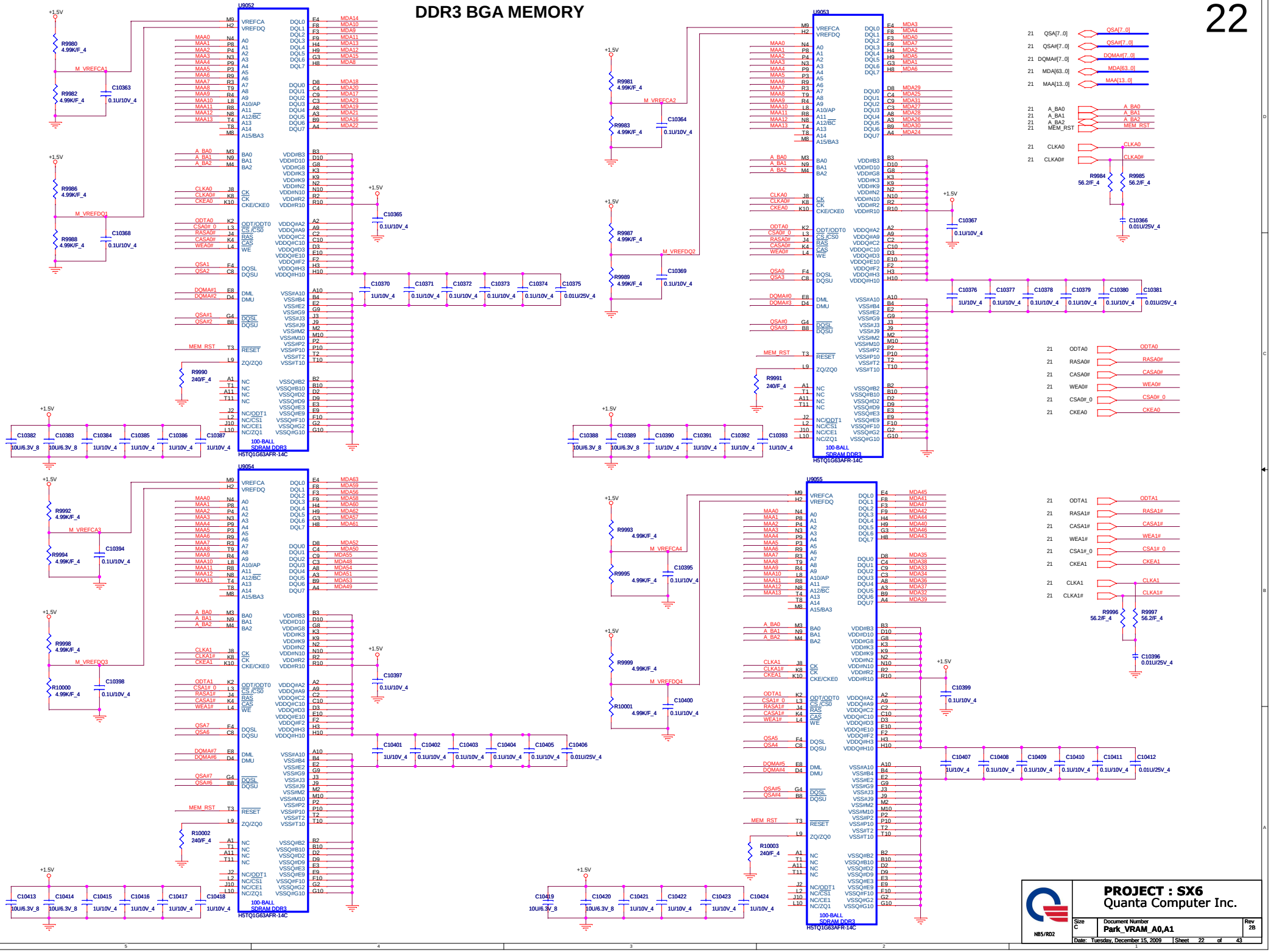
NB5/RD2

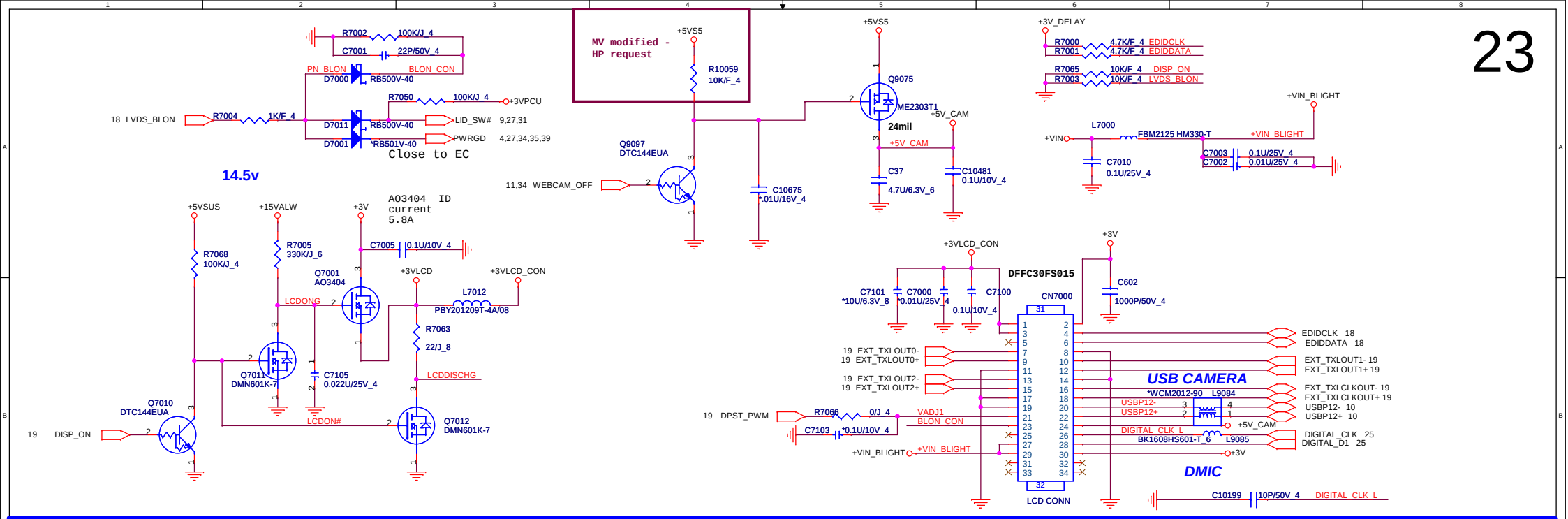
PROJECT : SX6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Park_MEM_Interface	2B

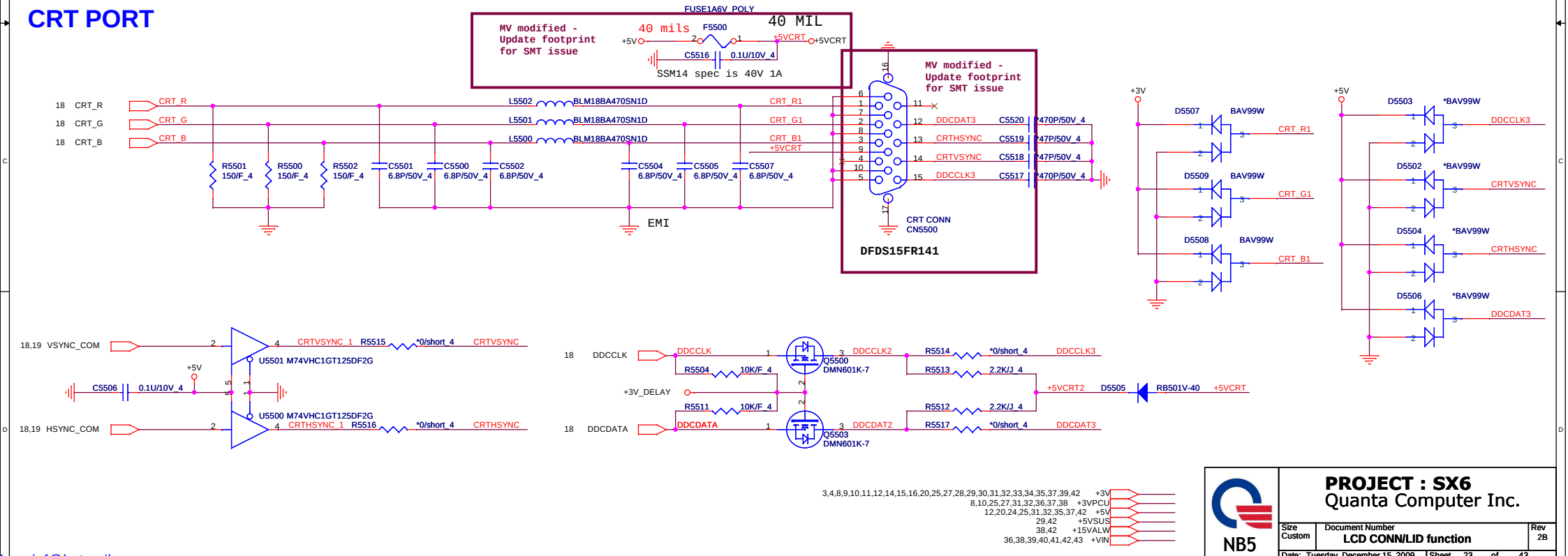
Date: Tuesday, December 15, 2009 | Sheet 21 of 43

DDR3 BGA MEMORY



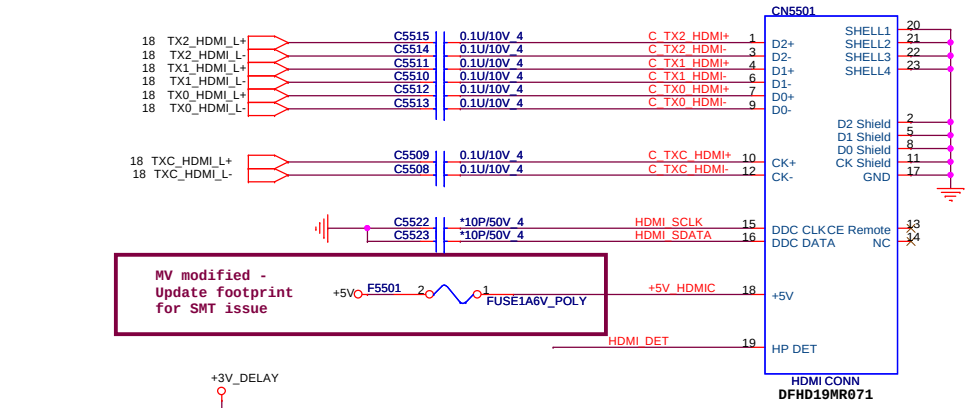


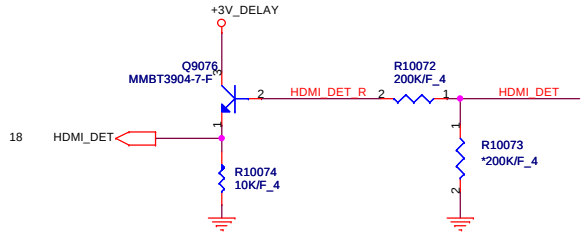
CRT PORT

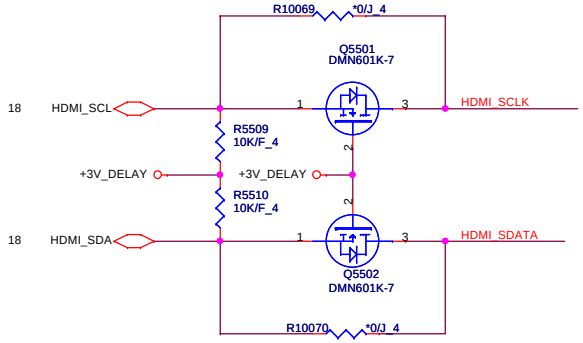


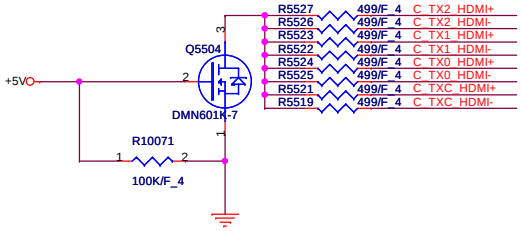
NB5	**PROJECT : SX6** Quanta Computer Inc.	
Size: Custom	Document Number: **LCD CONN/LID function**	Rev: 2B
Date: Tuesday, December 15, 2009	Sheet 23 of 43	

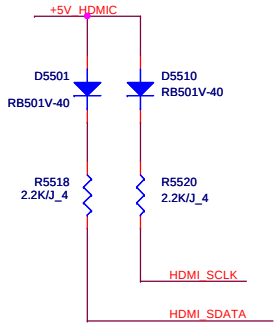
HDMI PORT











3,4,8,9,10,11,12,14,15,16,20,23,25,27,28,29,30,31,32,33,34,35,37,39,42 +3V

12,20,23,25,31,32,35,37,42 +5V

NB5

PROJECT : SX6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI Conn	2B
Date: Tuesday, December 15, 2009	Sheet 24 of 43	

PORT	PLACE TO
MONO_OUT	X
PORT A	External MIC
PORT B	HP OUT
PORT C	Internal MIC
PORT D	Internal Speckers

Close to CODEC

ALL CAPS CONNECTED TO THE 92HD80Bx
SHOULD BE X7R OR X5R--NO Y5V

Close to CODEC

>40mils trace

U9026

Digital

Analog

92HD80B1

HDA Bus

IDT recommand

SENSE_A -->EXT MIC/Headphone out

TO External MIC Jack

TO Headphone Jack

TO External Speaker

PV modified --- for EMI

PV modified
-Add diodefor
leakage issue

TO Digital MIC

IDT 92HD80 EAPD LOW--mute
HI--enable AMP

PV modified - Hp
request to add

MV modified -
ESD issue

FOR EMI

RESERVE

3,4,8,9,10,11,12,14,15,16,20,23,27,28,29,30,31,32,33,34,35,37,39,42 +3V
12,20,23,24,31,32,35,37,42 +5V

NB5

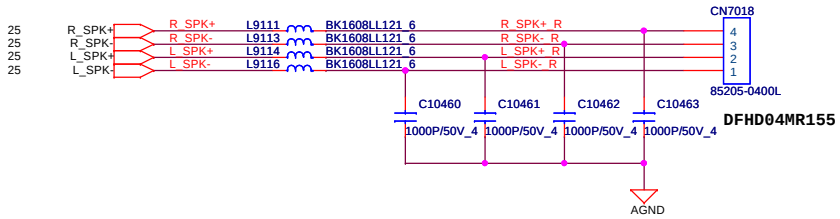
PROJECT : SX6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	IDT92HD80	2B

Date: Thursday, December 17, 2009 | Sheet 25 of 43

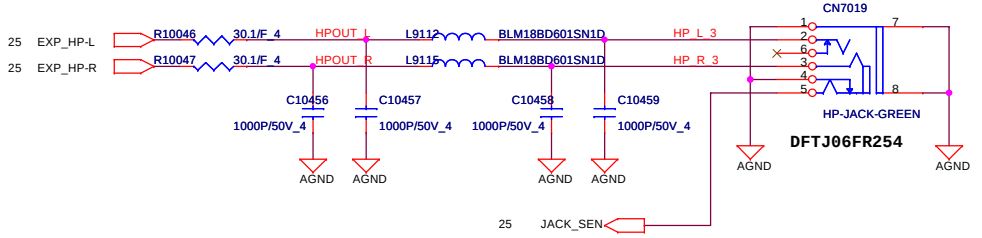
Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

INT. SPEAKER



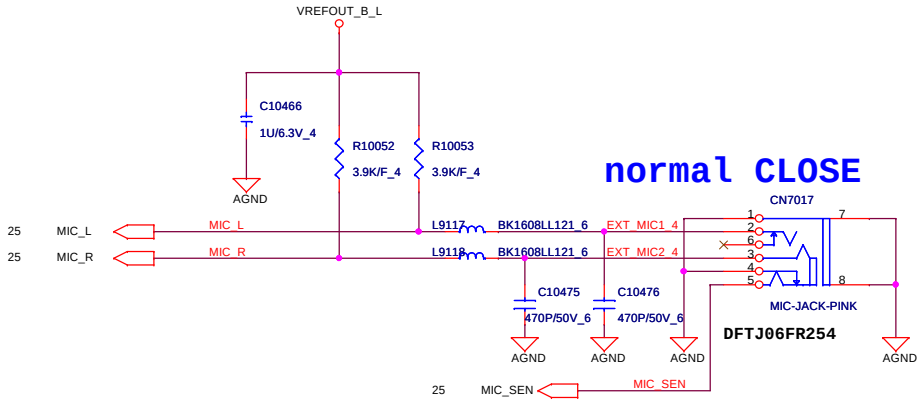
Headphone Jack

normal CLOSE



EXT Mic Jack

normal CLOSE



Note: MIC_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

NB5	PROJECT : SX6 Quanta Computer Inc.	
Size: Custom	Document Number: HP/MIC/SPK	Rev: 2B
Date: Tuesday, December 15, 2009	Sheet 26 of 43	

MV modified -
Remove for MV

CN7016

For debug(BIOS)

PV modified -
add 10uF

PV modified -
change from 0ohm
to short pad

PV modified -
change from 0ohm
to short pad

PV modified -
remove R10201for S5
power leakage issue

PV modified -
change from 0ohm
to short pad

PV modified -
change from 0ohm
to short pad

PV modified -
change from 0ohm
to short pad

PV modified -
change from 0ohm
to short pad

PV modified -
change from 1Kohm
to 200ohm

PV modified -
change from 0ohm
to short pad

PV modified -
change from 0ohm
to short pad

PV modified -
change from 0ohm
to short pad

PV modified from hp request

PV modified from hp request

PV modified -
change from 0ohm
to short pad

MB ID: 1=13"&14",
0=15&17.
for numeric keyboard

SMSC 1098

Keyboard/Mouse Interface

General Purpose I/O Interface

LPC Bus

to detect battery existance

Debounced AC
present output
signal from KBC
to system BIOS

To BAT SMBUS

GFX_SEL : PU-UMA , PD-DIS

TQFP128-16X16-4

4M byte SPI ROM for PCH ME & BIOS

MX25L6405DZN1-12G

MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00
Socket: DG008000031

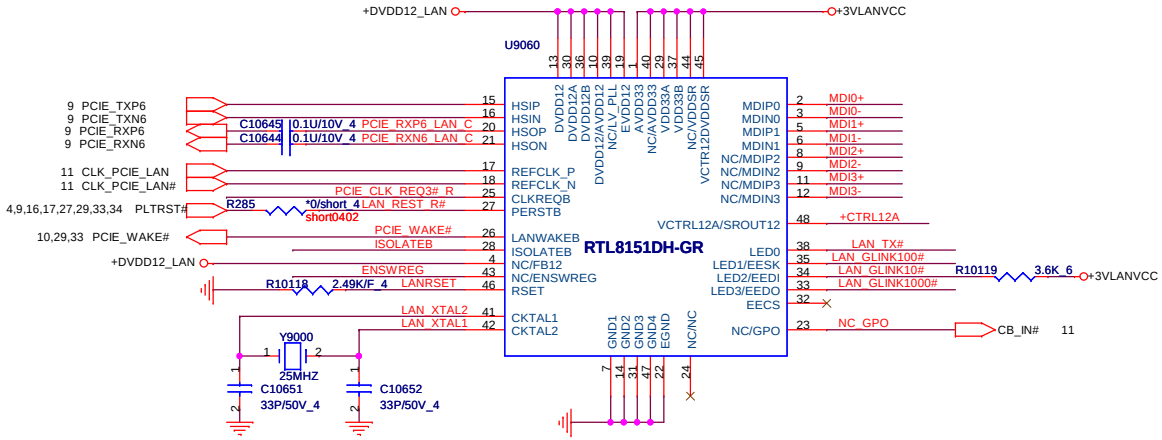
PROJECT : SX6
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	SMSC 1098	2B

Date: Tuesday, December 15, 2009 Sheet 27 of 43

3,4,8,9,10,11,12,14,15,16,20,23,25,27,29,30,31,32,33,34,35,37,39,42 +3V
42 +3VLANVCC



RTL8151DH-GR

+3VLANVCC

Close to PIN 1	C10482 .1U/10V_4
Close to PIN 29,37,40	C10483 .1U/10V_4 C10484 .1U/10V_4 C10485 .1U/10V_4
close Pin 44,45	C10486 .1U/10V_4 C10527 *10U/6.3V_8 C10534 22U/6.3V/X5R_8

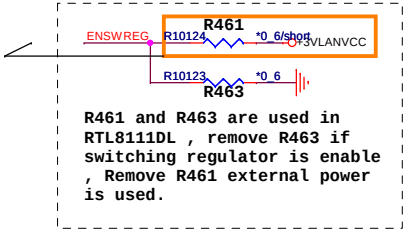
>200mil

+DVDD12_LAN

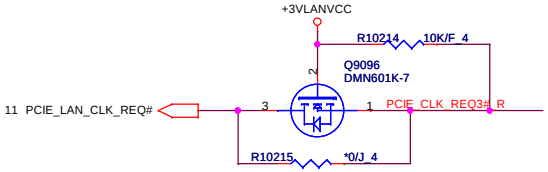
+CTRL12A L9131 L8 4.7UH,+-20%,650MA_1210 >200mil

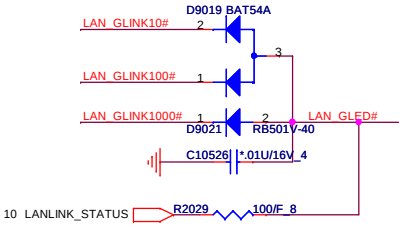
Close to 8111DL DVDD12 pins-- 19	C10531 22U/6.3V/X5R_8 C10530 .1U/10V_4 C10536 1U/6.3V_4 C10528 1U/6.3V_4
Close to 8111DL DVDD12 pins--10,13,30,36,39.	C10529 .1U/10V_4 C10532 .1U/10V_4 C10535 .1U/10V_4 C10533 .1U/10V_4

PV modified
- change
from 0ohm to
short pad

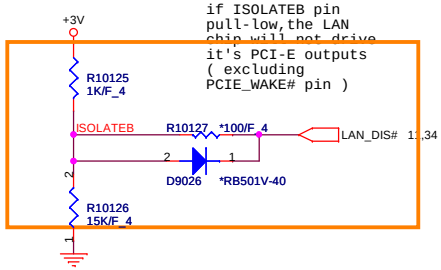


R461 and R463 are used in RTL8111DL , remove R463 if switching regulator is enable , Remove R461 external power is used.



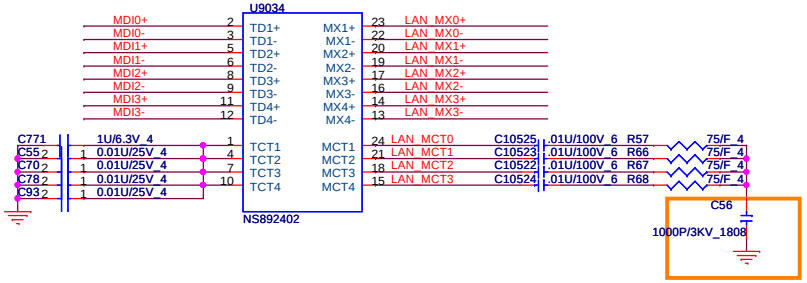


PV modified



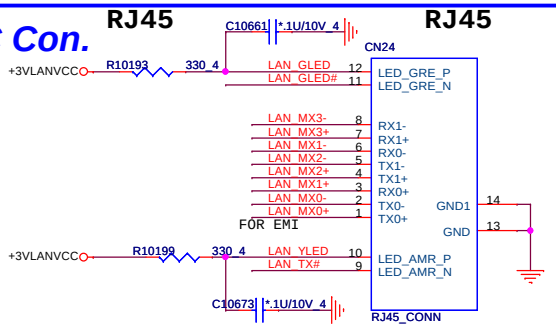
if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

Transformer for 10/100/1000



PV modified footprint

Lan and MDC Con.



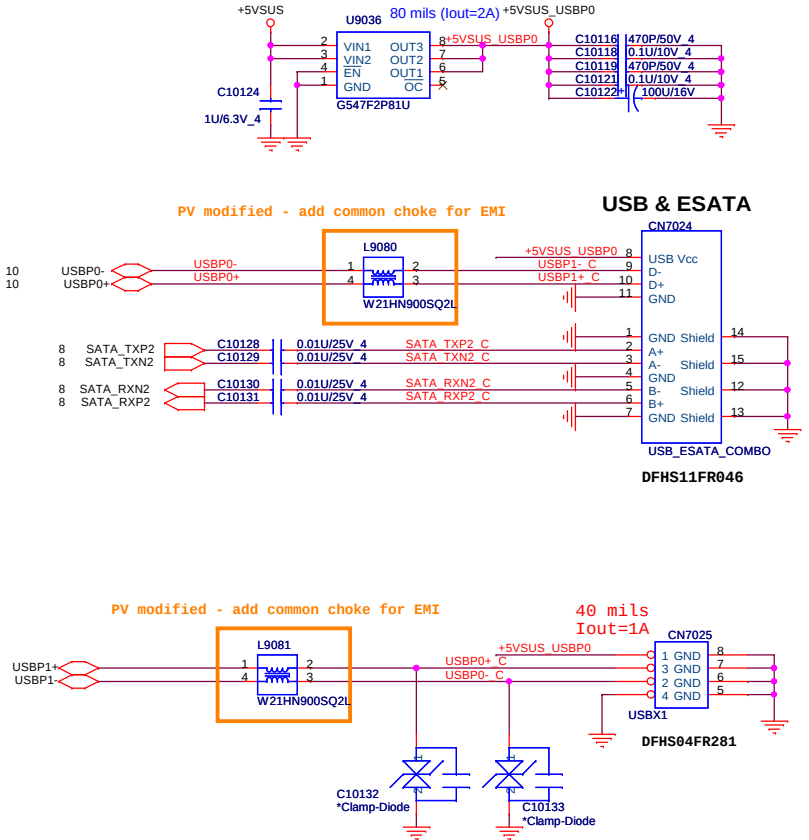
NB5

PROJECT : SX6
Quanta Computer Inc.

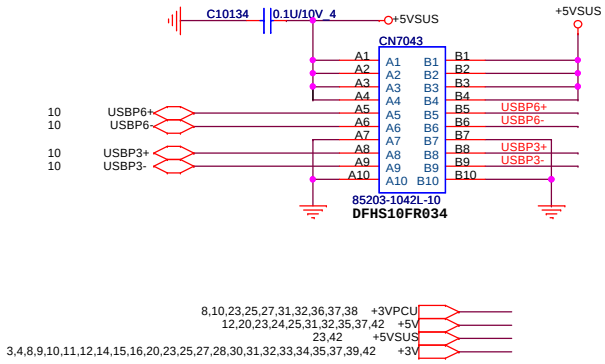
Size	Document Number	Rev
Custom	RTL8151DH-GR	2B

Date: Friday, December 18, 2009 Sheet 28 of 43

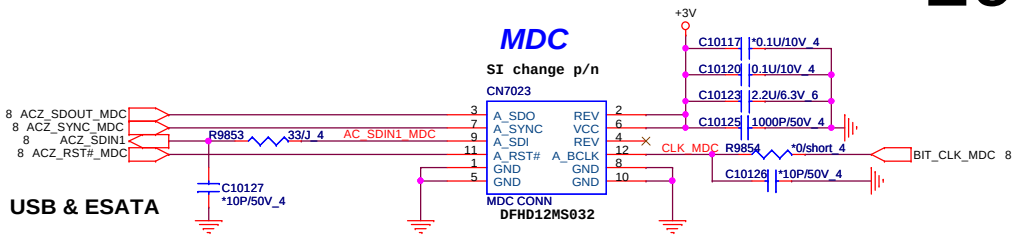
LEFT SIDE USBX1 and E-SATA/USB COMBO

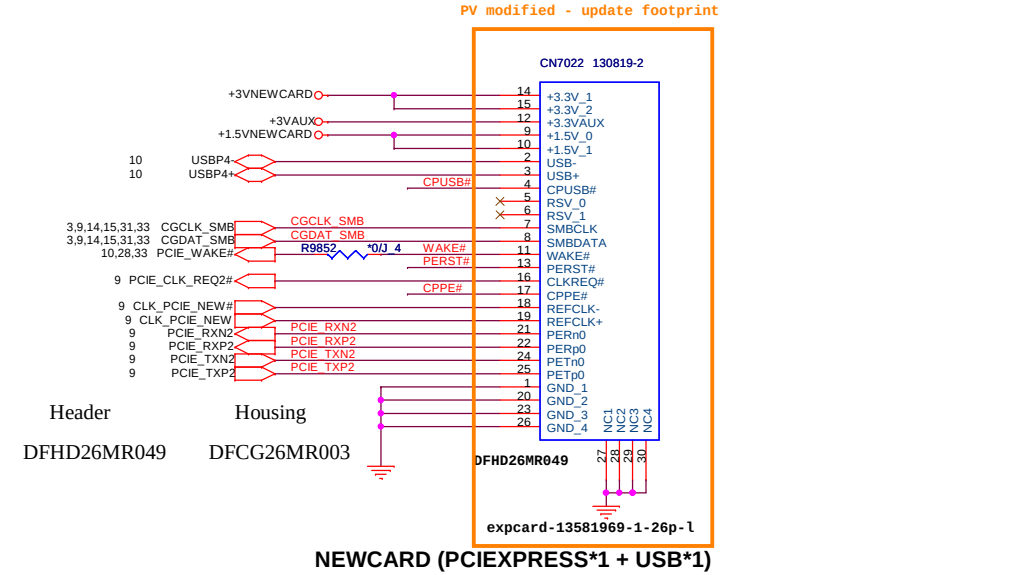


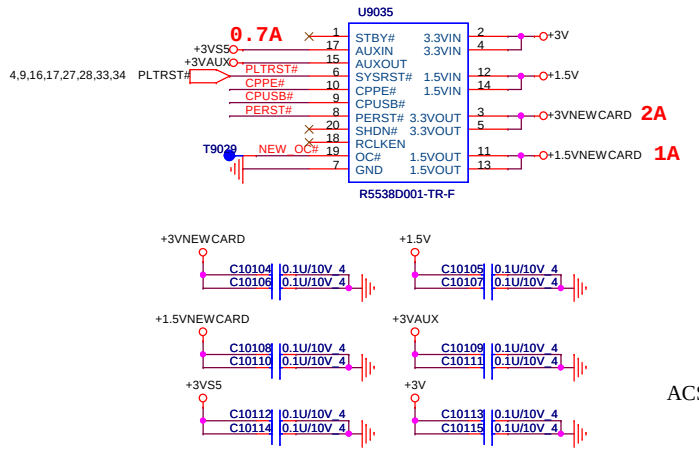
RIGHT SIDE USBX2



Modem CONN







ACS

NB5	PROJECT : SX6 Quanta Computer Inc.		
	Size: Custom	Document Number: EXTERNAL USB X2	Rev: 2B
	Date: Wednesday, December 16, 2009	Sheet 29 of 43	

3,4,8,9,10,11,12,14,15,16,20,23,25,27,28,29,31,32,33,34,35,37,39,42 +3V

Note:

	SD/MMC 4.2	MS	XD
SP0			
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7/MMC_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6/MMC_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5/MMC_DAT5		XD_D0
SP13	SD_DAT4/MMC_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

XTAL control pin for 12Mhz crystal or 48Mhz clk in

+3VSUS_RTS R717 *0/short_4

U56

XTAL_CTR GPIO0 EEDO EECS EESK EEDI XD_CD# SD_WP SD_CD# MS_D4 SD_DAT1/XD_D4 MS_D5 RREF DM DP 12MHZ_XTLO 12MHZ_XTLI MODE_SEL RST#

XD_CD# SP2 SD_CD# SP4

R727 6.19K/F_4 RREF

10 USBP2- R724 *0/short_4 DM
10 USBP2+ R722 *0/short_4 DP

9 CLK_48M_CR CLK_48M_CR

C949 *5.6P/50V_4 CLK_48M_CR
R728 *270K_4
*12MHz Y10
C952 *5.6P/50V_4 XTLI_CARD
reserve

MODE_SEL R731 *0/J_4

+3VSUS_RTS R729 *100K/F_4 5158_RST#
C950 1U/6.3V_4
Internal have pull Hi 200K

XD_CLE XD_CE# XD_ALE SD_DAT2/XD_RE# SD_DAT3/XD_WE# XD_RDY SD_DAT4/XD_WP#/MS_D7 SD_CMD SD_DAT5/XD_D0/MS_D6 SD_CLK/XD_D1/MS_CLK SD_DAT6/XD_D7/MS_D3 NC MS_INS# SD_DAT7/XD_D2/MS_D2 SD_DAT0/XD_D6/MS_D0 XD_D3/MS_D1 XD_D5/MS_BS AV_PLL_IN VREG_OUT 5V_IN NC D3V3_IN D3V3_IN NC CARD_3V3_OUT AG33 AG_PLL DGND2 DGND1

SP19 SP18 SP17 SP16 SP15 SP14 SP13 SD_CMD_R SP12 SP11 SP10 MS_CD# SP8 SP7 SP6 SP5

Realtek RTS5159

SP4 R732 *0/short_4 SD_DAT1
SD_CLK_MS_CLK R725 *0/short_4 SP11

Close to Chipset
SP11 C945 *270P/25V_4

C946 0.1U/10V_4 Vreg out 1.8V from Internal 3.3VLDO C926 1U/6.3V_4

PV modified - change from 0ohm to short pad

+3VSUS_RTS R718 *0_6/short +3V
Without memory card 43mA
suspend current 350uA

C936 0.1U/10V_4 C942 4.7U/6.3V_6

0.1U/10V_4 C941
+3VSUS_RTS
0.1U/10V_4 C947 C948 *4.7U/6.3V_6

+3VCARD
C931 1U/6.3V_4

+3VCARD
C928 *.1U/10V_4 C927 *.1U/10V_4 C930 *.1U/10V_4

RTS5159 max output current for ..
XD card 250mA
SD/MMC 250mA
MS/MSPRO 250mA

+3VCARD C955 2.2U/6.3V_6 R735 150K/F_4

+3VCARD C957 0.1U/10V_4 C958 0.1U/10V_4 C956 0.1U/10V_4

XD,MMC 4.2/SD,MS/MSP 7 IN1 CARD READER

CN42

SD C/D SD W/P xD-VCC xD-DATA7 xD-DATA6 xD-DATA5 xD-DATA4 xD-DATA3 xD-DATA2 xD-DATA1 GND SD-DATA1 MS-BS SD-DATA0 MS-DATA1 MMC-DATA7 MS-DATA0 MMC-DATA6 MS-DATA2 SD-CLK SD-VCC MS-INS

GND GND XD-CD XD-R/B XD-RE XD-CE XD-CLE XD-ALE xD-WE xD-WP XD-DATA0 GND SD-DATA2 SD-DATA3 MS-VCC MMC-DATA4 MS-SCLK SD-CMD MS-DATA3 MMC-DATA5

SD_CD# SP2 +3VCARD SP10 SP7 SP5 SP4 SP6 SP8 SP11 SD_DAT1 SP5 SP7 SP6 SP8 SP7 SP10 SP8 SD_CLK_MS_CLK +3VCARD MS_CD#

XD_CD# SP14 SP16 SP18 SP19 SP17 SP15 XD-WP#_L SP12 SP16 SP15 +3VCARD SP13 SD_CLK_MS_CLK SD_CMD_R SP10 SP12

C10513 *270P/25V_4

+3VCARD R10111 *10K/F_4

R10112 *0_6/short SP13

PLASTREN CM7S-02 CARD READER SOCKET

DFHD42MR011

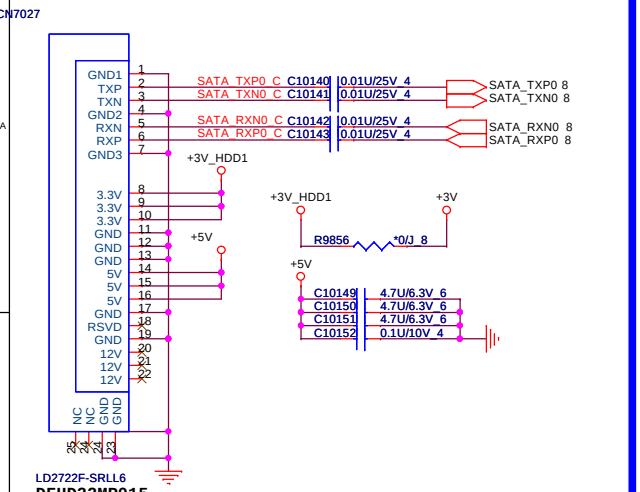
NB5

PROJECT : SX6
Quanta Computer Inc.

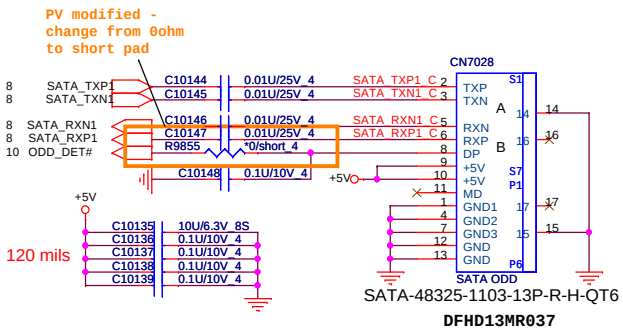
Size	Document Number	Rev
Custom	RTS5159 & CR SOCKET	2B

Date: Tuesday, December 15, 2009 Sheet 30 of 43

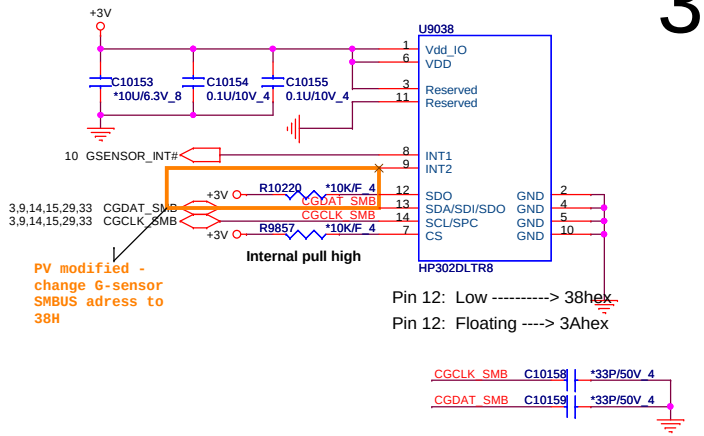
SATA HDD CONNECTOR



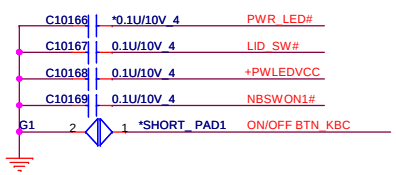
SATA CD-ROM



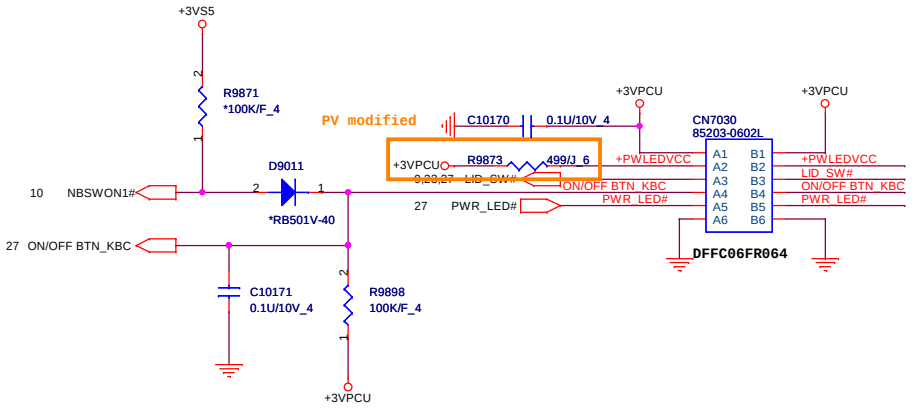
Accelerometer Sensor



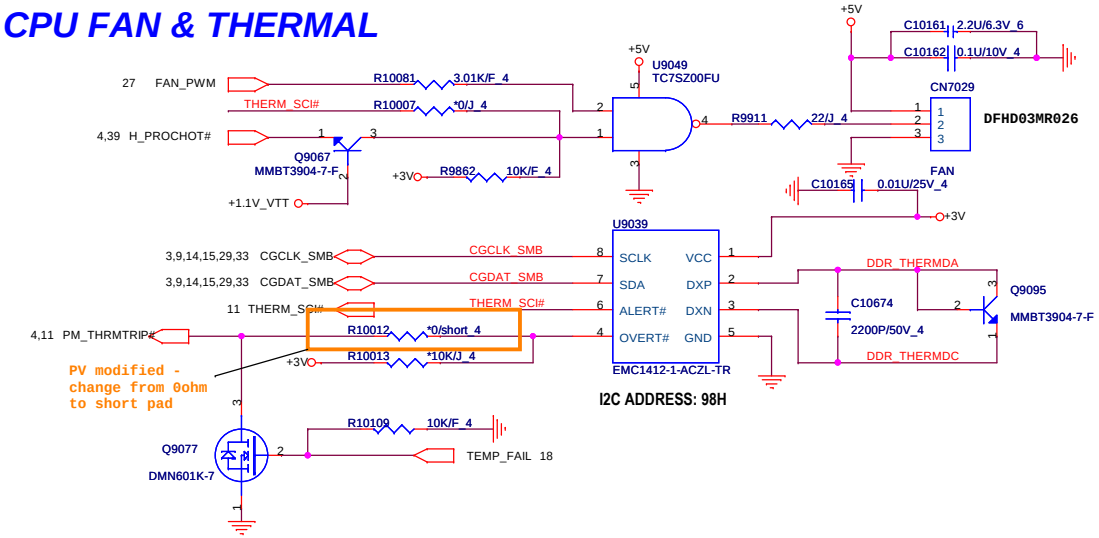
POWER BOTTON CONNECT



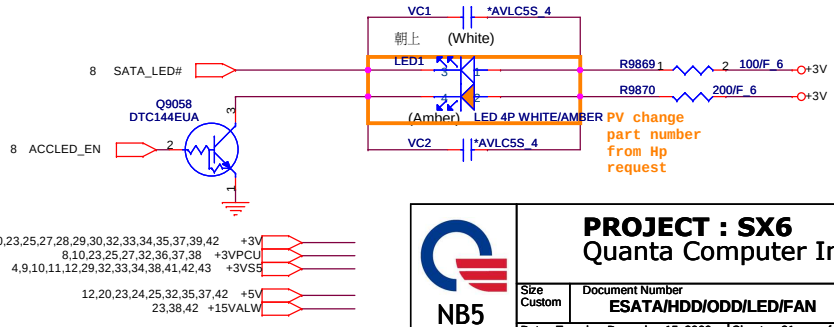
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND



CPU FAN & THERMAL



LED

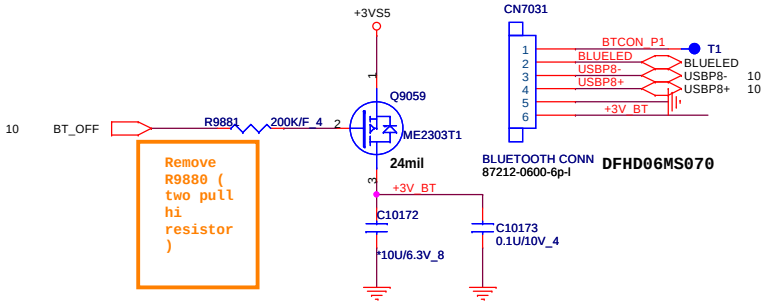


NB5

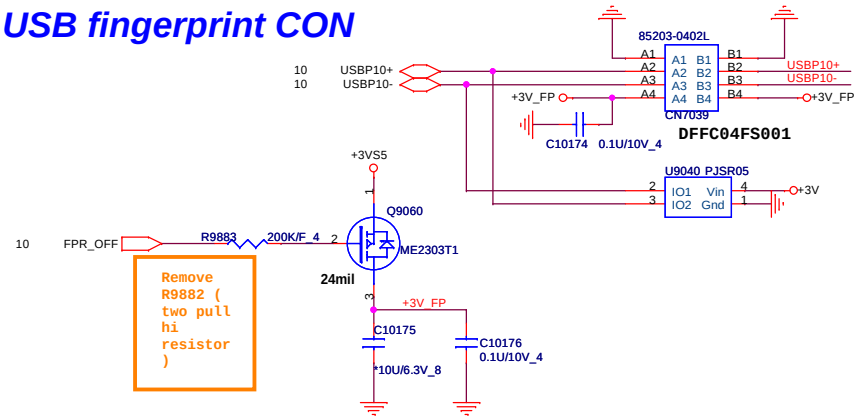
PROJECT : SX6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ESATA/HDD/ODD/LED/FAN	2B
Date: Tuesday, December 15, 2009	Sheet 31 of 43	

BLUETOOTH

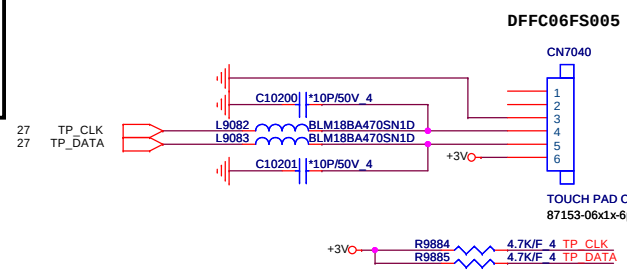


USB fingerprint CON

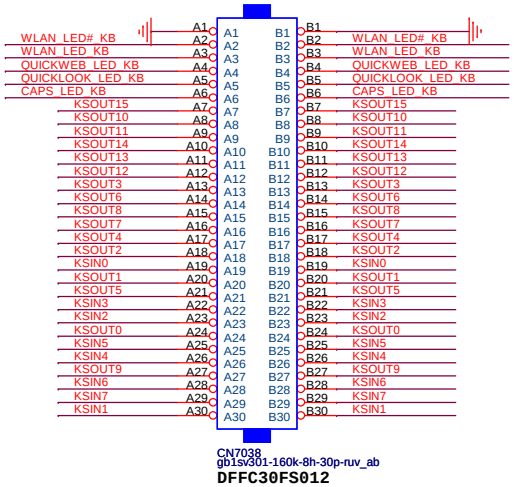


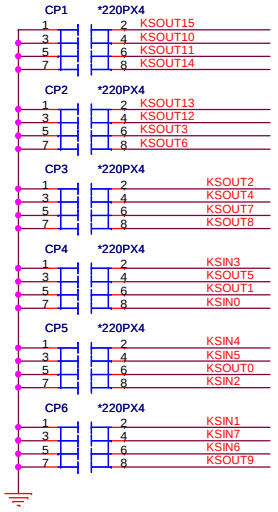
TOUCH PAD CONNECTOR

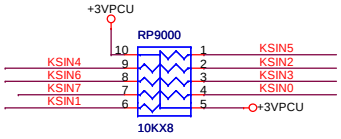
Pin1	VDD
Pin2	DATA
Pin3	CLK
Pin4	GND
Pin5	X
Pin6	X

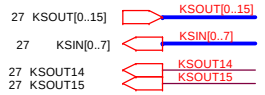


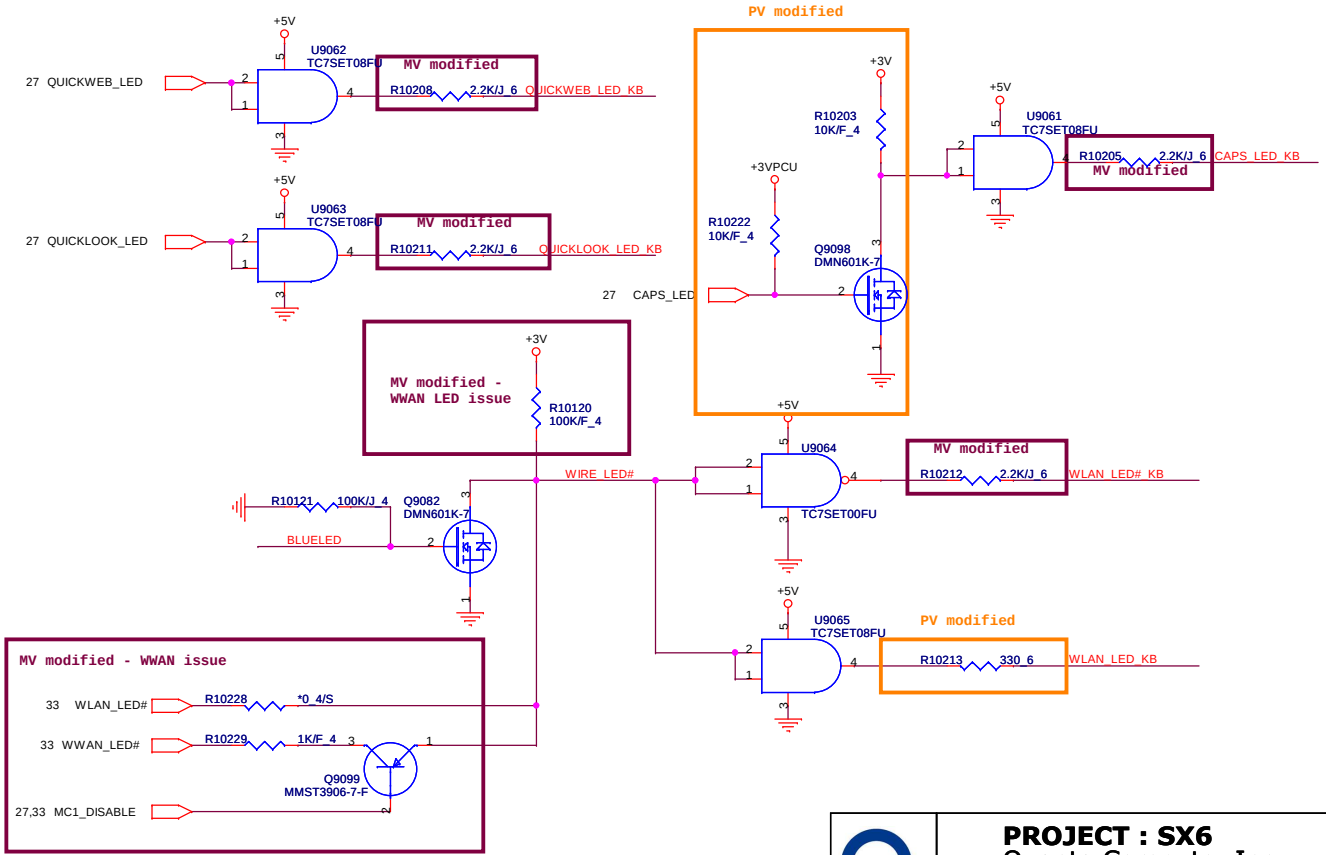
KEYBOARD CONNECTOR.











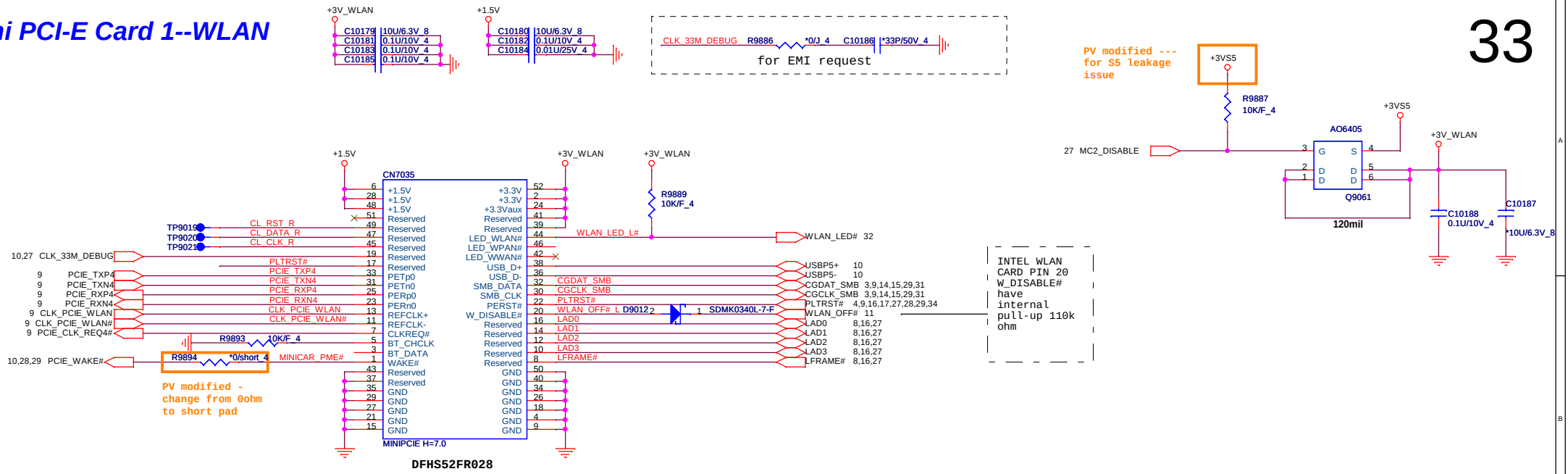
NB5

PROJECT : SX6
Quanta Computer Inc.

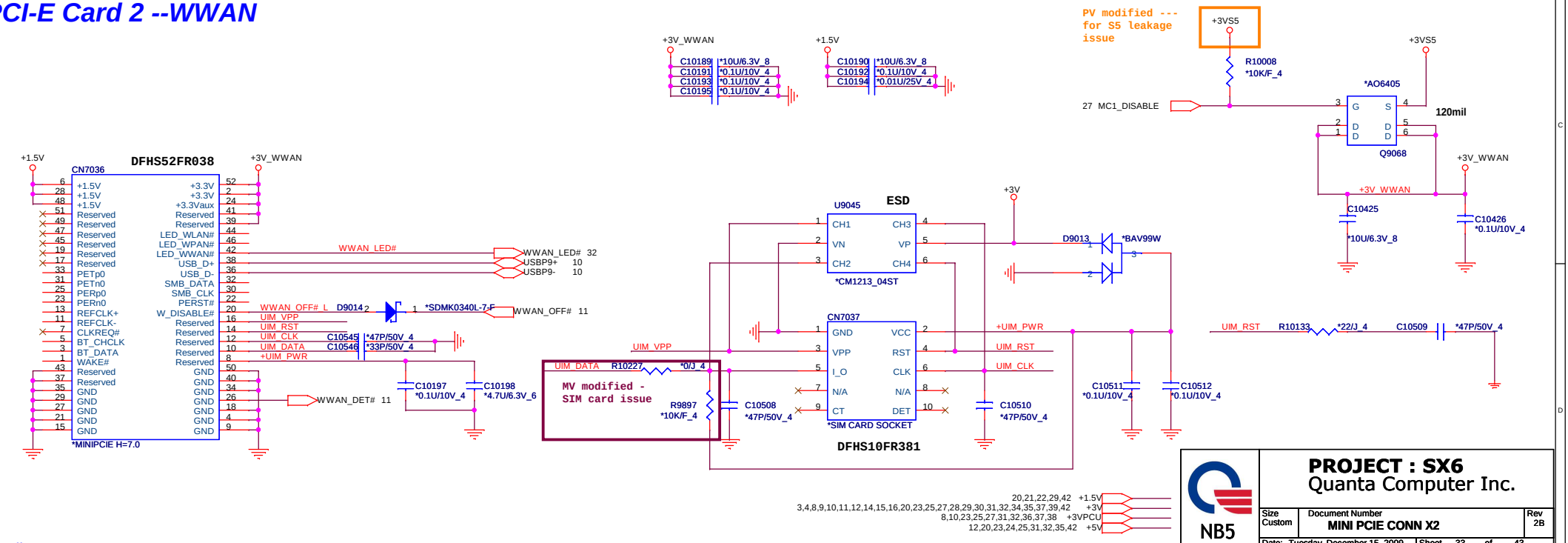
Size	Document Number	Rev
Custom	BT/WC/FT/ESATA/USB/LED	2B

Date: Thursday, December 17, 2009 | Sheet 32 of 43

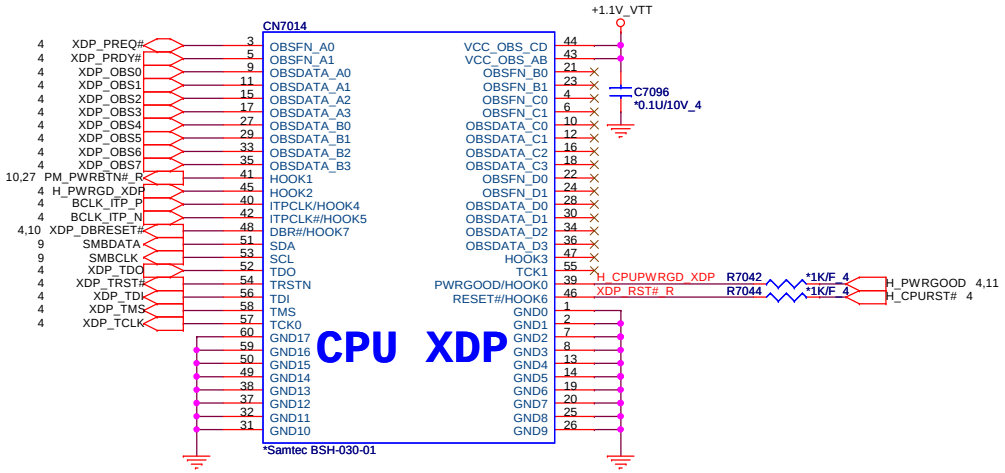
Mini PCI-E Card 1--WLAN



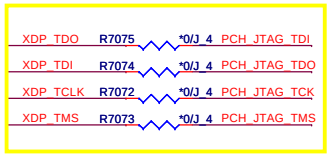
Mini PCI-E Card 2 --WWAN

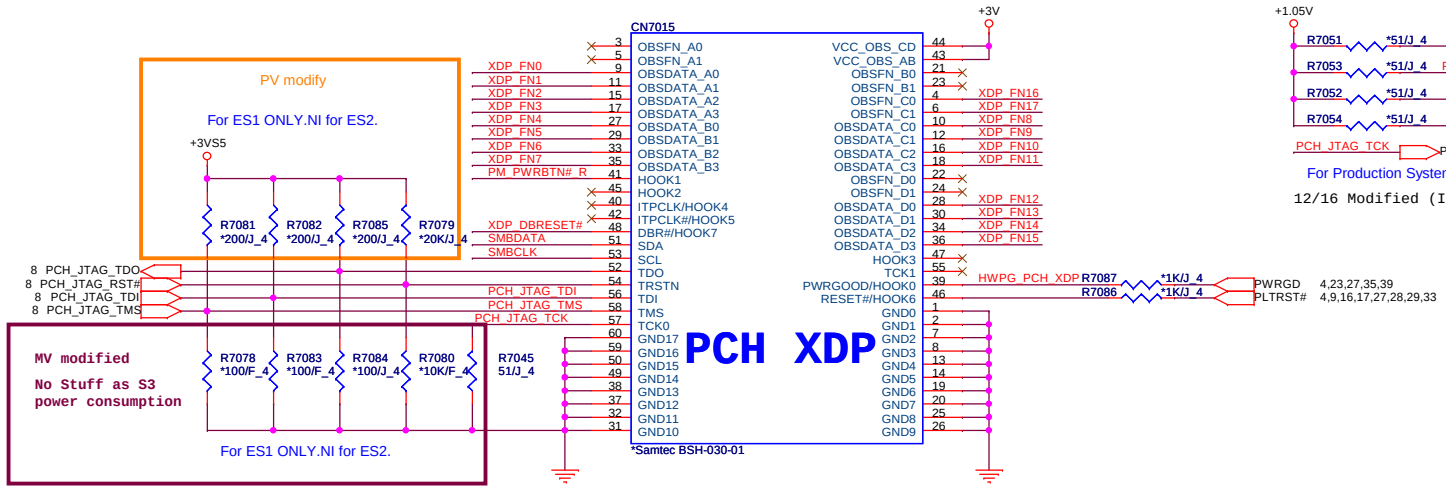


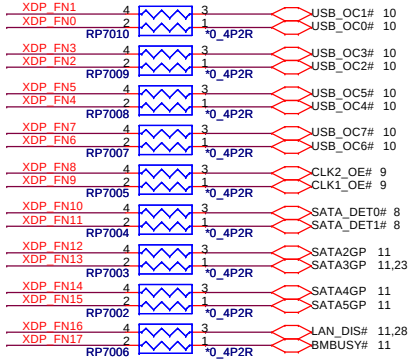
NB5	PROJECT : SX6 Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCIE CONN X2	Rev: 2B
Date: Tuesday, December 15, 2009	Sheet 33 of 43	



Reserve for BSDL

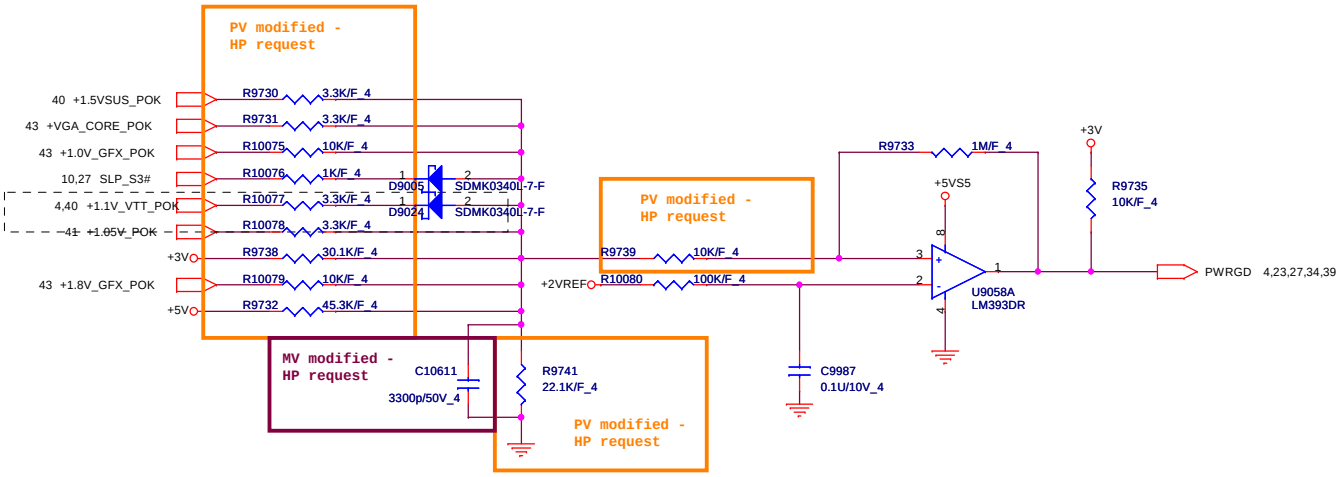






4,6,11,12,31,39,40 +1.1V_VTT
3,8,9,10,12,39,41 +1.05V
6,11,12,41,42 +1.8V
3,4,8,9,10,11,12,14,15,16,20,23,25,27,28,29,30,31,32,33,35,37,39,42 +3V
4,9,10,11,12,29,31,32,33,38,41,42,43 +3VS5

NB5	PROJECT : SX6 Quanta Computer Inc.	
Size: Custom	Document Number: XDP/BRAIDWOOD	Rev: 2B
Date: Tuesday, December 15, 2009	Sheet 34 of 43	



NB5	**PROJECT : SX6** Quanta Computer Inc.	
Size: Custom	Document Number: **POWER Sequance**	Rev: 2B
Date: Tuesday, December 15, 2009	Sheet 35 of 43	

DC-IN Connector

SI change P/N
DFWF08MS007

MP for HF

MP footprint modify for SMT

pv modified

To PWR LED

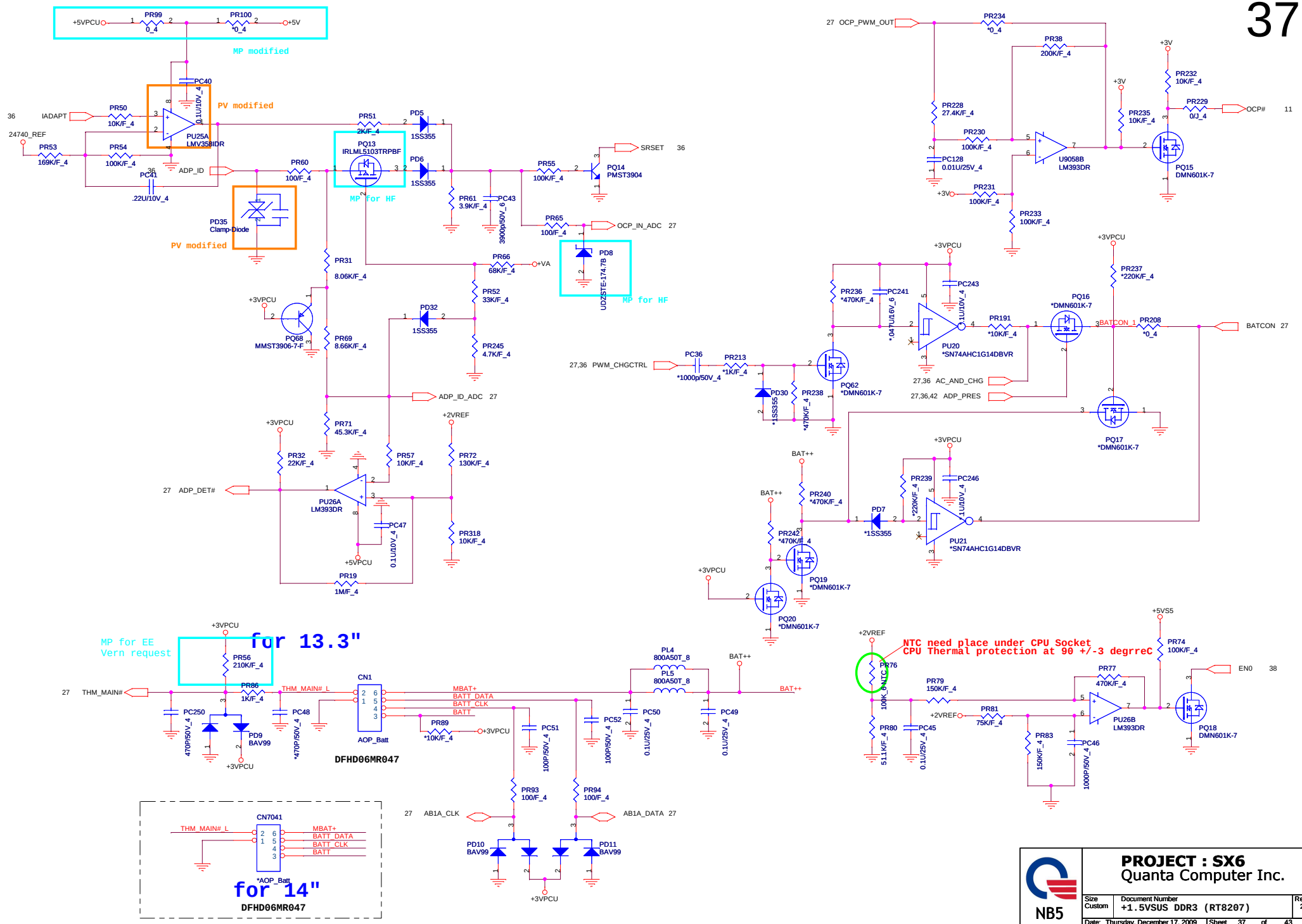
MP footprint modified for SMT

AC Detector
HI: 11.85V
Lo: 10.55V

Charge Detector
HI: 17.588V
Lo: 17.292V

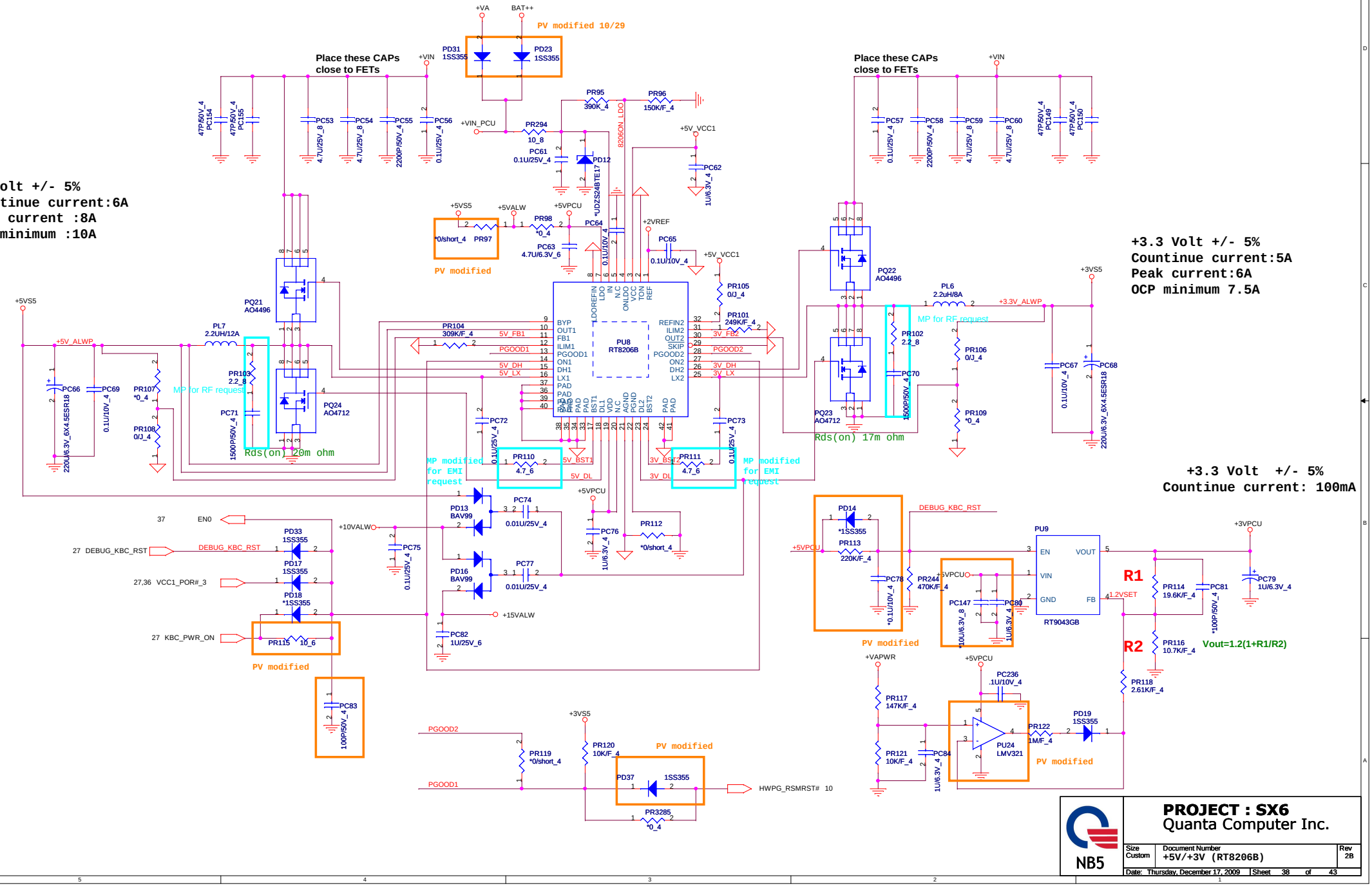
10/30 for shortage

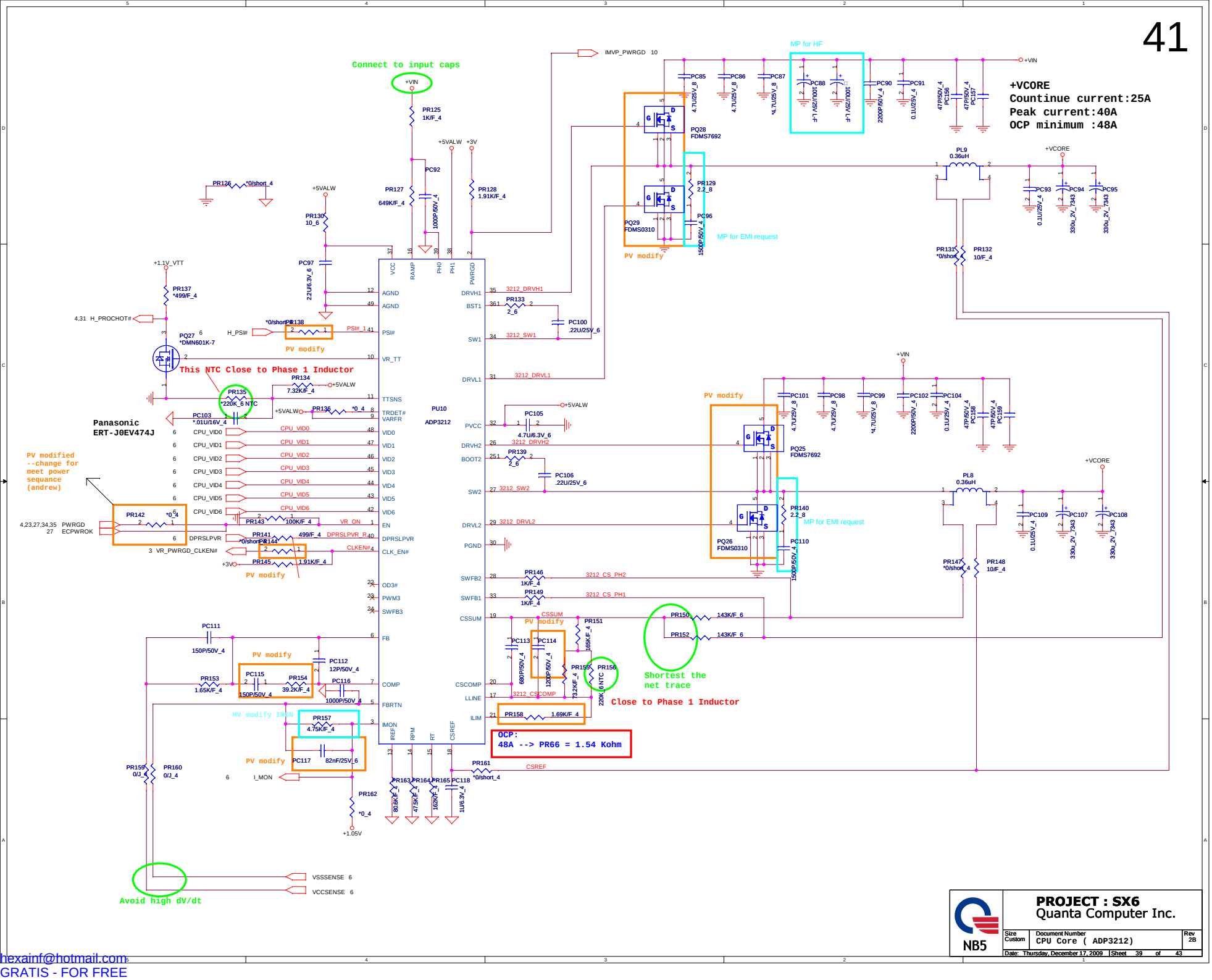
PU2
bq24740

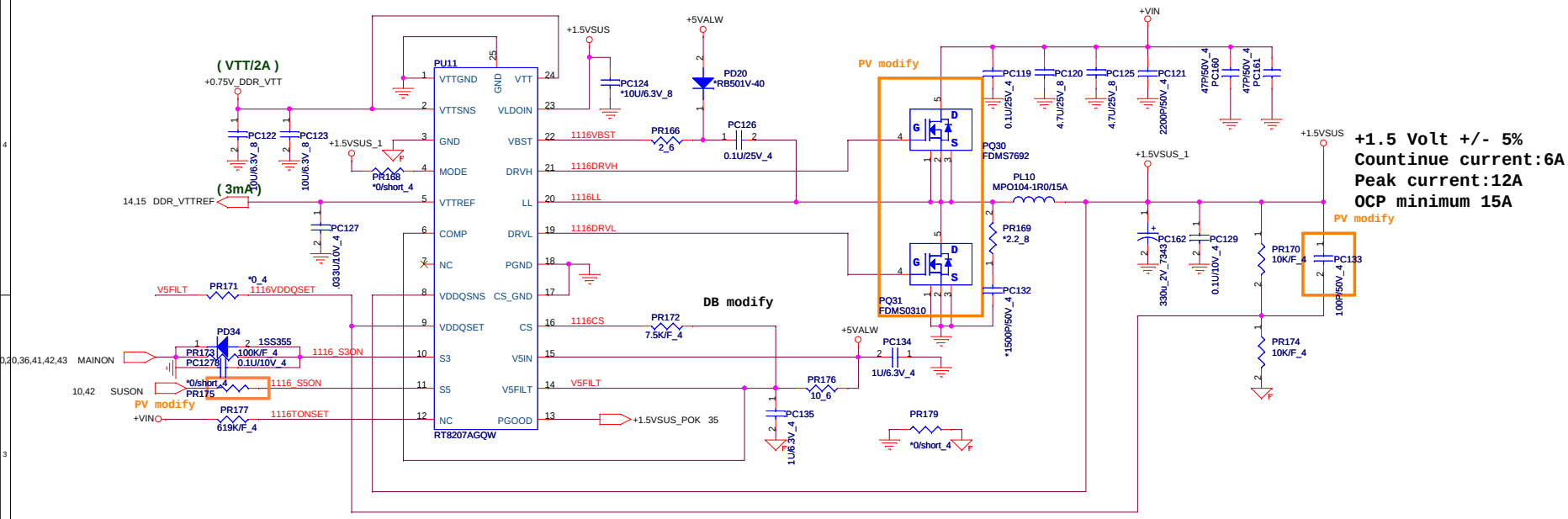


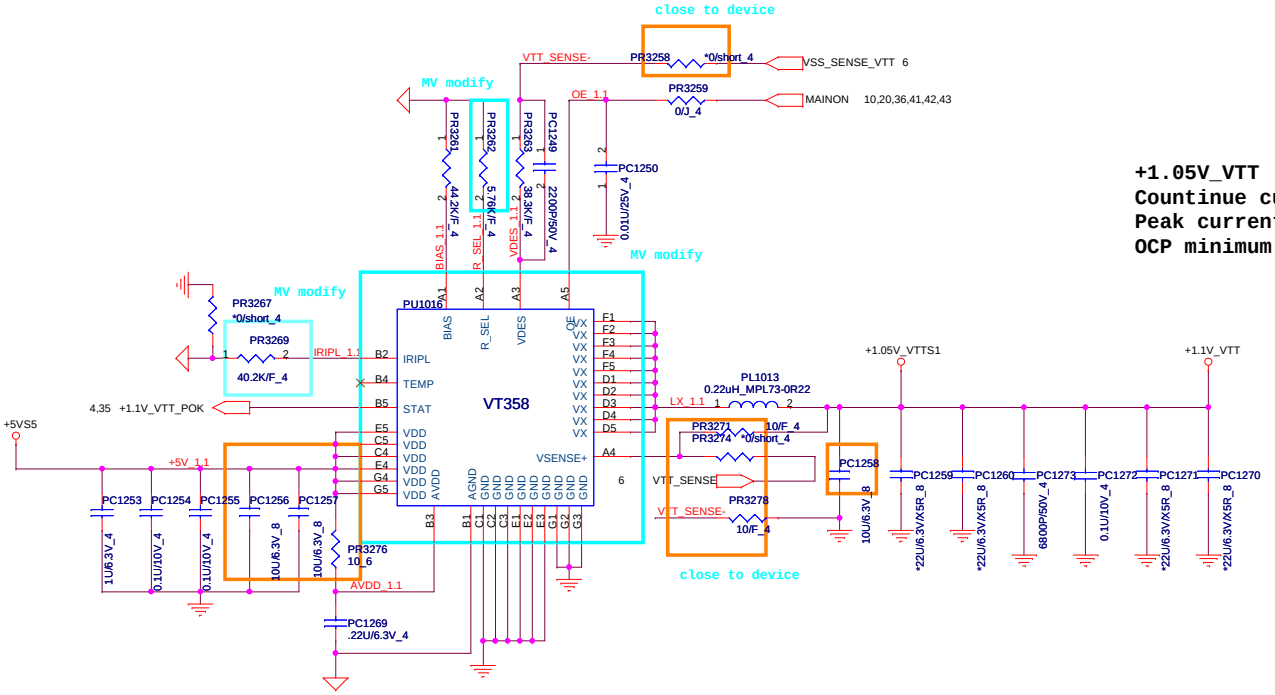
NB5	PROJECT : SX6 Quanta Computer Inc.		
	Size: Custom	Document Number: +1.5VSUS DDR3 (RT8207)	Rev: 2B
	Date: Thursday, December 17, 2009	Sheet 37 of 43	

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW







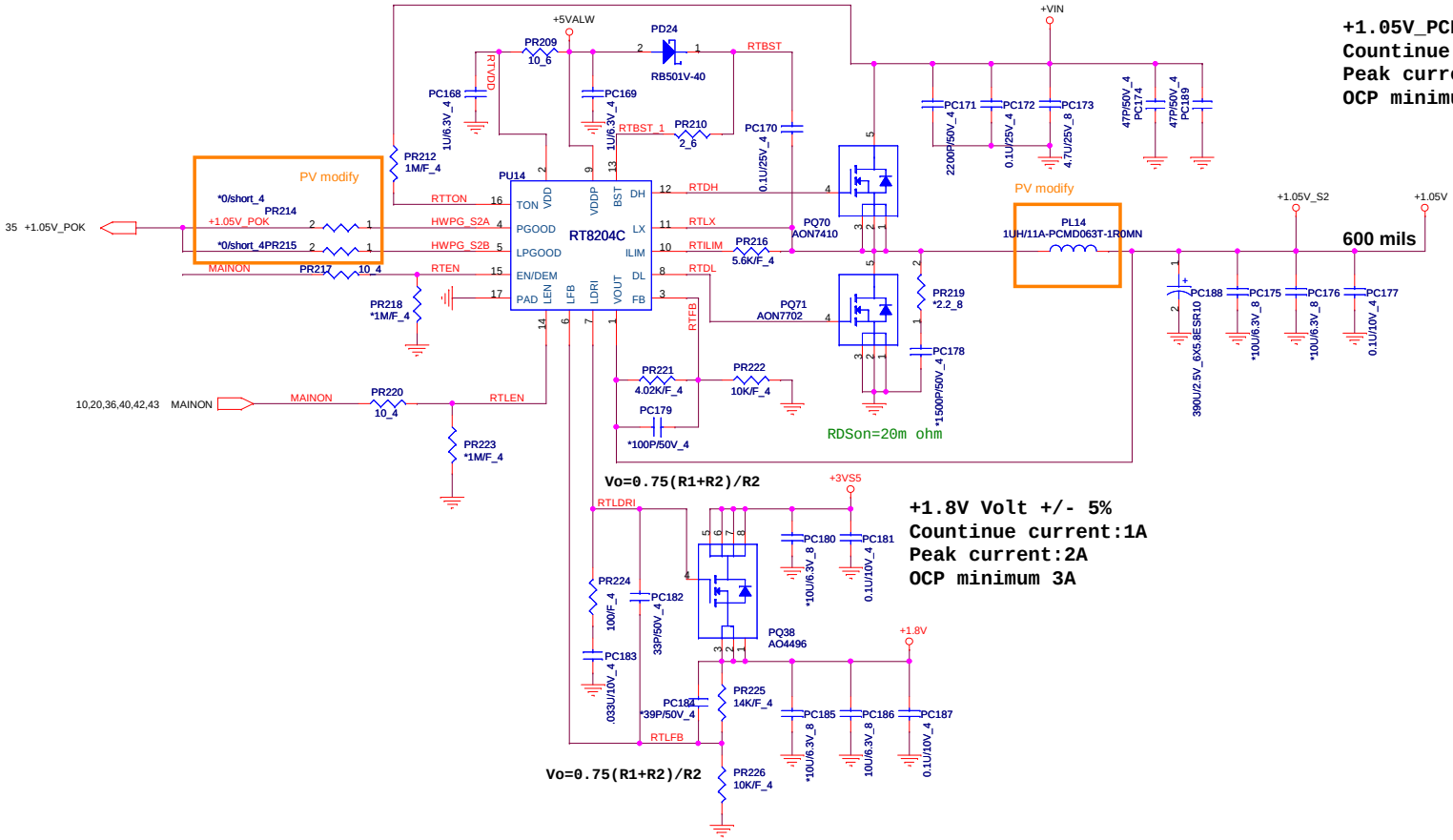


NB5

PROJECT : SX6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	2B

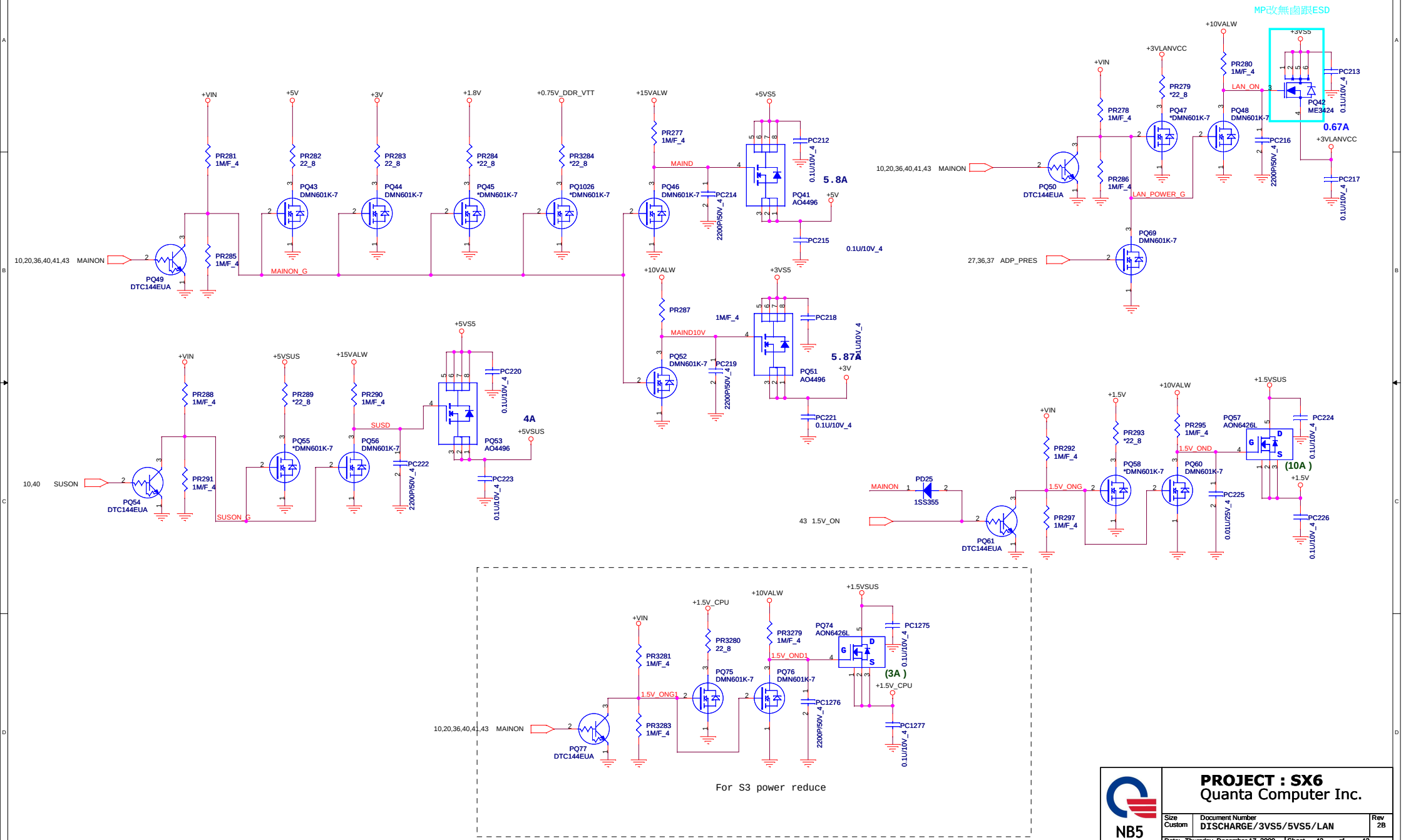
Date: Thursday, December 17, 2009 | Sheet 40 of 43



+1.05V_PCH Volt +/- 5%
Countinue current:4A
Peak current:7A
OCP minimum 9A

+1.8V Volt +/- 5%
Countinue current:1A
Peak current:2A
OCP minimum 3A

NB5	**PROJECT : SX6** Quanta Computer Inc.	
Size: Custom	Document Number: PCH +1.05V	Rev: 2B
Date: Thursday, December 17, 2009	Sheet 41 of 43	



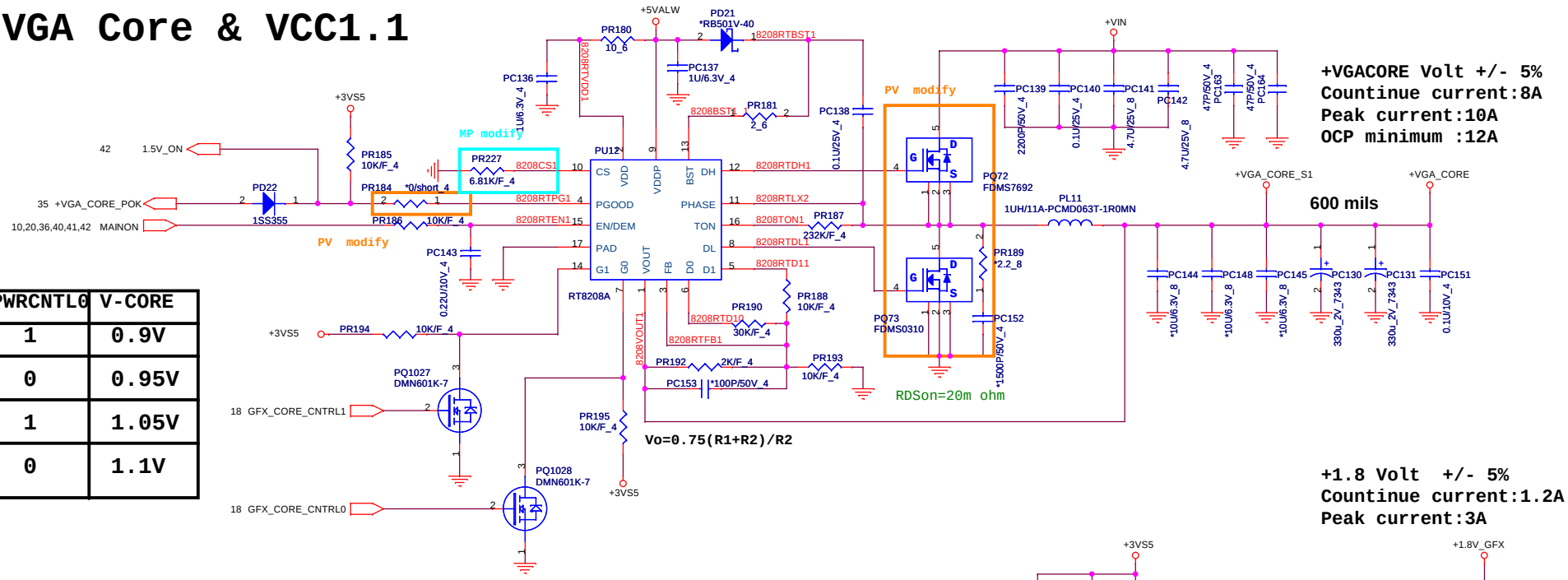
PROJECT : SX6
Quanta Computer Inc.

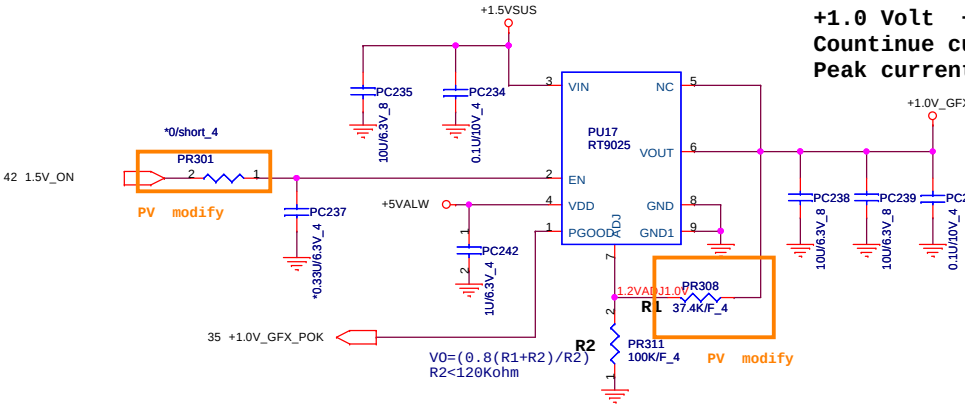
Size	Document Number	Rev
Custom	DISCHARGE/3VS5/5VS5/LAN	2B
Date: Thursday, December 17, 2009	Sheet 42 of 43	

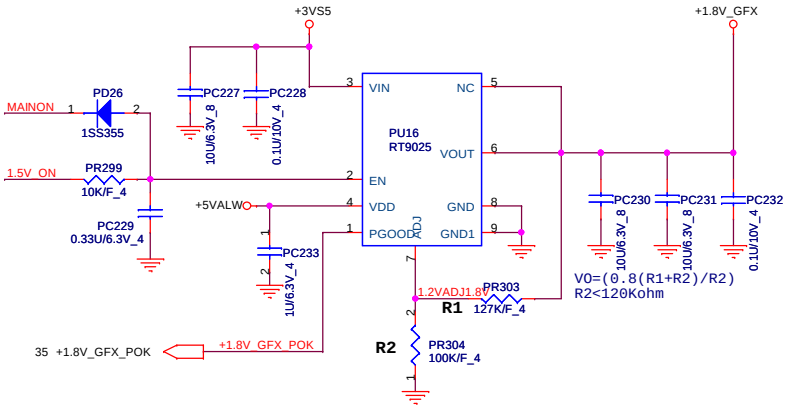
NB5

VGA Core & VCC1.1

	PWRCNTL1	PWRCNTL0	V-CORE
	1	1	0.9V
	1	0	0.95V
	0	1	1.05V
	0	0	1.1V







NB5	PROJECT : SX6 Quanta Computer Inc.	
Size: Custom	Document Number: VGA Core/+1.8VGFX/1.0VGFX	Rev: 2B
Date: Thursday, December 17, 2009	Sheet 43 of 43	