

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : SGND2
LAYER 8 : BOT

Cable Docking

TV_OUT
VGA
RJ-45
CIR/Pwr btn
SPDIF Out
Stereo MIC
Headphone Jack
USB Port
VOL Cntr

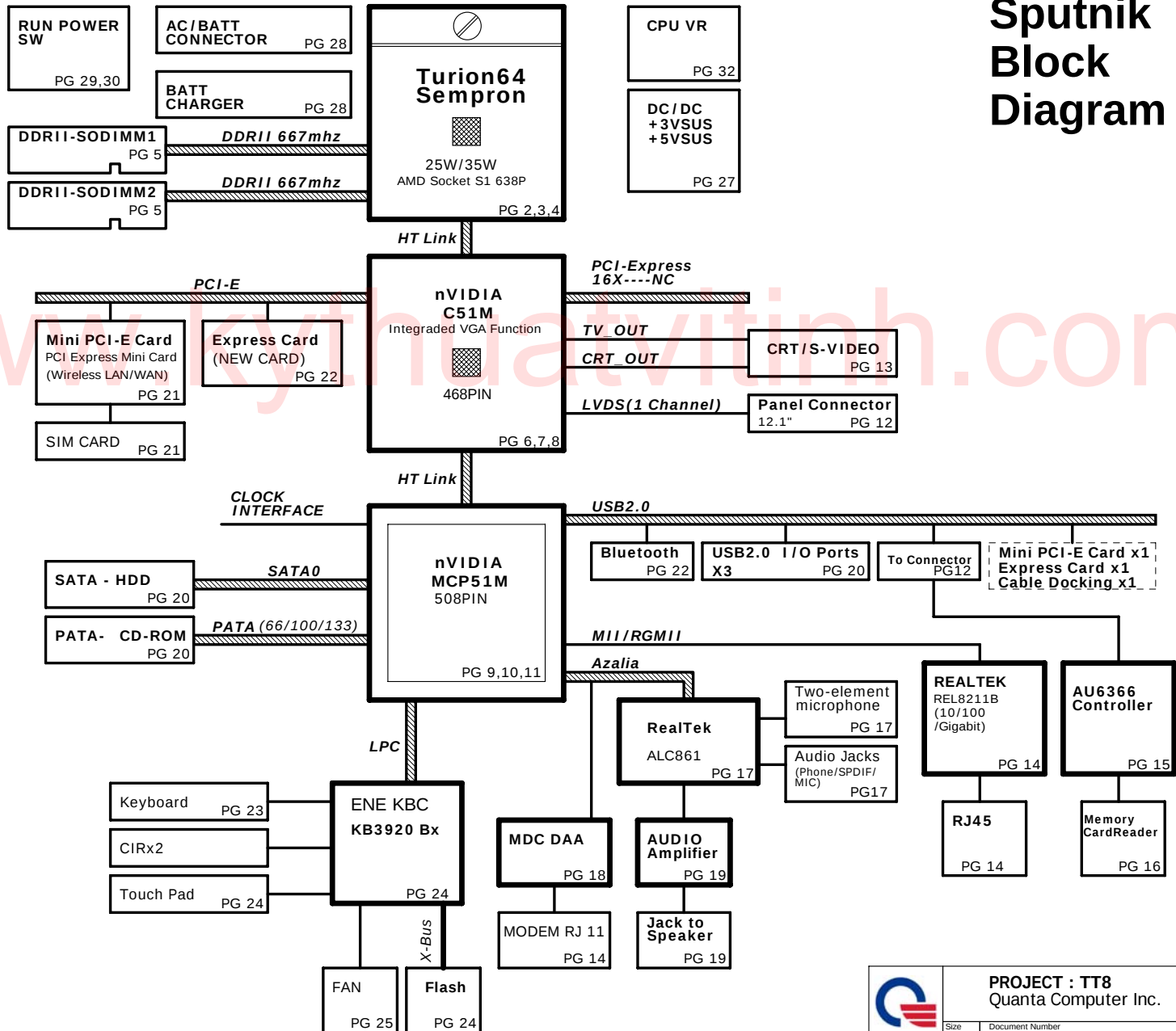
PG 25

VAULE DEFINE

A=0603,B=0805,C=1206,F=1%,
OTHER IS 0402

EXAMPLE

10R=10ohm(0402)
10A=10ohm(0603)
10B=10ohm(0805)
10C=10ohm(1206)
10/F=10ohm(0402 and 1%)



Sputnik Block Diagram



Size
Custom

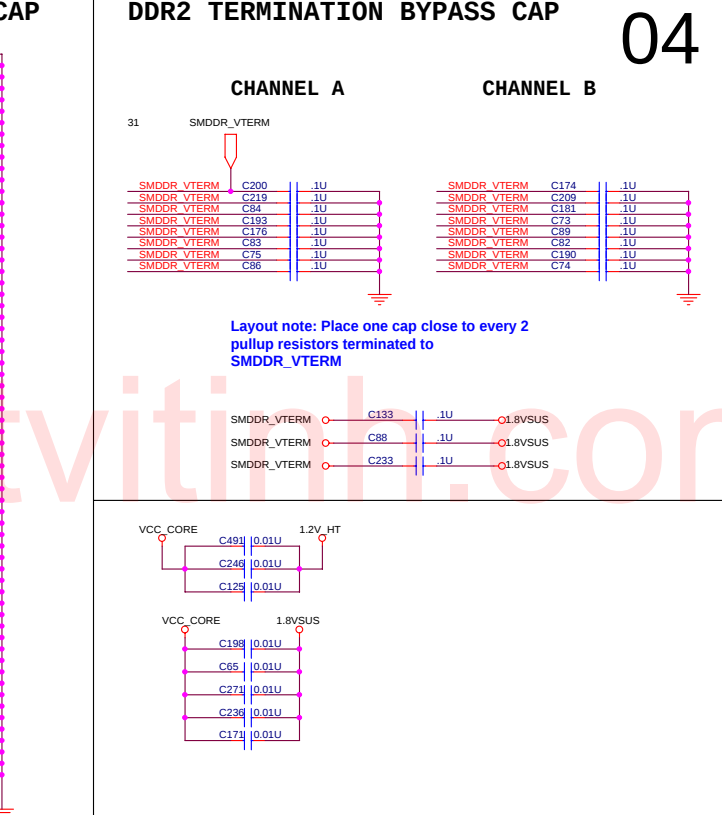
PROJECT : TT8
Quanta Computer Inc.

Document Number
Block Diagram

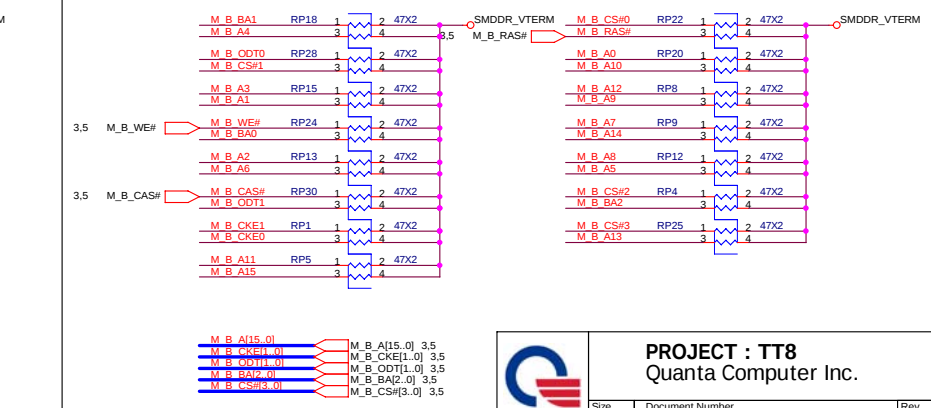
Date: Friday, November 24, 2006 Sheet 1 of 36

Rev
1A

04



DDRII CHANNEL B TERMINATION



M_A_CKE[0..1] 3,4
M_A_CS[0..3] 3,4
M_A_RAS# 3,4
M_A_CAS# 3,4
M_A_WE# 3,4

M_A_CLK1 3
M_A_CLK1# 3
M_A_CLK2 3
M_A_CLK2# 3
M_A_BA[0..2] 3,4
M_A_ODT[0..1] 3,4

M_A_DQM[0..7] 3
M_A_DQM[0..63] 3
M_A_DQS[0..7] 3
M_A_DQS[0..63] 3
M_A_A[15..0] 3,4
M_A_A[15..0] 3,4

M_B_CKE[0..1] 3,4
M_B_CS[0..3] 3,4
M_B_RAS# 3,4
M_B_CAS# 3,4
M_B_WE# 3,4

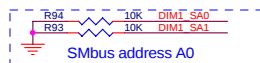
M_B_CLK1 3
M_B_CLK1# 3
M_B_CLK2 3
M_B_CLK2# 3
M_B_BA[0..2] 3,4
M_B_ODT[0..1] 3,4

M_B_DQM[0..7] 3
M_B_DQM[0..63] 3
M_B_DQS[0..7] 3
M_B_DQS[0..63] 3
M_B_A[15..0] 3,4
M_B_A[15..0] 3,4

M_A_DQ0 5 DQ0
M_A_DQ1 7 DQ1
M_A_DQ2 17 DQ2
M_A_DQ3 19 DQ3
M_A_DQ4 4 DQ4
M_A_DQ5 6 DQ5
M_A_DQ6 14 DQ6
M_A_DQ7 16 DQ7
M_A_DQ8 23 DQ8
M_A_DQ9 35 DQ9
M_A_DQ10 37 DQ10
M_A_DQ11 20 DQ11
M_A_DQ12 22 DQ12
M_A_DQ13 36 DQ13
M_A_DQ14 38 DQ14
M_A_DQ15 43 DQ15
M_A_DQ16 55 DQ16
M_A_DQ17 57 DQ17
M_A_DQ18 46 DQ18
M_A_DQ19 59 DQ19
M_A_DQ20 44 DQ20
M_A_DQ21 56 DQ21
M_A_DQ22 58 DQ22
M_A_DQ23 45 DQ23
M_A_DQ24 61 DQ24
M_A_DQ25 63 DQ25
M_A_DQ26 75 DQ26
M_A_DQ27 77 DQ27
M_A_DQ28 64 DQ28
M_A_DQ29 74 DQ29
M_A_DQ30 76 DQ30
M_A_DQ31 76 DQ31

M_A_A0 102 A0
M_A_A1 101 A1
M_A_A2 100 A2
M_A_A3 99 A3
M_A_A4 98 A4
M_A_A5 97 A5
M_A_A6 94 A6
M_A_A7 92 A7
M_A_A8 93 A8
M_A_A9 91 A9
M_A_A10 105 A10
M_A_A11 90 A11
M_A_A12 89 A12
M_A_BA0 107 BA0
M_A_BA1 106 BA1
M_A_BA2 85 NC/BA2
M_A_CLK1 30 CLK1
M_A_CLK1# 32 CLK1#
M_A_CLK2 164 CLK2
M_A_CLK2# 166 CLK2#
DDR_SMBCLK1 197 SCL
DDR_SMBCLK2 198 SDA
DIM1_SA0 198 SA0
DIM1_SA1 200 SA1
3V 199 VDDSPD
CKE0 199 CKE0
CKE1 80 CKE1

CKE 0,1
REV type : H 6.5



M_B_DQ0 5 DQ0
M_B_DQ1 7 DQ1
M_B_DQ2 17 DQ2
M_B_DQ3 19 DQ3
M_B_DQ4 4 DQ4
M_B_DQ5 6 DQ5
M_B_DQ6 16 DQ6
M_B_DQ7 16 DQ7
M_B_DQ8 23 DQ8
M_B_DQ9 35 DQ9
M_B_DQ10 37 DQ10
M_B_DQ11 20 DQ11
M_B_DQ12 22 DQ12
M_B_DQ13 36 DQ13
M_B_DQ14 38 DQ14
M_B_DQ15 43 DQ15
M_B_DQ16 55 DQ16
M_B_DQ17 57 DQ17
M_B_DQ18 46 DQ18
M_B_DQ19 59 DQ19
M_B_DQ20 44 DQ20
M_B_DQ21 56 DQ21
M_B_DQ22 58 DQ22
M_B_DQ23 45 DQ23
M_B_DQ24 61 DQ24
M_B_DQ25 63 DQ25
M_B_DQ26 75 DQ26
M_B_DQ27 77 DQ27
M_B_DQ28 64 DQ28
M_B_DQ29 74 DQ29
M_B_DQ30 76 DQ30
M_B_DQ31 76 DQ31

M_B_A0 102 A0
M_B_A1 101 A1
M_B_A2 100 A2
M_B_A3 99 A3
M_B_A4 98 A4
M_B_A5 97 A5
M_B_A6 94 A6
M_B_A7 92 A7
M_B_A8 93 A8
M_B_A9 91 A9
M_B_A10 105 A10
M_B_A11 90 A11
M_B_A12 89 A12
M_B_BA0 107 BA0
M_B_BA1 106 BA1
M_B_BA2 85 NC/BA2
M_B_CLK1 30 CLK1
M_B_CLK1# 32 CLK1#
M_B_CLK2 164 CLK2
M_B_CLK2# 166 CLK2#
DDR_SMBCLK1 197 SCL
DDR_SMBCLK2 198 SDA
DIM2_SA0 198 SA0
DIM2_SA1 200 SA1
3V 199 VDDSPD
CKE0 199 CKE0
CKE1 80 CKE1

CKE 2,3
REV type : H 11



M_B_DQ0 5 DQ0
M_B_DQ1 7 DQ1
M_B_DQ2 17 DQ2
M_B_DQ3 19 DQ3
M_B_DQ4 4 DQ4
M_B_DQ5 6 DQ5
M_B_DQ6 16 DQ6
M_B_DQ7 16 DQ7
M_B_DQ8 23 DQ8
M_B_DQ9 35 DQ9
M_B_DQ10 37 DQ10
M_B_DQ11 20 DQ11
M_B_DQ12 22 DQ12
M_B_DQ13 36 DQ13
M_B_DQ14 38 DQ14
M_B_DQ15 43 DQ15
M_B_DQ16 55 DQ16
M_B_DQ17 57 DQ17
M_B_DQ18 46 DQ18
M_B_DQ19 59 DQ19
M_B_DQ20 44 DQ20
M_B_DQ21 56 DQ21
M_B_DQ22 58 DQ22
M_B_DQ23 45 DQ23
M_B_DQ24 61 DQ24
M_B_DQ25 63 DQ25
M_B_DQ26 75 DQ26
M_B_DQ27 77 DQ27
M_B_DQ28 64 DQ28
M_B_DQ29 74 DQ29
M_B_DQ30 76 DQ30
M_B_DQ31 76 DQ31

M_B_A0 102 A0
M_B_A1 101 A1
M_B_A2 100 A2
M_B_A3 99 A3
M_B_A4 98 A4
M_B_A5 97 A5
M_B_A6 94 A6
M_B_A7 92 A7
M_B_A8 93 A8
M_B_A9 91 A9
M_B_A10 105 A10
M_B_A11 90 A11
M_B_A12 89 A12
M_B_BA0 107 BA0
M_B_BA1 106 BA1
M_B_BA2 85 NC/BA2
M_B_CLK1 30 CLK1
M_B_CLK1# 32 CLK1#
M_B_CLK2 164 CLK2
M_B_CLK2# 166 CLK2#
DDR_SMBCLK1 197 SCL
DDR_SMBCLK2 198 SDA
DIM2_SA0 198 SA0
DIM2_SA1 200 SA1
3V 199 VDDSPD
CKE0 199 CKE0
CKE1 80 CKE1

M_B_DQ0 5 DQ0
M_B_DQ1 7 DQ1
M_B_DQ2 17 DQ2
M_B_DQ3 19 DQ3
M_B_DQ4 4 DQ4
M_B_DQ5 6 DQ5
M_B_DQ6 16 DQ6
M_B_DQ7 16 DQ7
M_B_DQ8 23 DQ8
M_B_DQ9 35 DQ9
M_B_DQ10 37 DQ10
M_B_DQ11 20 DQ11
M_B_DQ12 22 DQ12
M_B_DQ13 36 DQ13
M_B_DQ14 38 DQ14
M_B_DQ15 43 DQ15
M_B_DQ16 55 DQ16
M_B_DQ17 57 DQ17
M_B_DQ18 46 DQ18
M_B_DQ19 59 DQ19
M_B_DQ20 44 DQ20
M_B_DQ21 56 DQ21
M_B_DQ22 58 DQ22
M_B_DQ23 45 DQ23
M_B_DQ24 61 DQ24
M_B_DQ25 63 DQ25
M_B_DQ26 75 DQ26
M_B_DQ27 77 DQ27
M_B_DQ28 64 DQ28
M_B_DQ29 74 DQ29
M_B_DQ30 76 DQ30
M_B_DQ31 76 DQ31

M_B_A0 102 A0
M_B_A1 101 A1
M_B_A2 100 A2
M_B_A3 99 A3
M_B_A4 98 A4
M_B_A5 97 A5
M_B_A6 94 A6
M_B_A7 92 A7
M_B_A8 93 A8
M_B_A9 91 A9
M_B_A10 105 A10
M_B_A11 90 A11
M_B_A12 89 A12
M_B_BA0 107 BA0
M_B_BA1 106 BA1
M_B_BA2 85 NC/BA2
M_B_CLK1 30 CLK1
M_B_CLK1# 32 CLK1#
M_B_CLK2 164 CLK2
M_B_CLK2# 166 CLK2#
DDR_SMBCLK1 197 SCL
DDR_SMBCLK2 198 SDA
DIM2_SA0 198 SA0
DIM2_SA1 200 SA1
3V 199 VDDSPD
CKE0 199 CKE0
CKE1 80 CKE1

M_B_DQ0 5 DQ0
M_B_DQ1 7 DQ1
M_B_DQ2 17 DQ2
M_B_DQ3 19 DQ3
M_B_DQ4 4 DQ4
M_B_DQ5 6 DQ5
M_B_DQ6 16 DQ6
M_B_DQ7 16 DQ7
M_B_DQ8 23 DQ8
M_B_DQ9 35 DQ9
M_B_DQ10 37 DQ10
M_B_DQ11 20 DQ11
M_B_DQ12 22 DQ12
M_B_DQ13 36 DQ13
M_B_DQ14 38 DQ14
M_B_DQ15 43 DQ15
M_B_DQ16 55 DQ16
M_B_DQ17 57 DQ17
M_B_DQ18 46 DQ18
M_B_DQ19 59 DQ19
M_B_DQ20 44 DQ20
M_B_DQ21 56 DQ21
M_B_DQ22 58 DQ22
M_B_DQ23 45 DQ23
M_B_DQ24 61 DQ24
M_B_DQ25 63 DQ25
M_B_DQ26 75 DQ26
M_B_DQ27 77 DQ27
M_B_DQ28 64 DQ28
M_B_DQ29 74 DQ29
M_B_DQ30 76 DQ30
M_B_DQ31 76 DQ31

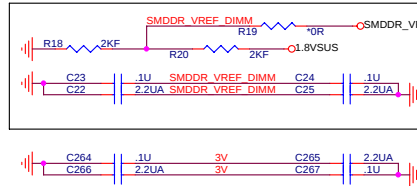
M_B_A0 102 A0
M_B_A1 101 A1
M_B_A2 100 A2
M_B_A3 99 A3
M_B_A4 98 A4
M_B_A5 97 A5
M_B_A6 94 A6
M_B_A7 92 A7
M_B_A8 93 A8
M_B_A9 91 A9
M_B_A10 105 A10
M_B_A11 90 A11
M_B_A12 89 A12
M_B_BA0 107 BA0
M_B_BA1 106 BA1
M_B_BA2 85 NC/BA2
M_B_CLK1 30 CLK1
M_B_CLK1# 32 CLK1#
M_B_CLK2 164 CLK2
M_B_CLK2# 166 CLK2#
DDR_SMBCLK1 197 SCL
DDR_SMBCLK2 198 SDA
DIM2_SA0 198 SA0
DIM2_SA1 200 SA1
3V 199 VDDSPD
CKE0 199 CKE0
CKE1 80 CKE1

M_B_DQ0 5 DQ0
M_B_DQ1 7 DQ1
M_B_DQ2 17 DQ2
M_B_DQ3 19 DQ3
M_B_DQ4 4 DQ4
M_B_DQ5 6 DQ5
M_B_DQ6 16 DQ6
M_B_DQ7 16 DQ7
M_B_DQ8 23 DQ8
M_B_DQ9 35 DQ9
M_B_DQ10 37 DQ10
M_B_DQ11 20 DQ11
M_B_DQ12 22 DQ12
M_B_DQ13 36 DQ13
M_B_DQ14 38 DQ14
M_B_DQ15 43 DQ15
M_B_DQ16 55 DQ16
M_B_DQ17 57 DQ17
M_B_DQ18 46 DQ18
M_B_DQ19 59 DQ19
M_B_DQ20 44 DQ20
M_B_DQ21 56 DQ21
M_B_DQ22 58 DQ22
M_B_DQ23 45 DQ23
M_B_DQ24 61 DQ24
M_B_DQ25 63 DQ25
M_B_DQ26 75 DQ26
M_B_DQ27 77 DQ27
M_B_DQ28 64 DQ28
M_B_DQ29 74 DQ29
M_B_DQ30 76 DQ30
M_B_DQ31 76 DQ31

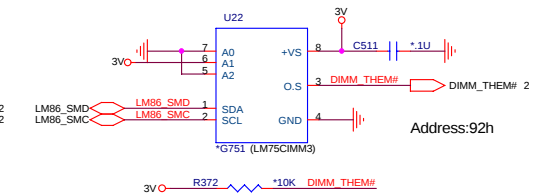
M_B_A0 102 A0
M_B_A1 101 A1
M_B_A2 100 A2
M_B_A3 99 A3
M_B_A4 98 A4
M_B_A5 97 A5
M_B_A6 94 A6
M_B_A7 92 A7
M_B_A8 93 A8
M_B_A9 91 A9
M_B_A10 105 A10
M_B_A11 90 A11
M_B_A12 89 A12
M_B_BA0 107 BA0
M_B_BA1 106 BA1
M_B_BA2 85 NC/BA2
M_B_CLK1 30 CLK1
M_B_CLK1# 32 CLK1#
M_B_CLK2 164 CLK2
M_B_CLK2# 166 CLK2#
DDR_SMBCLK1 197 SCL
DDR_SMBCLK2 198 SDA
DIM2_SA0 198 SA0
DIM2_SA1 200 SA1
3V 199 VDDSPD
CKE0 199 CKE0
CKE1 80 CKE1

SMDDR_VREF_DIMM :
TRACE WIDTH > 20 MIL
PUT BYPASS CAP ON EACH DIMM

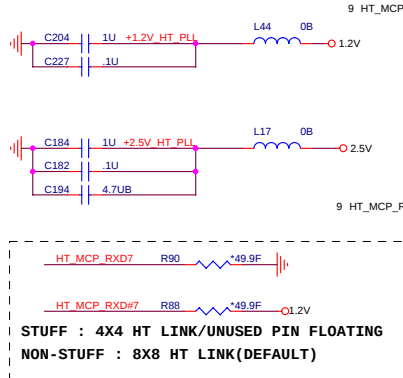
SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.



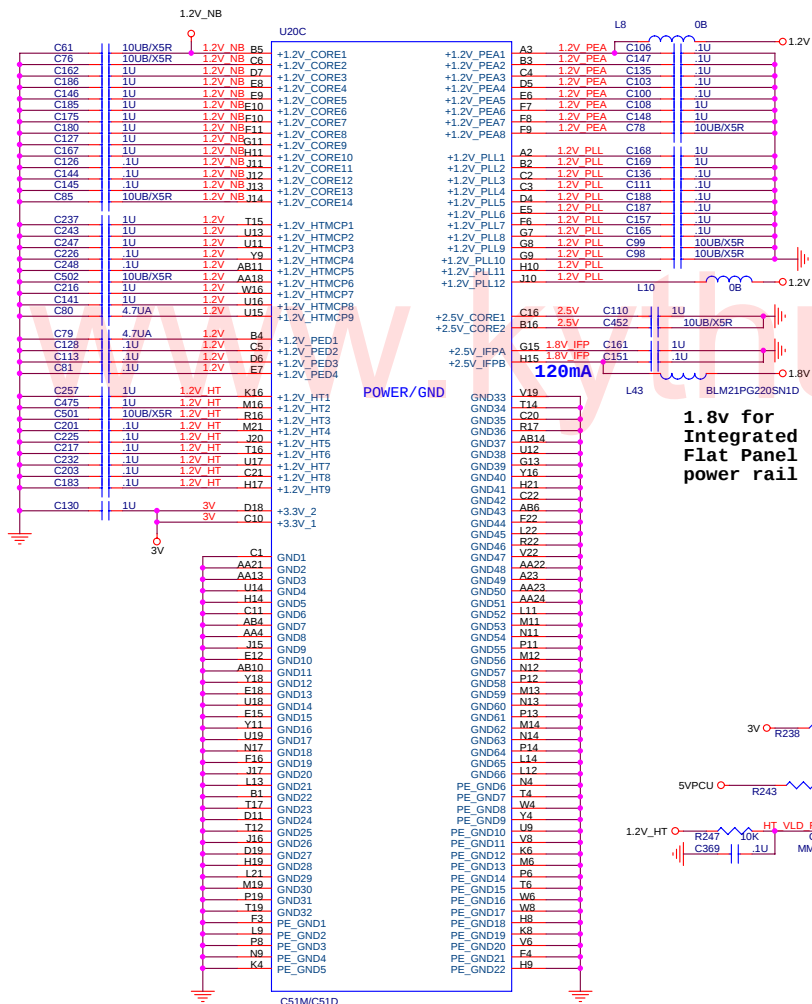
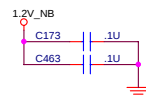
Close DDR2 socket



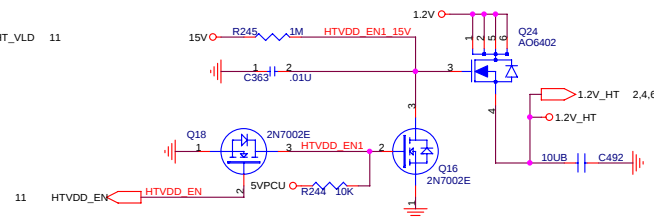
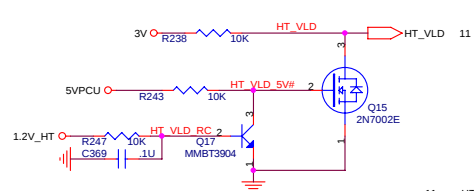
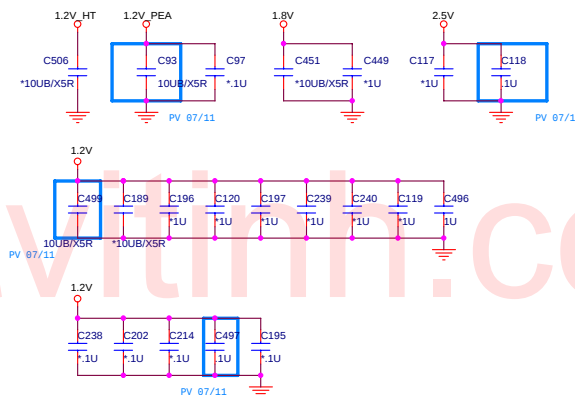
PROJECT : TT8
Quanta Computer Inc.



C51M POWER PLANE/GND & BYPASS



1.8v for
Integrated
Flat Panel
power rail



6 HT_MCP_TXD[0..7] HT_MCP_RXD[0..7] U11A HT_MCP_RXD[0..7] 6 HT_MCP_RXD[0..7] 6 HT_MCP_TXD[0..7]

HT LINK

HT_MCP_TXD0 K1
HT_MCP_TXD1 L1
HT_MCP_TXD2 M1
HT_MCP_TXD3 N1
HT_MCP_TXD4 R1
HT_MCP_TXD5 T1
HT_MCP_TXD6 U1
HT_MCP_TXD7 V1

HT_MCP_RXD0 K2
HT_MCP_RXD1 L2
HT_MCP_RXD2 M2
HT_MCP_RXD3 N2
HT_MCP_RXD4 R2
HT_MCP_RXD5 T2
HT_MCP_RXD6 U2
HT_MCP_RXD7 V2

6 HTMCP_DWNCCLK0 P1
6 HTMCP_DWNCCLK0 P2
6 HTMCP_DWNCCLK0 W1
6 HTMCP_DWNCCLK0 W2

6 HTMCP_REQ# AD13
6 HTMCP_STOP# AA5
R189 150R HTMCP_COMP_GND1 AB1
R187 49.9F HTMCP_COMP_GND2 AB2

1.5V_PLL_CPU_HT M6

3V_PLL_CPU_HT M5

PCI

AE19 PCI_AD0
AB21 PCI_AD1
AC19 PCI_AD2
AA20 PCI_AD3
AA19 PCI_AD4
AE20 PCI_AD5
AE19 PCI_AD6
AE20 PCI_AD7
AB20 PCI_AD8
AB19 PCI_AD9
AA18 PCI_AD10
AE18 PCI_AD11
AE18 PCI_AD12
AE18 PCI_AD13
AC17 PCI_AD14
AB17 PCI_AD15
AB15 PCI_AD16
AE15 PCI_AD17
AE15 PCI_AD18
AE14 PCI_AD19
AE14 PCI_AD20
AA14 PCI_AD21
AC13 PCI_AD22
AB13 PCI_AD23
AE13 PCI_AD24
AE13 PCI_AD25
AE13 PCI_AD26
AA12 PCI_AD27
AE12 PCI_AD28
AE12 PCI_AD29
AE12 PCI_AD30
AE11 PCI_AD31

AD19 PCI_CBE0#
AB17 PCI_CBE1#
AA15 PCI_CBE2#
AA13 PCI_CBE3#

HT_MCP_TXD0 P
HT_MCP_TXD1 P
HT_MCP_TXD2 P
HT_MCP_TXD3 P
HT_MCP_TXD4 P
HT_MCP_TXD5 P
HT_MCP_TXD6 P
HT_MCP_TXD7 P

HT_MCP_RXD0 N
HT_MCP_RXD1 N
HT_MCP_RXD2 N
HT_MCP_RXD3 N
HT_MCP_RXD4 N
HT_MCP_RXD5 N
HT_MCP_RXD6 N
HT_MCP_RXD7 N

V5 HT_MCP_TX_CLK_P
V6 HTMCP_UPCLK#0 6
N5 HT_MCP_TXCTL_P
N6 HTMCP_UPCLK#1 6
AC1 HTMCP_OUT_200M_P
AC2 HTMCP_OUT_200M_P 6

CLKOUT_200MHZ_P
CLKOUT_200MHZ_N
CLK200_TERM_GND
K6 200MHZ_THRM_GND
R443 502F

10mil/10mil

Y5 MCPOUT_25M_C
R421 22R MCPOUT_25M 6

PCI_FRAME# AC15 FRAME#
PCI_IRDY# AD15 IRDY#
PCI_TRDY# AB16 TRDY#
PCI_STOP# AE16 STOP#
PCI_DEVSEL# AA16 DEVSEL#
PCI_PAR AE17 PERR#
PCI_PERR/GPIO43# AE17 PERR#
PCI_SERR# AE17 SERR#
PCI_PME/GPIO30# AD11 BTLED
PCI_CLKRUN/GPIO42#(3V) AE25 CLKRUN# 24

PCI_REQ0# AE22 REQ0#
PCI_REQ1# AE22 REQ1#
PCI_REQ2# AE21 REQ2#
PCI_REQ3#(GPIO38#) AE22 WWAN_OFF#
PCI_REQ4#(GPIO40#) AE22 WLAN_OFF#

PCI_GNT0# AE21 GNT0#
PCI_GNT1# AC21 GNT1#
PCI_GNT2# AE21 GNT2#
PCI_GNT3#(GPIO39#) AB24 NB_BEEPEN R420 0R AMPBEEP_EN 19
PCI_GNT4#(GPIO41#) AB22 NB_LCDBK R412 0R LCD_BK 12

PCI_INTW# AE11 INTA#
PCI_INTX# AB11 INTB#
PCI_INTY# AC11 INTX#
PCI_INTZ# AE11 INTD#
AE24 PCI_CLK_5C832 L T74
AE24 PCLK_MINI L T72
AE23 MCP51_PCLK3 T78
AB23 PCI_CLK4 R418 22R

PCI_CLKIN AC23 PCI_CLKIN
W22 MCP51_PCSRST3# T113
AE26 MCP51_PCSRST2# T77
AE24 PCSRST_R# T76
AE25 IDERST_R# R163 33R IDERST# 20
AD2 HTMCP_PWRGD L R181 0R HTMCP_PWRGD 6
AE1 HTMCP_RST1#

LPC

LPC_PWRDWN#(GPIO54#) 3V
LPC_CLK0
LPC_CLK1
LPC_CLK2
LPC_CLK3
LPC_CLK4

LPC_FRAME# G25
LPC_DRQ0# K21
LPC_DRQ1# K22
LPC_DRQ2# K23
LPC_DRQ3# K24

LPC_RST# R203 33R
LPC_RST1# L26
LPC_RESET#(RVCC)

JTAG

JTAG_TCK
JTAG_TDI
JTAG_TMS
JTAG_TRST#

NVIDIA MCP51

5 MIL (75mA)
C585 .1U 1.5V_PLL_CPU_HT R436 0A 1.5V

1.5V_PLL_CPU_HT

5 MIL (20mA)
C587 .1U 3V_PLL_CPU_HT L30 BLM21PG220SNID 0.3V
C355 10UB
C353 .01U C360 .1U

3V_PLL_CPU_HT

RP34 10P8R-8.2K
DEVSEL# 6 INTD# 5
TRDY# 7 INTB# 4
FRAME# 8 INTX# 3
IRDY# 9 INTA# 1

PV 67/11
SERIRQ R440 10K 0.3V
BTLED BTLED R413 8.2K 0.3V
LFRAME# R214 8.2K 0.3V

RP35 10P8R-8.2K
CLKRUN# 6 LAD2# 5
LDREQ# 7 LAD3# 4
LAD1 8 LAD0 3
LAD3 2 REQ0# 1

RP33 10P8R-8.2K
SERR# 7 REQ1# 5
PERR# 8 REQ2# 4
STOP# 9 PR_NC 1

PCI/LPC PULL-UP

HT_MCP_TXD7 R195 *49.9F 1.2V
HT_MCP_TXD7 R192 *49.9F

STUFF : 4X4 HT LINK/UNUSED PIN FLOATING (DEFAULT)
NON-STUFF : 8X8 HT LINK

C359 10P/50V PCLK_LPC_DEBUG
C356 10P/50V PCLK_LPC_KB3920
C552 10P/50V MCPOUT_25M

CLOCK BYPASS

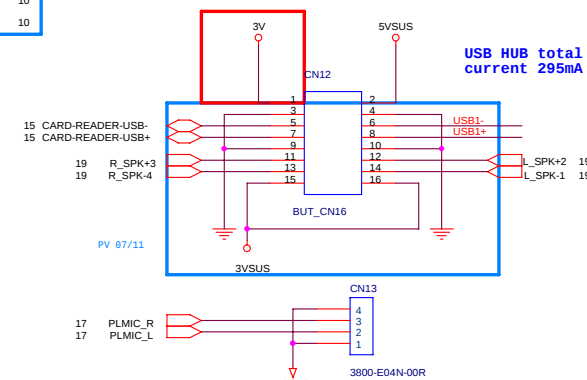
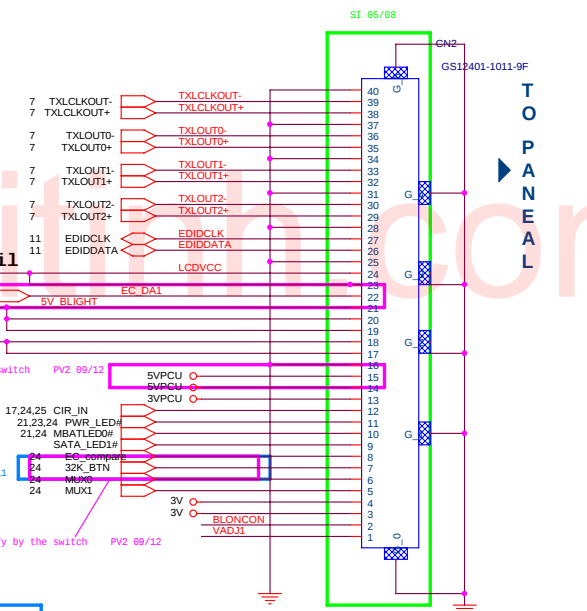
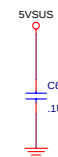
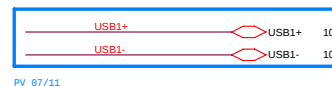
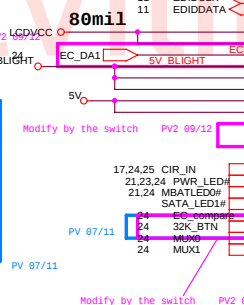
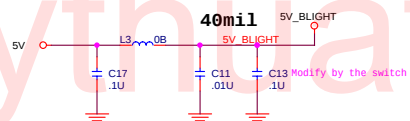
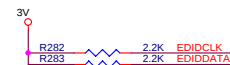
PV 67/11
6 HTMCP_RST# HTMCP_RST# D37 CH5014-40HTMCP_PWRGD R416 1.5KF
R180 1.5KF
HTMCP_REQ# R182 1.5KF
HTMCP_STOP# R422 1.5KF

HTMCP_PWRGD R415 *0R VCORE_ON VCORE_ON 11.32
Reserve for A02 version.

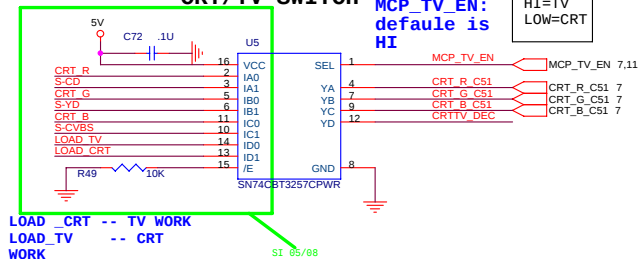


PROJECT : TT8
Quanta Computer Inc.

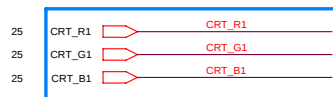
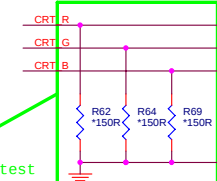
Size Custom Document Number MCP51 (1 of 3) Rev 1A
Date: Friday, November 24, 2006 Sheet 9 of 36



CRT/TV SWITCH

MCP_TV_EN:
default is
HIHI=TV
LOW=CRT

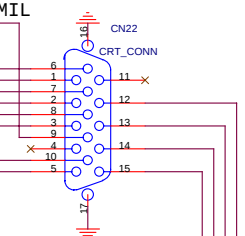
PV 07/11

150-R as possible as
closed to CRT connector
(close with in 600 mil)

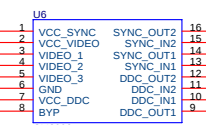
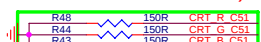
Change from nVIDIA for B-test



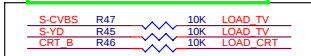
CRT PORT

close conn within
600mils

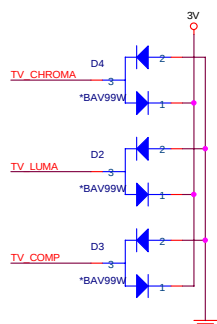
ESD PROTECTION

close within 600mils (
close data switch)

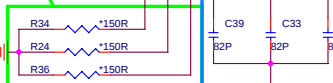
Change from nVIDIA for B-test

That is for CRT and TV choose..
used impedance and driver to
choose

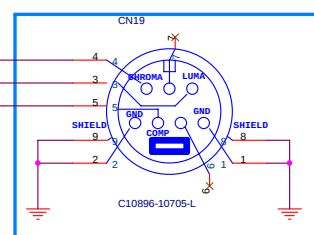
PV 07/11



Change from nVIDIA for B-test

150-R as possible as
closed to Tv connector (close with
in 600 mil)

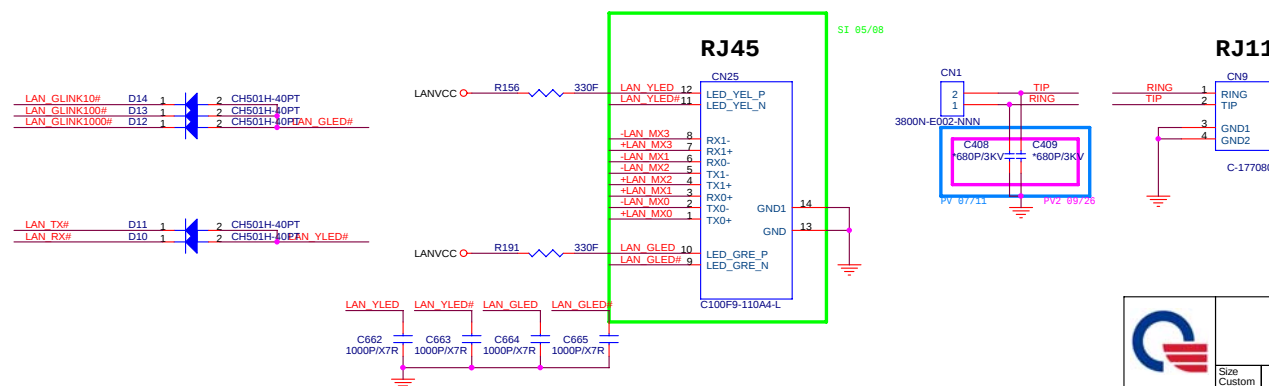
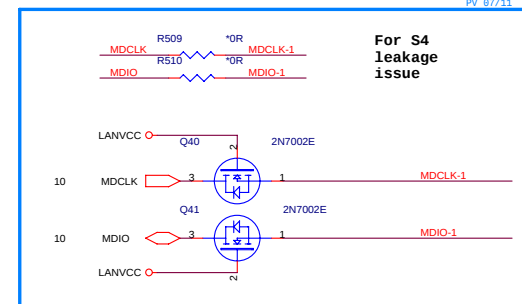
TV_OUT

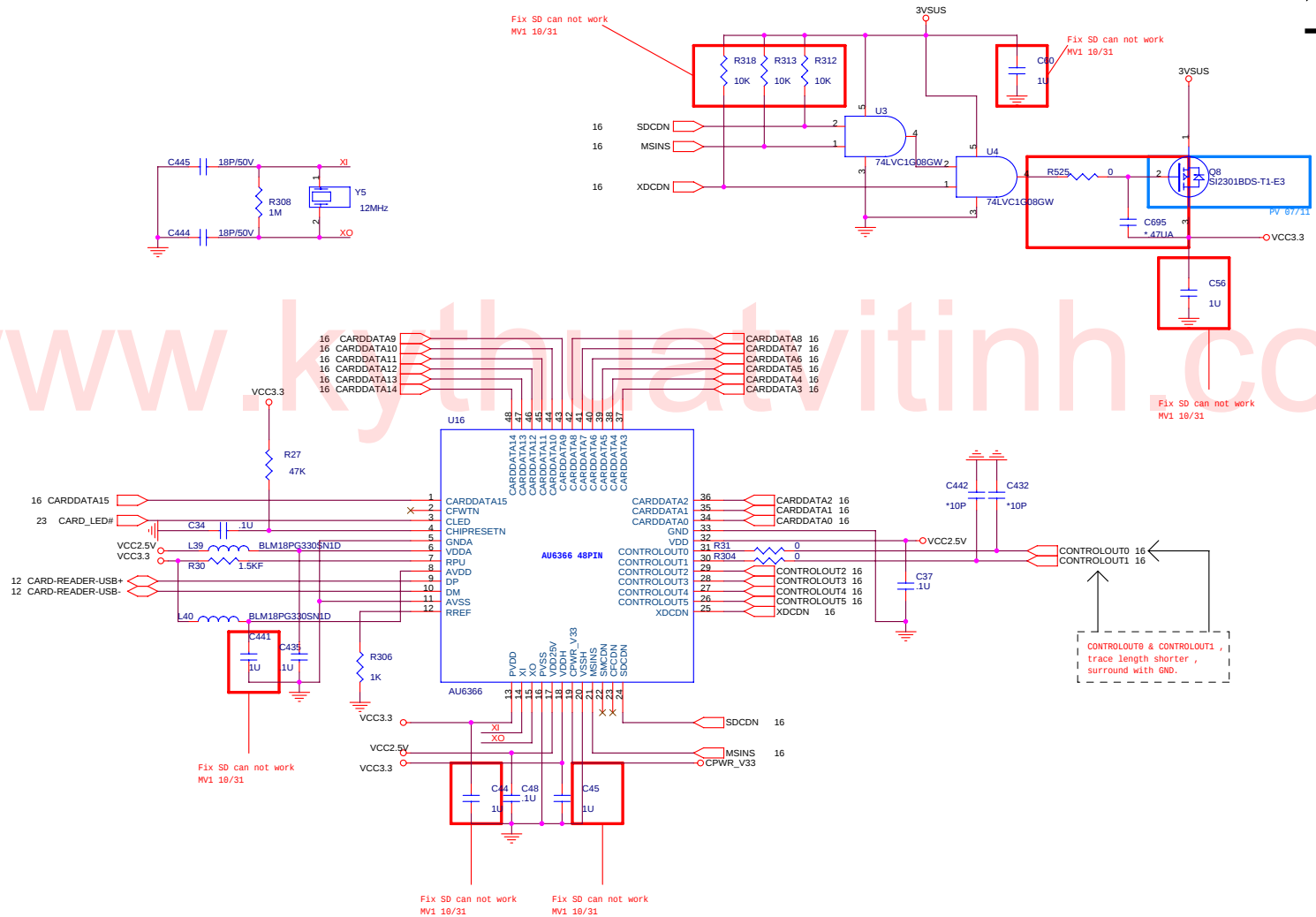


PV 07/11

PROJECT : TT8
Quanta Computer Inc.

Size Custom	Document Number CRT_TV_OUT	Rev 1A
Date: Friday, November 24, 2006	Sheet 13 of 36	



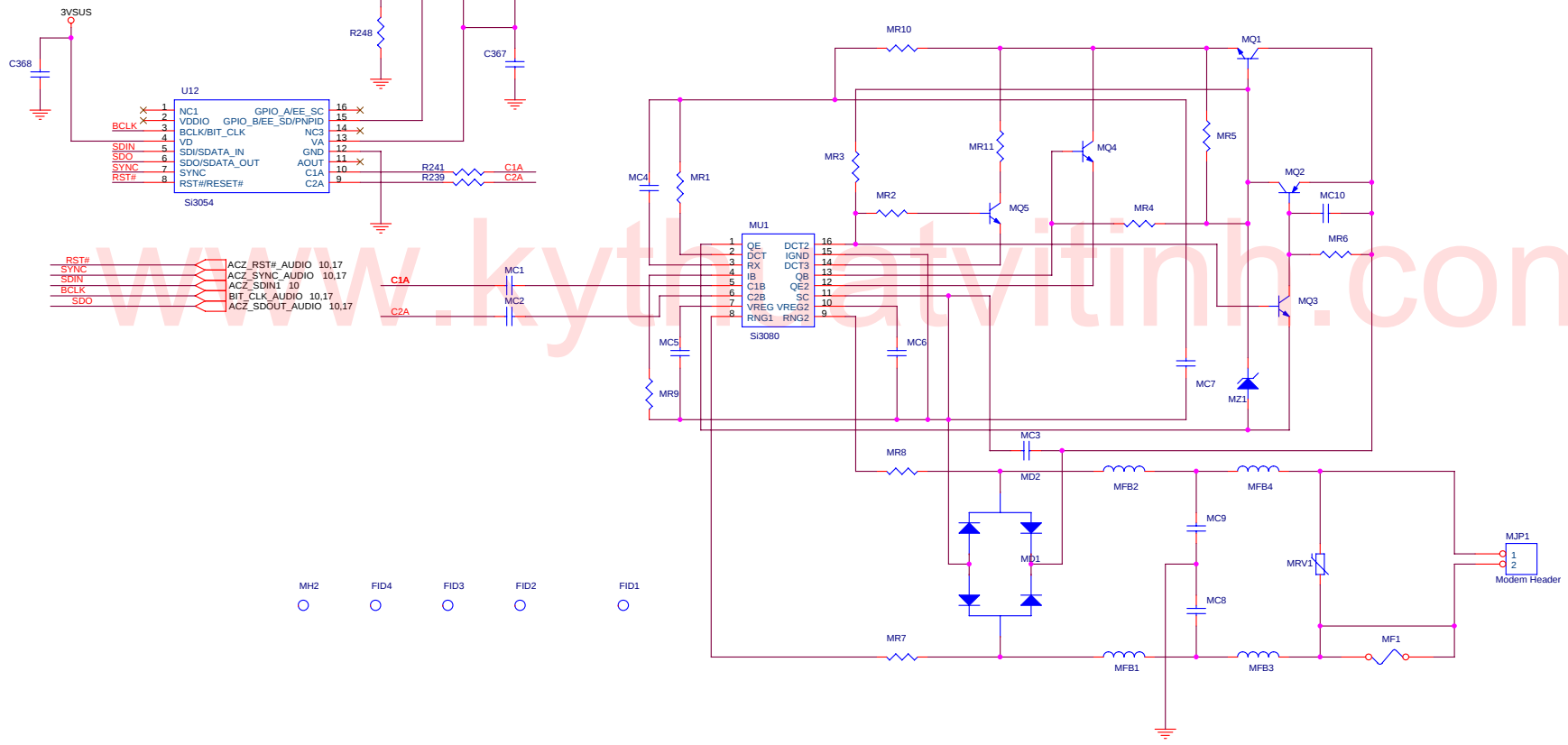


NBS/RD2/HW1

PROJECT : TT8
Quanta Computer Inc.

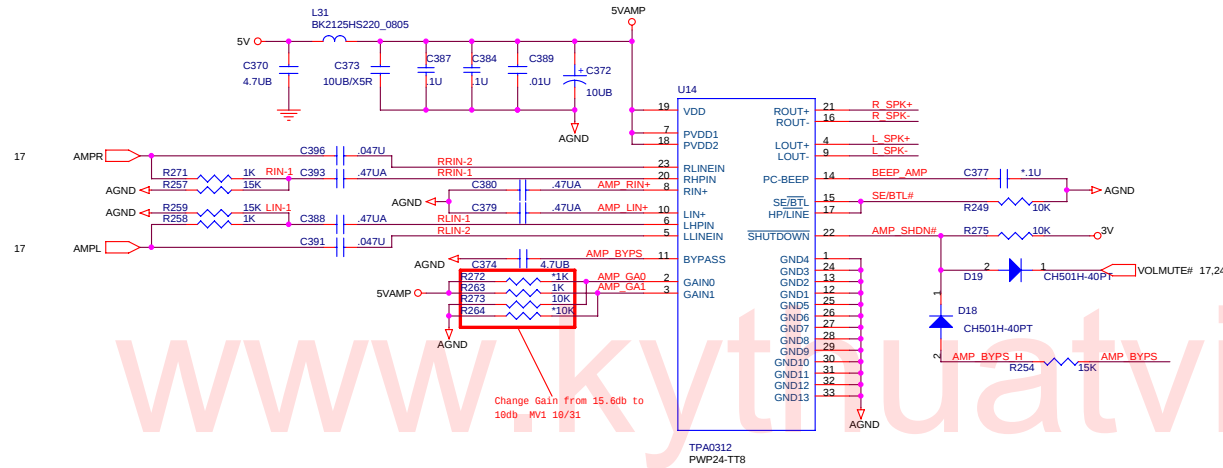
Size
CustomDocument Number
AU6366 controllerRev
1A

Date: Friday, November 24, 2006 Sheet 15 of 36



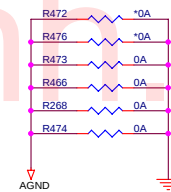
DESIGN SUBJECT TO CHANGE

SILICON LABORATORIES CONFIDENTIAL



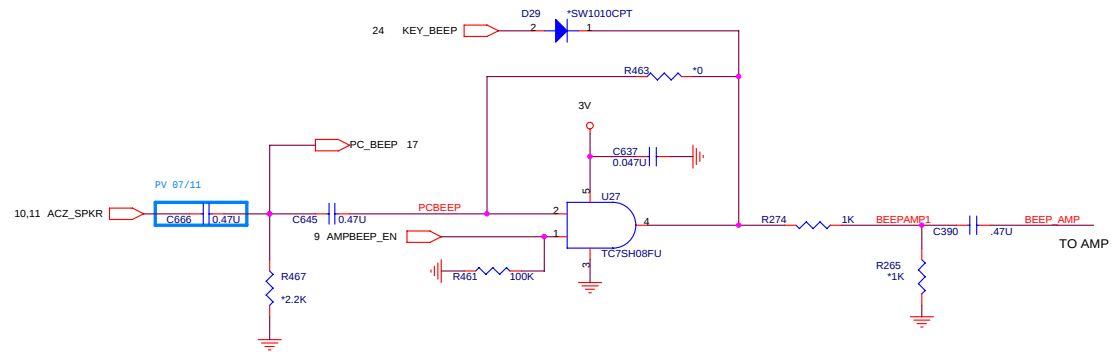
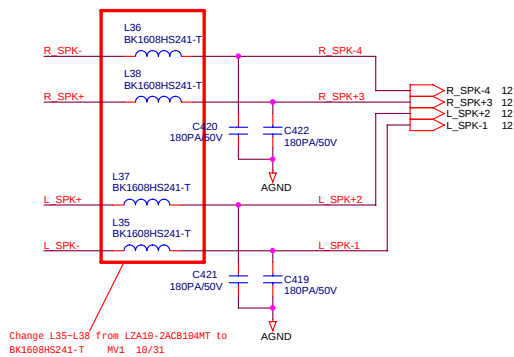
0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



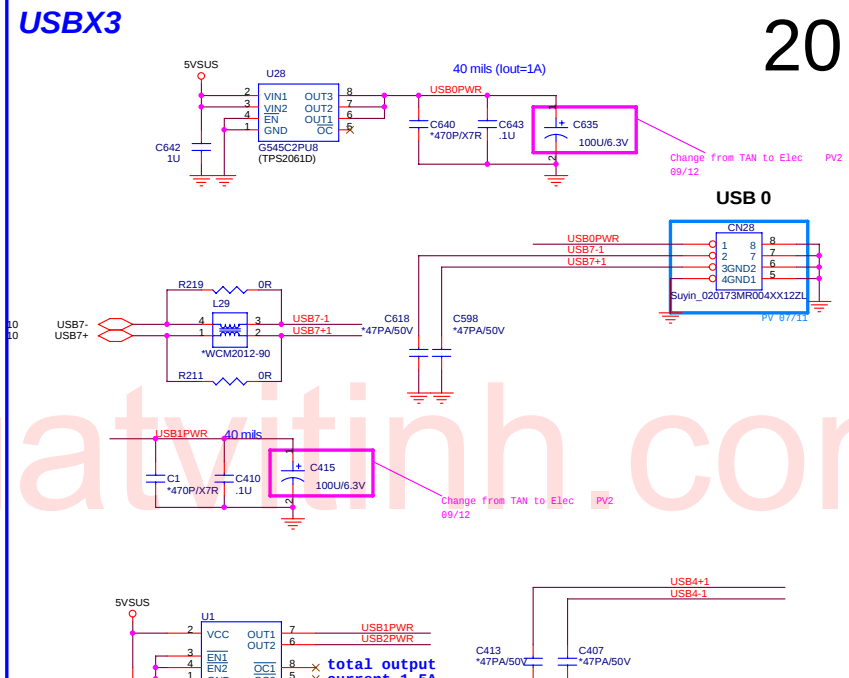
INT. SPEAKER

PCSPK BEEP

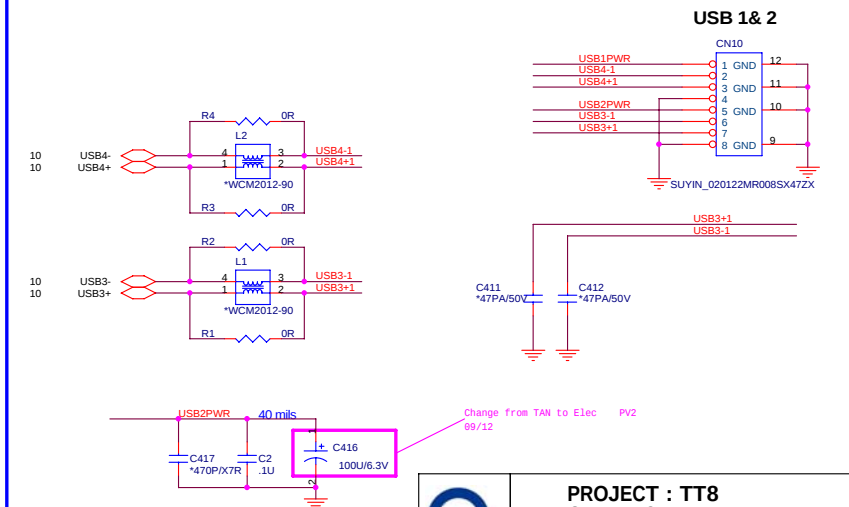


PROJECT : TT8
Quanta Computer Inc.

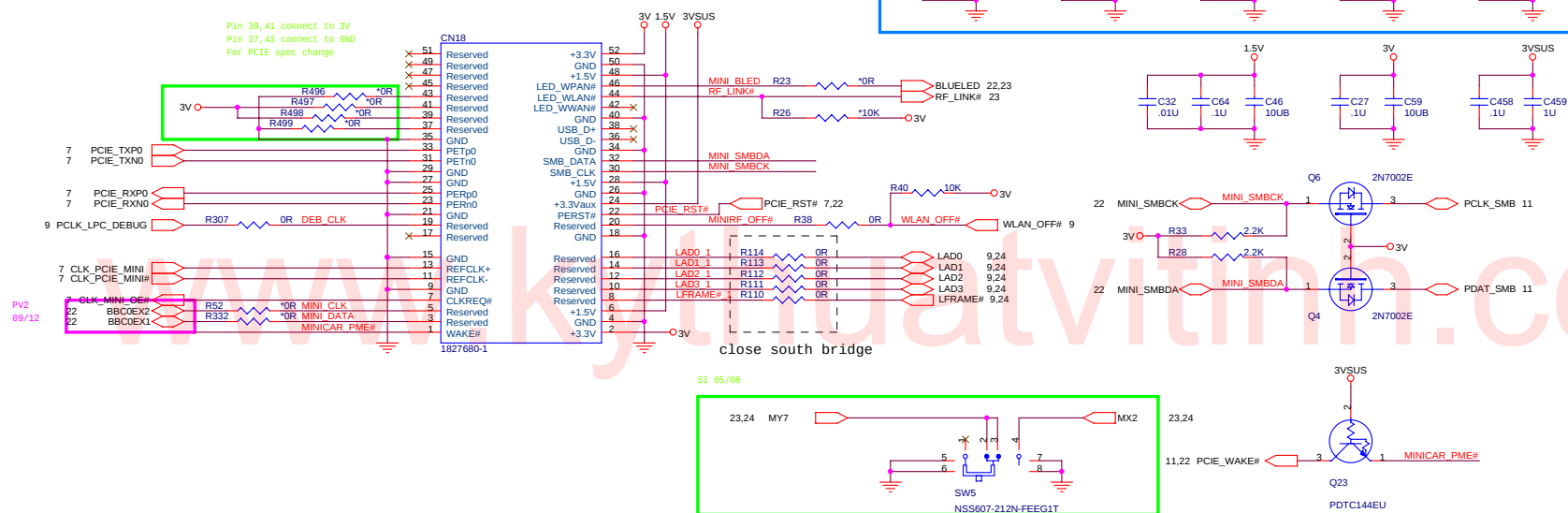
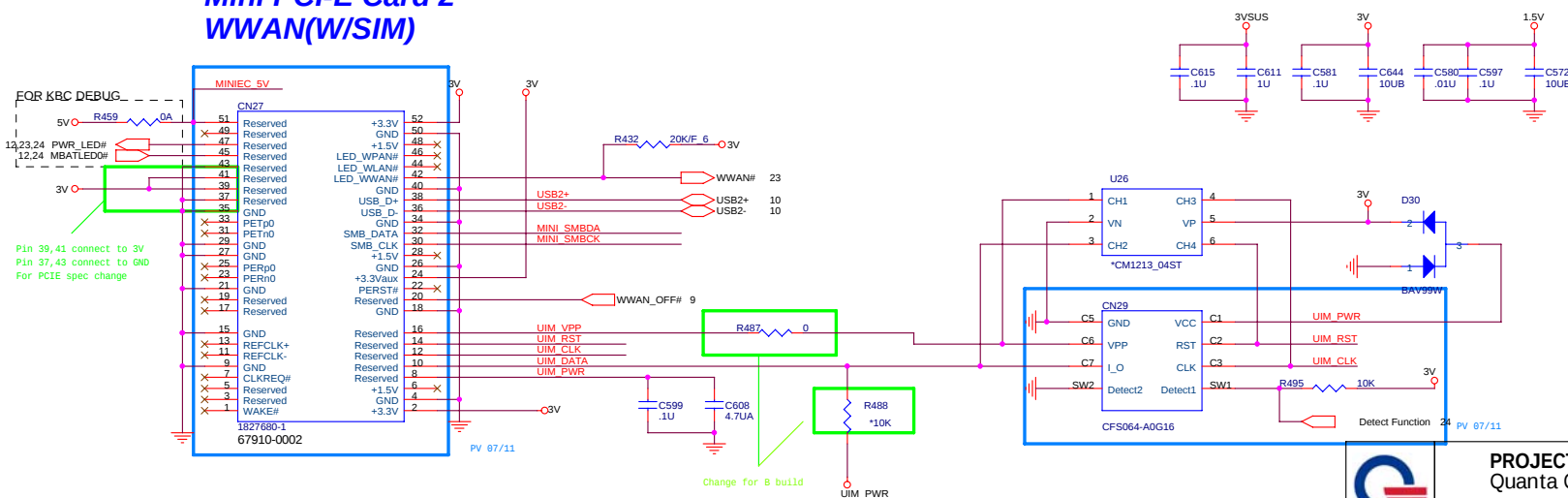
Size Custom	Document Number JACK, AMP_TPA0312	Rev 1A
Date: Friday, November 24, 2006	Sheet 19 of 36	



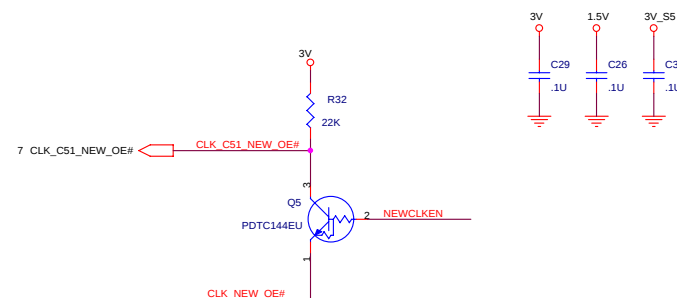
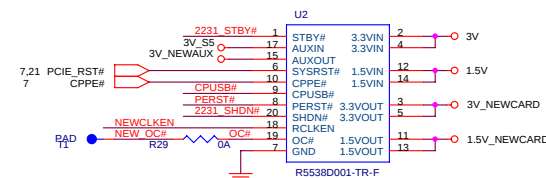
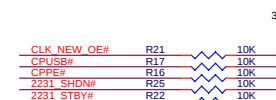
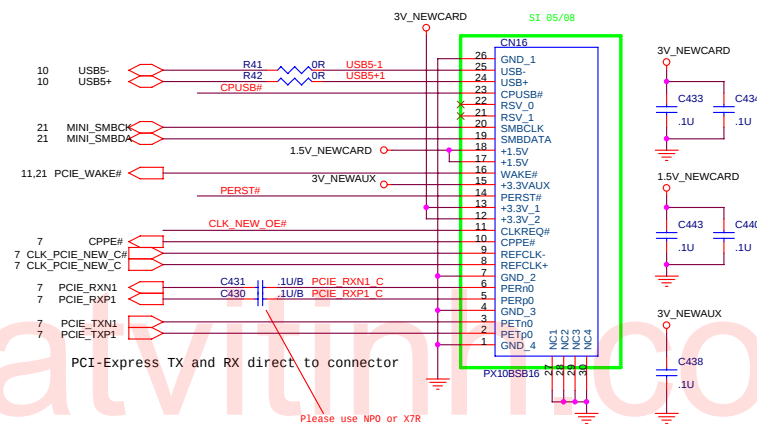
USB 1& 2



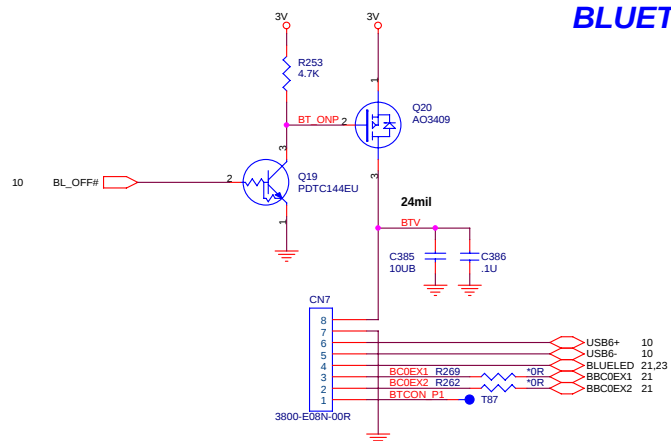
Mini PCI-E Card 1 WLAN

**Mini PCI-E Card 2**
WWAN(W/SIM)

NEWCARD



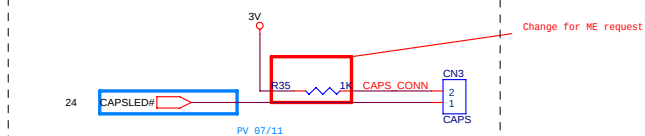
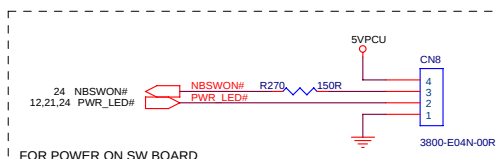
BLUETOOTH



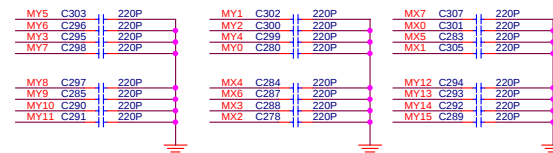
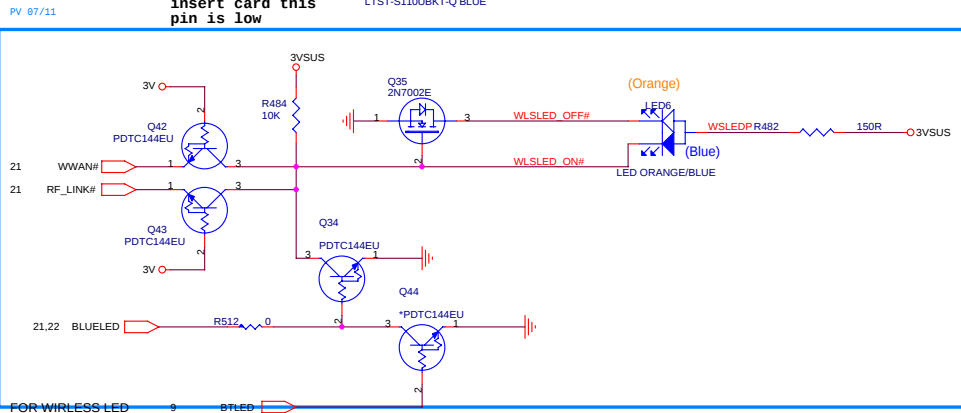
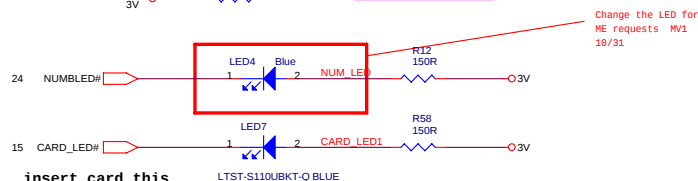
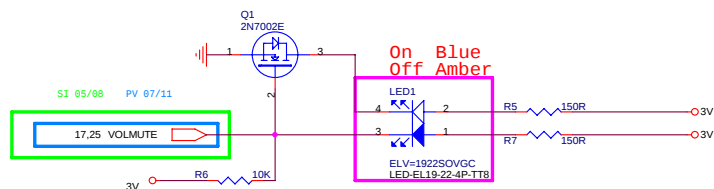
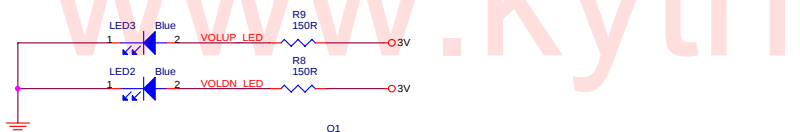
NBS/RD2/HW1

Size
CustomPROJECT : TT8
Quanta Computer Inc.Document Number
NEW CARD/BTRev
1A

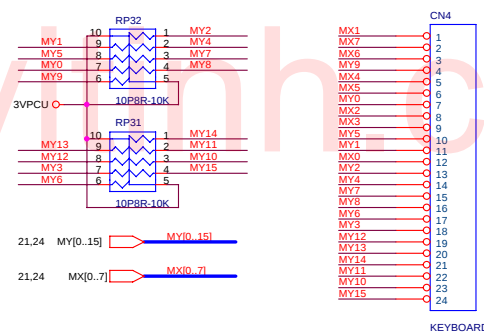
Date: Friday, November 24, 2006 Sheet 22 of 36



for caps lock LED board



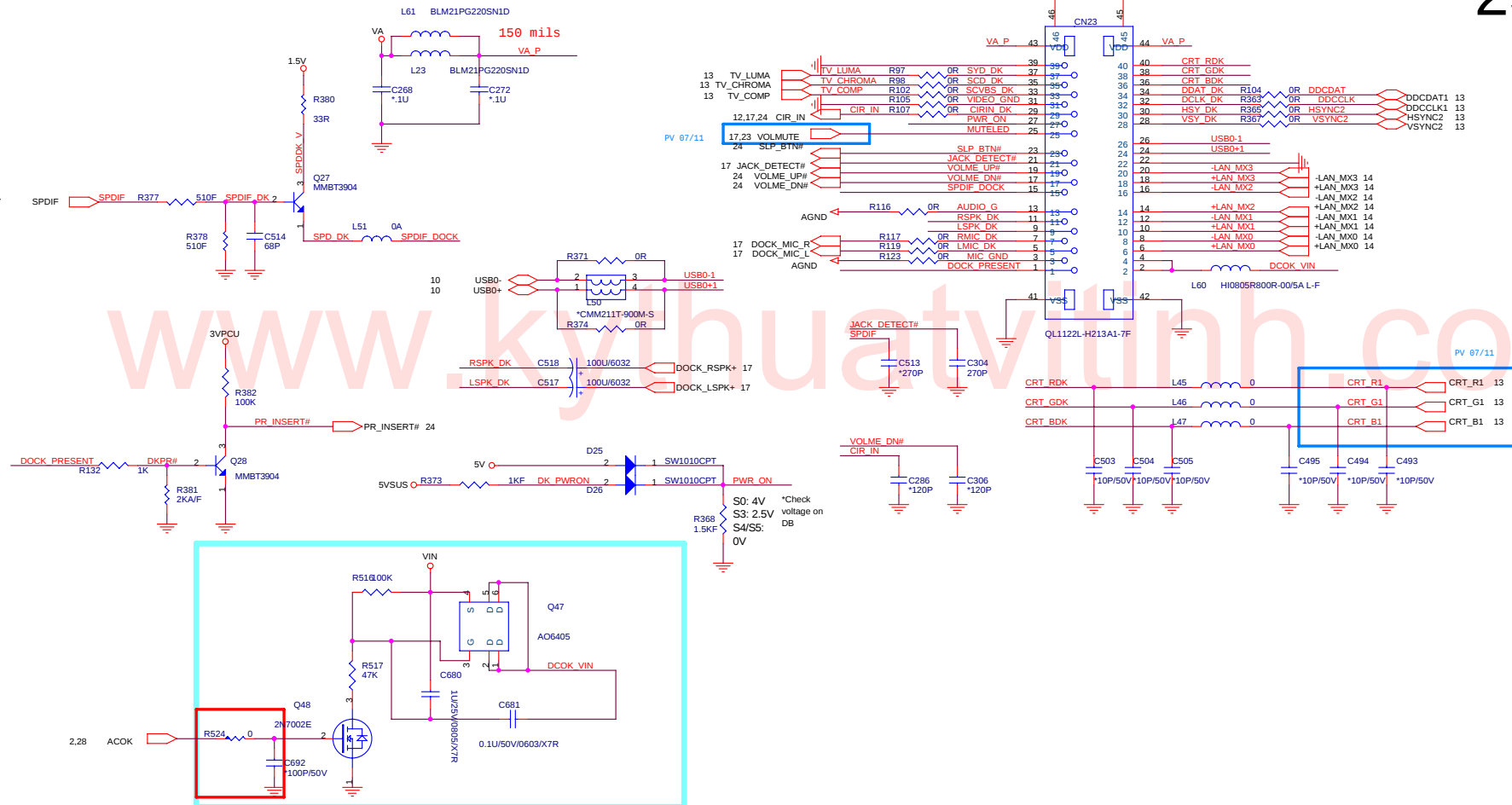
KEYBOARD PULL-UP



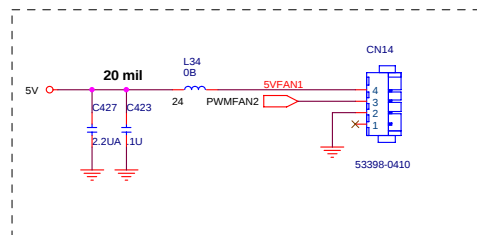
PROJECT : TT8
Quanta Computer Inc.

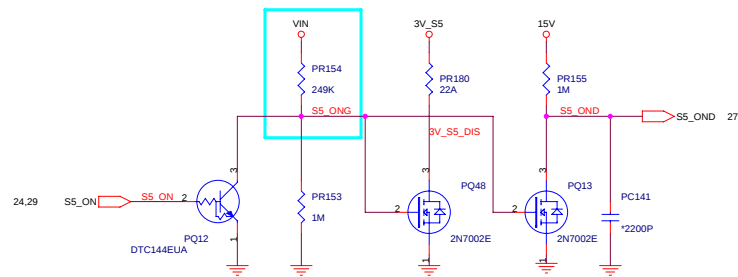
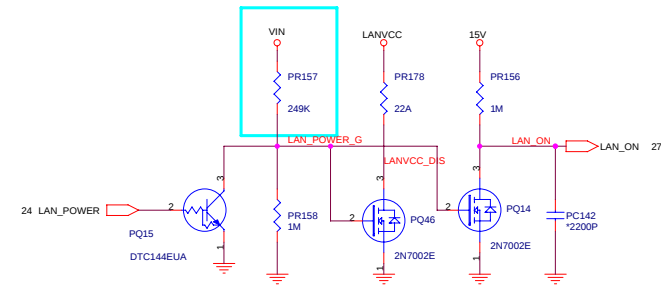
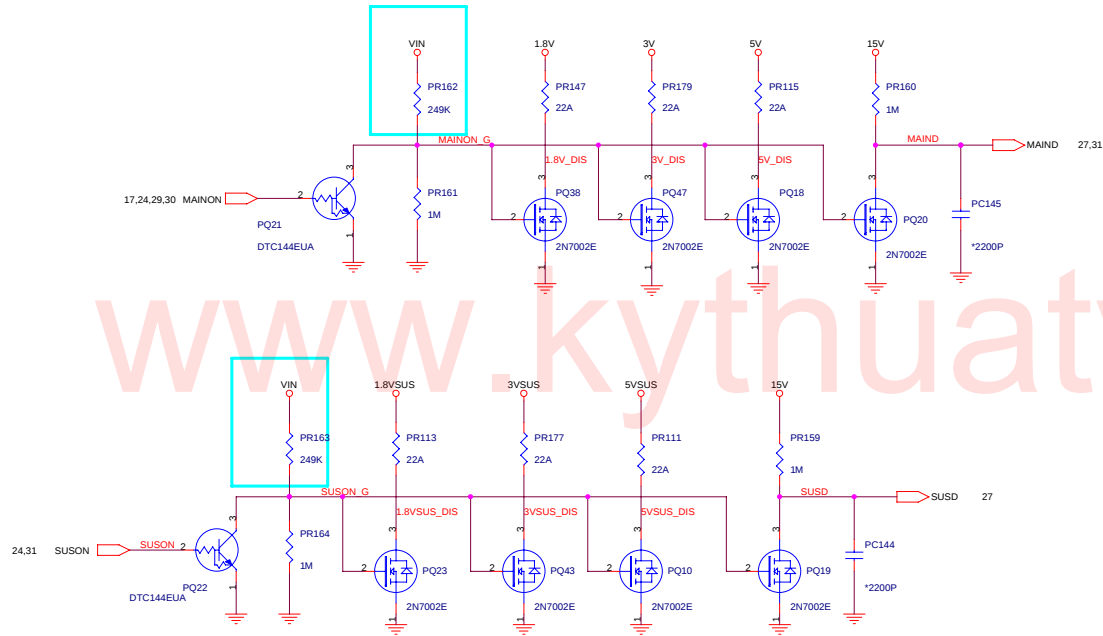
CABLE DOCK

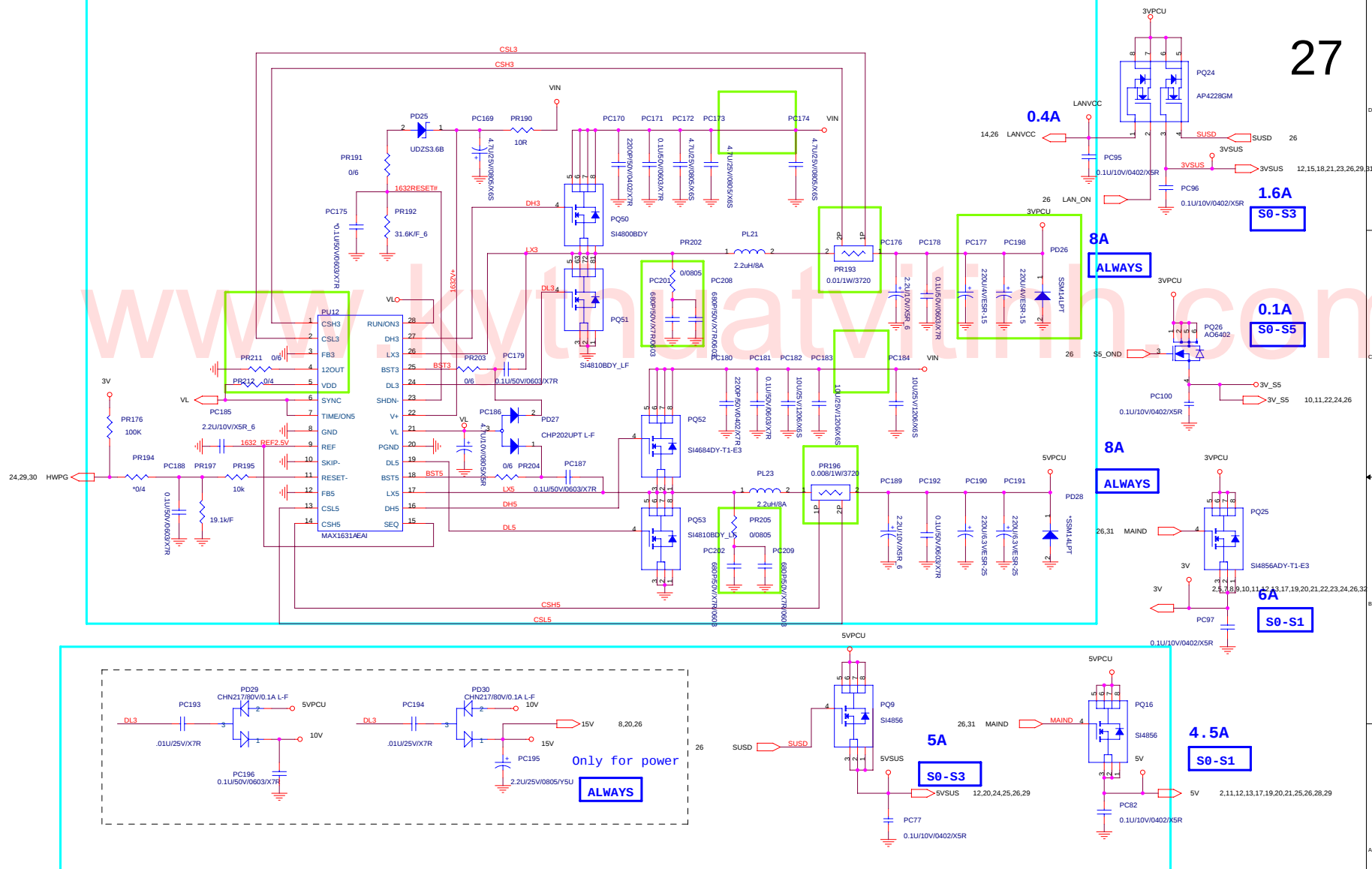
25



FAN



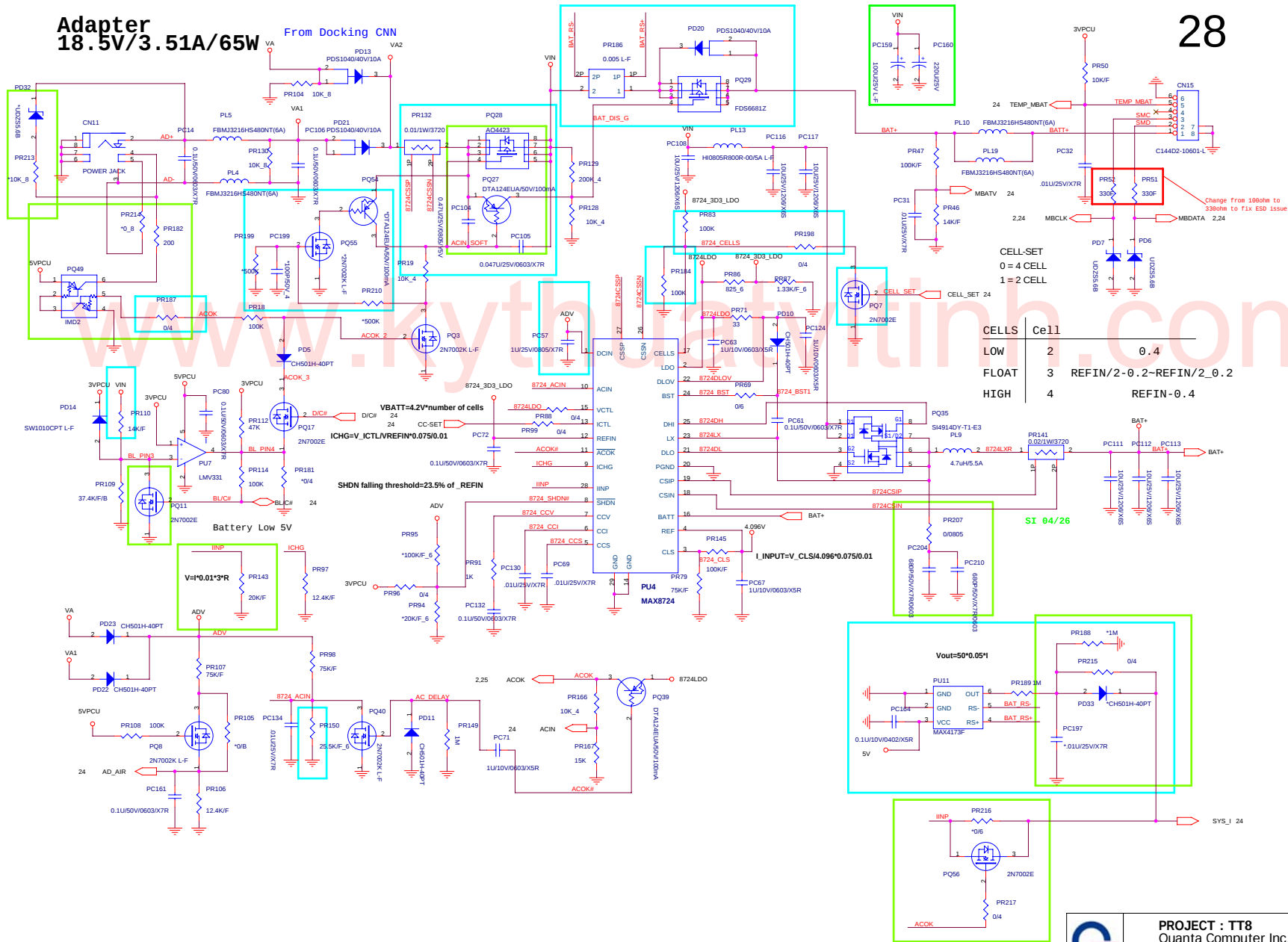


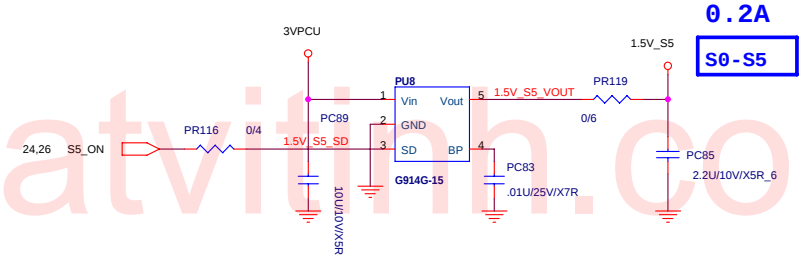
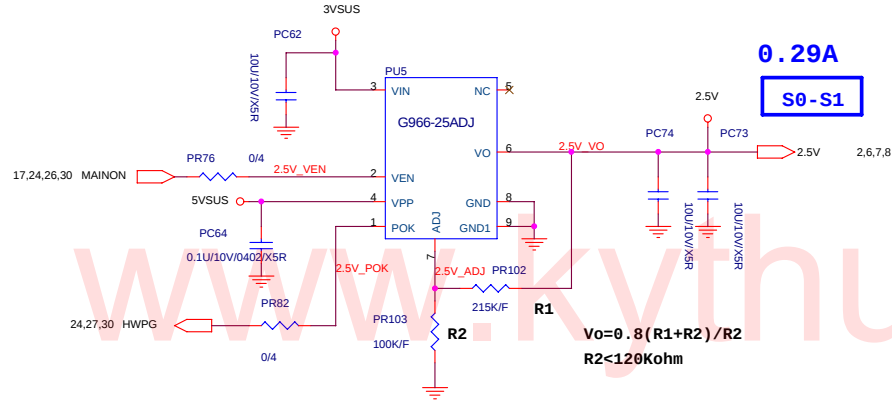


Adapter
18.5V/3.51A/65W

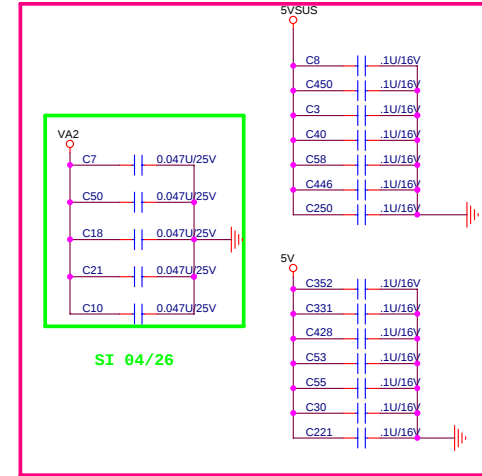
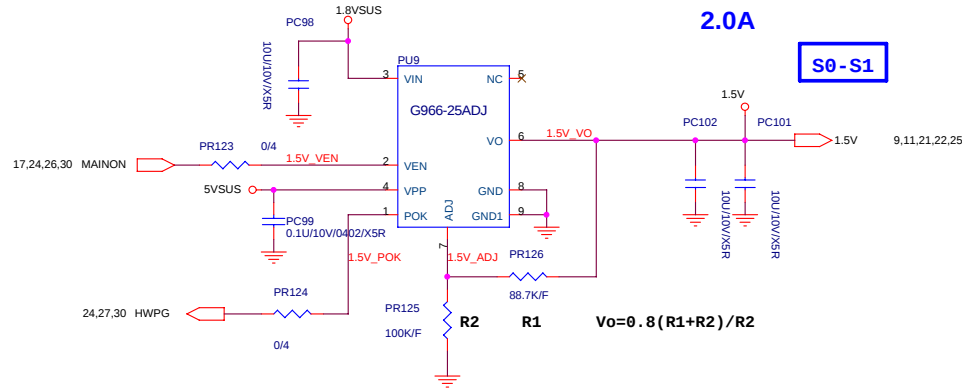
From Docking CNN

28





EMI



MAX1549

S0-S1

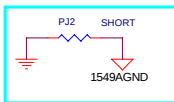
3A

$$V_{cs} = I_L(A) * L_{DCR}(m\Omega) = V_{ILIM}(mV) / 10$$

DCR 28m OHM

$$V_{out} = 0.5V(1 + R1/R2)$$

SI-2 modified



FBLANK			
VCC	OPEN	REF	GND
150us	100us	50us	blanking disabled
150us	100us	50us	100us

OU1 fault protection and PG01 blanking
OU1 forced-PWM transition operation

S0-S1

3.7A

$$V_{cs} = I_L(A) * L_{DCR}(m\Omega) = V_{ILIM}(mV) / 10$$

DCR 28m OHM

FSEL: VCC=400KHZ, open=300kHz

$$V_{out1} = 2.0V(REQ / (R_b + REQ))$$

INPUTS		OUTPUTS			REQ	VOUT1
G1	G0	OD1	OD2	OD3		
0	0	High-Z	High-Z	High-Z	Ra=150K	1.2V
1	0	0	High-Z	High-Z	Ra//R0D1=100.1K	1.0V
0	1	High-Z	0	High-Z	Ra//R0D2=122.4K	1.1V
1	1	High-Z	High-Z	0	Ra//R0D3=82.02K	



PROJECT : TT8
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	MAX1549 1.2V/1.2V_NB	
Date: Friday, November 24, 2006	Sheet 30	of 36



$\text{Slew rate} = (12.5\text{mV}/\mu\text{s}) * (71.5\text{K}/\text{R_TIME})$
 $\text{VFB} = \text{V_VID} + 0.125(\text{VREF} - \text{VOFS})$
 VRHOT is low when VTHRM below 1.5V
 $\text{Tsw} = 16.26\text{pF}(\text{R_TON} + 6.5\text{K})/\text{ohm}$
 $\text{CCV_CAP} = 470\text{pF} * (2/\text{total phase}) * 300\text{KHz}/\text{fsw}$

VCC_CORE MAX8774

32

OCP=44A
 VCC_CORE
 35A / 1.05V

DCR=1.1m/+ -5%

DCR=1.1m/+ -5%

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.550V	1	0	0	0	0	0	0.7425V
0	0	0	0	0	1	1.525V	1	0	0	0	0	1	0.7500V
0	0	0	0	1	0	1.500V	1	0	0	0	1	0	0.7375V
0	0	0	0	1	1	1.475V	1	0	0	0	1	1	0.7250V
0	0	0	1	0	0	1.450V	1	0	0	1	0	0	0.7125V
0	0	0	1	0	1	1.425V	1	0	0	1	0	1	0.7000V
0	0	0	1	1	0	1.400V	1	0	0	1	1	0	0.6875V
0	0	0	1	1	1	1.375V	1	0	0	1	1	1	0.6750V
0	0	1	0	0	0	1.350V	1	0	1	0	0	0	0.6625V
0	0	1	0	0	1	1.325V	1	0	1	0	0	1	0.6500V
0	0	1	0	1	0	1.300V	1	0	1	0	1	0	0.6375V
0	0	1	0	1	1	1.275V	1	0	1	0	1	1	0.6250V
0	0	1	1	0	0	1.250V	1	0	1	1	0	0	0.6125V
0	0	1	1	0	1	1.225V	1	0	1	1	0	1	0.6000V
0	0	1	1	1	0	1.200V	1	0	1	1	1	0	0.5875V
0	0	1	1	1	1	1.175V	1	0	1	1	1	1	0.5750V
0	1	0	0	0	0	1.150V	1	1	0	0	0	0	0.5625V
0	1	0	0	0	1	1.125V	1	1	0	0	0	1	0.5500V
0	1	0	0	1	0	1.100V	1	1	0	0	1	0	0.5375V
0	1	0	0	1	1	1.075V	1	1	0	0	1	1	0.5250V
0	1	0	1	0	0	1.050V	1	1	0	1	0	0	0.5125V
0	1	0	1	0	1	1.025V	1	1	0	1	0	1	0.5000V
0	1	0	1	1	0	1.000V	1	1	0	1	1	0	0.4875V
0	1	0	1	1	1	0.975V	1	1	0	1	1	1	0.4750V
0	1	1	0	0	0	0.950V	1	1	1	0	0	0	0.4625V
0	1	1	0	0	1	0.925V	1	1	1	0	0	1	0.4500V
0	1	1	0	1	0	0.900V	1	1	1	0	1	0	0.4375V
0	1	1	0	1	1	0.875V	1	1	1	0	1	1	0.4250V
0	1	1	1	0	0	0.850V	1	1	1	1	0	0	0.4125V
0	1	1	1	0	1	0.825V	1	1	1	1	0	1	0.4000V
0	1	1	1	1	0	0.800V	1	1	1	1	1	0	0.3875V
0	1	1	1	1	1	0.775V	1	1	1	1	1	1	0.3750V



PROJECT : TT8
 Quanta Computer Inc.

Size Custom
 Document Number MAX8774 VCC_CORE
 Date: Friday, November 24, 2006 Sheet 32 of 36
 Rev 1A

MODEL	DB1 --->SI1	CHANGE LIST	Model	OT1 MB BOARD	
			Page	FROM	TO
TT8 MB 31TT8MB0006	4/17 - 4/20	1.Change Audio port and senser pin resistor. Internal MIC change from Pin14,15 to Pin16,17 Docking Mic Change from Pin16,17 to Pin14,15 Docking spk change from Pin23,24 to Pin 43,44 Swap Pin30 and Pin31 Change R486 from Pin 13 to Pin 34 and change from 5.1KK to 10K Change R251 10K to R485 5.1K 2.Change WWAN and WLAN Pin define Add R487 and R488 3.Change TEMP Control chip for leakage, Change Q9 and Q10 to BAM70020074 4.Change HDD connector type, RJ45/CRT connector footprint 5.Swap LCD connector singnal from machine require 6.Swap U5 CRT/TV singnal from nVIDIA require 7.Change battery and D30 footprint 8.Change C251,C242,C138,C66,C71,C276,C277 footprint from 0603 to 0402 9.Add Q36,Q37,R489,C661,R490 for Docking MIC detect 10.Change SW5 and CN8 footprint for machinecal request 11.Change L41 to PB201209T-300Y-N (Footprint : 0805) 12.Delect H3 and H4 for machinecal change 13.Change C20 from 0.1U to 1U (Fix LCD rise time) 14.Move Net "SLP_BTN#" from pin99 to pin87 15.Modify Docking mute LED circuit 16.Modify U25 SCI# signal from BIOS request, AddR491,R492 17.Modify Buletooth switch and ODD BAYINS# to EC 18.Change caps lock connector footprint from machencal request 19.Add U30,R495,R494,R493,Q38 for reserve SIM card 20.Change 4-in-1 card footprint 21.Add R44,R43,R48 Remove R62,R64,R69,R34,R24,R36 22.Change L45,L46,L47 to 0 ohm Del C503,C504,C505,C493,C494,C495 for D-SUB function	1	1A	
			2	1A	
			3	1A	
			4	1A	
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	1A	
			11	1A	
			12	1A	
			13	1A	
			14	1A	
			15	1A	
			16	1A	
			17	1A	
			18	1A	
			19	1A	
			20	1A	
			21	1A	
			22	1A	
			23	1A	
			24	1A	
			25	1A	
			26	1A	
			27	1A	
			28	1A	
			29	1A	
			30	1A	
			31	1A	
			32	1A	
			33	1A	



PROJECT : TT8
Quanta Computer Inc.

Size Custom

Document Number
--> SI** Change history

Rev 1A

NBS /RD2 /HW1

Date: Friday, November 24, 2006

Sheet 33 of 36

MODEL		CHANGE LIST	OT1 MB BOARD	
SI1 ---->PV1	Page		FROM	TO
TT8 MB 31TT8MB0006	5/17 - 7/11	1.Exchange Audio port External MIC Exchange Pin22 and Pin21 CD Line Exchange Pin18 and Pin20 Internal MIC Exchange Pin16 and Pin17 Docking Mic Exchange Pin14 and Pin15	1	1A
		3.Change R478 from 22ohm to 0ohm	2	1A
		4.Change R462 0ohm to C666 0.47u for Audio chip distortion	3	1A
		5.Exchange R272 and R263, R273 and R264 for amplifier gain change	4	1A
		6.Change Q8 from BAM51030Z15 to BAM23010Z30 for Rdson issue	5	1A
		7.Remove C439 for MS pro card can not detect	6	1A
		8.Add C667,C668,C669,C670,C671,C672,C673,C674,C675,C676 for WLAN con not detect issue	7	1A
		9.Add reverse circuit for LED issue	8	1A
		10.Delect Q7 for Cap lock LED	9	1A
		11.Add EMI Cap C93,C118,C496,C497,C499,C566,C589,C555,C334,C337	10	1A
		12.Change CN19,CN27,CN28,CN29 footprint	11	1A
		14.Change Sim connector (Add detect pin)	12	1A
		15.Move Docking CRT signal after PI circuit	13	1A
		16.Add R500, R501 for Audio chip function	14	1A
		17.Add D37 and R502 for nVIDIA solution	15	1A
		18.Move D22 from +5VCRT to +5VCRT3	16	1A
		19.Change Docking detect circuit	17	1A
		20.Delet H20 H21	18	1A
		21.Exchange MINI_DATA and MINI_CLK	19	1A
		22.Add Diode for SATA and ODD LED control	20	1A
		23.Add power controller for 5V shutdown	21	1A
		24.Change WLAN LED circuit	22	1A
		25.Add Res for ACZ signal	23	1A
		26.Delete H7 and H14 for ME change	24	1A
		27.Modify SB to Audio and Modem signal	25	1A
			26	1A
			27	1A
			28	1A
			29	1A
			30	1A
			31	1A
			32	1A
			33	1A



NBS / RD2 / HW1

Size Custom

PROJECT : TT8

Quanta Computer Inc.

Document Number
--> SI** Change history

Date: Friday, November 24, 2006

Rev 1A

Sheet 34 of 36

MODEL		CHANGE LIST	Model	OT1 MB BOARD	
			Page	FROM	TO
TT8 MB 31TT8MB0006	PV1 ---->PV2 9/8-10/17	1.Page17 change voltage from +3V to 3V fix the Mic can not work 2.Page17 change R14 from 4.7K to 5.6K to fix LCCVDD rise time 3.Page17 change LCD cable Pin22 and Pin15 for switch function, Pin7 change to 32K_BTN 4.Page24 add GPIO for switch function 5.Page10 Change cap from 18p to 22p 6.Page17 Change C392 and C395 from 10U to 1U to fix Docking noise 7.Page16 add PA11(EMI spring) 8.Page21 Exchange BBC0EX1 and BBC0EX2 9.Page20 remove C614, C607, C406, C414, C404, C405 10.Page20 Change C635, C415, C416 from TAN to ELEC 11.Page11 Del R205 and Add R207 for Bios check	1	1A	
			2	1A	
			3	1A	
			4	1A	
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	1A	
			11	1A	
			12	1A	
			13	1A	
			14	1A	
			15	1A	
			16	1A	
			17	1A	
			18	1A	
			19	1A	
			20	1A	
			21	1A	
			22	1A	
			23	1A	
			24	1A	
			25	1A	
			26	1A	
			27	1A	
			28	1A	
			29	1A	
			30	1A	
			31	1A	
			32	1A	
			33	1A	
 NBS / RD2 / HW1 PROJECT : TT8 Quanta Computer Inc. Size Custom Document Number --> SI** Change history Date: Friday, November 24, 2006 Sheet 35 of 36 Rev 1A					

MODEL		CHANGE LIST	Model	OT1 MB BOARD	
			Page	FROM	TO
TT8 MB 31TT8MB0006	PV2 ---->MV1 10/17-11/15	1.Page10 Exchange USB0+/- with USB3+/- signal 2.Page12 Change CN12 Pin1 from 5VSUS to 3V 3.Page17 Change C648 and C656 from 4.7U to 22U to fix Vista issue 4.Page19 Change L35~L38 from LZA10-2ACB104MT to BK1608HS241-T 5.Page19 Change Gain from 15.6db to 10db 6.Page17 Del R260,R267,D312,D322 for Docking MIC 7.Page17 ADD R520,R521,R522,R523 for Docking MIC 8.Page21 Change PR51 PR52 from 100ohm to 330ohm to fix ESD issue 9.Page20 unstuff R188 to fix ODD problem 10.Page11 Change the board ID1 from low to high 11.Page15 Change Cap (C60,C56,C441,C44,C45)from 0.1u to 1u 12.Page15 Change Res (R318,R313,R312)from 39K to 10K 13.Page17 Add 0.01u(C693, C694) to fix high frequency problem 14.Page14 remove the cap(C408,C409) from MV build 15.Page7 Reserve C696 for nVIDIA 16.Page15 Reserve R525 and C695 for 3VSUS drop 17.Page23 Change LED4 for ME requests	1	1A	
			2	1A	
			3	1A	
			4	1A	
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	1A	
			11	1A	
			12	1A	
			13	1A	
			14	1A	
			15	1A	
			16	1A	
			17	1A	
			18	1A	
			19	1A	
			20	1A	
			21	1A	
			22	1A	
			23	1A	
			24	1A	
			25	1A	
			26	1A	
			27	1A	
			28	1A	
			29	1A	
			30	1A	
			31	1A	
			32	1A	
			33	1A	
 NBS /RD2 /HW1 PROJECT : TT8 Quanta Computer Inc. Size Custom Document Number --> SI** Change history Date: Friday, November 24, 2006 Rev 1A Sheet 35 of 36					