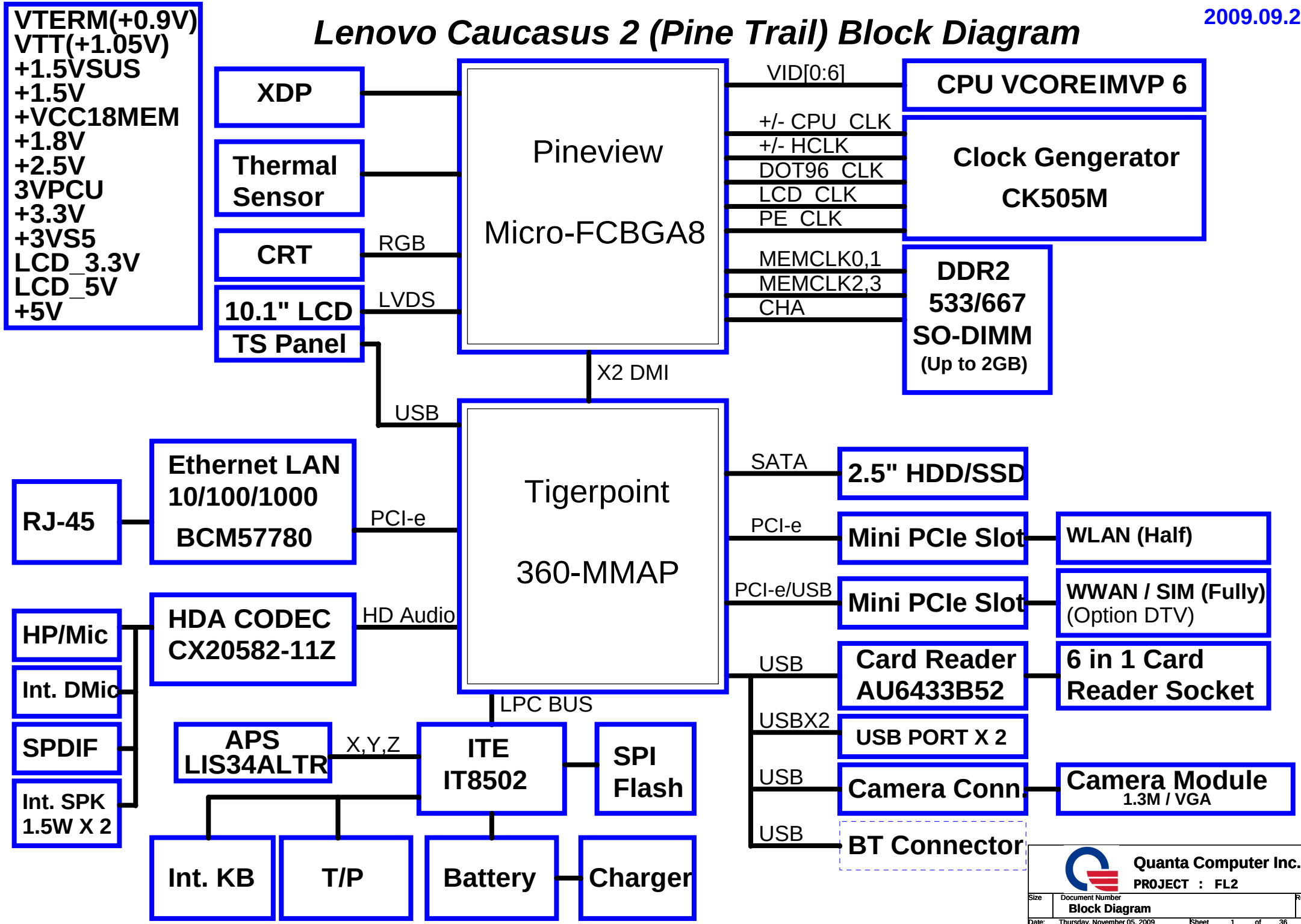
Lenovo Caucasus 2 (Pine Trail) Block Diagram

2009.09.28.



hexainf@hotmail.com

Table of Contents

PAGE	DESCRIPTION
1	Schematic Block Diagram
2	

Voltage Rails & Power States

POWER PLANE	DESCRIPTION	VOLTAGE	CONTROL SIGNAL	S0	S3	S4	S5
VA	Adapter Power Pulg In	20V		Y	Y	Y	Y
VBAT	Battery Power	12V ~ 10V		Y	Y	Y	Y
VIN	System Power (Adapter or Battery Power)	10V ~ 20V		Y	Y	Y	Y
5VPCU	System Always Power	5V	PWM IC	Y	Y	Y	Y
3VPCU	System Always Power	3.3V	PWM IC	Y	Y	Y	Y
+5V_S5	System Aux Power (Wake Up On LAN)	5V	S5_ON	Y	Y	N /(Y)	N /(Y)
+3V_S5	System Aux Power (Wake Up On LAN)	3.3V	S5_ON	Y	Y	N /(Y)	N /(Y)
+5VSUS	System Aux Power	5V	SUS_ON	Y	Y	N	N
+3VSUS	System Aux Power	3.3V	SUS_ON	Y	Y	N	N
+5V	System Normal Power	5V	Main_ON	Y	N	N	N
+3V	System Normal Power	3.3V	Main_ON	Y	N	N	N

GND PLANE	PAGE	DESCRIPTION
GND	ALL	

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PROJECT : FL2

Size	Document Number	Rev
	POWER MANAGER	1A

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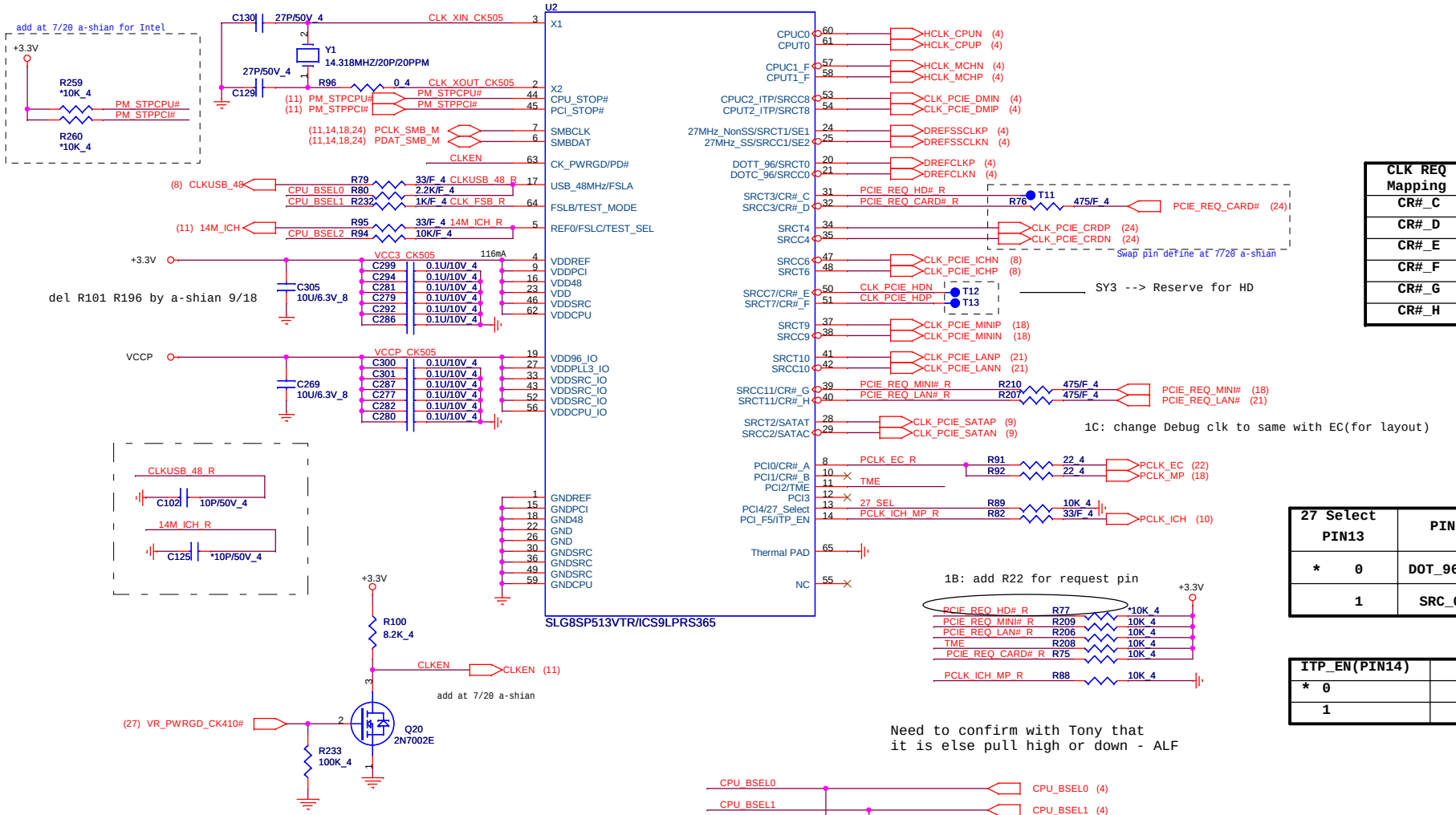

CLK REQ Mapping	REQ Mapping
CR#_C	SRC_0 or SRC_2
CR#_D	LCCLK or SRC_4
CR#_E	SRC_6
CR#_F	SRC_8
CR#_G	SRC_9
CR#_H	SRC_10

27 Select PIN13	PIN 20/21	PIN 24/25
* 0	DOT_96 / DOT_96#	LCDCLK / LCDCLK#
1	SRC_0 / SRC_0#	27M / 27M_SS

ITP_EN(PIN14)	PIN53/54
* 0	SRC8#/SRC8
1	ITP/ITP#

FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
0	1	0	200.00	100	33.33	14.318	48	96	0.5 Down
0	1	1	**166.66**	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	RESERVED						

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PROJECT : FL2

Size	Document Number	Rev
	Clock Gen SLG8SP513VTR	1A

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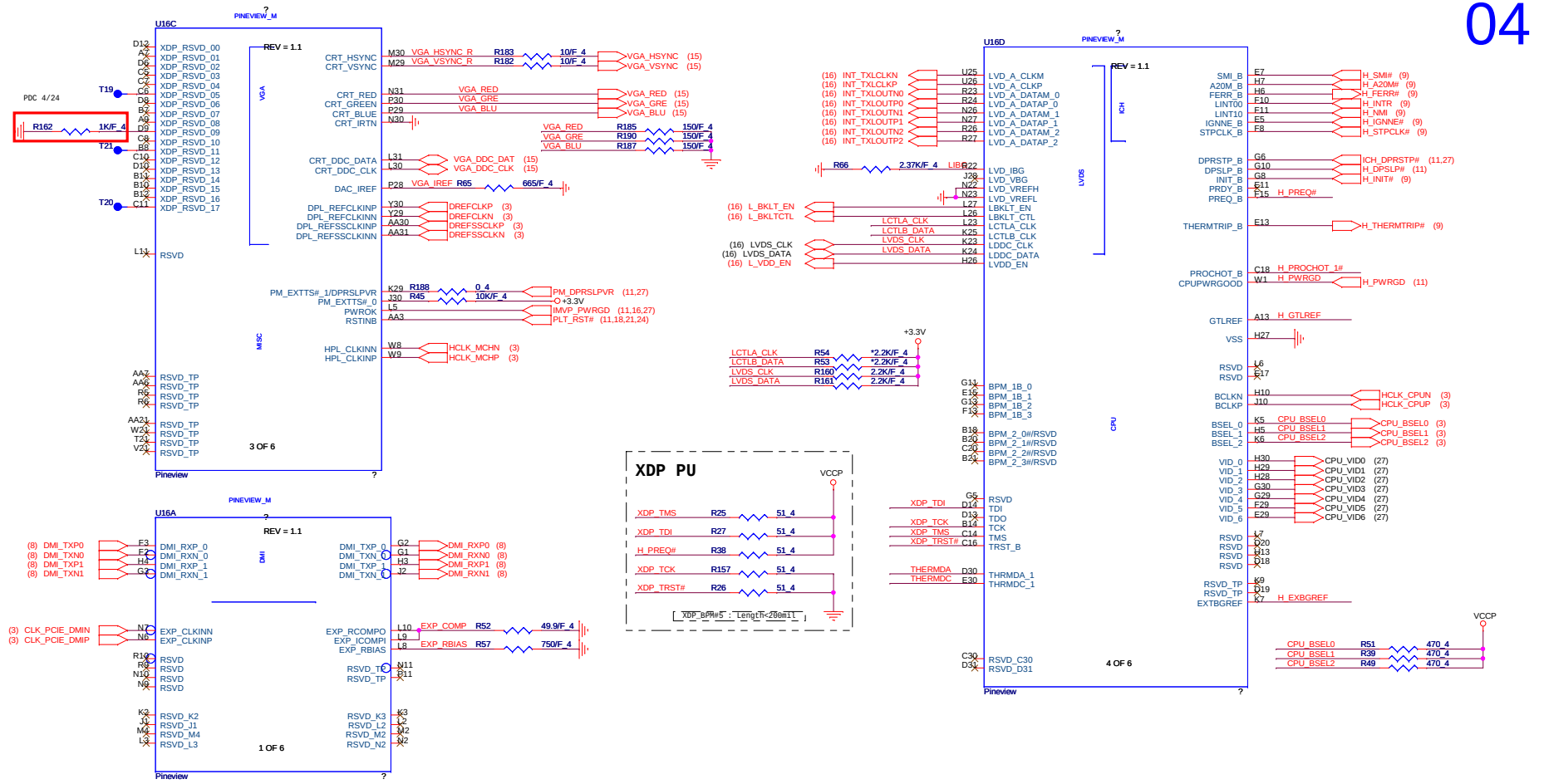
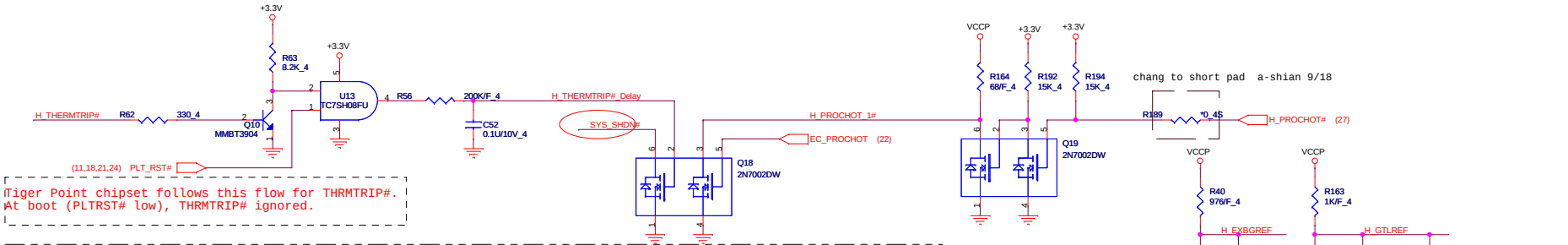
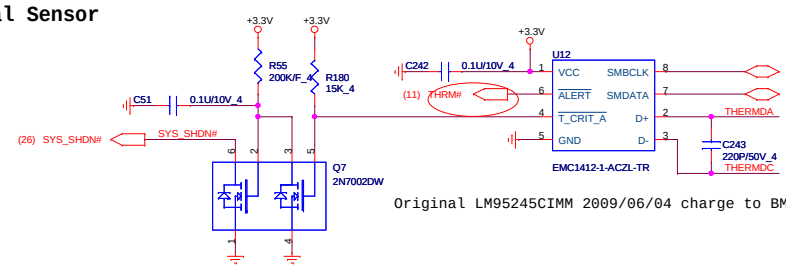




Tiger Point chipset follows this flow for THRMTRIP#.
At boot (PLTRST# low), THRMTRIP# ignored.

Thermal Sensor



Original LM95245CIMM 2009/06/04 charge to BMC1412-1-ACZL-TR

Themal I2C

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PROJECT : FL2

Size	Document Number	Rev
	Pineview DMI/Display	1A
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PINEVIEW_M

U16B REV = 1.1

(14) M_A_A[14..0]

M_A_A0	AH19	DDR_A_MA_0
M_A_A1	AJ18	DDR_A_MA_1
M_A_A2	AK18	DDR_A_MA_2
M_A_A3	AK16	DDR_A_MA_3
M_A_A4	AJ14	DDR_A_MA_4
M_A_A5	AH14	DDR_A_MA_5
M_A_A6	AK14	DDR_A_MA_6
M_A_A7	AJ12	DDR_A_MA_7
M_A_A8	AH13	DDR_A_MA_8
M_A_A9	AK12	DDR_A_MA_9
M_A_A10	AK20	DDR_A_MA_10
M_A_A11	AH12	DDR_A_MA_11
M_A_A12	AJ11	DDR_A_MA_12
M_A_A13	AJ24	DDR_A_MA_13
M_A_A14	AJ10	DDR_A_MA_14

(14) M_A_WE#
(14) M_A_CAS#
(14) M_A_RAS#

M_A_WE#	AK22	DDR_A_WEB
M_A_CAS#	AJ22	DDR_A_CASB
M_A_RAS#	AK21	DDR_A_RASB

(14) M_A_BS0
(14) M_A_BS1
(14) M_A_BS2

M_A_BS0	AJ20	DDR_A_BS_0
M_A_BS1	AH20	DDR_A_BS_1
M_A_BS2	AK11	DDR_A_BS_2

(14) M_CS#0
(14) M_CS#1

M_CS#0	AH22	DDR_A_CSB_0
M_CS#1	AK25	DDR_A_CSB_1
	AJ21	DDR_A_CSB_2
	AJ25	DDR_A_CSB_3

(14) M_CKE0
(14) M_CKE1

M_CKE0	AH10	DDR_A_CKE_0
M_CKE1	AH9	DDR_A_CKE_1
	AK10	DDR_A_CKE_2
	AJ9	DDR_A_CKE_3

(14) M_ODT0
(14) M_ODT1

M_ODT0	AK24	DDR_A_ODT_0
M_ODT1	AH26	DDR_A_ODT_1
	AH24	DDR_A_ODT_2
	AK27	DDR_A_ODT_3

(14) M_CLK0
(14) M_CLK#0
(14) M_CLK1
(14) M_CLK#1

M_CLK0	AG15	DDR_A_CK_0
M_CLK#0	AF15	DDR_A_CKB_0
M_CLK1	AD13	DDR_A_CK_1
M_CLK#1	AC13	DDR_A_CKB_1
	AC15	DDR_A_CK_3
	AD15	DDR_A_CKB_3
	AF13	DDR_A_CK_4
	AG13	DDR_A_CKB_4
	AD17	RSVD_AD17
	AC17	RSVD_AC17
	AB15	RSVD_AB15
	AB17	RSVD_AB17

1C: reserve for ES1(WW10 MOW)

1.8VSUS R86 10K/F_4 AB4 VSS
R81 *10K/F_4 AK8 RSVD

change valume 0.01 to 0.1 at 7/20 a-shian

C297 0.1U/10V_4 AB11 RSVD_TP
AB13 RSVD_TP
DDR_VREF_P AL28 DDR_VREF
1.8VSUS R230 80.6/F_4 SM_RCOMP AK28 DDR_RPD
R226 80.6/F_4 SM_RCOMP# AJ26 DDR_RPU
C296 0.01U/25V_4 AK29 RSVD

DDR_A

1.8VSUS
R227 1K/F_4
(14,28) SMVREF_GMCH R228 *0_4 DDR_VREF_P
R229 1K/F_4

1D: add optional power for DDR_VREF(CRB)

DDR_A_DQSB_0	AD3	M_A_DQS0
	AD2	M_A_DQS#0
DDR_A_DM_0	AD4	M_A_DM0
DDR_A_DQ_0	AC4	M_A_DQ0
DDR_A_DQ_1	AC1	M_A_DQ1
DDR_A_DQ_2	AF4	M_A_DQ2
DDR_A_DQ_3	AG2	M_A_DQ3
DDR_A_DQ_4	AB2	M_A_DQ4
DDR_A_DQ_5	AB3	M_A_DQ5
DDR_A_DQ_6	AE2	M_A_DQ6
DDR_A_DQ_7	AF3	M_A_DQ7
DDR_A_DQSB_1	AB8	M_A_DQS1
	AD7	M_A_DQS#1
DDR_A_DM_1	AA9	M_A_DM1
DDR_A_DQ_8	AB6	M_A_DQ8
DDR_A_DQ_9	AB7	M_A_DQ9
DDR_A_DQ_10	AE5	M_A_DQ10
DDR_A_DQ_11	AG5	M_A_DQ11
DDR_A_DQ_12	AA5	M_A_DQ12
DDR_A_DQ_13	AB5	M_A_DQ13
DDR_A_DQ_14	AB9	M_A_DQ14
DDR_A_DQ_15	AD6	M_A_DQ15
DDR_A_DQSB_2	AD8	M_A_DQS2
	AD10	M_A_DQS#2
DDR_A_DM_2	AE8	M_A_DM2
DDR_A_DQ_16	AG8	M_A_DQ16
DDR_A_DQ_17	AG7	M_A_DQ17
DDR_A_DQ_18	AE10	M_A_DQ18
DDR_A_DQ_19	AG11	M_A_DQ19
DDR_A_DQ_20	AF7	M_A_DQ20
DDR_A_DQ_21	AF8	M_A_DQ21
DDR_A_DQ_22	AD11	M_A_DQ22
DDR_A_DQ_23	AE10	M_A_DQ23
DDR_A_DQSB_3	AK5	M_A_DQS3
	AK3	M_A_DQS#3
DDR_A_DM_3	AJ3	M_A_DM3
DDR_A_DQ_24	AH1	M_A_DQ24
DDR_A_DQ_25	AJ2	M_A_DQ25
DDR_A_DQ_26	AK6	M_A_DQ26
DDR_A_DQ_27	AJ7	M_A_DQ27
DDR_A_DQ_28	AF3	M_A_DQ28
DDR_A_DQ_29	AH2	M_A_DQ29
DDR_A_DQ_30	AL5	M_A_DQ30
DDR_A_DQ_31	AJ6	M_A_DQ31
DDR_A_DQSB_4	AG22	M_A_DQS4
	AG21	M_A_DQS#4
DDR_A_DM_4	AD19	M_A_DM4
DDR_A_DQ_32	AE19	M_A_DQ32
DDR_A_DQ_33	AG19	M_A_DQ33
DDR_A_DQ_34	AF22	M_A_DQ34
DDR_A_DQ_35	AD22	M_A_DQ35
DDR_A_DQ_36	AG17	M_A_DQ36
DDR_A_DQ_37	AF19	M_A_DQ37
DDR_A_DQ_38	AE21	M_A_DQ38
DDR_A_DQ_39	AD21	M_A_DQ39
DDR_A_DQSB_5	AE26	M_A_DQS5
	AG27	M_A_DQS#5
DDR_A_DM_5	AJ27	M_A_DM5
DDR_A_DQ_40	AE24	M_A_DQ40
DDR_A_DQ_41	AG25	M_A_DQ41
DDR_A_DQ_42	AD25	M_A_DQ42
DDR_A_DQ_43	AD24	M_A_DQ43
DDR_A_DQ_44	AC22	M_A_DQ44
DDR_A_DQ_45	AG24	M_A_DQ45
DDR_A_DQ_46	AD27	M_A_DQ46
DDR_A_DQ_47	AE27	M_A_DQ47
DDR_A_DQSB_6	AE30	M_A_DQS6
	AE29	M_A_DQS#6
DDR_A_DM_6	AE30	M_A_DM6
DDR_A_DQ_48	AG31	M_A_DQ48
DDR_A_DQ_49	AG30	M_A_DQ49
DDR_A_DQ_50	AD30	M_A_DQ50
DDR_A_DQ_51	AD29	M_A_DQ51
DDR_A_DQ_52	AJ30	M_A_DQ52
DDR_A_DQ_53	AJ29	M_A_DQ53
DDR_A_DQ_54	AE29	M_A_DQ54
DDR_A_DQ_55	AD28	M_A_DQ55
DDR_A_DQSB_7	AB27	M_A_DQS7
	AA27	M_A_DQS#7
DDR_A_DM_7	AB26	M_A_DM7
DDR_A_DQ_56	AA24	M_A_DQ56
DDR_A_DQ_57	AB25	M_A_DQ57
DDR_A_DQ_58	W24	M_A_DQ58
DDR_A_DQ_59	W22	M_A_DQ59
DDR_A_DQ_60	AB24	M_A_DQ60
DDR_A_DQ_61	AB23	M_A_DQ61
DDR_A_DQ_62	AA23	M_A_DQ62
DDR_A_DQ_63	W27	M_A_DQ63

2 OF 6

Pineview

M_A_DQ[63..0] (14)
M_A_DM[7..0] (14)
M_A_DQS[7..0] (14)
M_A_DQS#[7..0] (14)

VTT_MEM

M_A_A10	RN4	1 2	47X4_4
M_A_A2		3 4	
M_A_A0		5 6	
M_A_A5		7 8	
M_A_A8	RN6	1 2	47X4_4
M_A_A14		3 4	
M_A_A11		5 6	
M_A_A9		7 8	
M_A_A6	RN5	1 2	47X4_4
M_A_A4		3 4	
M_A_A3		5 6	
M_A_A7		7 8	
M_CS#0	RN2	1 2	47X4_4
M_ODT0		3 4	
M_A_A13		5 6	
M_A_WE#		7 8	
M_A_RAS#	RN3	1 2	47X4_4
M_A_BS0		3 4	
M_A_BS1		5 6	
M_A_A1		7 8	
M_A_A12	RN7	1 2	47X4_4
M_CKE1		3 4	
M_A_BS2		5 6	
M_CKE0		7 8	
M_ODT1	RN1	1 2	47X4_4
M_A_CAS#		3 4	
M_CS#1		5 6	
		7 8	

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PROJECT : FL2

Size	Document Number	Rev
	Pineview DDR	1A

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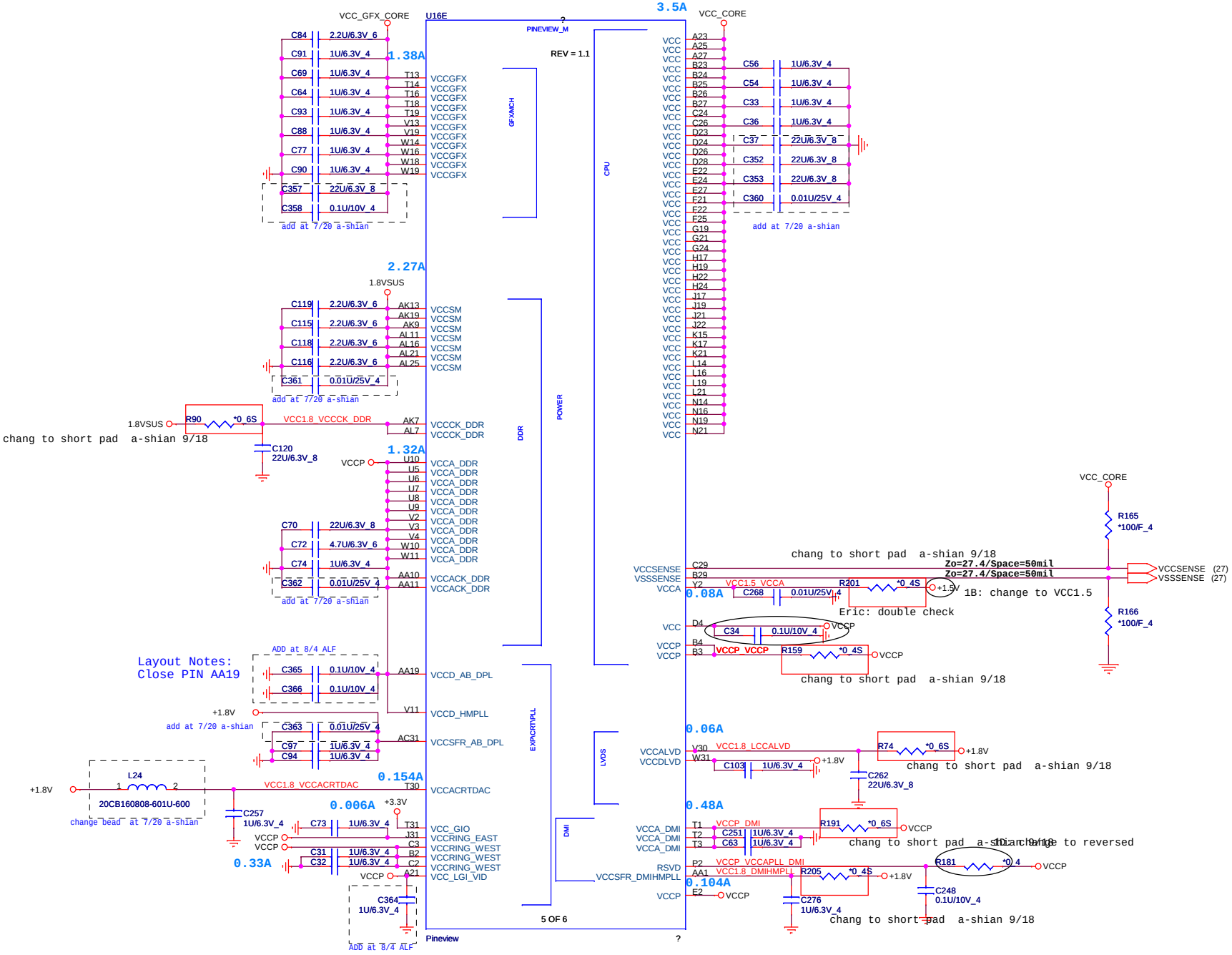

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PROJECT : FL2

Size	Document Number	Rev
	Pineview Power	1A

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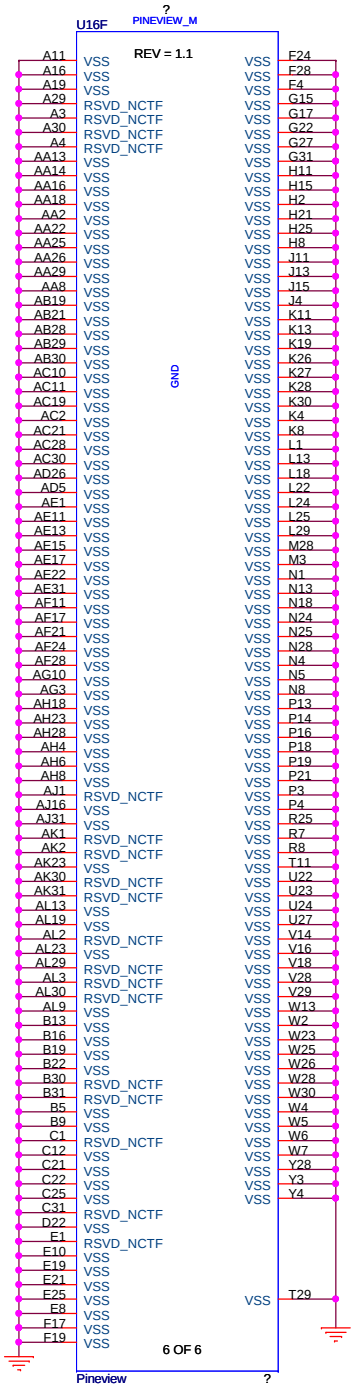

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PROJECT : FL2

Size	Document Number	Rev
	Pineview GND	1A

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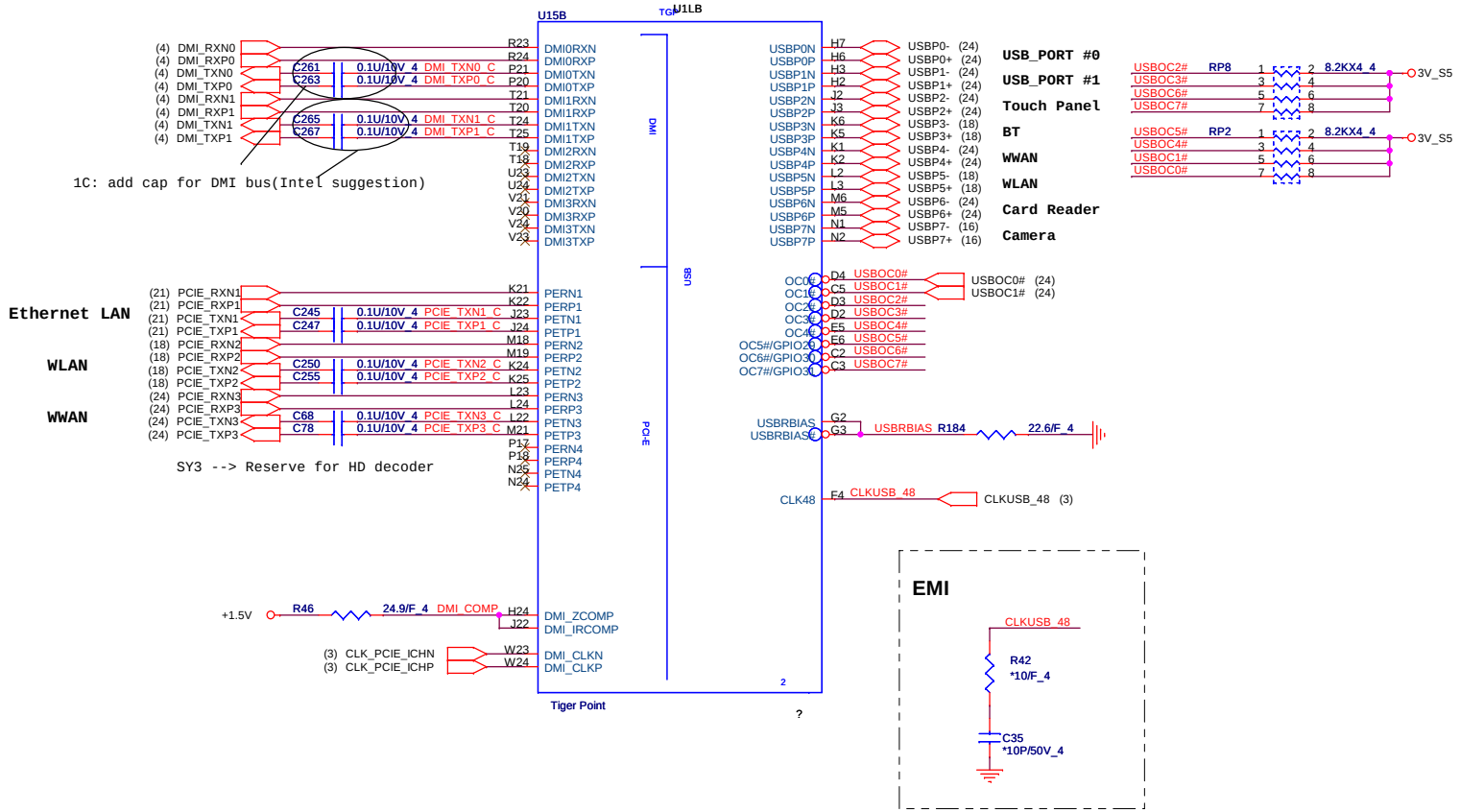

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PROJECT : FL2

Size	Document Number	Rev
	Tiger Point DMI/PCIE/USB	1A

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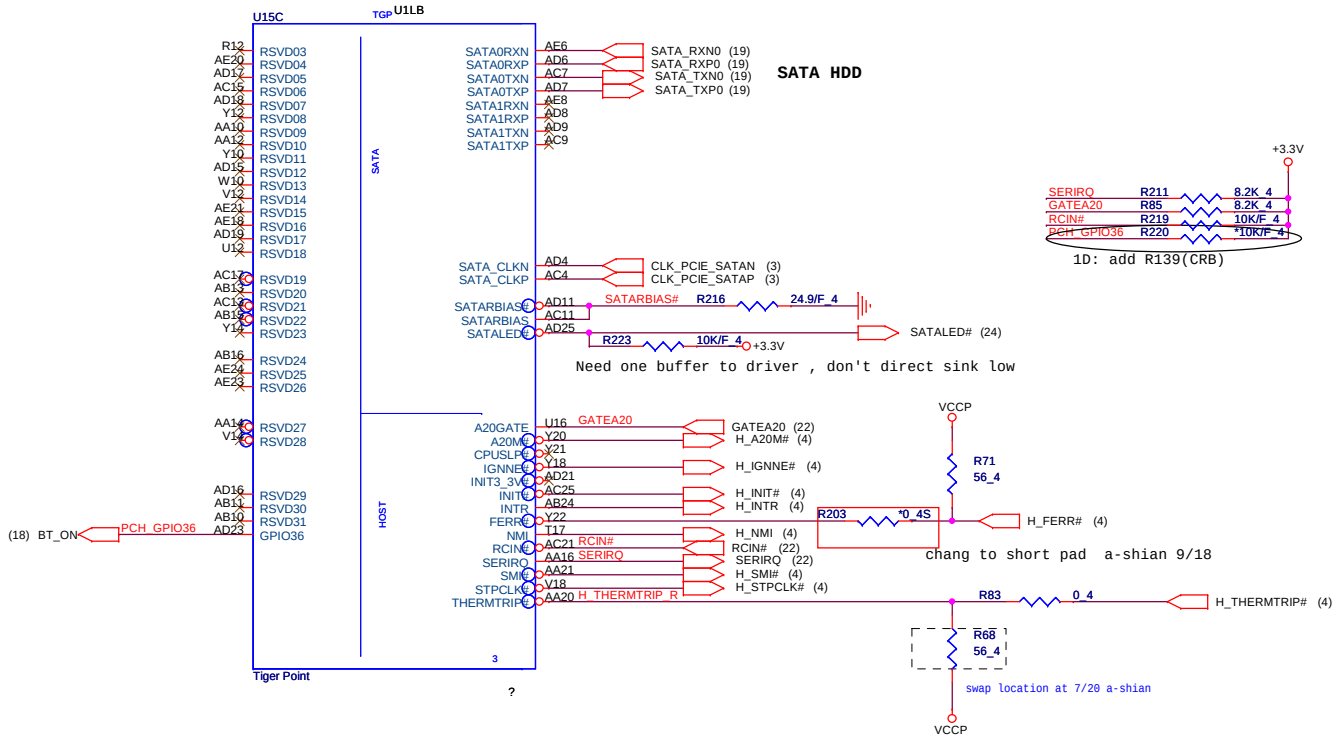

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PROJECT : FL2		
Size	Document Number: Tiger Point Sata/Host	Rev 1A
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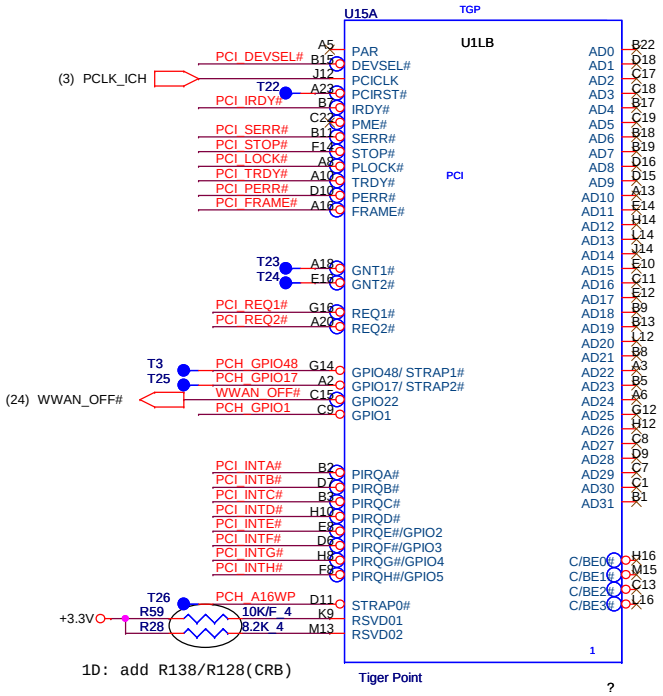
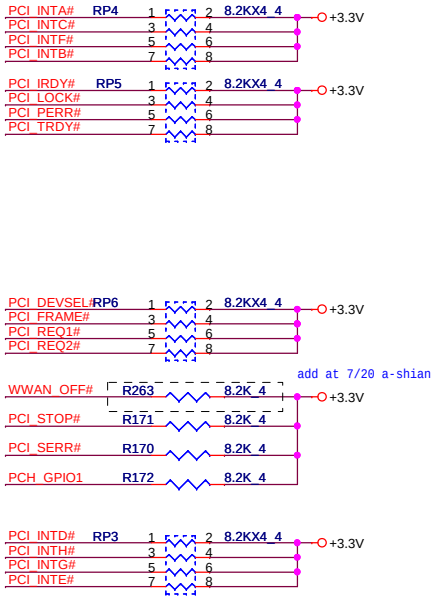


1D: add R138/R128(CRB)



IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UH Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2

PCI_GNT#2	Internal PU Should not be PD

ICH Boot BIOS select

PCH_GPIO17 (INT PU)	PCH_GPIO48 (INT PU)	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (Default)

A16 SWAP Override strap

PCH_A16WP (INT PU)	**Low = A16 swap override enabled** **High = Default**

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PROJECT : FL2

Size	Document Number	Rev
	TigerPoint PCI(3/6)	1A

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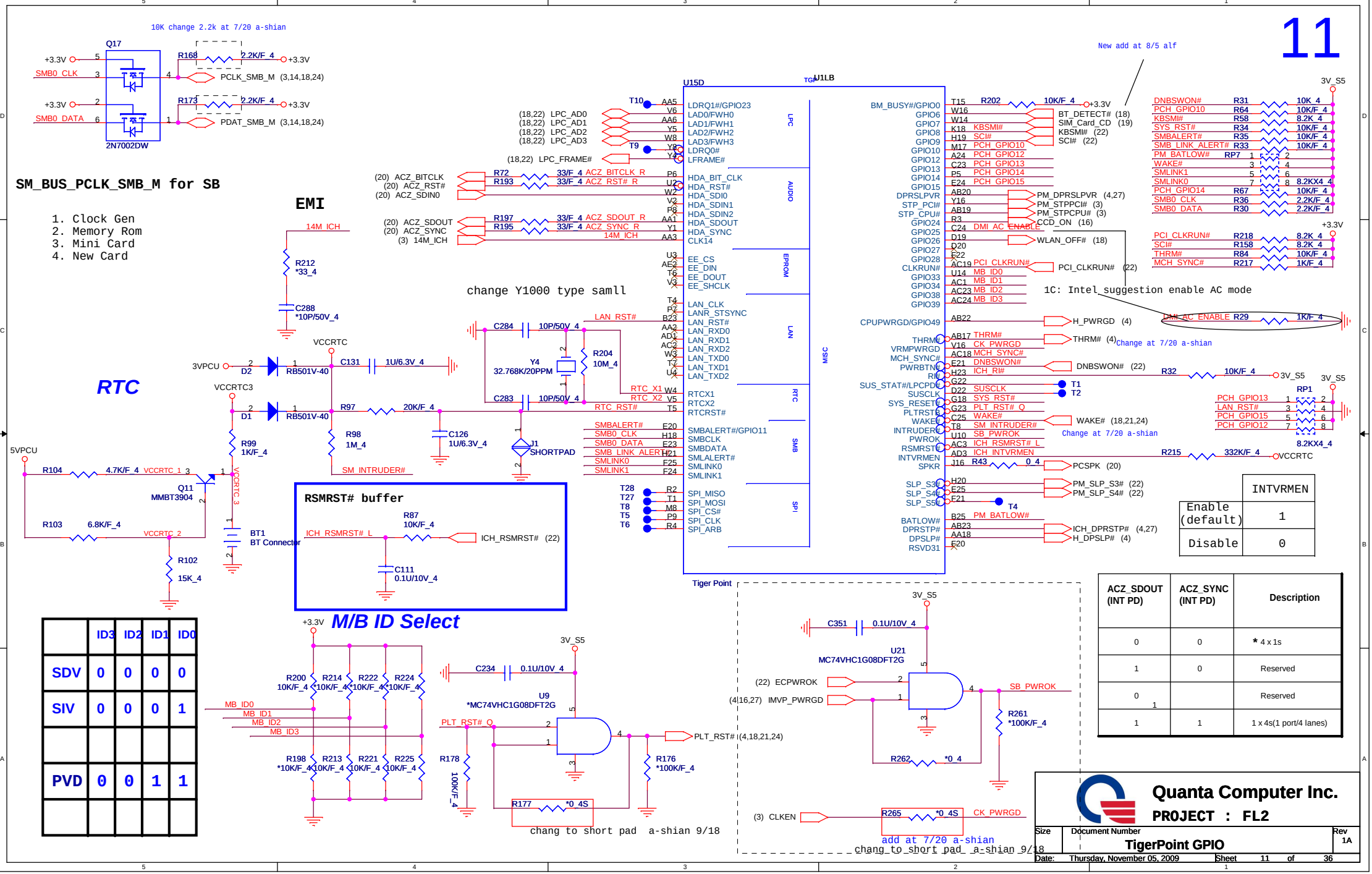

	INTVRMEN
Enable (default)	1
Disable	0

	ID3	ID2	ID1	ID0
SDV	0	0	0	0
SIV	0	0	0	1
PVD	0	0	1	1

ACZ_SDOUT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0	* 4 x 1s
1	0	Reserved
0	1	Reserved
1	1	1 x 4s(1 port/4 lanes)

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PROJECT : FL2

Size	Document Number	Rev
	TigerPoint GPIO	1A

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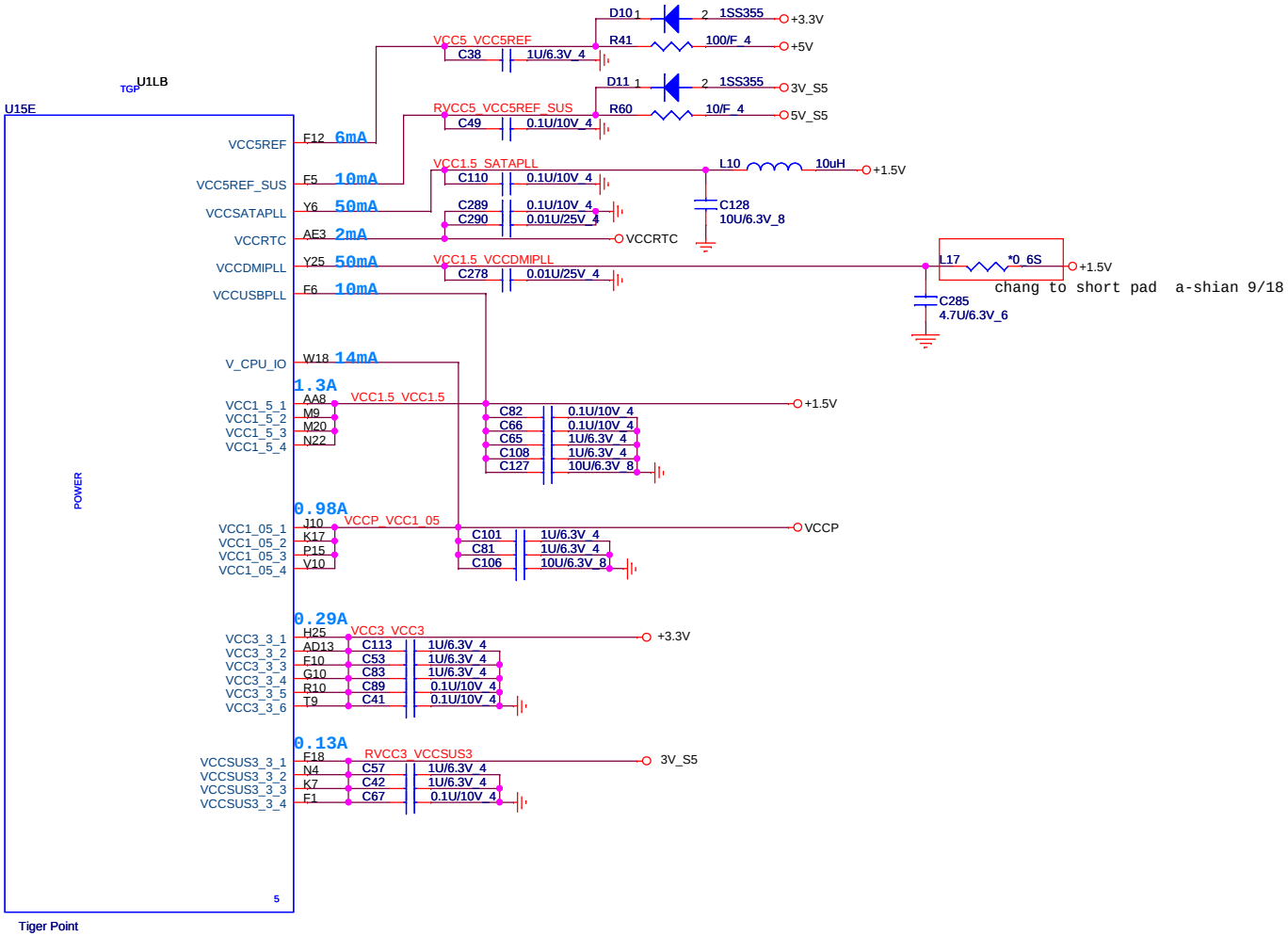

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PROJECT : FL2

Size	Document Number	Rev
	TigerPoint Power	1A

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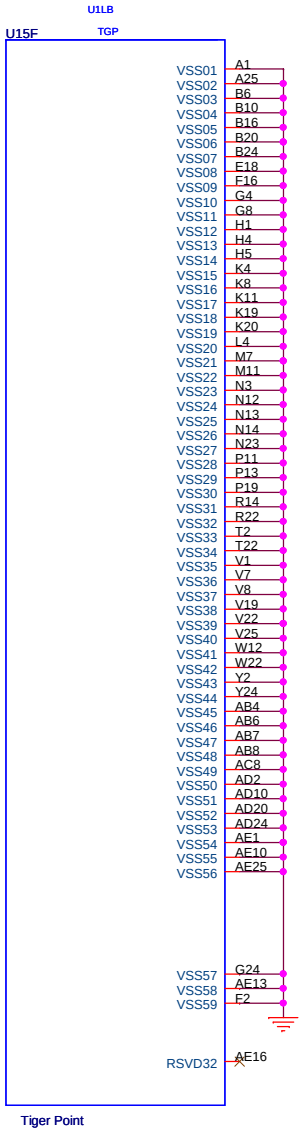

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PROJECT : FL2

Size	Document Number	Rev
	TigerPoint GND	1A

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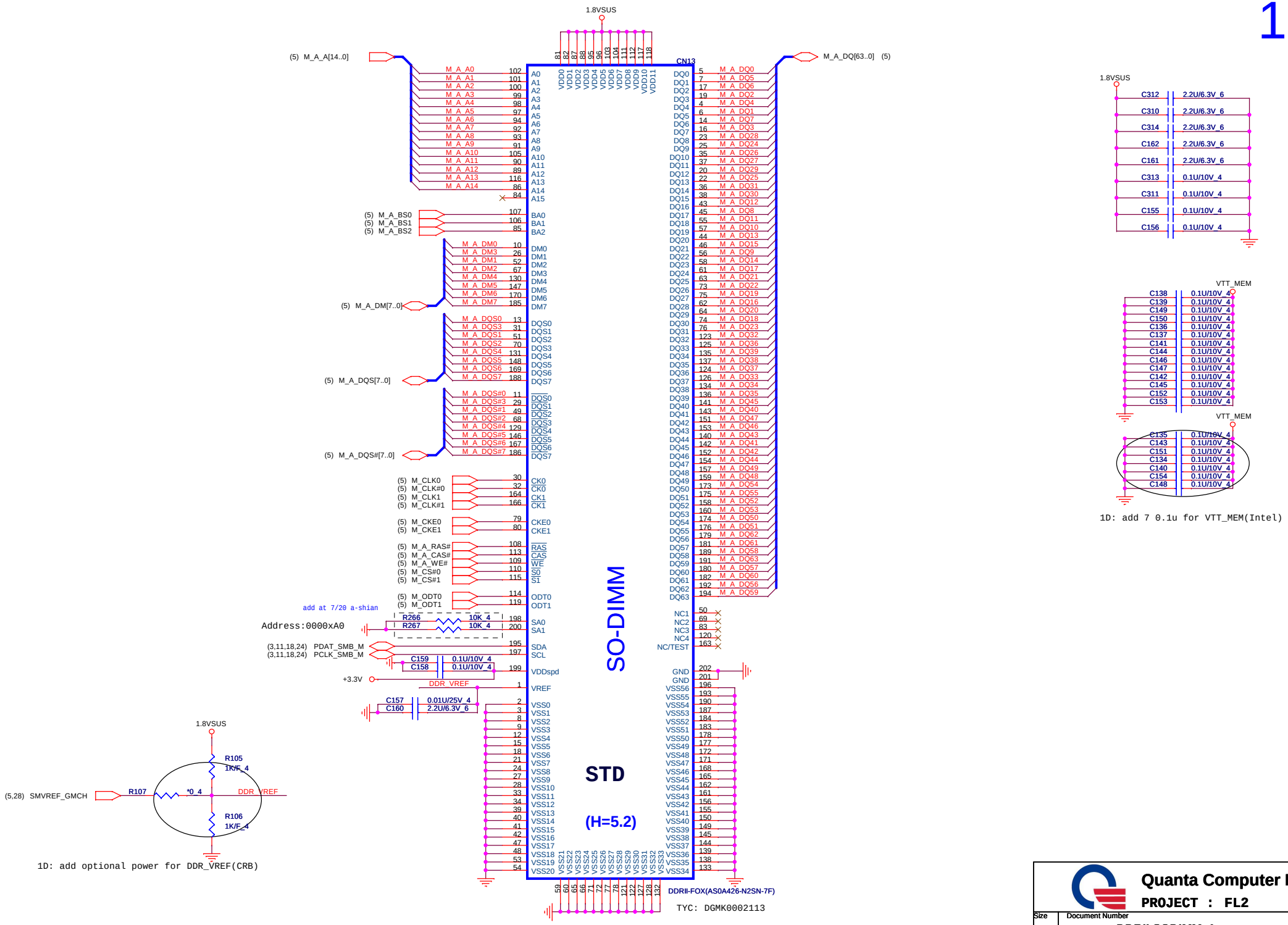

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PROJECT : FL2

Size	Document Number	Rev
	DDRII SODIMMx1	1A

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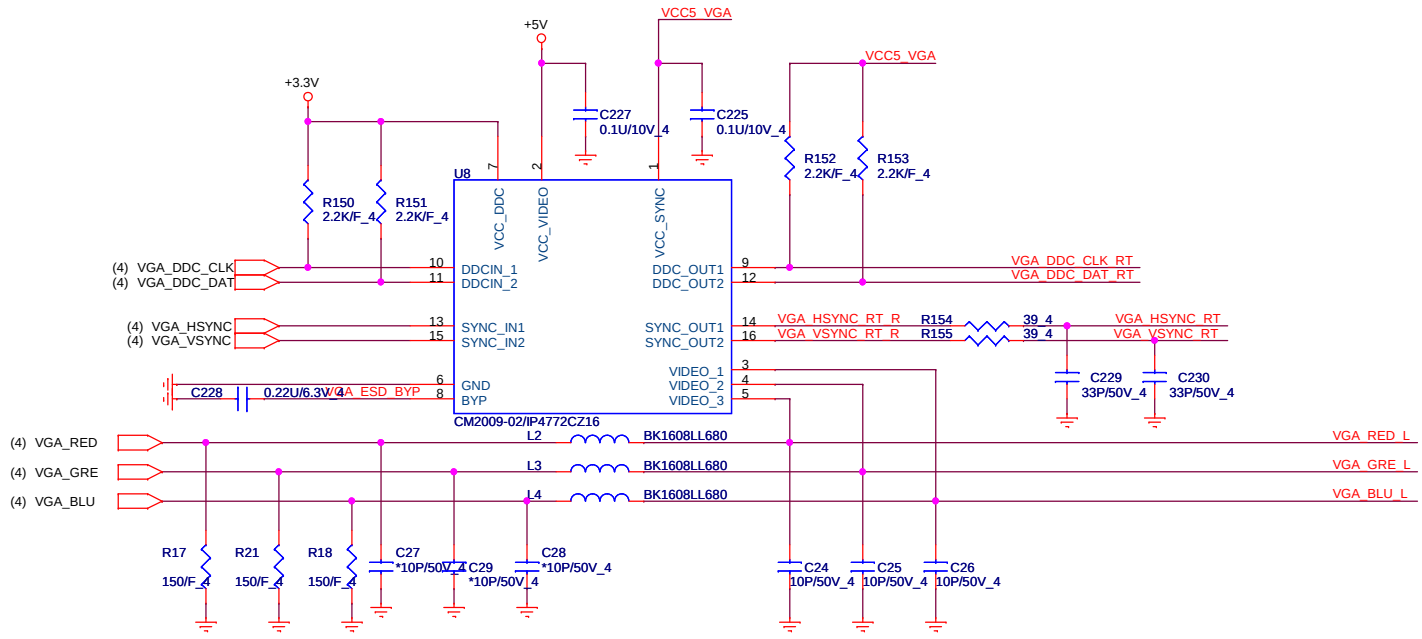
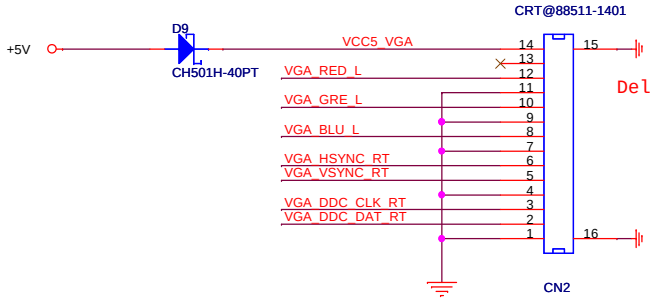
CRT



VCC5_VGA(5V+-10%)
Current limit <1A

VCC5<55mA
Current limit ~ 350mA



Del CN2 pin 2 for manufacture 1104 a-shian

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Size	Document Number: CRT	Rev 1A
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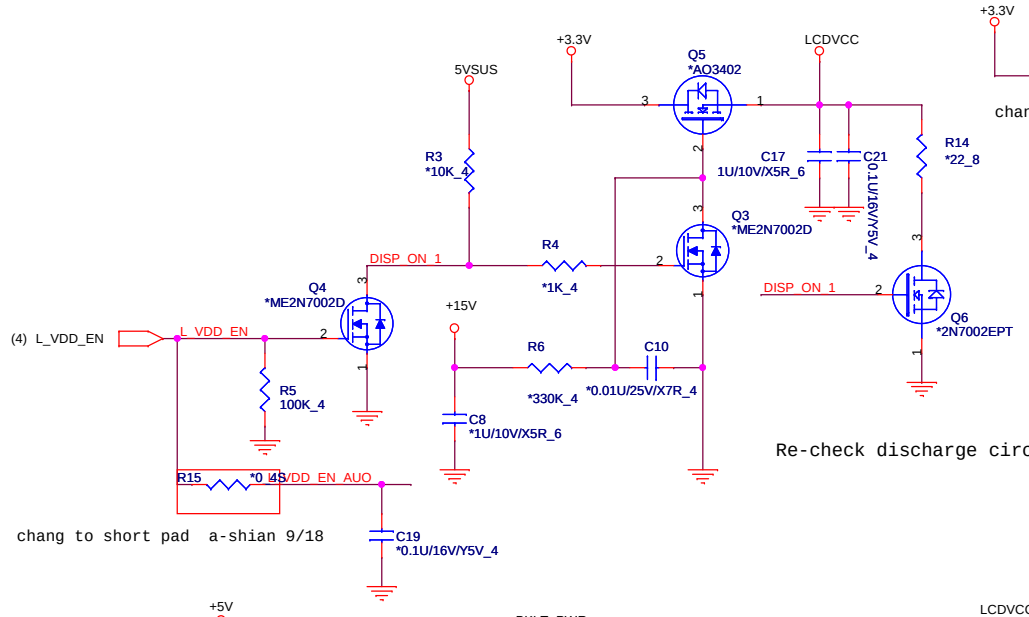
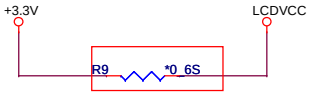
LVDS

LVDS Enable



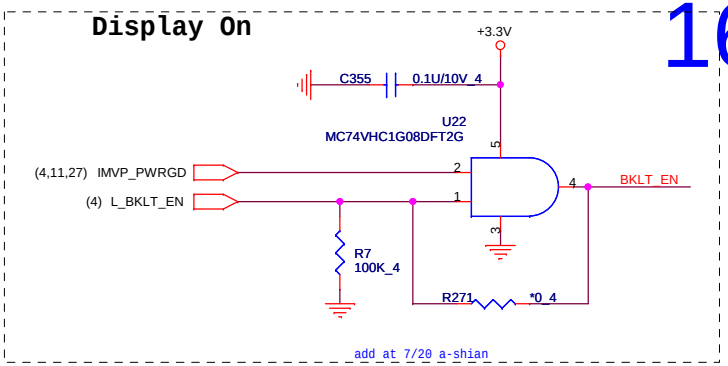
chang to short pad a-shian 9/18



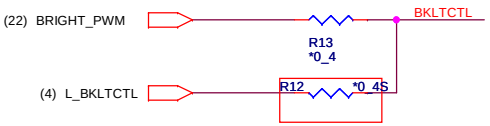
chang to short pad a-shian 9/18

Re-check discharge circuit on A stage--0611

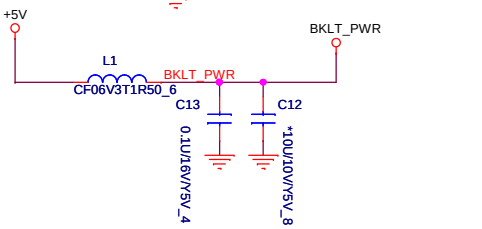
Display On

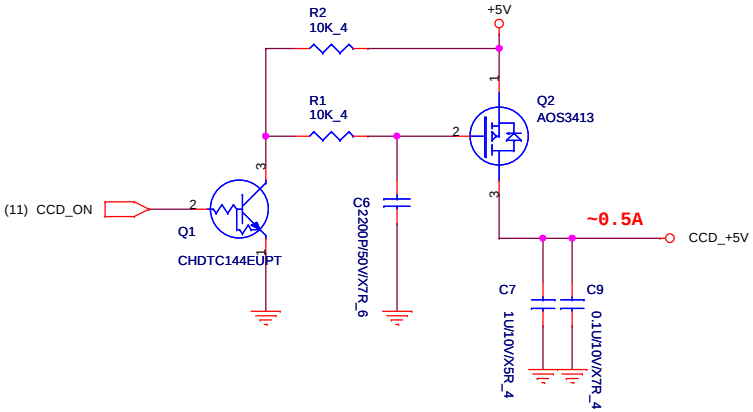


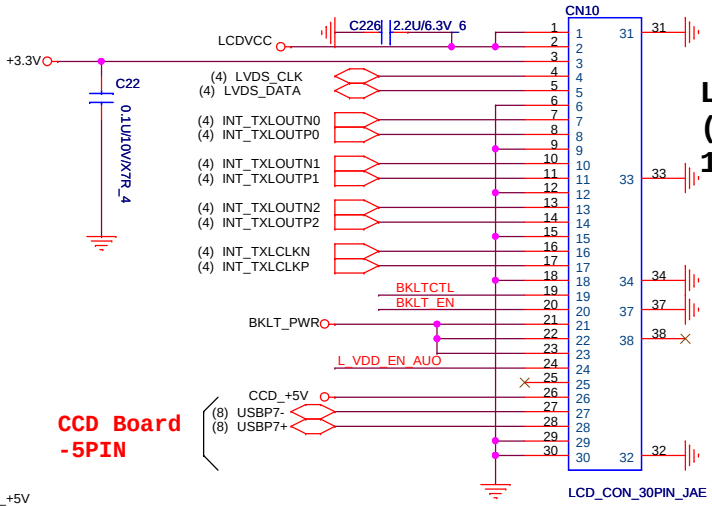
Backlight Control



chang to short pad a-shian 9/18







CCD Board
-5PIN

LVDS (10.1")
(1024x600, 1366x768)

OK -alf
change to JAE -0601

2009/06/04 reverse for layout

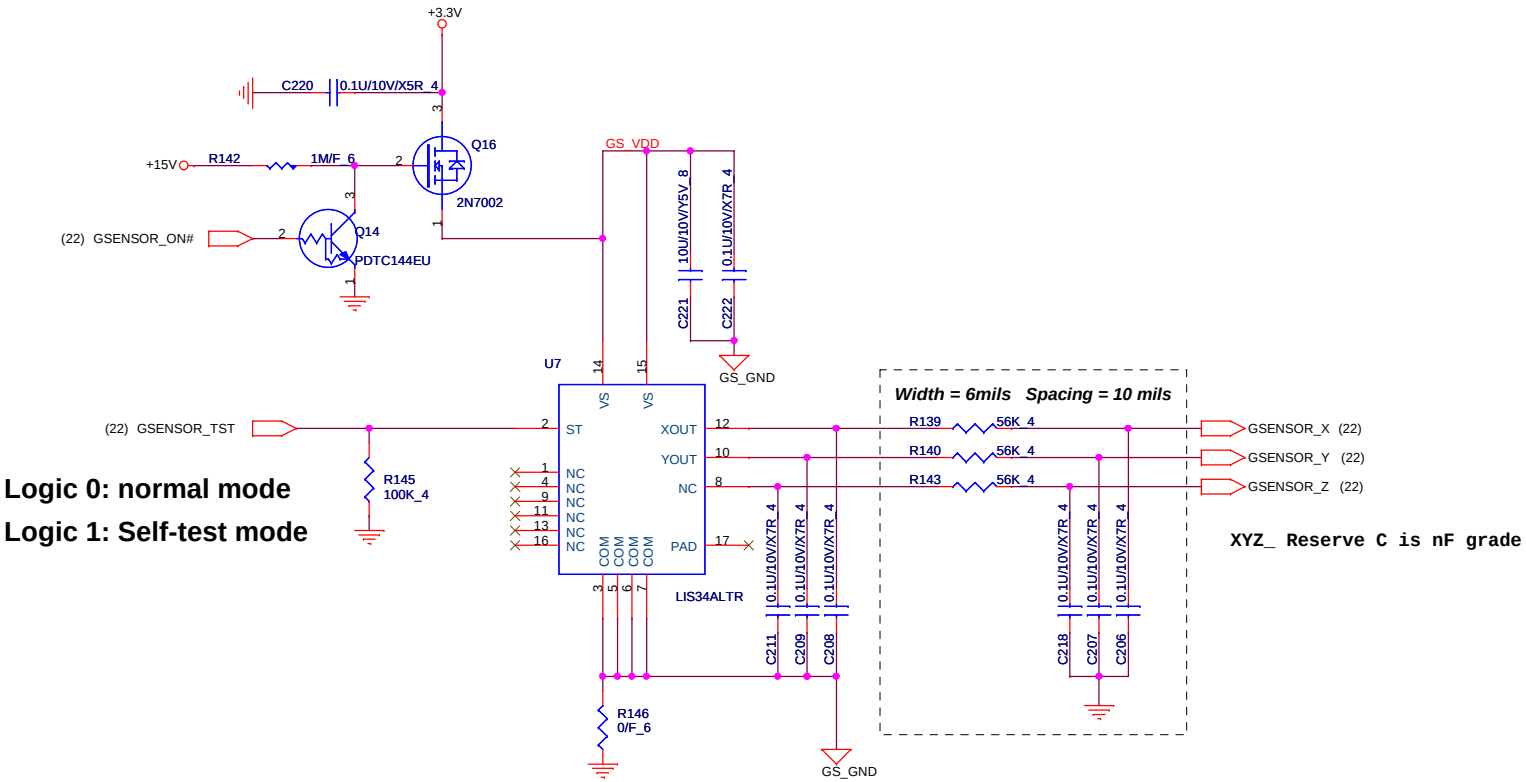
Quanta Computer Inc.

PROJECT : FL2

Size	Document Number	Rev
	LVDS	1A

Date: Thursday, November 05, 2009 Sheet 16 of 36

G-SENSOR (3-Axial)



Logic 0: normal mode

Logic 1: Self-test mode

Quanta Computer Inc.

PROJECT : FL2

Size	Document Number	Rev
	G_Sensor	1A

Date: Thursday, November 05, 2009 Sheet 17 of 36

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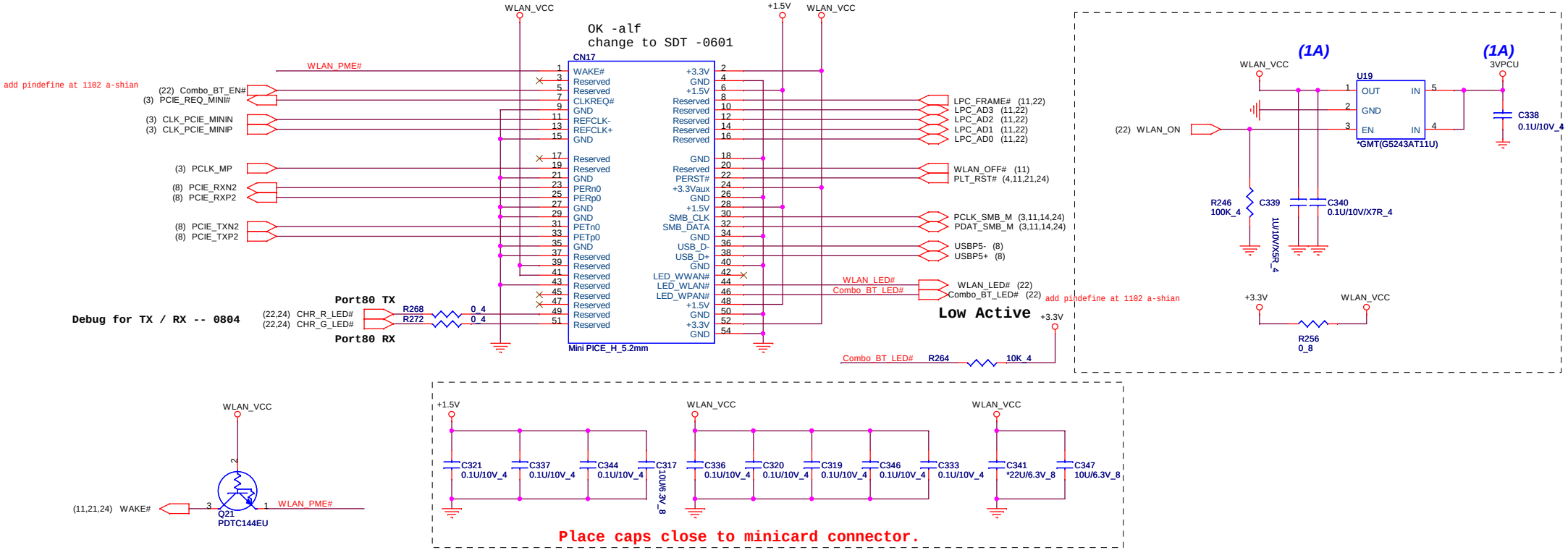
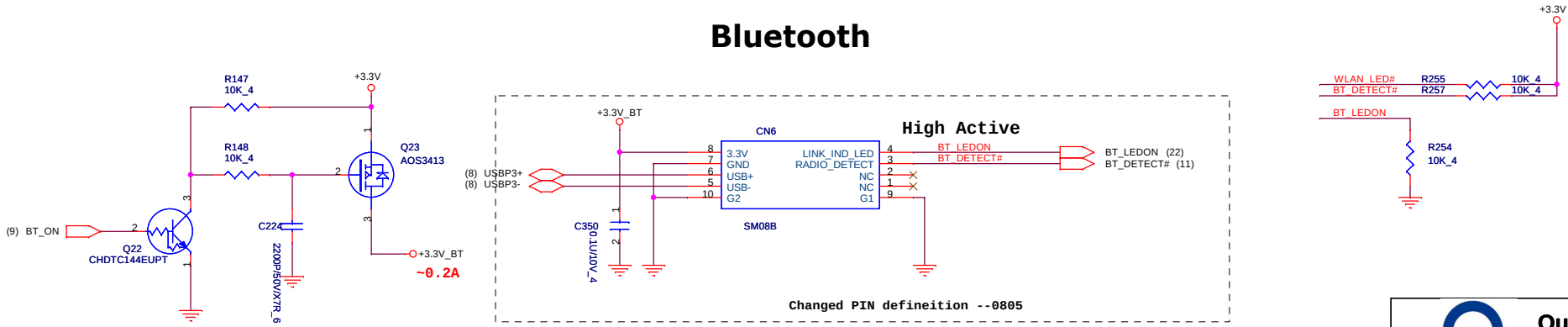
3G MiniCard WLAN connector
Mini Card Version1.2

+3.3V Max 1.1A / +1.5V Max 375mA

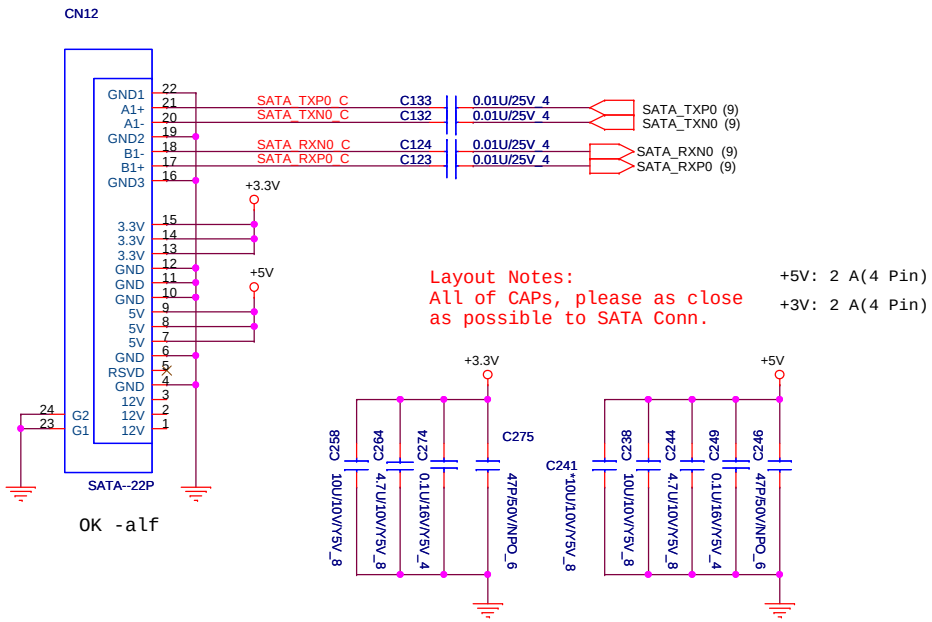


Bluetooth



Quanta Computer Inc.		
PROJECT : FL2		
Size	Document Number: MINI CARD (WLAN) / BT	Rev 1A
Date: Thursday, November 05, 2009	Sheet 18 of 36	

SATA CONNECTOR



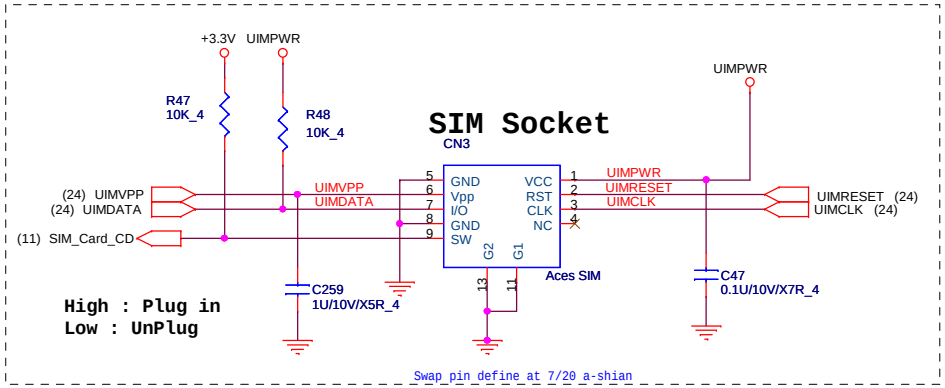
OK -alf

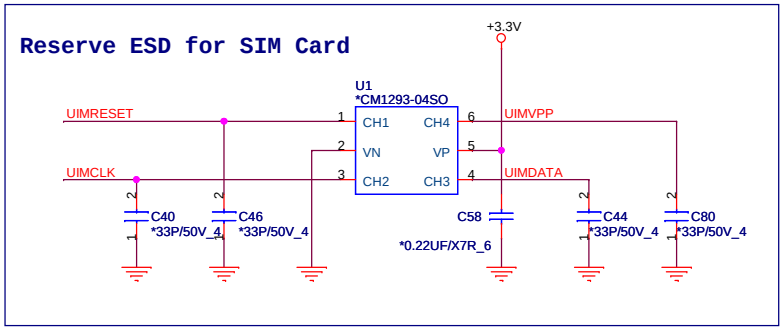
Layout Notes:
All of CAPs, please as close as possible to SATA Conn.

+5V: 2 A(4 Pin)
+3V: 2 A(4 Pin)

SIM Card CONNECTOR

Layout Notes for SIM Card
SIM Power (UIMPWR) trace more then 20mil





Quanta Computer Inc.
PROJECT : FL2

Size	Document Number	Rev
	SATA / SIM Card	1A

Date: Thursday, November 05, 2009 Sheet 19 of 36

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AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

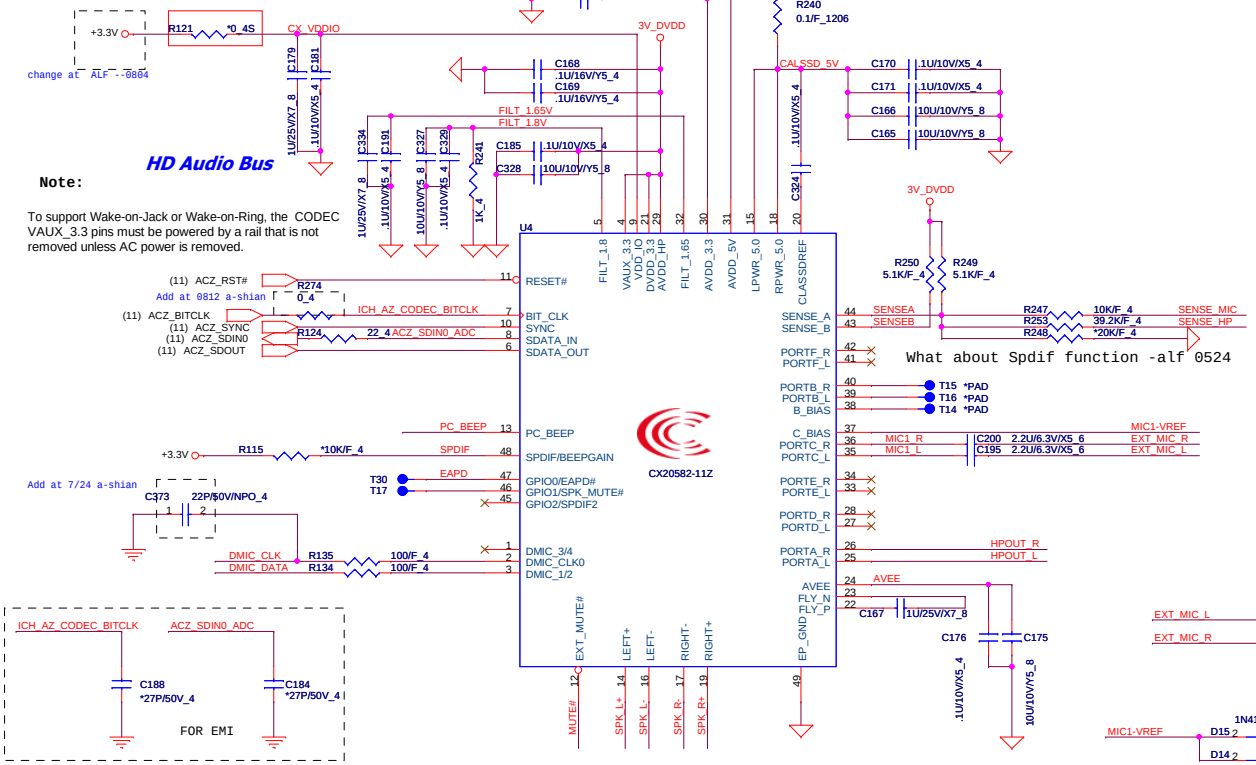
chang to short pad a-shian 9/18

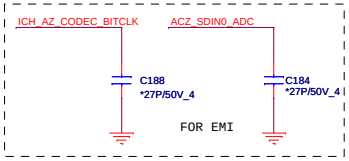
change at ALF - 0804

HD Audio Bus

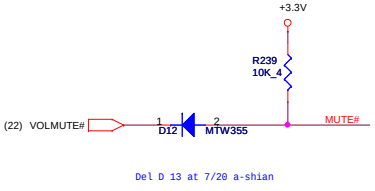
Note:

To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 pins must be powered by a rail that is not removed unless AC power is removed.





PORT	PLACE TO
MONO_OUT	X
PORT A	Head Phone Out
PORT B	X
PORT C	External MIC
PORT D	X
PORT E	X
PORT F	X
DM	Internal MIC
SPDIF	V



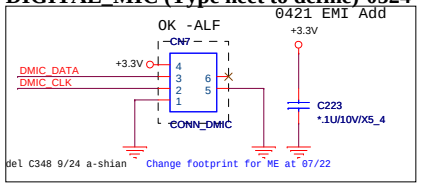
EMI Reserved

AGND and GND was connected by internal trace

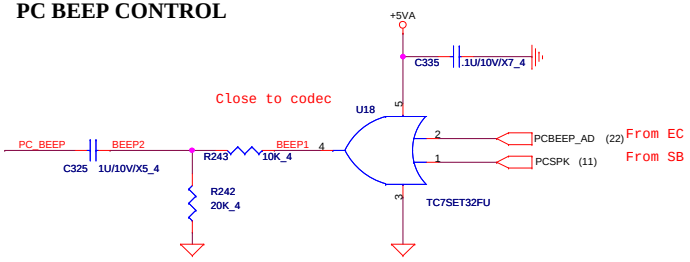
R236 *0_6

DIGITAL_MIC (Type neet to define)-0524

0421 EMI Add

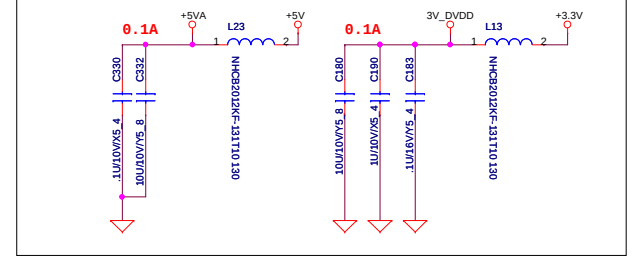


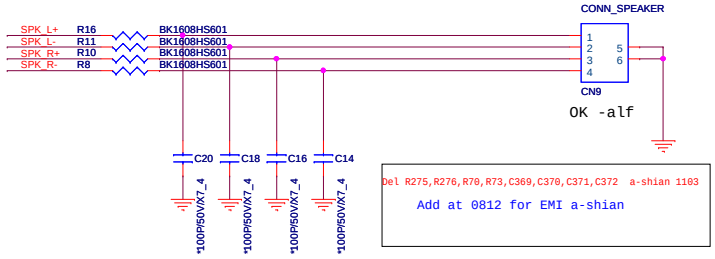
PC BEEP CONTROL



Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).

Place bypass caps very close to device.



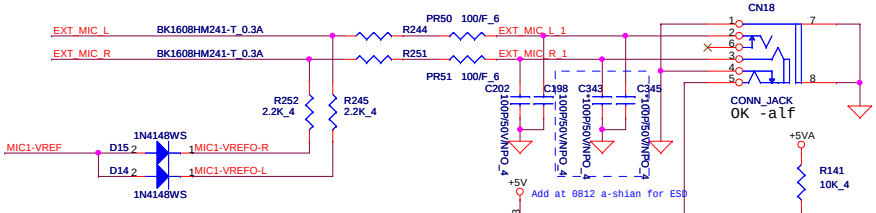


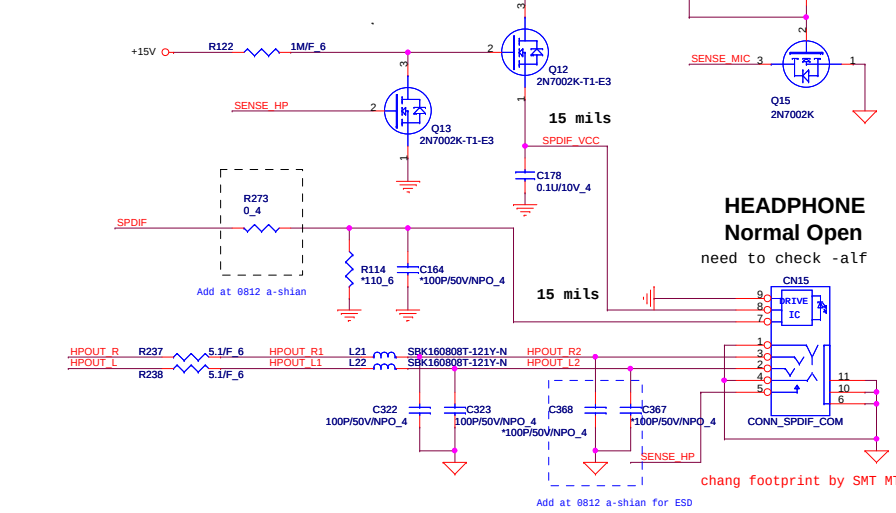
Del R275,R276,R70,R73,C369,C370,C371,C372 a-shian 1103

Add at 0812 for EMI a-shian

INT Speaker

External Microphone Jack Stereo MIC Normal Close





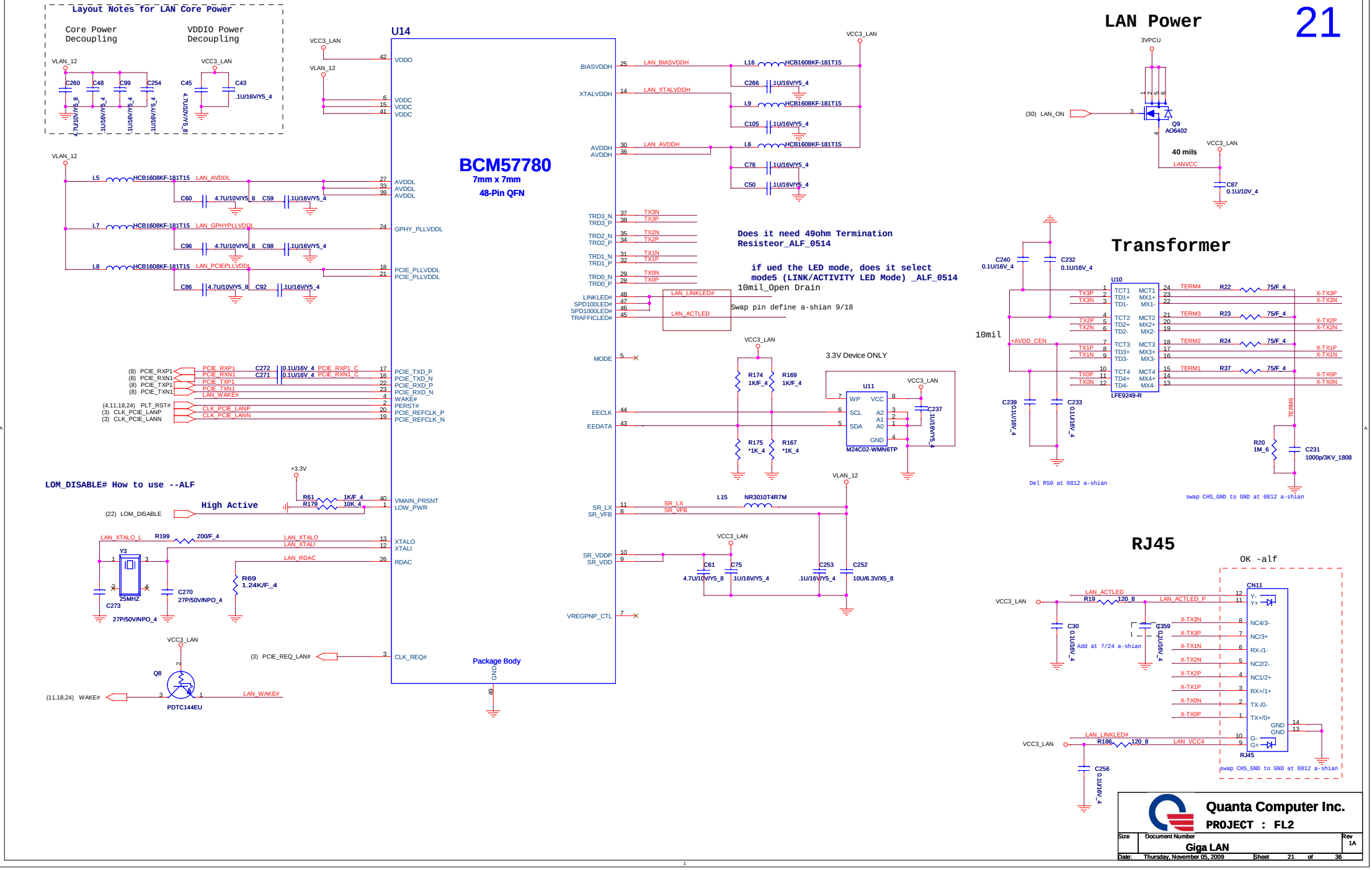
Quanta Computer Inc.

PROJECT : FL2

Size	Document Number	Rev
	AUDIO CODEC (CX20582-10Z)	1A

Date: Thursday, November 05, 2009 Sheet 20 of 36

LAN Power



Quanta Computer Inc.

PROJECT : FL2

Size	Document Number	Rev
	Giga LAN	1A

Date: Thursday, November 05, 2009 Sheet 21 of 36

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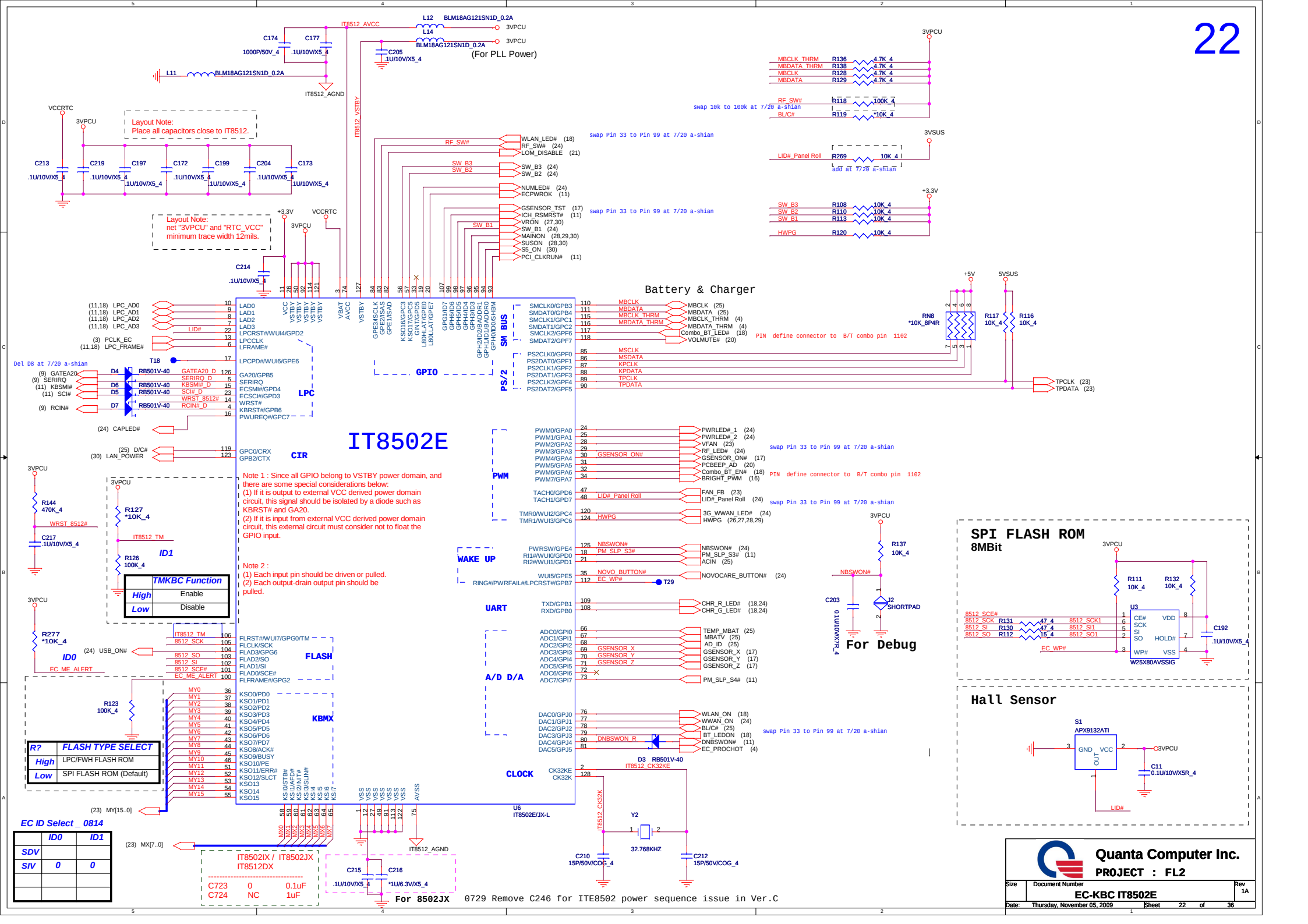
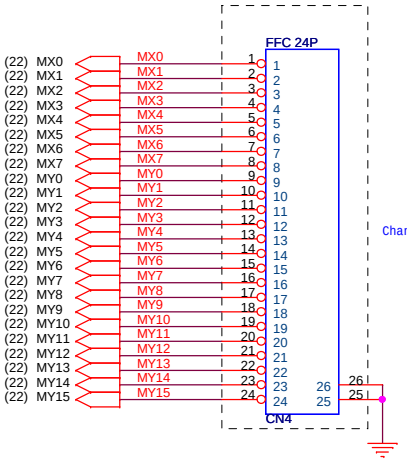

IT8502E
Battery & Charger
SPI FLASH ROM
8MBit
Hall Sensor
For Debug
(For PLL Power)
Layout Note:
Place all capacitors close to IT8512.
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
TMKBC Function
High Enable
Low Disable
FLASH TYPE SELECT
High LPC/FWH FLASH ROM
Low SPI FLASH ROM (Default)
EC ID Select _ 0814
ID0 ID1
SDV
SIV 0 0
IT8502IX / IT8502JX
IT8512DX
C723 0 0.1uF
C724 NC 1uF
For 8502JX 0729 Remove C246 for ITE8502 power sequence issue in Ver.C
Quanta Computer Inc.
PROJECT : FL2
Size Document Number Rev
EC-KBC IT8502E 1A
Date: Thursday, November 05, 2009 Sheet 22 of 36

INT. KEYBOARD



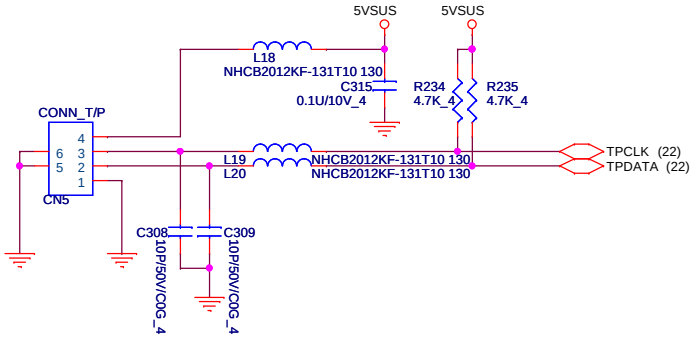
Change footprint for ME at 07/22/0804

C114	220P/50V_4	MY3
C79	220P/50V_4	MX3
C112	220P/50V_4	MY2
C109	220P/50V_4	MY1
C302	220P/50V_4	MY11
C104	220P/50V_4	MX7
C298	220P/50V_4	MY10
C100	220P/50V_4	MX6
C107	220P/50V_4	MY0
C71	220P/50V_4	MX2
C62	220P/50V_4	MX1
C55	220P/50V_4	MX0

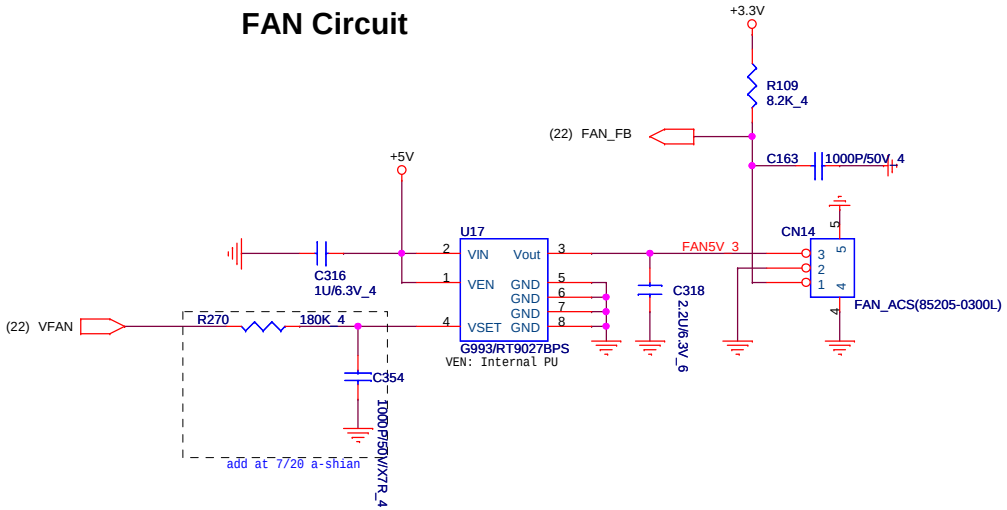
C291	220P/50V_4	MY7
C122	220P/50V_4	MY6
C121	220P/50V_4	MY5
C117	220P/50V_4	MY4
C307	220P/50V_4	MY15
C306	220P/50V_4	MY14
C304	220P/50V_4	MY13
C303	220P/50V_4	MY12
C293	220P/50V_4	MY8
C85	220P/50V_4	MX4
C295	220P/50V_4	MY9
C95	220P/50V_4	MX5

TOUCH PAD CONNECTOR

revers 6/6 for mechanism



FAN Circuit



Quanta Computer Inc.

PROJECT : FL2

Size	Document Number	Rev
	KB / TP / FAN	1A

Date: Thursday, November 05, 2009 Sheet 23 of 36

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LCD to MB wire

Layout Notes:
PLS close each power
PIN of CN1003 -- alf

chang footprint 9/21 a-shian

Wire_to_board_30PIN_JAE

CN8

LED Board
-11PIN
Touch Panel
-5PIN

Power Board
- 5PIN

SW Board
- 5PIN

(8) USBP2-
(8) USBP2+
(22) NUMLED#
(22) CAPLED#
(9) SATALED#
(22) PWRLED#_1
(18,22) CHR_G_LED#
(18,22) CHR_R_LED#
(22) RF_LED#
(22) PWRLED#_2
(22) NBSWON#
(22) SW_B1
(22) SW_B2
(22) SW_B3

Card Reader to MB wire

CN16

BTB 50PIN Conn

(8) USBP0-
(8) USBP0+
(8) USBP1-
(8) USBP1+
(8) USBP4-
(8) USBP4+
(8) USBP6-
(8) USBP6+
(3) CLK_PCIE_CRDN
(3) CLK_PCIE_CRDP
(8) PCIE_RXN3
(8) PCIE_RXP3
(8) PCIE_TXN3
(8) PCIE_TXP3
(8) USBOC1#
(8) USBOC0#

UIMVPP
UIMRESET
UIMCLK
UIMDATA
UIMPWR
3G_WWAN_LED#

UIMPWR
UIMVPP (19)
UIMRESET (19)
UIMCLK (19)
UIMDATA (19)
LID#_Panel Roll (22)
PCLK_SMB_M (3,11,14,18)
PDAT_SMB_M (3,11,14,18)
WAKE# (11,18,21)
3G_WWAN_LED# (22)
PCIE_REQ_CARD# (3)
PLT_RST# (4,11,18,21)
WWAN_OFF# (10)
RF_SW# (22)
+3.3V
5VSUS
WWAN_VCC
3VSUS
+1.5V
USB_ON# (22)

Wire to Board PIN SWAP --0803
modify CN16 Pin 23,24,25,32,33,34,35 pin define a-shian 9/18

Add WWAN LED -- 0803

WWAN LED PULL UP

+3.3V
R258
10K_4
3G_WWAN_LED#

EC - Reserve Power Control for WWAN -- 0205

+3.3V
WWAN_VCC
R125
0_12
C182
10U/6.3V_8
C356
*22U/6.3V_8
add at 7/20 a-shian

WWAN_VCC
(1A)
U5
OUT
GND
EN
IN
IN
*GMT(G5243AT11U)
(22) WWAN_ON
C187
C186
3VPCU
(1A)
C194
0.1U/10V_4
C193
*10U/6.3V_8

Function Board

NOVO_BUTTON#

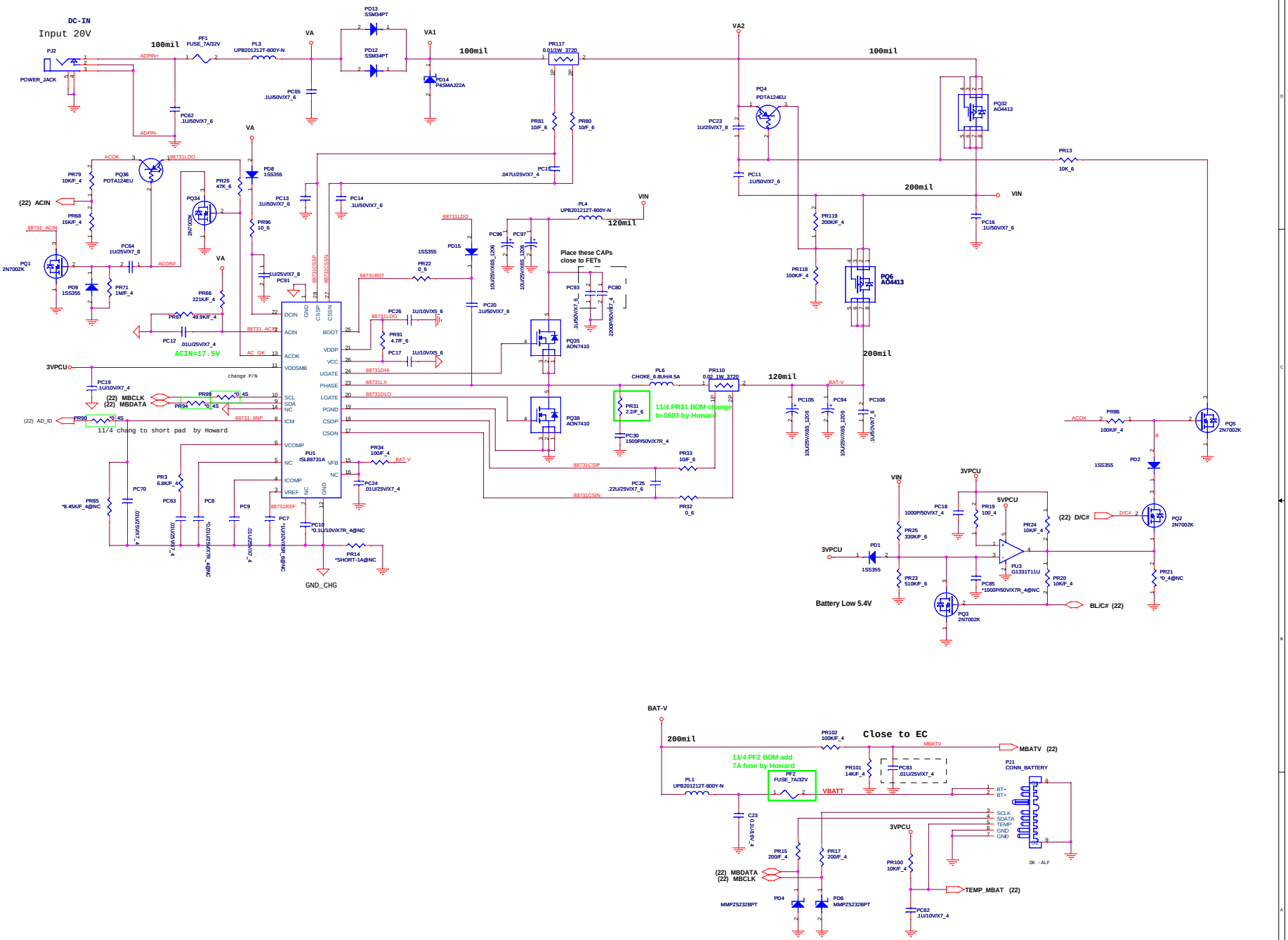
3VPCU
R149
10K_4
(22) NOVOCARE_BUTTON#
PC6
C15
CN1
MIC Conn

USB Power

5VSUS
move U20 to CRT board a-shian 9/18
Del R258 at 7/20 a-shian
C374
C375
C349

Quanta Computer Inc.
PROJECT : FL2

Size	Document Number	Rev
	Small Board	1A
Date: Thursday, November 05, 2009	Sheet 24 of 36	



Quanta Computer Inc.

PROJECT : FL2

Size	Document Number	Rev
	POWER_Charger (ISL88731A)	1A

Date: Thursday, November 05, 2009 Sheet 25 of 35

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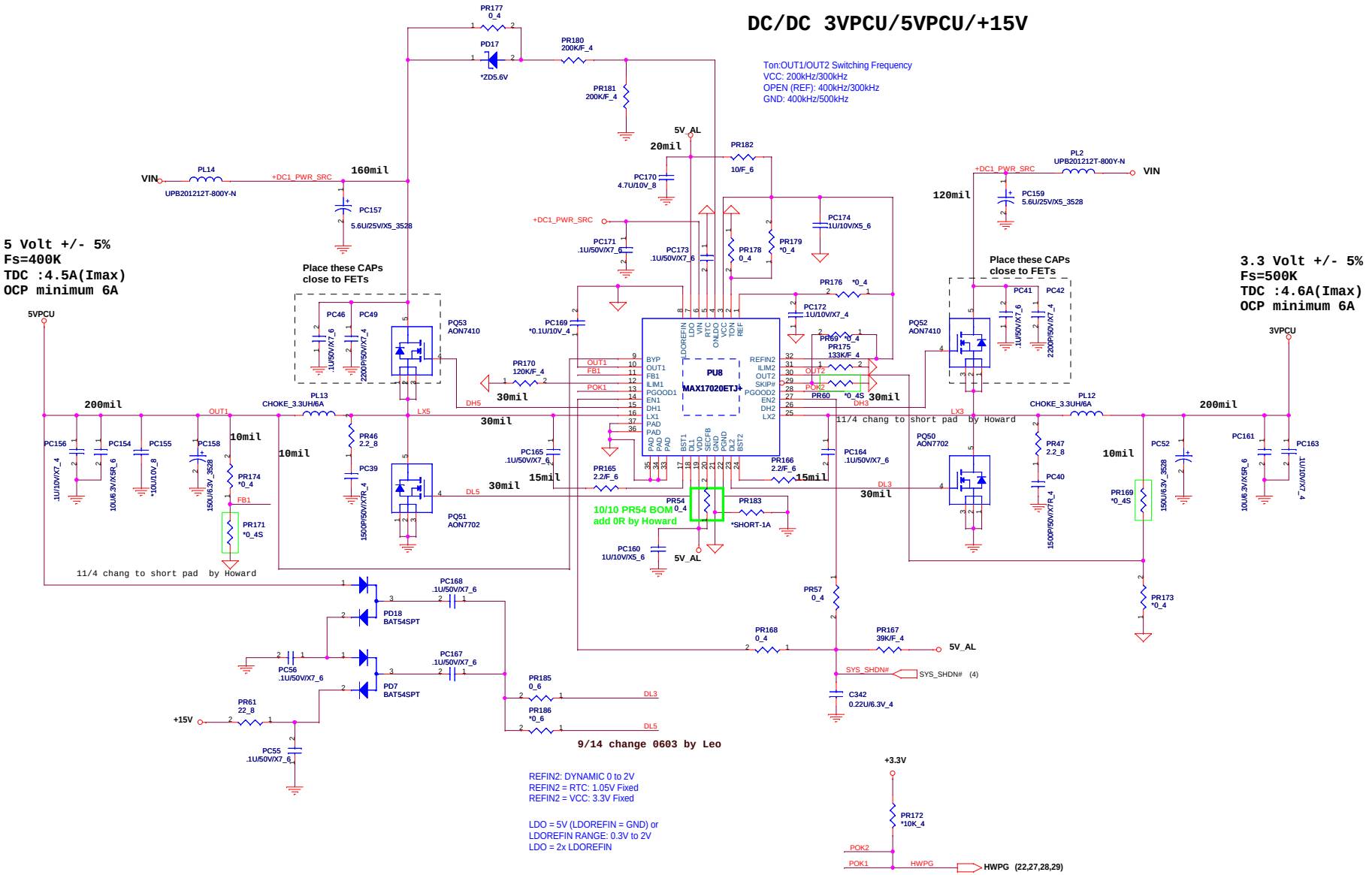
DC/DC 3VPCU/5VPCU/+15V

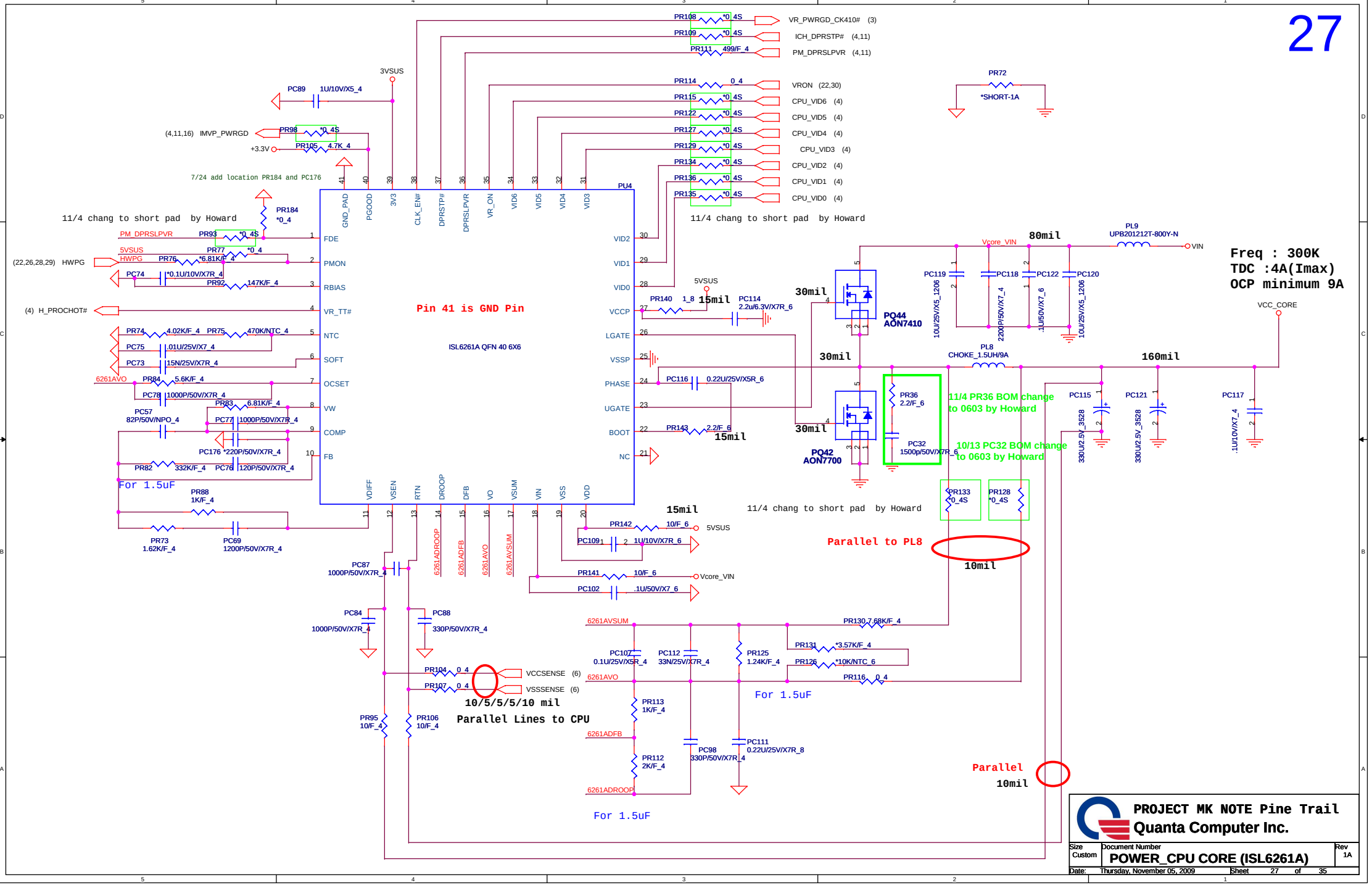


Quanta Computer Inc.

PROJECT : FL2

Size	Document Number	Rev
	POWER_3V/5V (MAX17020ETJ+)	1A

Date: Thursday, November 05, 2009 Sheet 26 of 35



PROJECT MK NOTE Pine Trail
Quanta Computer Inc.

Size	Document Number	Rev
Custom	POWER_CPU CORE (ISL6261A)	1A

Date: Thursday, November 05, 2009 Sheet 27 of 35

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1.8 Volt +/- 5%
Fs=400K
TDC :7.5A(Imax)
OCP minimum 10A

(VTT/2A)
VTT_MEM
80mil
PC147 10U/6.3V_8
PC143 10U/6.3V_8
PR154 *0_4
+1.8VSUS_1
PR155 *0_4S
(3mA)
(5,14) SMVREF_GMCH
PC139 .033U/10V_4

PU7
TPS51116RGER
VTTGND, VTTSNS, GND, MODE, VTTREF, COMP, NC, VDDQSNS, VDDQSET, S3, S5, NC, GND, VTT, VLDOIN, VBST, DRVH, LL, DRVL, PGND, CS_GND, CS, V5IN, V5FILT, PGOOD

+1.8VSUS_1
100mil
PC145 *10U/6.3V_8
5VPCU
PD16 *RB501V-40
15mil
1116VBST PR159 2.2/F_6
PC144 .1U/50V/X7_6
1116DRVH 30mil
1116LL 30mil
1116DRVL 30mil
PR156 7.87K/F_4
5VPCU
PC141 1U/10V/X5_6
PR152 5.1/F_6
PC140 1U/6.3V_4
PR157 *SHORT-1A
PR70 *0_4S
HWPG (22,26,27,29)
11/4 chang to short pad by Howard

V5FILT PR153 *0_4 1116VDDQSET
(22,29,30) MAINON PR149 0_4 1116_S3ON
(22,30) SUSON PR148 0_4 1116_S5ON
VIN_DDR PR158 619K/F_4 1116TONSET
10/10 PR158 BOM
add 619K by Howard
PC136 .1U/10V/X7_4
PC137 *0.1uF/10V_4

VIN
PC142 .1U/50V/X7_6
PL10 UPB201212T-800Y-N
120mil
VIN_DDR
PC148 .1U/50V/X7_6
PC146 4.7U/25V_8
PC151 4.7U/25V_8
PC149 2200P/50V_4
PQ47 AON7410
PQ45 AON7700
PL11 CHOKE_1.5UH/9A
PR42 2.2/J_8
PC37 1500P/50V_4
+1.8VSUS_1
320mil
PC150 330U/2.5V_7343
PC152 .1U/10V/X7_4
1.8VSUS
PC131 .1U/50V/X7_6
PC132 .1U/50V/X7_6
10mil
10mil
PR150 14K/F_4
PC138 *0.1U/10V_4
PR151 10K/F_4
Vout= 1.8V

+0.89 Volt +/- 5%
Countinue current:1.38A
Peak current:2.64A
Sustained current:1.05A

VCCP
100mil
PC129 10U/6.3V_8
PC127 *0.1U/10V_4
PU6
APL5912-KAC-TRL
VIN, VIN1, EN, VCNTL, POK, FB, NC, VOUT, GND
VCC_GFX_CORE
80mil
PC125 10U/6.3V_8
PC124 10U/6.3V_8
PC123 .1U/10V/X7_4
(22,29,30) MAINON PR147 10K/F_4
5VSUS
PC128 *.33U/6.3V_4
PC126 1U/6.3V_4
R1
R2
1.2VADJ
PR144 45.3K/F_4
10/10 PR144 BOM Change to
45.3K by Howard
(22,26,27,29) HWPG PR146 *0_4S
11/4 chang to short pad by Howard
PR145 402K/F_4
PC66 22P/50V/X7R_4
PR187 0_4
10/10 PR145 BOM Change to
402K by Howard
10/10 PC66 BOM Change to
22P by Howard
VO=(0.8(R1+R2)/R2) Vout= 0.89V

Quanta Computer Inc.
PROJECT : FL2

Size	Document Number	Rev
	POWER_1.8V(TPS5116)/0.89V(RT9205)	1A

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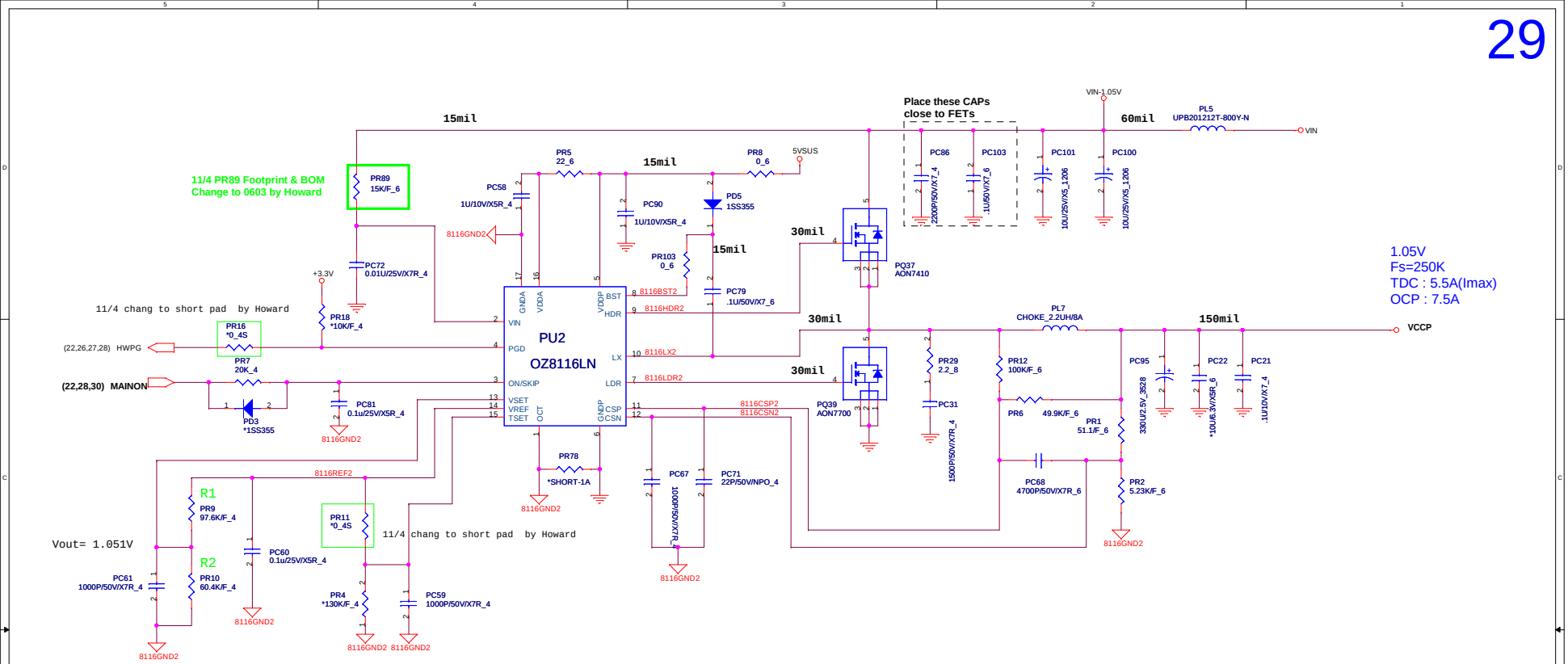

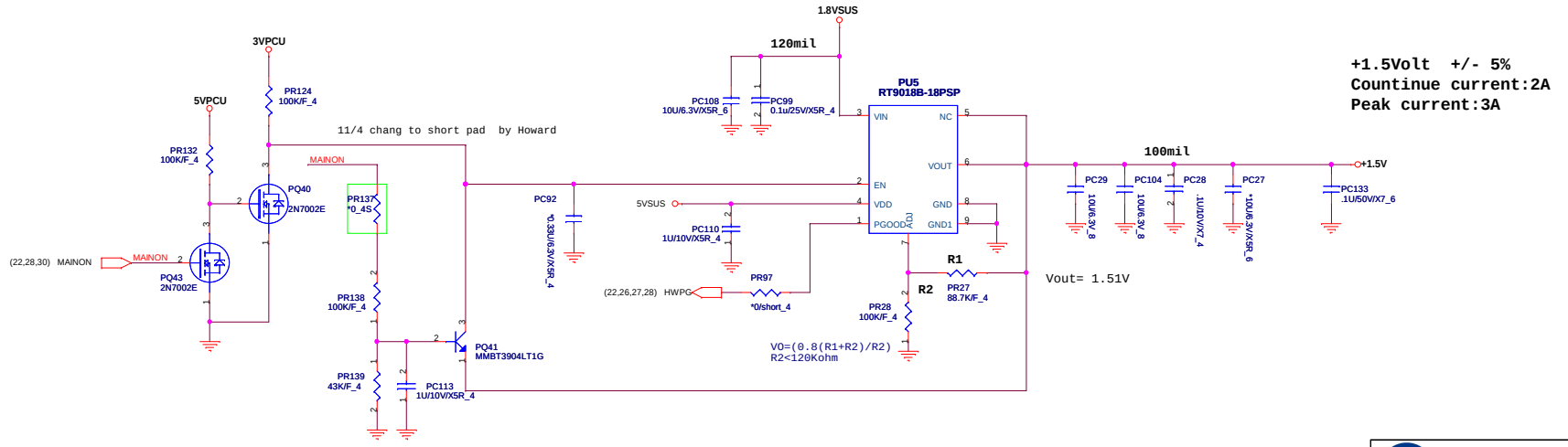

PROJECT MK NOTE Pine Trail
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Size	Document Number	Rev
Custom	VCCP (OZ8116LN)/1.5V(RT9018B)	1A

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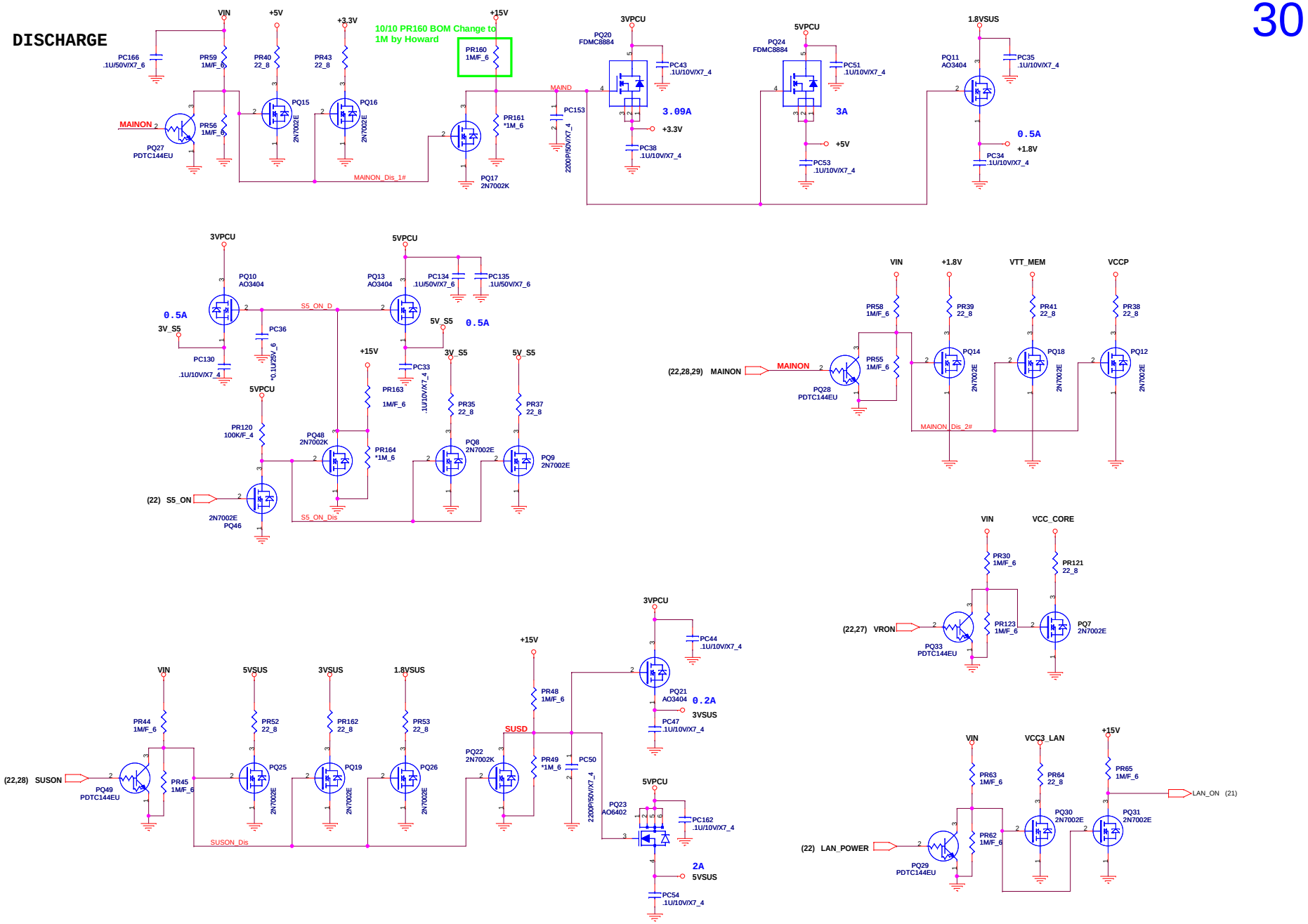
DISCHARGE



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Size	Document Number	Rev
	POWER_Discharge	1A

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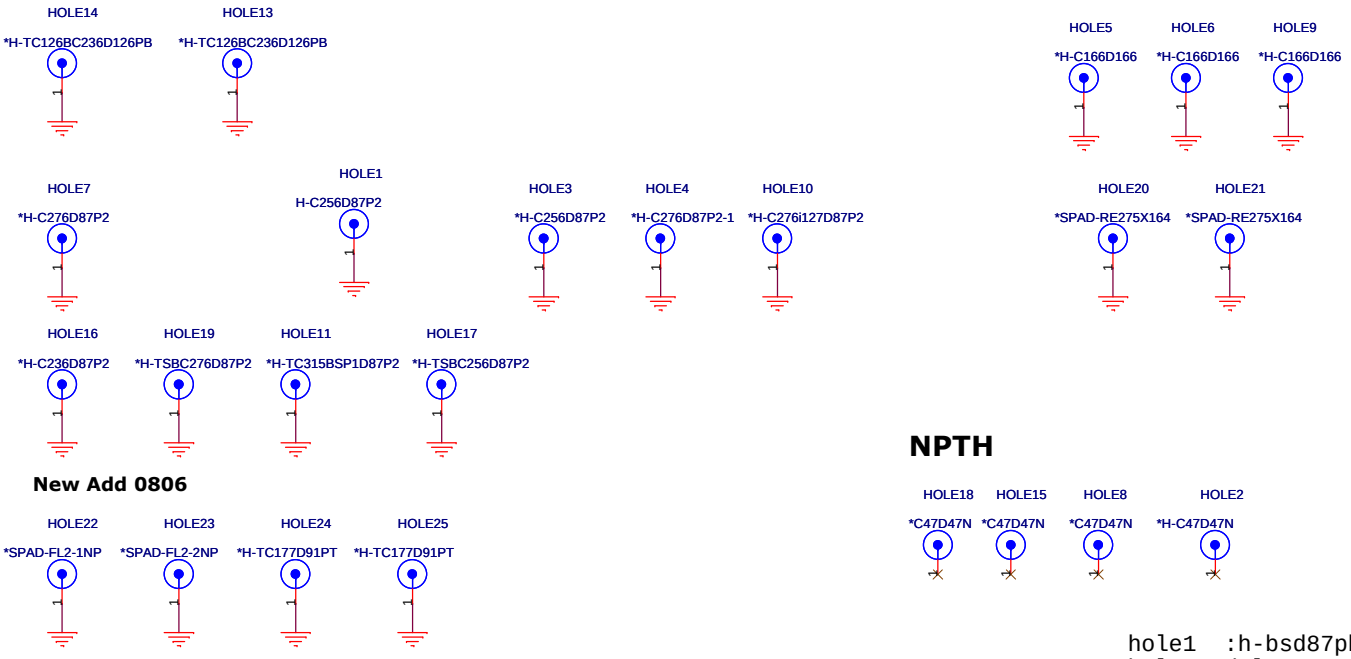
Screw Hole



hole4
hole11
hole3
hole10
hole1
hole2
hole17

New Add 0806

NPTH

hole1 :h-bsd87pb
hole2, del
hole4,hole3,hole10,: h-c87d87n
hole16: h-c236d87p2
hole19: h-tsbc276d87p2
hole11:h-bsp1d87pb
hole12 :del
hole17:h-tsd87pt

Decoulping Cap

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Size	Document Number: Screw Hole / EMI	Rev 1A
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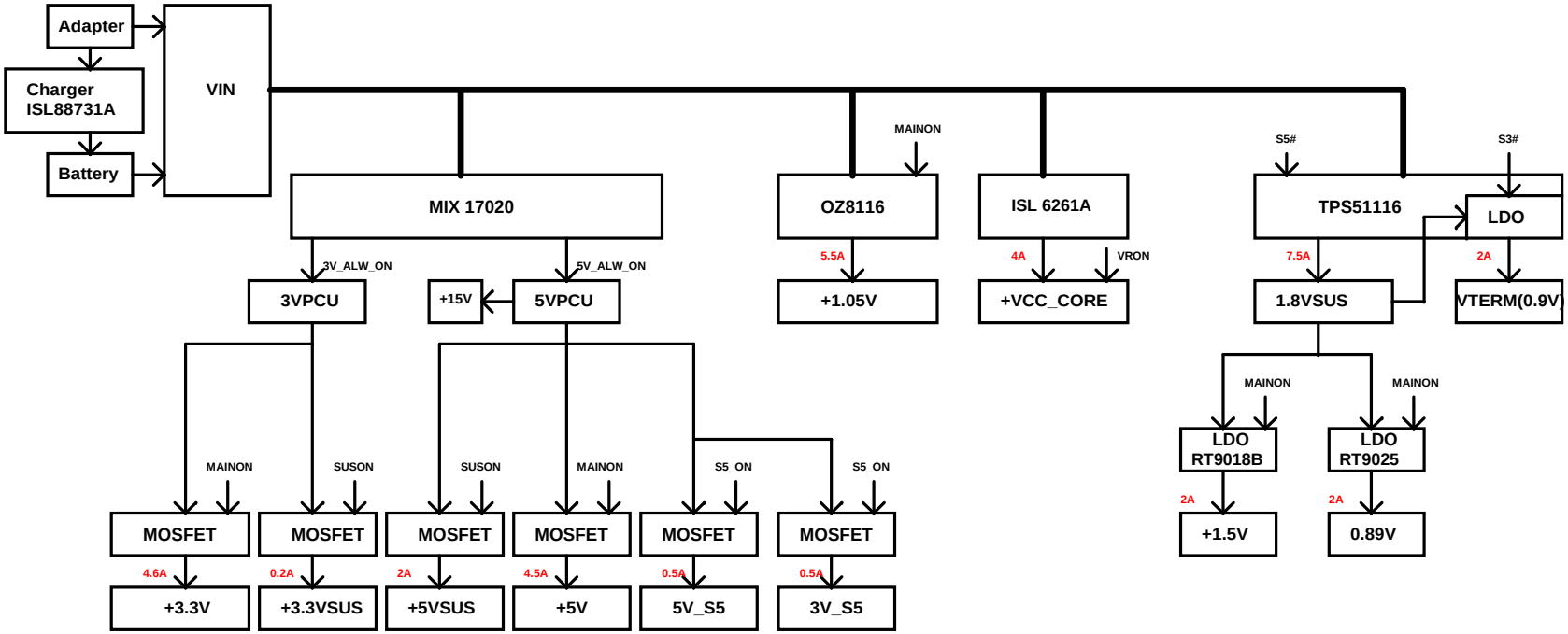

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PROJECT : FL2

Size	Document Number	Rev
	Power Block Diagram	1A

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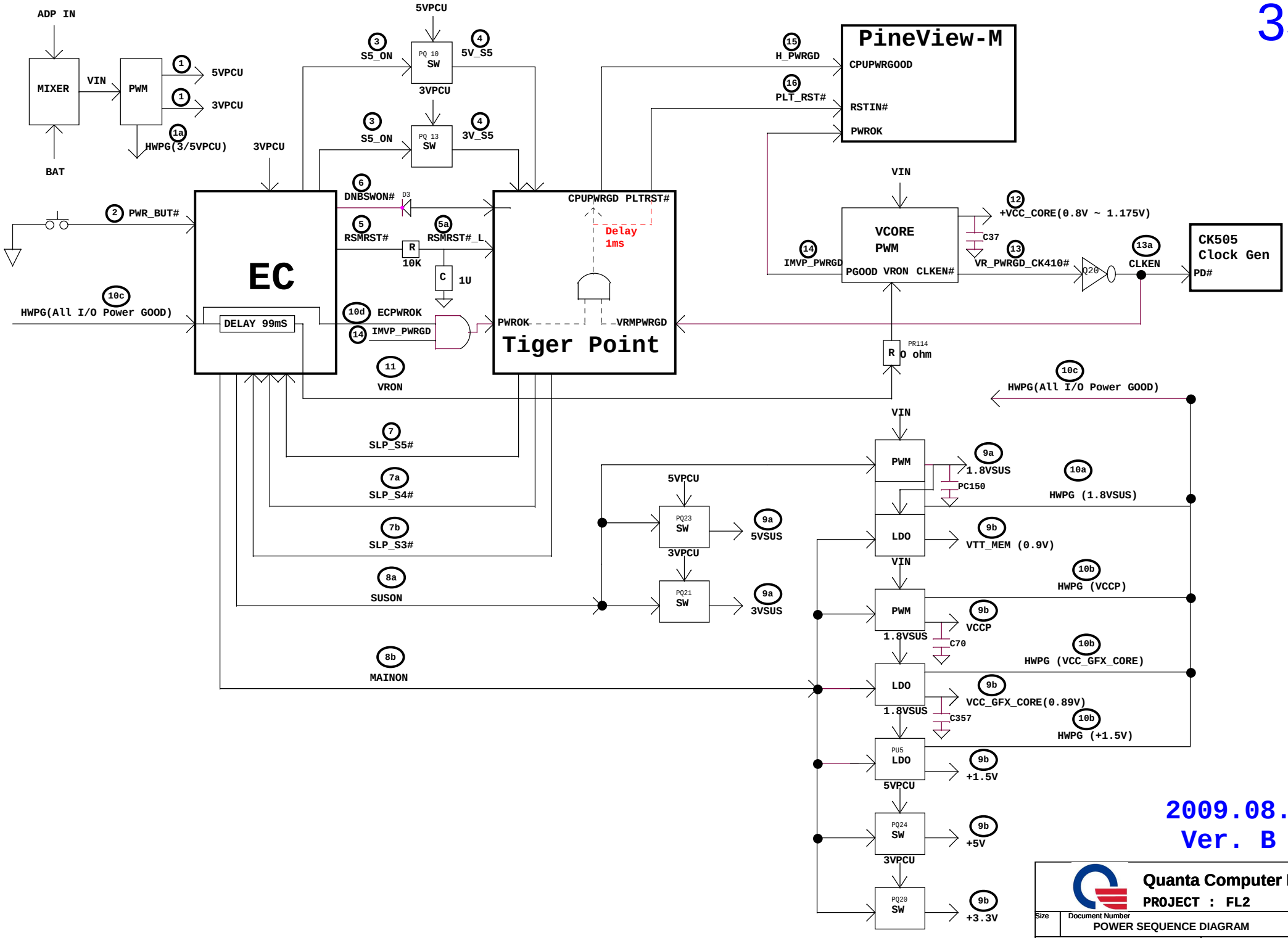

2009.08.03
Ver. B

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Size	Document Number	Rev
	POWER SEQUENCE DIAGRAM	1A

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MODEL:	REV:	CHANGE LIST:
FL2 MotherBoard	1A	FIRST RELEASE ON 2009/05/11
		Page 00 --> 1.
	2B	1. Add pull up resistor 10K on PM_SETCPU# and PM_STPPC# 2. Swap Clock GEN pin 31 to 32 3. Swap Clock GEN pin 50,51 to pin 35,34 4. Add off page symbol on CLKEN line 5. Change C297 Volume 0.01uF->0.1uF 6. Add capacitor 22uF (C352,C353) and 0.01uF(C360) on VCC_CORE 7. Swap capacitor 10uF to 22uF (C36) 8. Add capacitor 22uF(C357),0.01uF(C358) on VCC_GFX_CORE 9. Swap 0R(R73) to 600R @100MHZ(L24) Bead 10 Add 0.01uF (C361) on 1.8VSUS 11. Add 0.01uF (C362) on VCCP 12. Add 0.01uF (C363) on +1.8V 13. Swap R68 location to close chip 14 Add pull up resistor (R263) on WWAN_OFF# 15. Change R168 and R173 volume 10K-> 2.2K 16. Change sequence Add AND gate U21, C351, R261, R262 ,R264 ,R265 . 17. Add pull down resistor (R266, R267) on SA0 , SA1. 18. Improve backlight flash add U22,C355,R271 19. Modify SIM define (CN3) 20. Change audio VDD_IO voltage +1.5V->+3.3V 21. Del D13 on EAPD 22. Del D8 on SERIRQ 23. Swap EC ICH_RSMRST# (Pin33 -> Pin 99) 24. Add pull up resistor 10K (R269) on LID#_Panel Roll 25. Add 180K (R270) and 1000pF (C354) on FAN Circuit 26. Del R258 on USB_ON# 27. Add 22uF (C356) on WWAN_VCC 28. Del PR69 on HWPG 29. Del PR89A and PD10 on VRON Lline 30. Add R273 on SPDIF line 08/12 31. Add R274 on ICH_AZ_CODEC_BITCLK 08/12 32. Add C102 (10p) in BOM 08/12 33. L10 10uH ->0R 08/12 34. R150,R151 3.9K ->2.2K08/12 35. R14,R3,Q4,Q6, del in BOM (reserve)08/12 36. Swap CN7 part number (DMIC)08/12 37. Reserve R70,R275,R276,R73,369,C370,C372,C371 and C343,C345,C368,C367 in audio function for EMI and ESD08/12 38. Reserve R274, PC177, R273 in audio function for EMI 08/13 39. Cancel CHS_GND in LAN function of RJ4508/13 40. Swap S1 part number (Hall sensor)08/13 41. Swap CN4 part number (Key board connector)08/13 42. Add C55,C62,C71,C79,C85,C95,C100,C104,C107,C109,C112,C114,C117,C121,C122,C291,C293,C295,C298,C302,C303,C304,C306,C307 for EMI in Keyboard connector08/13
	3c	1.Del R101,R196 OHM 09/22'09 2.R189,R90,R201,R159,R74,R191,R205,R83,R177,R265,R121,L17,R9,R125,R12,R256 Use short pad. 09/22'09 3.change CN9 footprint 09/22'09 4.modify CN16 pin define 09/22'09 5. move U20 to CRT board
	4D	1.DEL 0R R275,R276,R70,R73 FOR audio output and DEL R221 for MB ID 2.ADD R222 for MB ID and ADD R264 10K 3.Change audio phone jack footprint CN13 4.DEL CN2 pin 2 Let it floating.

MODEL : FL2 MB

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
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35	1A	
36	1A	
37	1A	
38	1A	
39	1A	

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	FL2 EC Record List_A	1A

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MODEL:	REV:	CHANGE LIST:
FL2 MotherBoard		

MODEL : FL2 MB

PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
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38	1A	
39	1A	

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PROJECT : FL2

Size	Document Number	Rev
	FL2 EC Record List_B	1A

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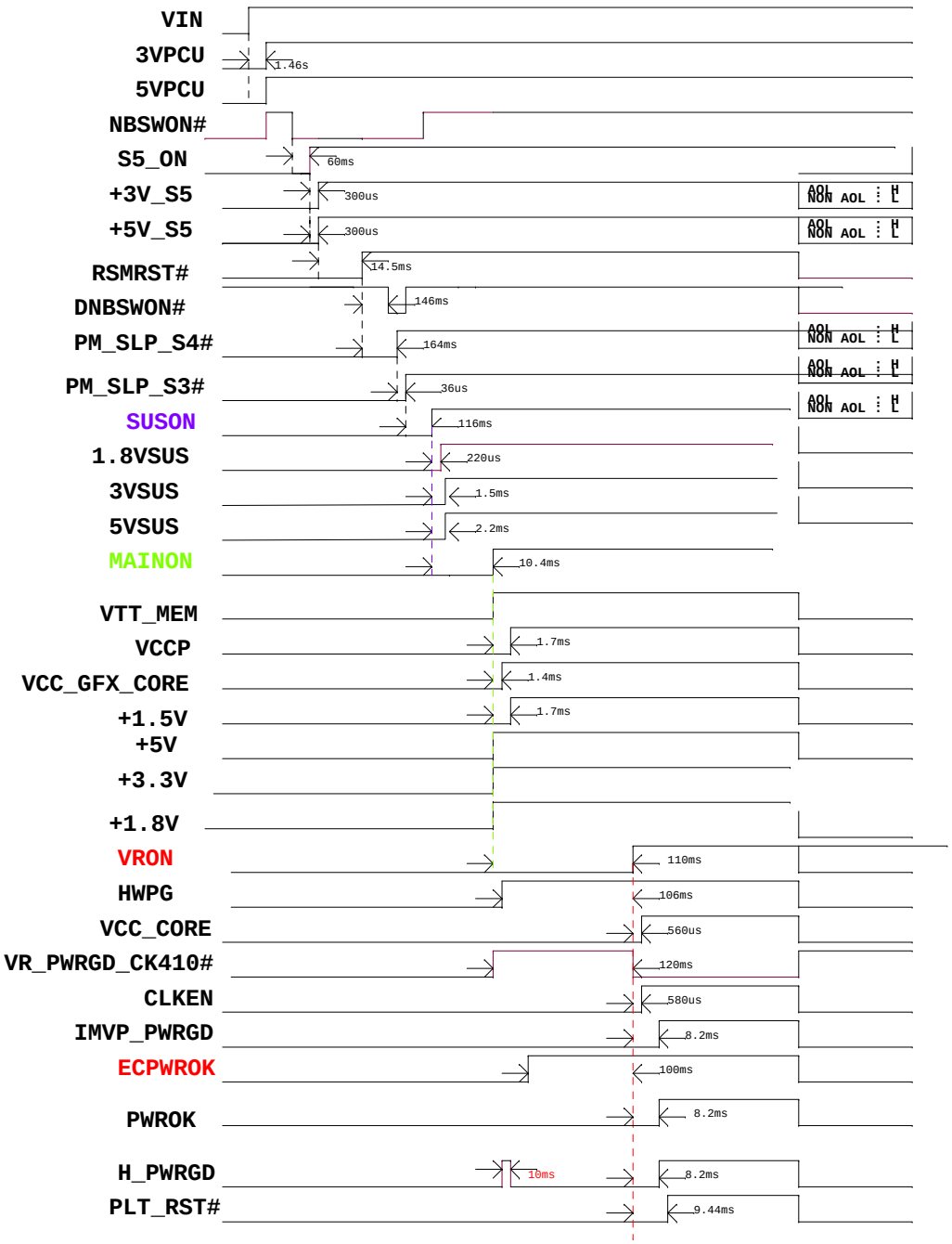

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PROJECT : FL2

Size	Document Number	Rev
	FL2 Power Sequence Ver B	1A

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