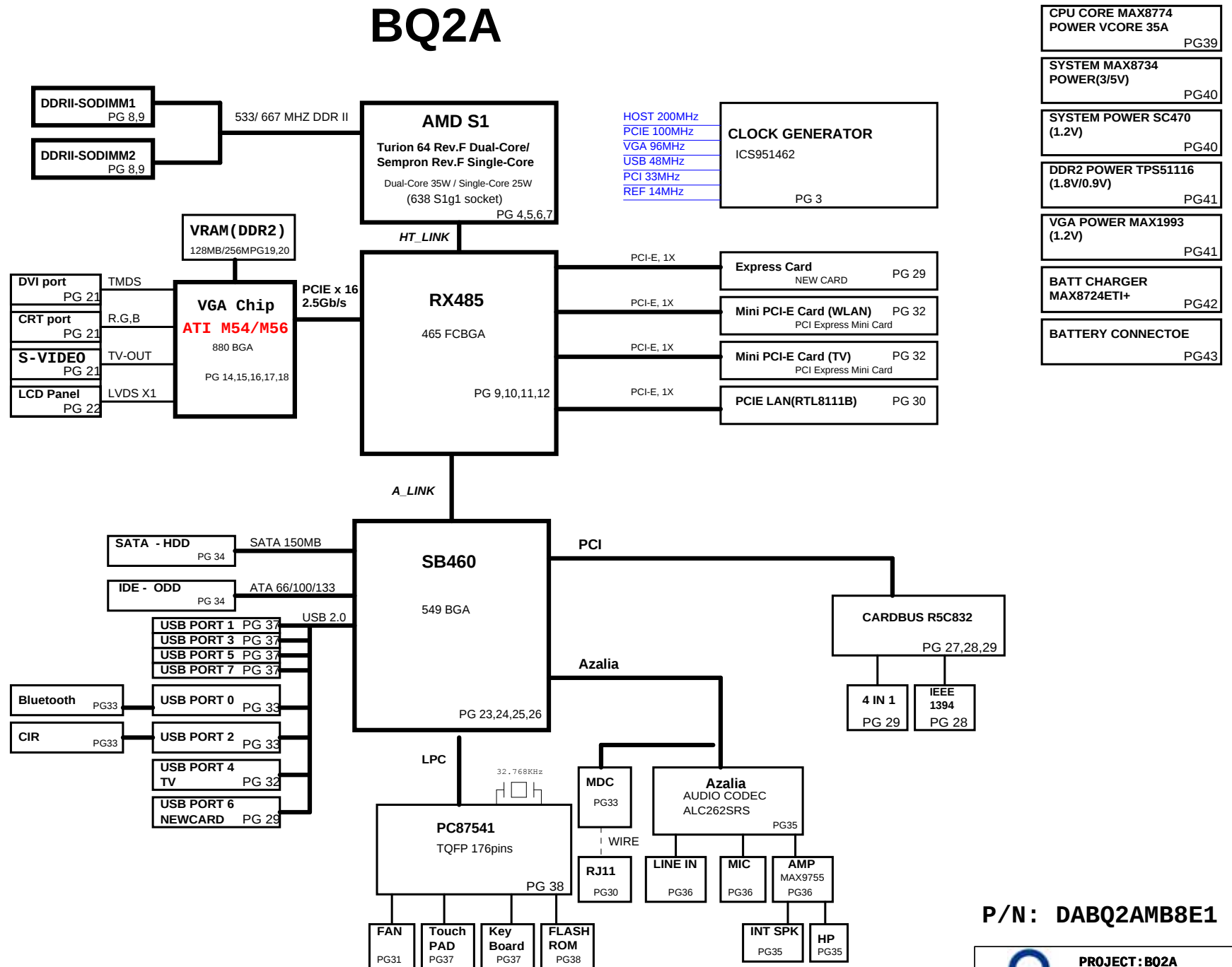


BQ2A BLOCK DIAGRAM 1

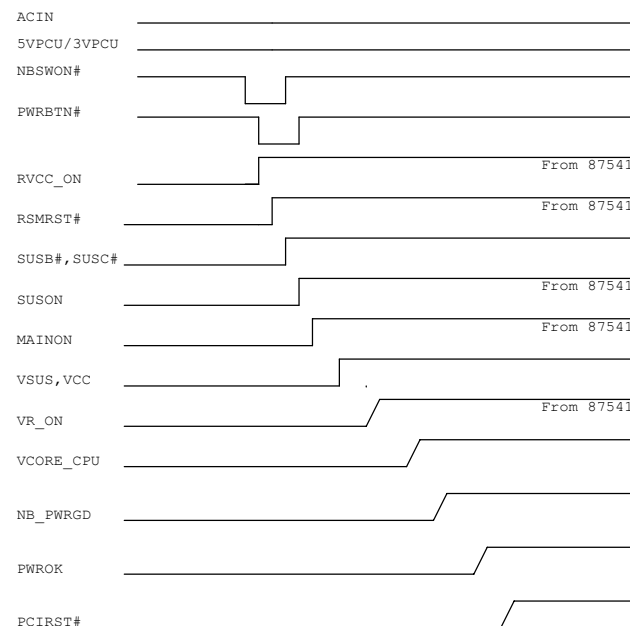


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Page 05:	AMD S1 DDR2
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Page 09:	DDR2 Termination
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Page 17:	M56 Straps
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Page 30:	PCIE LAN RTL8111B/RJ11/RJ45
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Page 38:	KBC PC87541/BIOS ROM
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Page 42:	1.8V/0.9V TPS51116
Page 43:	1.2V VGA_CORE MAX1993
Page 44:	Battery Charger MAX8724
Page 45:	Battery Connector

Voltage Rails

Power	Voltage	ON S0~S2	ON S3	ON S4	ON S5	Ctl Signal
9VPCU	9V	V	V	V	V	
5VPCU	5V	V	V	V	V	
3VPCU	3V	V	V	V	V	
RVCC3	3V	V	V	V		RVCC_ON
RVCC1.8	1.8V	V	V	V		RVCC_ON
5VSUS	5V	V	V			SUSON
3VSUS	3V	V	V			SUSON
1.8VSUS	1.8V	V	V			SUSON
VCC5	5V	V				MAINON
VCC3	3V	V				MAINON
VCC2.5	2.5V	V				MAINON
CPU_VDDA	2.5V	V				MAINON
VCC1.8	1.8V	V				MAINON
VCC1.5	1.5V	V				MAINON
VCC1.2	1.2V	V				MAINON
VGA_CORE	1.2V-1V	V				MAINON
SMDDR_VTERM	0.9V	V				MAINON
VCC_CORE	By CPU	V				VR_ON

Power On Sequence



PCB STACK UP

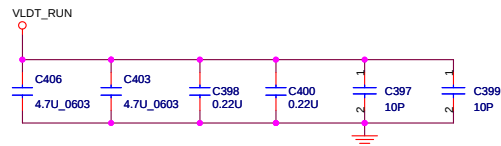
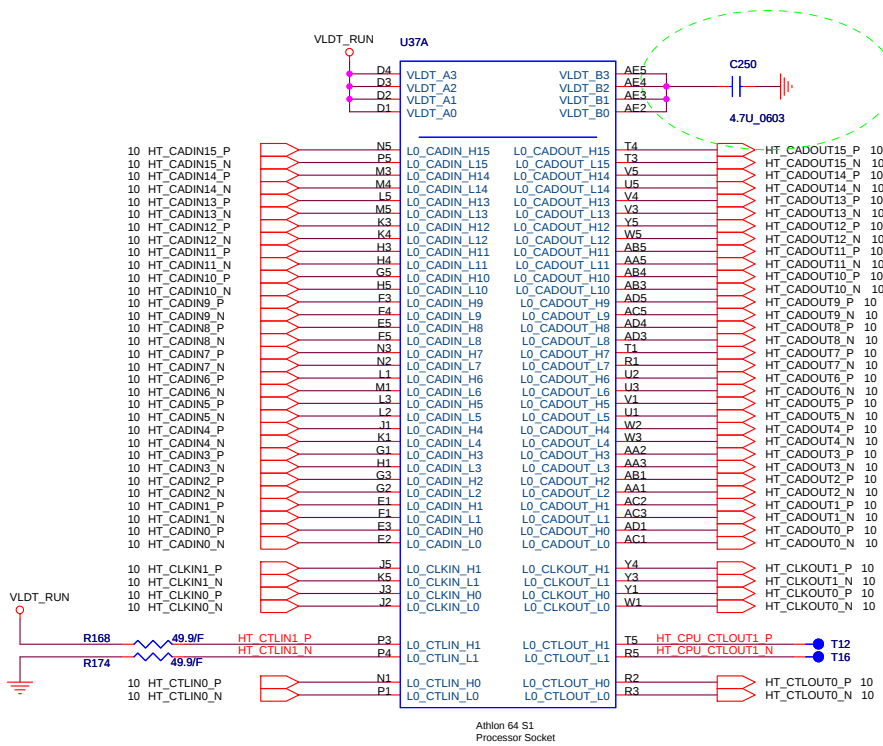
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

PCI DEVICES IRQ ROUTING

BQ2A PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
R5C832	AD17	REQ0# / GNT0#	INT E/F#

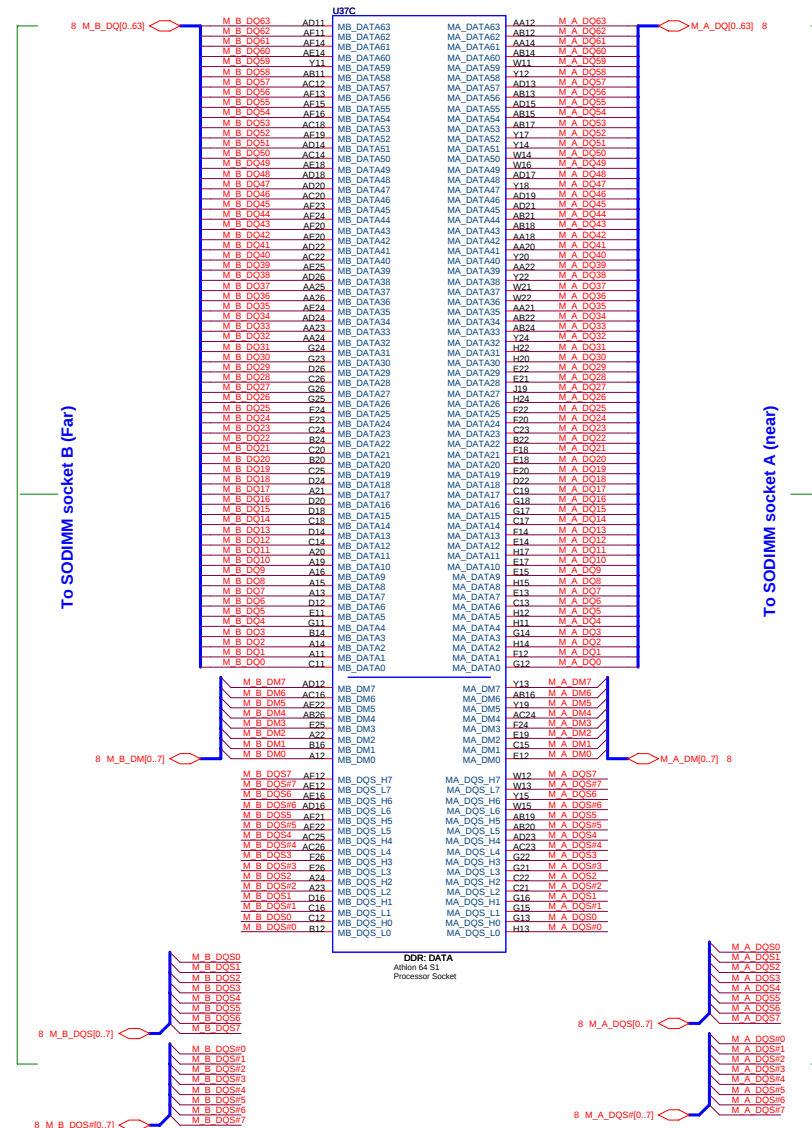
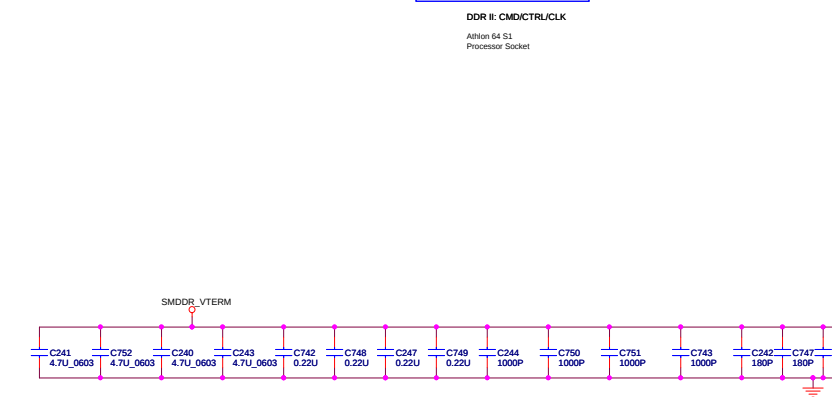
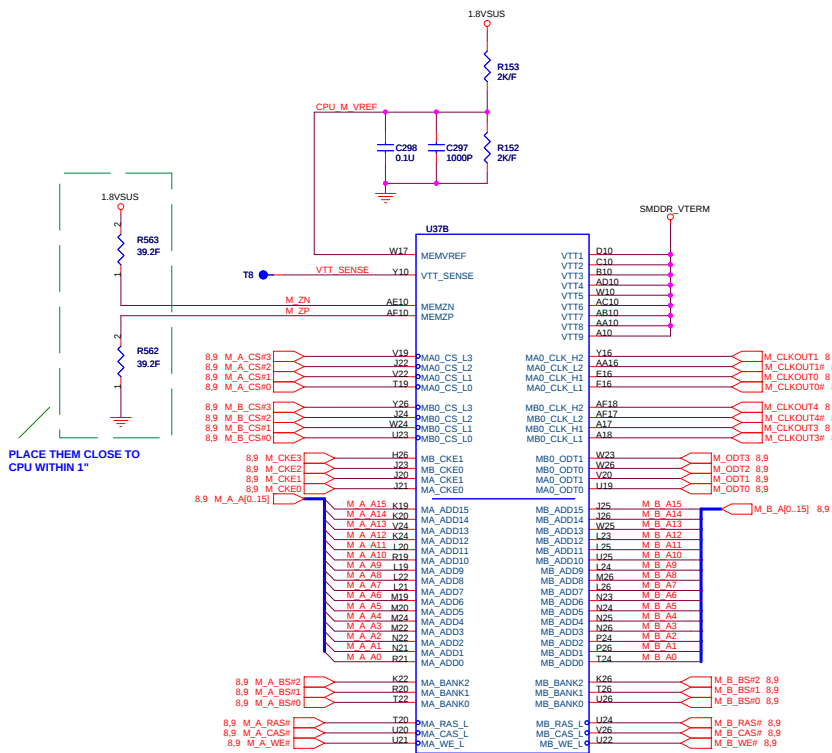
SB460 GPIO Setting

GPI07 :LCD backlight control
GPI031 :Restet R5C832

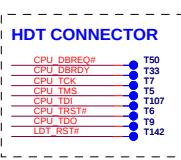
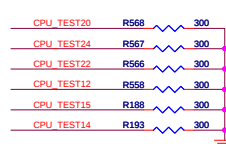
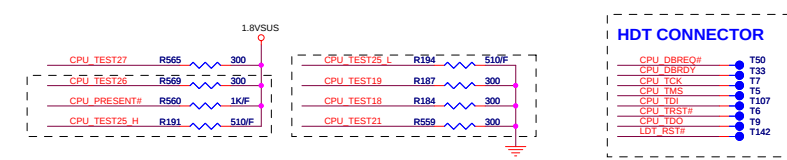
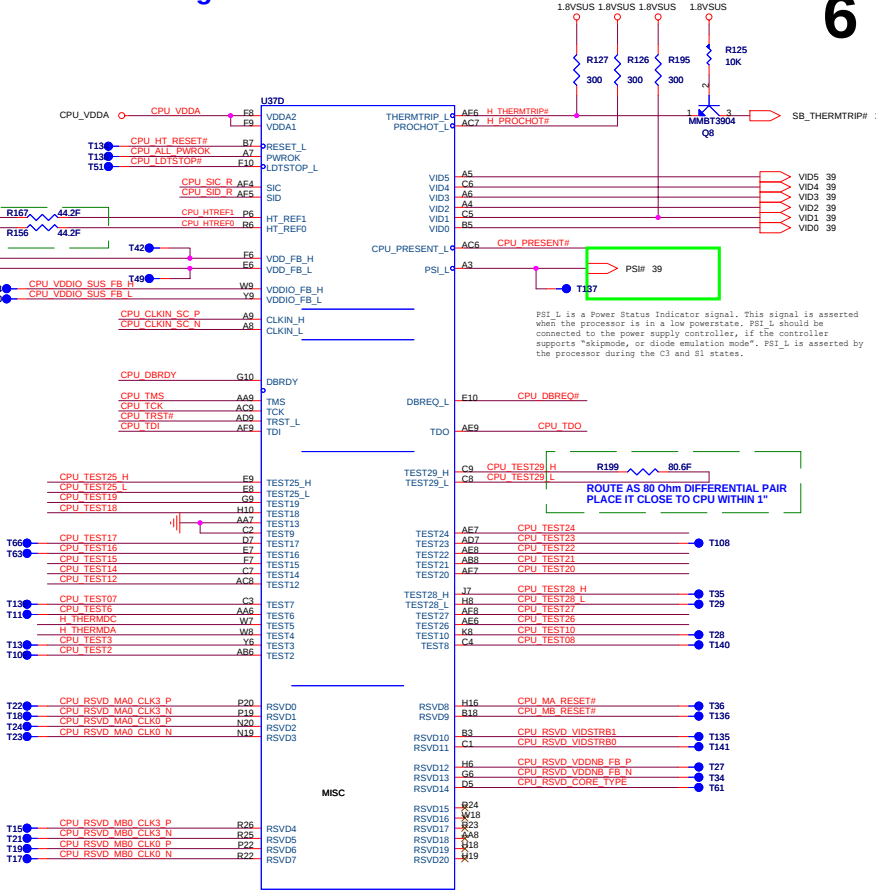
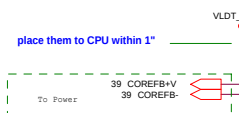
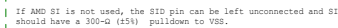


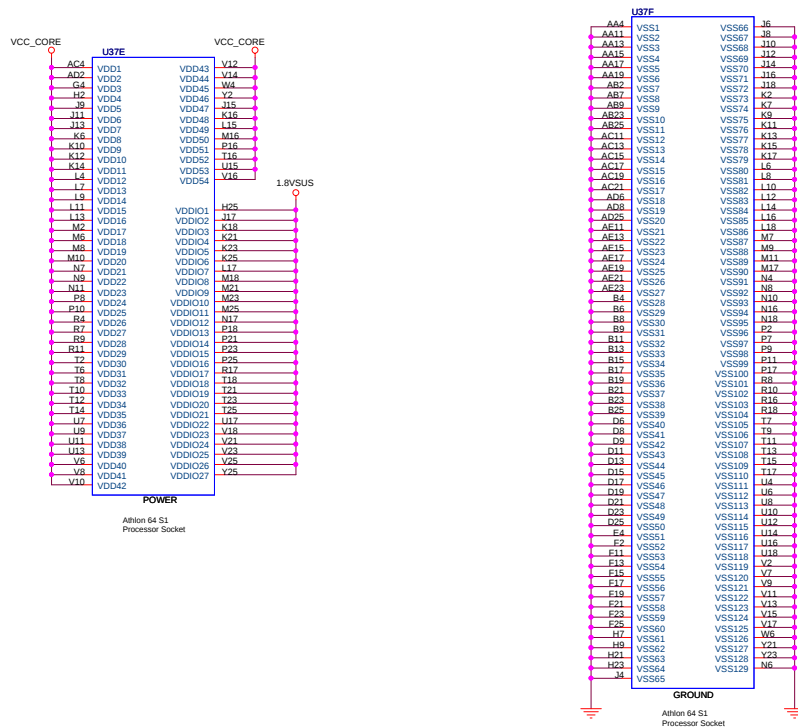
PROJECT : BQ2A
Quanta Computer Inc.

Processor DDR2 Memory Interface

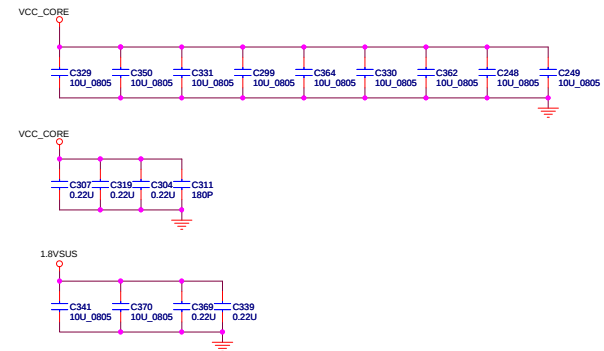


6

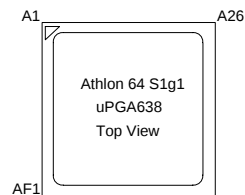
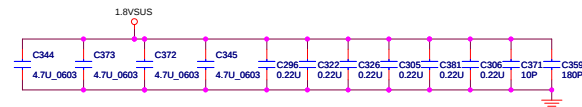




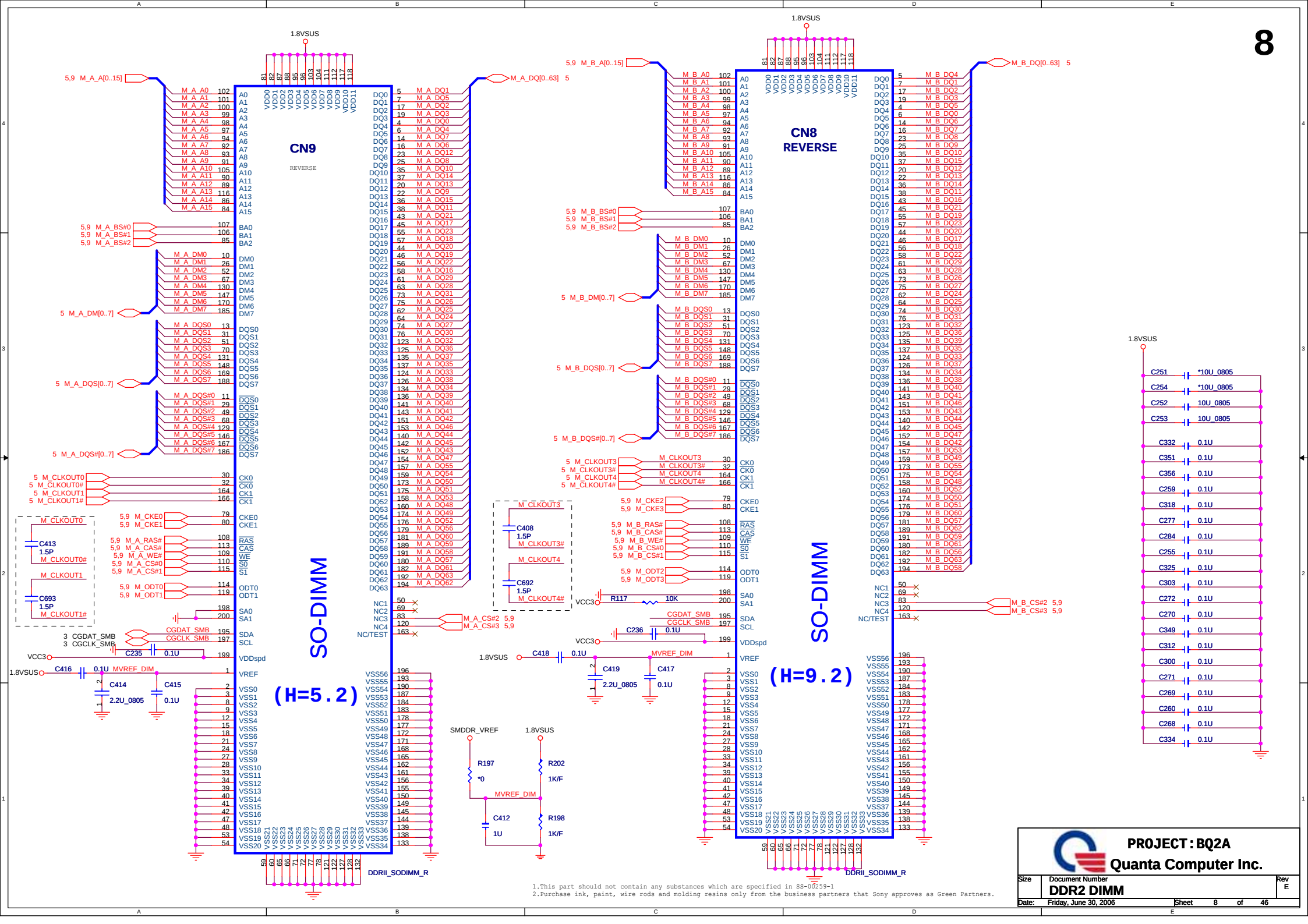
BOTTOMSIDE DECOUPLING

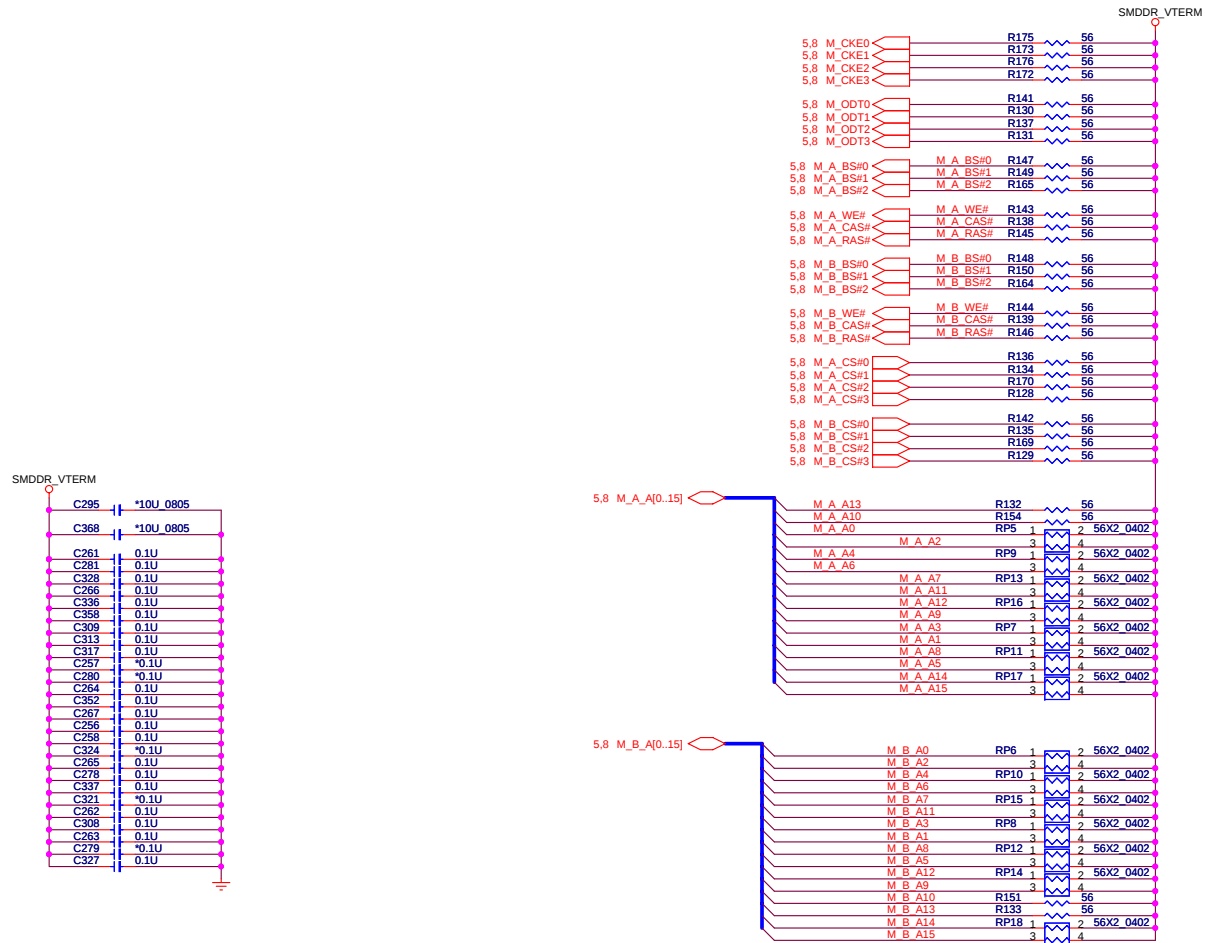


DECOUPLING BETWEEN PROCESSOR AND DIMMS PLACE CLOSE TO PROCESSOR AS POSSIBLE



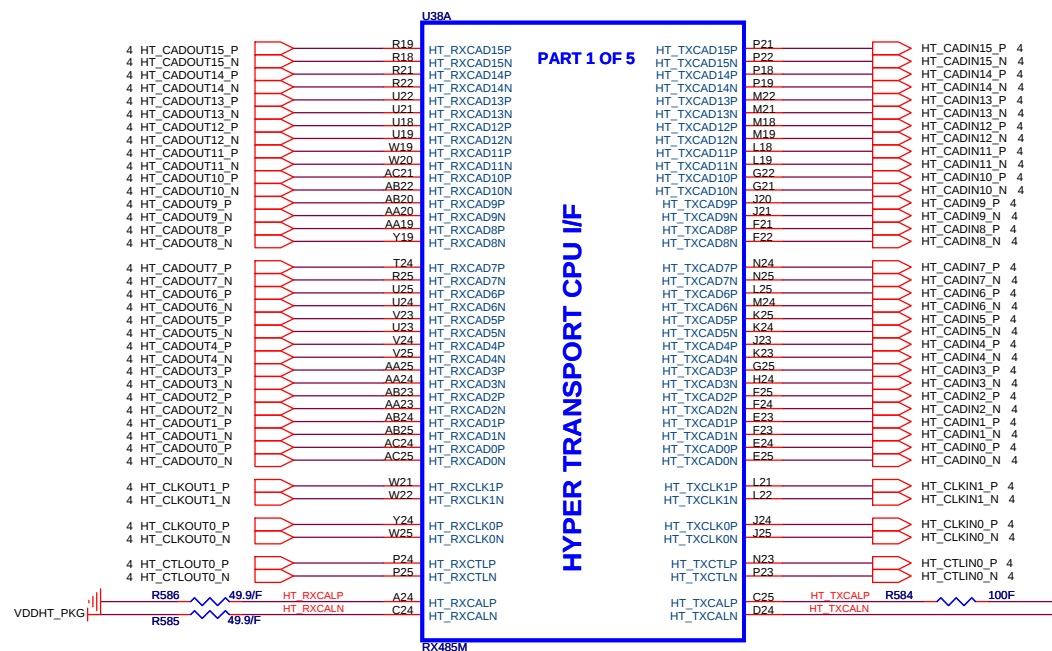
PROCESSOR POWER AND GROUND

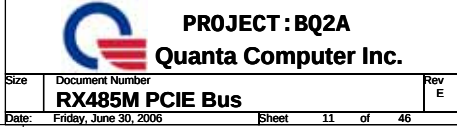


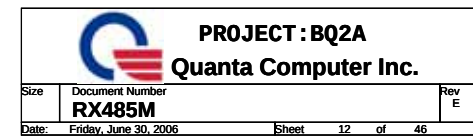


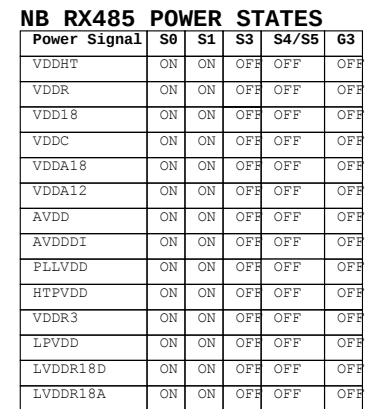
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Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 Termination	E
Date:	Friday, June 30, 2006	Sheet 9 of 46

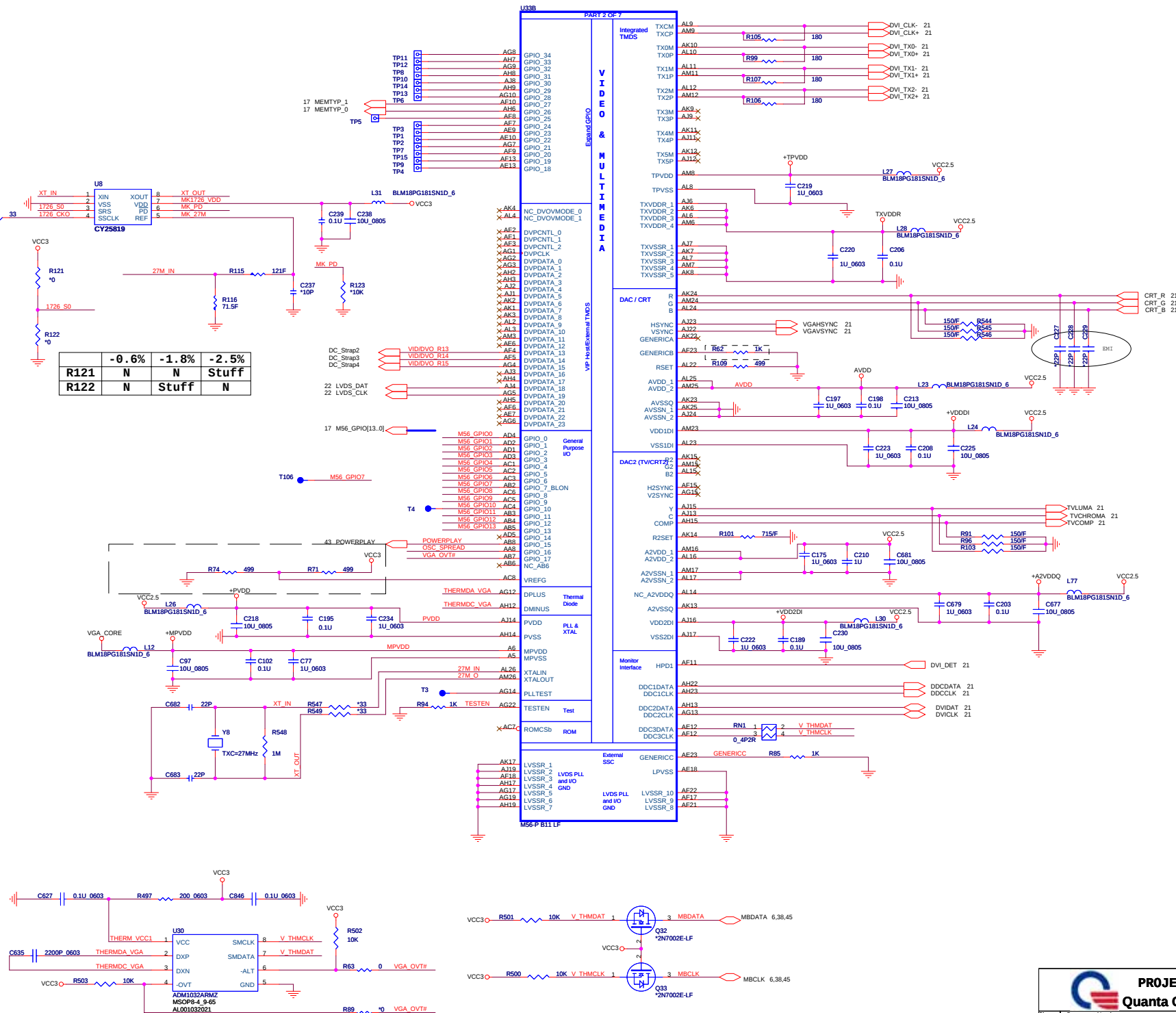




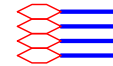




		-0.6%	-1.8%	-2.5%
R121	N	N	Stuff	N
R122	N	Stuff	N	N



11 PEG_RXP[15:0]
11 PEG_RXN[15:0]
11 PEG_TXP[15:0]
11 PEG_TXN[15:0]

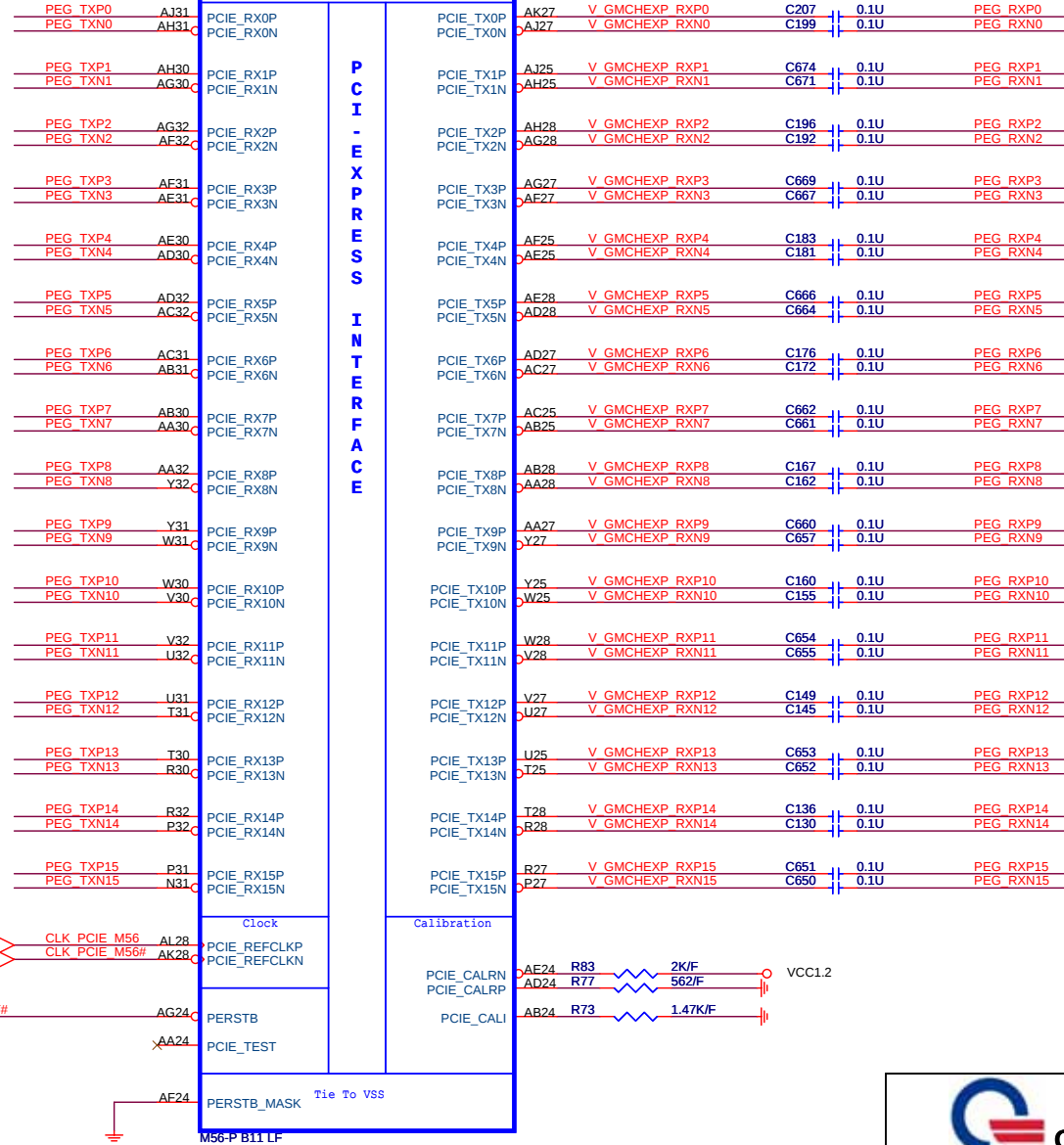


U33A

PART 1 OF 7

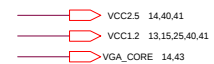
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PROJECT : BQ2A
Quanta Computer Inc.

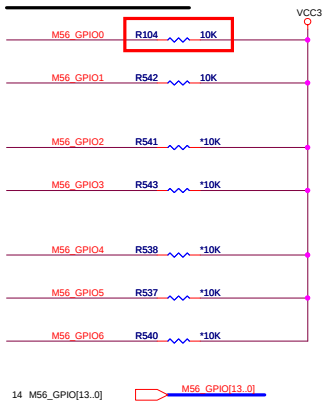
Size	Document Number	Rev
	M56P PCIe Bus	E
Date:	Friday, June 30, 2006	Sheet 15 of 46



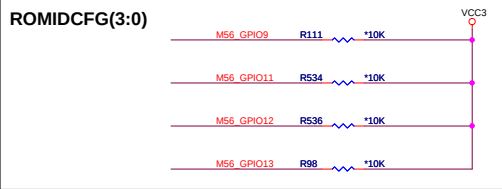
M56-P Strap

STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	Full swing	10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE - SETTING DEPENDS ON CHIPSET SEE M2X DATABOOKS	TBD
STRAP_PCIE_MODE	GPIO(3:2)	PCI-EXPRESS 1.0A MODE	DO NOT INSTALL 10K RESISTORS
STRAP_REVERSE_LANES	GPIO4	REVERSE PCIE LANES -NON REVERSED	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE	GPIO5	DO NOT FORCE COMPLIANCE STATE QUICKLY	DO NOT INSTALL 10K RESISTORS
STRAP_CM_RANGE	GPIO6	CM RANGE - NORMAL	DO NOT INSTALL 10K RESISTORS
ROMIDCFG(3:0)	ROMID (4:1)	SERIAL FLASH ROM TYPE SELECT - SERIAL M25P10 ROM	0000

OPTION STRAPS



14 M56_GPIO[13:0] M56_GPIO[13:0]



Memory ID

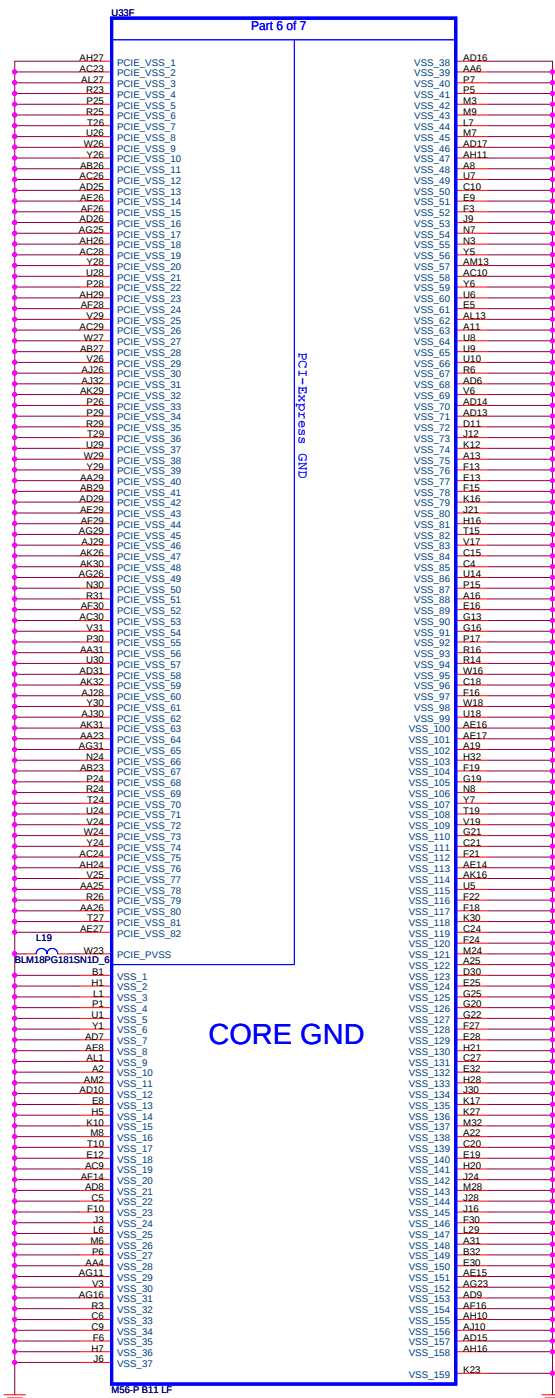
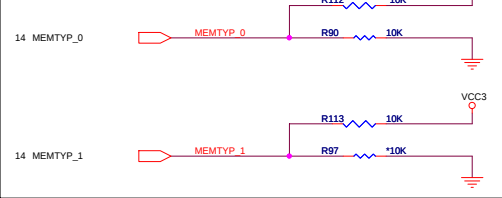
Memory identification for BIOS

00 - DDR2 16X16X4pcs 128MB

10 - DDR2 16X16X8pcs 256MB

01 - DDR2 32X16X4pcs 256MB

11 - DDR2 32X16X2pcs 128MB

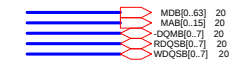


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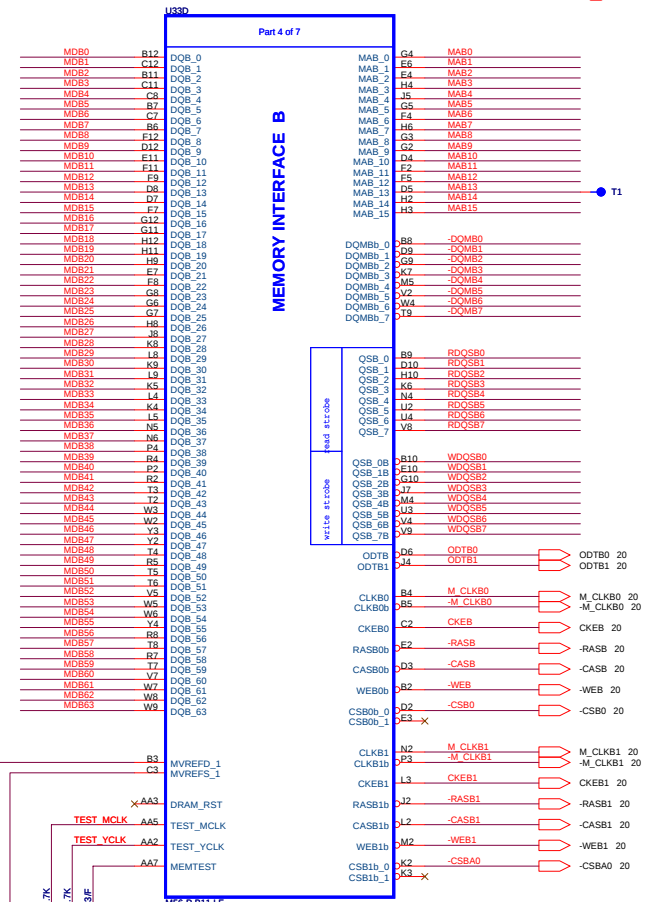
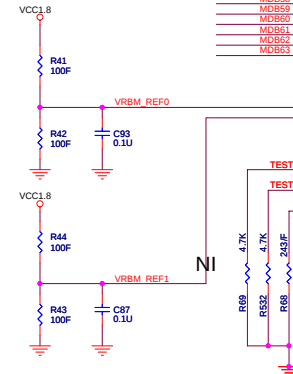
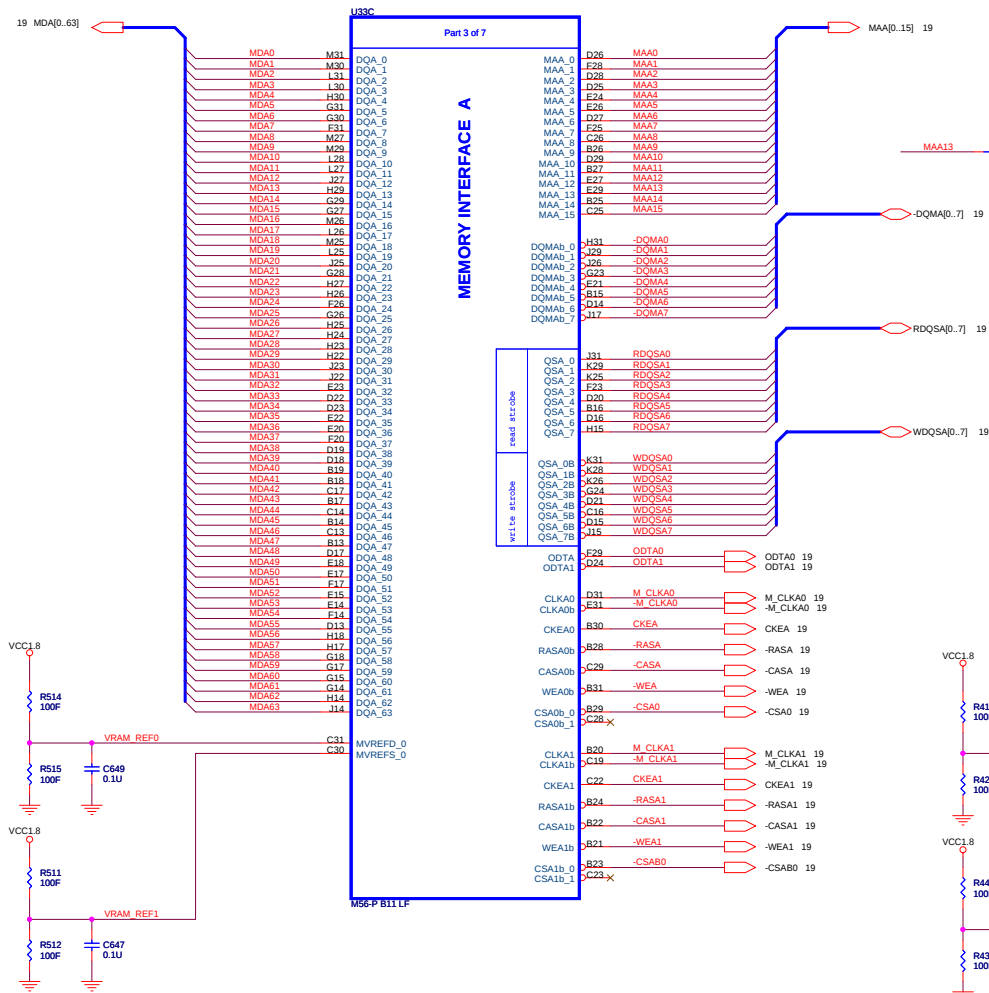
RV410 MEMORY CHANNELS A and B

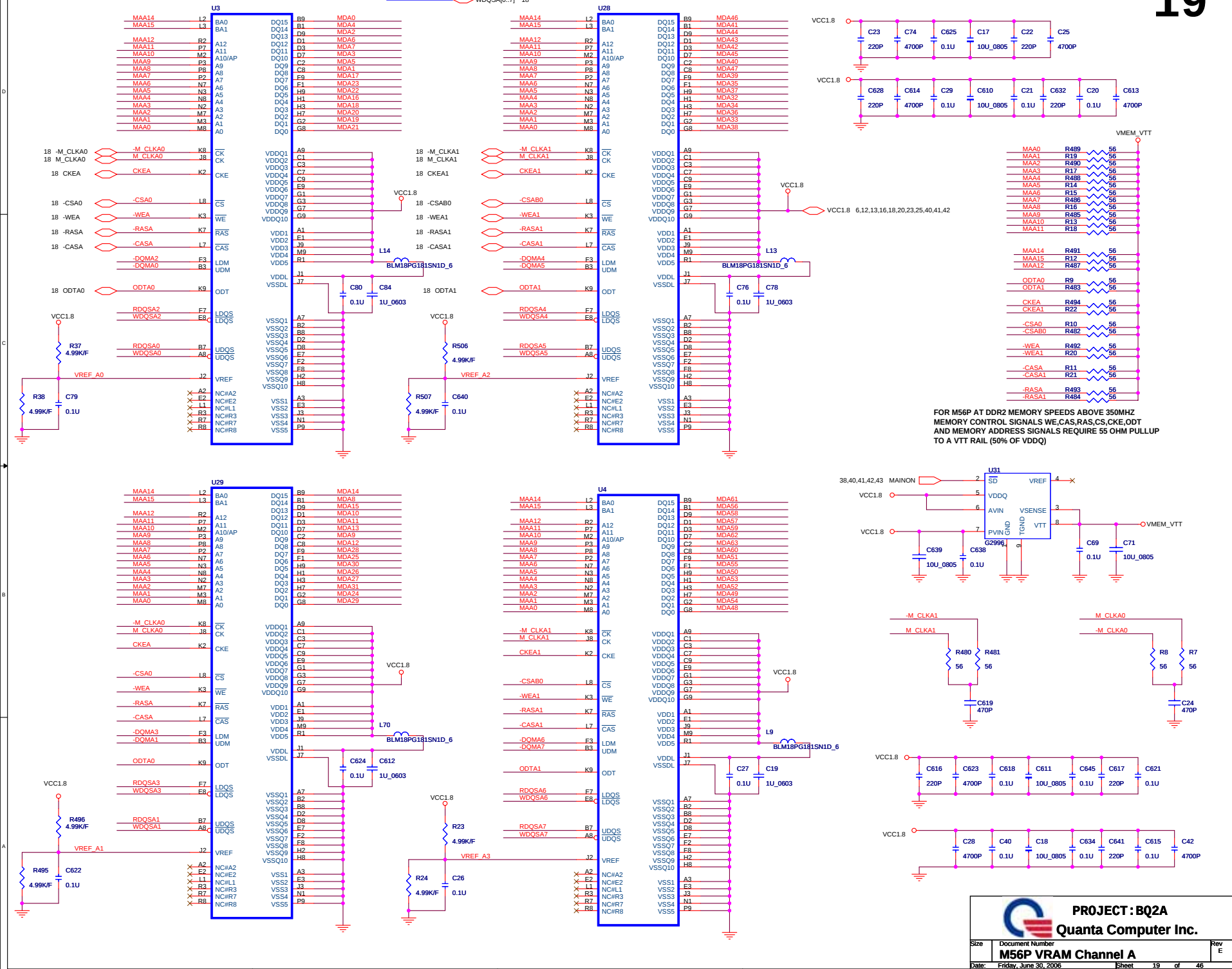
Channel A

Channel B

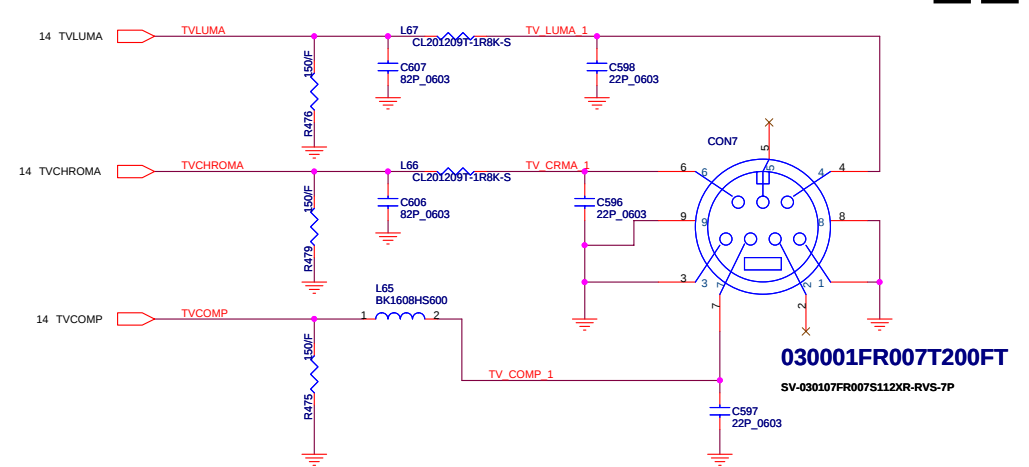
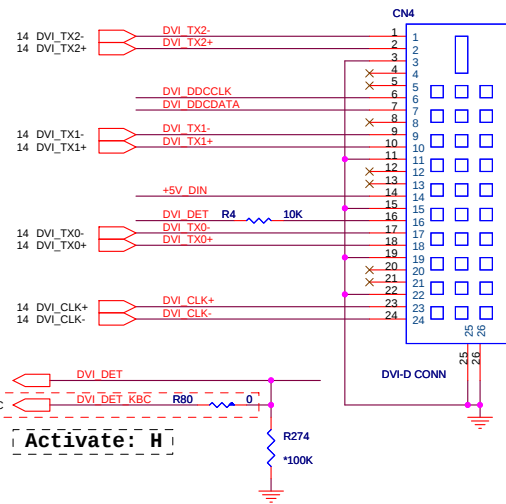
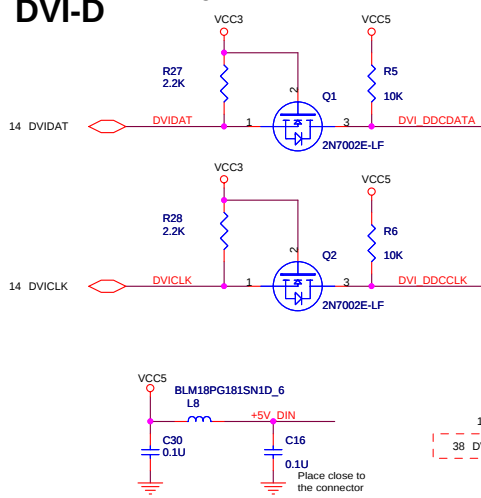


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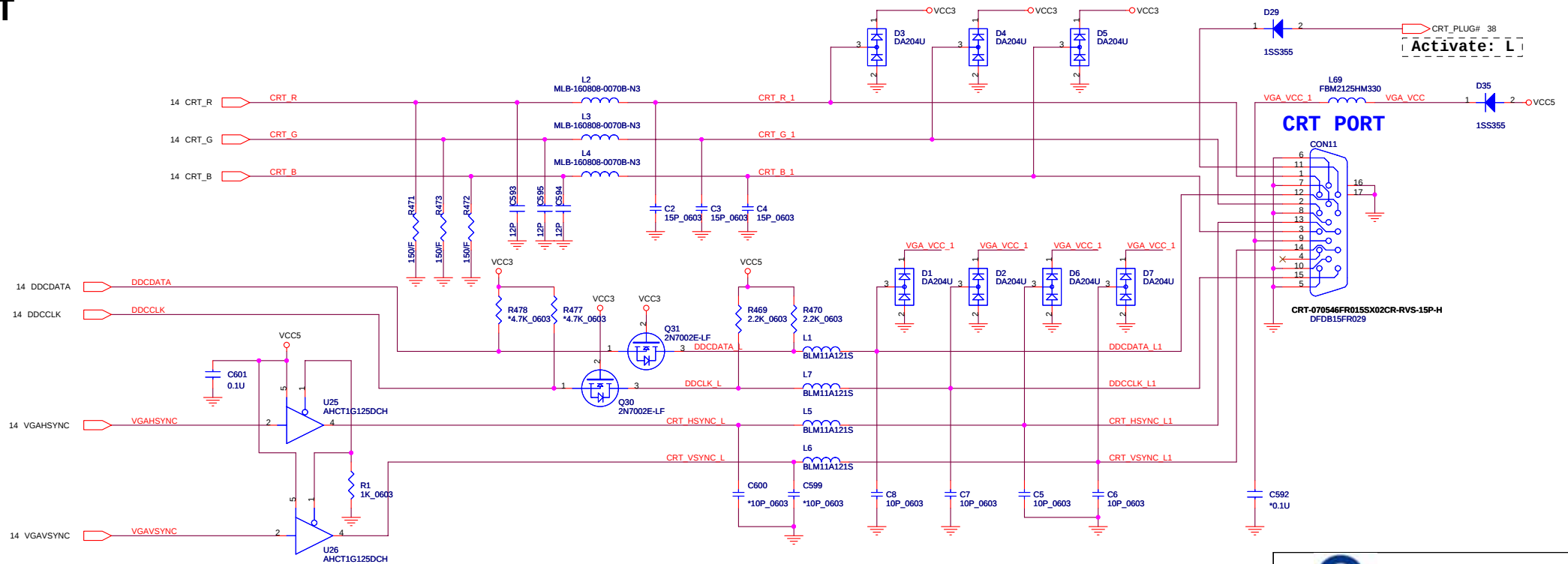




DVI-D



CRT

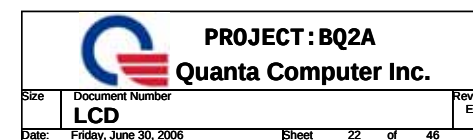




LID



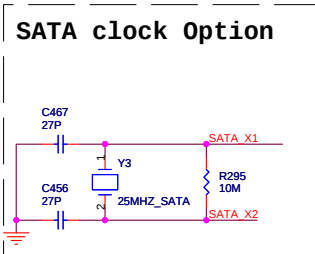
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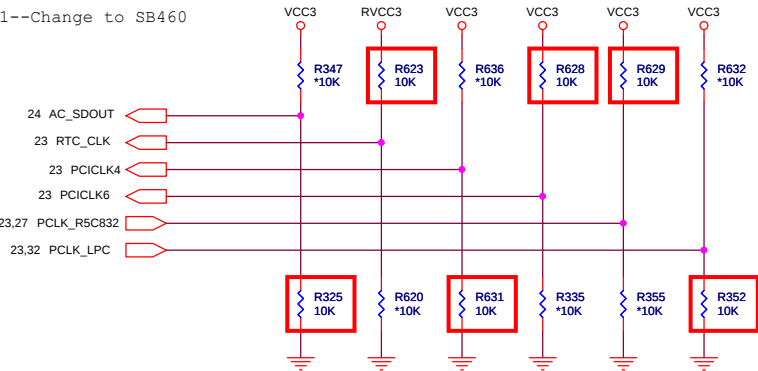


PROJECT: BQ2A
Quanta Computer Inc.



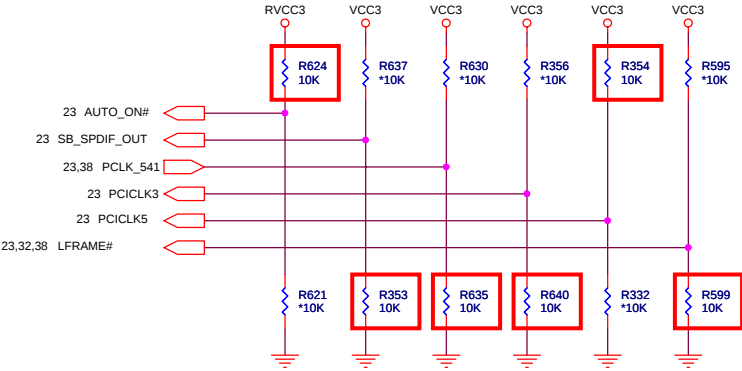
 PROJECT : BQ2A Quanta Computer Inc.		
Size	Document Number SB460	Rev E
Date:	Friday, June 30, 2006	Sheet 25 of 46

Edison-11/01--Change to SB460



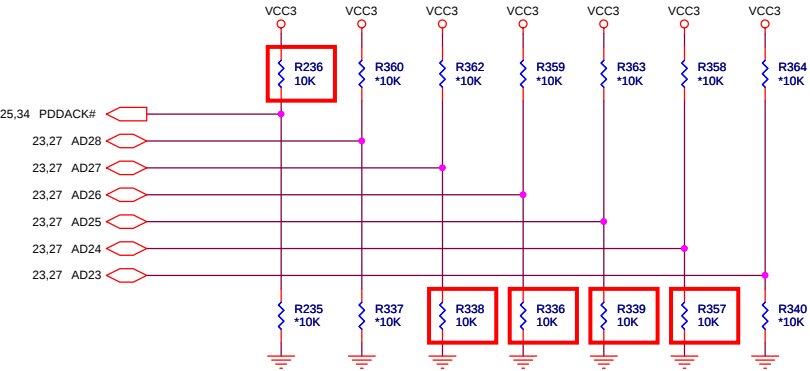
REQUIRED STRAPS

				PCLK_R5C832	PCLK_LPC
PULL HIGH	AC_SDOUT	RTC_CLK	PCICLK4	PCICLK6	PCI_CLK0
	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT	DEFAULT



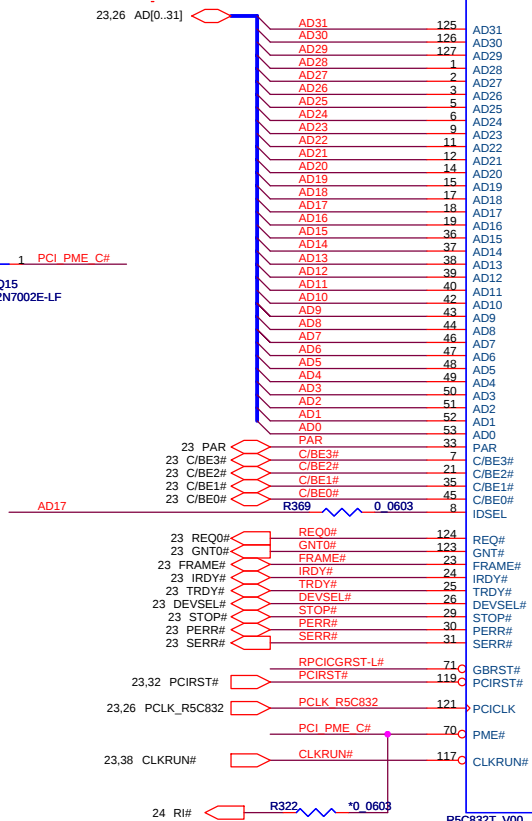
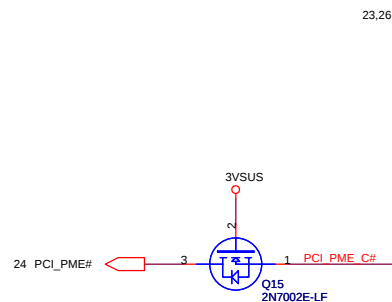
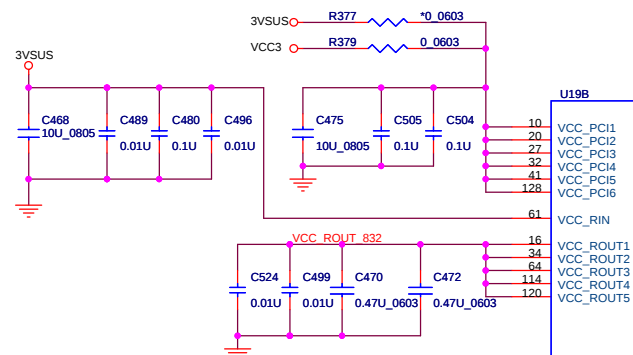
	AUTO_ON#	SB_SPDIF_OUT	PCLK_541	PCICLK3	PCICLK5	LFRAME#
	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

BIOS ENABLE AFTER STARTUP



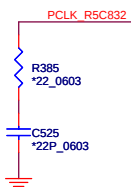
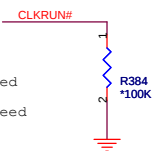
DEBUG STRAPS

	PDDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

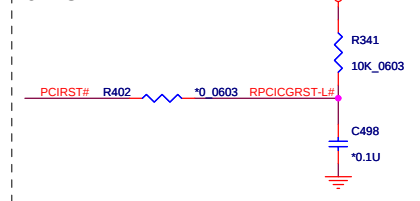


CoreLogic CLOCKRUN#

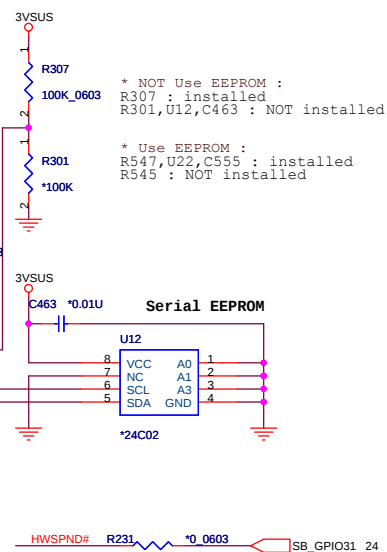
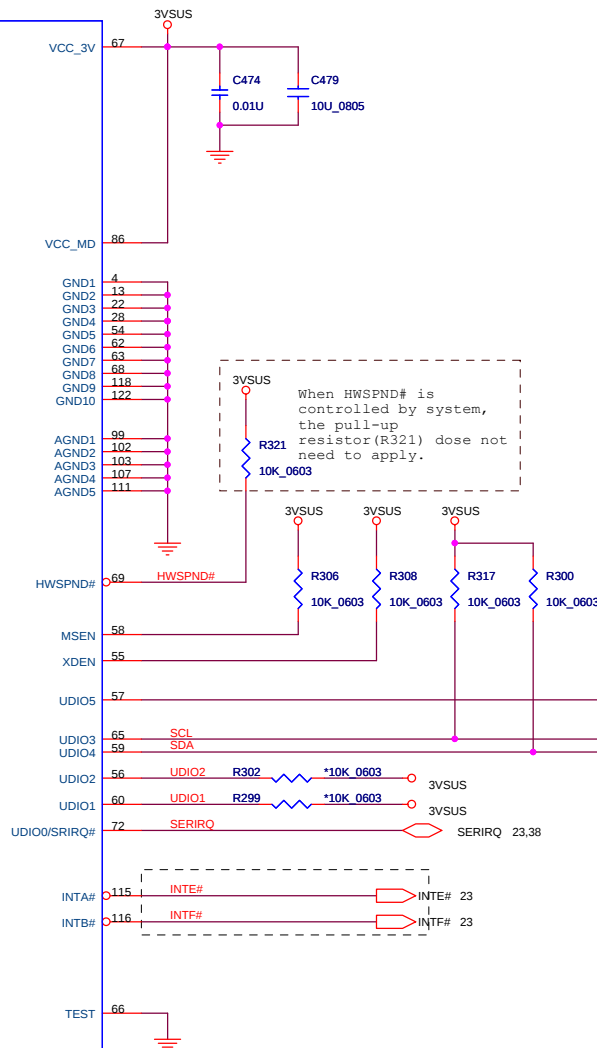
When CLKRUN# is controlled by system, the pull-down resistor(R14) dose not need to apply.

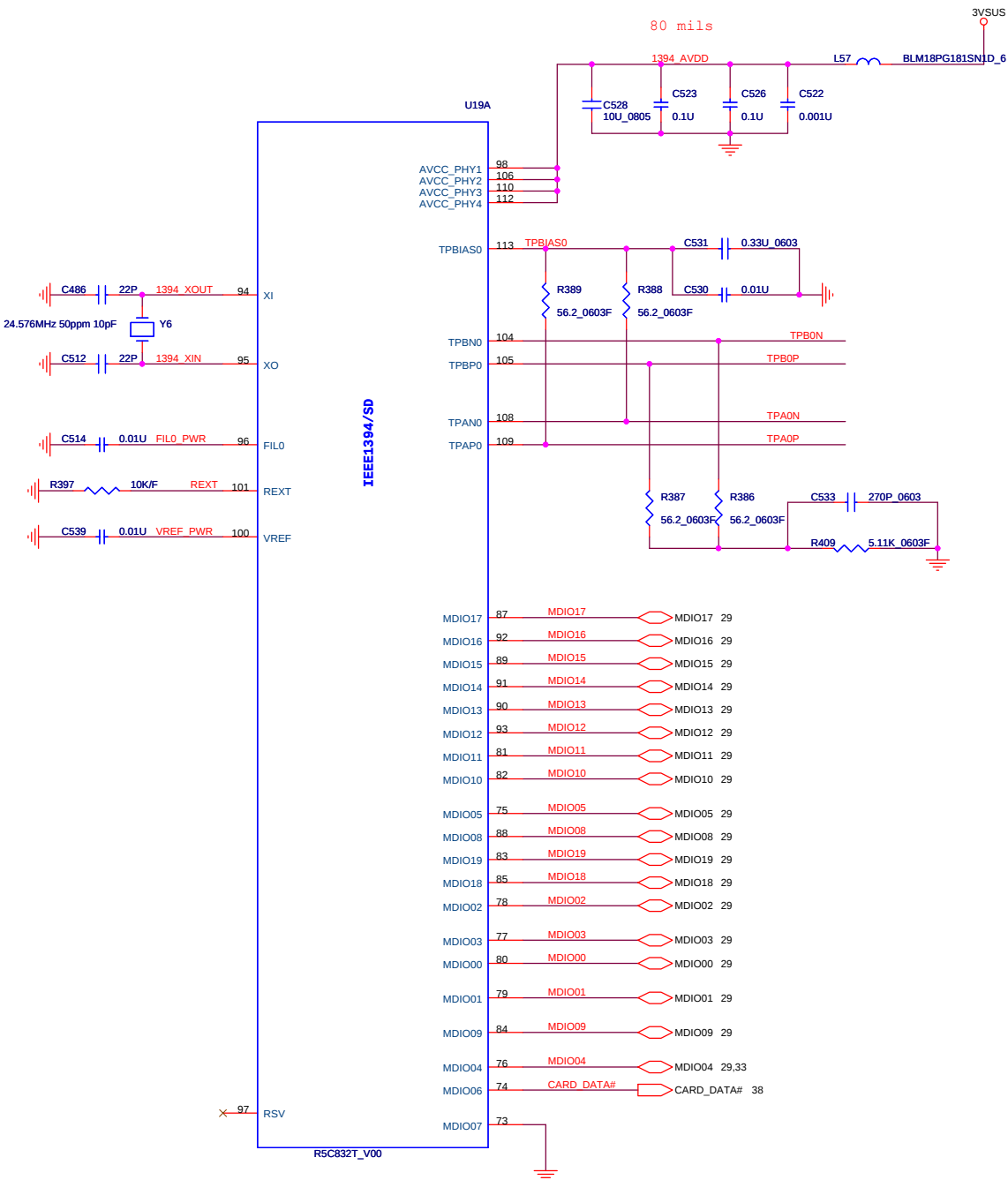


GBRST#

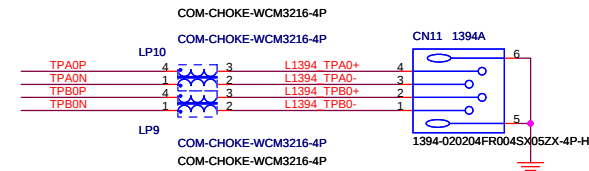


PCI / OTHER

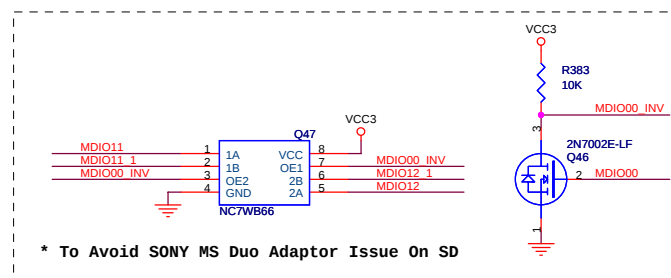
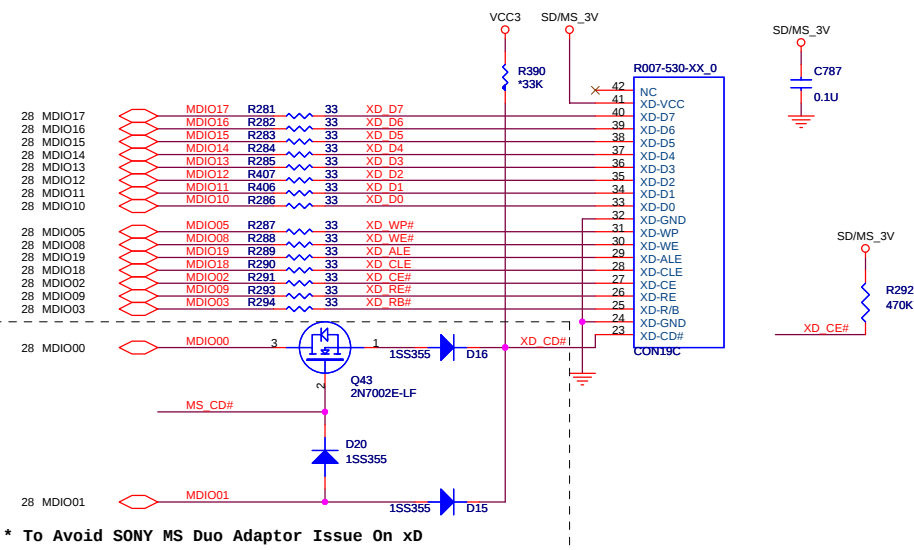
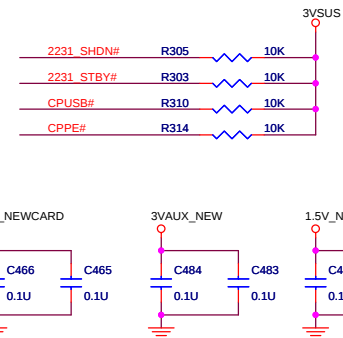




AS CLOSE AS POSSIBLE TO
1394 CONNECTOR.

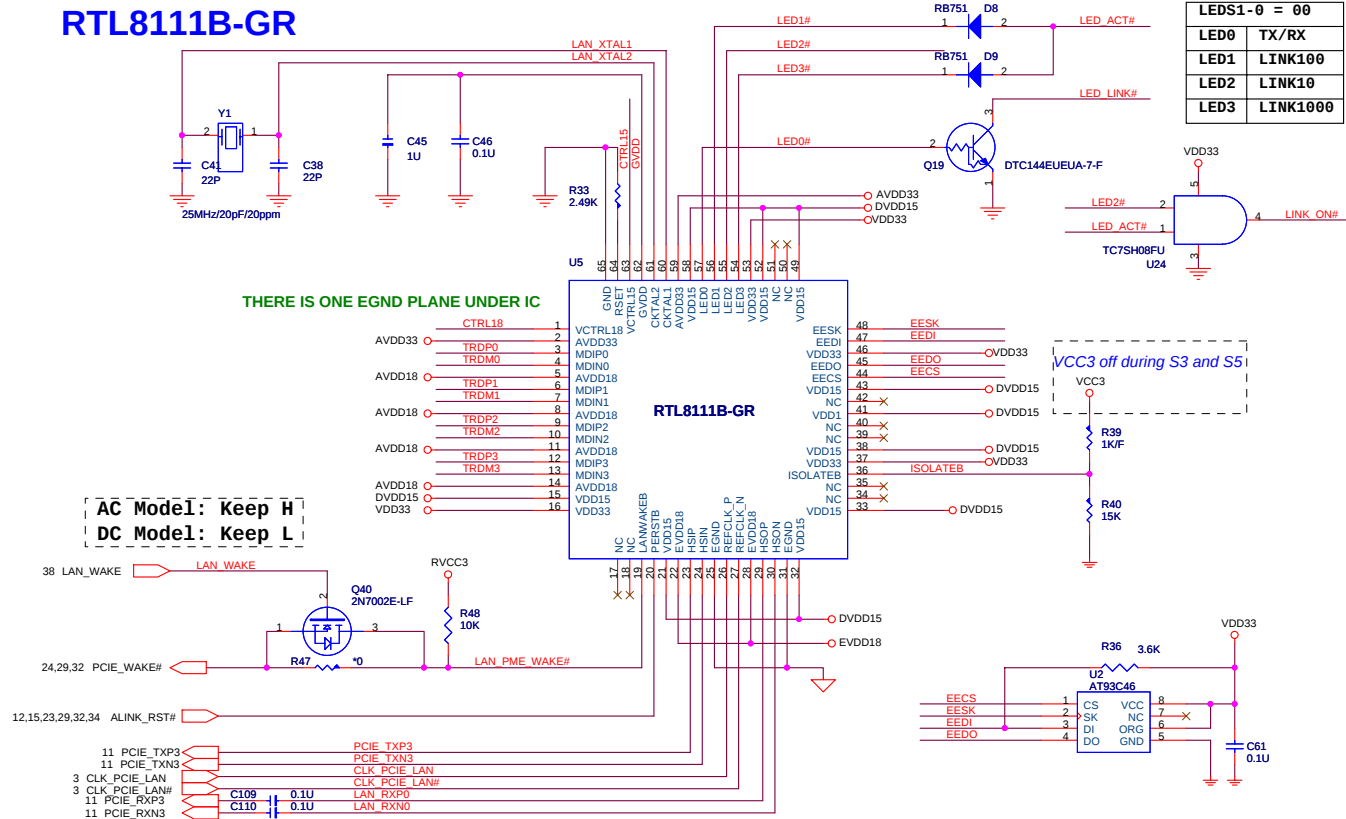


	Vendor ID	Device ID
1394	1180	0832
SD	1180	0822
MMC	1180	0843
MS	1180	0592
xD	1180	0852

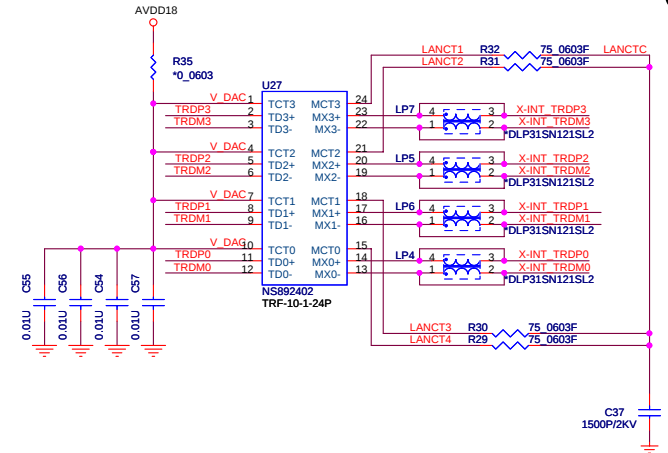


	MDI000	MDI001
SD/MMC	L	H
MS	H	L
xD	L	L

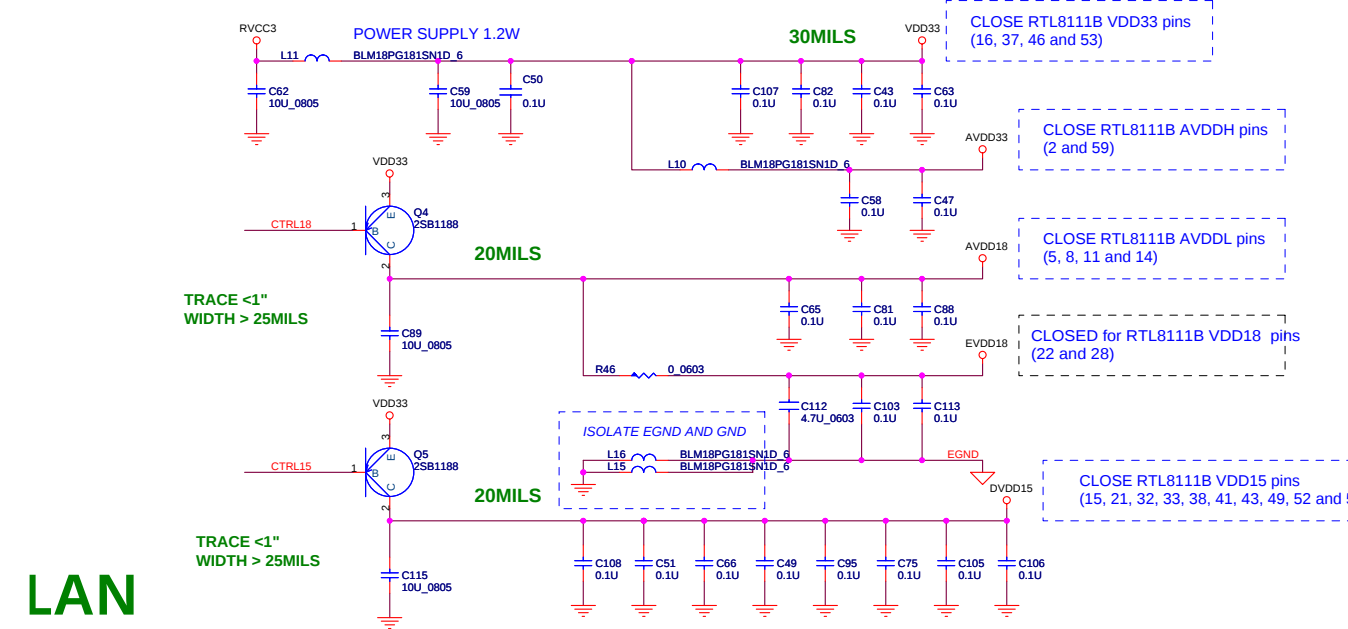
RTL8111B-GR



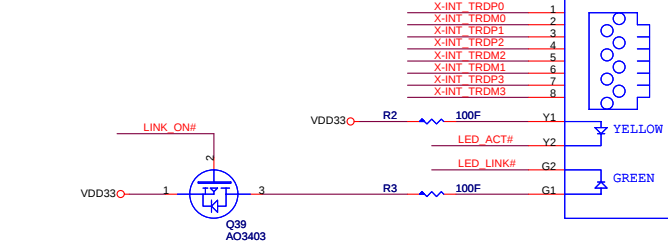
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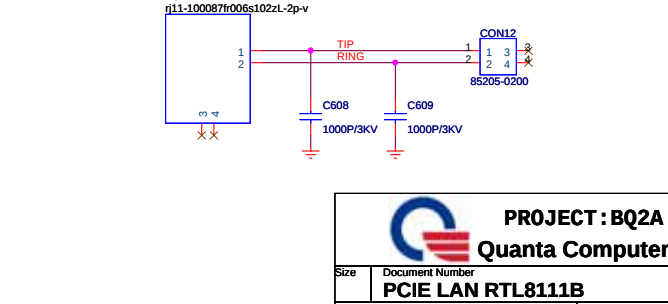
POWER SUPPLY



RJ45

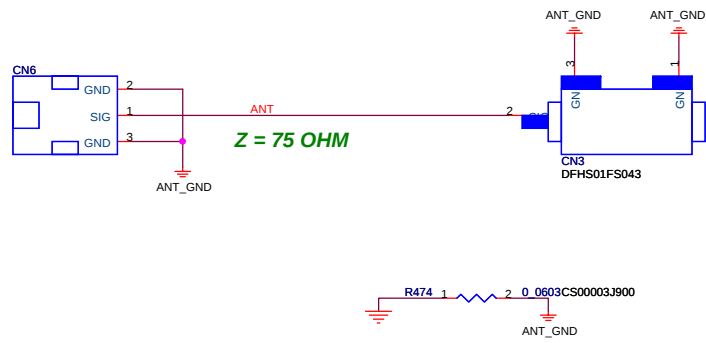


RJ11

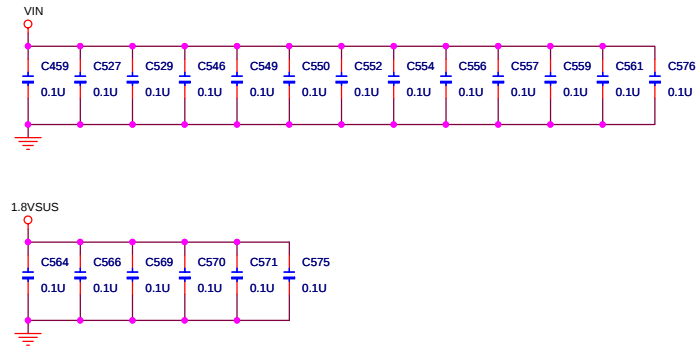


LAN

ANT. CONNECTOR

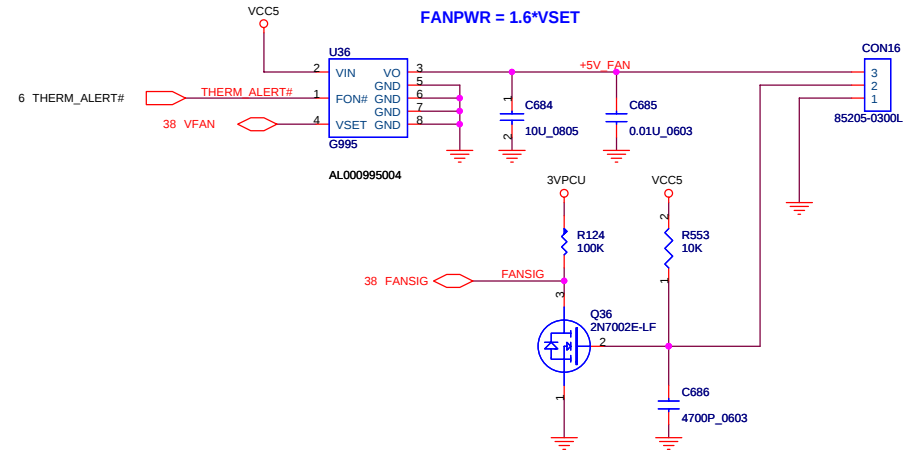


EMI

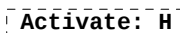
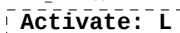


FAN CONN

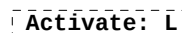
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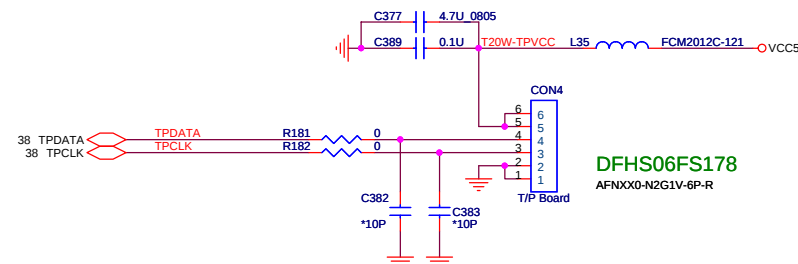


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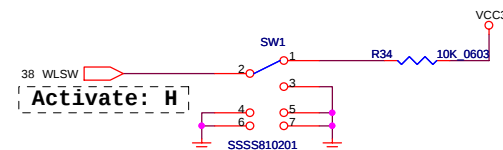


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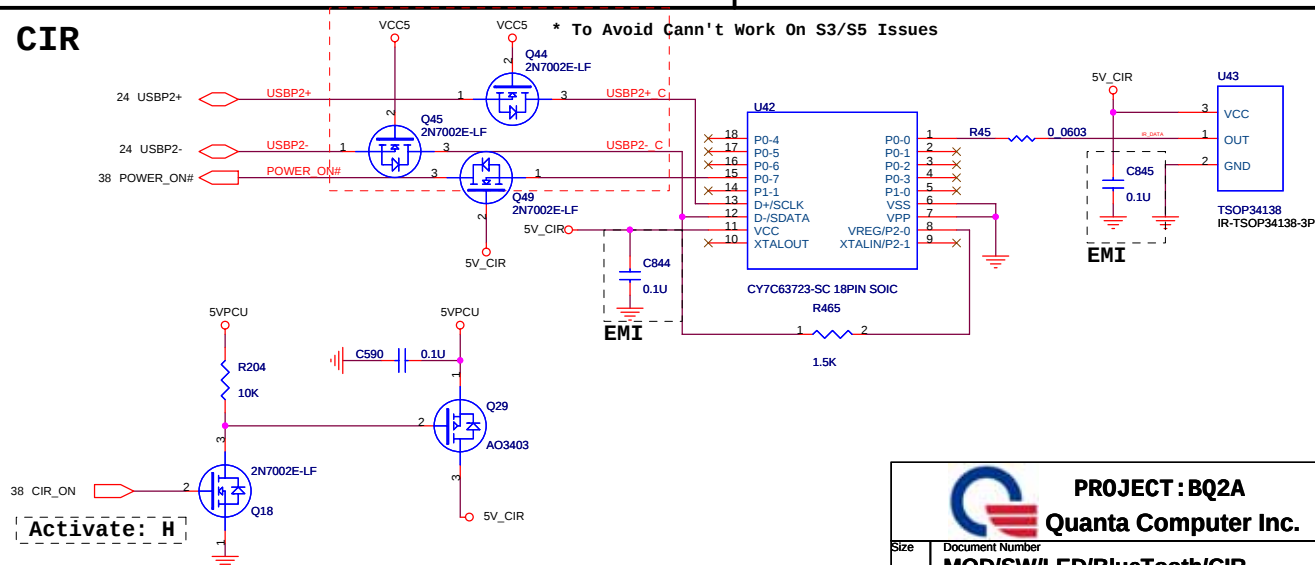




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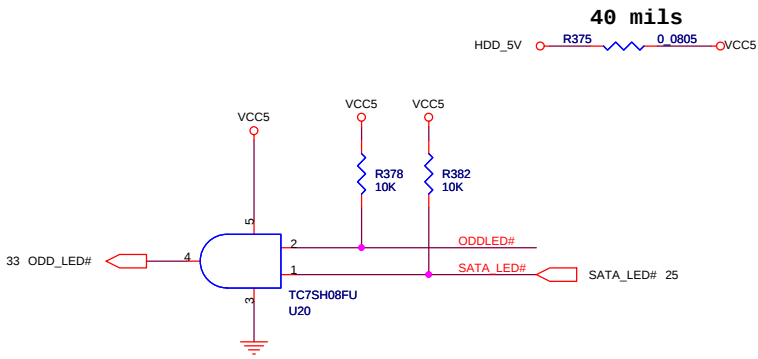
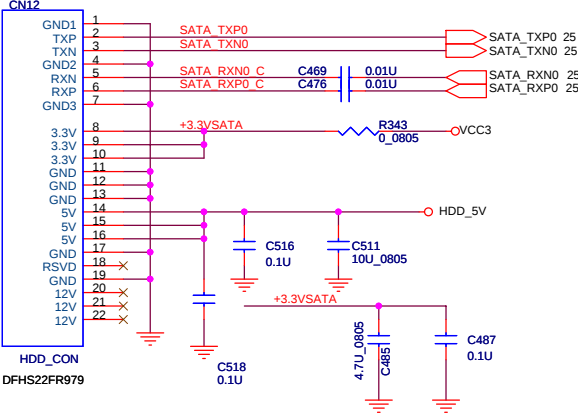
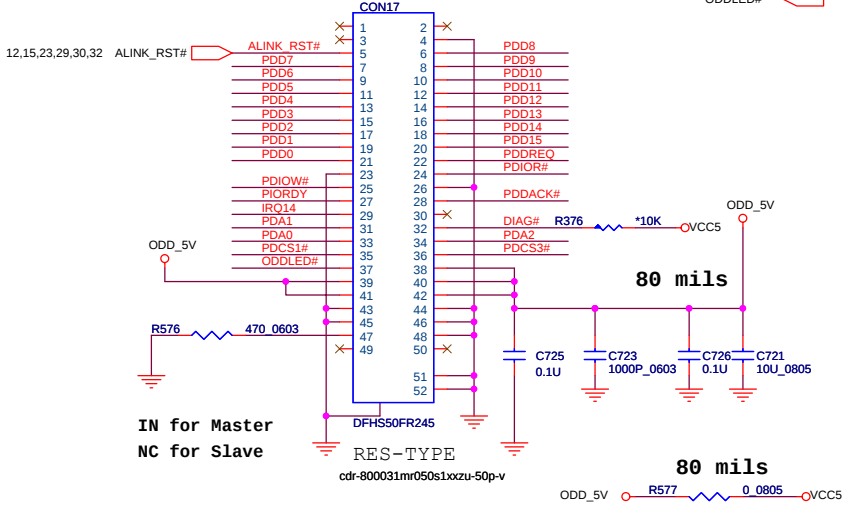


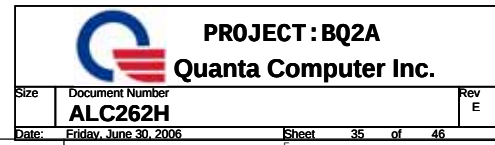
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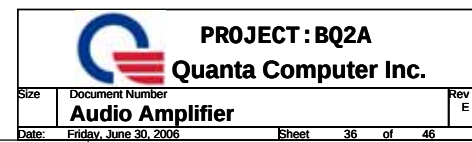


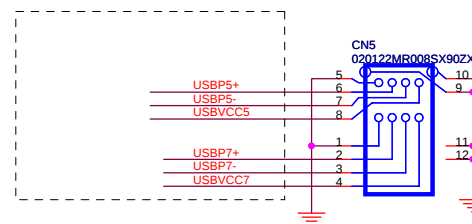
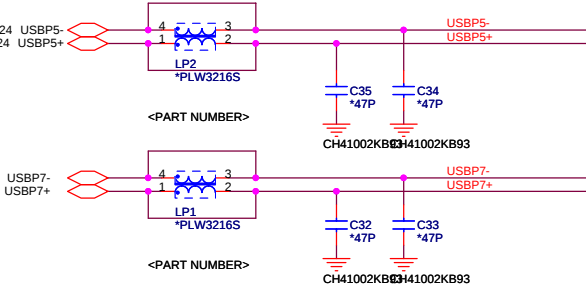
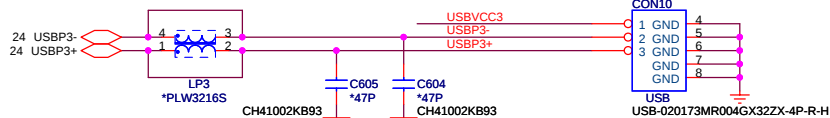
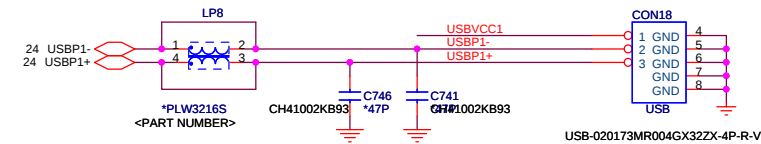
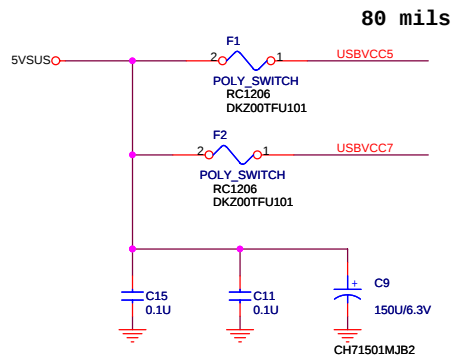
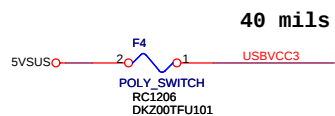
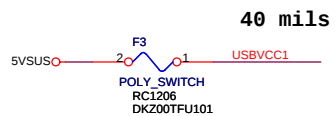
CD-ROM CONNECTOR
SMT TYPE CNN

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25 PDDREQ	PDDREQ
25 PDIOW#	PDIOW#
25 PDIOR#	PDIOR#
25 PIORDY	PIORDY
25 PDDACK#	PDDACK#
25,26 IRQ14	IRQ14
25 PDA1	PDA1
25 PDA0	PDA0
25 PDCS1#	PDCS1#
25 PDA2	PDA2
25 PDCS3#	PDCS3#
25 ODDLED#	ODDLED#

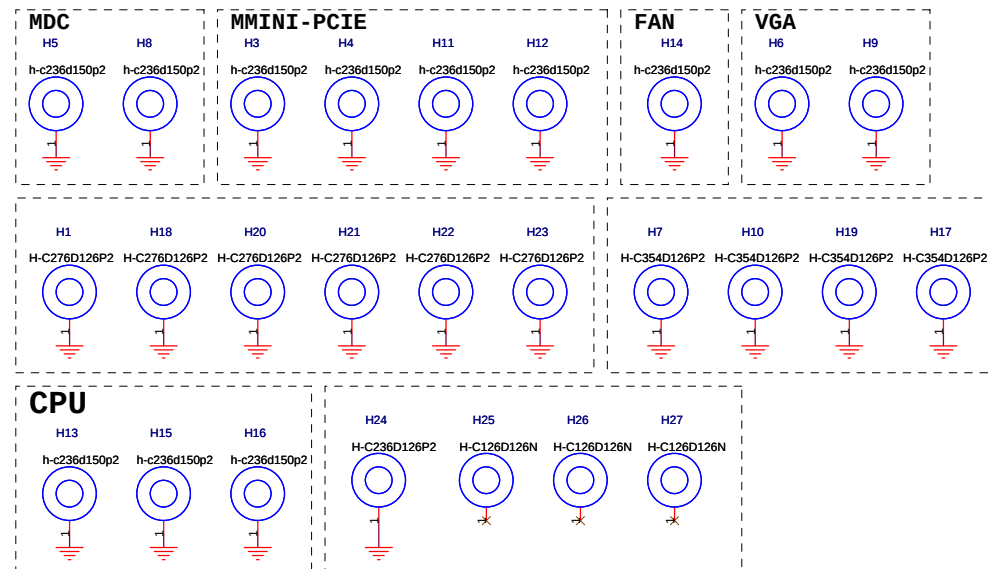
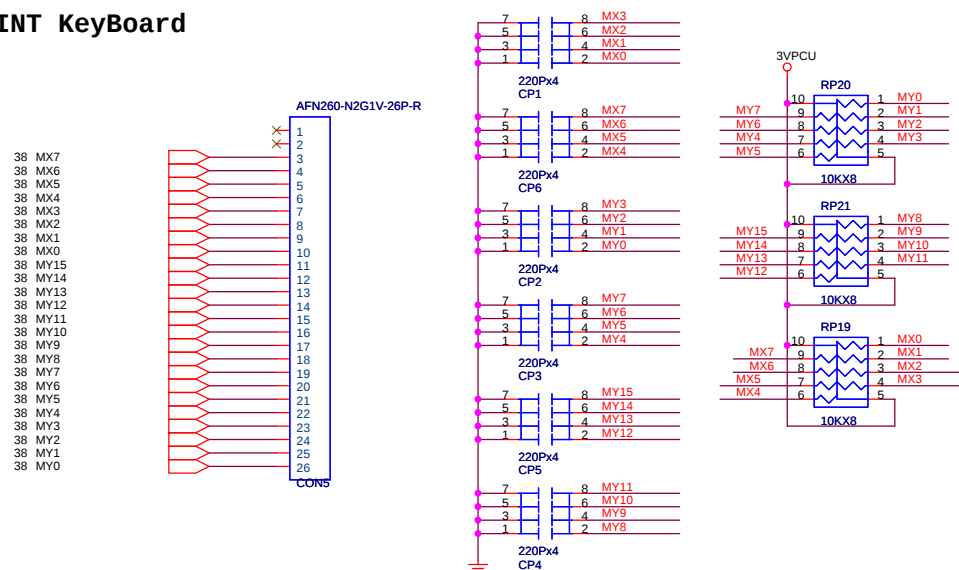




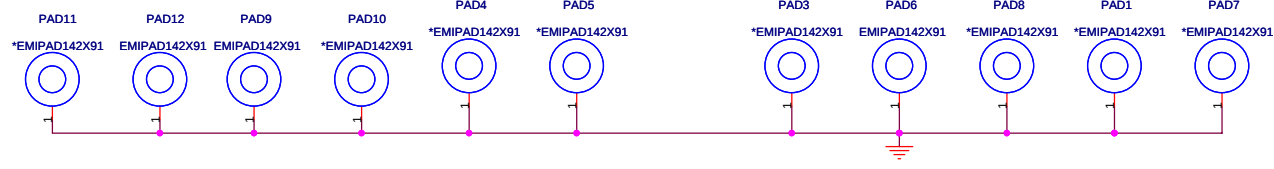


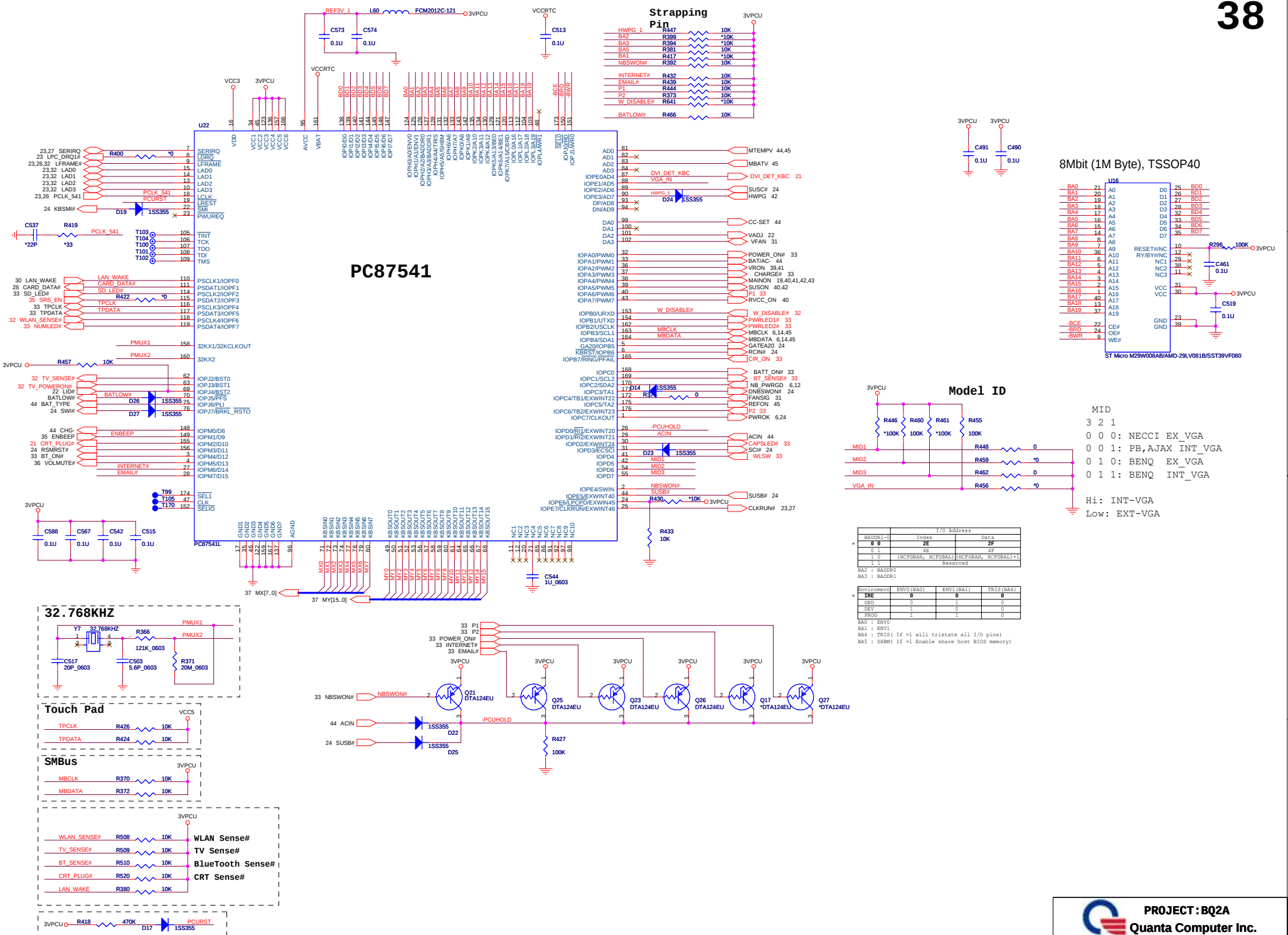


INT Keyboard

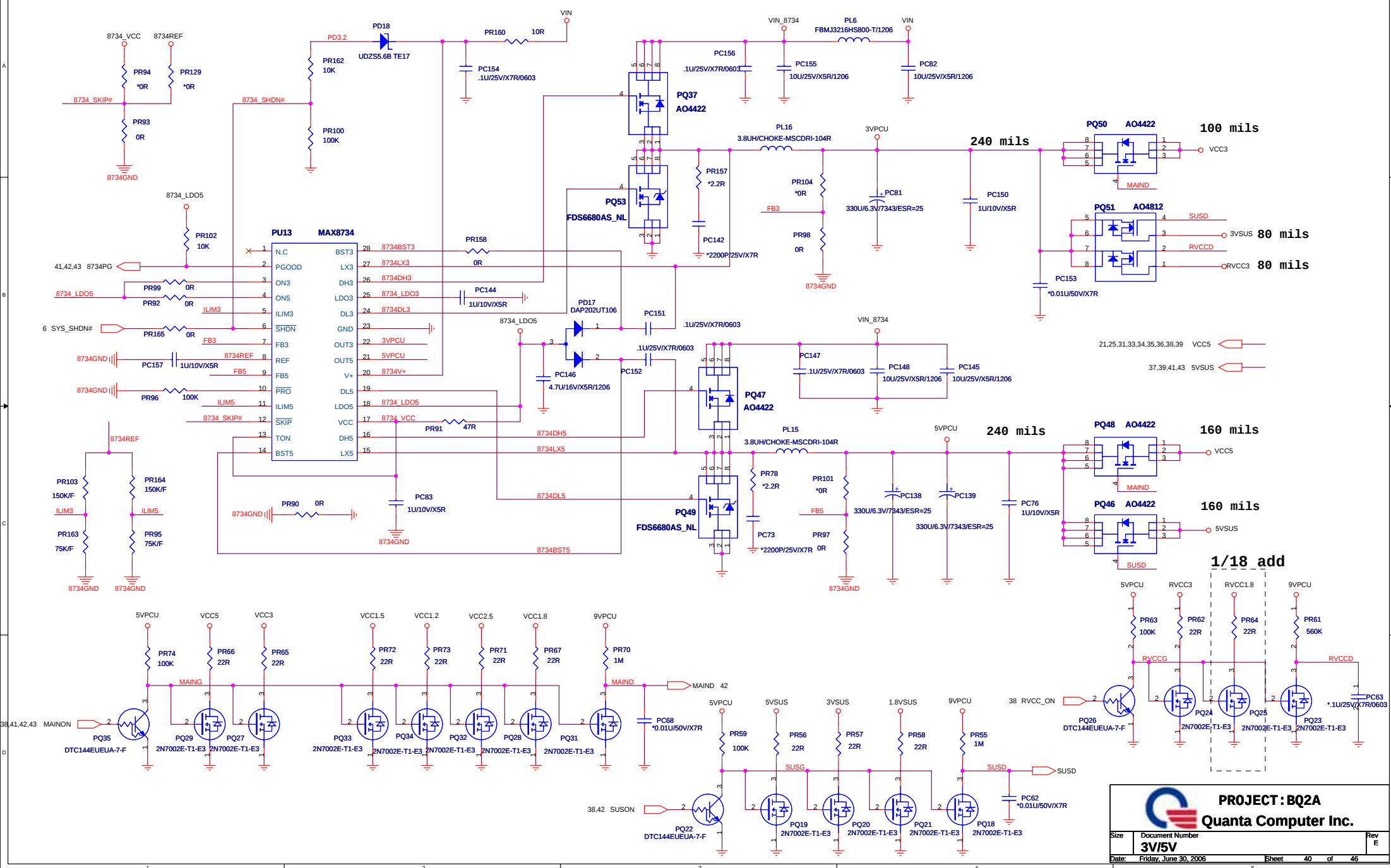


EMI PAD

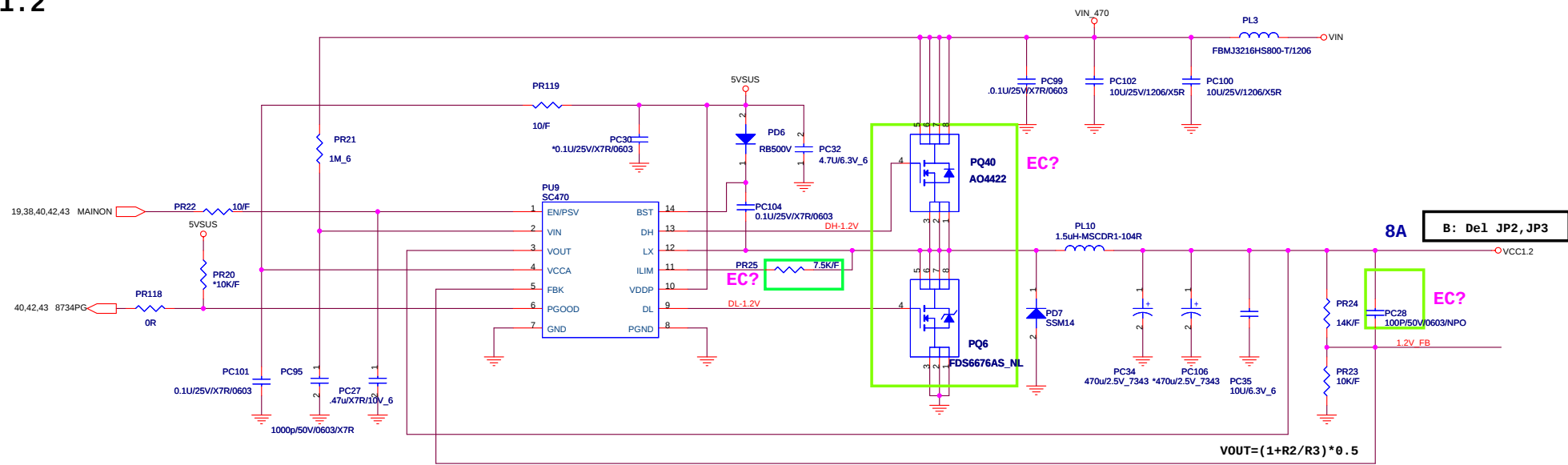




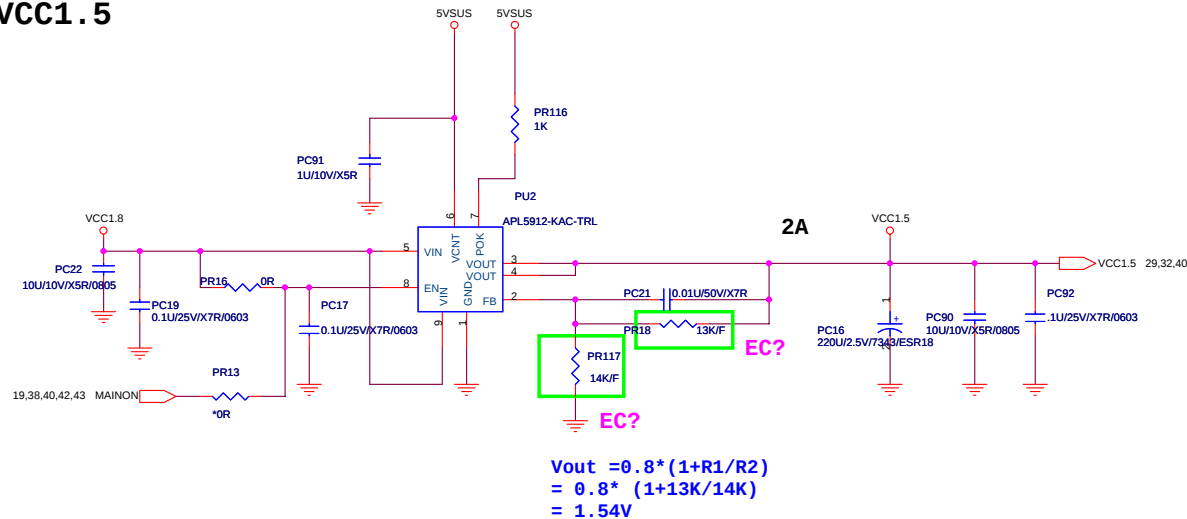
DC/DC 3.3V&5V POWER & Discharge



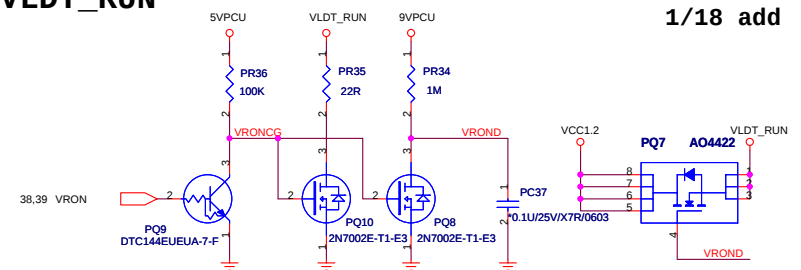
VCC1.2



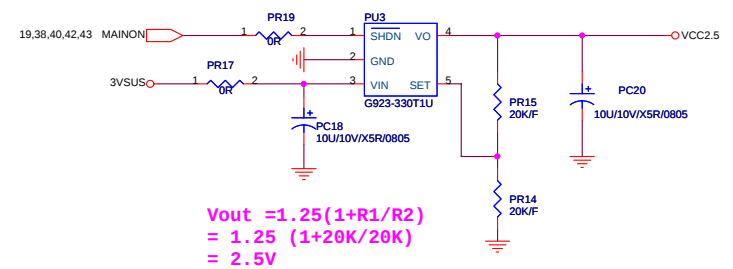
VCC1.5



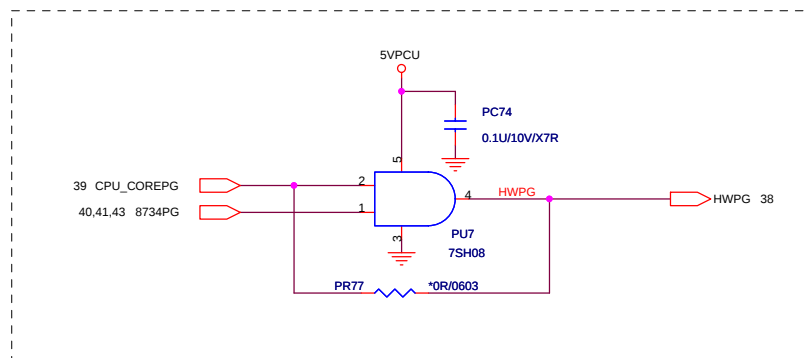
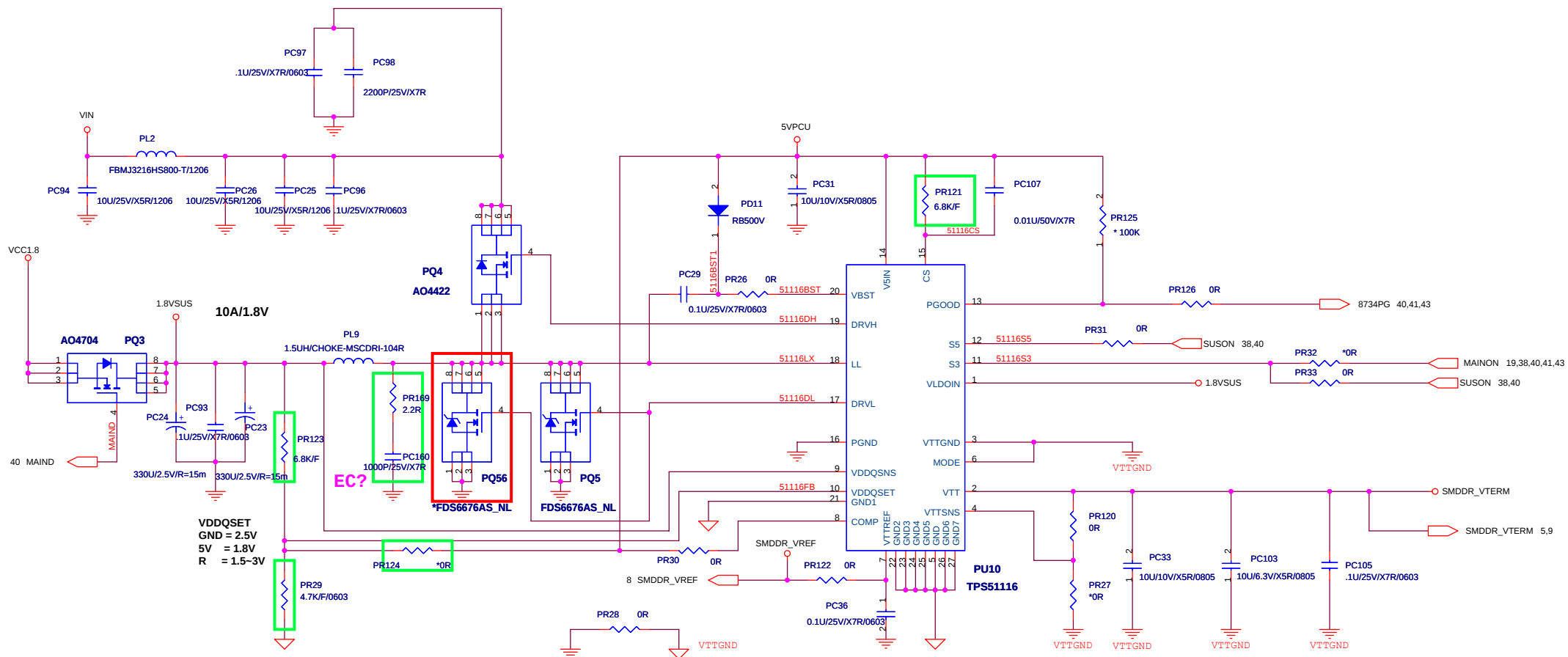
VLDT_RUN



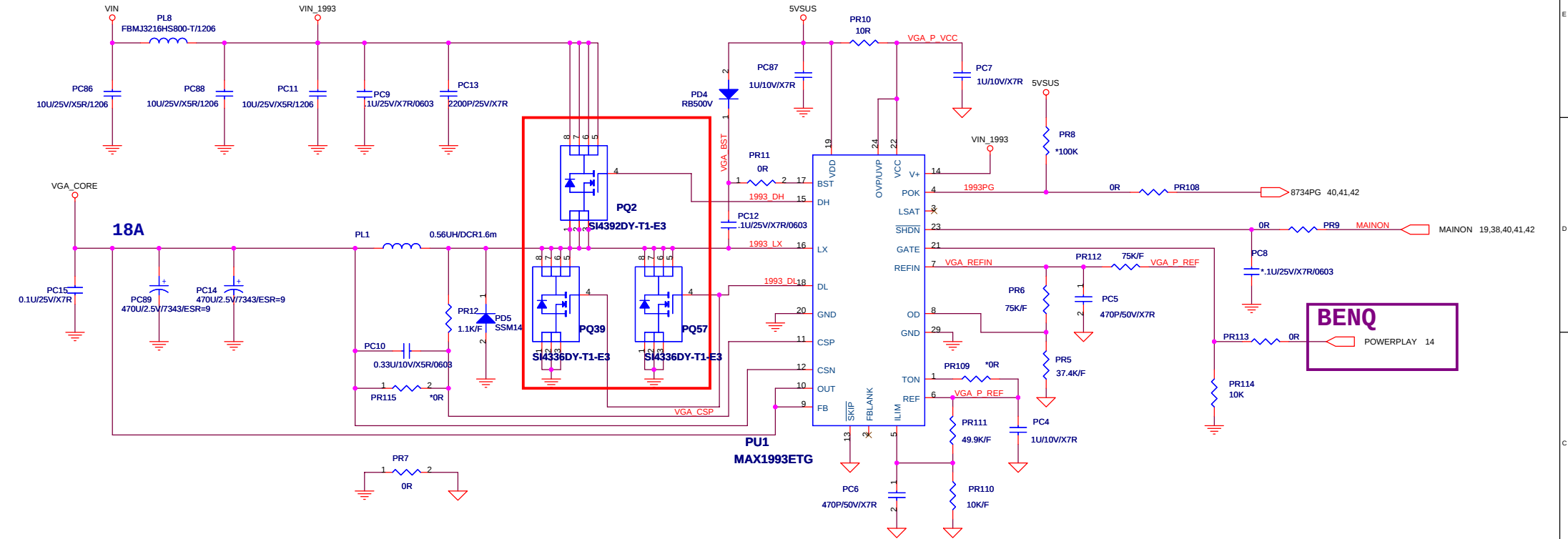
VCC2.5



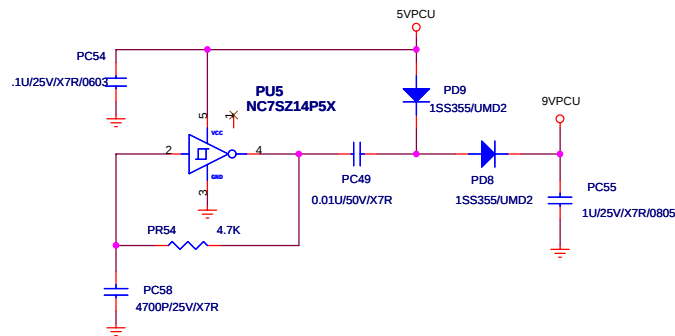
1.8VSUS & VTERM(DDR2) & VCC1.8



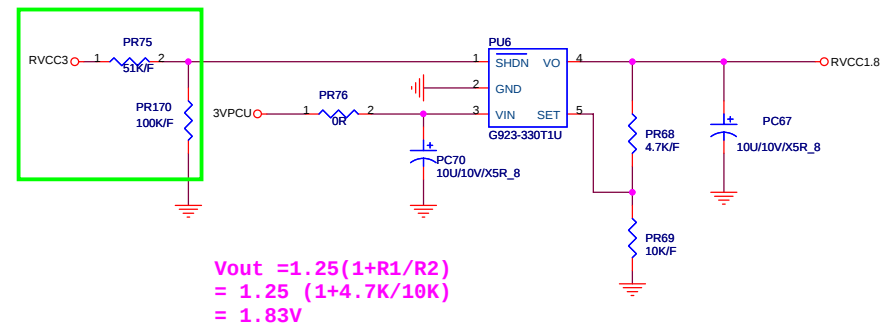
VGA_CORE



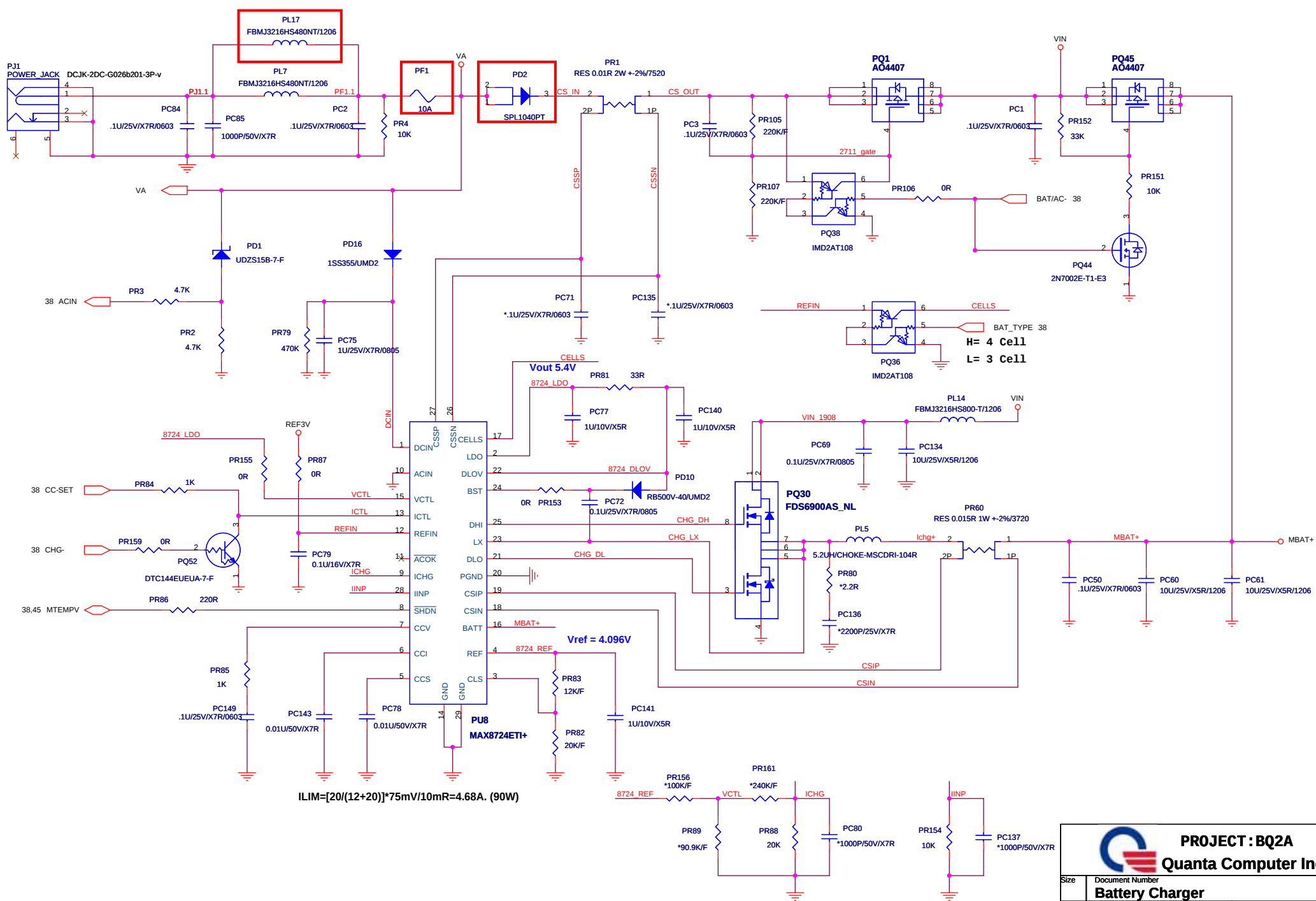
9VPCU



RVCC1.8

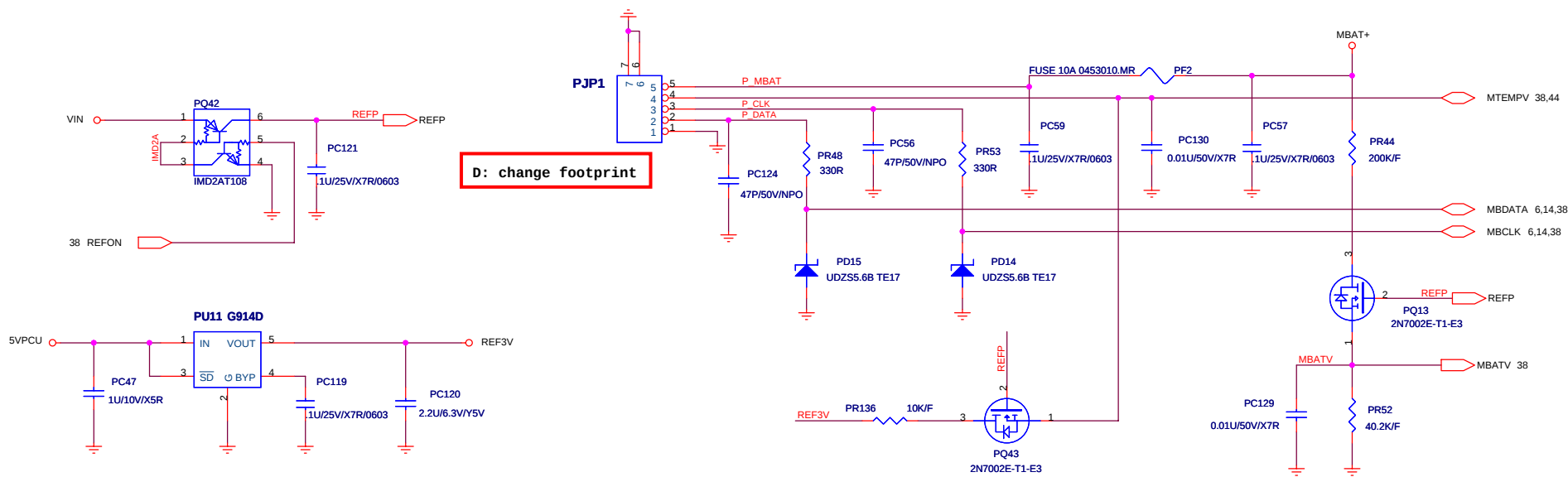


Battery Charger



Battery Connector

Battery Connector



D: change footprint

MTEMPV voltage :		
	System Off	System On
Battery	0V	1.6V
Adapter	3.3V	3.3V
Battery+Adapter	1.6V	1.6V

MBATV voltage :

$16.8V \cdot 40.2 / (200 + 40.2) = 2.812V$

$12.0V \cdot 40.2 / (200 + 40.2) = 2.008V$

$8.0V \cdot 40.2 / (200 + 40.2) = 1.34V$

	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1



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Size	Document Number	Rev
	Changing Lists	E