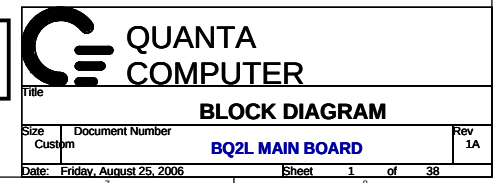


01

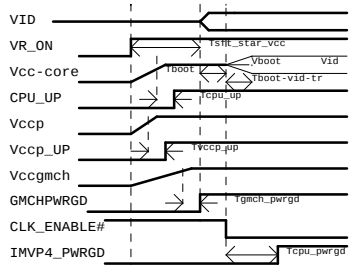


Board Stack up Description

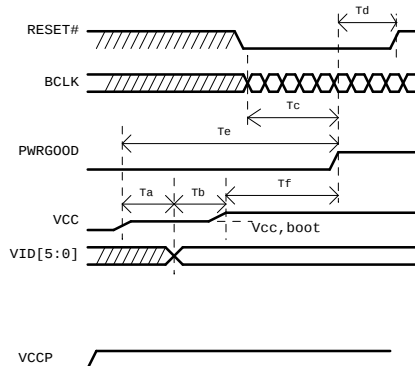
PCB Layers

Layer 1		TOP(Component,Other)
Layer 2		Ground Plane
Layer 3		IN1
Layer 4		IN2
Layer 5		Power Plane
Layer 6		IN3
Layer 7		Ground Plane
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



Dothan Power-up Timing Specifications

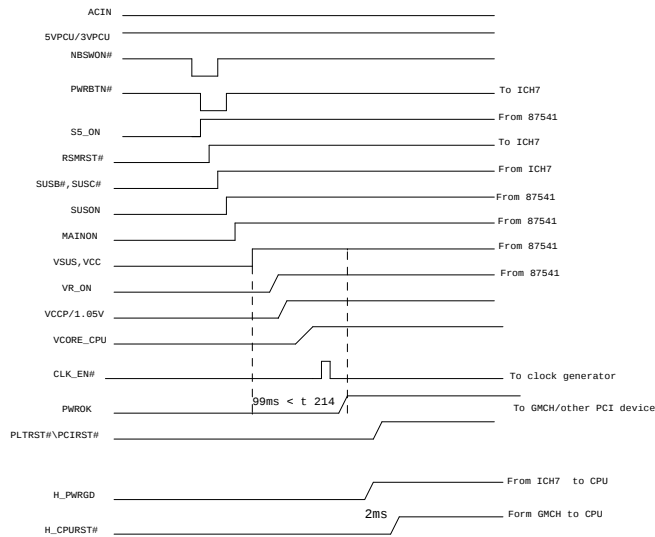


Ta=VCC and VCCP assertion to VID[5:0] valid
Tb=VID[5:0] stable to VCC valid
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=VCC, boot valid to PWRGOOD assertion time

Voltage Rails

Voltage Rails	ON S0-S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE Core voltage for Processor	X				VR_ON 0.726V-0.94V
VCCP Core voltage for CPU / NB	X				VR_ON
SMDDR_VTERM0.9V for DDR2 Termination voltage	X				MAINON
RVCC1.5	X	X	X		RVCC_ON
RVCC3	X	X	X		RVCCD
VCC1.5	X				MAIND
VCC2.5	X				MAINON
VCC3	X				MAIND
VCC5	X				MAIND
1.8VSUS	X	X			SUSON
3VSUS	X	X			SUSD
5VSUS	X	X			SUSD
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL
9VPCU	X	X	X	X	5VPCU

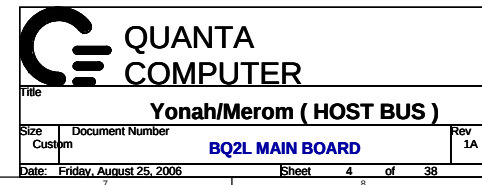
ACIN POWER ON TIMING

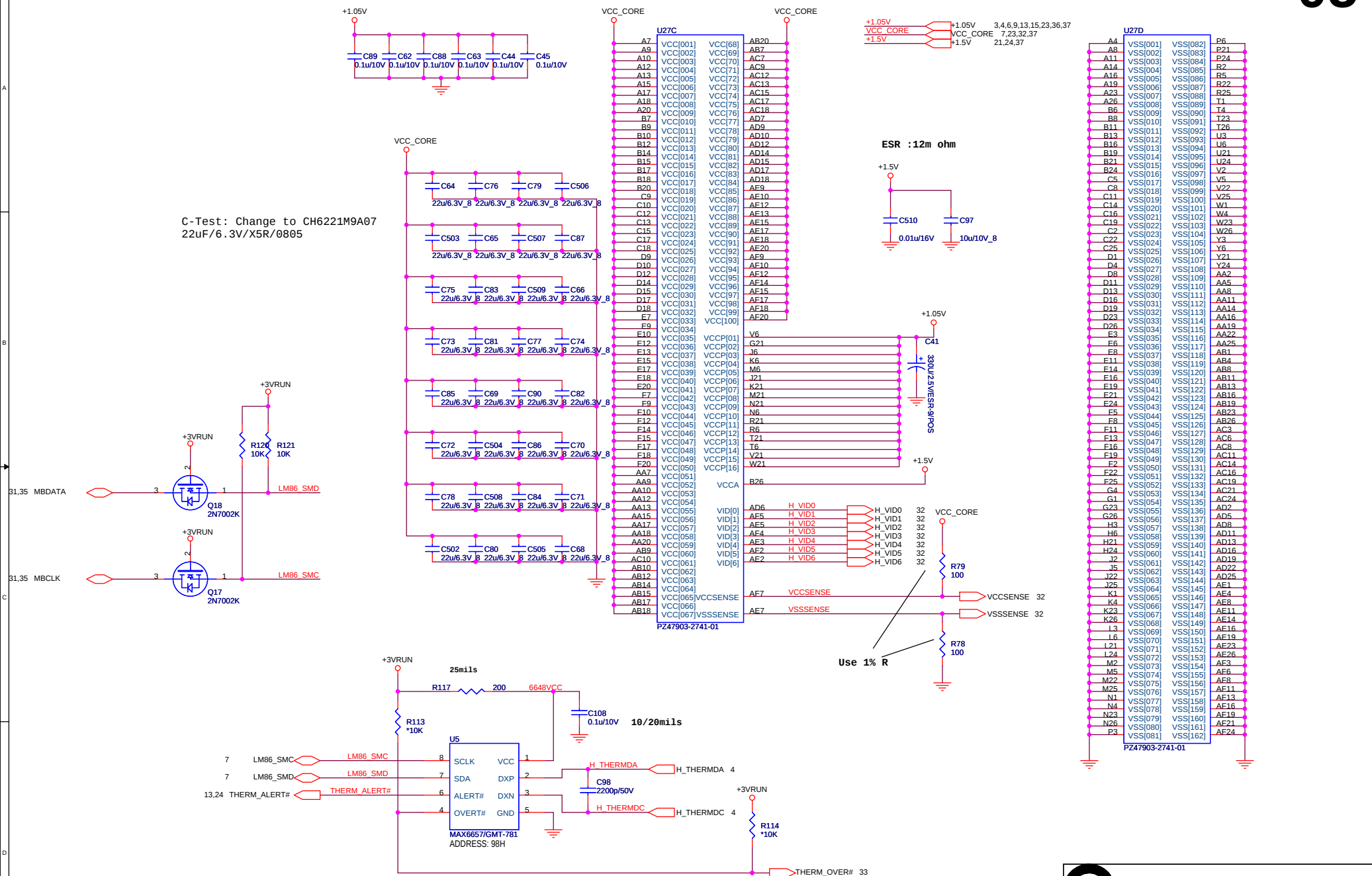


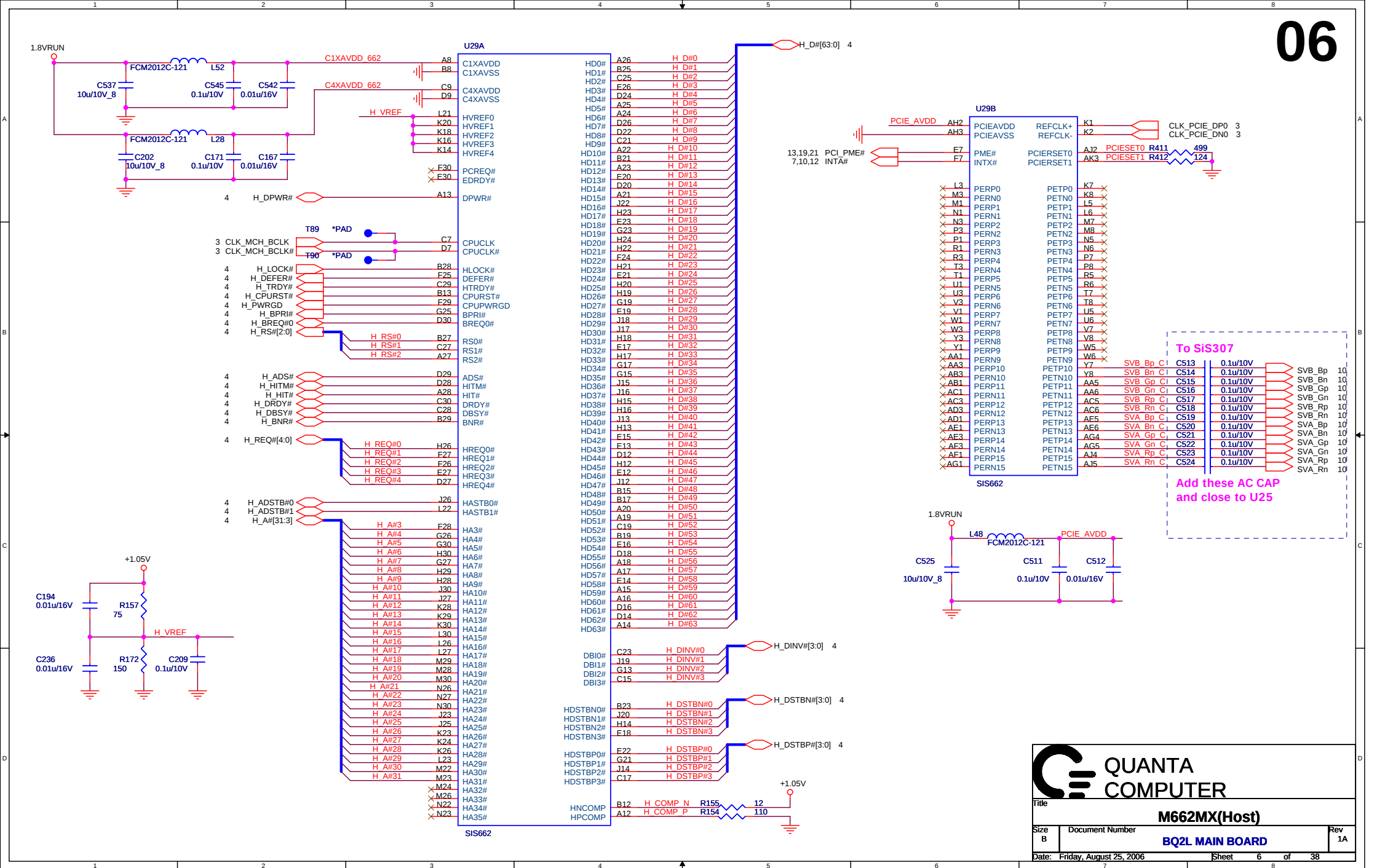
Voltage Rails	ON S0-S1	ON S3	ON S4	ON S5	Control signal
VCC_CORE Core voltage for Processor	X				VRON
GMCH_VTT Core voltage for GMCH 1.05V	X				MAINON
SMDDR_VTERM 0.9V for DDR II Termination voltage	X				MAINON
SMDDR_VREF 0.9V for DDR II Reference Voltage	X				MAINON
GMCH 1.5V	X				MAINON
1.8VSUS 1.8V for DDR II voltage	X	X			SUSON
2.5V	X				MAINON
3VPCU	X	X	X	X	VL
5VSUS	X	X			SUSON
3V	X				MAINON
5VPCU	X	X	X	X	VL
5VSUS	X	X			SUSON
3V	X				MAINON

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI#402	AD20	REQ2# / GNT2#	PIRQ C/D

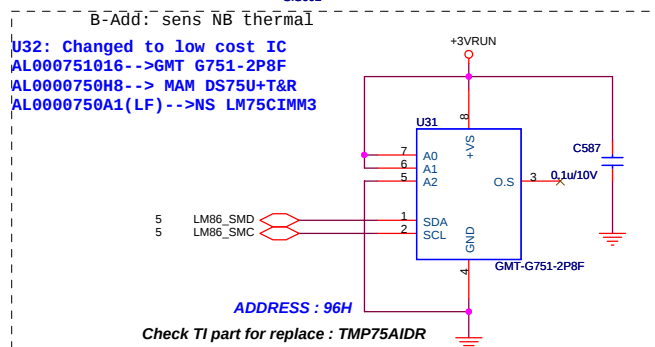
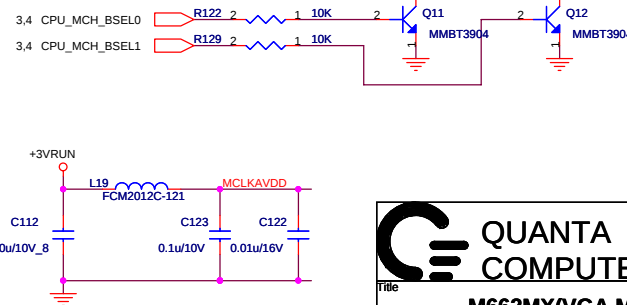
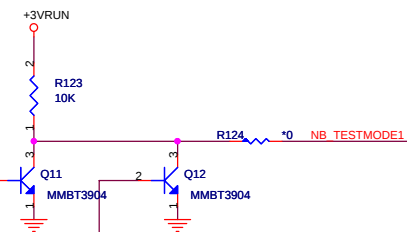
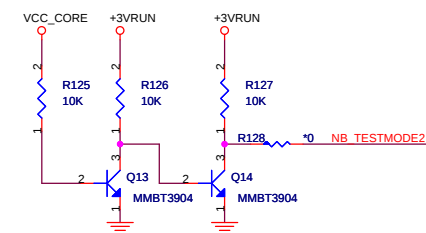
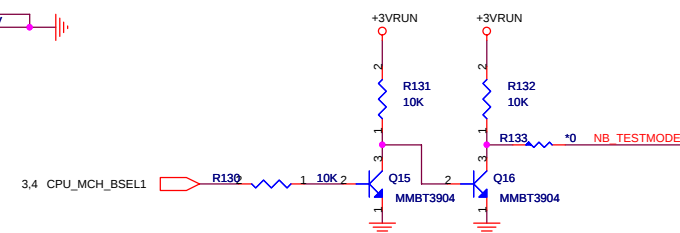
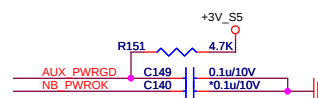
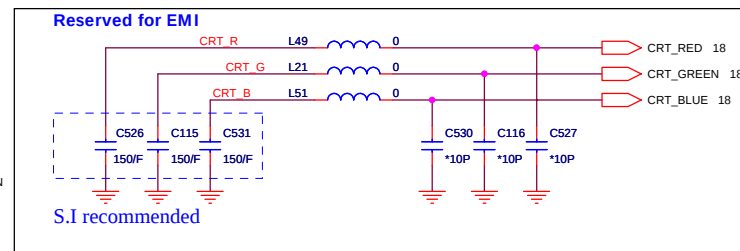
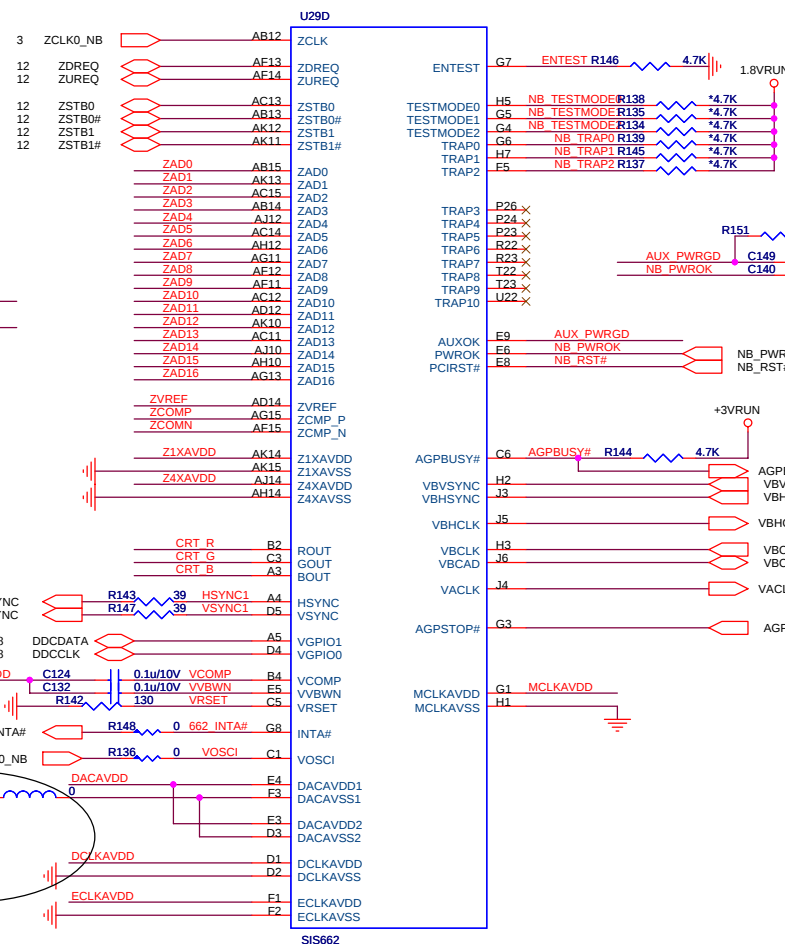


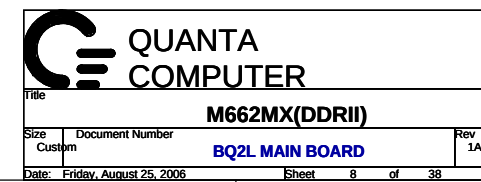


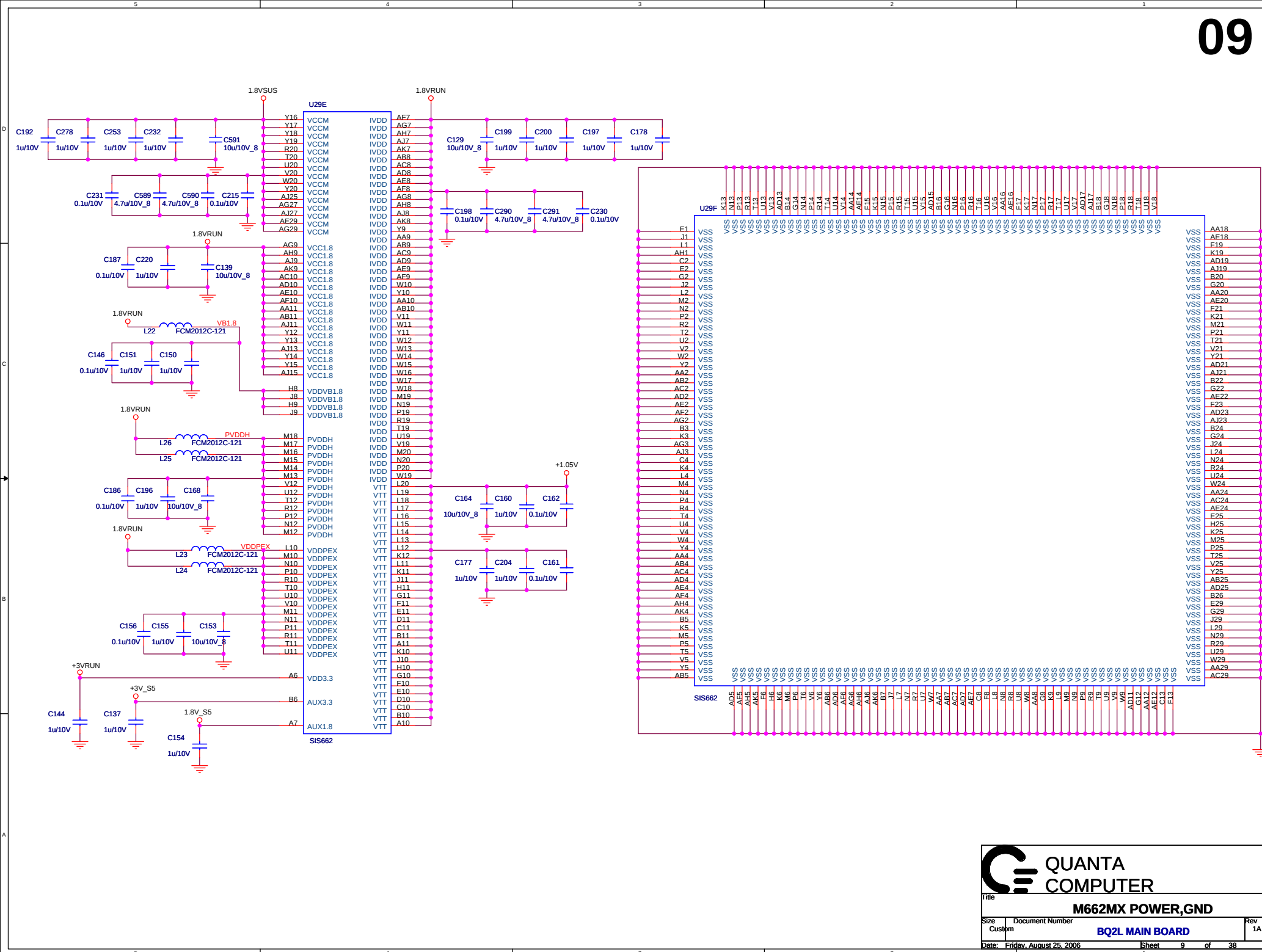


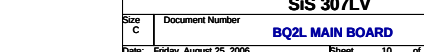
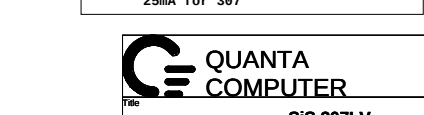
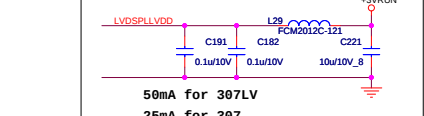
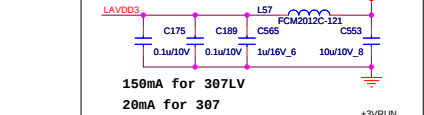
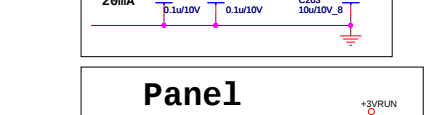
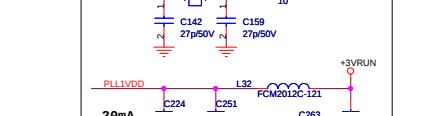
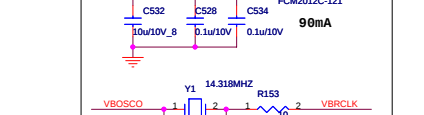
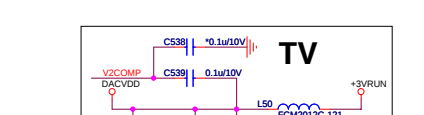
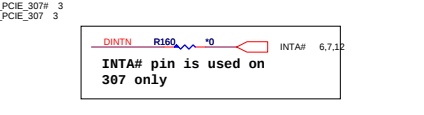
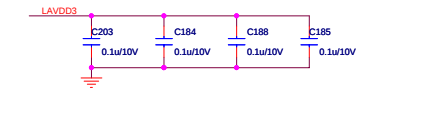
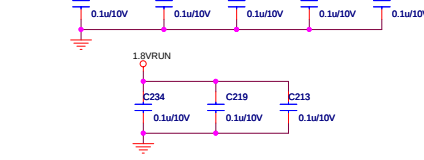


12 ZAD[16:0]





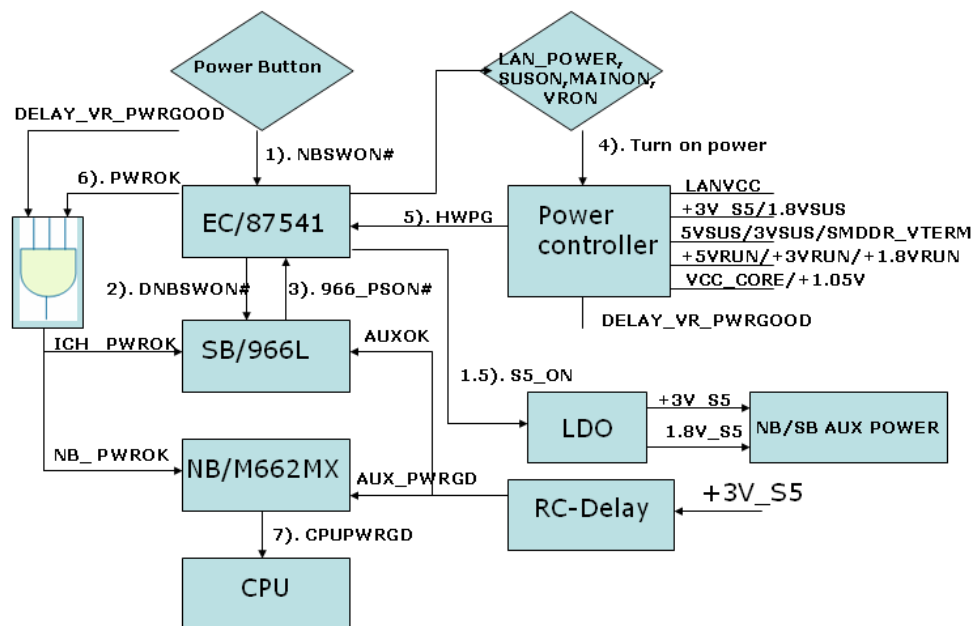


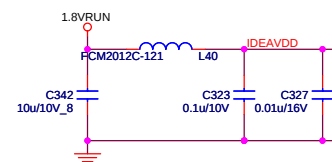
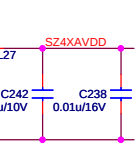
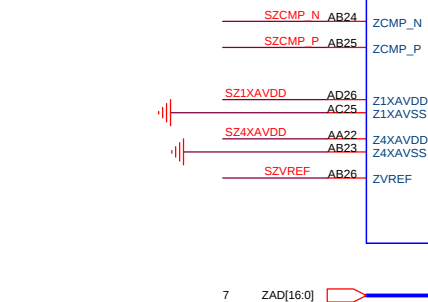
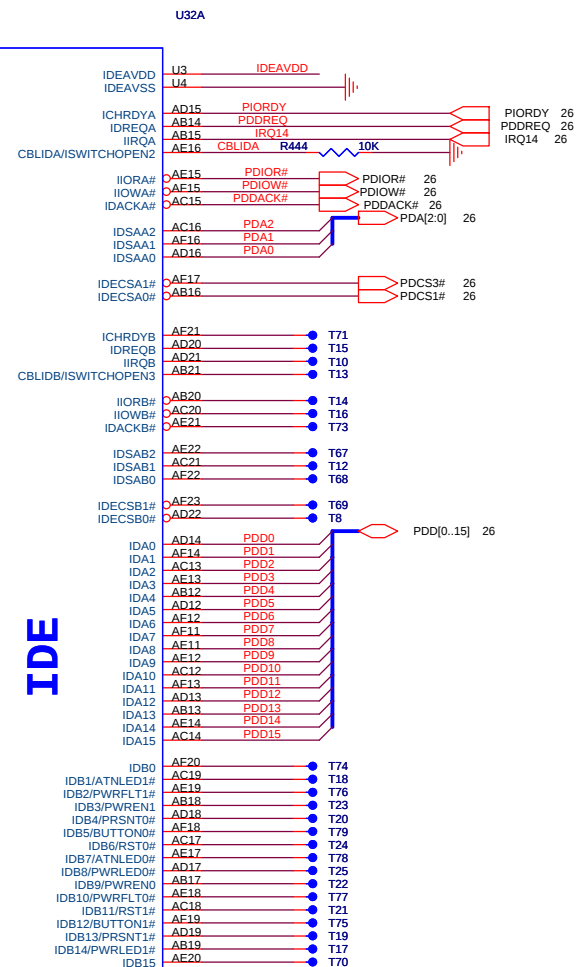


Panel

SIS307ELV: AJ003070T05(W/O TV); C-Test
SIS307LV: AJ003070T13 (With TV); A, B-Test

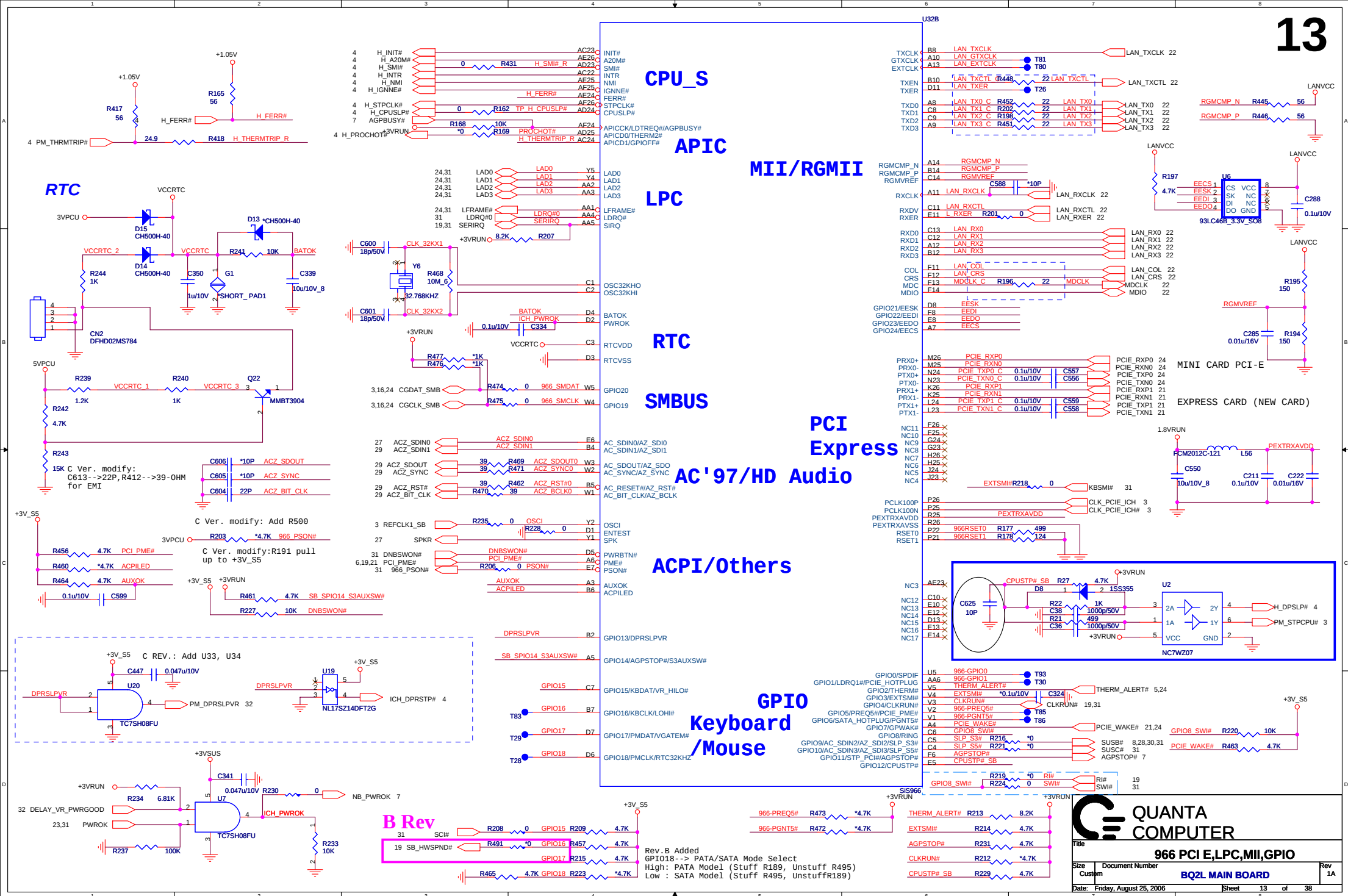
Power On sequence

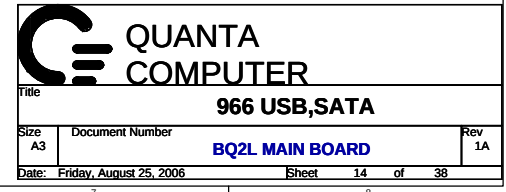


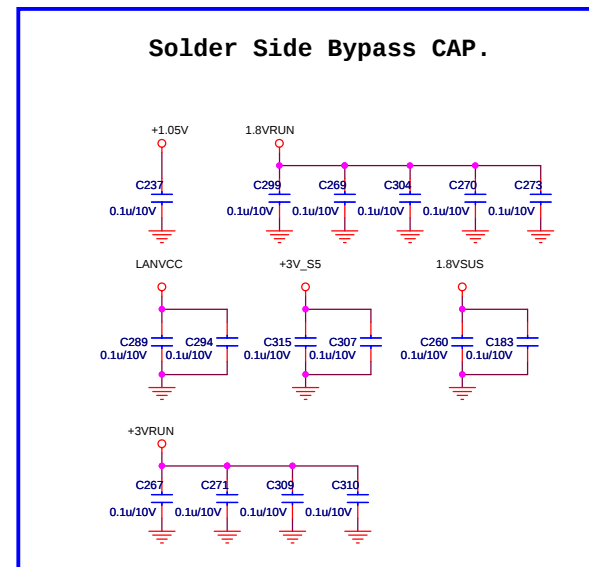


Rev.B Added for SiS SB request

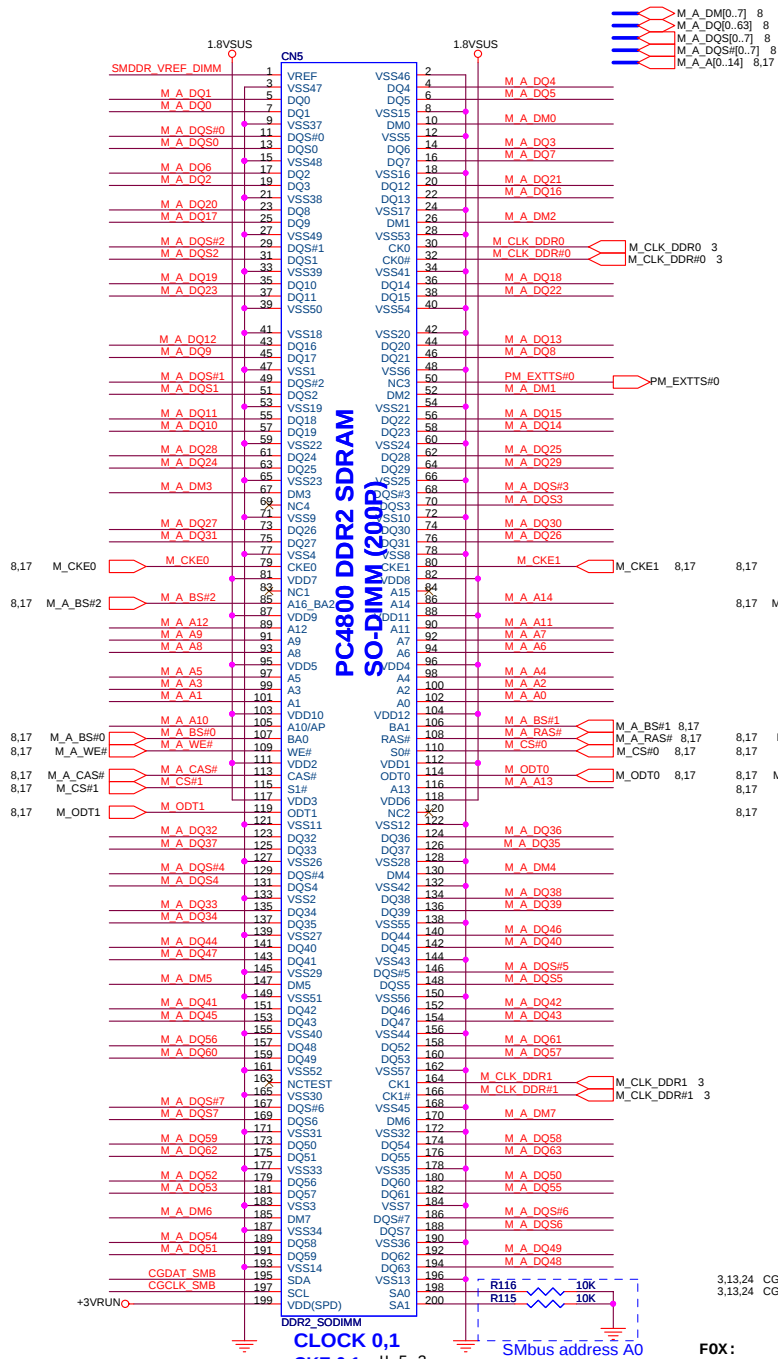




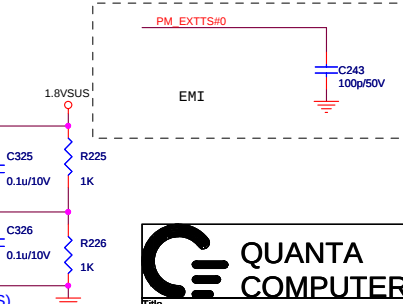
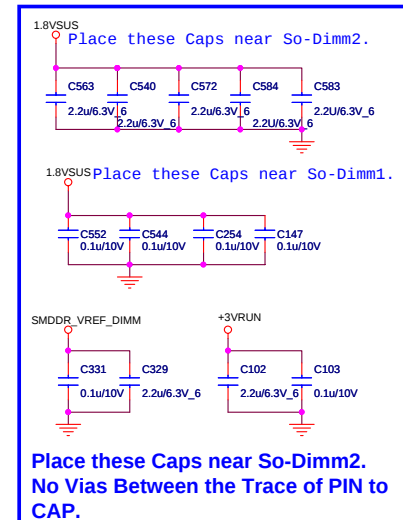
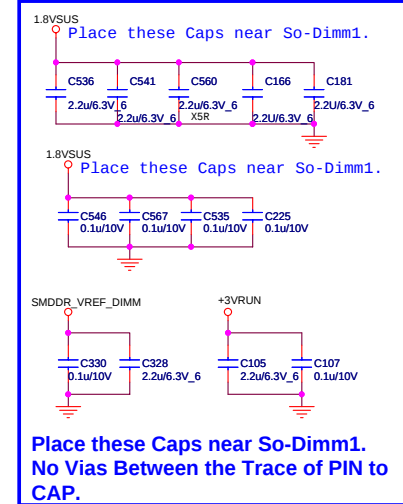
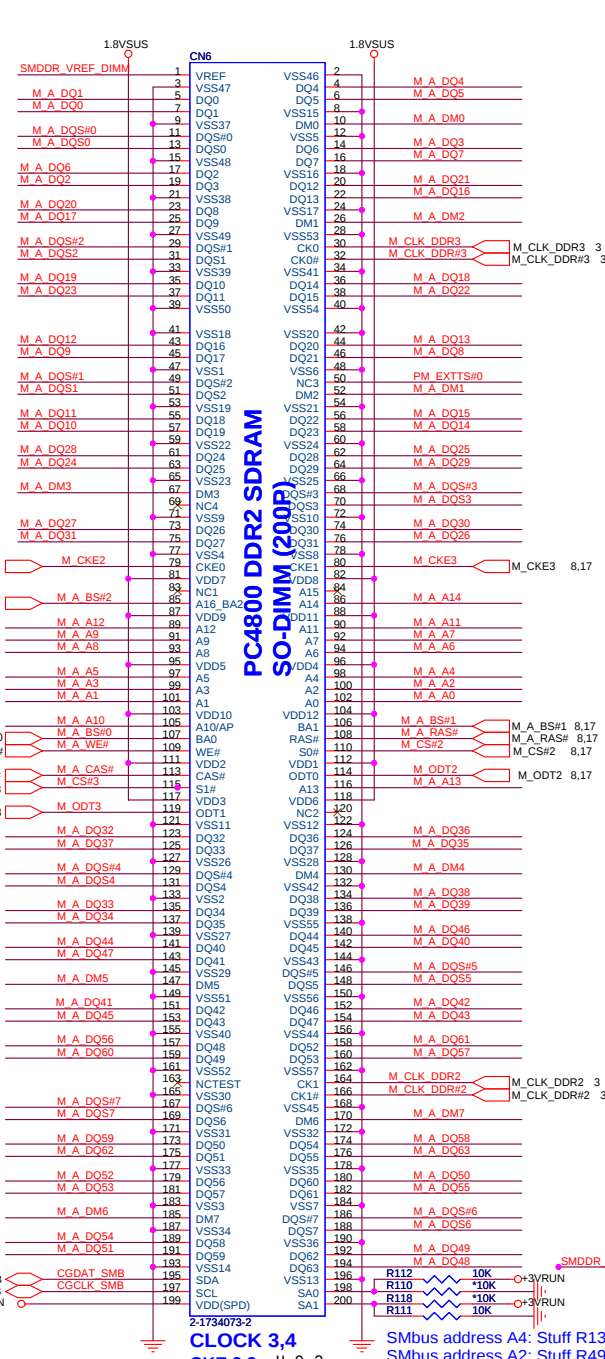




Solder Side Bypass CAP.



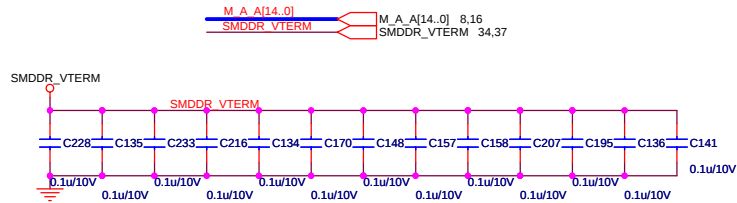
FOX:
H=5.2mm--> DGMK0000498
H=9.2mm--> DGMK0004205



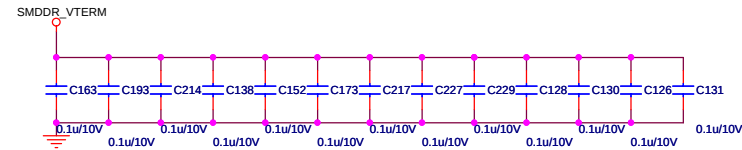
DDRII SINGLE CHANNEL.

17

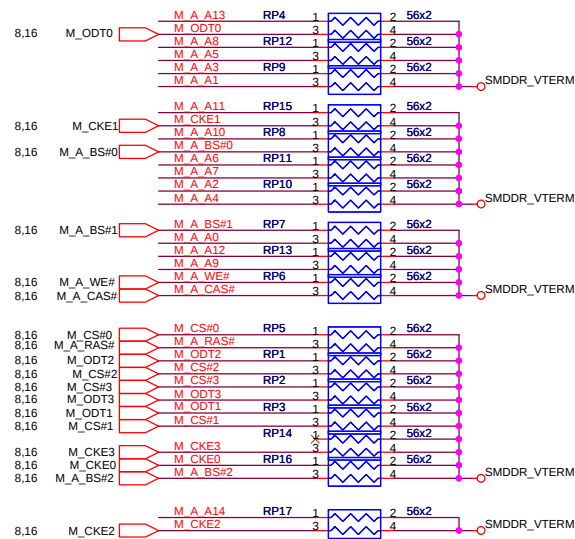
DDRII DIMM 1



DDRII DIMM 2

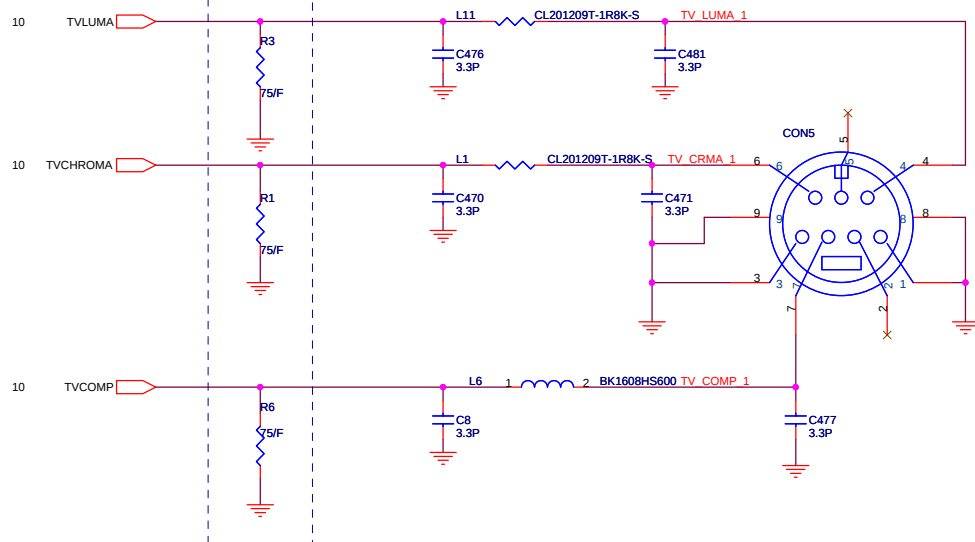


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



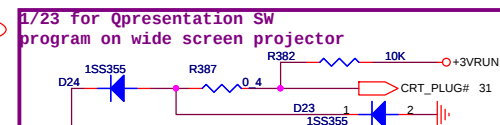
S-VIDEO

SiS recommended design 05/22
Close SiS 307LV

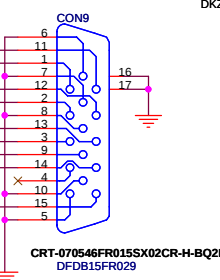


030001FR007T200FT
SV-030107FR007S112XR-RVS-7P

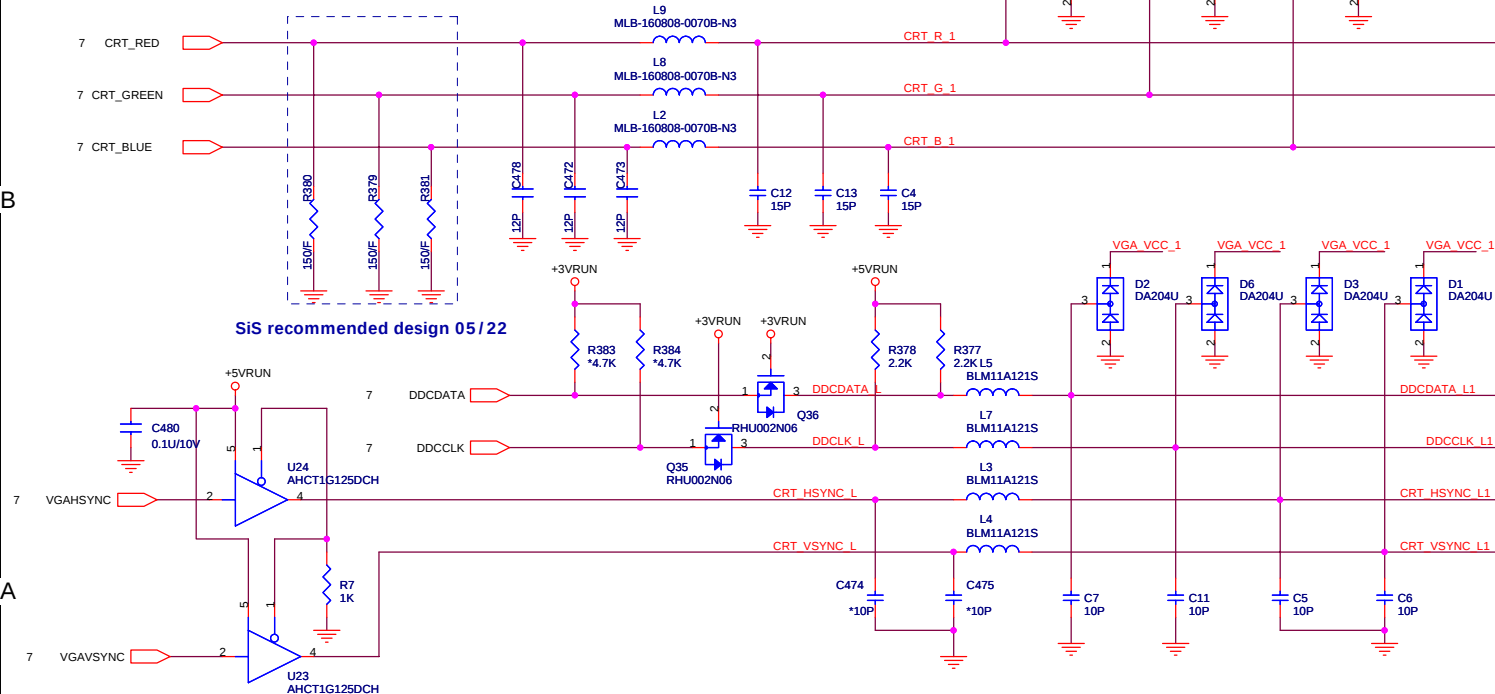
8/22



CRT PORT

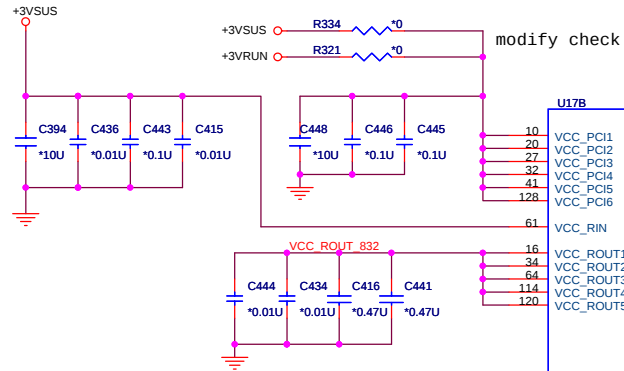


SiS recommended design 05/22



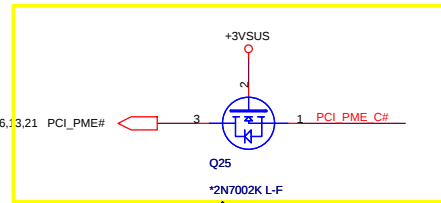
Reserved function

19

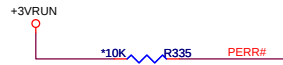


PowerOnReset for VccCore

When GRESET# is controlled by system, the pull-up resistor(R3) and capacitor(C13) do not need to apply.

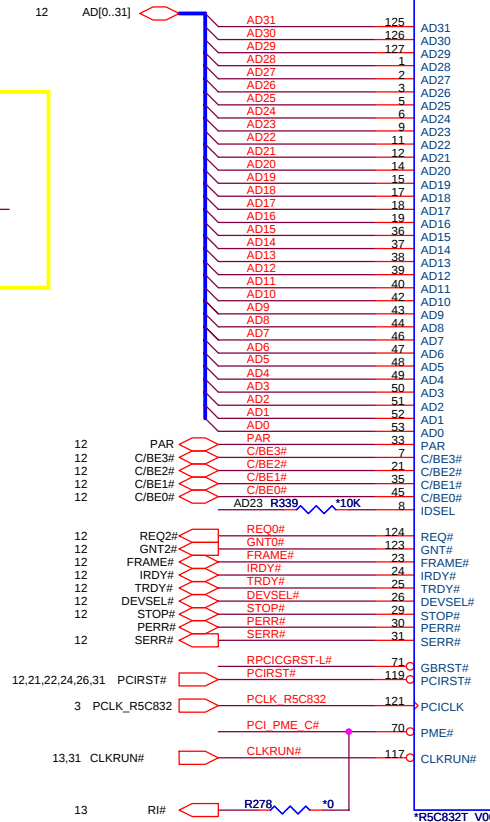


PV-1 modified to fix S5 WAKE-UP-LAN ISSUE (CH7M has leakage power to card reader)

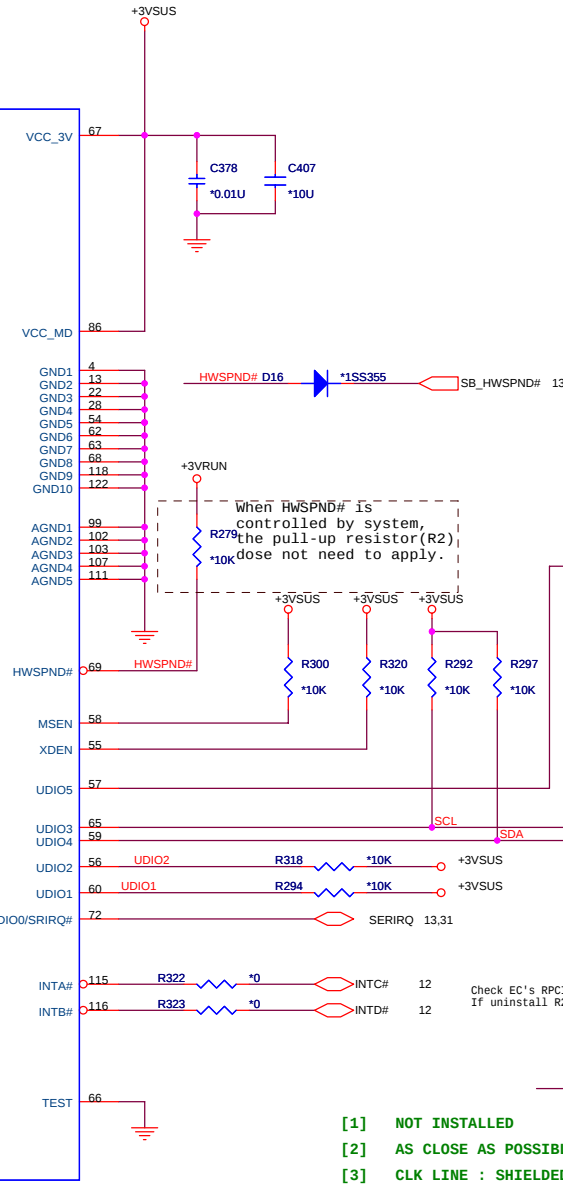


CoreLogic CLOCKRUN#

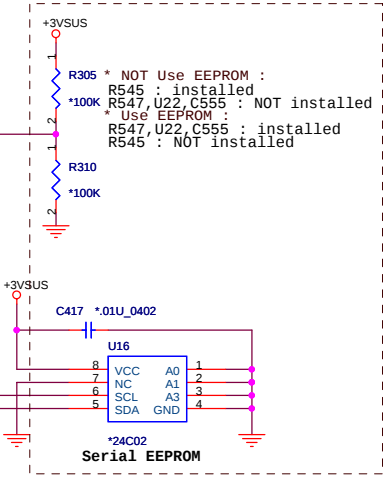
When CLKRUN# is controlled by system, the pull-down resistor(R14) dose not need to apply.



PCI / OTHER



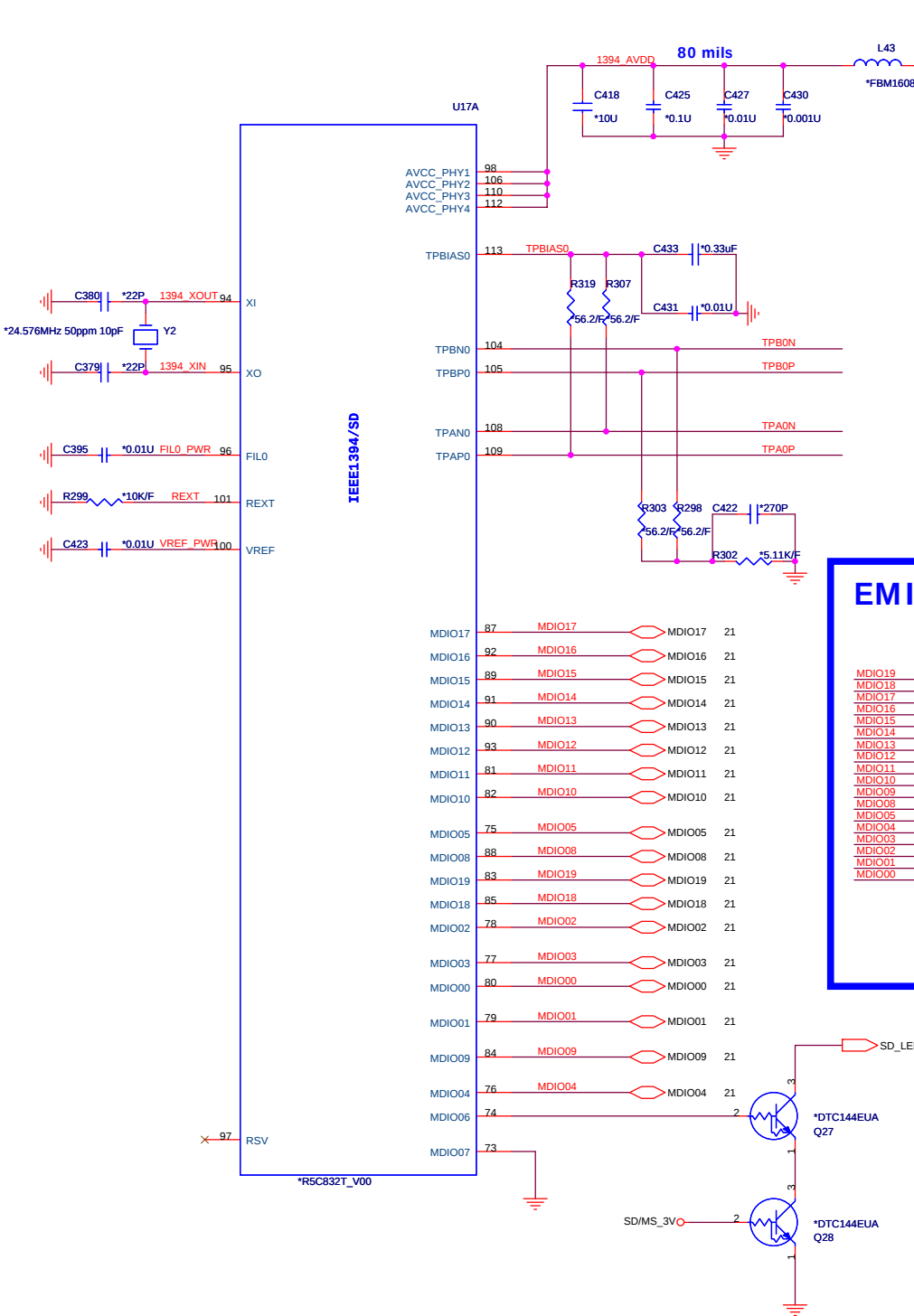
- [1] NOT INSTALLED
- [2] AS CLOSE AS POSSIBLE TO DEVICE TERMINALS
- [3] CLK LINE : SHIELDED BY GND. (RECOMMENDED)



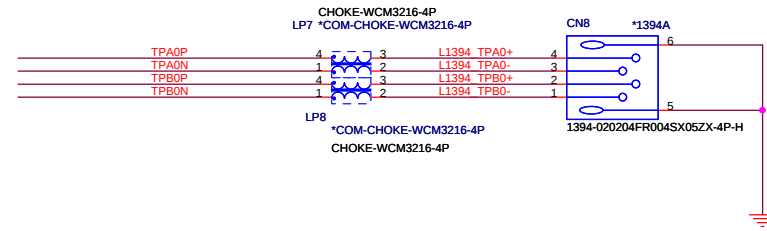
SI-2 modified

fix card reader LED alway on when system into the S3

Title	
R5C832(PCI)	
Size	Document Number
Custom	BQ2L MAIN BOARD
Date:	Rev 1A
Friday, August 25, 2006	Sheet 19 of 38

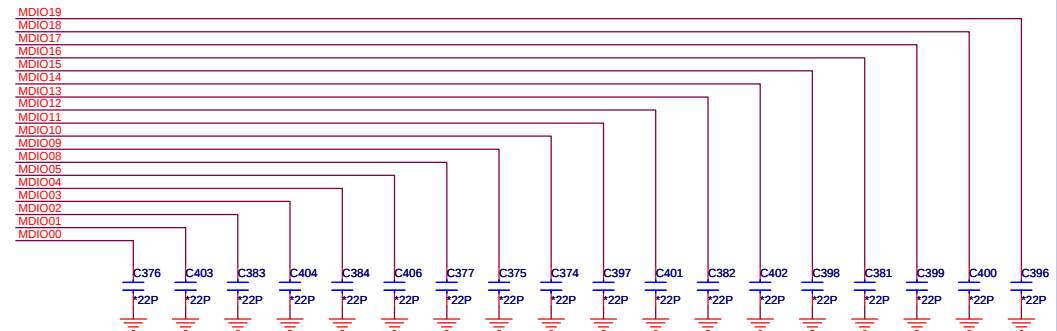


AS CLOSE AS POSSIBLE TO
1394 CONNECTOR.

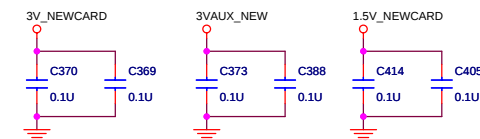
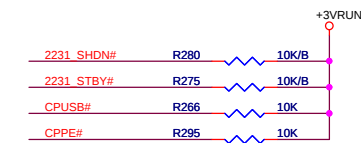


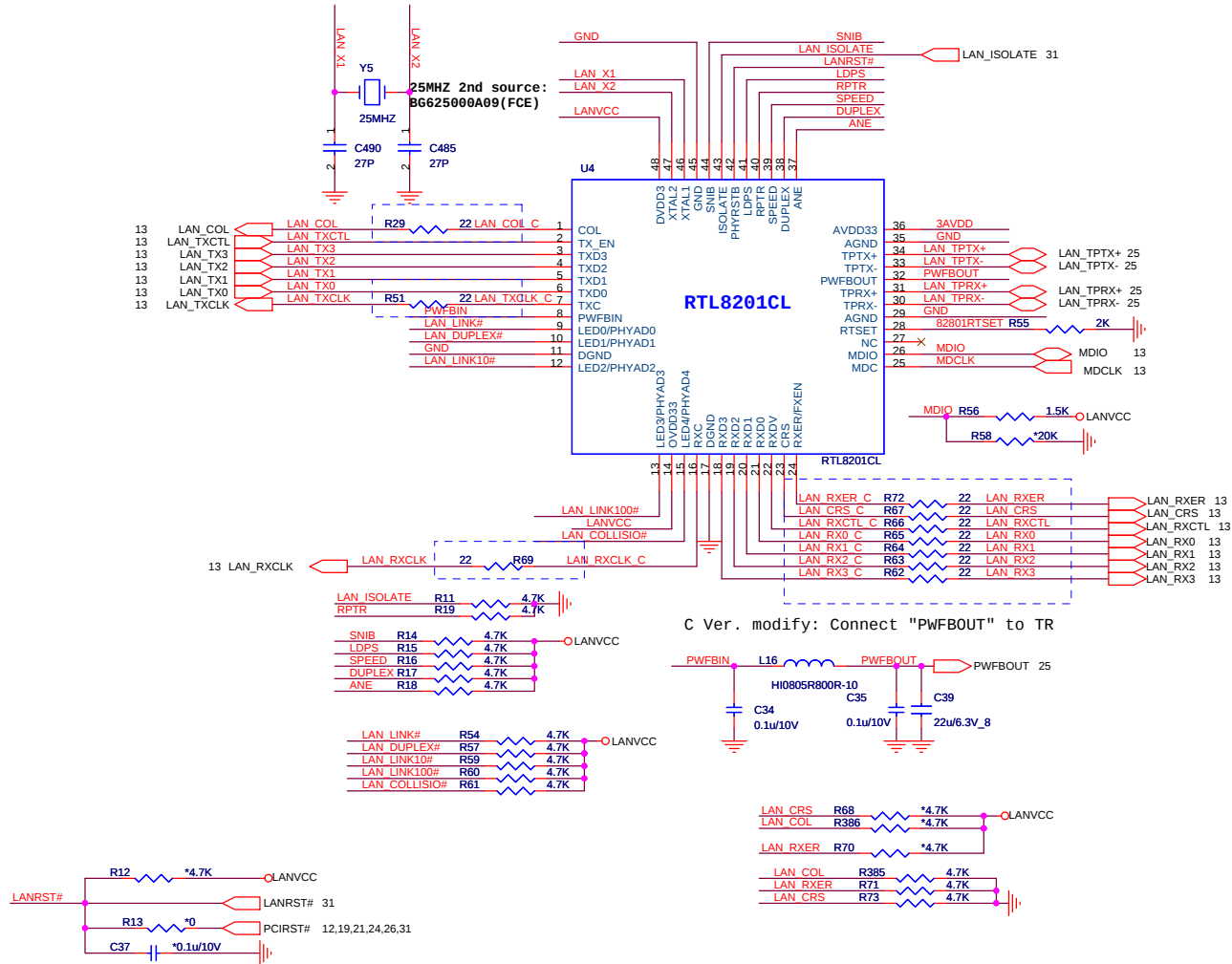
*TPA/TPA#,TPB/TPB# pair trace : As close as possible.
*TPA/TPA#,TPB/TPB# pair trace : Same length electrically.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

EMI

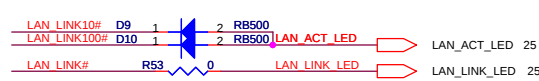
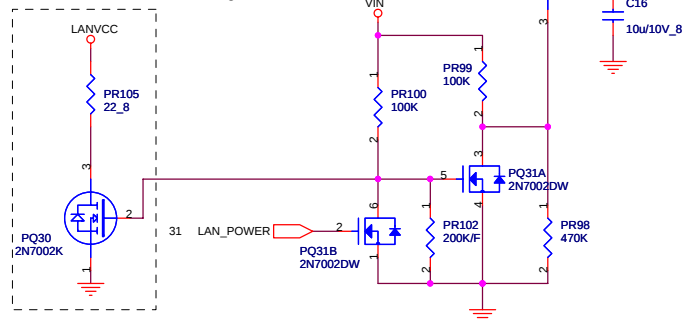


Reserved function

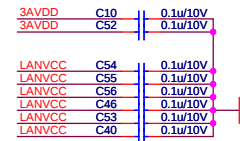
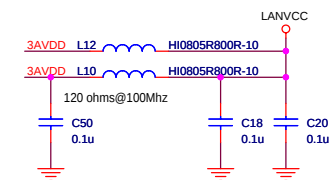




B-Add: LANVCC discharge circuit



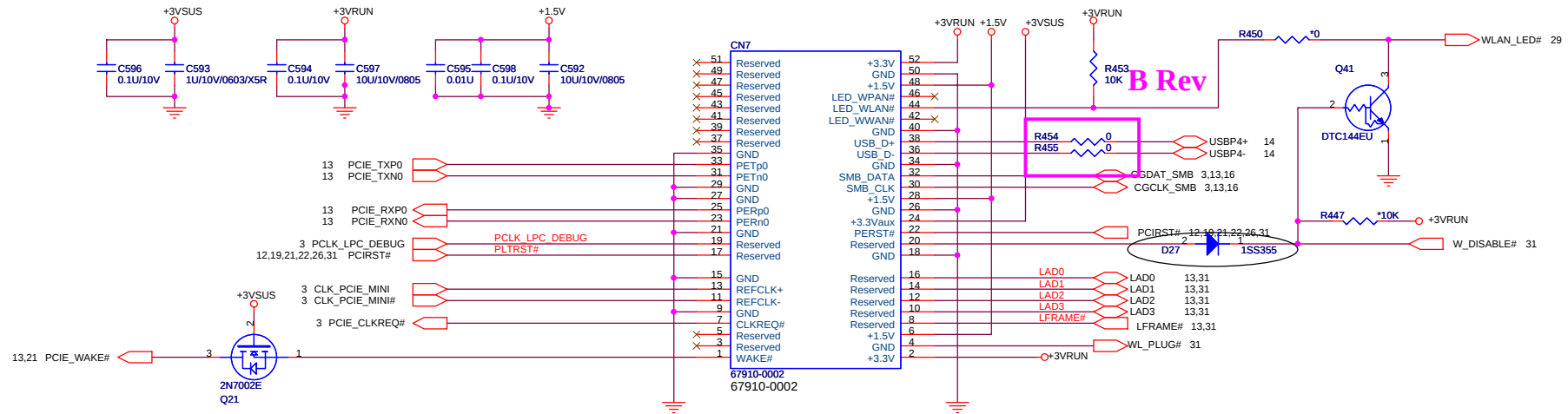
LAN_COL	1		RTL8201BL LED
LAN_RXER_R	0	Default	RTL8201CL LED
LAN_CRS	0	Default	Fiber Mode
	0	Default	UTP Mode
	0	Default	Ensure operating at normal mode



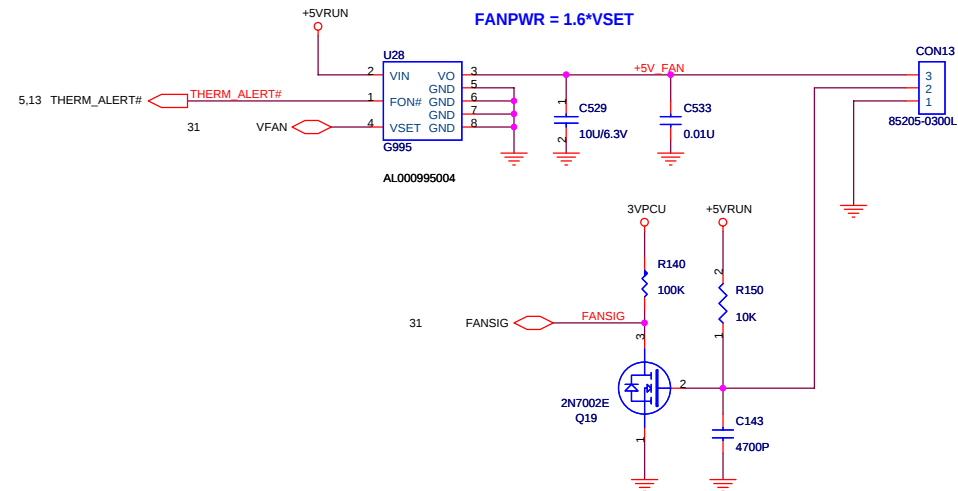
QUANTA
COMPUTER

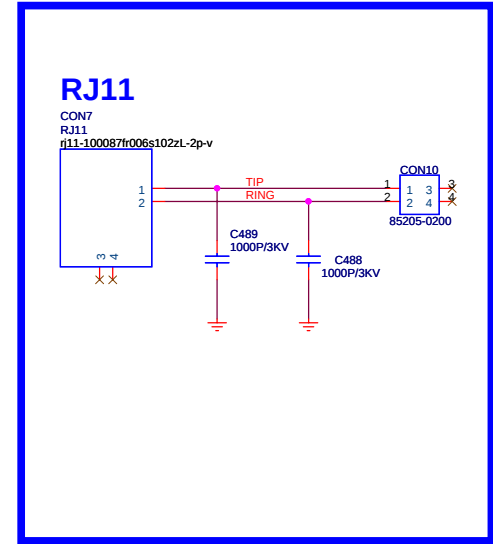
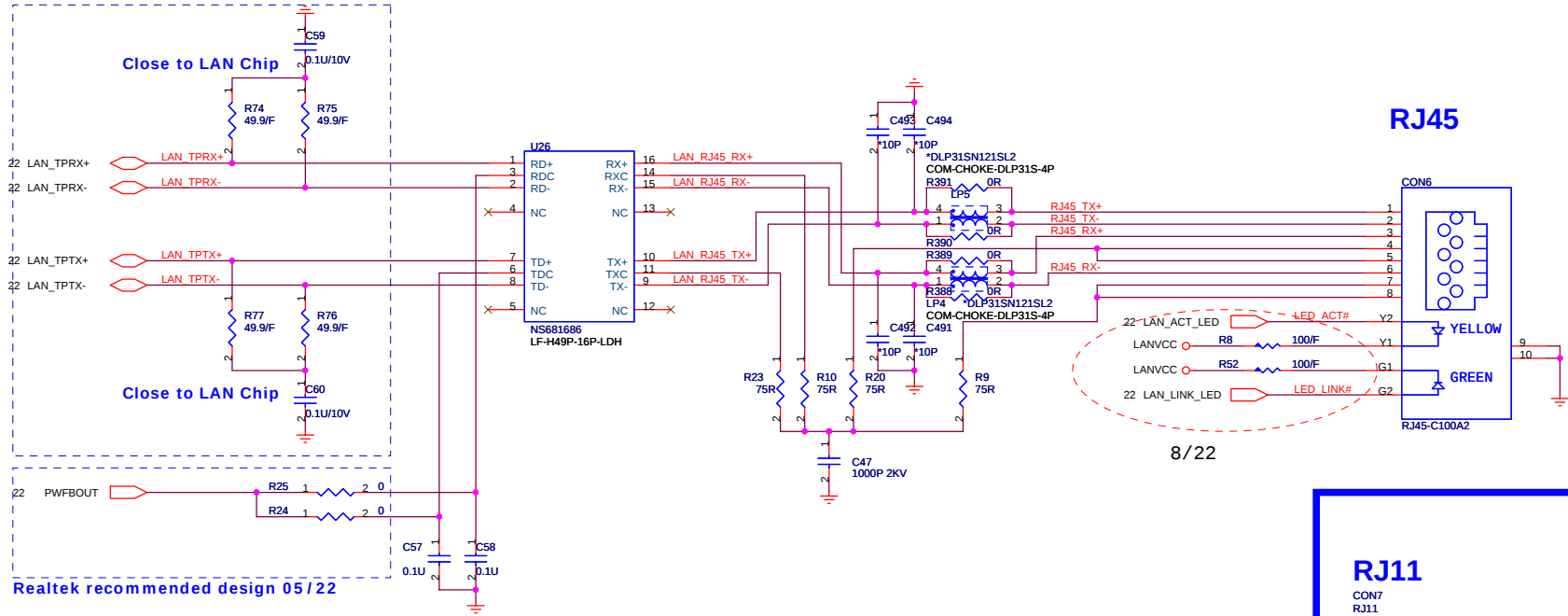
Title	LAN-RTL8201CL		
Size	Document Number	Rev	
Custom	BQ2L MAIN BOARD	1A	
Date:	Friday, August 25, 2006	Sheet	22 of 38

MINI PCI-E CARD

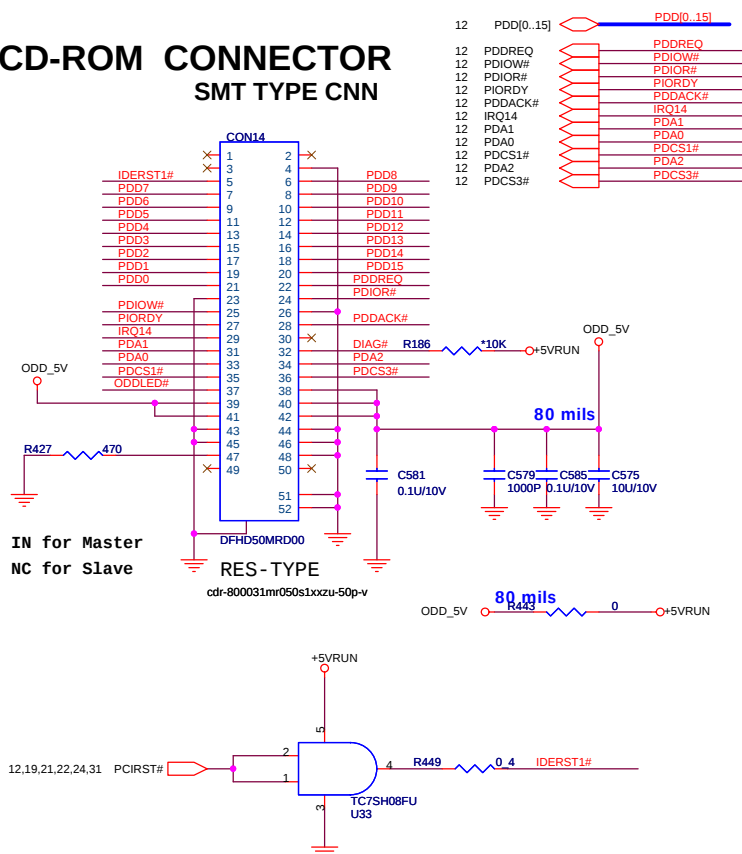


FAN CONN

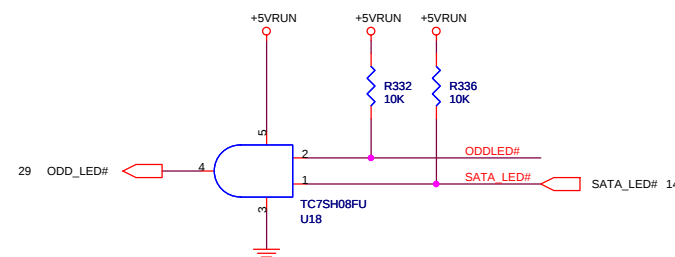
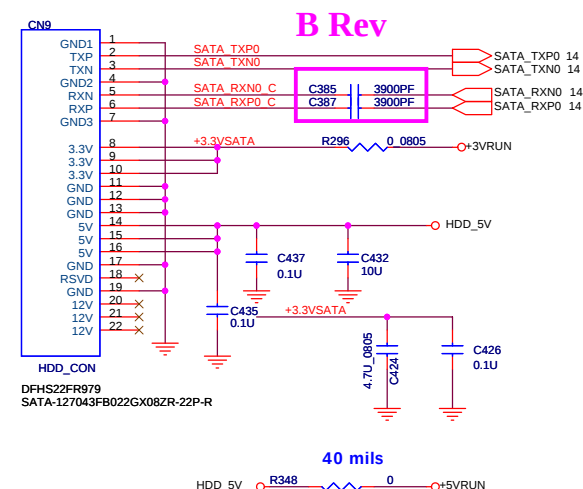


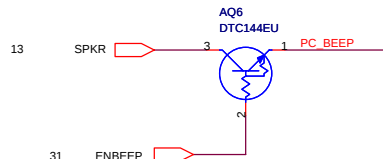


CD-ROM CONNECTOR

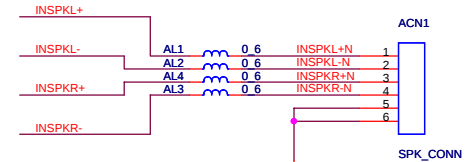
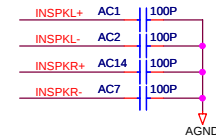
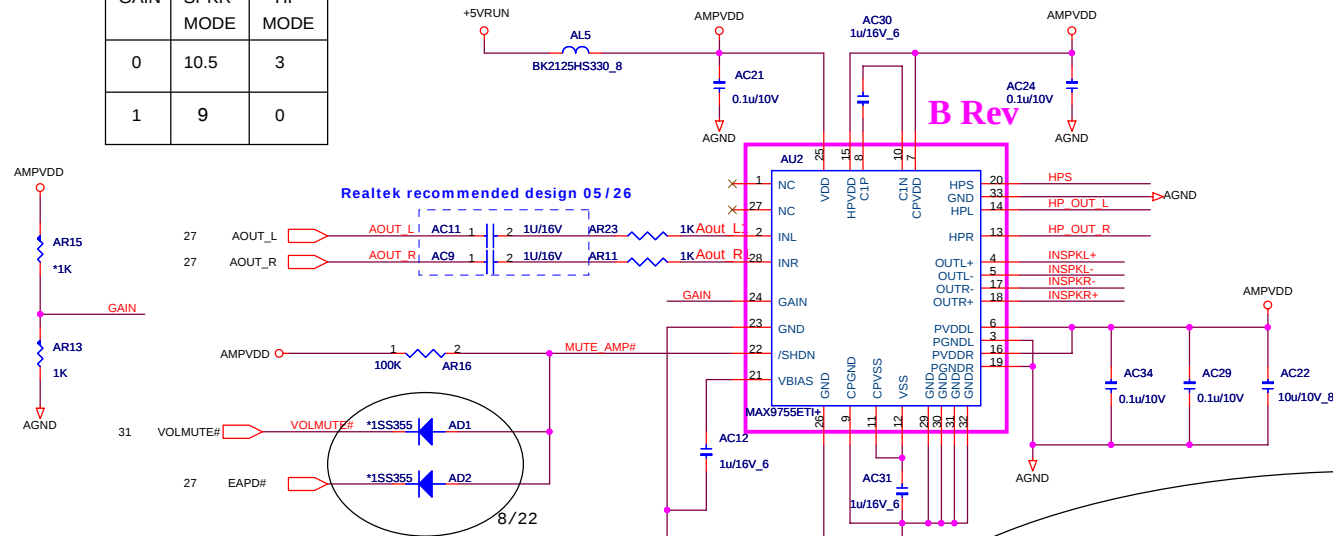


SATA HDD CONNECTOR



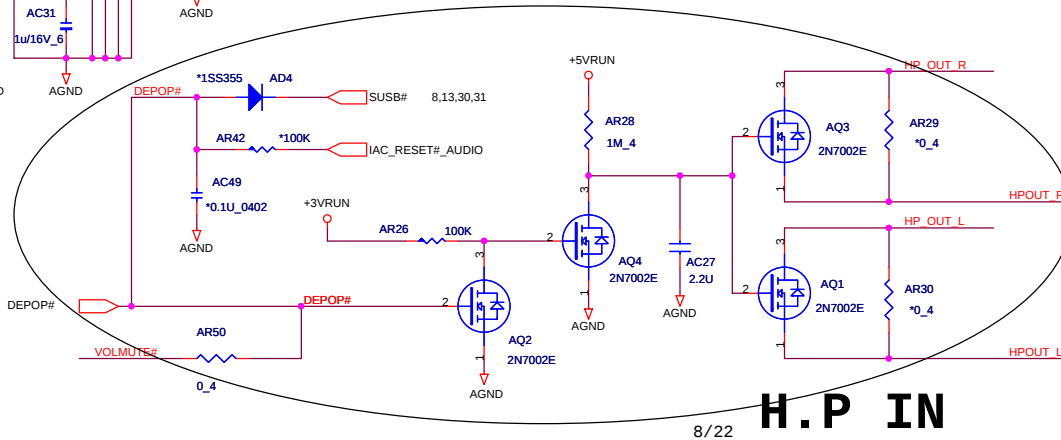
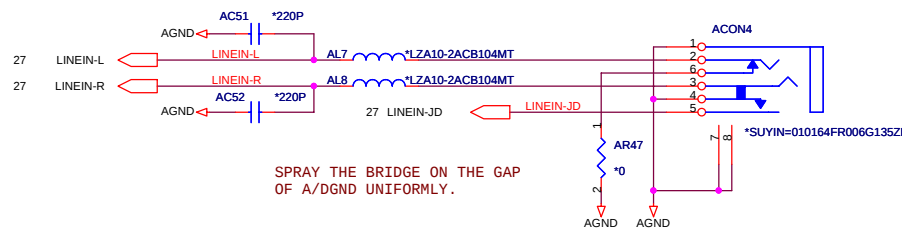


GAIN	SPKR MODE	HP MODE
0	10.5	3
1	9	0



Reserved footprint

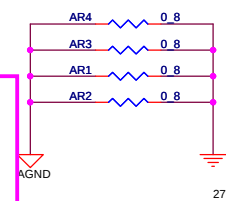
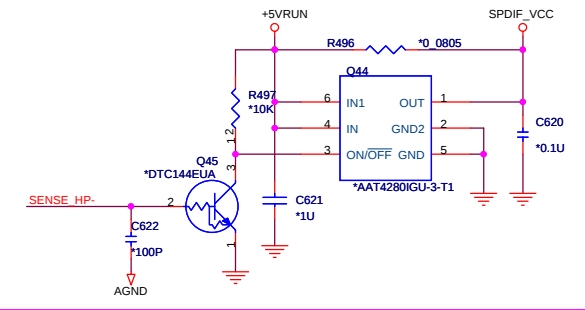
LINE IN



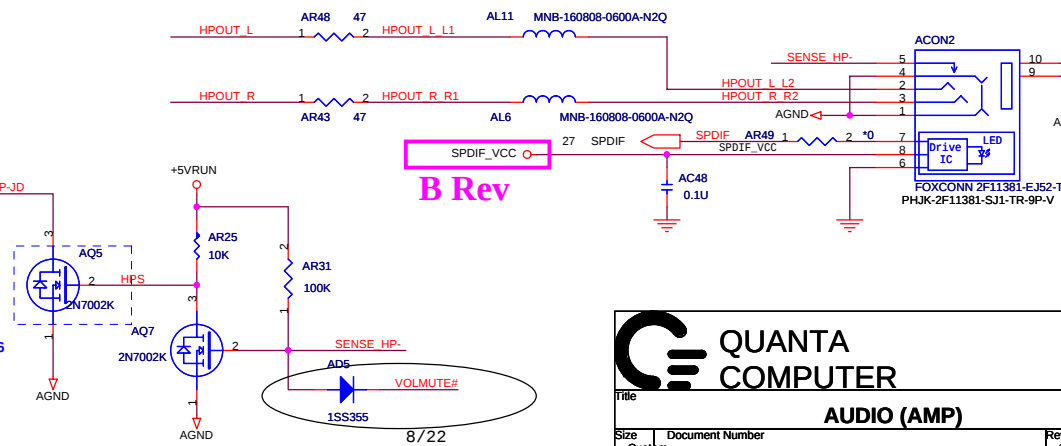
H.P IN

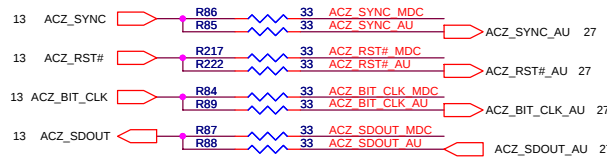
B Rev

SPDIF Power Switch

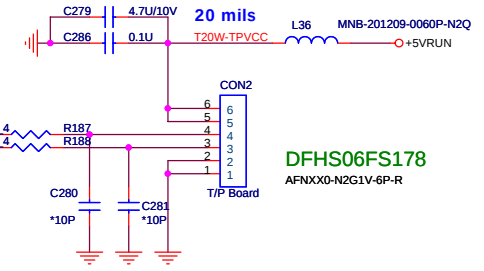


Realtek recommended design 05/26



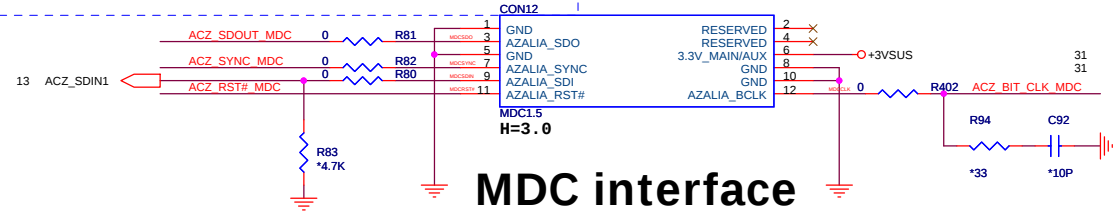


TOUCH PAD

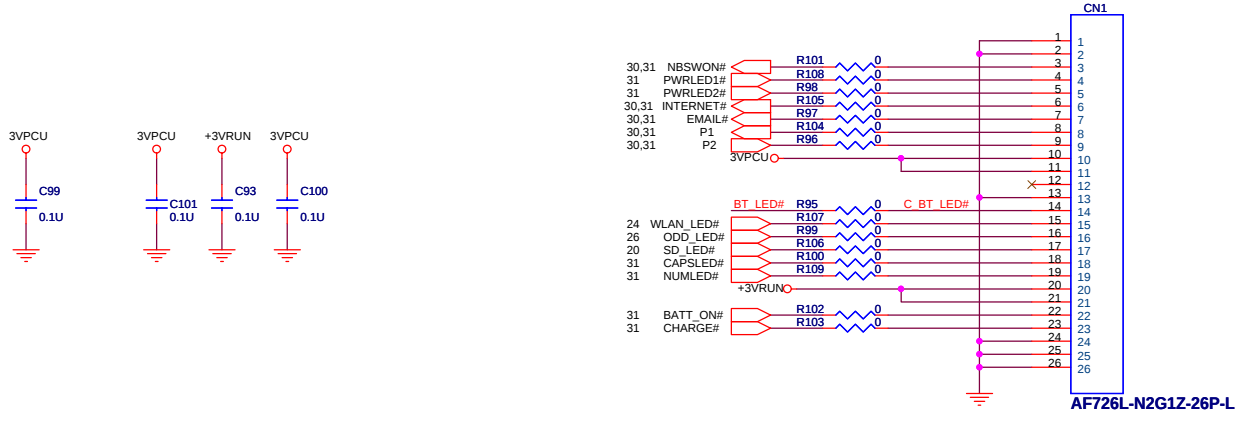


DFHS06FS178
AFNXX0-N2G1V-6P-R

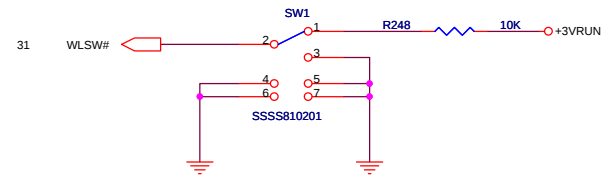
MDC interface



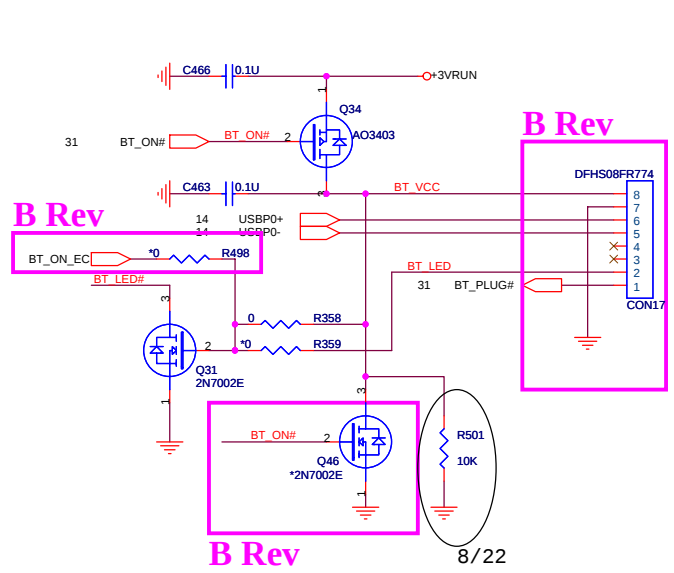
SWITCH/LED BOARD



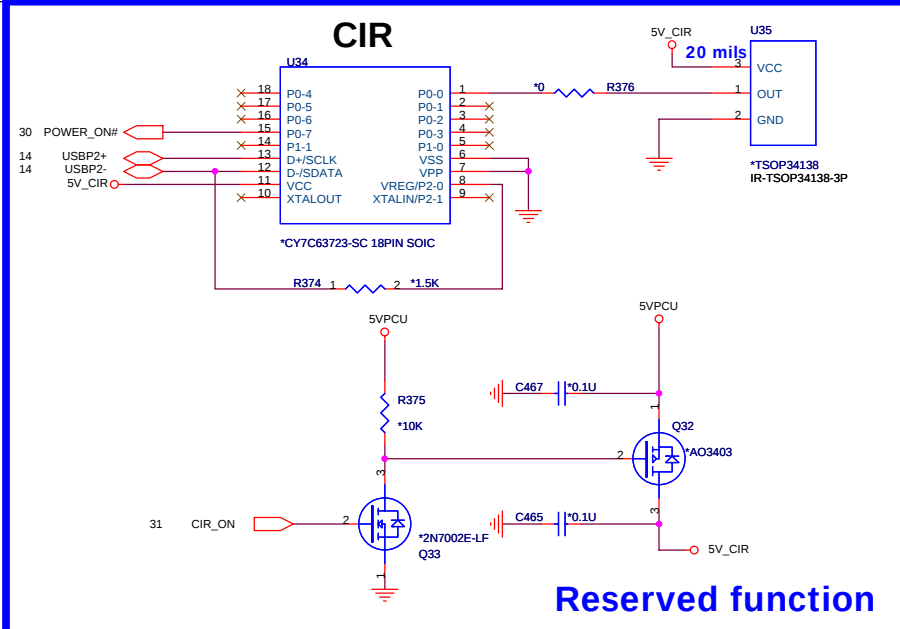
RF SWITCH



BT CONNECTOR

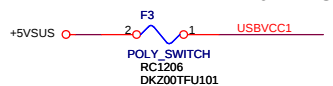


CIR

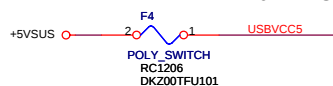


Reserved function

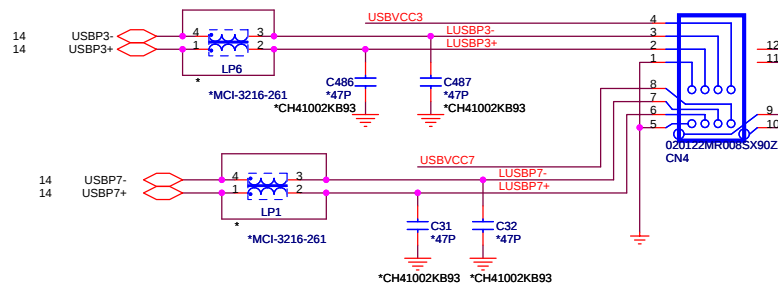
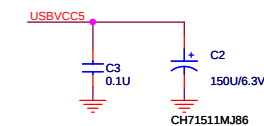
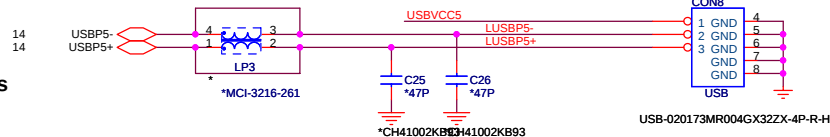
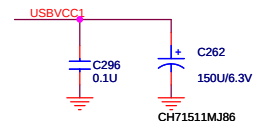
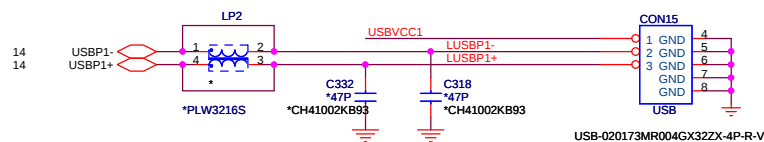
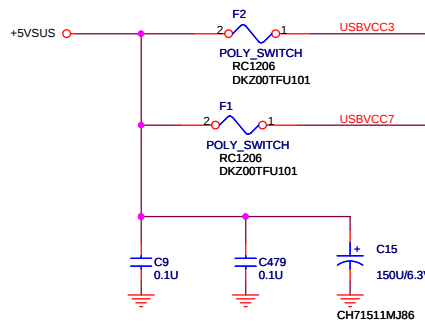
40 mils



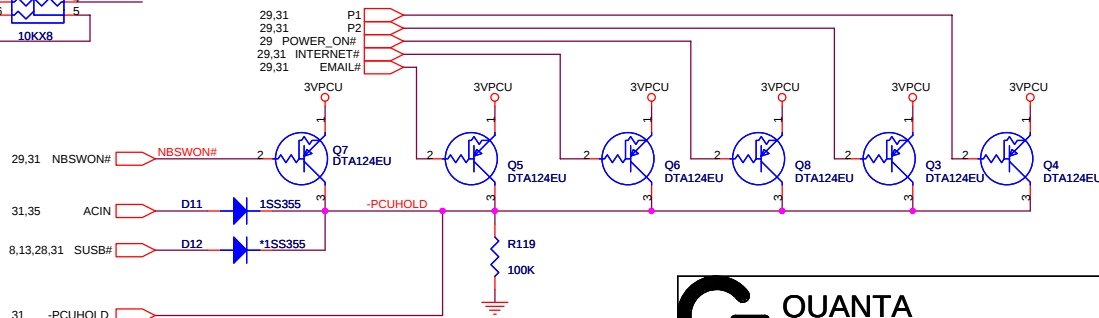
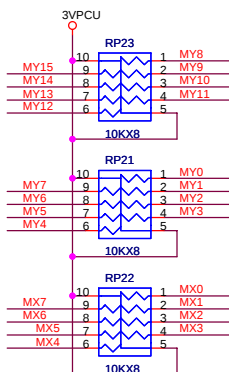
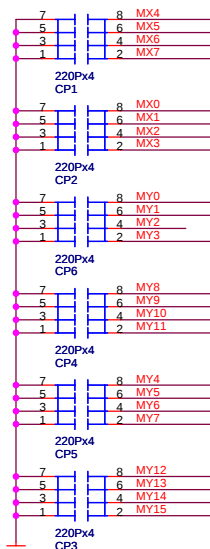
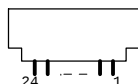
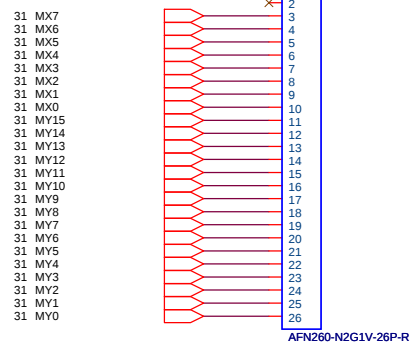
40 mils

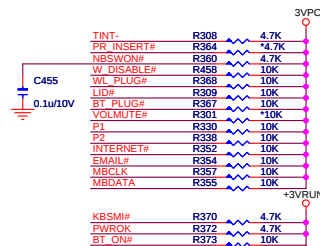


80 mils



INT K/B





MODEL ID

3VPCU

R326 100K

R371 100K

R324

R361

MBID1

MBID2

*0

*0

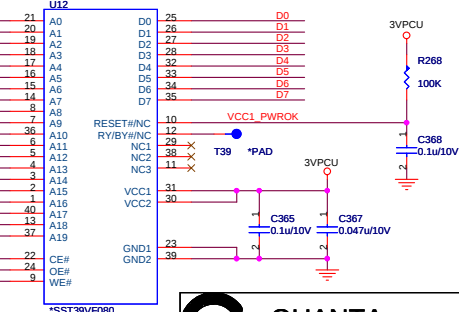
U13

Pin	Signal	Pin	Signal
1	ENV0	13	D0
2	ENV1	14	D1
3	BADDR0	15	D2
4	BADDR1	16	D3
5	TRIS	17	D4
6	SHBM	18	D5
7	A6	19	D6
8	A7	20	D7
9	A8	21	A17
10	A9	22	VCC
11	A10		
12	A11		
13	A12		
14	A13		
15	A14		
16	A15		
17	A16		
18	CS#		
19	RD#		
20	WR#		
21	A18		
22			

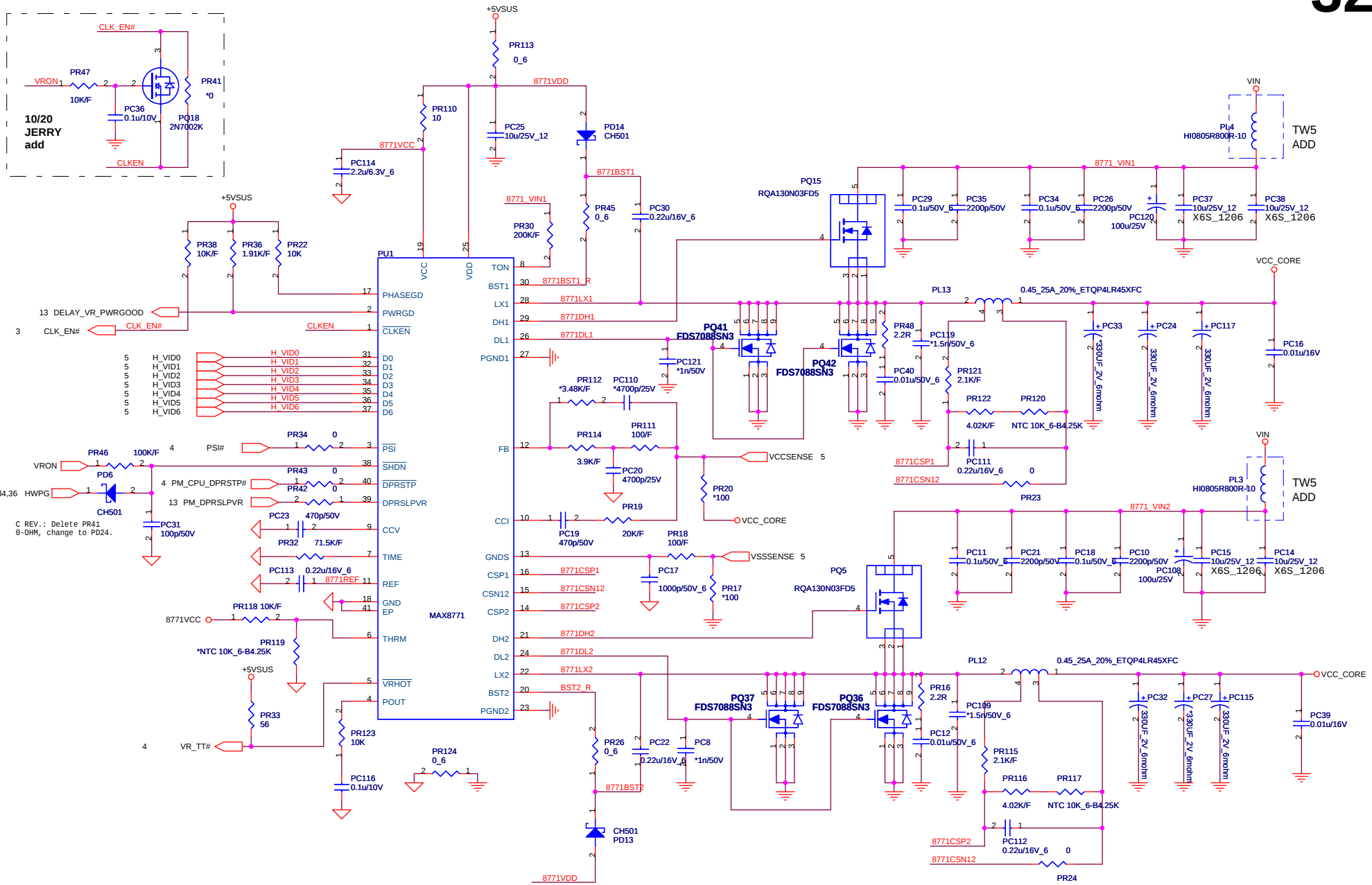
39VF04 PLLC

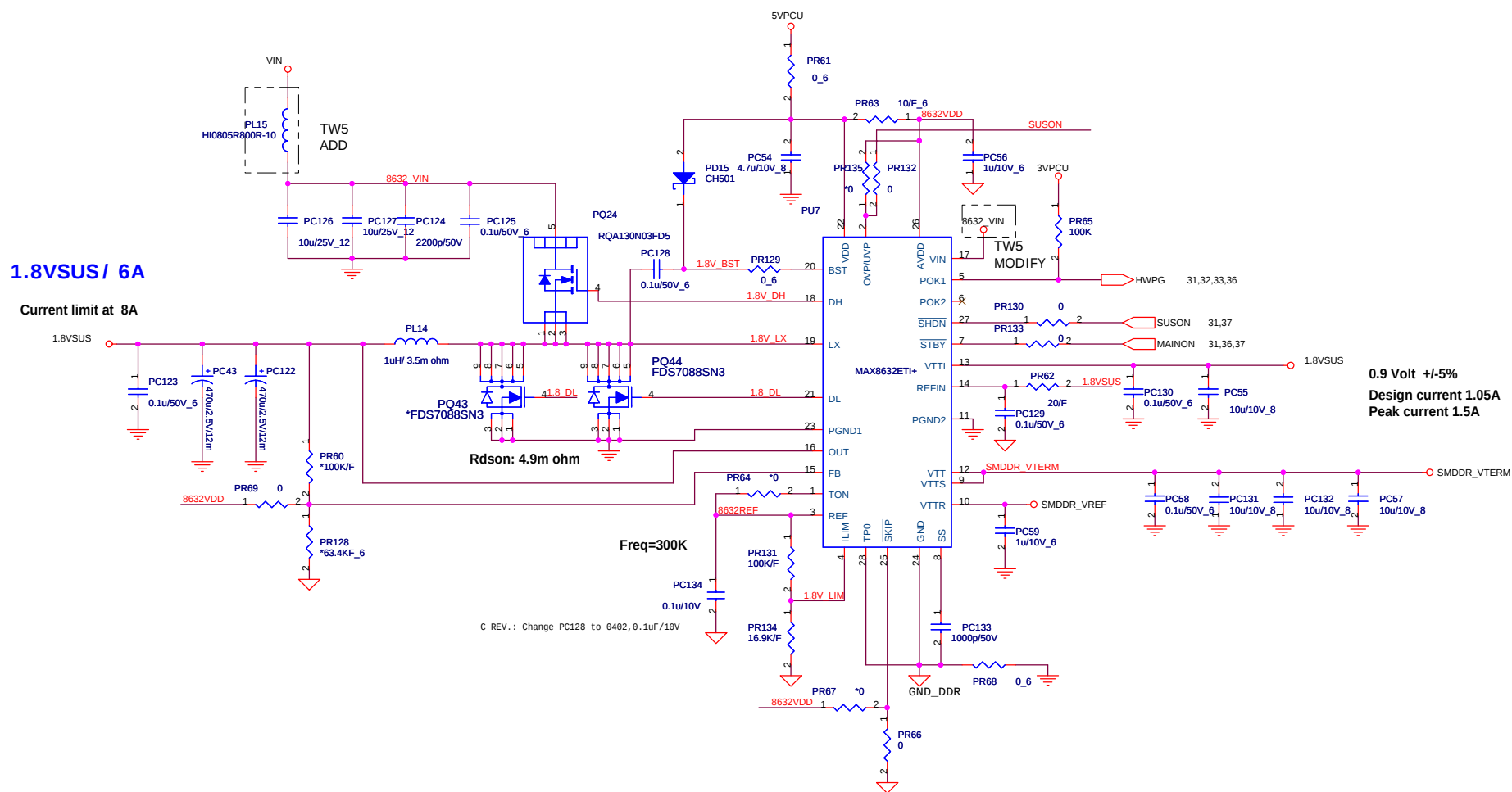
AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

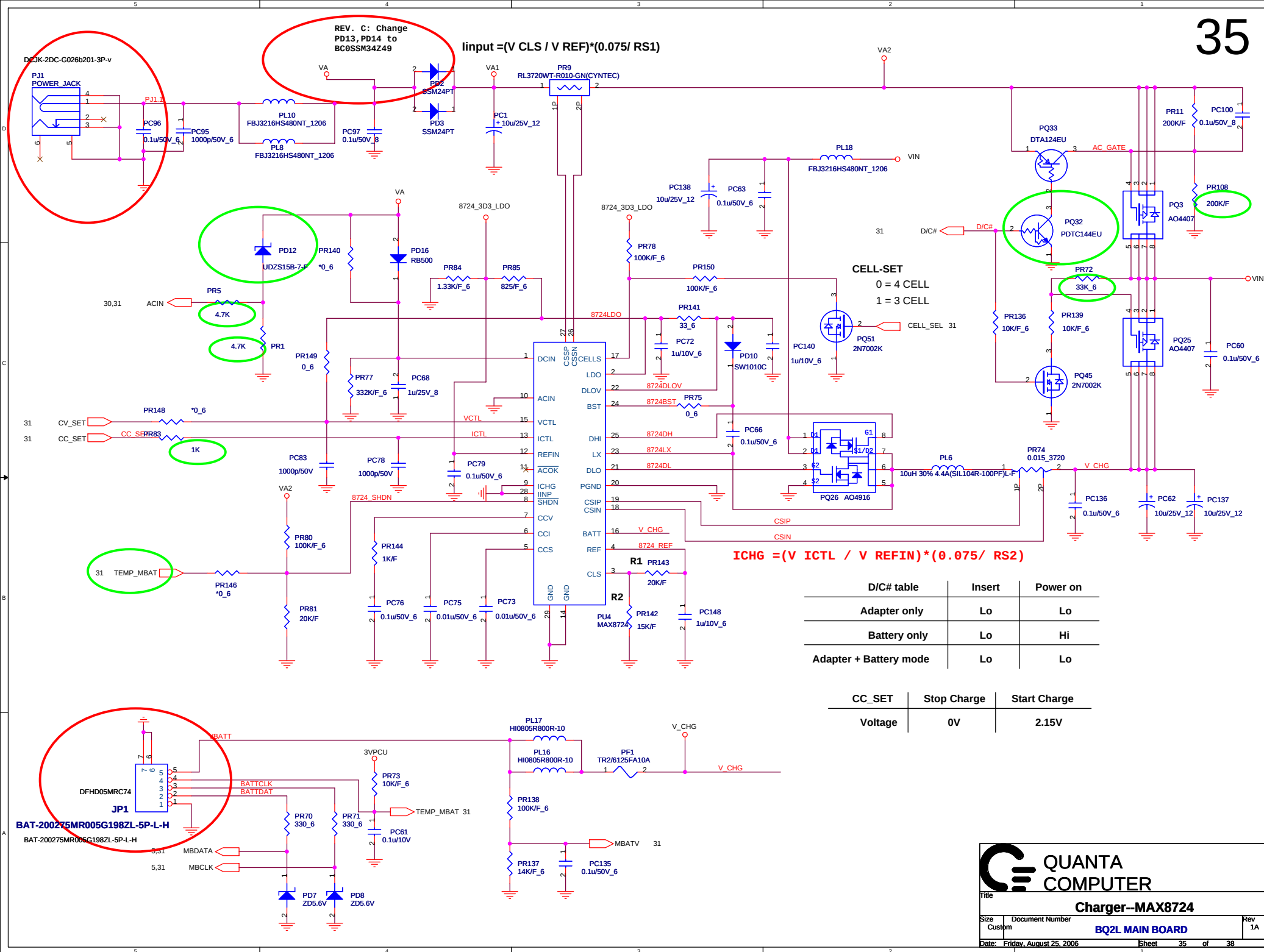
FLASH:
MXI: AKE358AKZ87
SST: AKE35ZAKK17



1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.



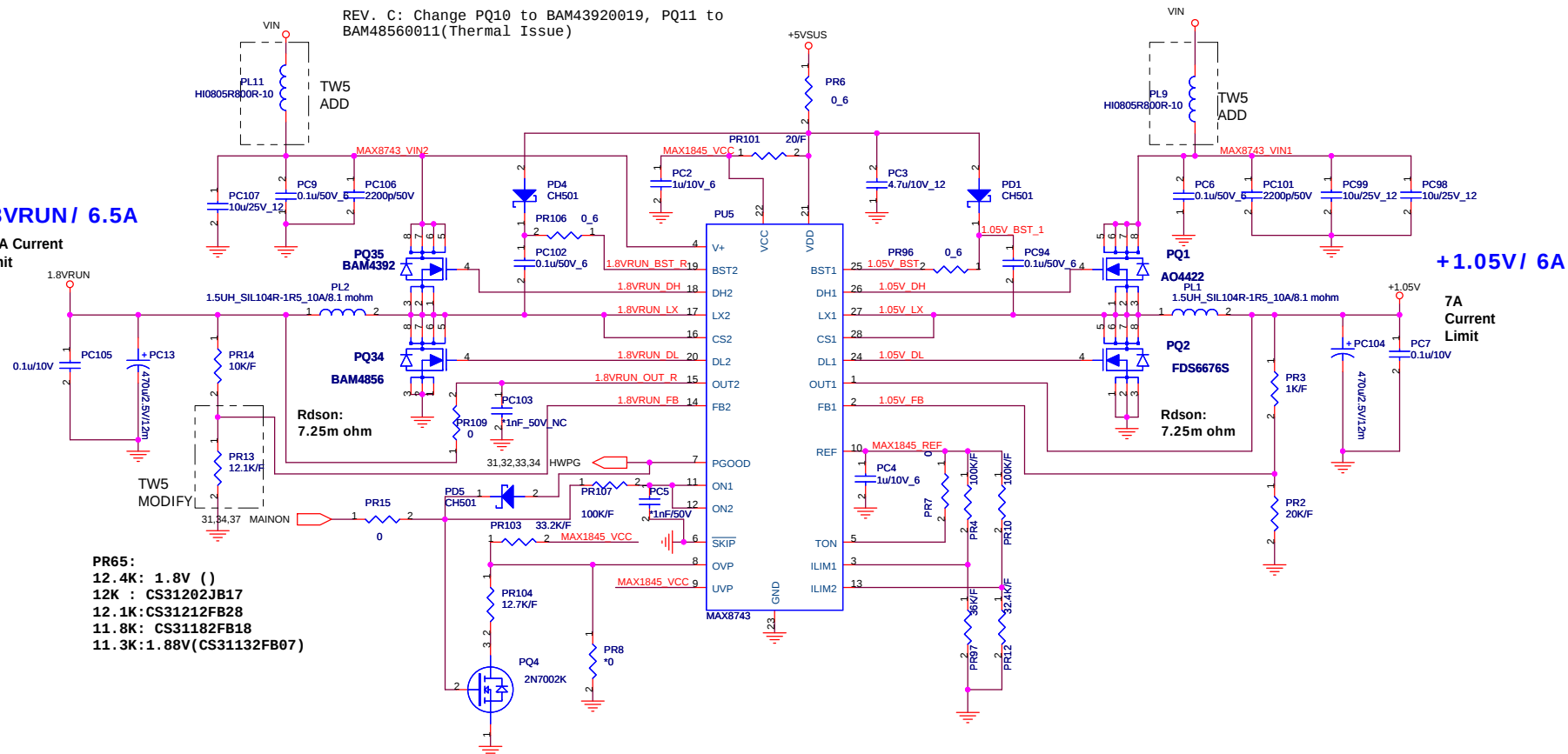




REV. C: Change PQ10 to BAM43920019, PQ11 to
BAM48560011(Thermal Issue)

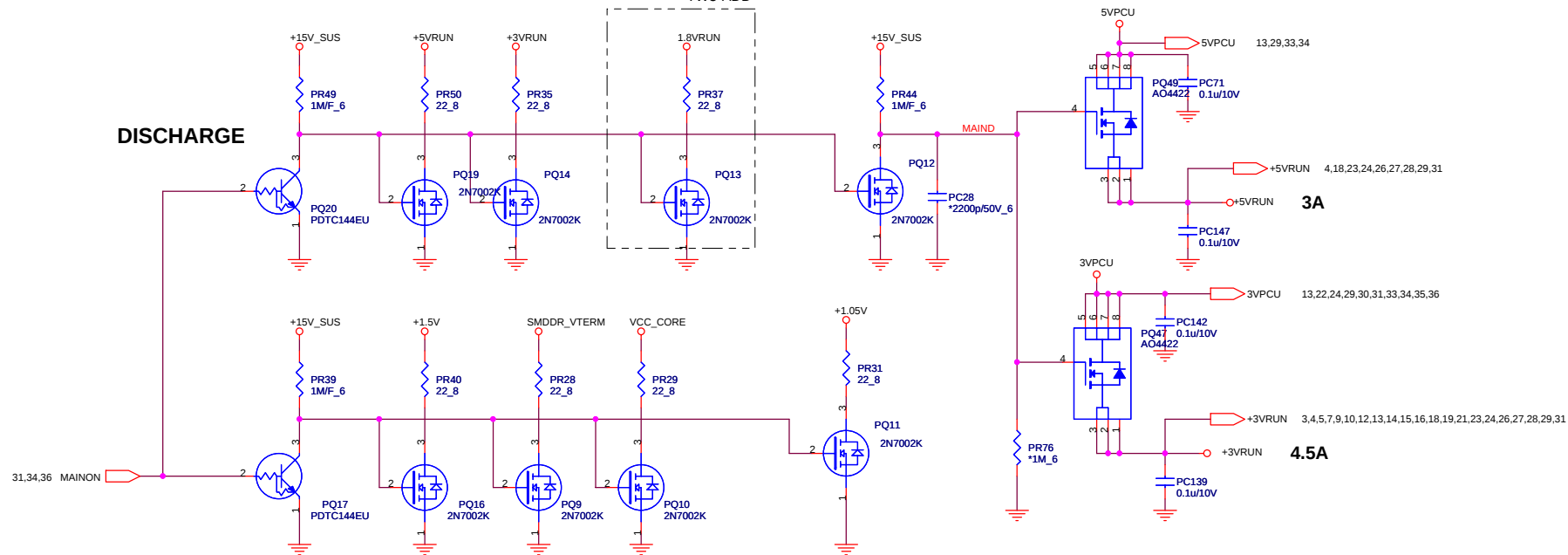
1.8VRUN/ 6.5A

**7.5A Current
Limit**

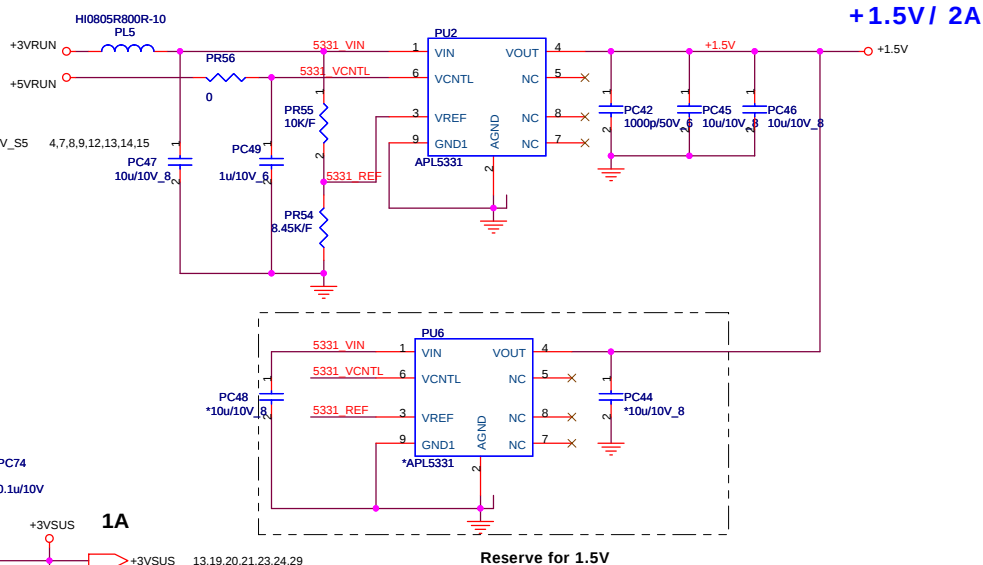
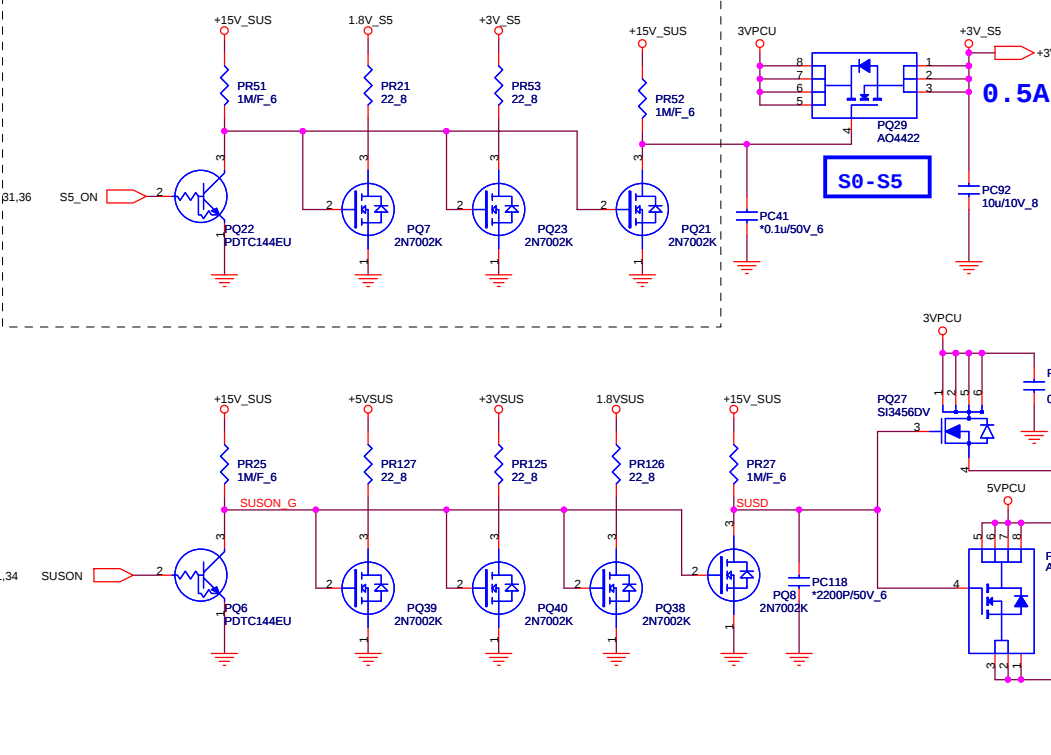


1.8V_S5 / 200mA

TW5 Add



B-Add: +3V_S5, 1.8V_S5 discharge circuit



B Rev

PAGE-13:SB_HWSPND# change GPIO6 from GPIO0 for reserved function.

PAGE-21:To support newcard hot-plug function.The newcard WAKE# pin must connected to 966L PME# pin.

PAGE-24:Add R454,R455 to support SiS PCIE wireless card.

PAGE-25:Add the connection between GND and LAN_GND

PAGE-26:C385,C387 change 3900PF from 0.01UF

PAGE-28:<1>AU2 change footprint from QFN28-5*5-5 to QFN28-5*5-5-29P

<2>Add SPDIF Power switch design

PAGE-29:<1>B/T interface change PIN definition.

<2>Add Q46 for BT_VCC discharge function.To fix B/T LED abnormal display

<3>Reserved R498 component.EC can control B/T LED.

PAGE-31>Delete PIN175 of signal nets.

QUANTA
COMPUTER

Title		
CHANGE HISTORY		
Size Custom	Document Number BQ2L MAIN BOARD	Rev 1A
Date: Friday, August 25, 2006	Sheet 1	38 of 38