

FM7 Hepburn Intel Discrete GFX

VER : D3B

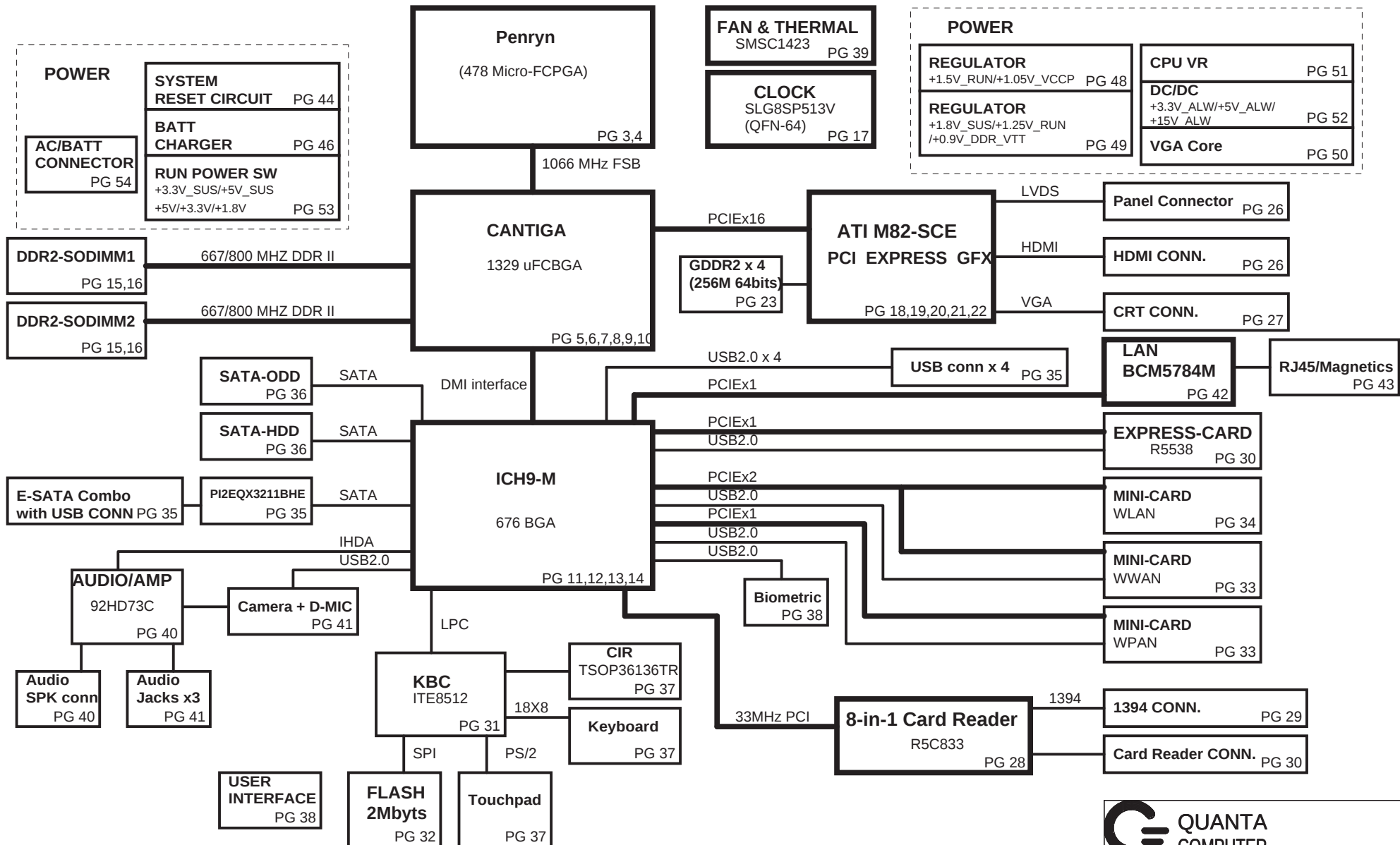


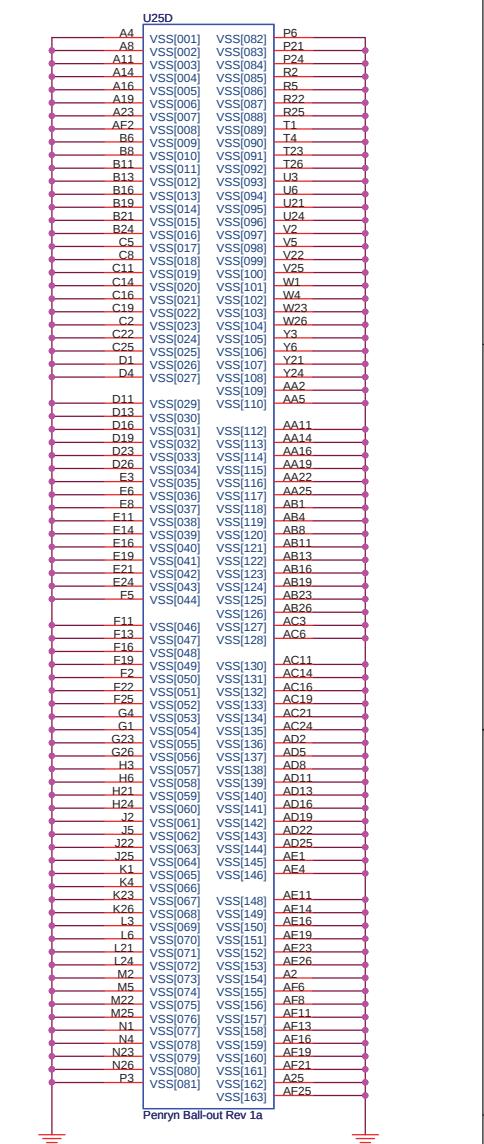
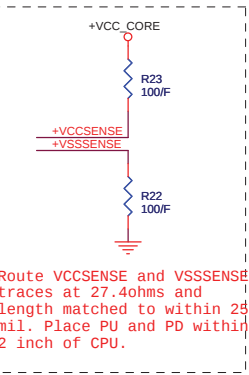
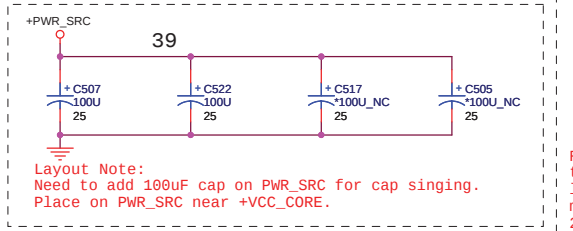
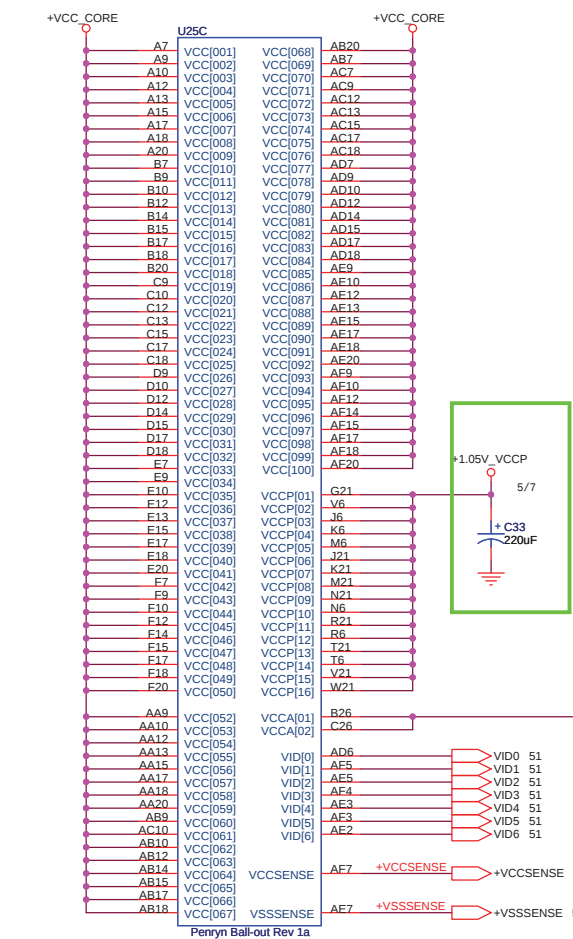
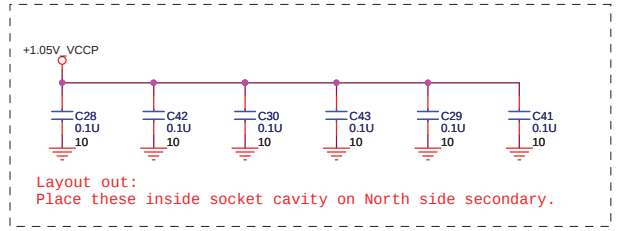
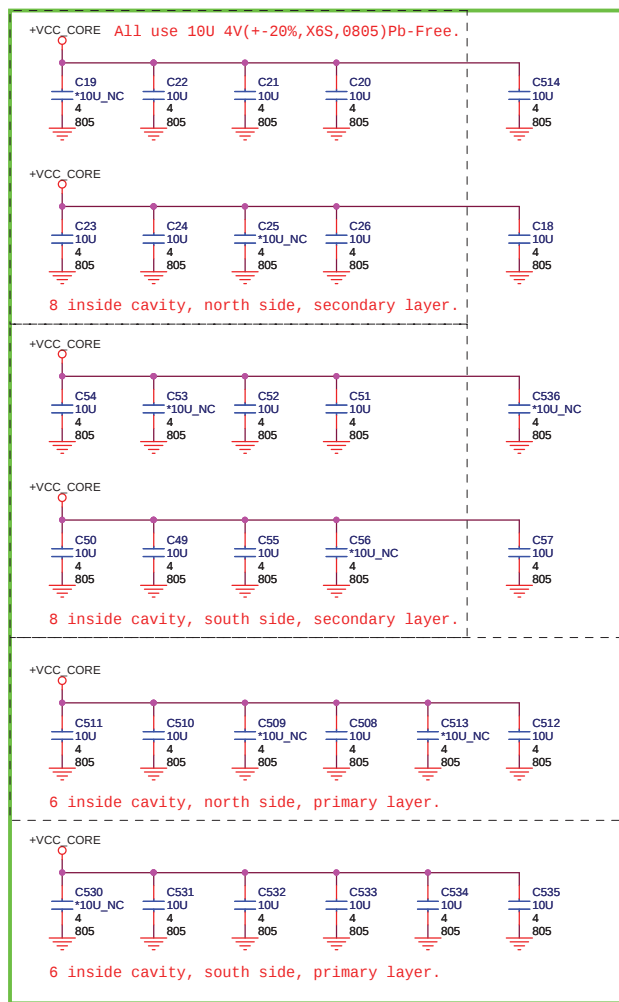
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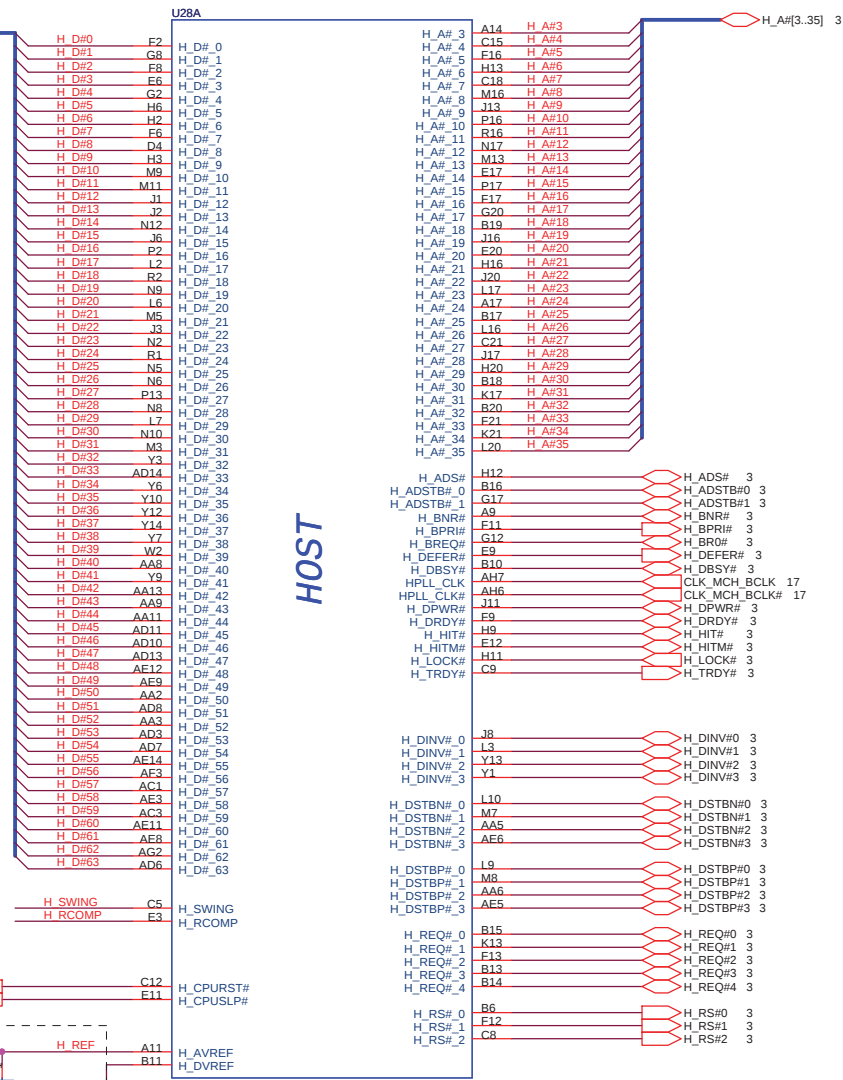
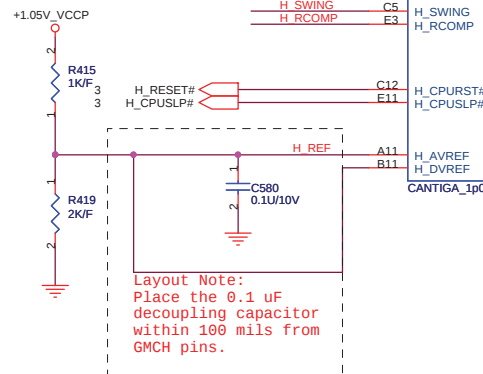
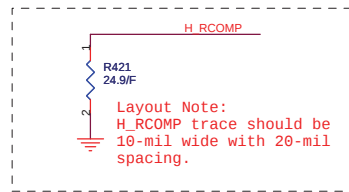
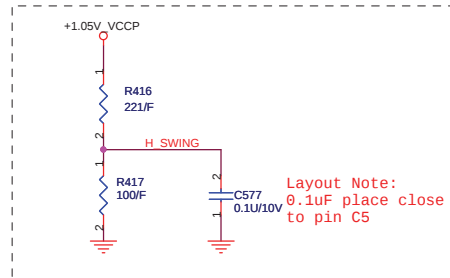
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25	BLANK PAGE
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27	CRT CONN
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31	SIO (ITE8512)
32	FLASH / RTC
33	MINI-Card (WPAN, WWAN)
34	MINI-Card (WLAN)
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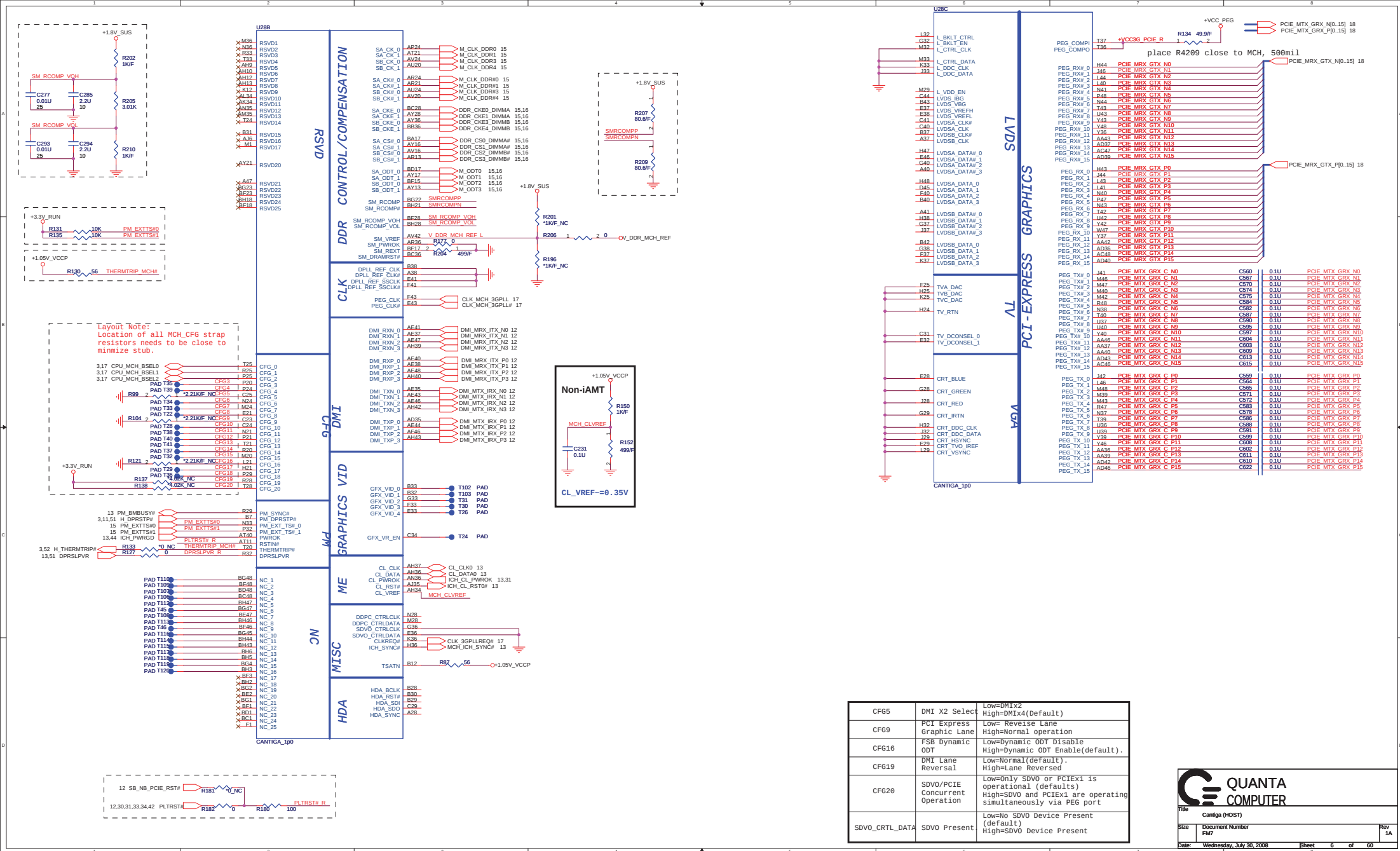
Power States

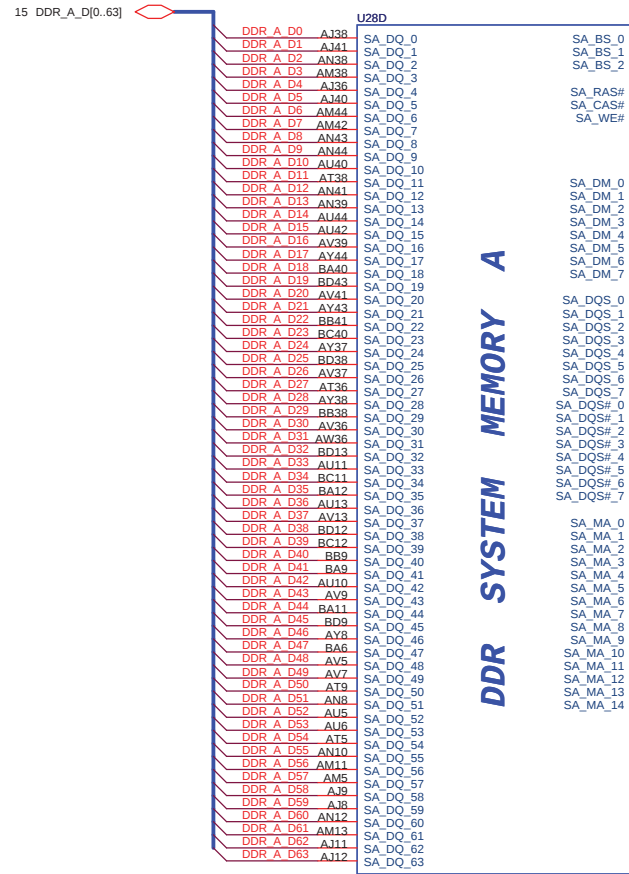
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,46,48,49,50,51,52,56	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0~S5
+5V_ALW2	+5V	37,38,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,26,30,37,38,43,48,49,50,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,26,27,36,37,38,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	6,8,9,11,12,13,14,15,17,19,20,22,26,27,28,30,31,33,34,36,38,39,40,41,42,53,56	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,53,56	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.2V_LOM	+1.25V	42	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.1V_GFX_PCIE	+1.1V	21,50	VGA POWER	RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,48,56	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,51,56	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	

GND PLANE	PAGE	DESCRIPTION
 8731AGND	46	
 AGND_0.9V	49	
 AGND_DC/DC	52	
 AGND_DC2	48	
 AGND_DDR	49	
 AGND_ISL6260	51	
 GND	ALL	

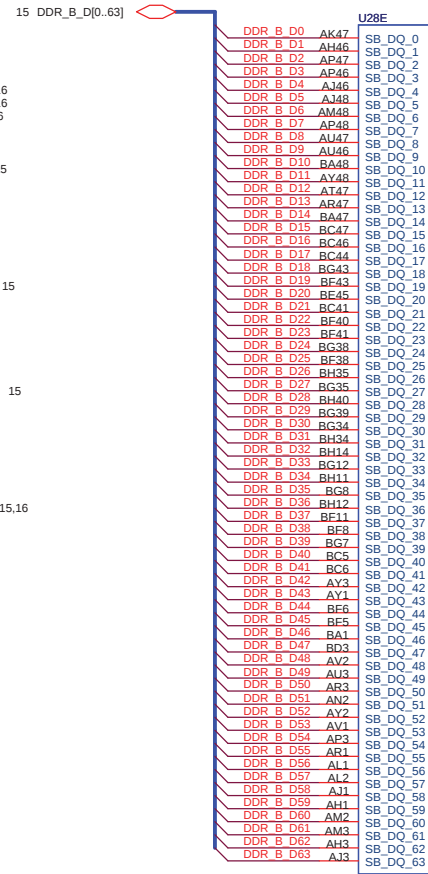




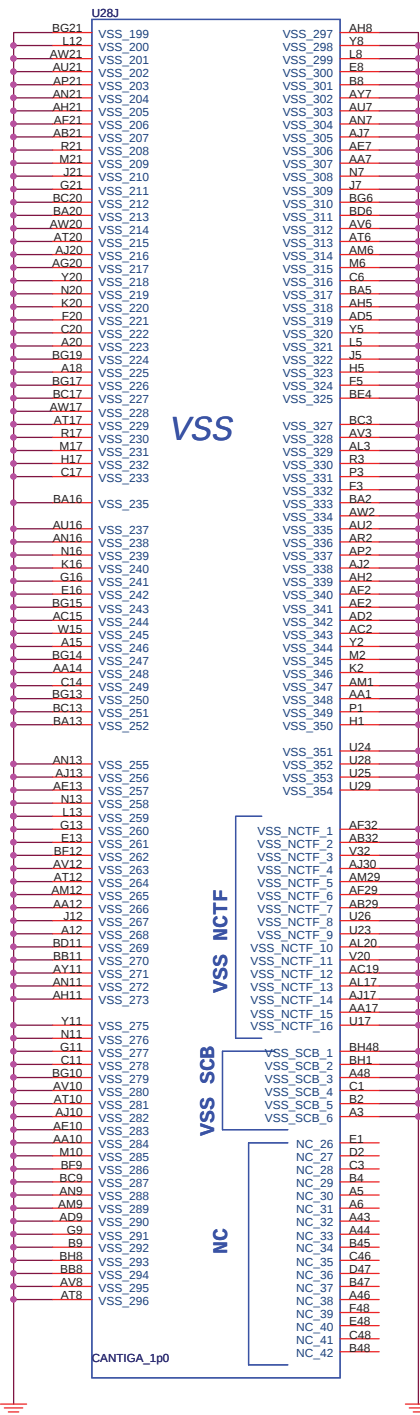
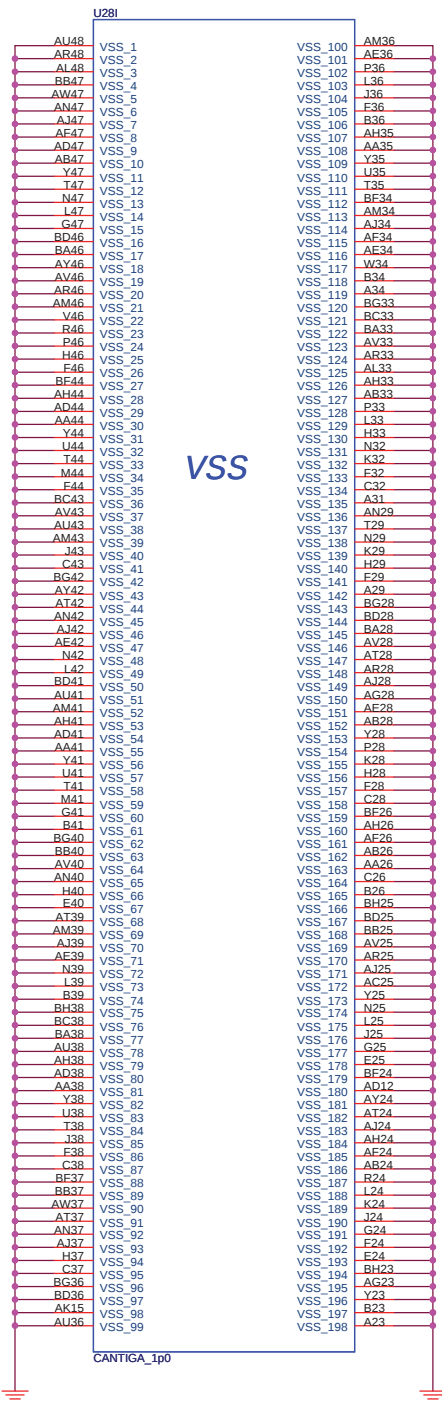




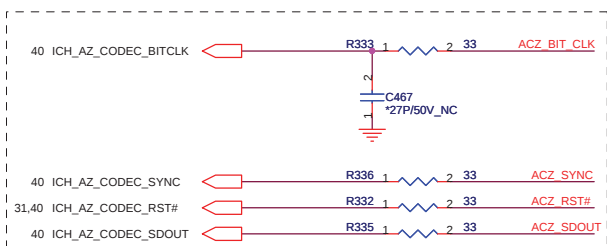
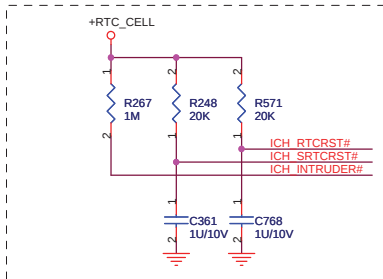
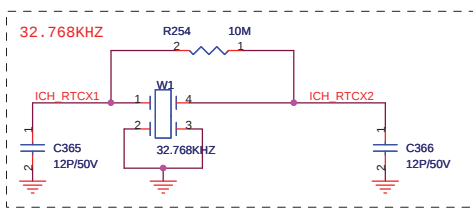
DDR SYSTEM MEMORY A



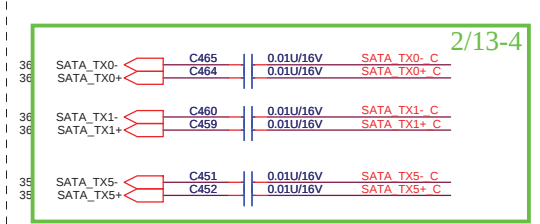
DDR SYSTEM MEMORY B



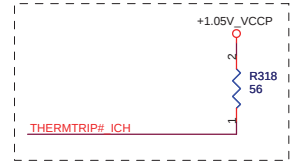
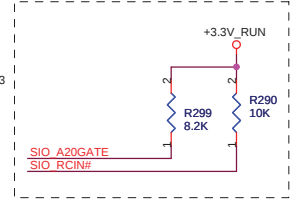
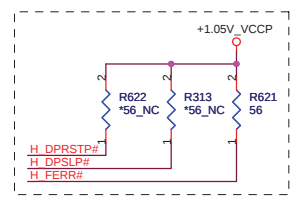
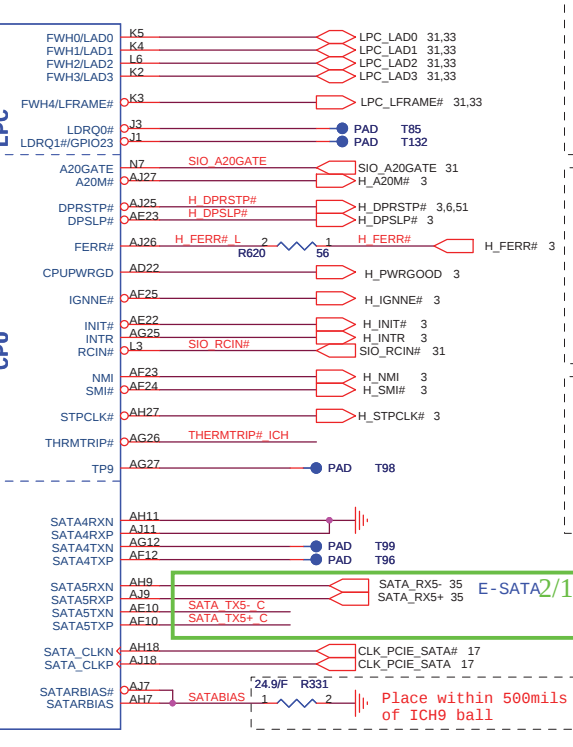
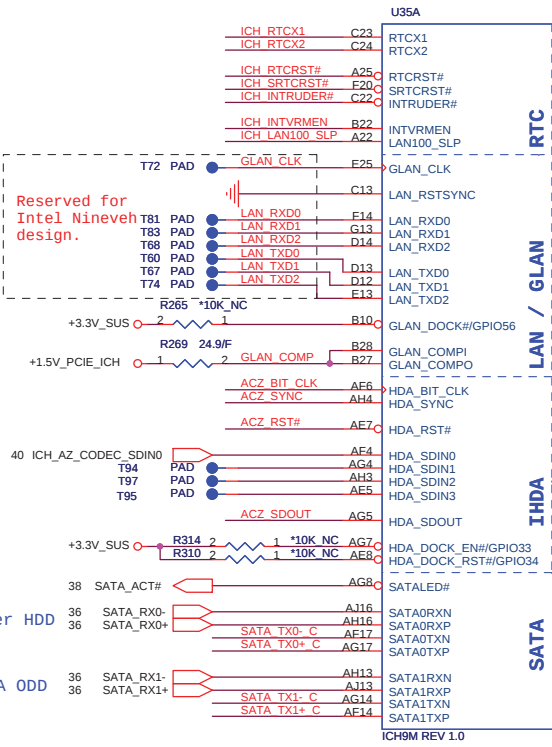
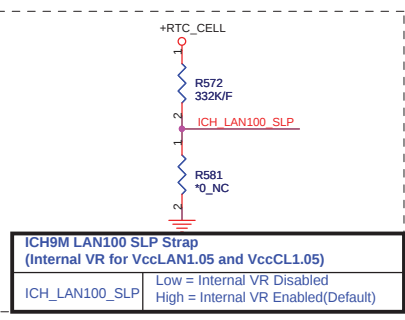
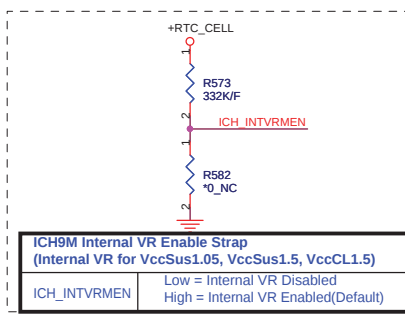
Title Cantiga (HOST)		
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Place all series terms close to ICH9 except for SDIN input lines, which should be close to source. Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respectively. Basically, keep the same distance from T for all series termination resistors.



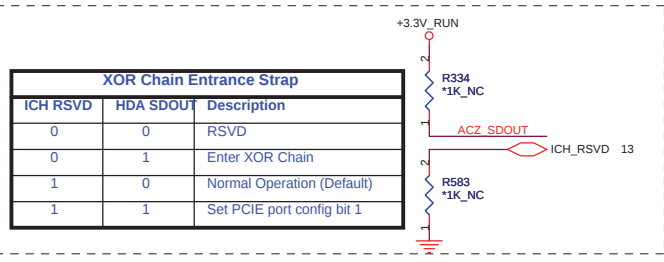
Distance between the ICH-9 M and cap on the "P" signal should be identical distance between the ICH-9 M and cap on the "N" signal for same pair.



Master HDD

SATA ODD

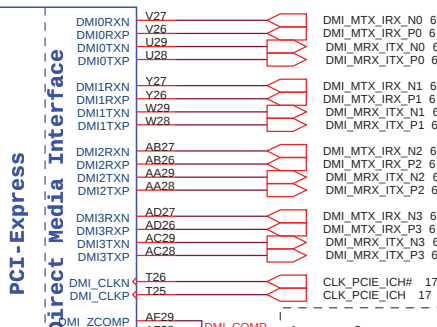
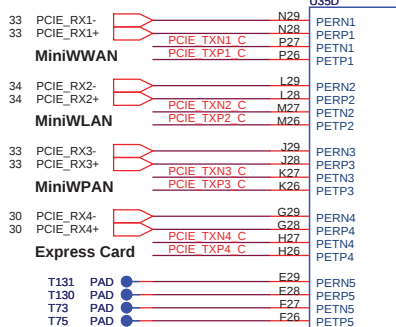
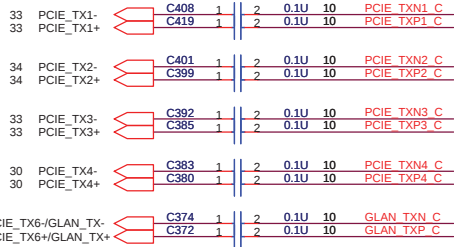
E-SATA2/13-4



XOR Chain Entrance Strap		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIe port config bit 1



Place TX DC blocking caps close ICH8.

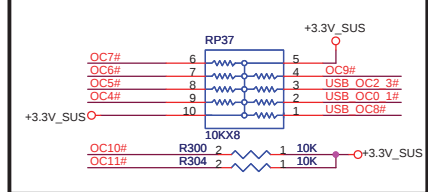
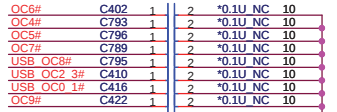


Boot BIOS Strap			
		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

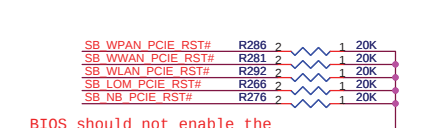
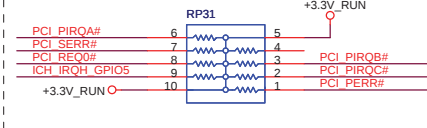
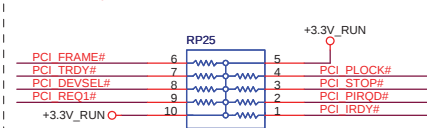
Places within 500 mils of the ICH9



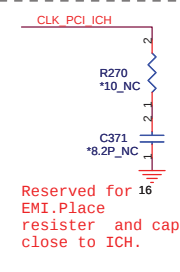
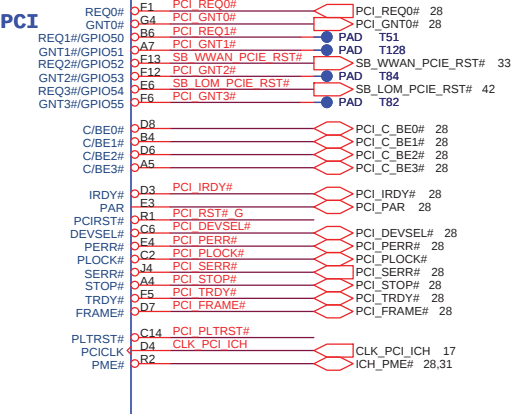
WWAN Noise - ICH improvements



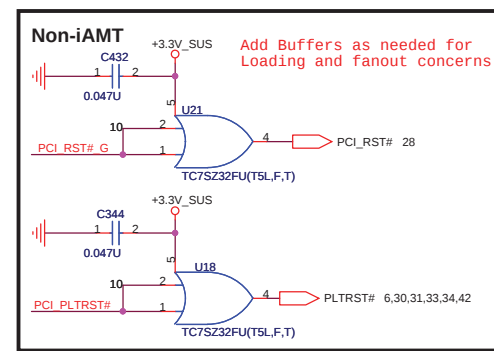
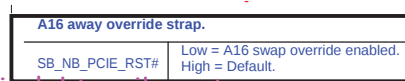
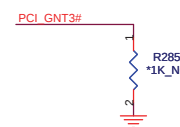
PCI Pullups



BIOS should not enable the internal GPIO pull up resistor.



Reserved for EMI. Place resistor and cap close to ICH.



Add Buffers as needed for Loading and fanout concerns.

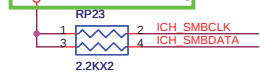


Title			ICH9M (USB, DMI, PCIE, PCI)
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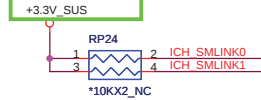
2/13-5 2/18-19

Non-iAMT

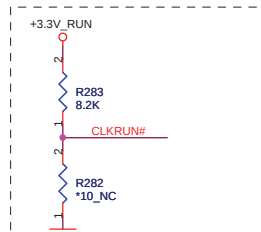


2/13-5 2/18-19

Non-iAMT

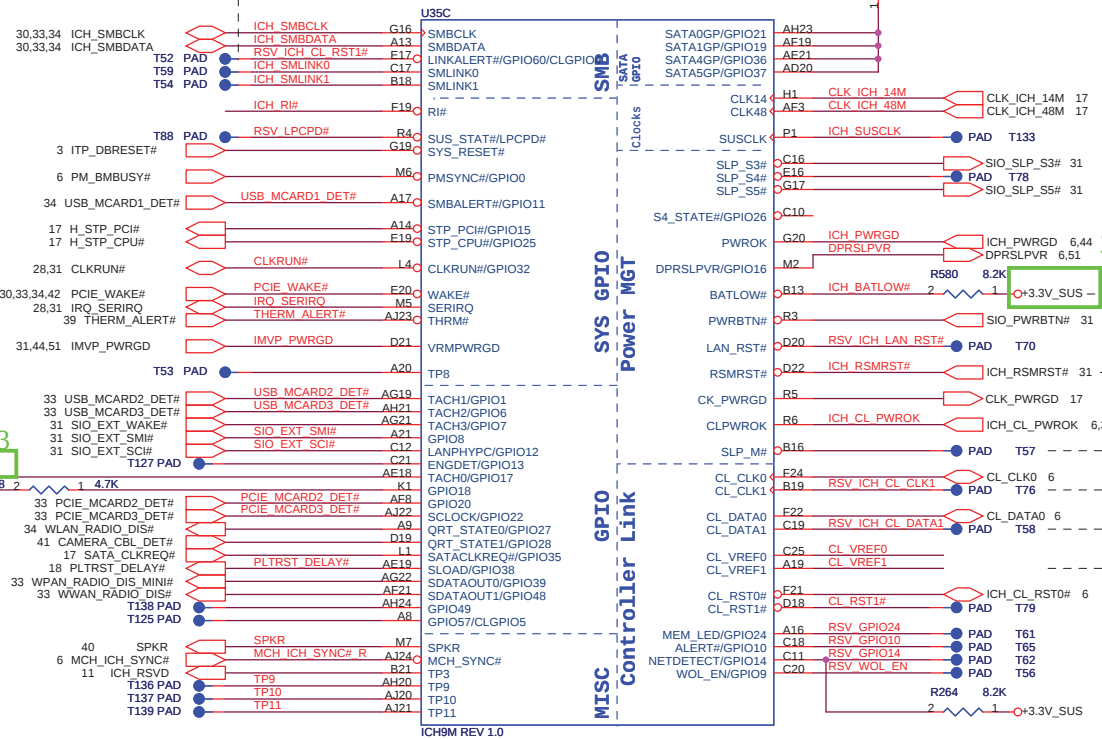
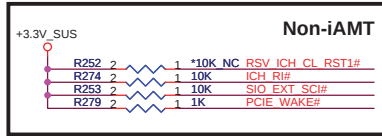
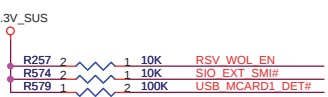
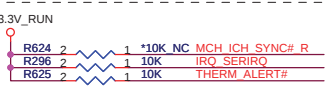
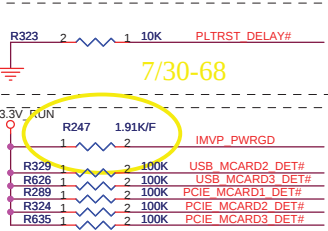


ASF 2.0

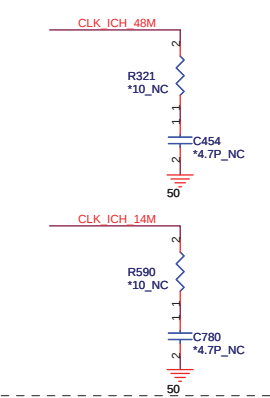


Option to "Disable" clkrun. Pulling it down will keep the clks running.

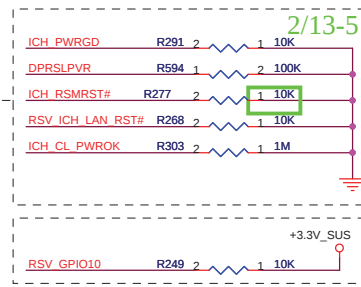
2/25-29 6/11-53



Place these close to ICH8.

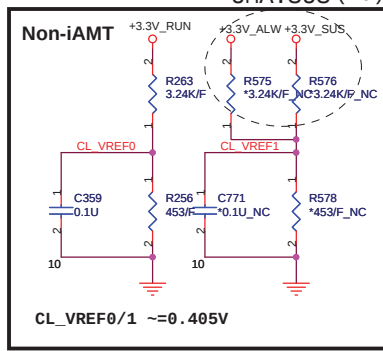


2/13-5



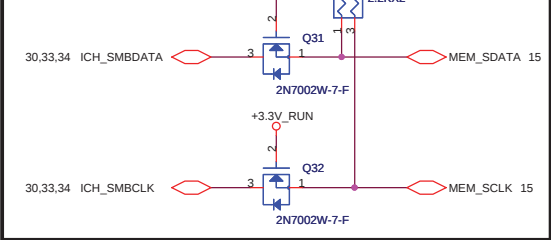
Non-iAMT

DIS:ALW
UMA:SUS (19)



SMbus address D2

These are for backdrive issue.



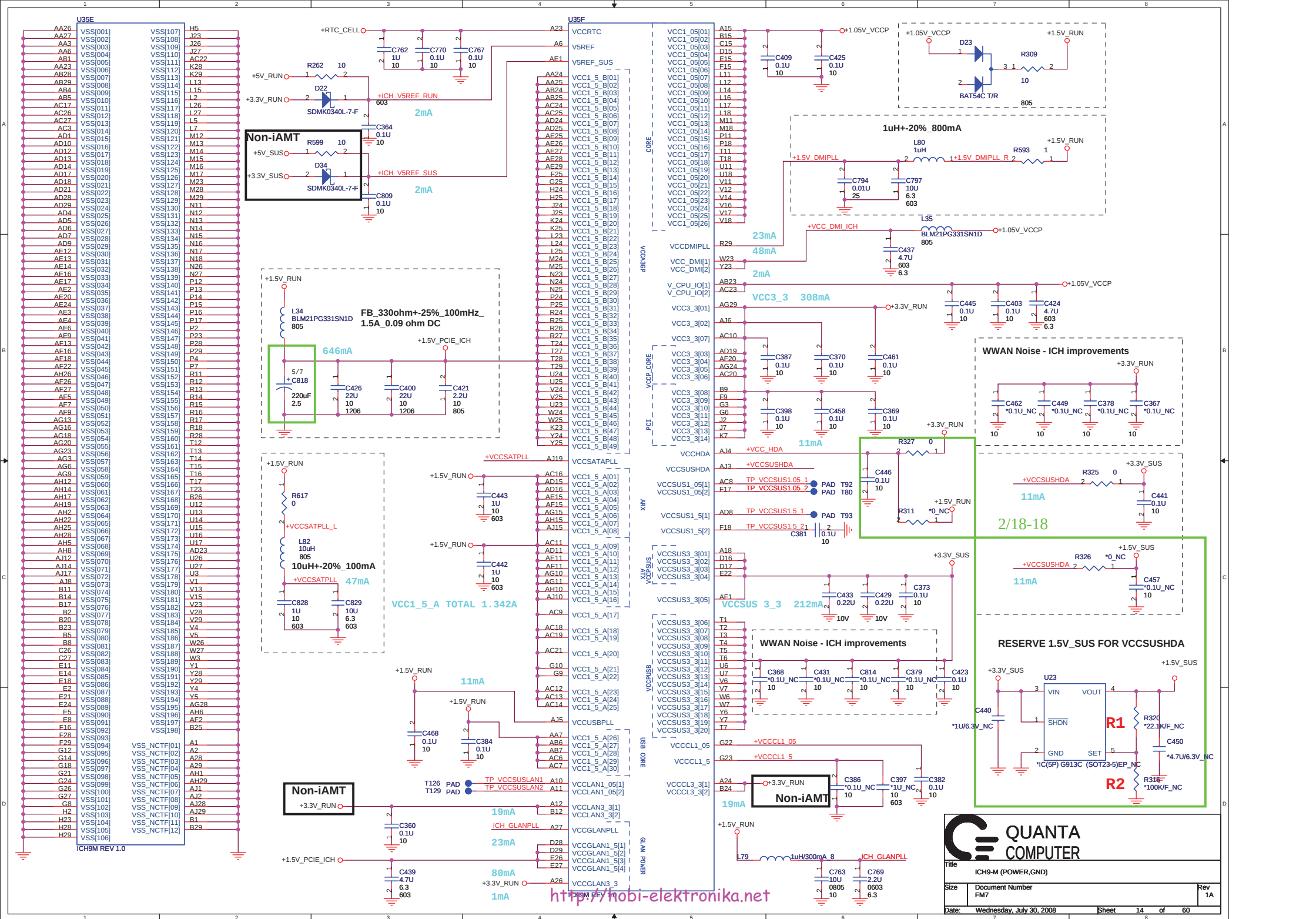
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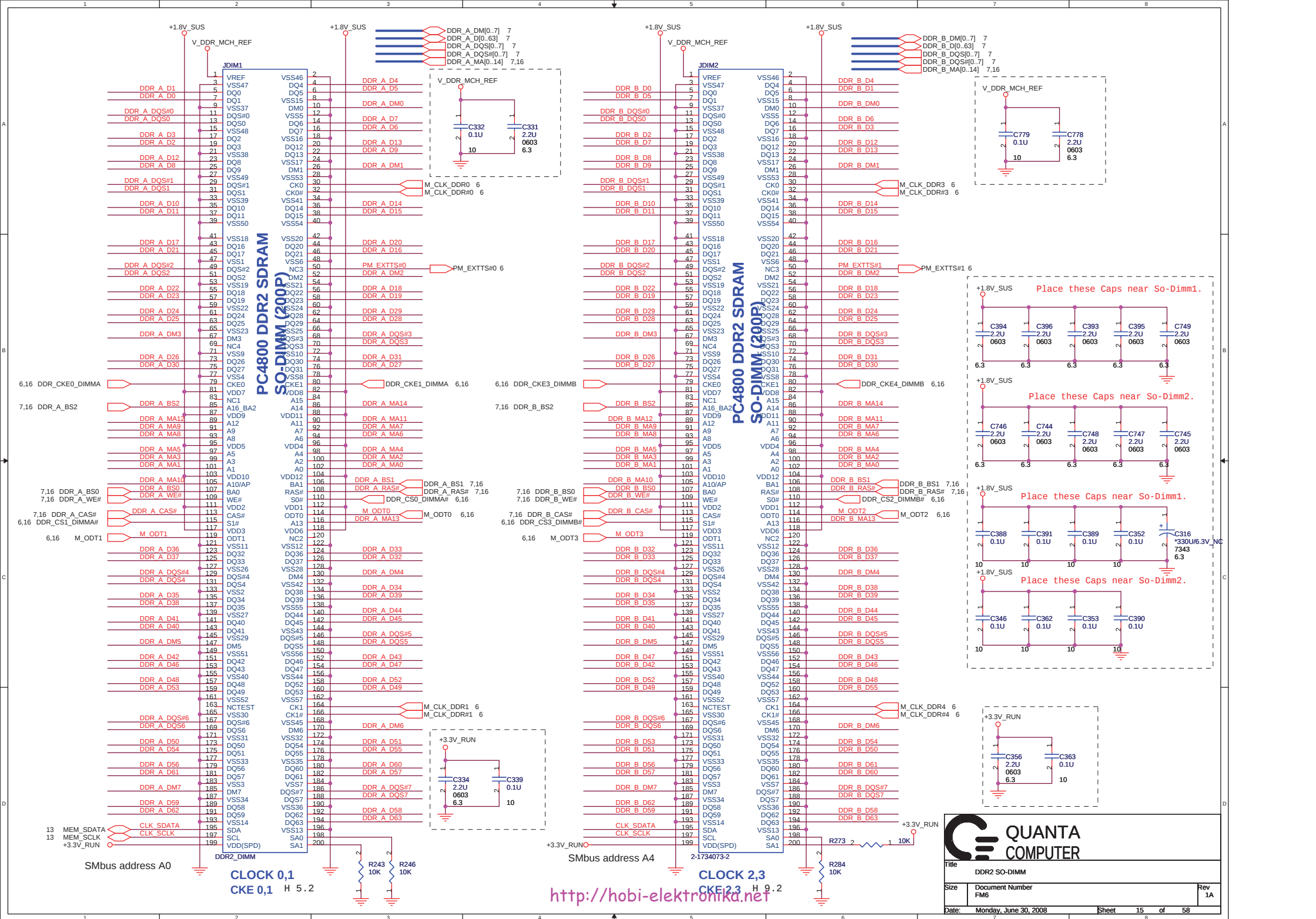
No Reboot strap.
SPKR Low = Default. High = No Reboot.

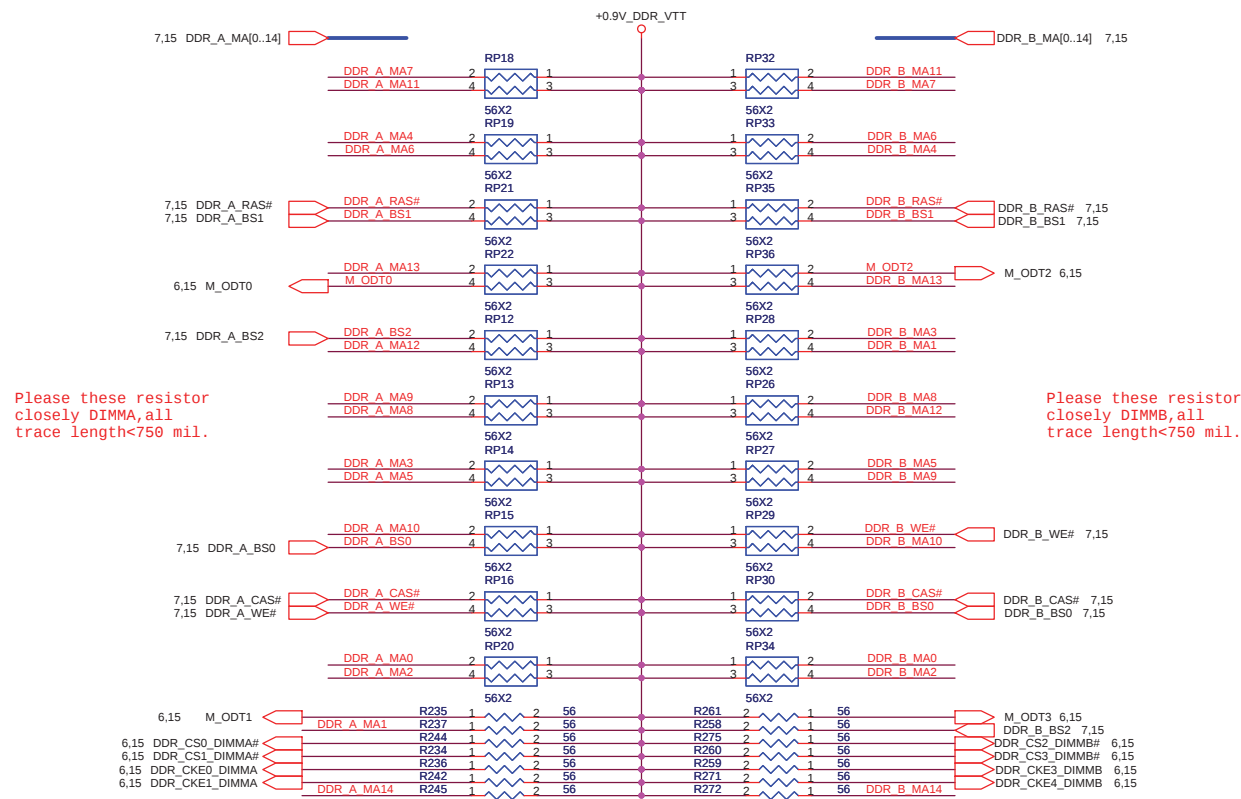
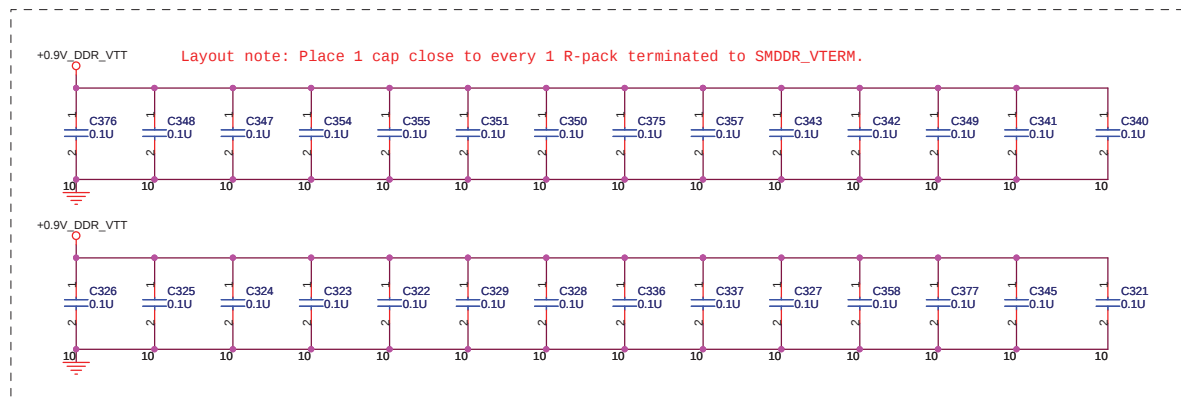


Title		ICH9-M (PM,GPIO,SMB,CL)
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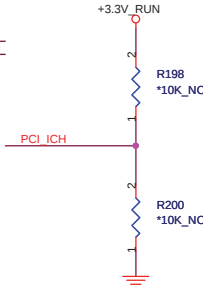
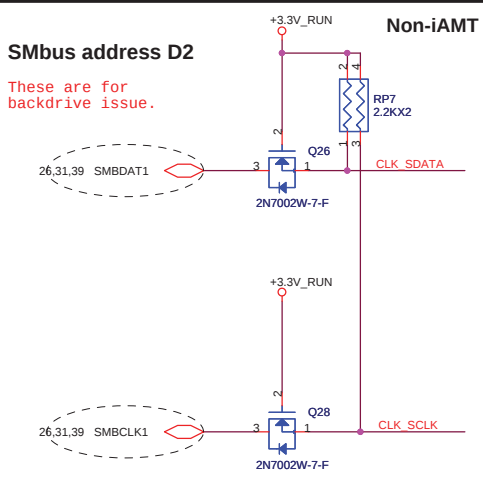
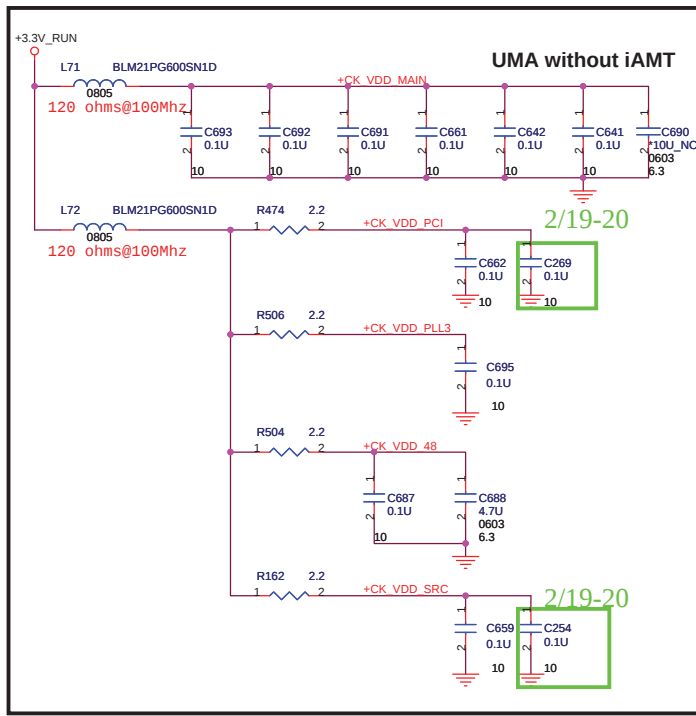
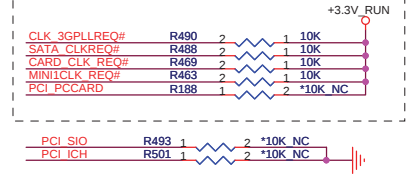
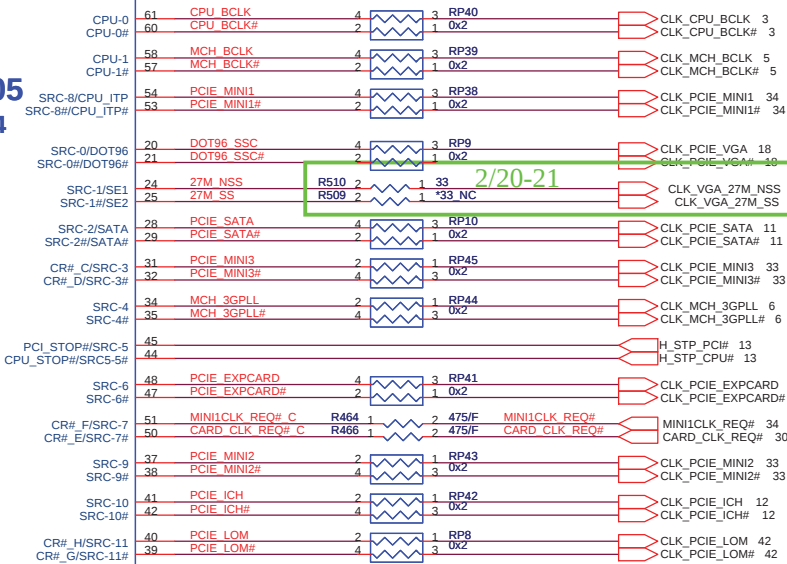
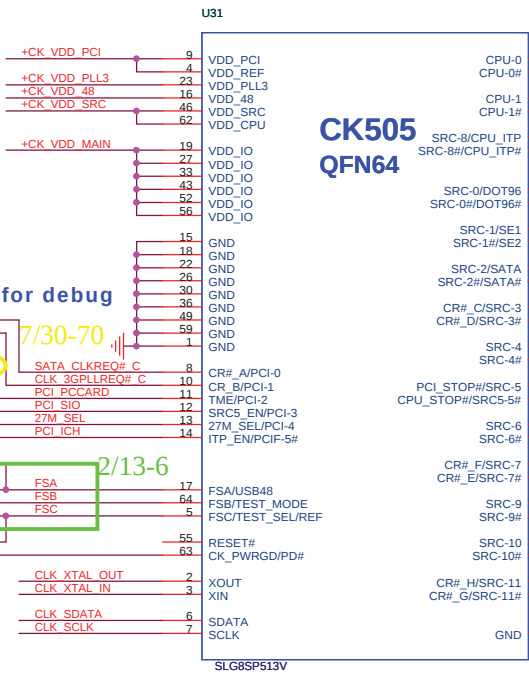
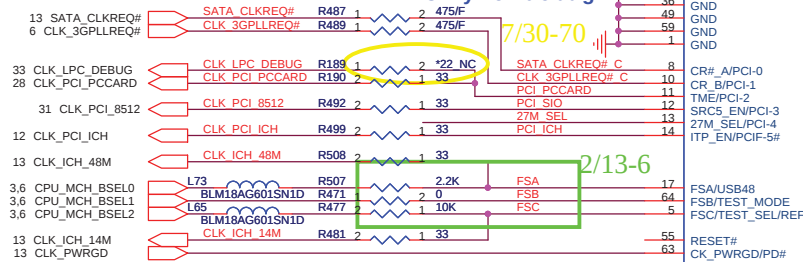
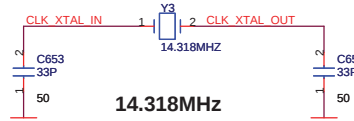
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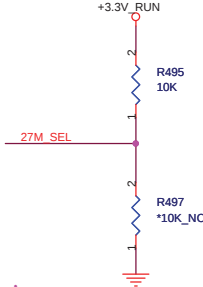




C694		20P	50	CLK ICH 48M
C666	1	2 *27P NC	50	CLK ICH 14M
C679	1	2 *27P NC	50	CLK PCI 8512
C272	1	2 *27P NC	50	CLK PCI PCCARD
C689	1	2 *27P NC	50	CLK PCI ICH



R188 POP: For Internal pull-low.
R191 POP: For internal pull-high



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M_SEL	PIN20	PIN21	PIN24	PIN25
27M_SEL (PIN13)				
0=UMA	DOT96T	DOT96C	96/ 100M_T	96/ 100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout



Title	CLOCK GENERATOR
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Size

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6 PCIE_MTX_GRX_P[0..15]
6 PCIE_MTX_GRX_N[0..15]

U27A

PART 1 OF 6

P C I E
-
E X P R E S S
I
N
T
E
R
F
A
C
E

PCIE_MTX_GRX_P0 AC30
PCIE_MTX_GRX_N0 AC31
PCIE_MTX_GRX_P1 AC29
PCIE_MTX_GRX_N1 AB29
PCIE_MTX_GRX_P2 AB31
PCIE_MTX_GRX_N2 AB30
PCIE_MTX_GRX_P3 AA31
PCIE_MTX_GRX_N3 AA30
PCIE_MTX_GRX_P4 W30
PCIE_MTX_GRX_N4 W31
PCIE_MTX_GRX_P5 W29
PCIE_MTX_GRX_N5 V29
PCIE_MTX_GRX_P6 V31
PCIE_MTX_GRX_N6 V30
PCIE_MTX_GRX_P7 U31
PCIE_MTX_GRX_N7 U30
PCIE_MTX_GRX_P8 P30
PCIE_MTX_GRX_N8 P31
PCIE_MTX_GRX_P9 P29
PCIE_MTX_GRX_N9 N29
PCIE_MTX_GRX_P10 N31
PCIE_MTX_GRX_N10 N30
PCIE_MTX_GRX_P11 M31
PCIE_MTX_GRX_N11 M30
PCIE_MTX_GRX_P12 K30
PCIE_MTX_GRX_N12 K31
PCIE_MTX_GRX_P13 K29
PCIE_MTX_GRX_N13 J29
PCIE_MTX_GRX_P14 J31
PCIE_MTX_GRX_N14 J30
PCIE_MTX_GRX_P15 H31
PCIE_MTX_GRX_N15 H30

Clock
PCIE_REFCLKP
PCIE_REFCLKN
SMBUS
NC_SMBCLK
NC_SMBDATA
PERSTB

Calibration

PCIE_CALRN
PCIE_CALRP

NC_1
NC_2

M82-S

PCIE_TX0P AA28
PCIE_TX0N AA27
PCIE_TX1P AA25
PCIE_TX1N AA24
PCIE_TX2P Y28
PCIE_TX2N Y27
PCIE_TX3P Y25
PCIE_TX3N Y24
PCIE_TX4P V28
PCIE_TX4N V27
PCIE_TX5P V25
PCIE_TX5N V24
PCIE_TX6P T28
PCIE_TX6N T27
PCIE_TX7P T25
PCIE_TX7N T24
PCIE_TX8P P28
PCIE_TX8N P27
PCIE_TX9P P25
PCIE_TX9N P24
PCIE_TX10P M28
PCIE_TX10N M27
PCIE_TX11P M25
PCIE_TX11N M24
PCIE_TX12P L28
PCIE_TX12N L27
PCIE_TX13P L25
PCIE_TX13N L24
PCIE_TX14P J28
PCIE_TX14N J27
PCIE_TX15P G28
PCIE_TX15N G27

R45 2K/F
PCIE_VDDC

R58 1.27K/F

6 PCIE_MRX_GTX_P[0..15]
6 PCIE_MRX_GTX_N[0..15]

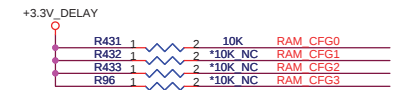
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PCIE_MRX_GTX_P3 0.1U 2
PCIE_MRX_GTX_P4 0.1U 2
PCIE_MRX_GTX_P5 0.1U 2
PCIE_MRX_GTX_P6 0.1U 2
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PCIE_MRX_GTX_P12 0.1U 2
PCIE_MRX_GTX_P13 0.1U 2
PCIE_MRX_GTX_P14 0.1U 2
PCIE_MRX_GTX_P15 0.1U 2

PCIE_MRX_GTX_N0 0.1U 2
PCIE_MRX_GTX_N1 0.1U 2
PCIE_MRX_GTX_N2 0.1U 2
PCIE_MRX_GTX_N3 0.1U 2
PCIE_MRX_GTX_N4 0.1U 2
PCIE_MRX_GTX_N5 0.1U 2
PCIE_MRX_GTX_N6 0.1U 2
PCIE_MRX_GTX_N7 0.1U 2
PCIE_MRX_GTX_N8 0.1U 2
PCIE_MRX_GTX_N9 0.1U 2
PCIE_MRX_GTX_N10 0.1U 2
PCIE_MRX_GTX_N11 0.1U 2
PCIE_MRX_GTX_N12 0.1U 2
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PCIE_MRX_GTX_N14 0.1U 2
PCIE_MRX_GTX_N15 0.1U 2

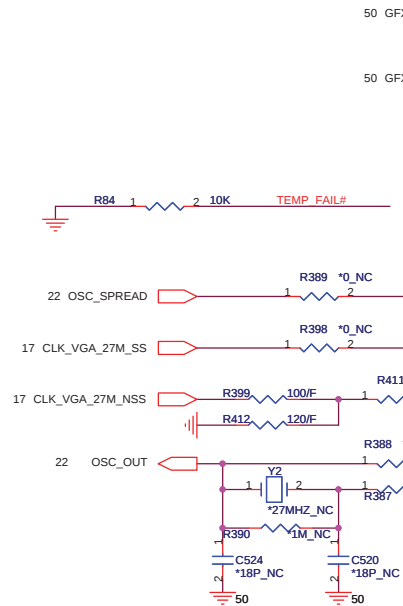
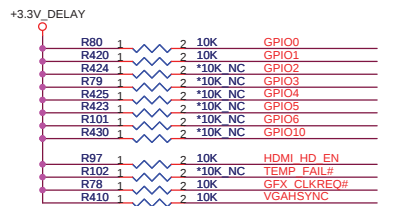


Title VGA-M82-S (PCie)		
Size	Document Number FM7	Rev 1A
Date:	Wednesday, July 30, 2008	Sheet 18 of 58

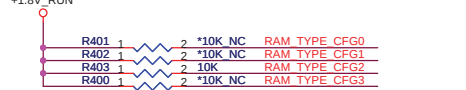
MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	X	0	0	0
256MB	X	0	0	1
64MB	X	0	1	0
512MB	X	1	0	0



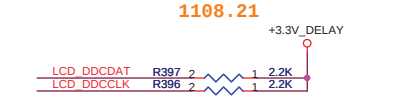
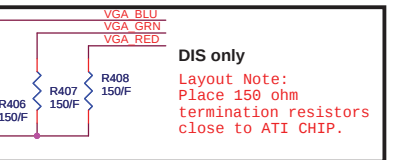
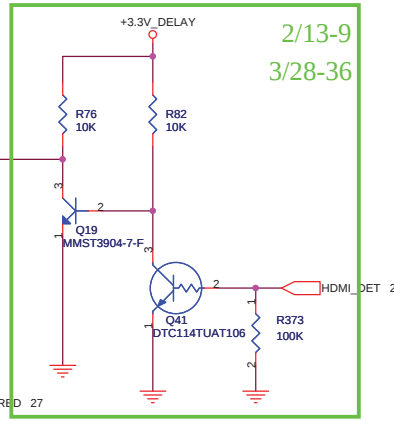
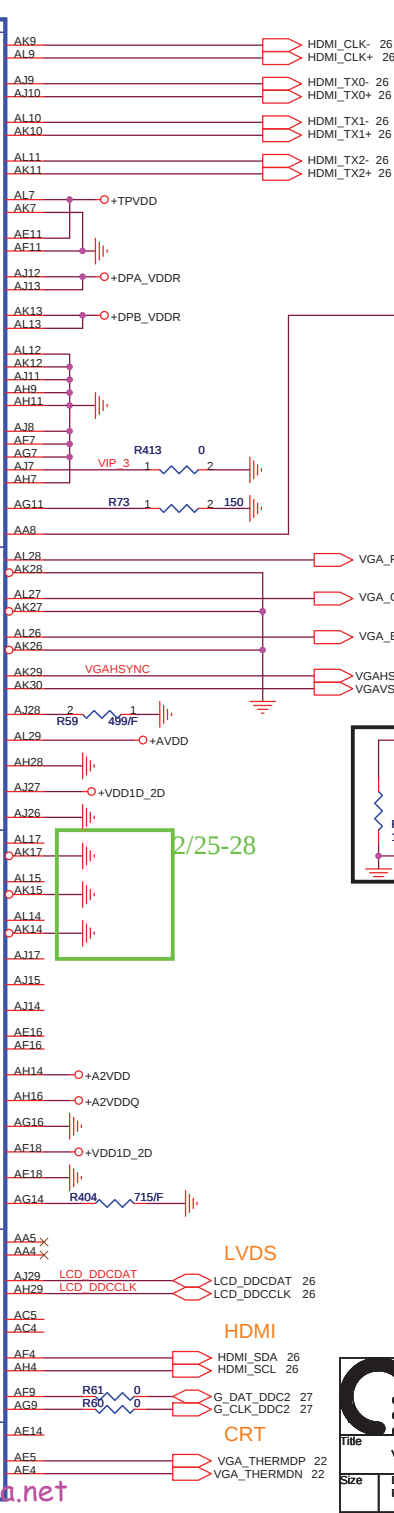
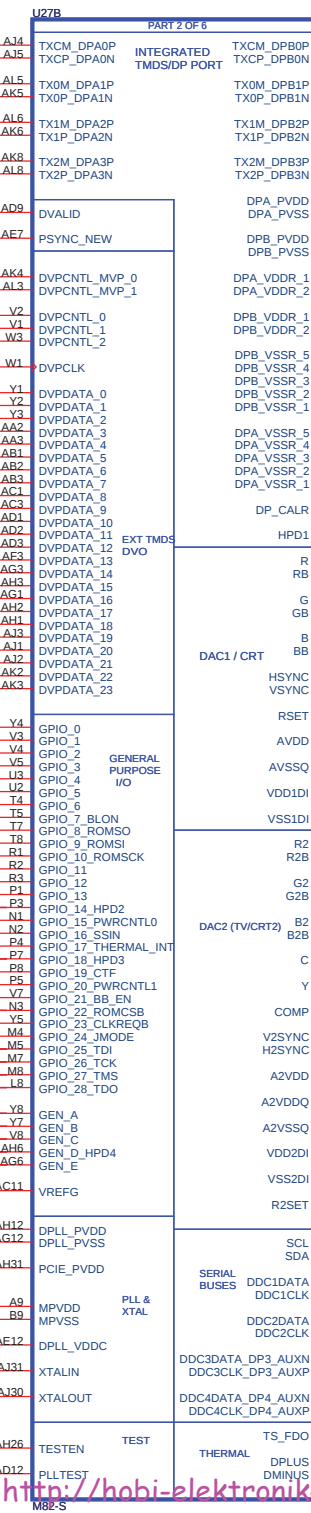
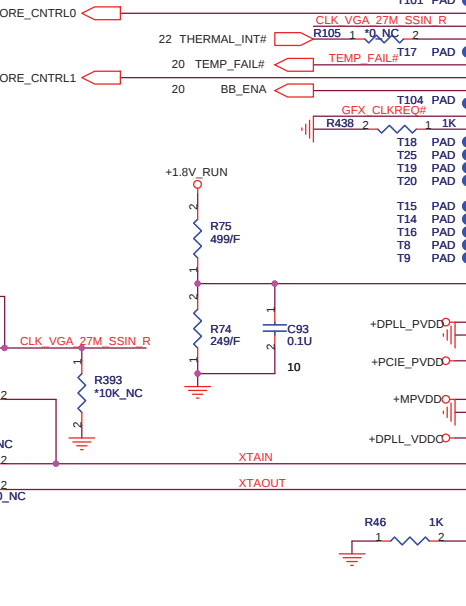
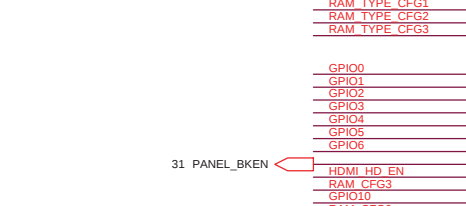
GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	ATI Usage	FM6 Usage
GPIO0	PCIe FULL TX OUTPUT SWING	X	1
GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED	X	1
GPIO2	ATI reserved configuration straps.	RSVD	0
GPIO3	ATI reserved configuration straps.	RSVD	0
GPIO4	DEBUG SIGNALS MUXED OUT	0	0
GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
GPIO6	ATI Internal use only	0	0
GPIO10	Serial ROM clock to ROM.	0	0



Memory Straps	RAM_TYPE_CFG3	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0
400MHz 256MB(32M*16) Samsung	0	0	1	0
400MHz 256MB(32M*16) Hynix	0	0	1	1
500MHz 256MB(32M*16) Samsung	0	1	1	0
500MHz 256MB(32M*16) Qimonda	0	1	0	0



ATI Usage	FM6 Usage
0= DO NOT INSTALL RESISTOR, X = DESIGN DEPENDANT, RSVD = ATI RESERVED (DO NOT INSTALL)	



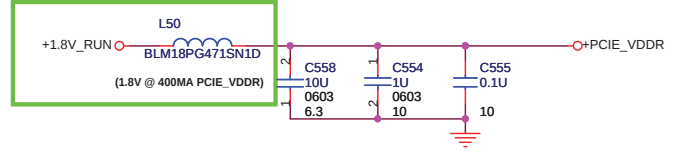
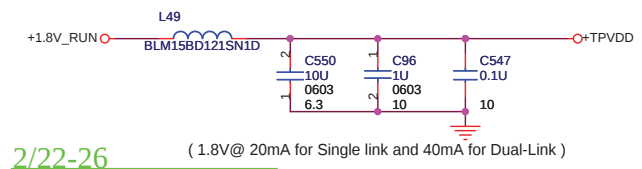
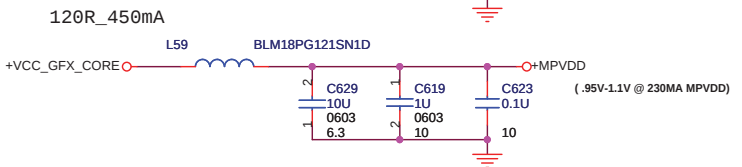
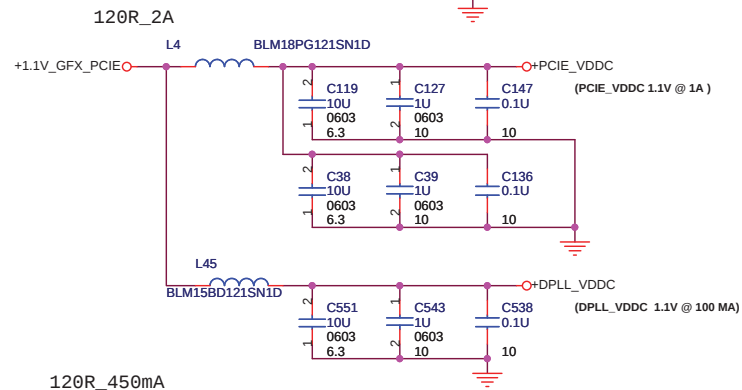
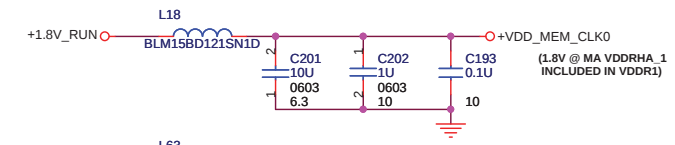
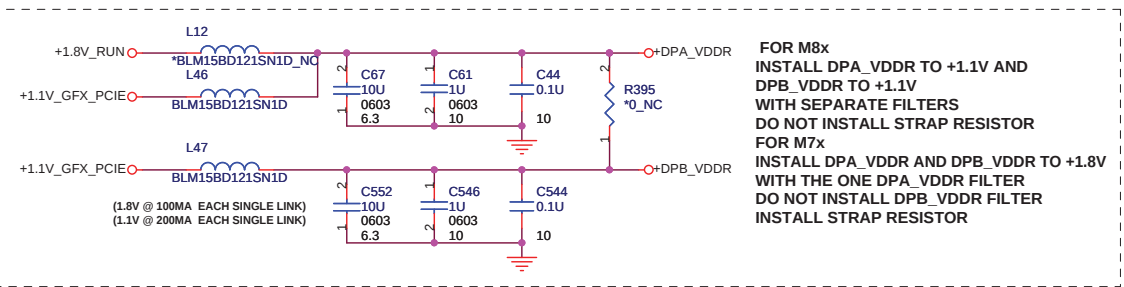
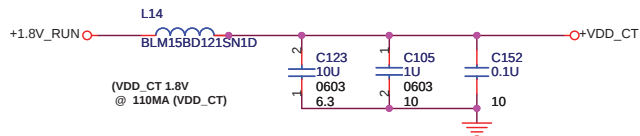
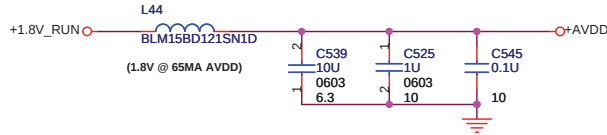
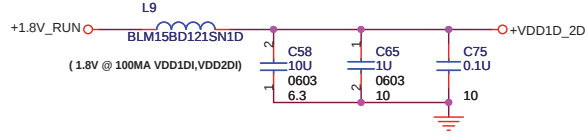
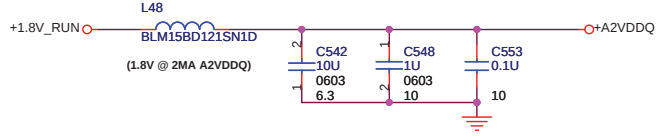
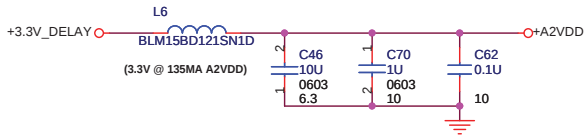
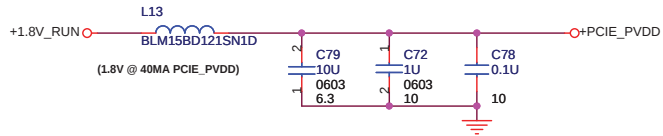
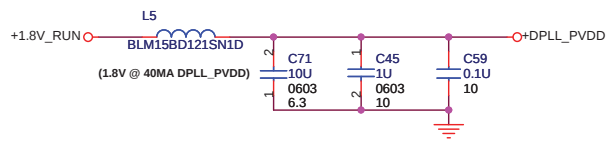
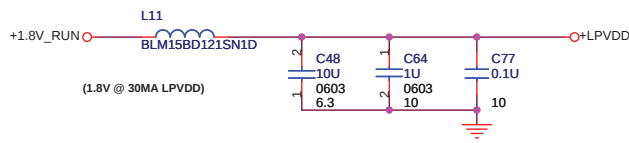
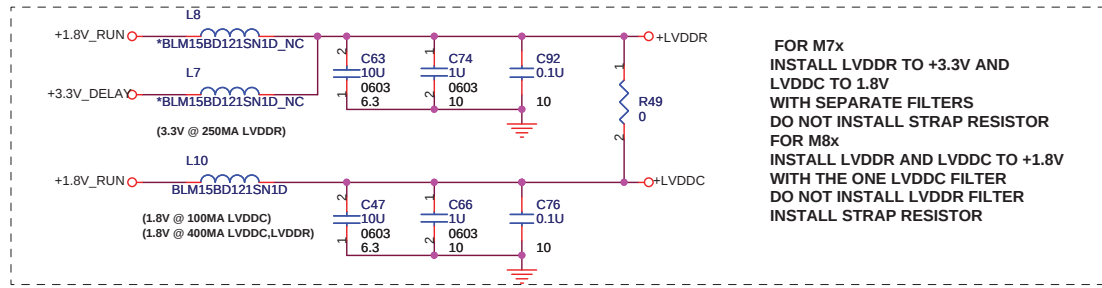
QUANTA
COMPUTER

Title: VGA-G86GLM (VIDEO)

Size: Document Number FM6 Rev 2A

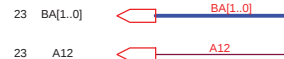
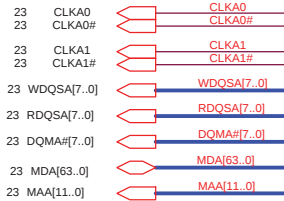
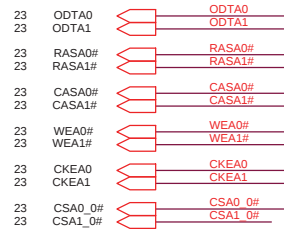
Date: Monday, June 30, 2008 Sheet 19 of 58

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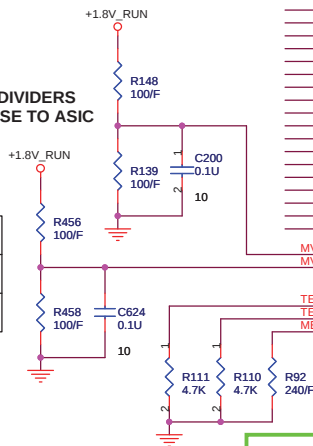


PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE

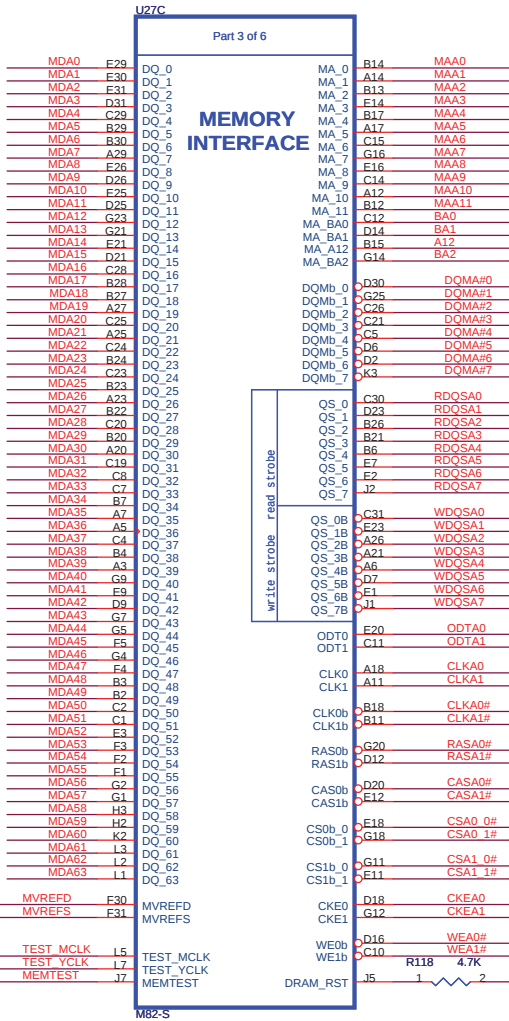
Title		
VGA-M82-S (PCIe)		
Size		
Document Number		Rev
FM6		1A
Date: Monday, June 30, 2008		
Sheet		21 of 58



PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC



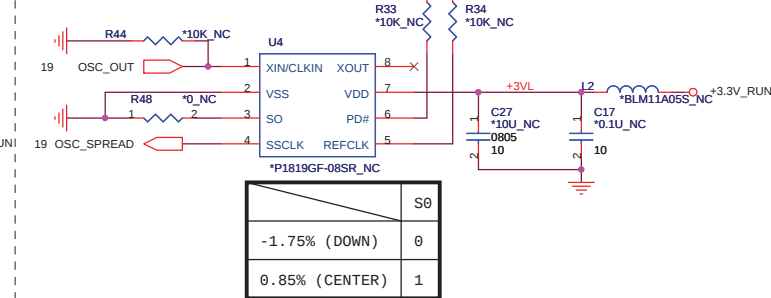
DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



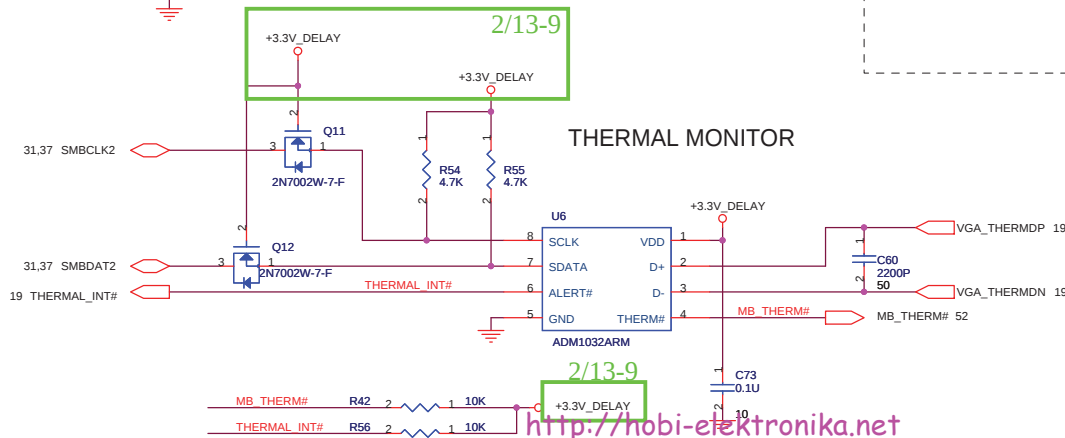
Remove MEM_RST

Spread Spectrum

If U4, the discrete spread spectrum chip is not used, then pop R48 in order to pull-down BXTALOUT for EMI reasons.



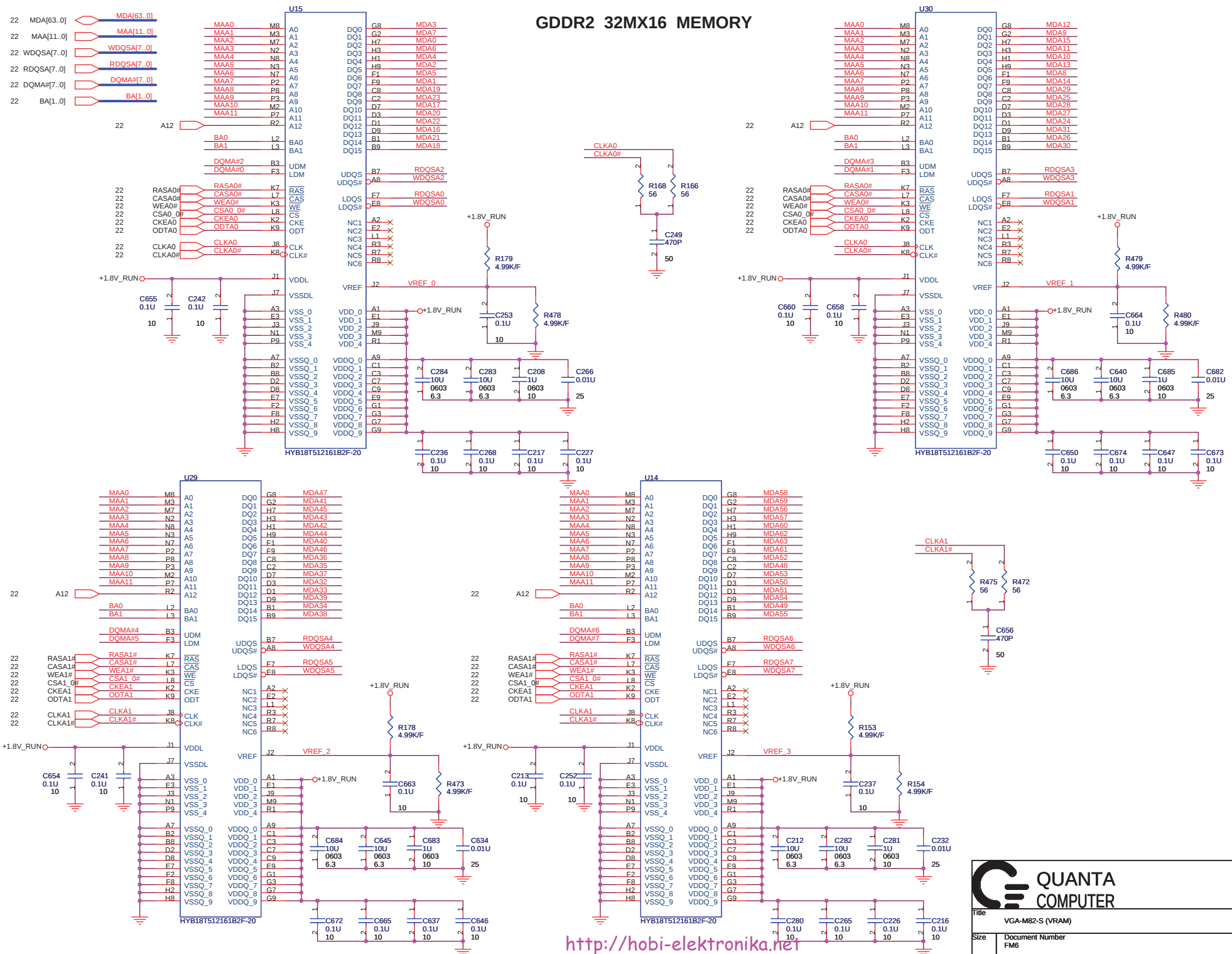
THERMAL MONITOR



Title		
VGA-M82-S (PCIe)		
Size	Document Number	Rev
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GDDR2 32MX16 MEMORY



GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	ATI Usage	FM6 Usage
GPIO0	PCIE FULL TX OUTPUT SWING	X	1
GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	1
GPIO2	ATI reserved configuration straps.	RSVD	0
GPIO3	ATI reserved configuration straps.	RSVD	0
GPIO4	DEBUG SIGNALS MUXED OUT	0	0
GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
GPIO6	ATI Internal use only	0	0
GPIO10	Serial ROM clock to ROM.		0
ATI Usage recommended settings		0= DO NOT INSTALL RESISTOR, X = DESIGN DEPENDANT, RSVD = ATI RESERVED (DO NOT INSTALL)	

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 QUANTA COMPUTER			
Title: VGA-M82-S (PCIe)			
Size	Document Number FM6		Rev 1A
Date:	Monday, June 30, 2008	Sheet	24 of 58

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Title

VGA-M82-S (PCIe)

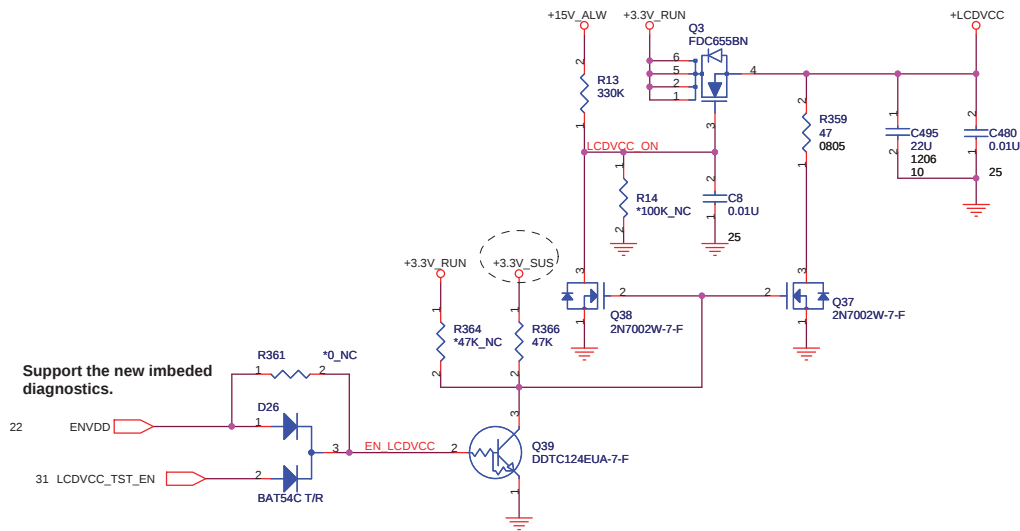
Size

Document Number FM6

Rev	1
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Date: Monday, June 30, 2008

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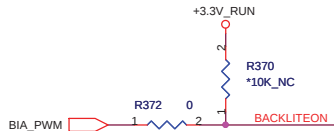


Support the new imbedded diagnostics.

UMA

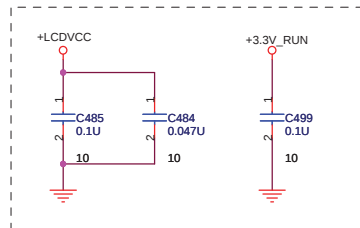
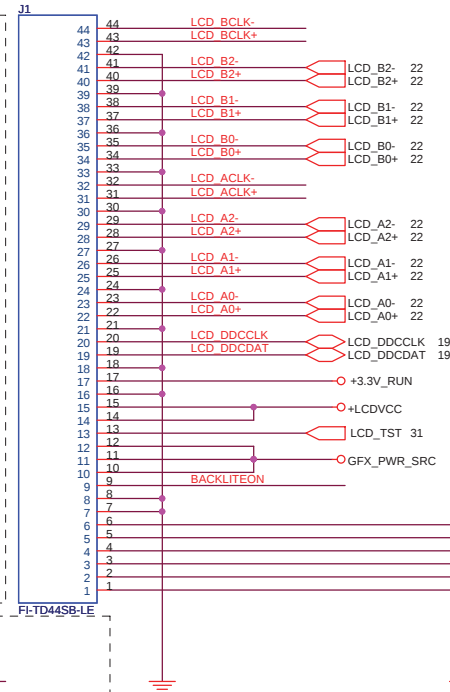
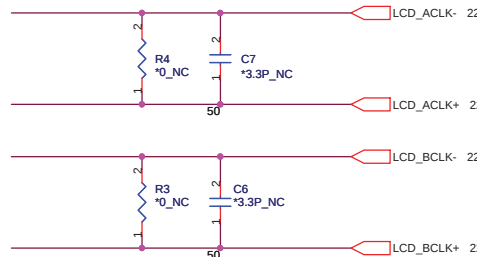
Populate R355 for DPST implementation only.

Populate R353 for platform without DPST support. No Stuff for Discrete DPST support due to back up plan.

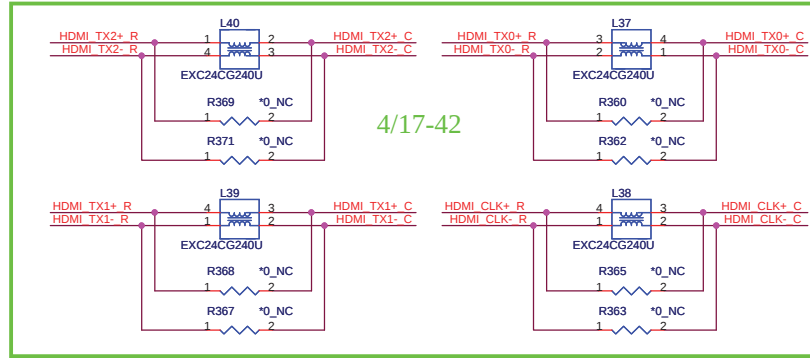


Shunt capacitors on LVDS for improving WWAN.

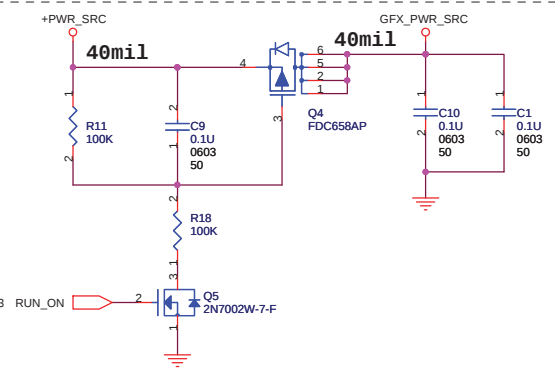
LCD_B0-	C490	1	2	*3.3P	NC	50	LCD_B0+
LCD_B1-	C493	1	2	*3.3P	NC	50	LCD_B1+
LCD_B2-	C489	1	2	*3.3P	NC	50	LCD_B2+
LCD_A0-	C3	1	2	*3.3P	NC	50	LCD_A0+
LCD_A1-	C483	1	2	*3.3P	NC	50	LCD_A1+
LCD_A2-	C2	1	2	*3.3P	NC	50	LCD_A2+



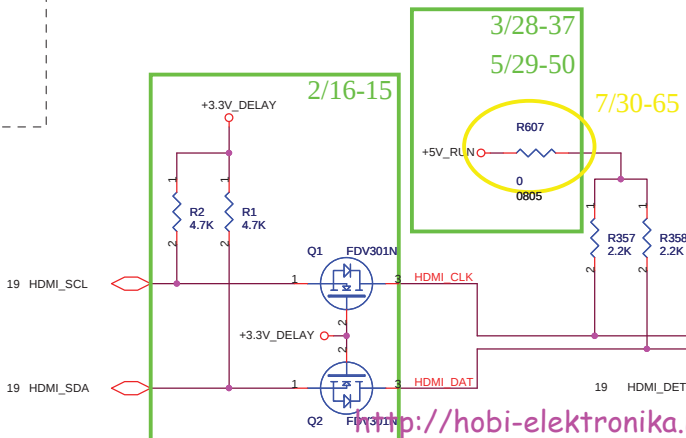
Address : A9H --Contrast
AAH --Backlight



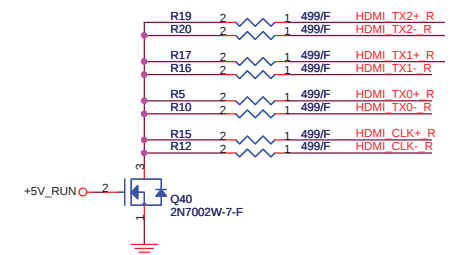
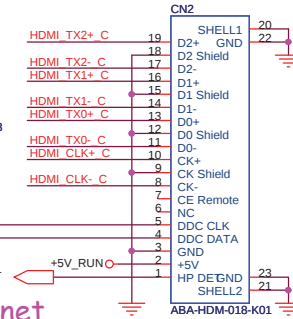
4/17-42



HDMI_TX2+	C502	0.1U/10V/X7R	HDMI_TX2+ R
HDMI_TX2-	C503	0.1U/10V/X7R	HDMI_TX2- R
HDMI_TX1+	C501	0.1U/10V/X7R	HDMI_TX1+ R
HDMI_TX1-	C500	0.1U/10V/X7R	HDMI_TX1- R
HDMI_TX0+	C491	0.1U/10V/X7R	HDMI_TX0+ R
HDMI_TX0-	C494	0.1U/10V/X7R	HDMI_TX0- R
HDMI_CLK+	C498	0.1U/10V/X7R	HDMI_CLK+ R
HDMI_CLK-	C497	0.1U/10V/X7R	HDMI_CLK- R



HDMI



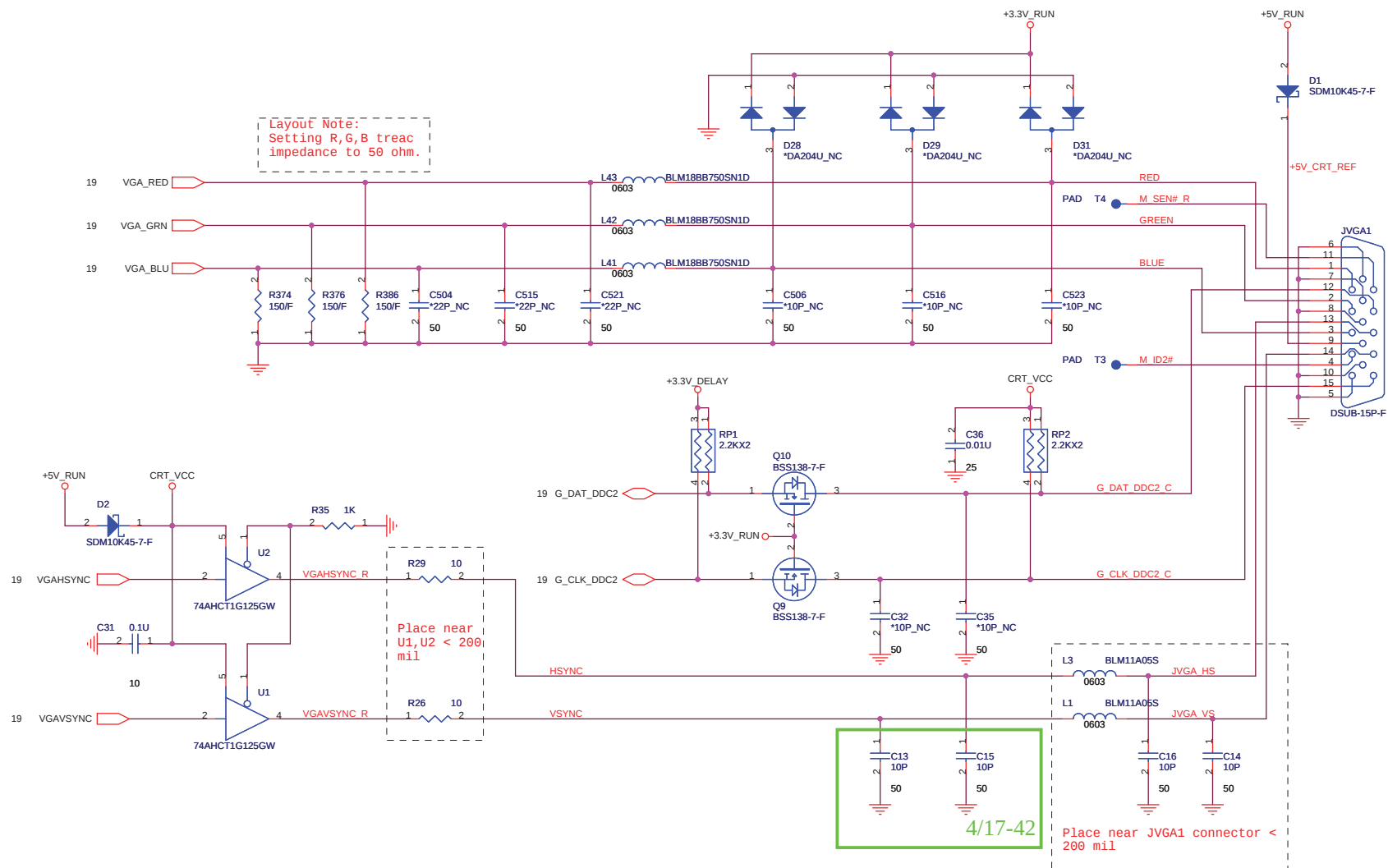
QUANTA COMPUTER

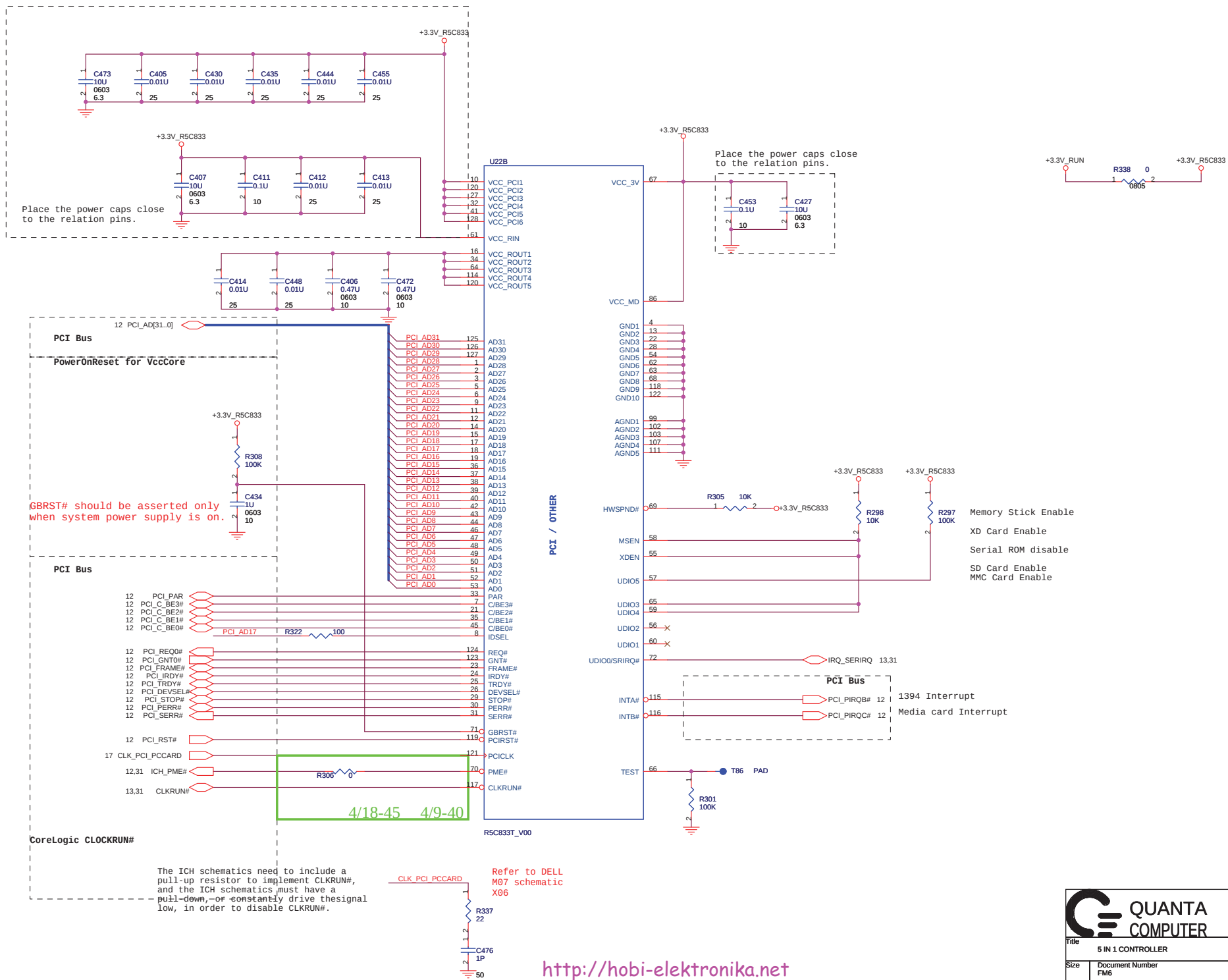
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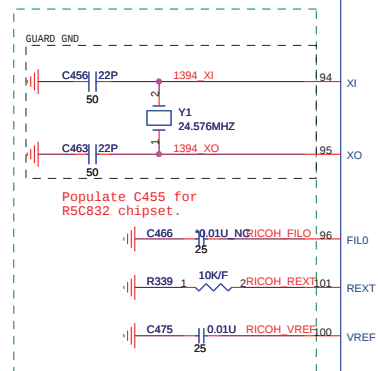
Size: Document Number FM6 Rev 2A

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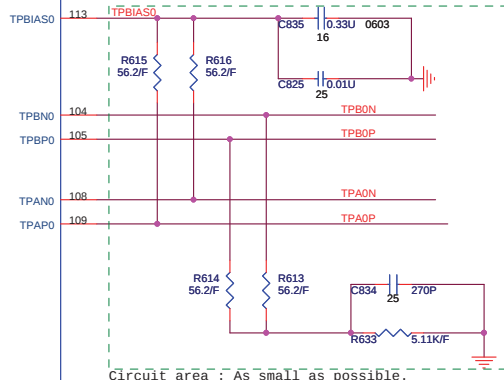
Populate C455 for R5C832 chipset.

80 mils

U22A
AVCC_PHY1
AVCC_PHY2
AVCC_PHY3
AVCC_PHY4

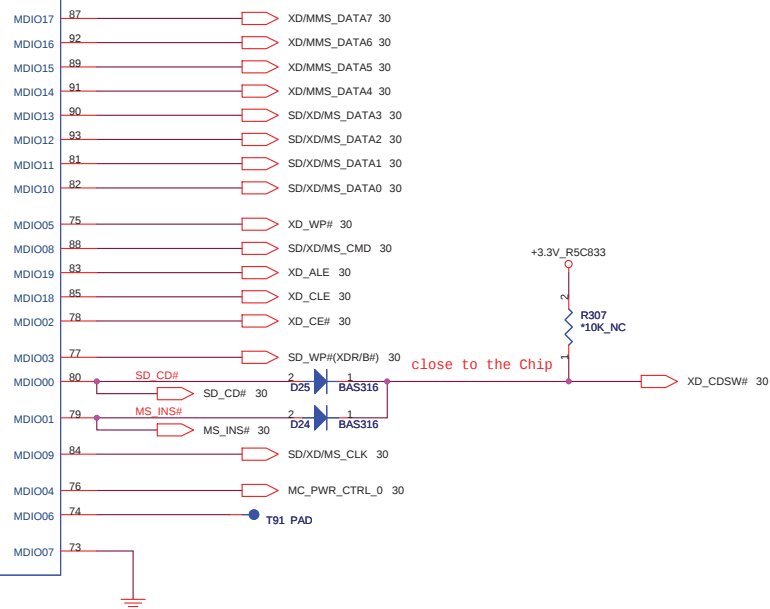
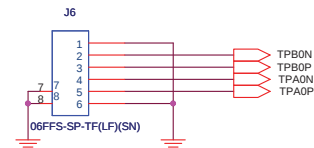
Place these caps as close to the R5C833 as possible.

AS CLOSE AS POSSIBLE TO R5C833



Circuit area : As small as possible.

*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).



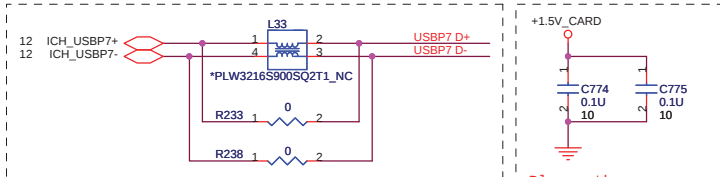
+3.3V_R5C833
R307
*10K_NC

close to the Chip

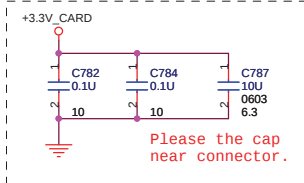


Title	IEEE 1394	Rev	2A
Size	Document Number FM6		
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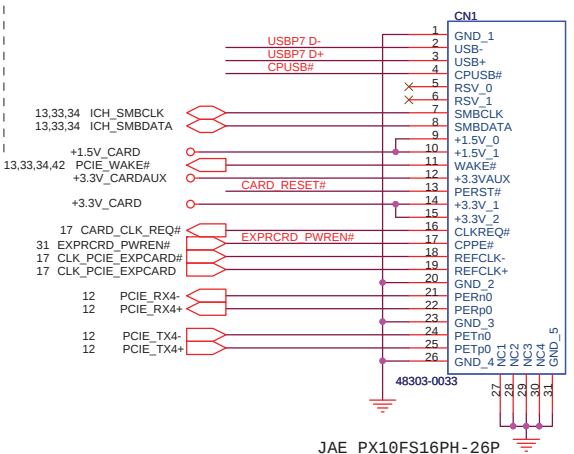
Express Card



Please the cap near connector.

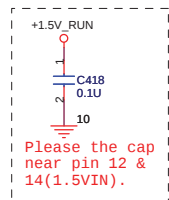
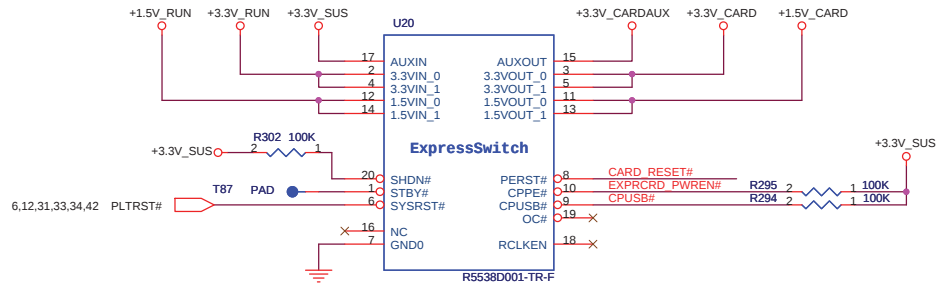


Please the cap near connector.

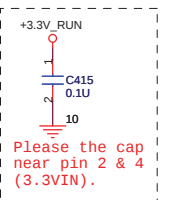


PCI-Express TX and RX direct to connector.

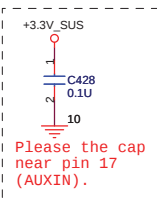
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



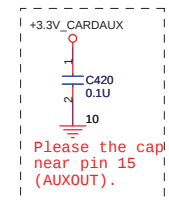
Please the cap near pin 12 & 14(1.5VIN).



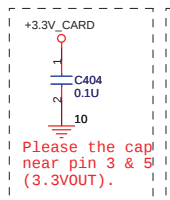
Please the cap near pin 2 & 4 (3.3VIN).



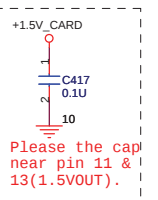
Please the cap near pin 17 (AUXIN).



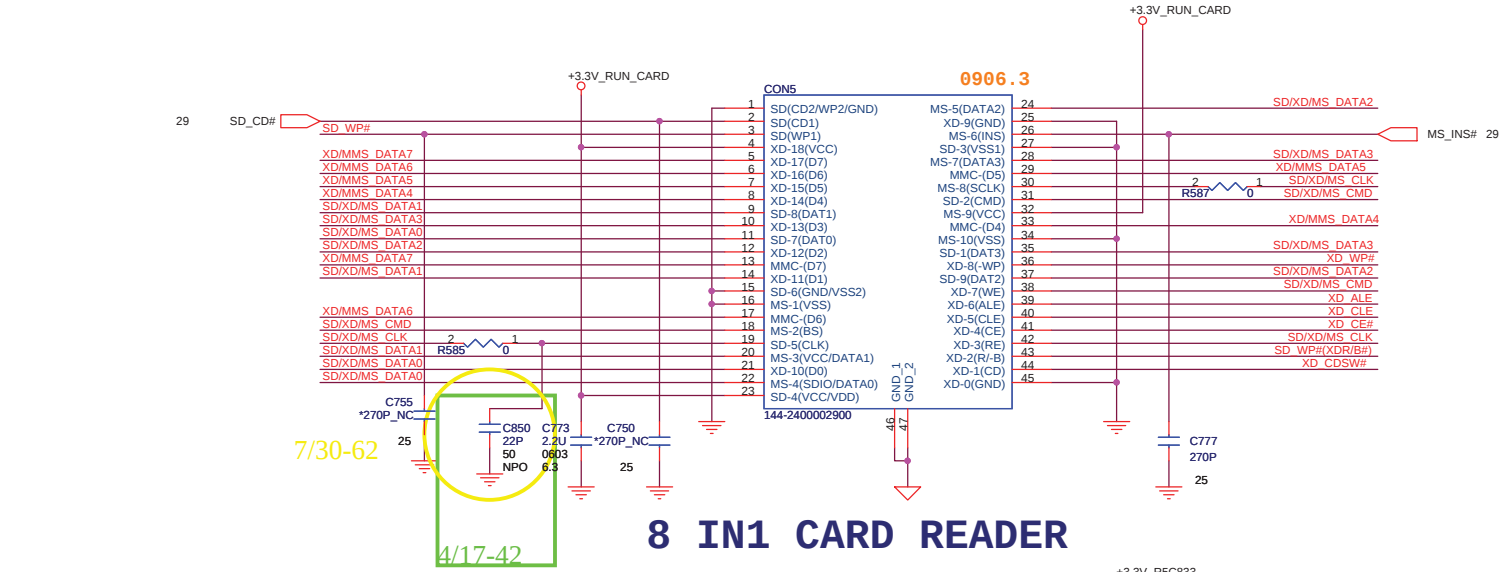
Please the cap near pin 15 (3.3VOUT).



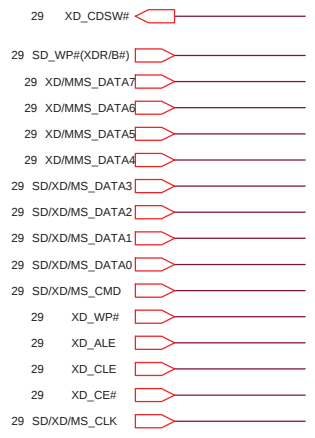
Please the cap near pin 3 & 5 (3.3VOUT).



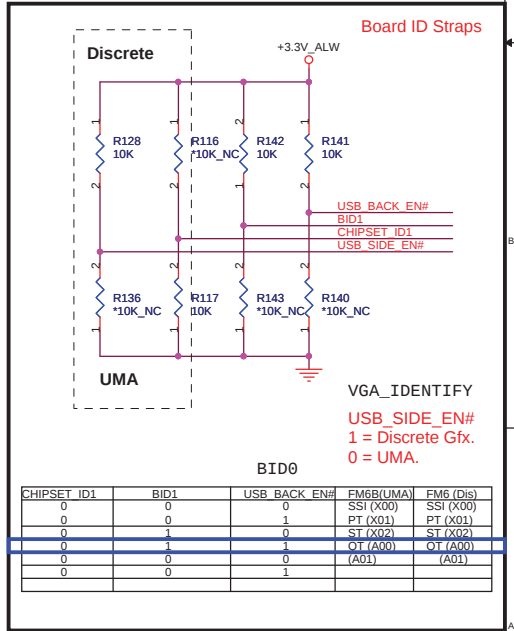
Please the cap near pin 11 & 13(1.5VOUT).



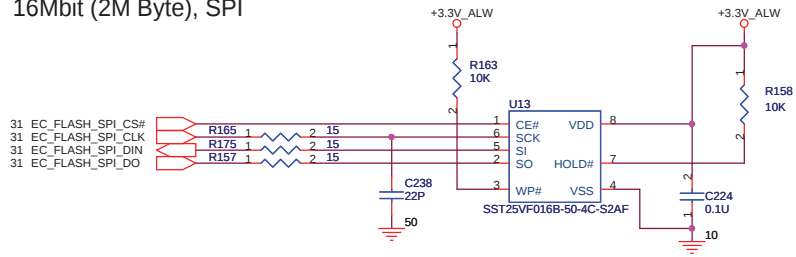
8 IN1 CARD READER



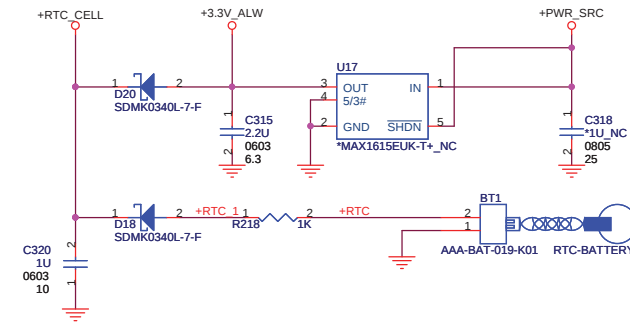
<http://hobi-elektronika.net>

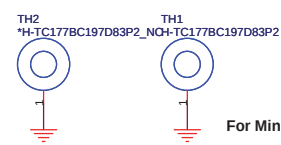


16Mbit (2M Byte), SPI



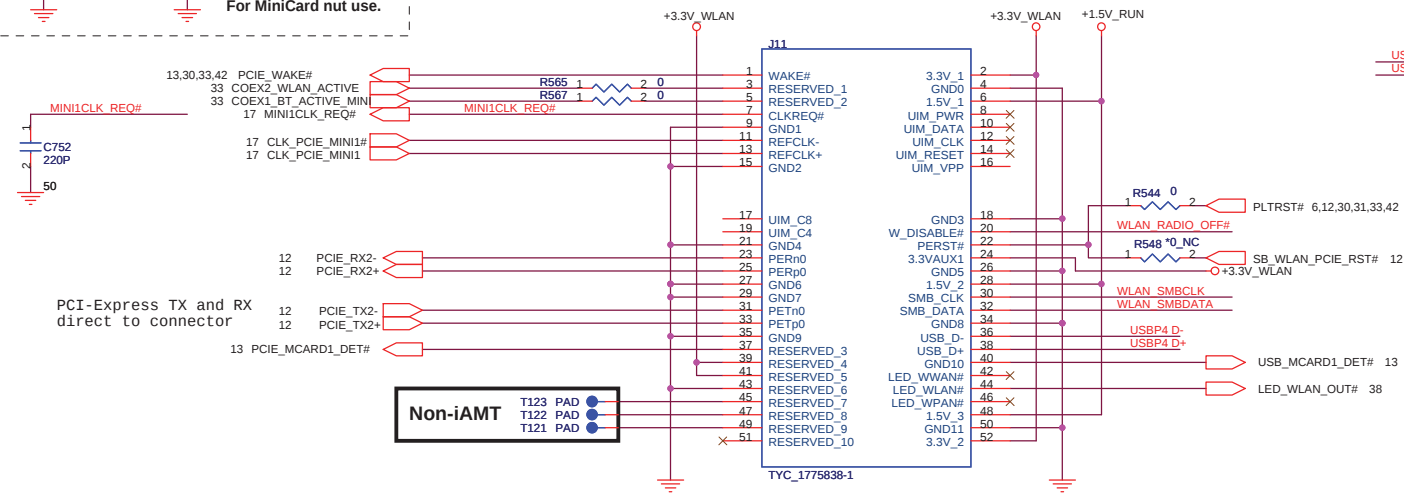
RTC BATTERY



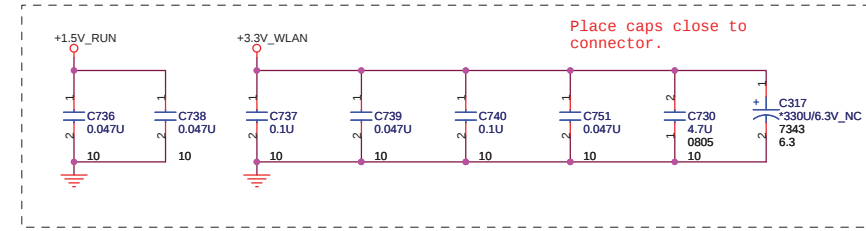
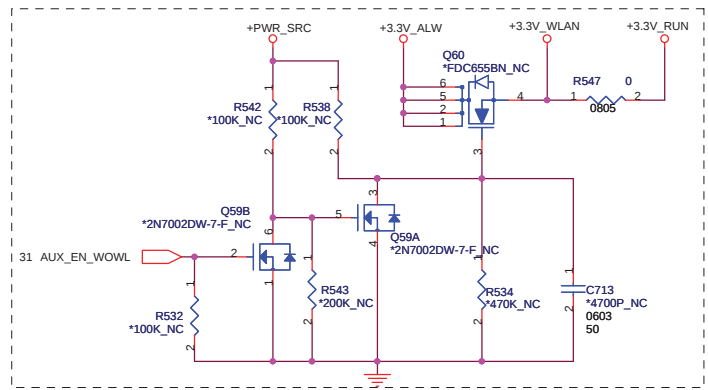
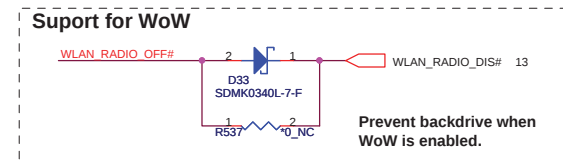
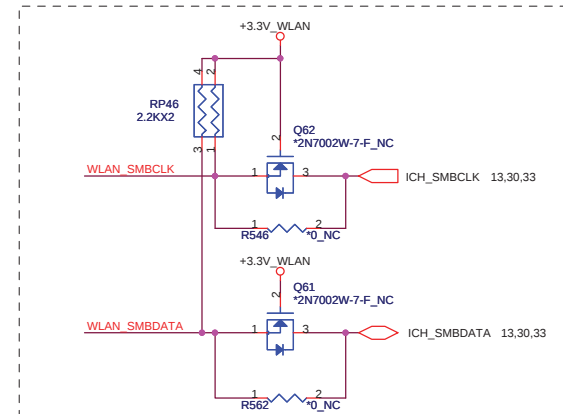
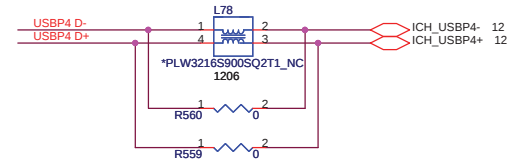


For MiniCard nut use.

MiniCard WLAN connector



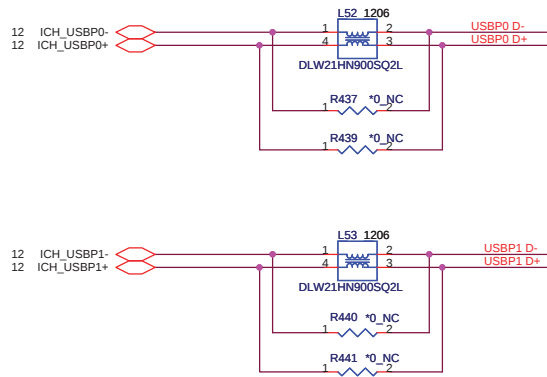
Non-iAMT
T123 PAD
T122 PAD
T121 PAD



QUANTA
COMPUTER

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External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

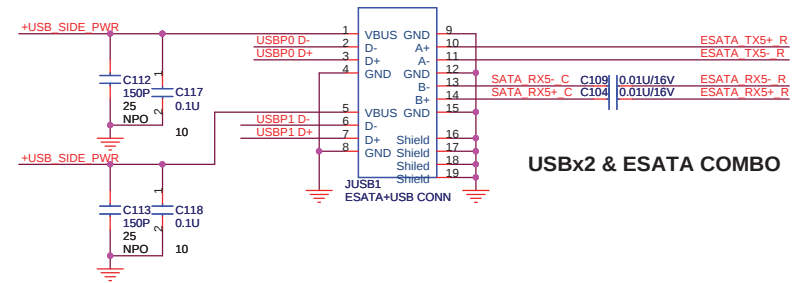


2/22-25
4/17-42

Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Side External USBX2

2/13-4

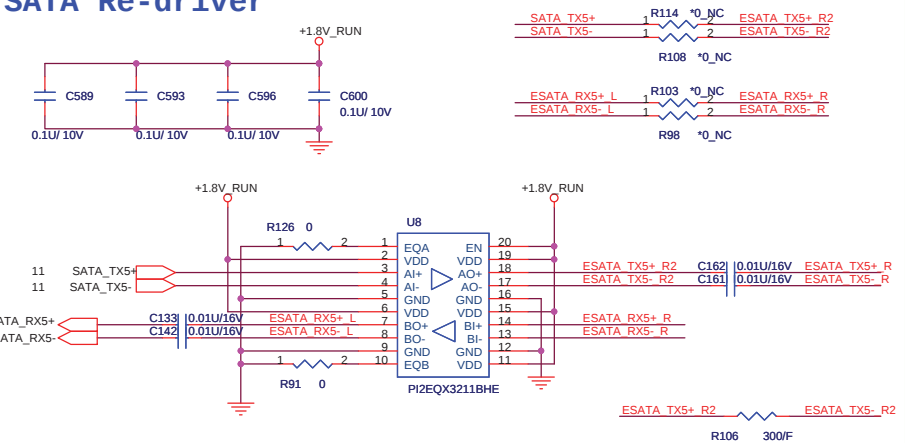


USBx2 & ESATA COMBO

5/29-52

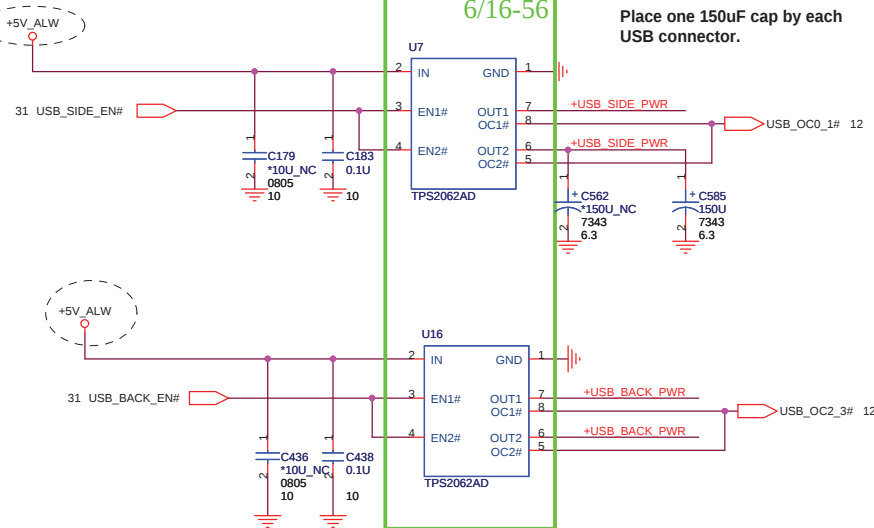
2/20-22

E-SATA Re-driver



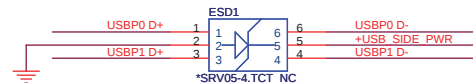
6/16-56

Place one 150uF cap by each USB connector.

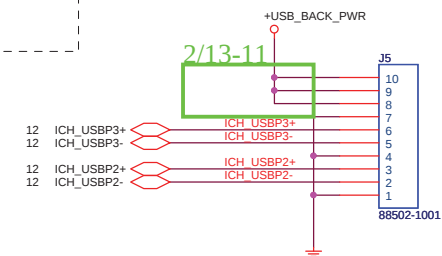


Each channel is 1A

Place ESD diodes as close as USB connector.



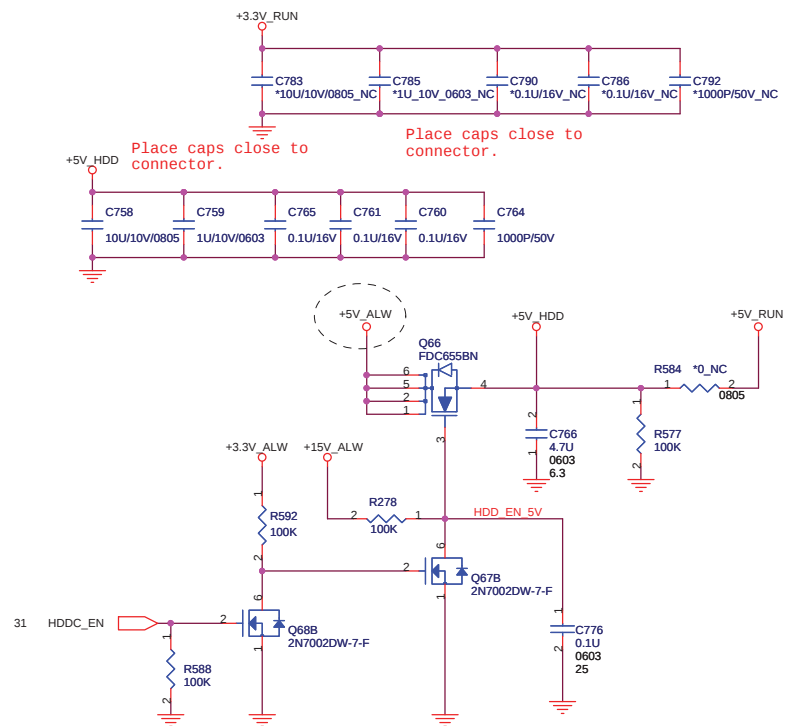
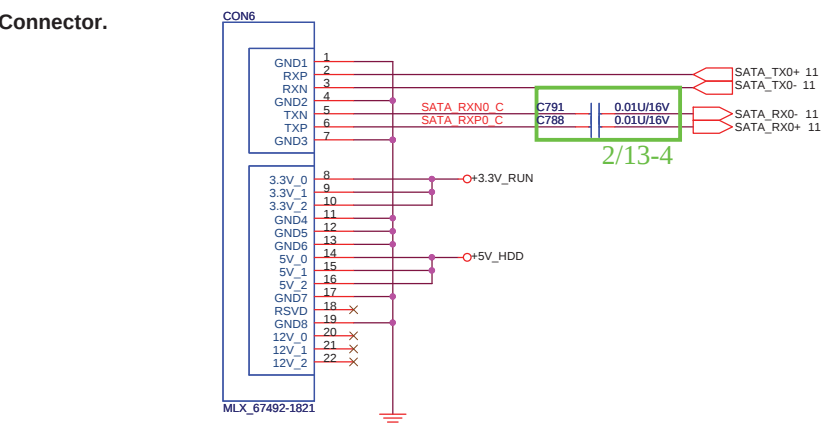
MB side



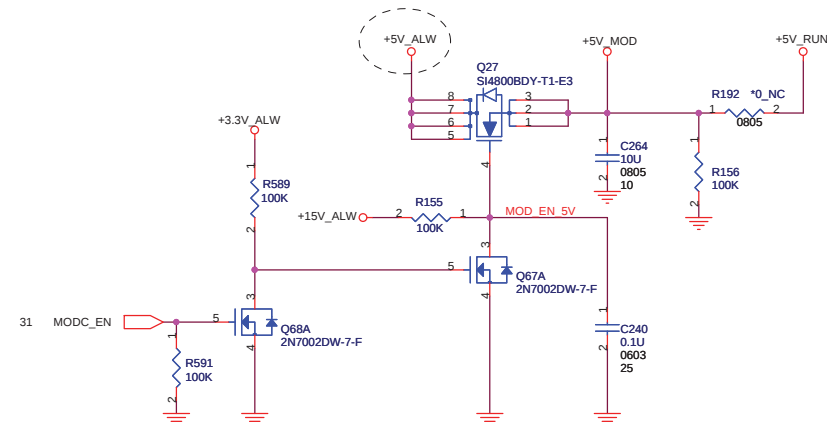
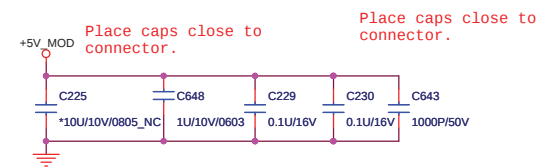
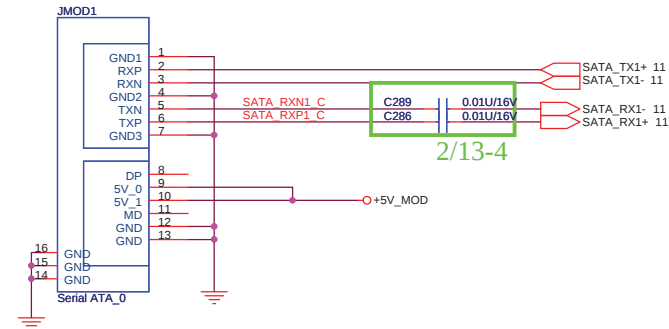
Title			SERIAL PORT & USB
Size	Document Number	Rev	
	FM6	3A	
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<http://hobi-elektronika.net>

SATA Connector.



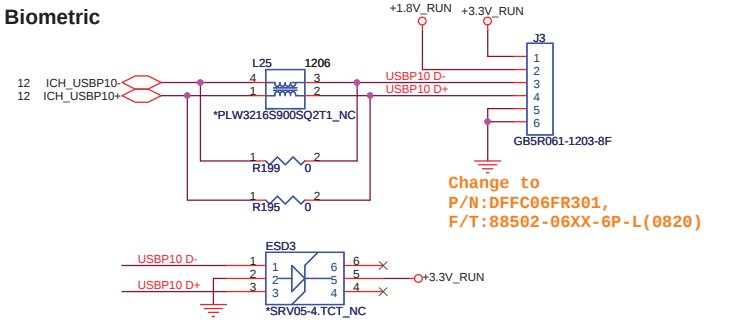
ODD Connector



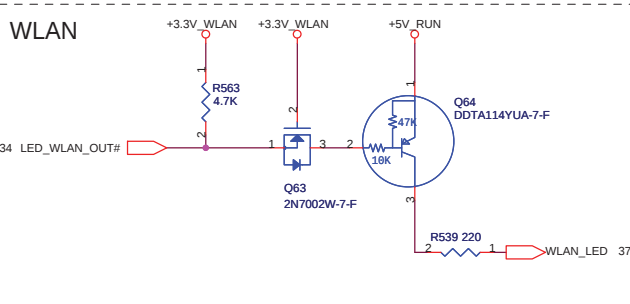
Title			SATA (HDD&CD_ROM)
Size	Document Number	Rev	
FM6		2A	
Date:	Wednesday, July 30, 2008	Sheet	36 of 58

<http://hobi-elektronika.net>

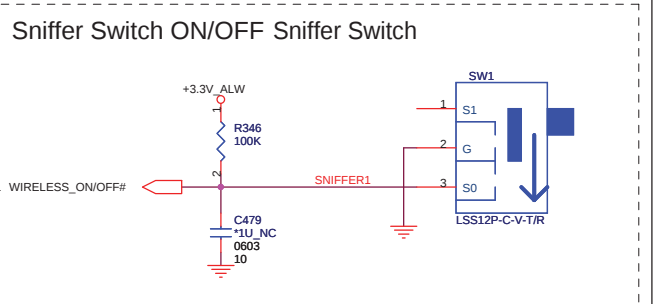
Biometric



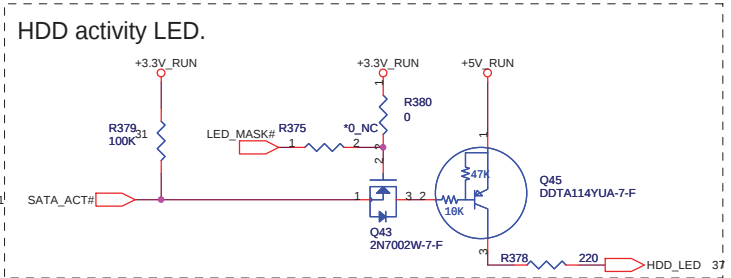
WLAN



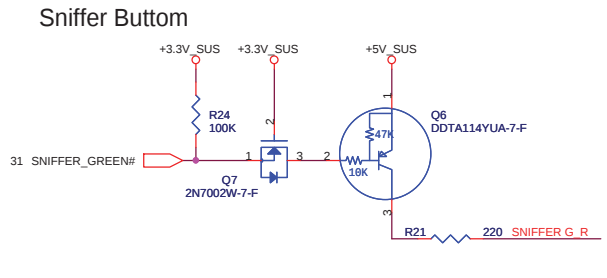
Sniffer Switch ON/OFF Sniffer Switch



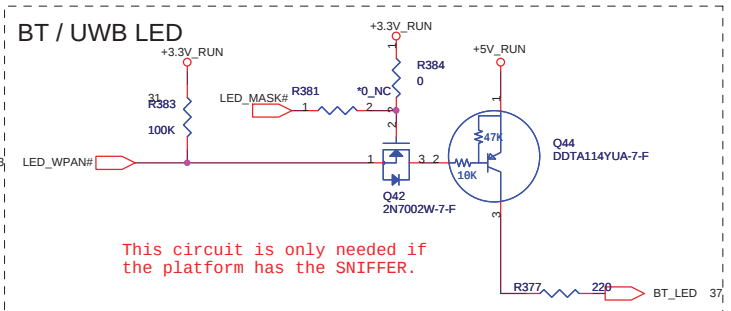
HDD activity LED.



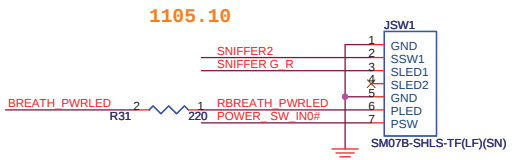
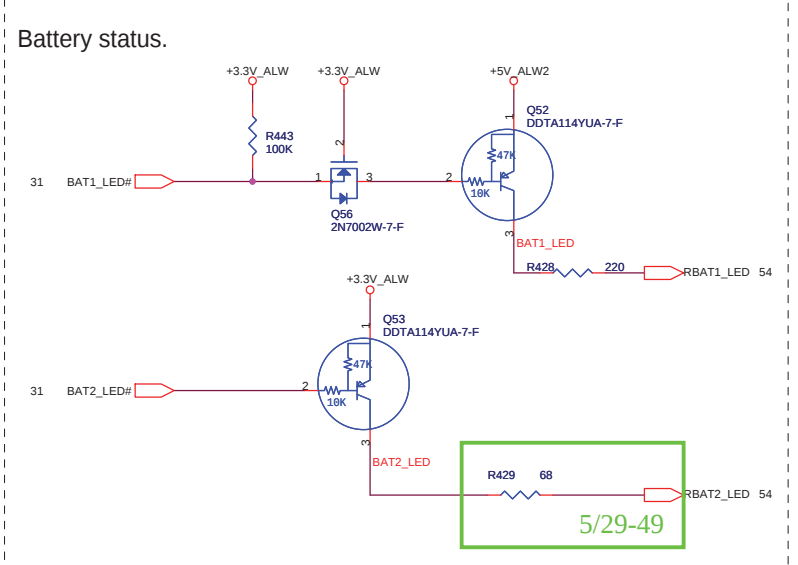
Sniffer Bottom



BT / UWB LED

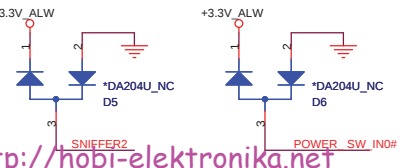


Battery status.

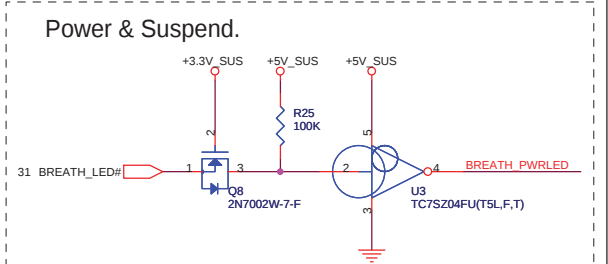


SNIFFER Y_R:WLAN on/off
SNIFFER G_R:AP detection

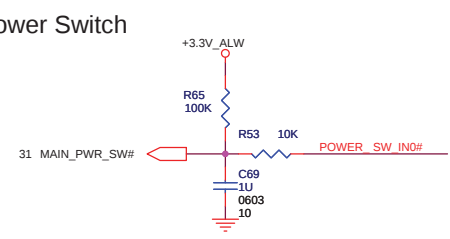
SNIFFER2	C526	100P	50
SNIFFER G_R	C527	100P	50
RBREATH_PWRLED	C528	100P	50
POWER_SW_IN0#	C529	100P	50

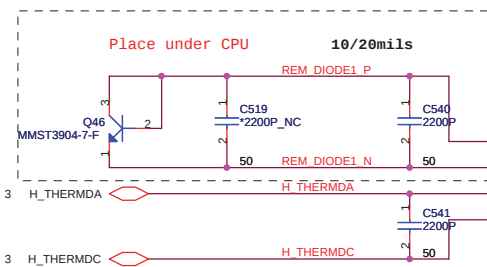
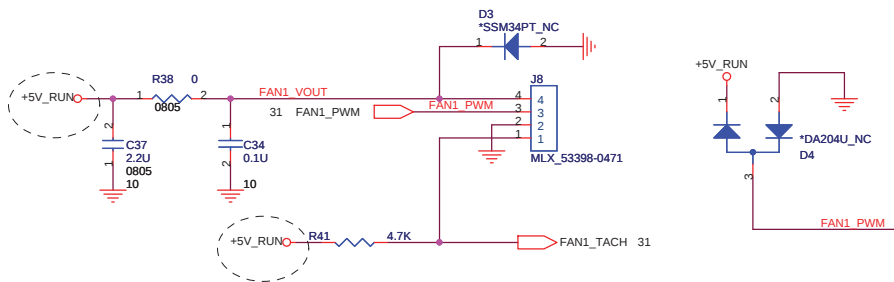


Power & Suspend.

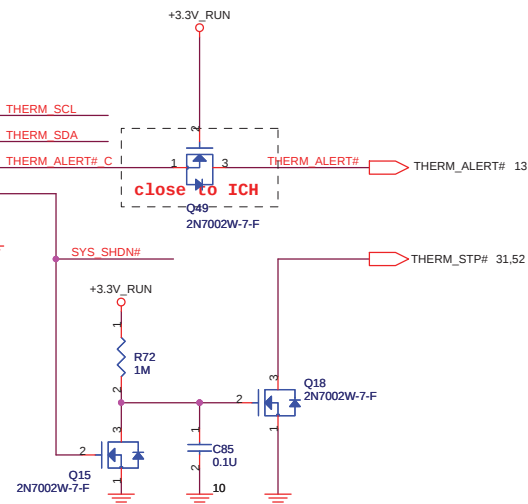
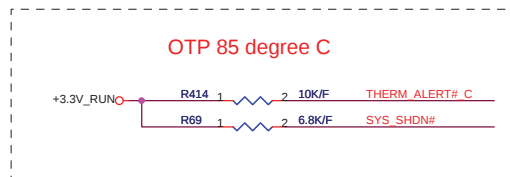
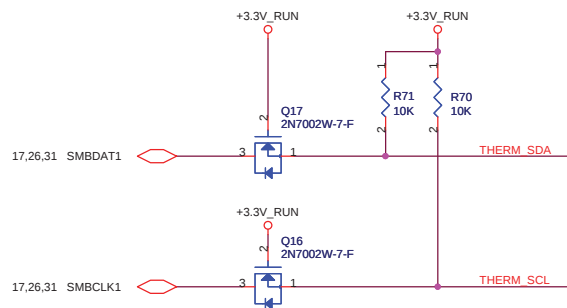


Power Switch

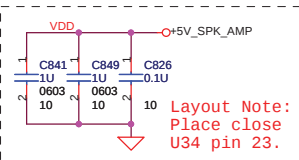
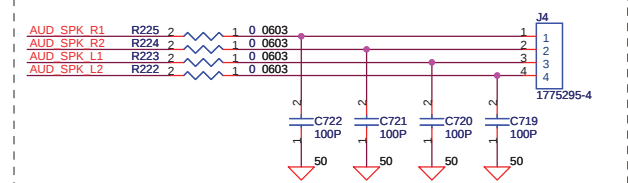
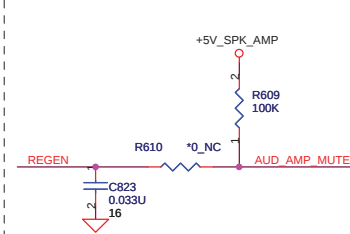
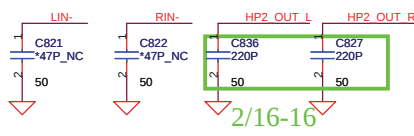
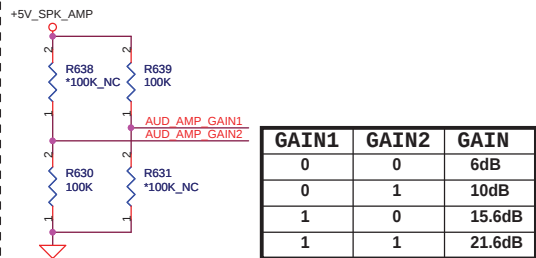




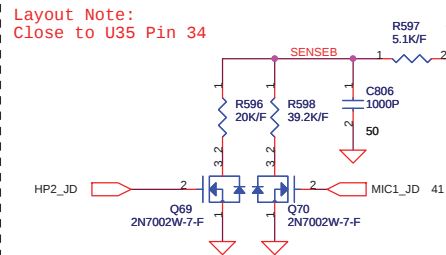
C523, C524 should close to thermal IC



Title		
FAN & THERMAL		
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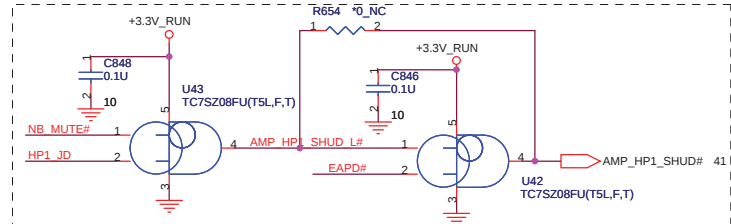
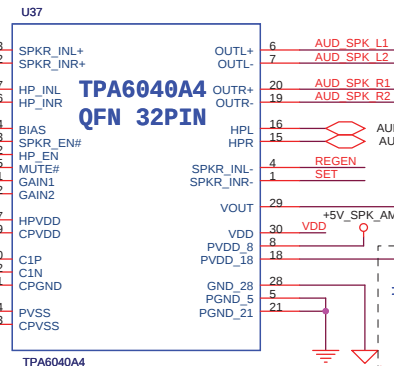


Layout Note:
Place close
U34 pin 23.

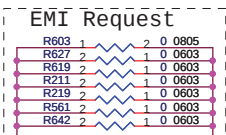


2/16-16

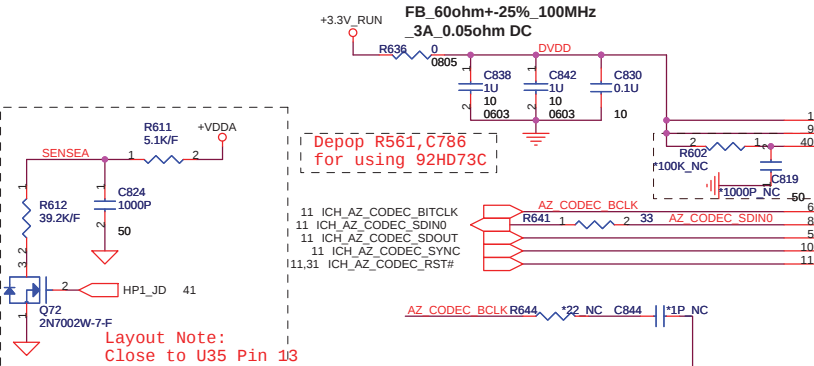
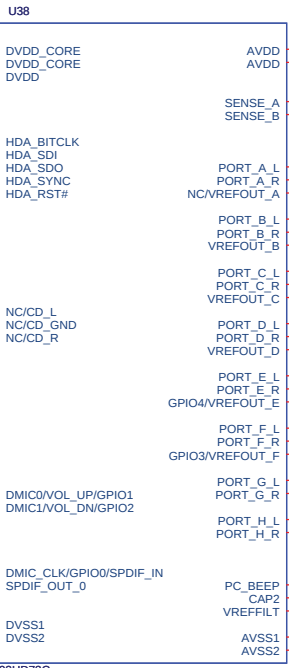
INTERNAL SPEAKER AMP



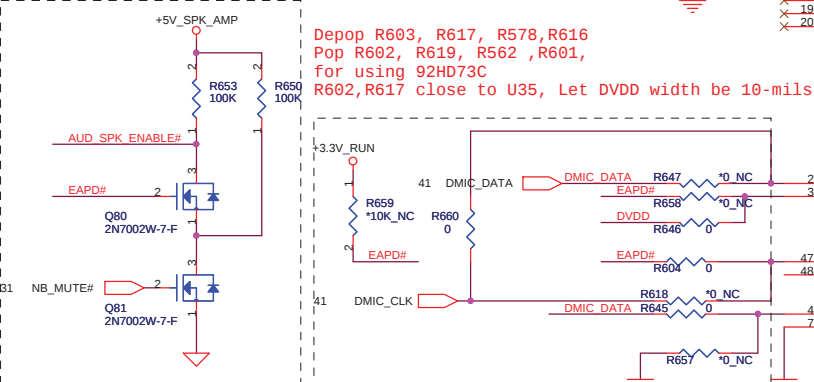
Layout Note:
Place close
U34.



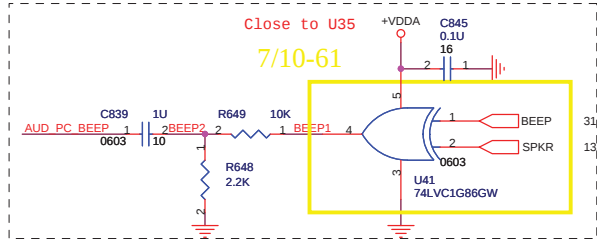
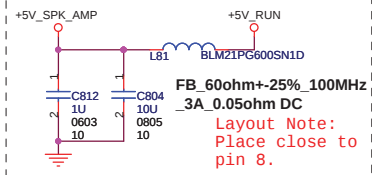
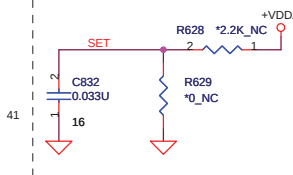
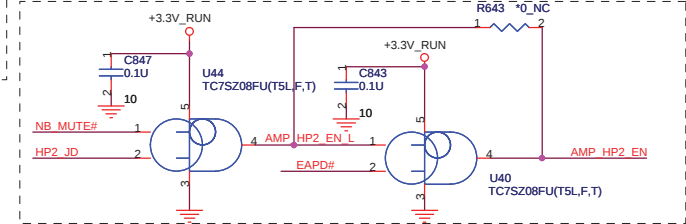
AZALIA (HD) CODEC



Depop R561, C786
for using 92HD73C



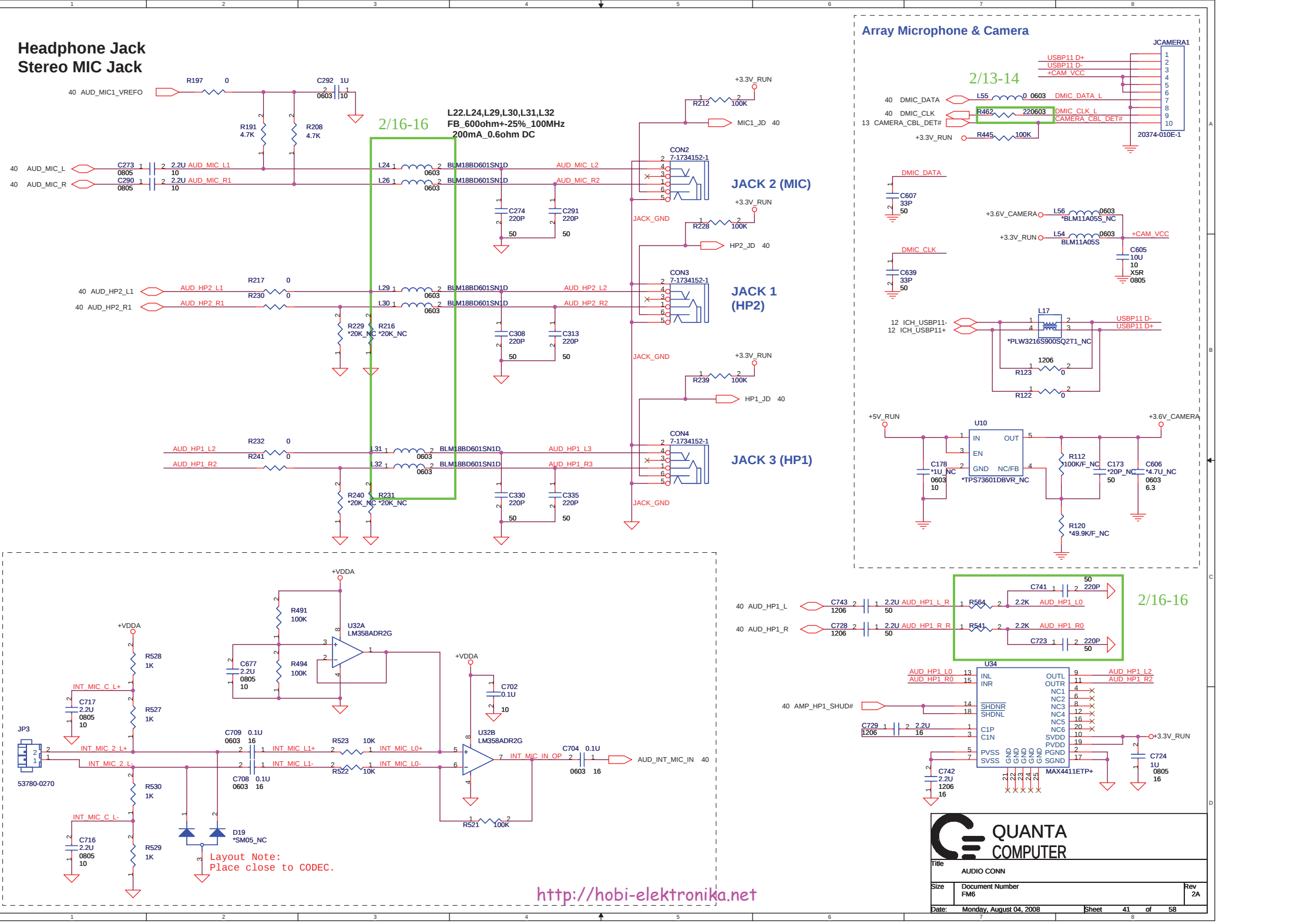
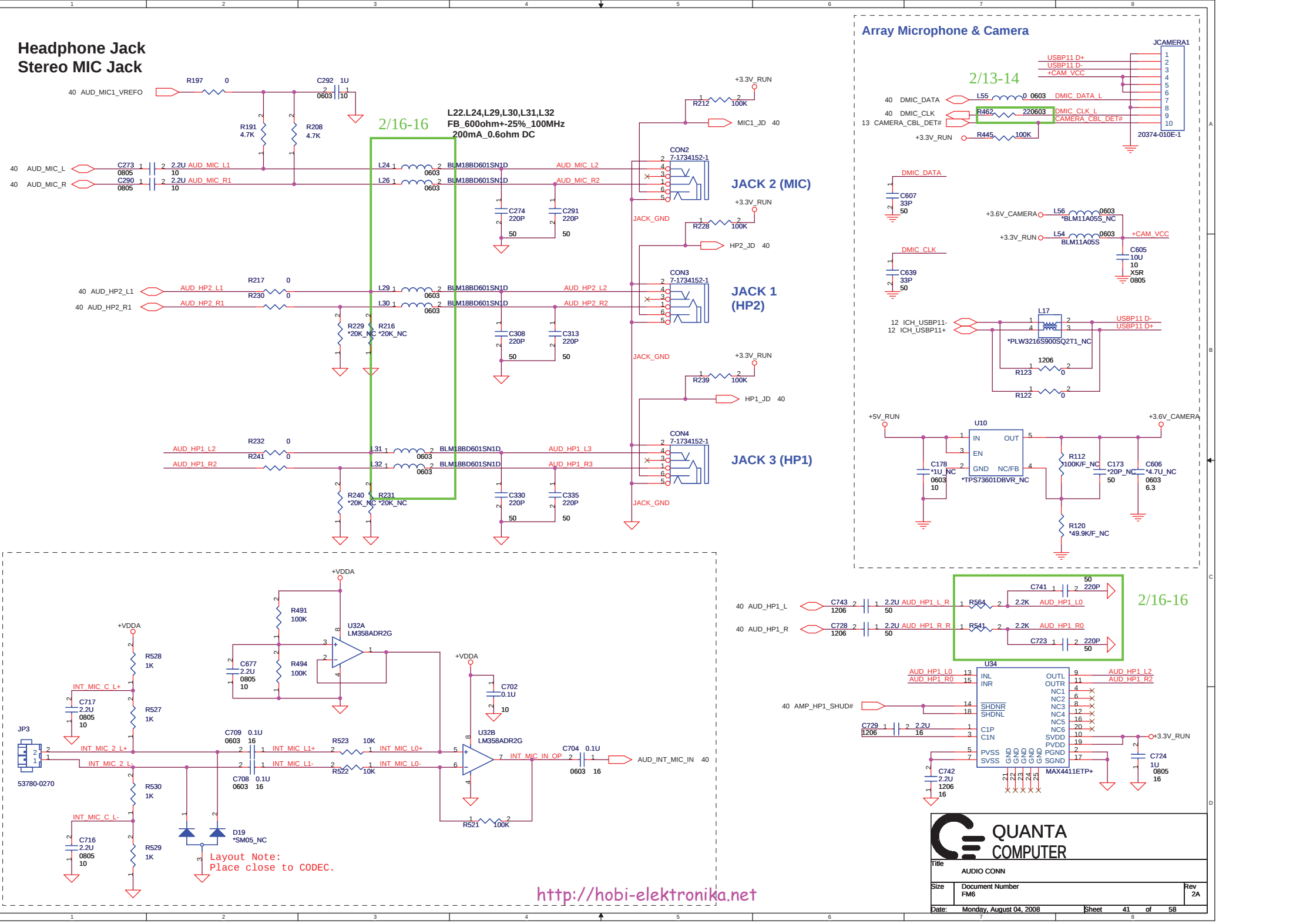
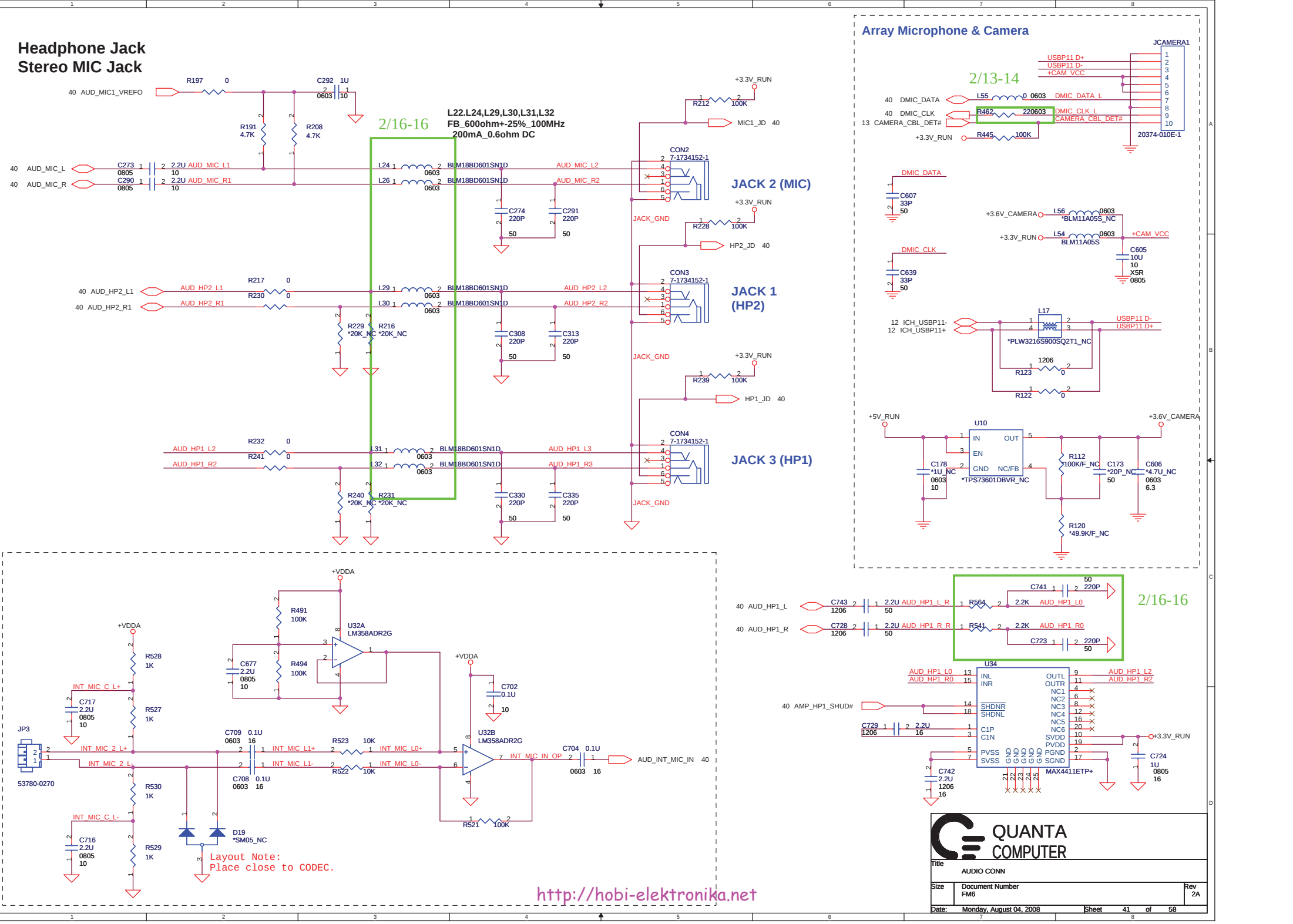
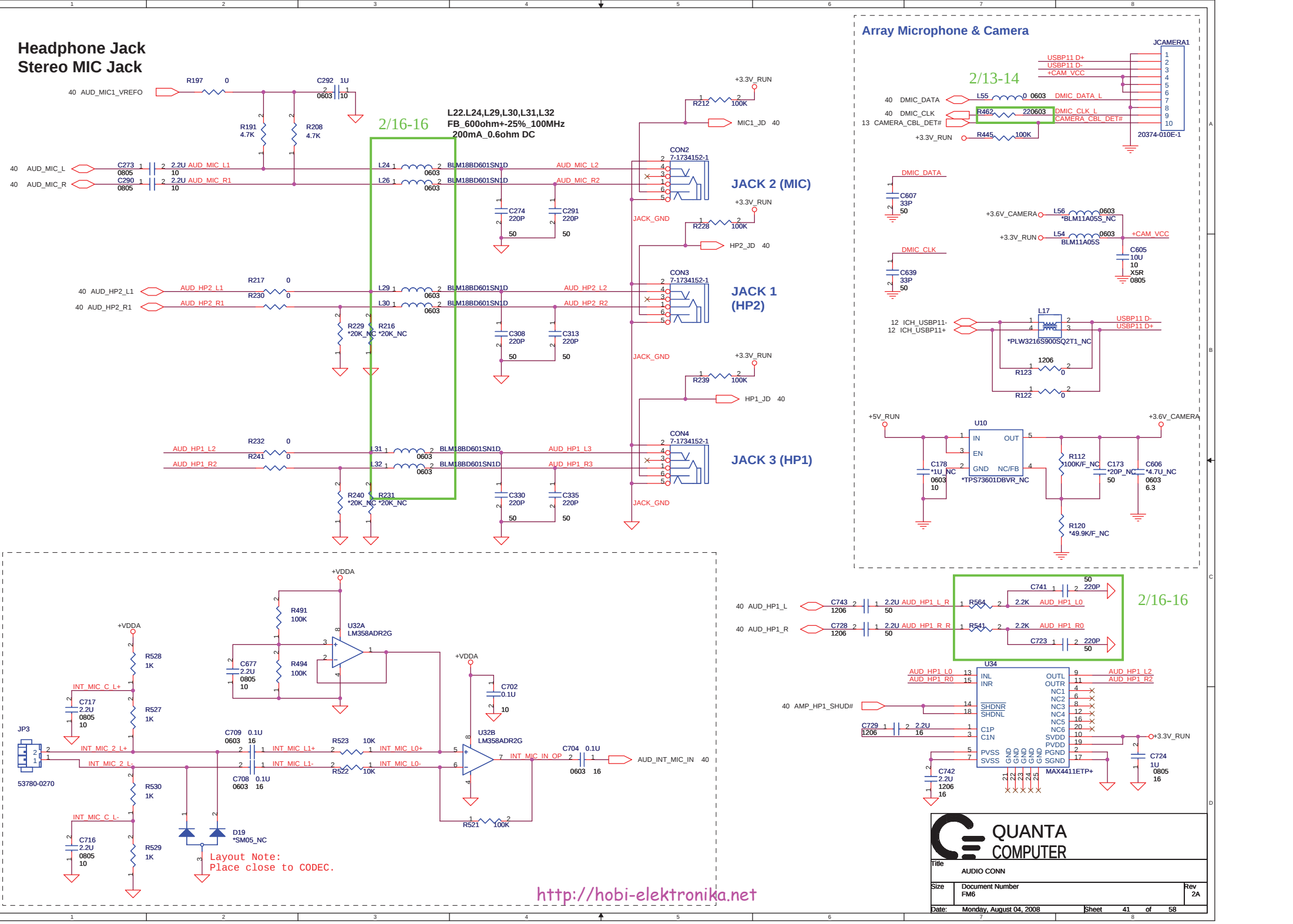
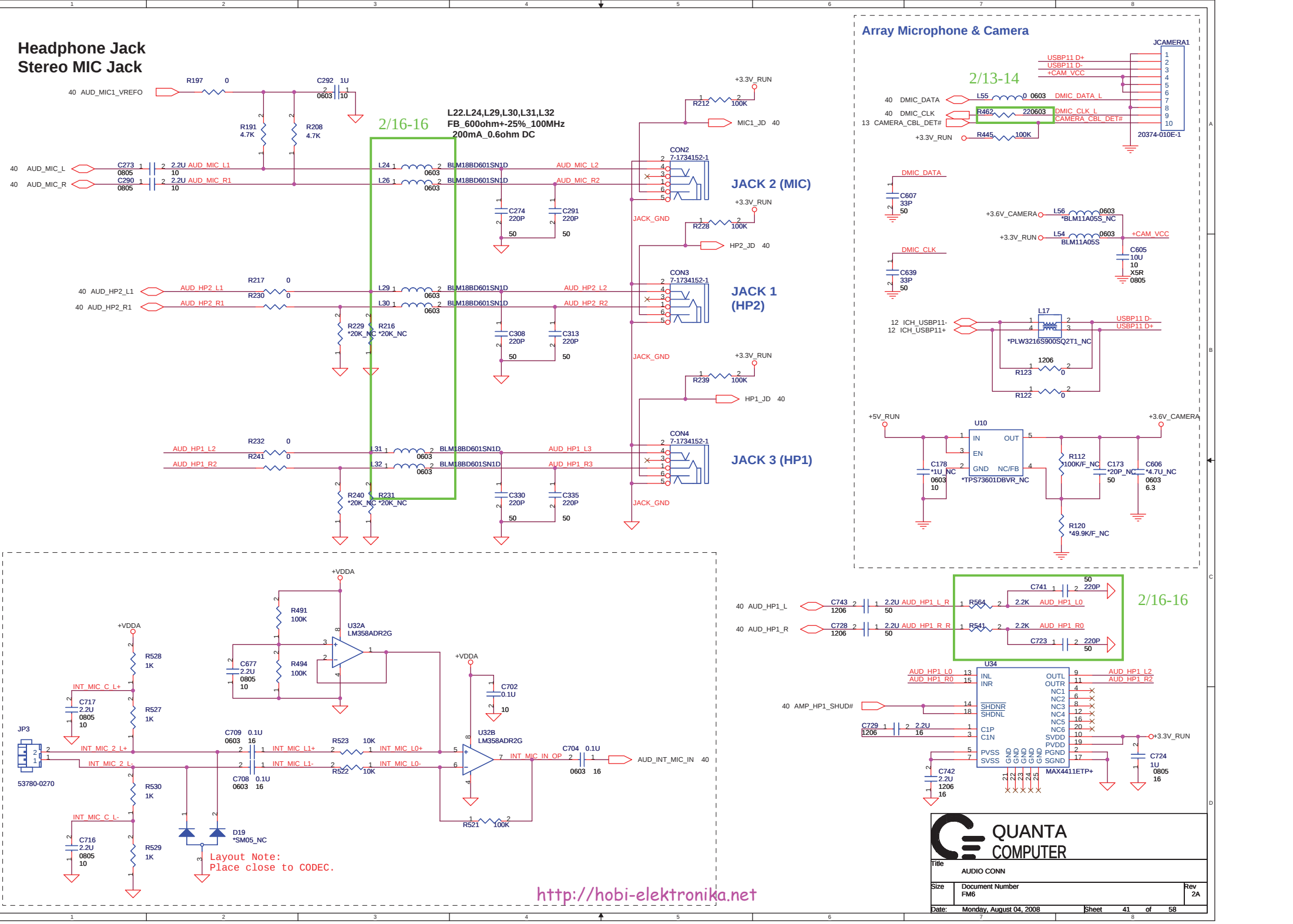
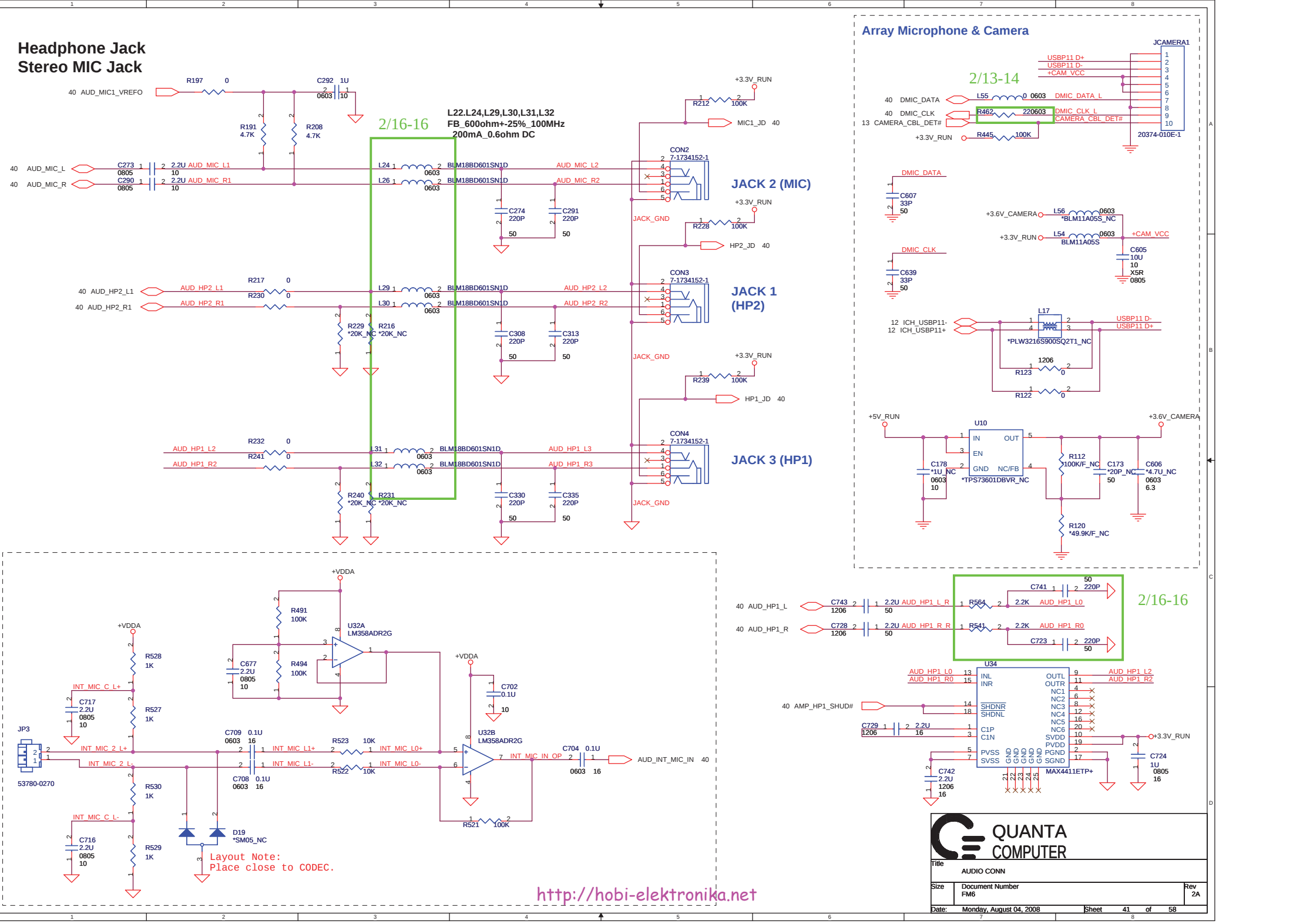
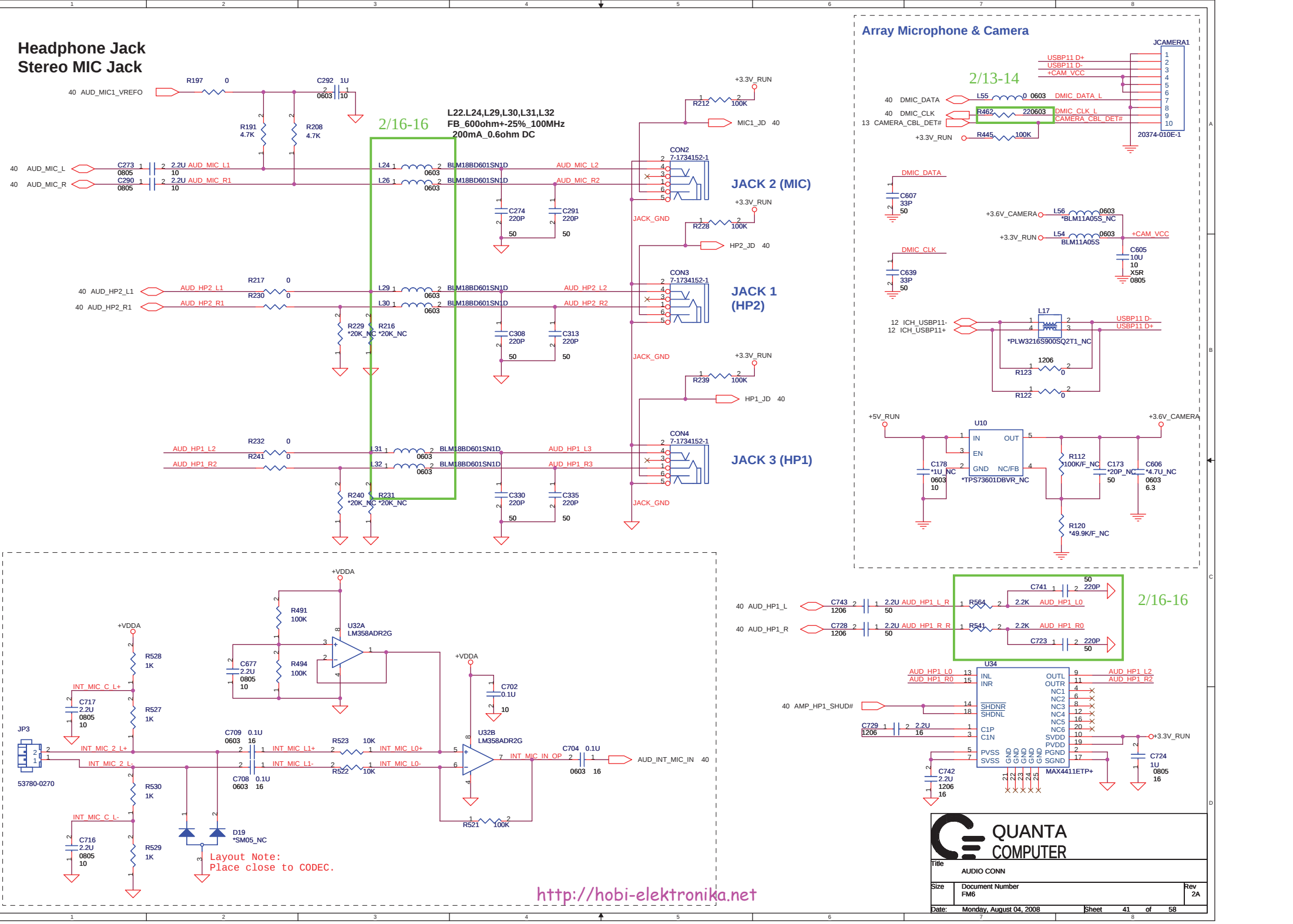
Depop R603, R617, R578, R616
Pop R602, R619, R562, R601,
for using 92HD73C
R602, R617 close to U35, Let DVDD width be 10-mils

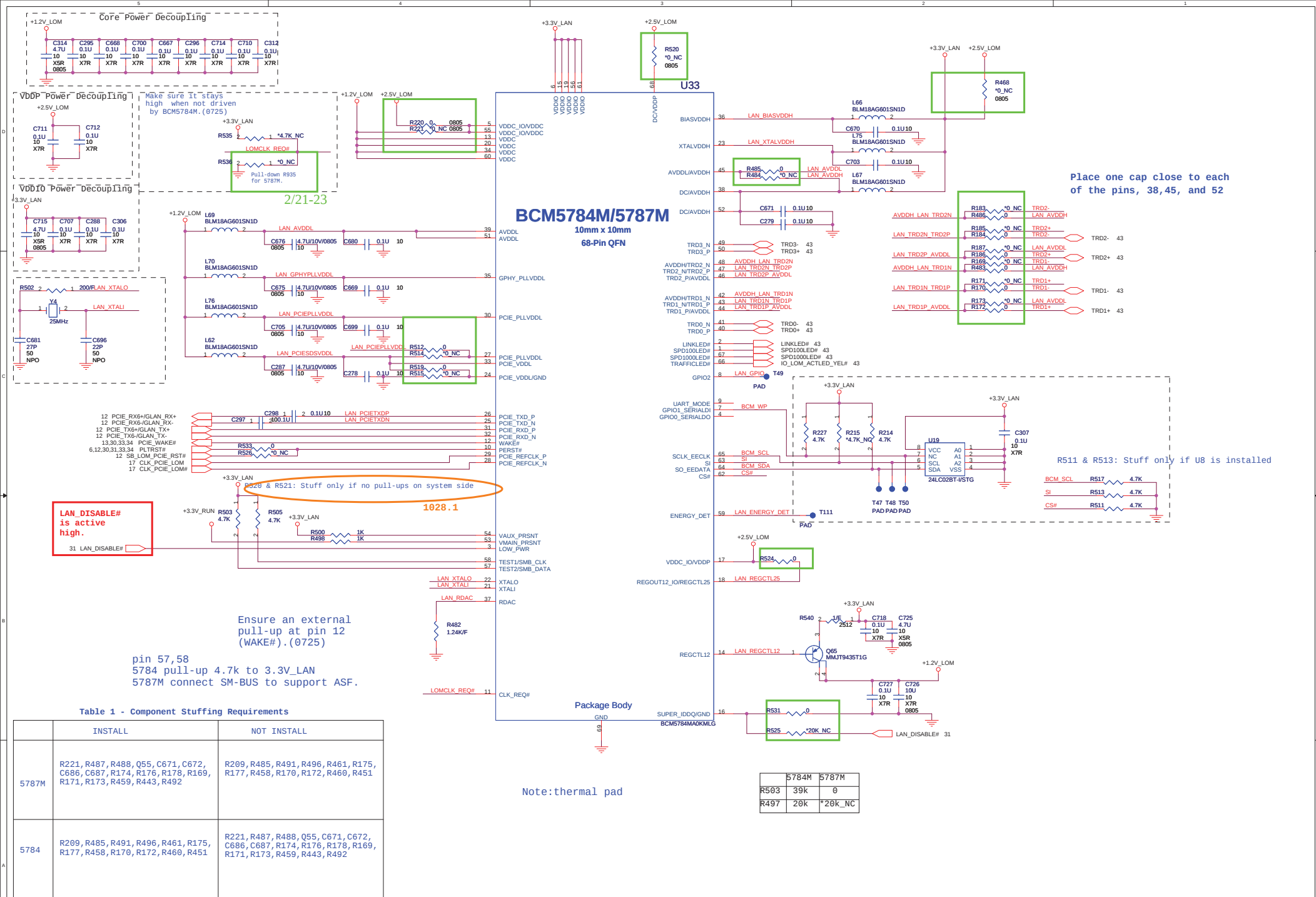


Close to U35
7/10-61

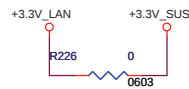
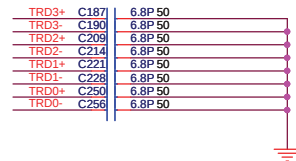
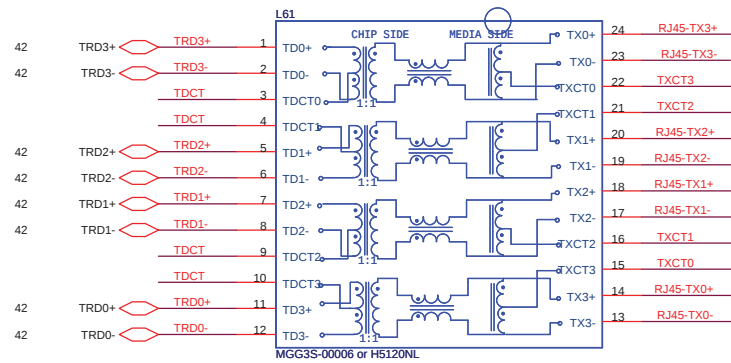
Headphone Jack Stereo MIC Jack

Headphone Jack Stereo MIC Jack

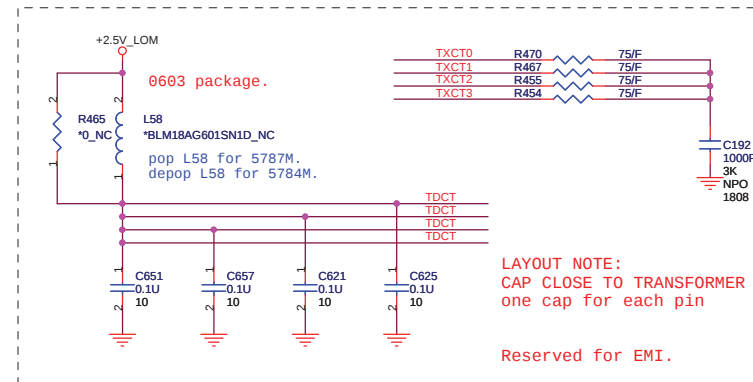
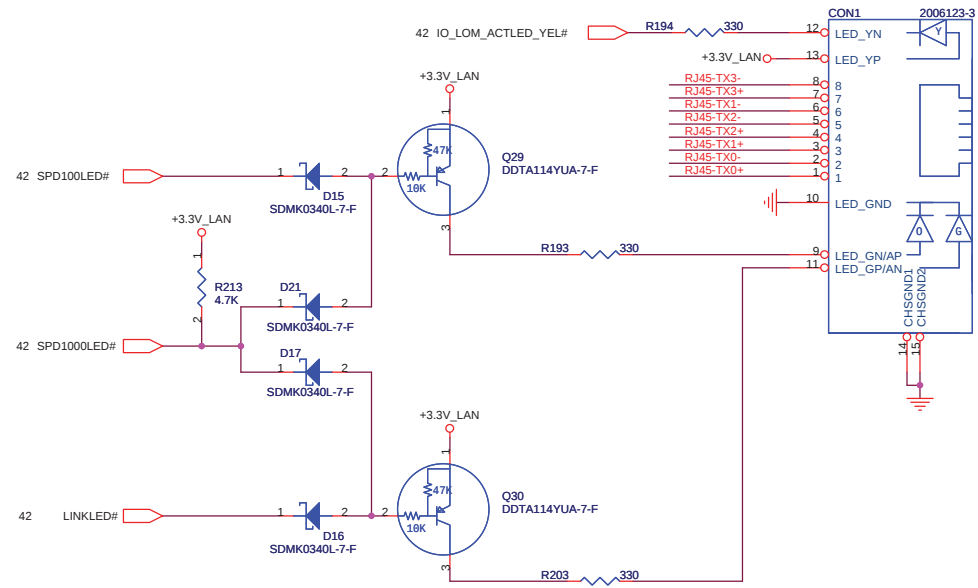
[illegible]

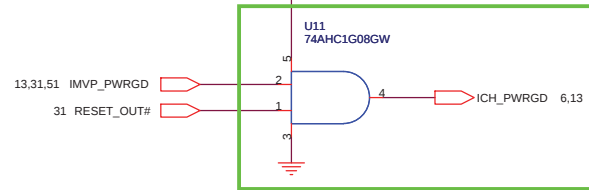
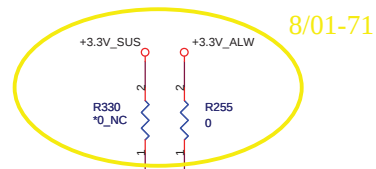


TRANSFORM TRANSFORM

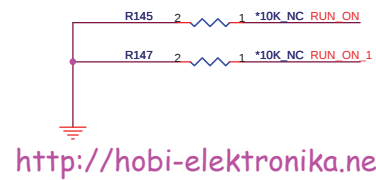
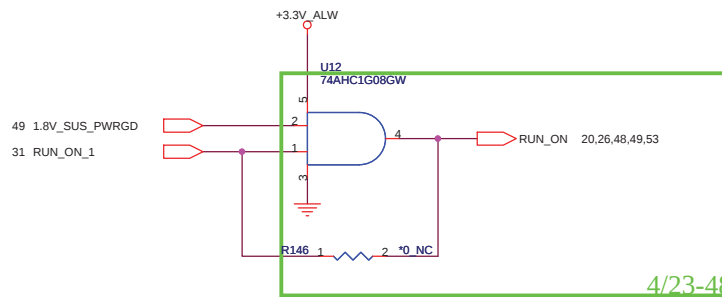
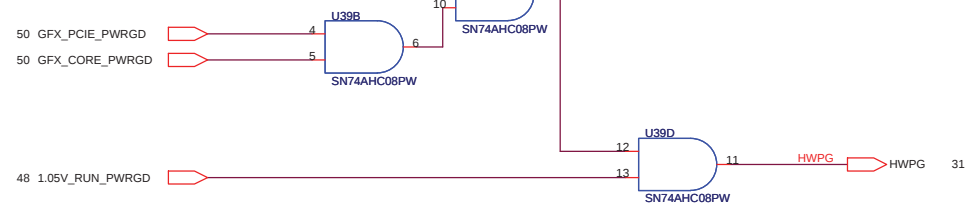
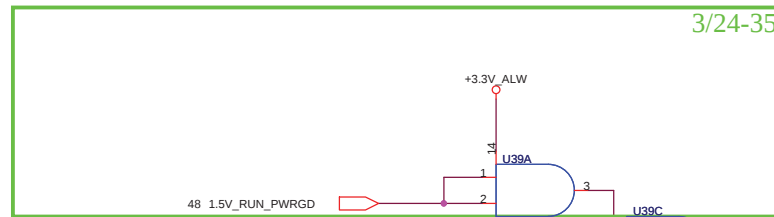


RJ-45 Connector





Keep Away from high speed buses



	1	2	3	4	5
A					
B					
C					
D					
	1	2	3	4	5

 QUANTA COMPUTER		
Title Battery Selector		
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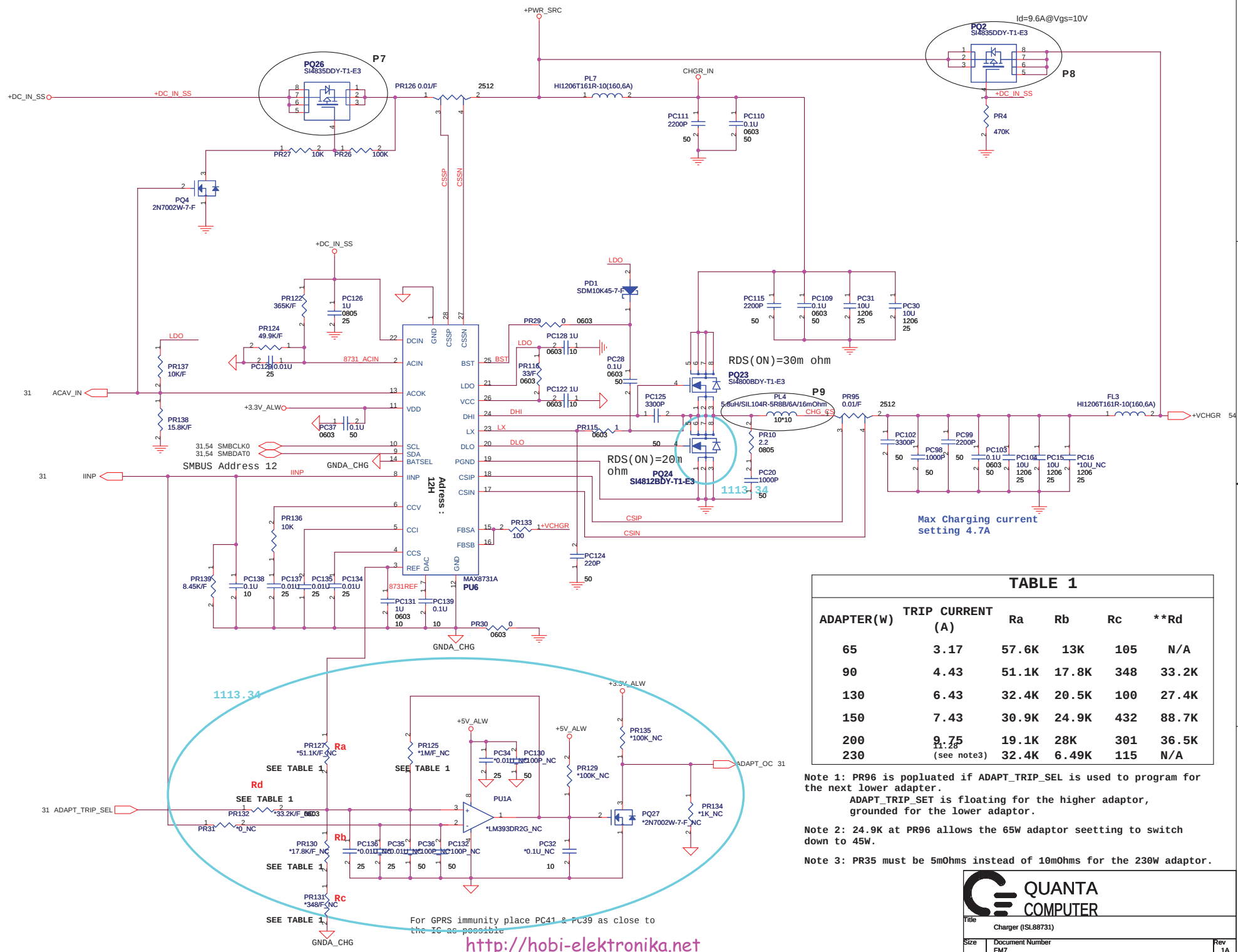


TABLE 1					
ADAPTER(W)	TRIP CURRENT (A)	Ra	Rb	Rc	**Rd
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28 (see note3)	32.4K	6.49K	115	N/A

Note 1: PR96 is populated if ADAPT_TRIP_SEL is used to program for the next lower adaptor.
 ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

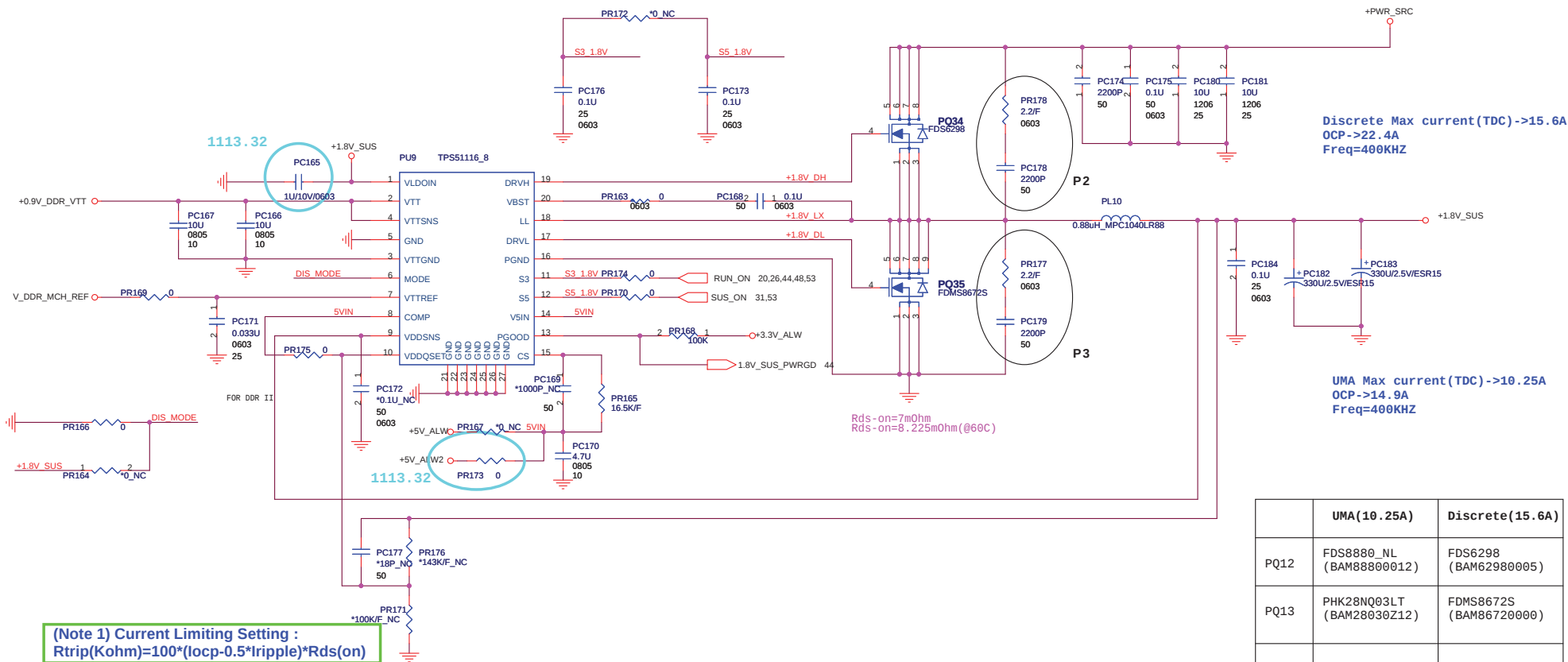
Note 2: 24.9K at PR96 allows the 65W adaptor setting to switch down to 45W.

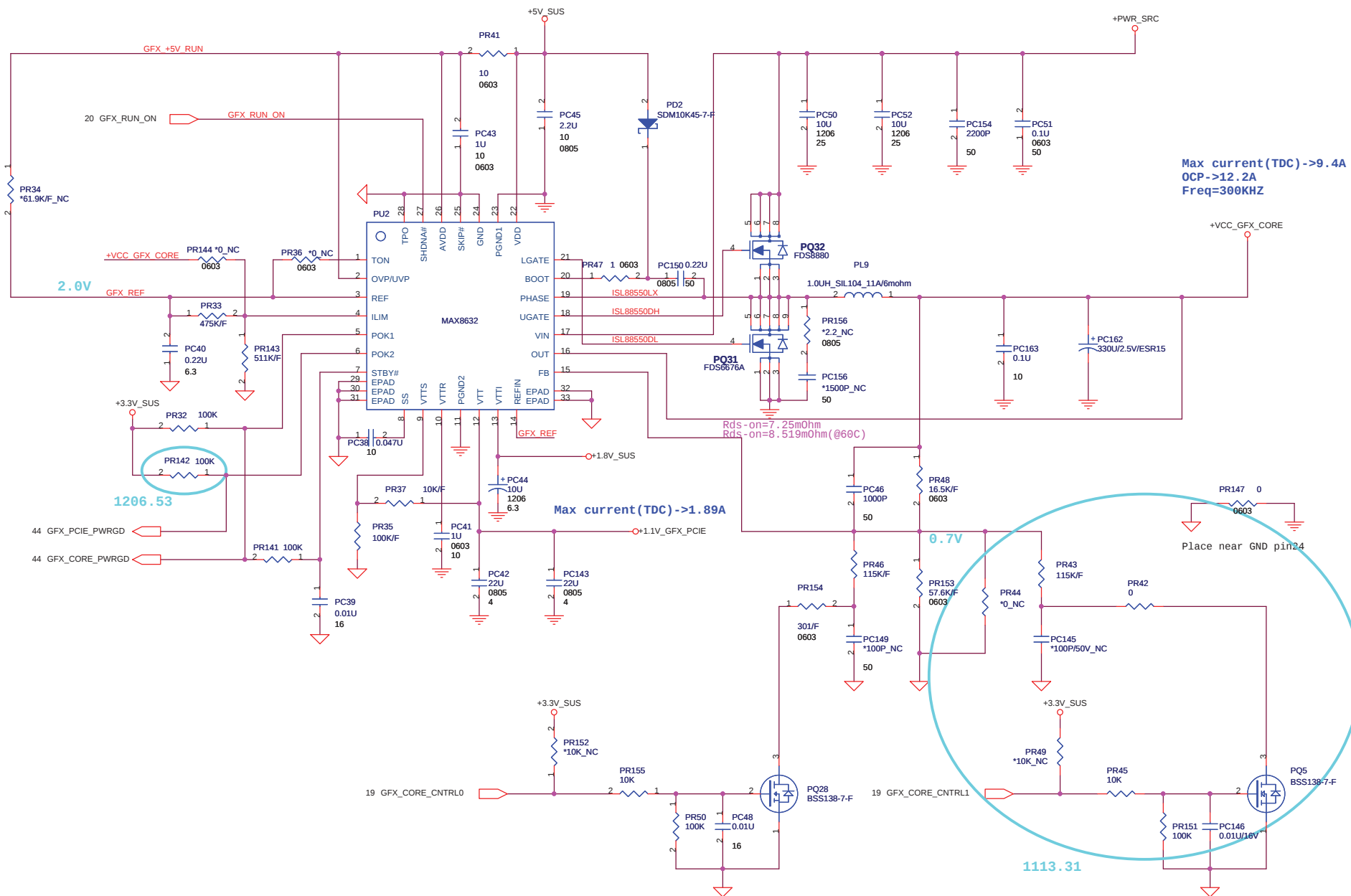
Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.

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GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9
HIGH	LOW	1.0V
HIGH	HIGH	1.1V

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Title: VGA DC/DC		
Size: FM7	Document Number:	Rev: 1A
Date: Wednesday, July 30, 2008	Sheet: 50	of 60

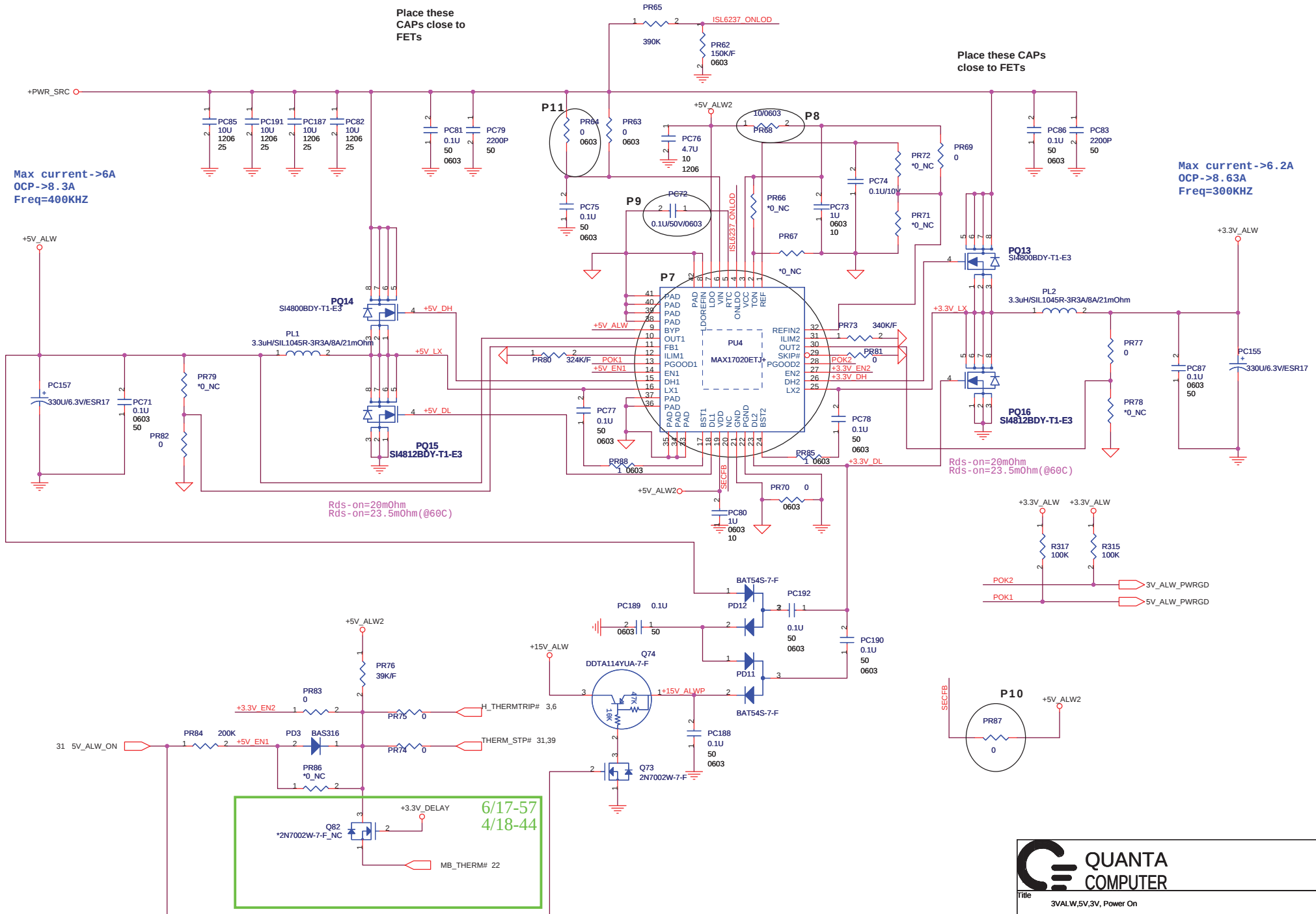
DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW

Place these
CAPs close to
FETs

Place these CAPs
close to FETs

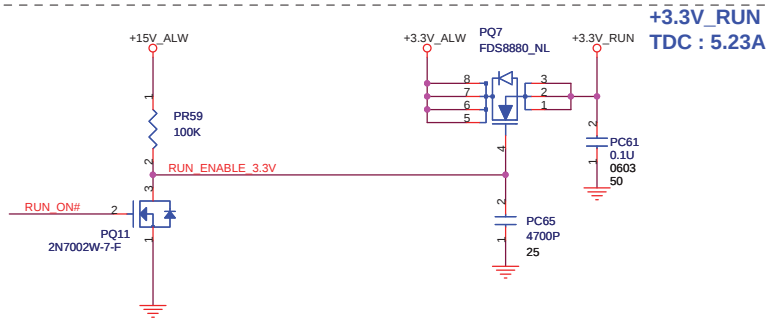
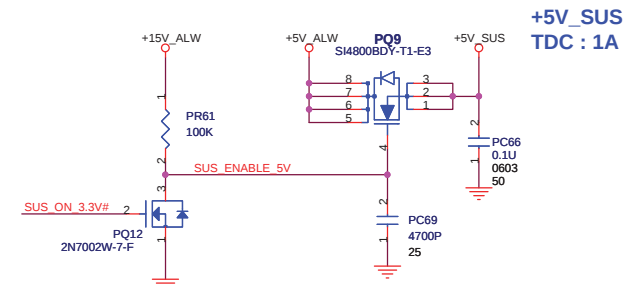
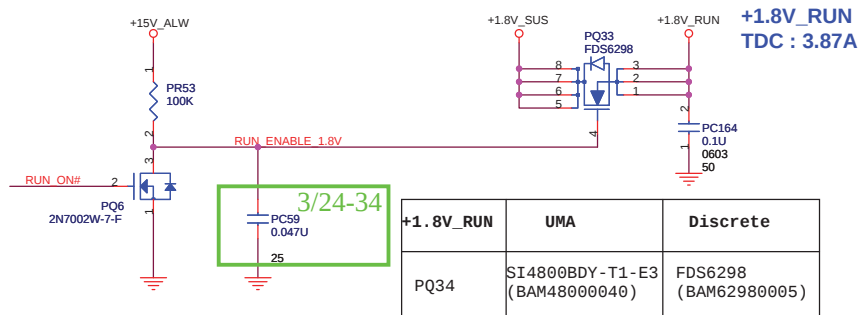
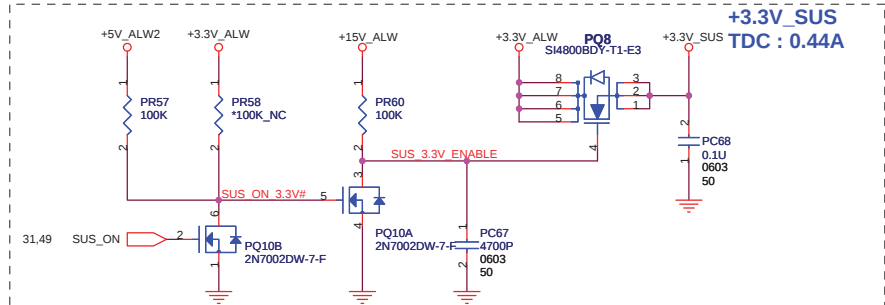
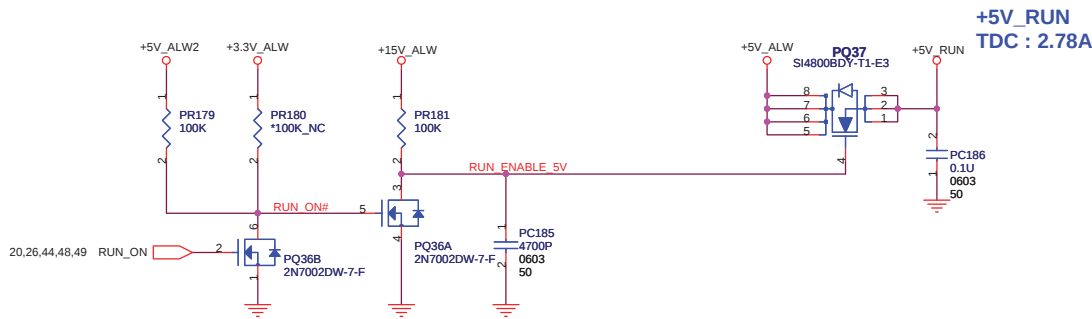
Max current->6A
OCP->8.3A
Freq=400KHZ

Max current->6.2A
OCP->8.63A
Freq=300KHZ

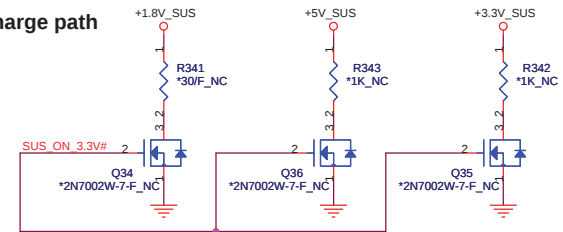


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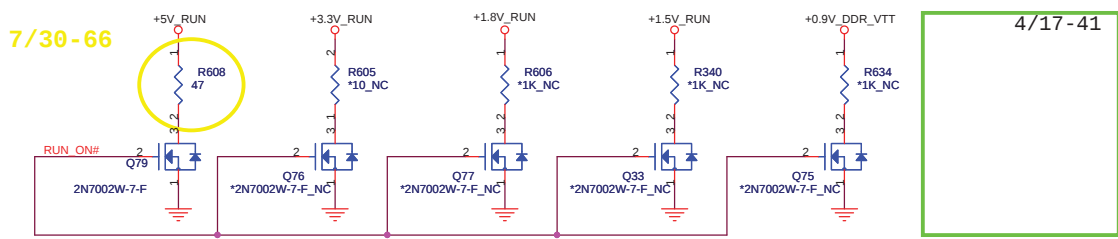
Title: 3VALW.5V.3V, Power On		
Size: FM7	Document Number:	Rev: 1A
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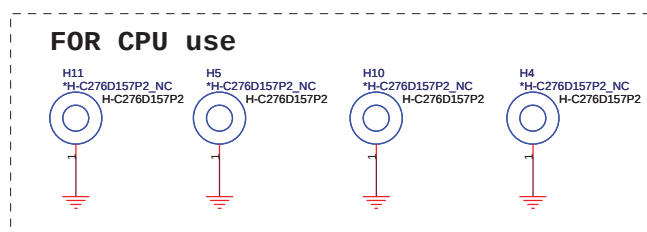
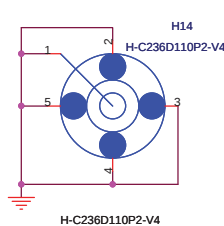
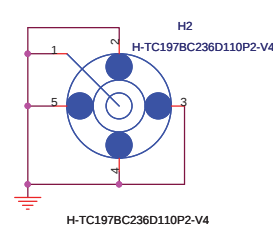
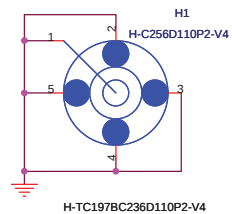
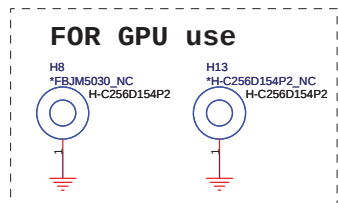
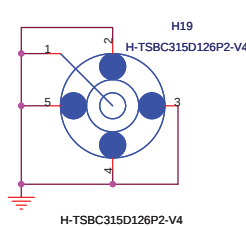
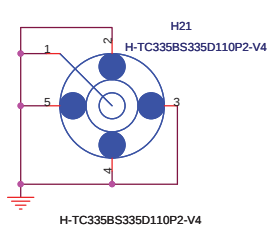
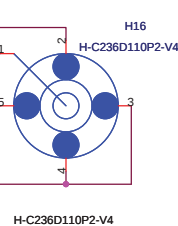
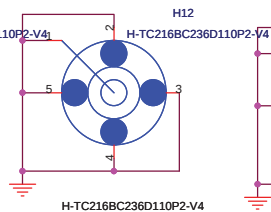
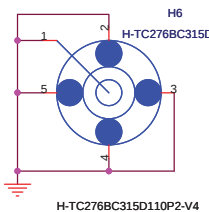
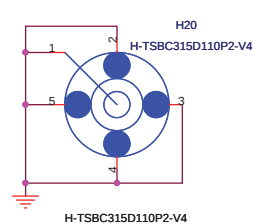
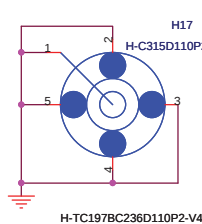
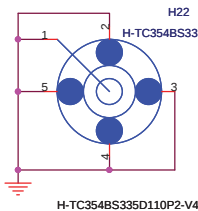
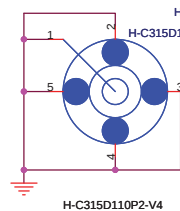
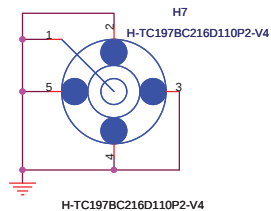
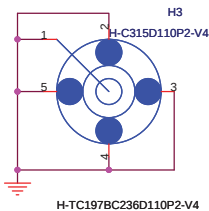
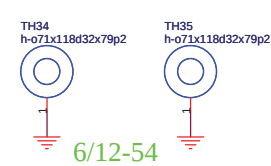
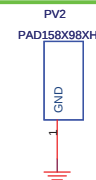
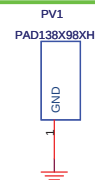
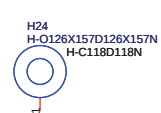
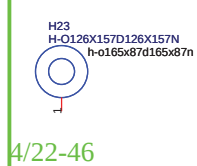
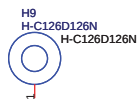
Reserve discharge path



Reserve discharge path

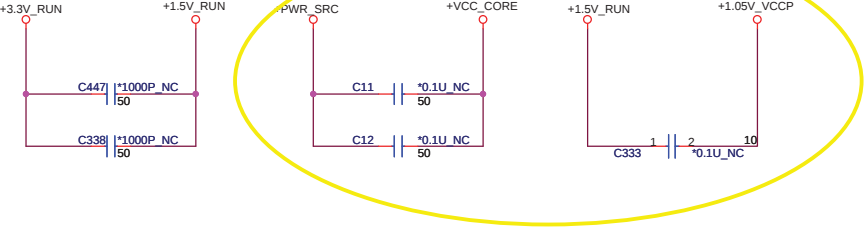


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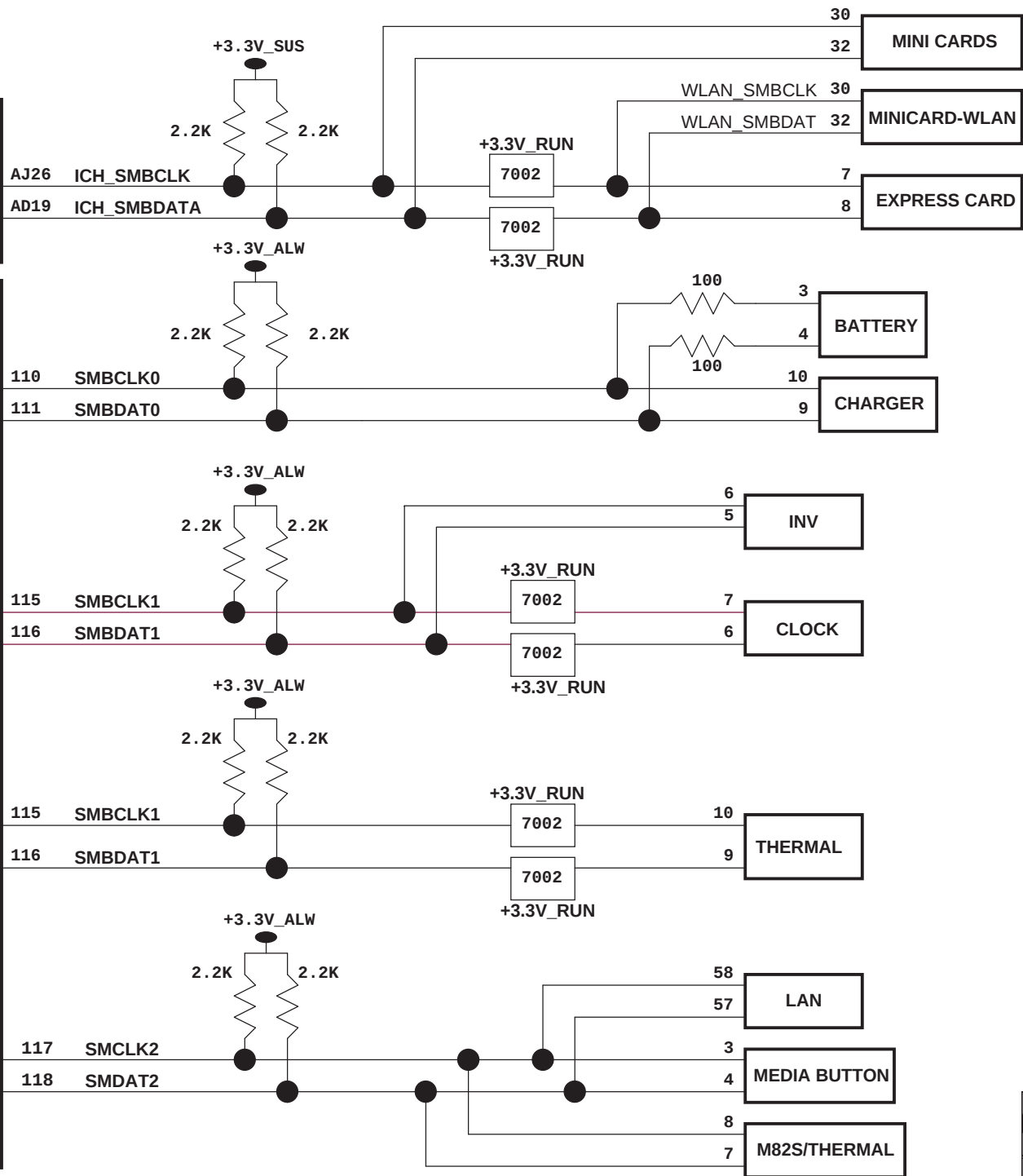
Reserved for EMI.

0906.1



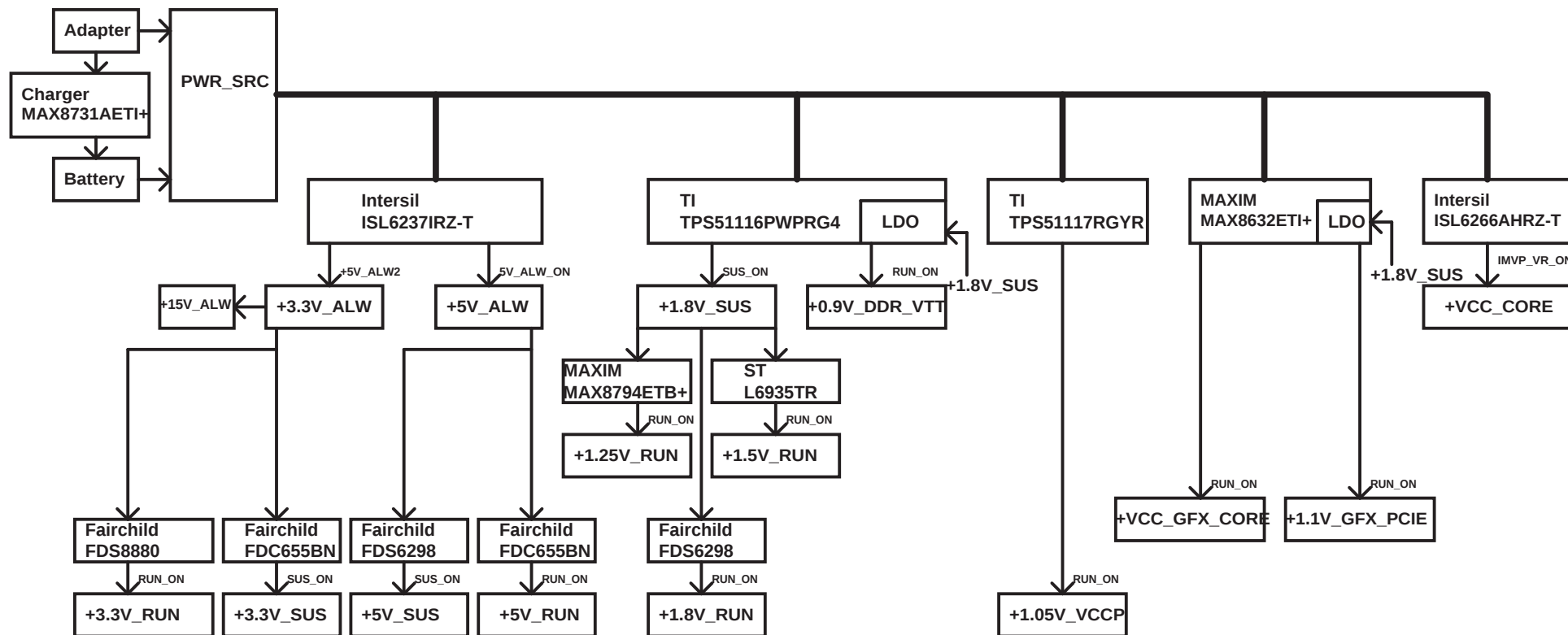
ICH8-M

SIO
ITE8512



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 QUANTA COMPUTER		
Title: SMBUS BLOCK		
Size: FM6	Document Number: 1A	Rev: 1A
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Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
FM7	1	3	2-13-08				Debug port needs to be updated for MV	Change the BOM, and add a pull high circuit on ITP_BPM#5
	2	3	2-13-08				H_THERM circuit has risk	Change the BOM in order to make it same with FM6
	3	8	2-13-08				VCC_AXG and VCC_AXG_NCTF are different with MV DG	Change VCC_AXG, and VCC_AXG_NCTF to ground
	4	11, 35	2-13-08				Add E-SATA function	Refer to page 11 and 35
	5	13	2-13-08				Some power rails don't mach with DG	Refer to page 13
	6	17	2-13-08				BSEL0, BSEL1, and BSEL2's seris resisters don't mach with DG	Refer to page 17
	7	9	2-13-08				VCCA_SM doesn't mach with DG	Add 0-ohm in order to make it same with other project
	8	9	2-13-08				VCCD_TVDAC and VCCD_QDAC are different with DG	Grond VCCD_TVDAC and update another circuit for VCCD_QDAC
	9	19,22	2-13-08				Change the power rail for avoiding leakage during power up	Change +3.3V_RUN to +3.3V_DELAY
	10	37	2-13-08				MMB vender changed it's F/W to fix the LED flash issue. Change Num /Cap LED circuit for avoiding leakage voltage	Change the circuit, refer to page 37
	11	35	2-13-08				Fulfill reliability's request	Add one more power pin on connector
	12	31	2-13-08				New chip version for ITE	Change the circuit
	13	40,42	2-13-08				Change chip version for Codec and LOM	Done
	14	41	2-13-08				Approve DMIC'S performance according to IDT's recommendation	Change o-ohm to 22-ohm
	15	26	2-16-08				DDC BUS for HDMI Certificate	Add Level Shift on DDC BUS of HDMI
	16	40,41	2-16-08				Need to meet WLP4.0	Refer to page 40 and 41
	17	31	2-16-08				Add audio solution for PO noise issue when loading driver	Connect ICH_AZ_CODEC_RST# to SIO.22
	18	14	2-18-08				Reserve +1.5V_SUS for VCCSUSHDA	Add a LDO and reserve 0-ohm for +1.5V_SUS
	19	13	2-18-08				Avoid leakage voltage	Follow the SR FM6 design
	20	17	2-19-08				After FAE review, modify circuit in order to let wave form smooth	Add two 0.1u cap
	21	17	2-20-08				After FAE review, modify circuit for single end nets	change 0-ohm to 33-ohm, add pull high resister
	22	35	2-20-08				Add E-SATA redriver function	Refer to page 35
	23	42	2-21-08				According to FAE, stub a resister	Refer to page 42
	24	17	2-21-08				In order to meet spec, we need to swap two signals	Refer to page 17
	25	35	2-22-08				Co-work with GM3 team and decide to take USB charger function off	Refer to page 35
	26	21	2-22-08				According to realiability team request, change BOM	Change L51
	27	12	2-25-08				Need to meet Dell USB port requirement	Refer to page 12
	28	19	2-25-08				FAE's suggestion is add ground	Refer to page 19
	29	13,37	2-25-08				Add one pin for LCD inverter det	Refer to pages
	30	30	3-03-08				Footprint is wrong for express card	Refer to FM6 footprint
	31	32 35	3-24-08				Change locations for USB and Coin Battery for safty requirement	Refer to those pages
	32	26 35	3-24-08				Change BOM for HDMI and E-sata	Refer to those pages
	33	49	3-24-08				Del 1.25V power rail	Refer to page 49
	34	53	3-24-08				Change BOM for correcting power sequence	Refer to page 53
								 QUANTA COMPUTER Title Change List Size Document Number Rev FM7 1A Date: Wednesday, June 18, 2008 Sheet 1 of 6

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