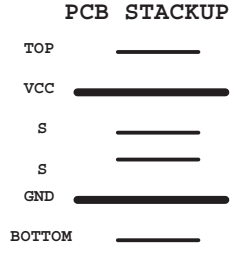
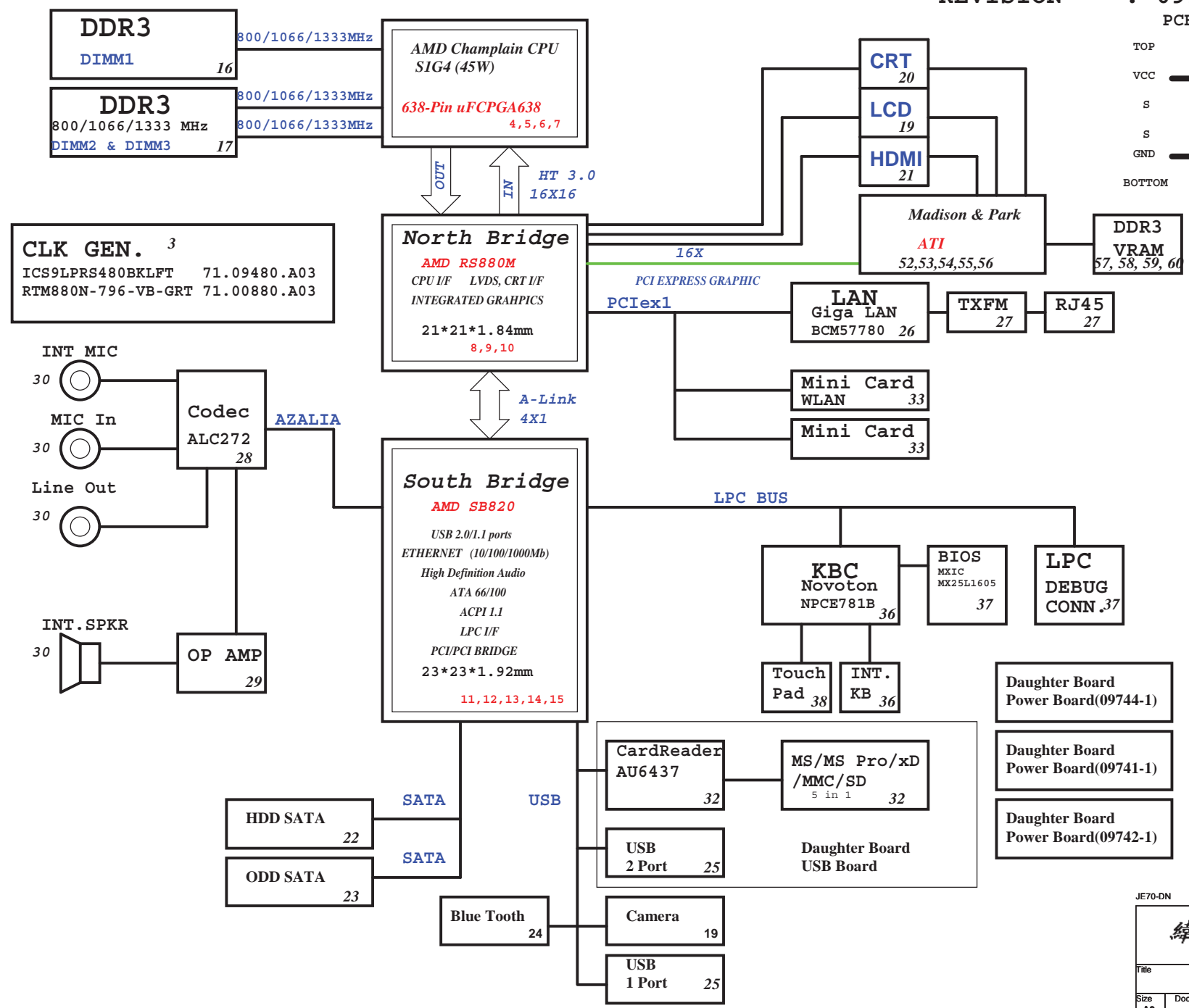


JE70-DN/SJV71-DN/HM72-DN Block Diagram

Project code: 91.4HP01.001
 PCB P/N : 48.4HP01.011
 REVISION : 09929-1



SYSTEM DC/DC RT8223 45	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (5A)
	3D3V_S5 (5A)
SYSTEM DC/DC RT8209E 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3
SYSTEM DC/DC RT8015A 47	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0
RT9025 48	
5V_S5	1D05V_S0
RT9161 48	
3D3V_S0	2D5V_S0 (200mA)
RT9025 48	
3D3V_S0	1V_VGA (1.2A)
RT9025, RT8209E 47	
3D3V_S5	1D1V_S5
5V_S5	1D1V_S0
CHARGER BQ24745 49	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A
	UP+5V 5V 100mA
CPU DC/DC ISL6265HR 44	
INPUTS	OUTPUTS
	VCC_CORE_S0_0 0~1.55V 18A
DCBATOUT	VCC_CORE_S0_1 0~1.55V 18A
	VDDNB 0~1.55V 18A



JE70-DN

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLOCK DIAGRAM**

Size: A3 Document Number: **JE70-DN** Rev: SB

Date: Wednesday, March 31, 2010 Sheet 1 of 63

EC Functional Strap Definitions

page9

<p>STRAP_DEBUG_BUS_GPIO_ENABLEB Enables the Test Debug Bus using GPIO. (PIN: RS780M--> VSYNC#) * 1 :Disable 0 : Enable</p>
<p>RS780: Enables Side port memory (RS880 use HSYNC#) * 1 :Disable 0 : Enable</p>

<p>SUS_STAT# Selects Loading of STRAPS From EEPROM * 1 : Bypass the loading of EEPROM straps and use Hardware Default Values 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected</p>

page15

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL <i>DEFAULT</i>	DISABLE ILA AUTORUN <i>DEFAULT</i>	USE FC PLL <i>DEFAULT</i>	USE DEFAULT PCIE STRAPS <i>DEFAULT</i>	DISABLE PCI MEM BOOT <i>DEFAULT</i>
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

page15

	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200	GPIO199
PULL HIGH	ALLOW PCIE Gen2 <i>DEFAULT</i>	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE <i>DEFAULT</i>	EC ENABLED	CLKGEN ENABLED <i>DEFAULT</i>	LOW POWER MODE	H,H = Reserved H,L = SPI ROM	
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled <i>DEFAULT</i>	IGNORE DEBUG STRAP <i>DEFAULT</i>	FUSION CLOCK MODE	EC DISABLED <i>DEFAULT</i>	CLKGEN DISABLED	PERFORMANCE MODE <i>DEFAULT</i>	L,H = LPC ROM (Default) L,L = FWH ROM	

NOTE: SB820 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

Signal	Comment
TEST# pin110	Test Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to determine the device operation mode as follows: No pull-down resistor: Normal operation mode (XORTR and TRIST strap pins are ignored). 10 KΩ external pull-down resistor:Test mode (ICT or XOR-Tree Test mode, according to XORTR and TRIST strap pins).
XORTR# pin111	XOR-Tree Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the XOR-Tree Test mode, if TEST is strapped low: No pull-down resistor: Not allowed if TEST pin is strapped low. 10 KΩ external pull-down resistor:XOR-Tree Test mode .Note: TRIST strap pin must be left unconnected.
TRIST# pin112	ICT Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the ICT Test mode, if TEST is strapped low: No pull-down resistor: Not allowed if TEST pin is strapped low. 10 KΩ external pull-down resistor:ICT Test mode (see Section 3.4.1 on page 53), forces the device to float its output and I/O pins.Note: XORTR strap pin must be left unconnected.
JEN0#, JENK# pin49,53	JTAG Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the JTAG signals to device pins (see Table 4 on page 35 for details). Both JEN0 and JENK, are pulled to 1 by an internal resistor The external 10 KΩ pull-down resistor must be connected to GND.
SHBM pin83	Shared Host BIOS Memory. Sampled at VCC Power-Up reset or VCC_POR Input reset, to determine the state of the shared BIOS memory. No pull-down resistor:Disable the shared BIOS memory. 10 KΩ external pull-down resistor:Enable the shared BIOS memory
SDP_VIS# pin41	Port80 (SDP) Visibility Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the Visibility mode for the Port80 (SDP). No pull-down resistor: SDP in Normal mode 10 KΩ external pull-down resistor:SDP in Visibility mode.
XOR_OUT pin35	XOR-Tree Output. The device pins are internally connected in a XOR-tree structure

page12

USB	
Pair	Device
12	MINI2 CARD
11	NC
10	NC
9	CCD
8	NC
7	Bluetooth
6	USB3
5	USB2
4	CardReader
3	NC
2	USB4
1	MINI1 CARD
0	USB1

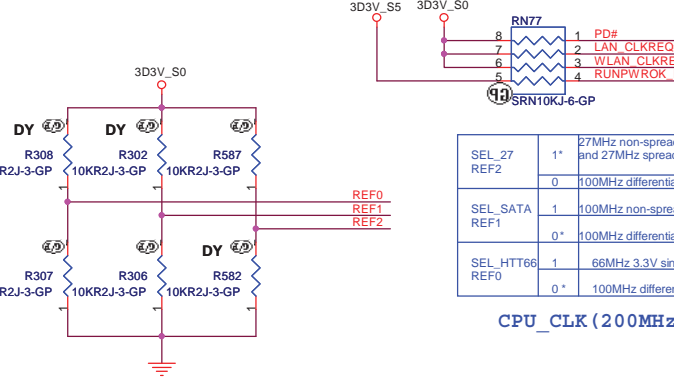
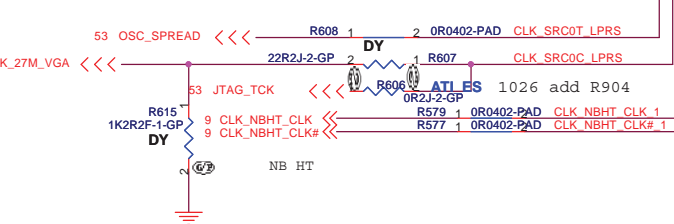
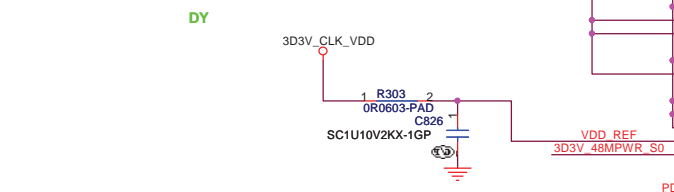
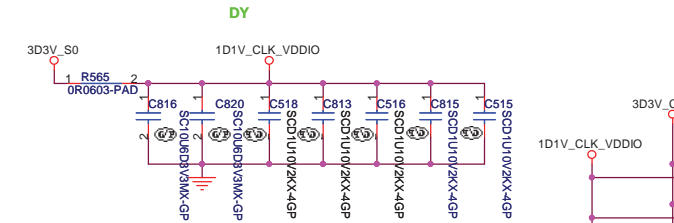
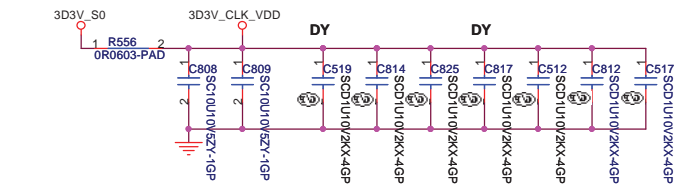
OCP3#

OCP2#

OCP0#

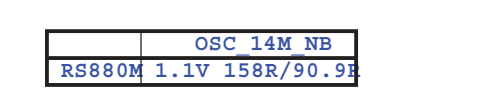
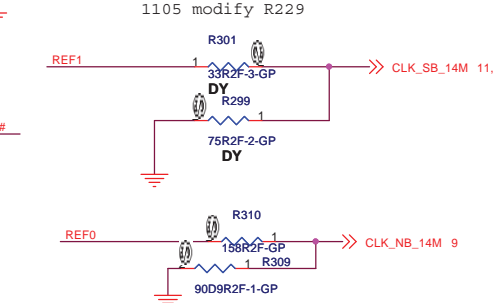
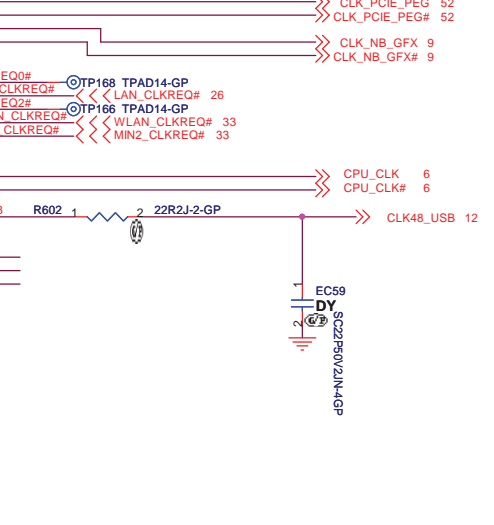
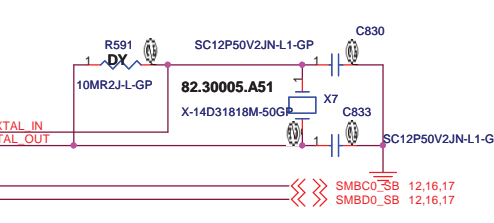
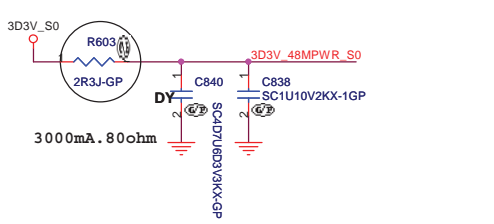
JE70-DN

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Reference	
Size A3	Document Number JE70-DN
Date: Thursday, November 19, 2009	Sheet 2 of 63



SEL_27	REF2	1*	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
SEL_SATA	REF1	0	100MHz differential spreading SRC clock
SEL_SATA	REF1	0*	100MHz differential spreading SRC clock
SEL_HTT66	REF0	1	66MHz 3.3V single ended HTT clock
SEL_HTT66	REF0	0*	100MHz differential HTT clock

CPU_CLK (200MHz)



OSC 14M NB	
RS880M	1.1V 158R/90.9

CLK_PCIE_PEG	1	EC62	SC22P50V2JN-4GP
CLK_PCIE_PEG#	DY	EC63	SC22P50V2JN-4GP
CLK_NB_GFX	DY	EC68	SC22P50V2JN-4GP
CLK_NB_GFX#	DY	EC64	SC22P50V2JN-4GP
CLK_PCIE_SB	DY	EC68	SC22P50V2JN-4GP
CLK_PCIE_SB#	DY	EC68	SC22P50V2JN-4GP
CLK_PCIE_LAN	DY	EC67	SC22P50V2JN-4GP
CLK_PCIE_LAN#	DY	EC68	SC22P50V2JN-4GP
CLK_NB_GPPSB	DY	EC71	SC22P50V2JN-4GP
CLK_NB_GPPSB#	DY	EC70	SC22P50V2JN-4GP
CLK_PCIE_MINI1	DY	EC73	SC22P50V2JN-4GP
CLK_PCIE_MINI1#	DY	EC72	SC22P50V2JN-4GP
CLK_PCIE_MINI2	DY	EC78	SC22P50V2JN-4GP
CLK_PCIE_MINI2#	DY	EC77	SC22P50V2JN-4GP
CPU_CLK	DY	EC75	SC22P50V2JN-4GP
CPU_CLK#	DY	EC74	SC22P50V2JN-4GP
CLK_NBHT_CLK	DY	EC79	SC22P50V2JN-4GP
CLK_NBHT_CLK#	DY	EC78	SC22P50V2JN-4GP
CLK_27M_VGA	DY	EC80	SC22P50V2JN-4GP

SB_1224 EMI

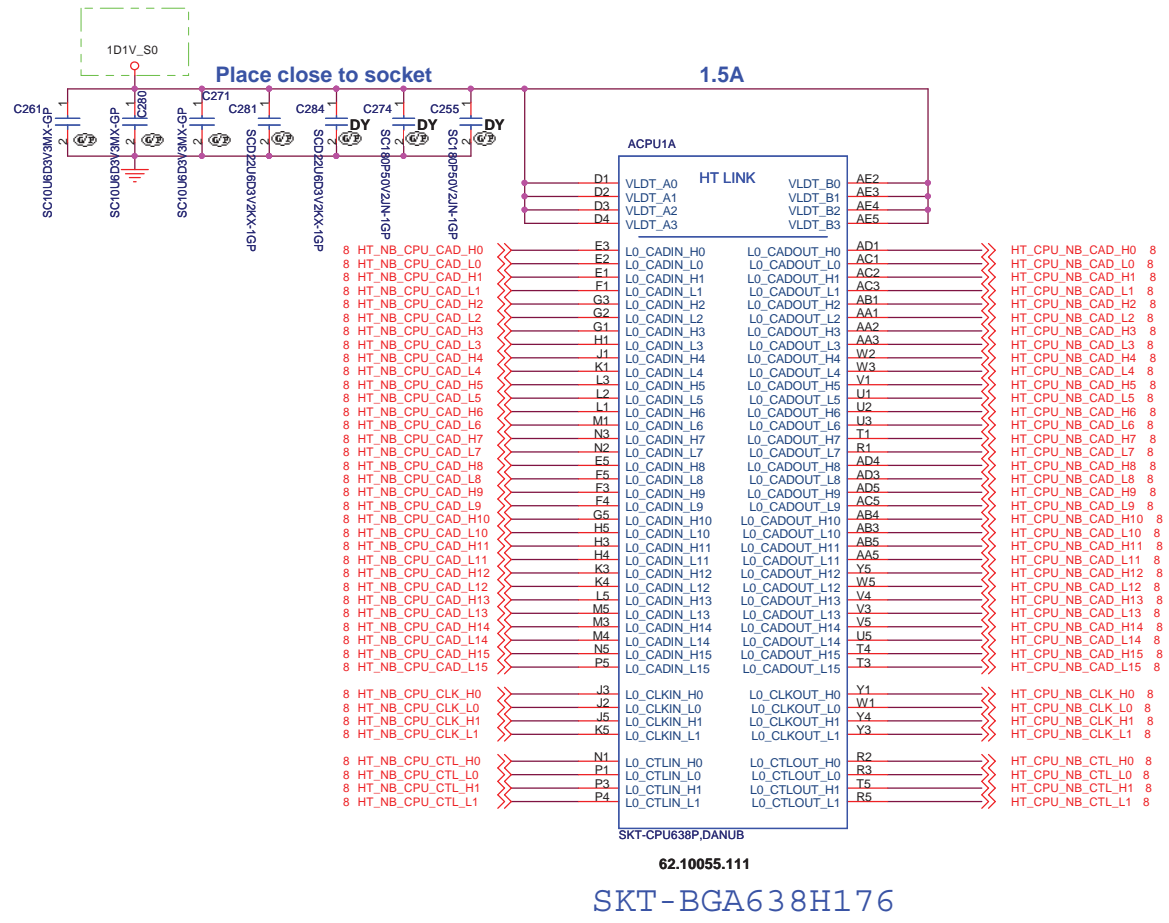
NB CLOCK INPUT TABLE

NB CLOCKS	RS880
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC
GPPSB_REFCLK	100M DIFF

JE70-DN

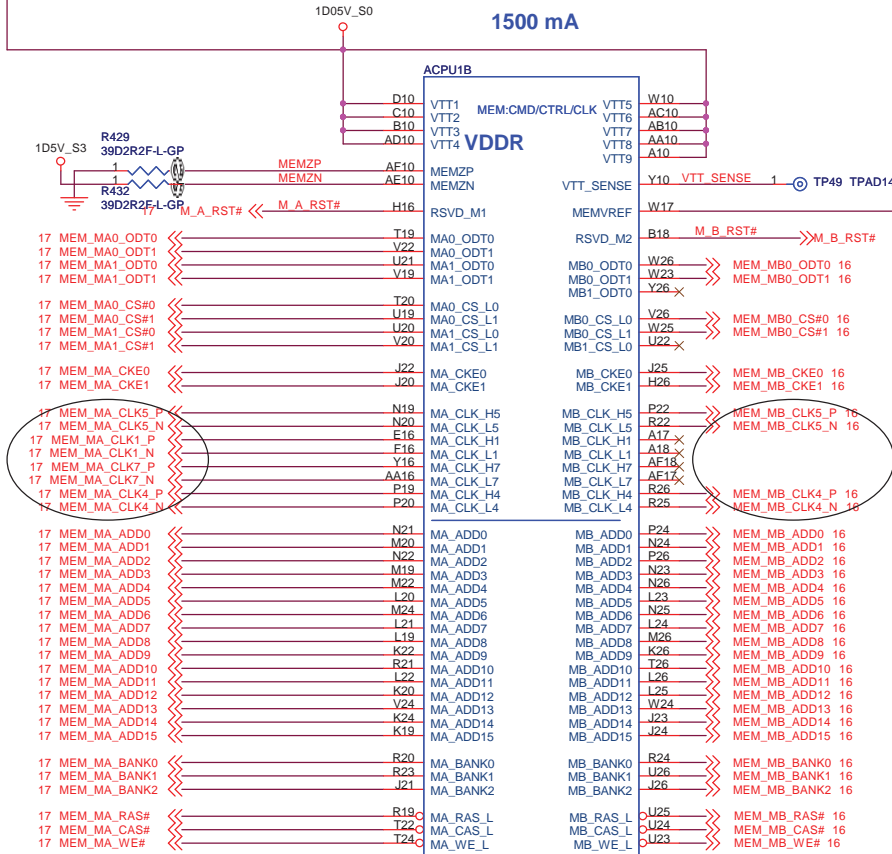
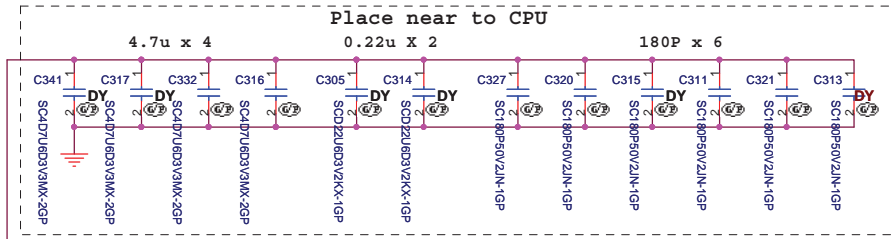
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Title			CLKGEN ICS9LPRS480		
Size	Document Number		Rev		
A3			JE70-DN	SB	
Date:	Monday, March 01, 2010	Sheet	3	of	63



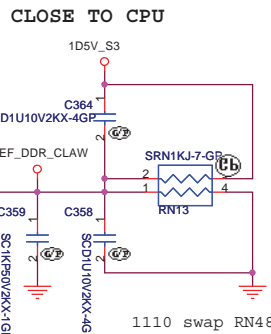
JE70-DN

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Title			
CPU HT LINK I/F (1/4)			
Size	Document Number		Rev
A3	JE70-DN		SB
Date: Monday, March 01, 2010			
Sheet		of	
4		63	

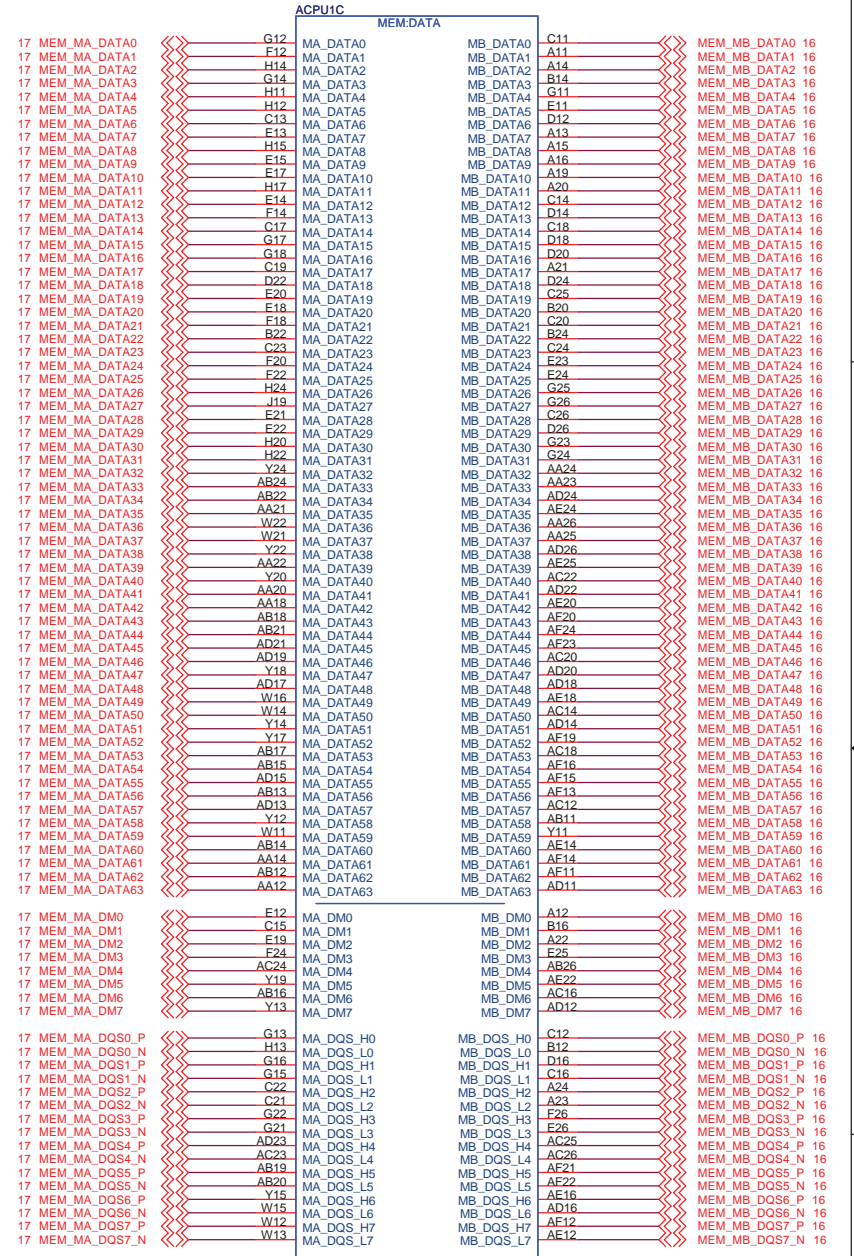


SKT-CPU638P,DANUB

62.10055.111



1110 swap RN48

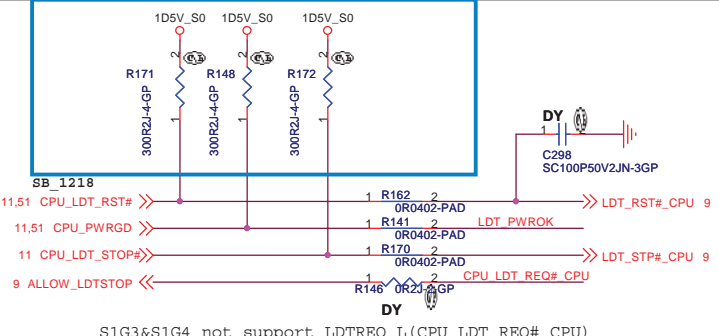


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JE70-DN

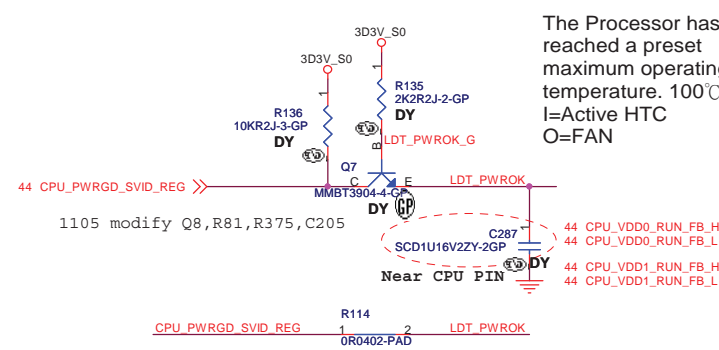
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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hstchih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU DDR (2/4)		
Size	Document Number	Rev
A3	JE70-DN	SB
Date:	Monday, March 01, 2010	Sheet 5 of 63

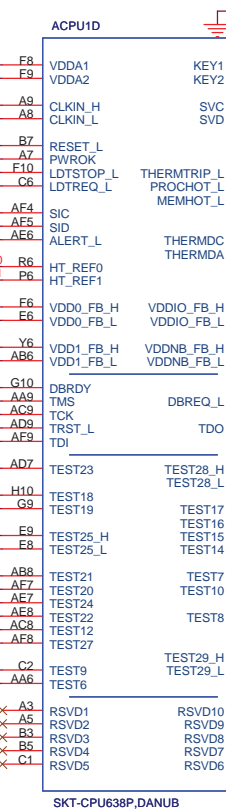
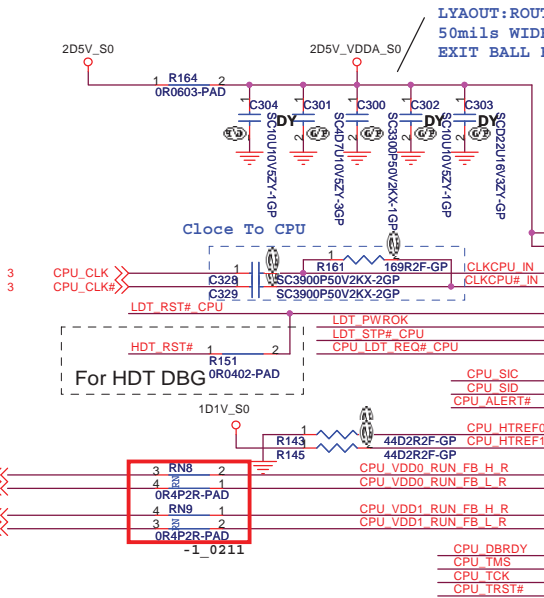


IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LAYOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

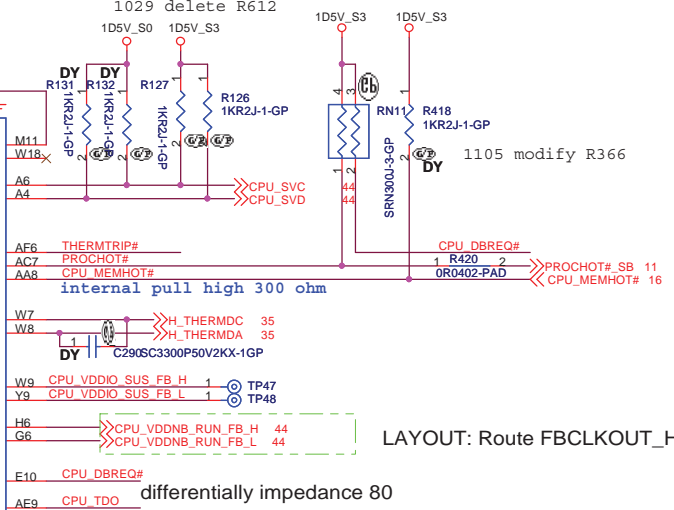


The Processor has reached a preset maximum operating temperature. 100°C
I=Active HTC
O= FAN

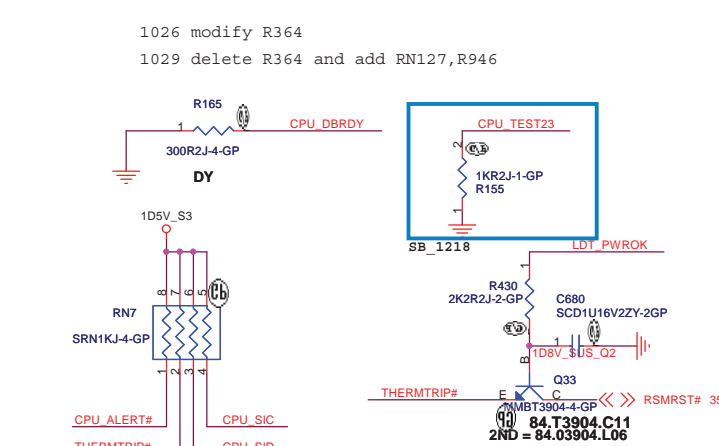


1026 modify RN84,R612,R611

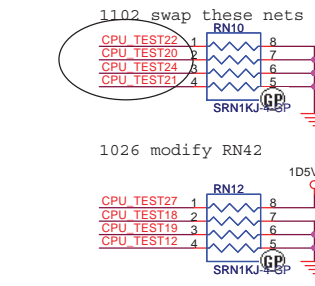
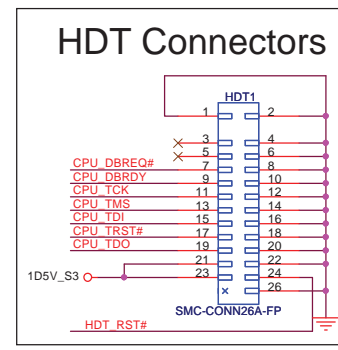
1029 delete R612



LAYOUT: Route FBCLKOUT_H/L



CPU exceeds to 125°C



JE70-DN

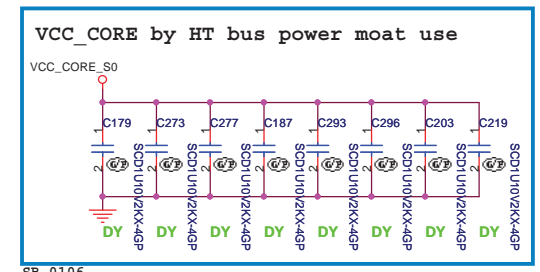
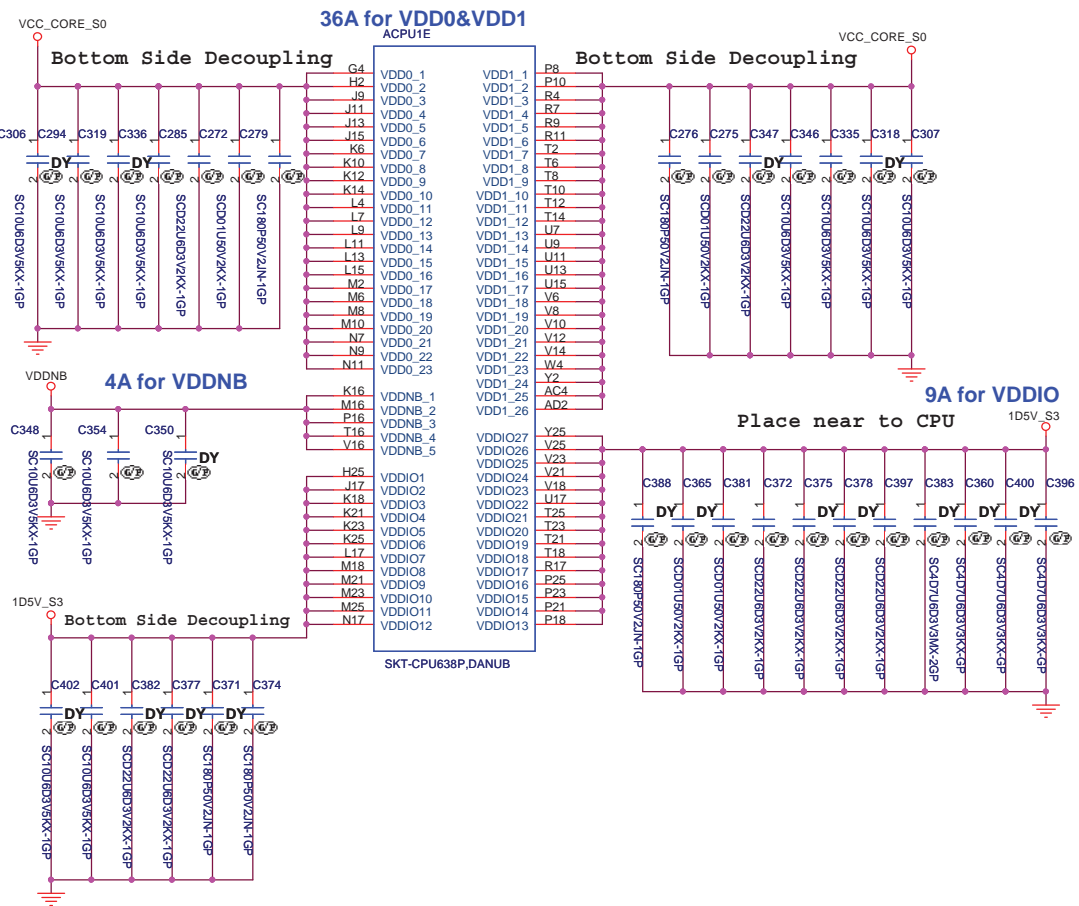
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_Control&Debug_(3/4)**

Size: A3	Document Number: JE70-DN	Rev: SB
Date: Tuesday, February 23, 2010	Sheet: 6 of 63	

ACPU1F		
AA4	VSS1	VSS66
AA11	VSS2	VSS67
AA13	VSS3	VSS68
AA15	VSS4	VSS69
AA17	VSS5	VSS70
AA19	VSS6	VSS71
AB2	VSS7	VSS72
AB7	VSS8	VSS73
AB9	VSS9	VSS74
AB23	VSS10	VSS75
AB25	VSS11	VSS76
AC11	VSS12	VSS77
AC13	VSS13	VSS78
AC15	VSS14	VSS79
AC17	VSS15	VSS80
AC19	VSS16	VSS81
AC21	VSS17	VSS82
AD6	VSS18	VSS83
AD8	VSS19	VSS84
AD25	VSS20	VSS85
AE11	VSS21	VSS86
AE13	VSS22	VSS87
AE15	VSS23	VSS88
AE17	VSS24	VSS89
AE19	VSS25	VSS90
AE21	VSS26	VSS91
AE23	VSS27	VSS92
B4	VSS28	VSS93
B6	VSS29	VSS94
B8	VSS30	VSS95
B9	VSS31	VSS96
B11	VSS32	VSS97
B13	VSS33	VSS98
B15	VSS34	VSS99
B17	VSS35	VSS100
B19	VSS36	VSS101
B21	VSS37	VSS102
B23	VSS38	VSS103
B25	VSS39	VSS104
D6	VSS40	VSS105
D9	VSS41	VSS106
D11	VSS42	VSS107
D13	VSS43	VSS108
D15	VSS44	VSS109
D17	VSS45	VSS110
D19	VSS46	VSS111
D21	VSS47	VSS112
D23	VSS48	VSS113
D25	VSS49	VSS114
E4	VSS50	VSS115
F2	VSS51	VSS116
F11	VSS52	VSS117
F13	VSS53	VSS118
F15	VSS54	VSS119
F17	VSS55	VSS120
F19	VSS56	VSS121
F21	VSS57	VSS122
F23	VSS58	VSS123
F25	VSS59	VSS124
H7	VSS60	VSS125
H9	VSS61	VSS126
H21	VSS62	VSS127
H23	VSS63	VSS128
J4	VSS64	VSS129
	VSS65	VSS130

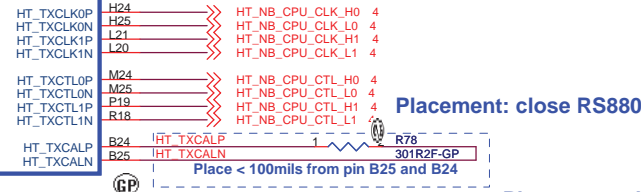
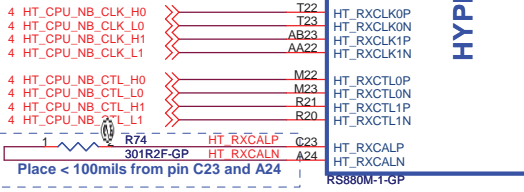
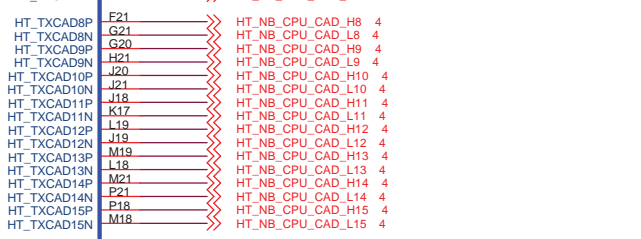
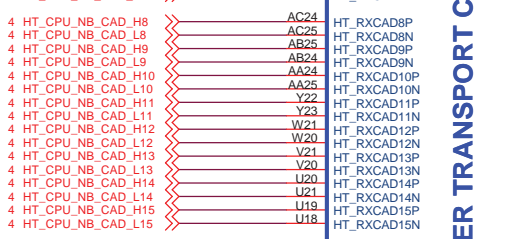
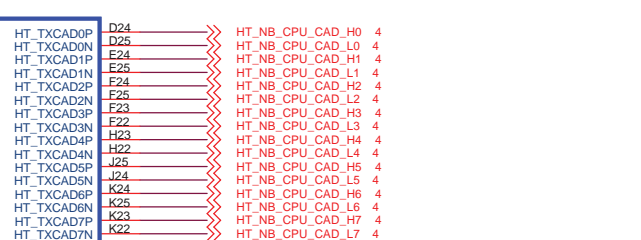
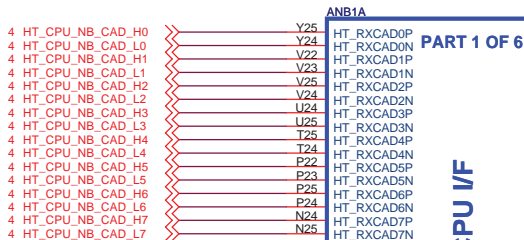
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SB_0106

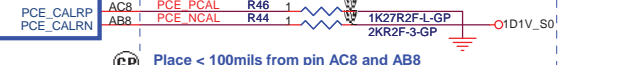
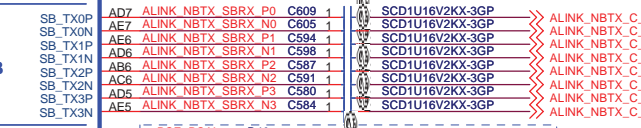
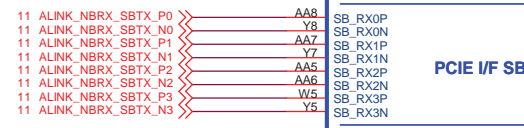
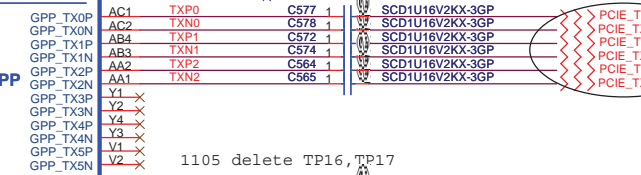
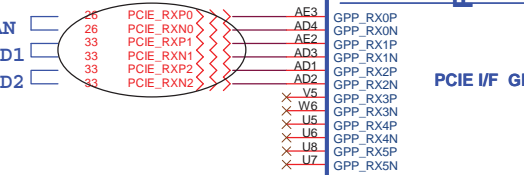
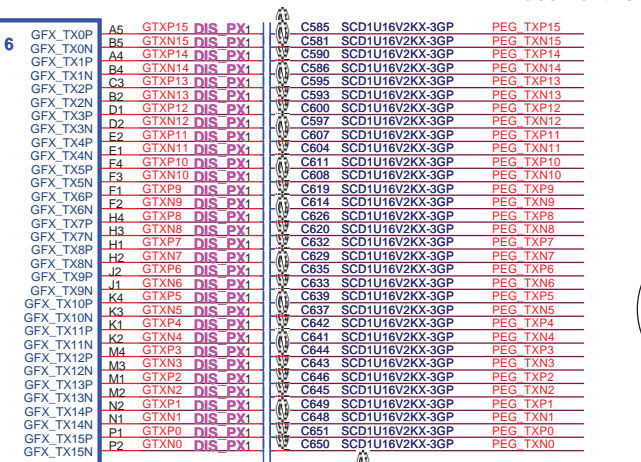
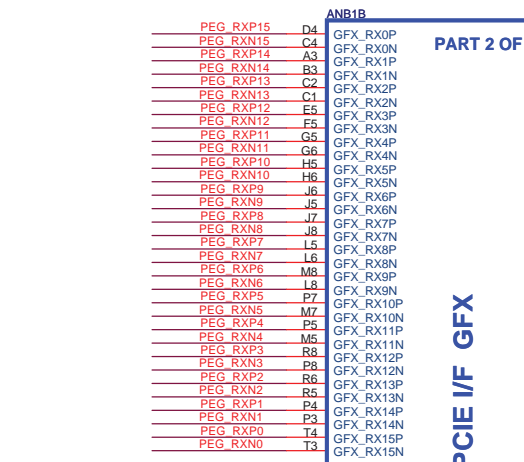
JE70-DN

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hstchih,		Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU_Power_(4/4)			
Size A3	Document Number	JE70-DN	
Date: Wednesday, January 06, 2010	Sheet 7	of	63
			Rev SB



Place < 100mils from pin C23 and A24

Place < 100mils from pin B25 and B24



PART 1 OF 6
HYPER TRANSPORT CPU I/F

PART 2 OF 6
PCIE I/F GFX

PCIE I/F SB

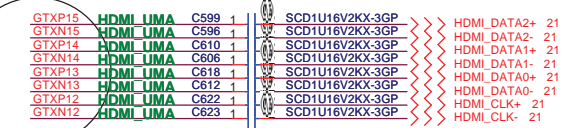
Placement: close RS880

Placement: close RS880

PEG_TXP[15.0] 52
PEG_TXN[15.0] 52

RS880M Display Port Support (muxed on GFX)

DP0	GFX_TX0, TX1, TX2, TX3, AUX0, HPD0
DP1	GFX_TX4, TX5, TX6, TX7, AUX1, HPD1



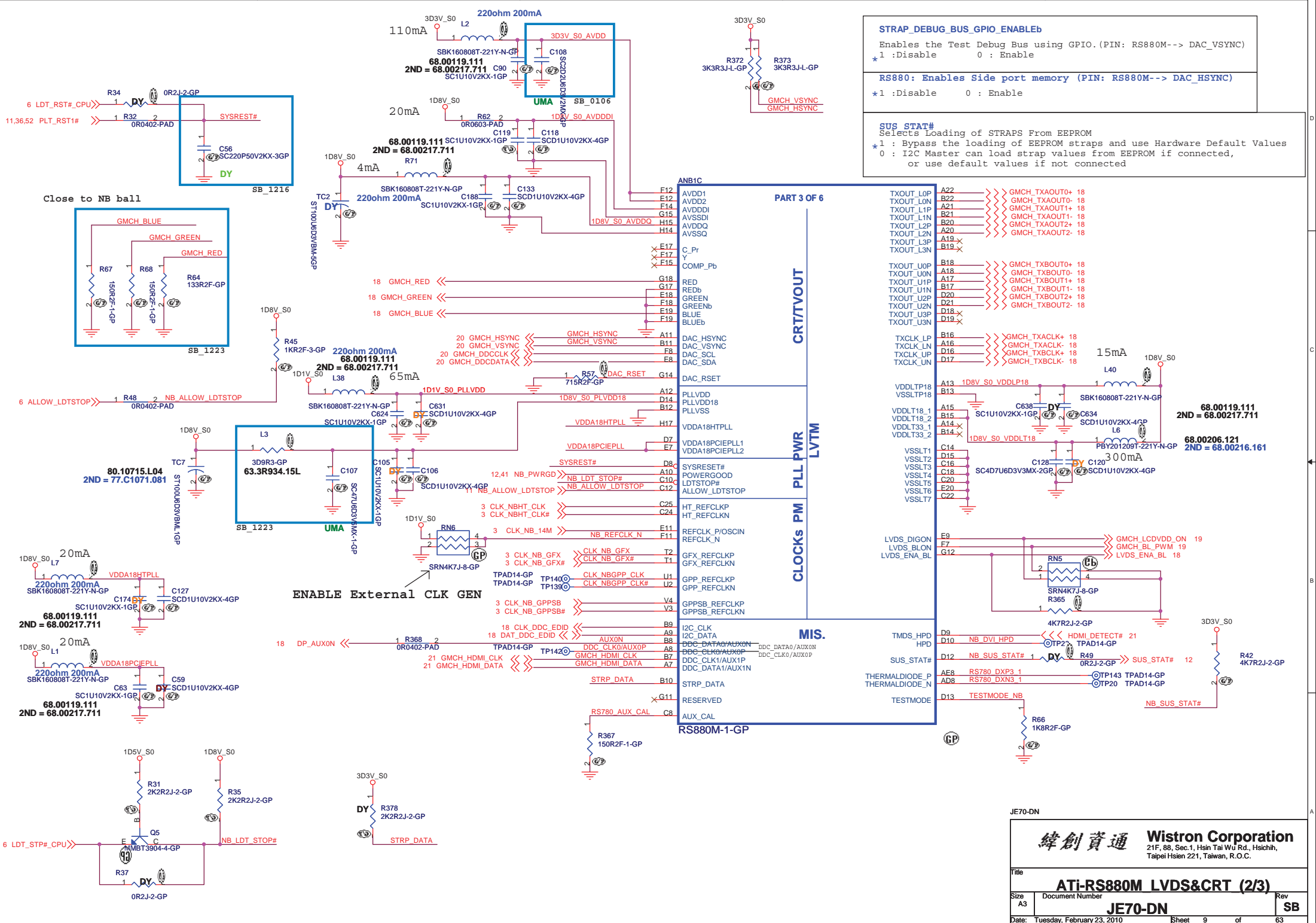
1105 delete TP16, TP17

JE70-DN

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ATI-RS880M_HT LINK&PCIE(1/3)

Size A3	Document Number	Rev SB
Date: Tuesday, February 23, 2010	Sheet 8 of 63	



STRAP_DEBUG_BUS_GPIO_ENABLEB
 Enables the Test Debug Bus using GPIO. (PIN: RS880M--> DAC_VSYNC)
 * 1 : Disable 0 : Enable

RS880: Enables Side port memory (PIN: RS880M--> DAC_HSYNC)
 * 1 : Disable 0 : Enable

SUS_STAT#
 Selects Loading of STRAPS from EEPROM
 * 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

CRITVOUT

TXOUT_L0P	A22	>>>	GMCH_TXAOUT0+ 18
TXOUT_L0N	B22	>>>	GMCH_TXAOUT0- 18
TXOUT_L1P	A21	>>>	GMCH_TXAOUT1+ 18
TXOUT_L1N	B21	>>>	GMCH_TXAOUT1- 18
TXOUT_L2P	B20	>>>	GMCH_TXAOUT2+ 18
TXOUT_L2N	A20	>>>	GMCH_TXAOUT2- 18
TXOUT_L3P	A19	>>>	GMCH_TXAOUT2+ 18
TXOUT_L3N	B19	>>>	GMCH_TXAOUT2- 18
TXOUT_U0P	B18	>>>	GMCH_TXBOUT0+ 18
TXOUT_U0N	A18	>>>	GMCH_TXBOUT0- 18
TXOUT_U1P	A17	>>>	GMCH_TXBOUT1+ 18
TXOUT_U1N	B17	>>>	GMCH_TXBOUT1- 18
TXOUT_U2P	D20	>>>	GMCH_TXBOUT2+ 18
TXOUT_U2N	D21	>>>	GMCH_TXBOUT2- 18
TXOUT_U3P	D18	>>>	GMCH_TXBOUT2+ 18
TXOUT_U3N	D19	>>>	GMCH_TXBOUT2- 18

PLL PWR

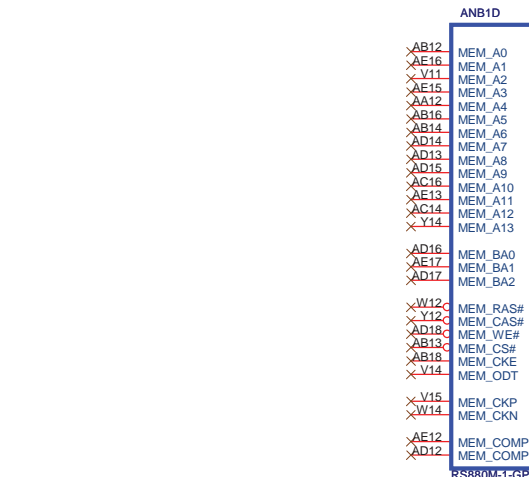
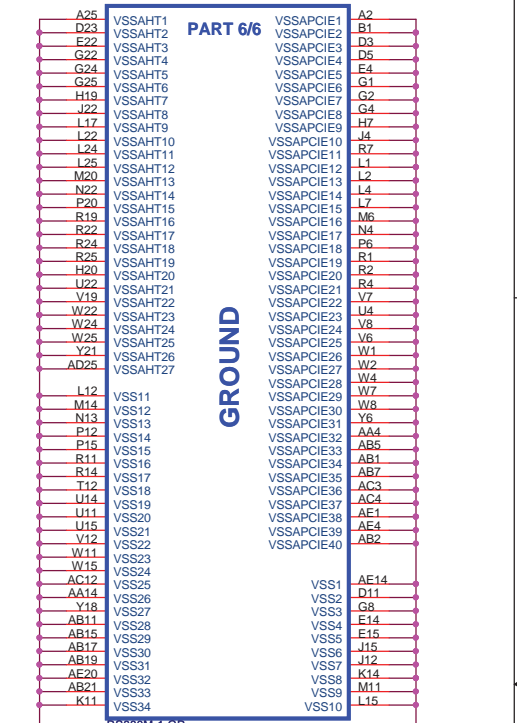
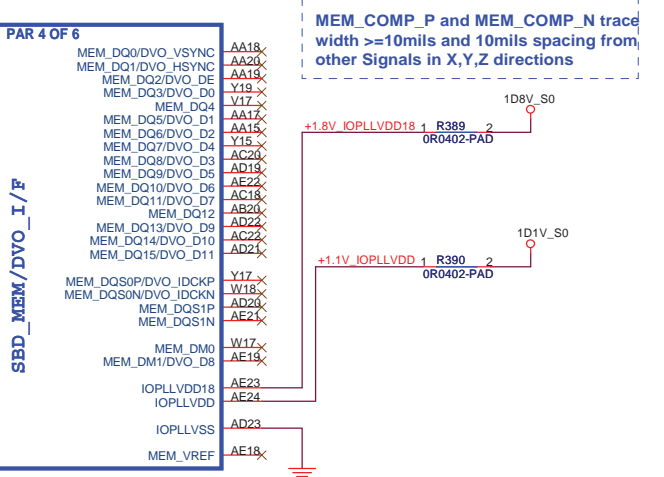
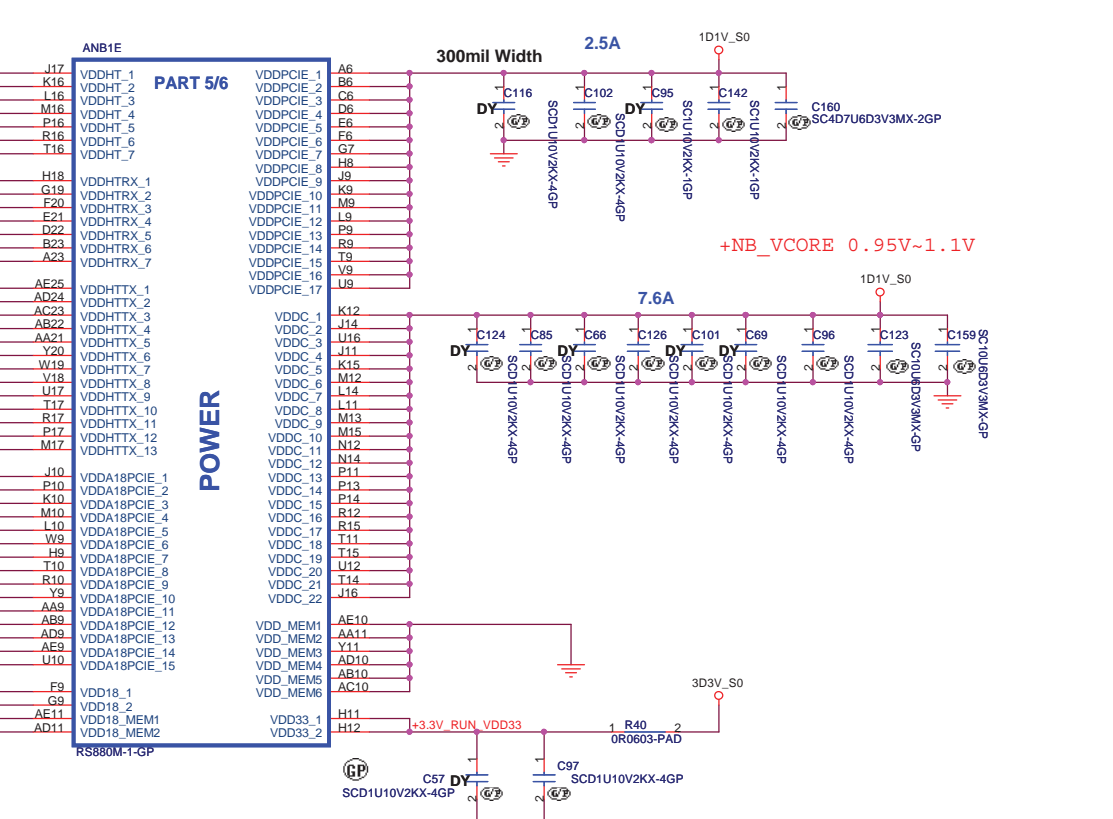
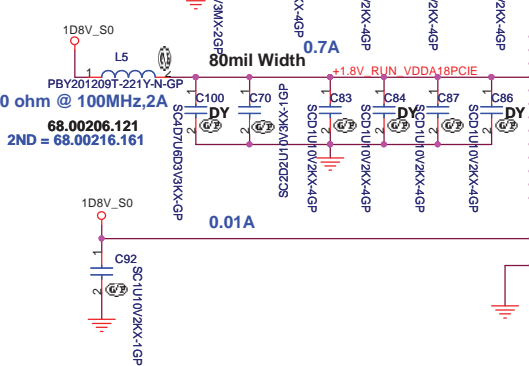
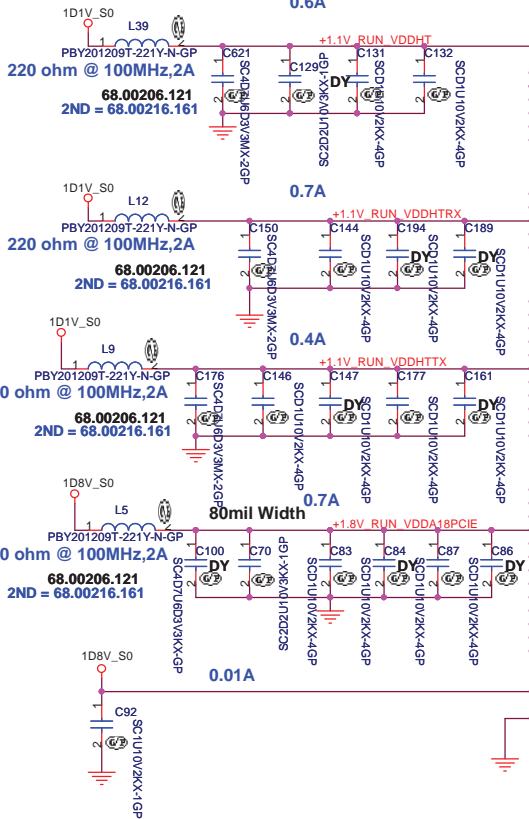
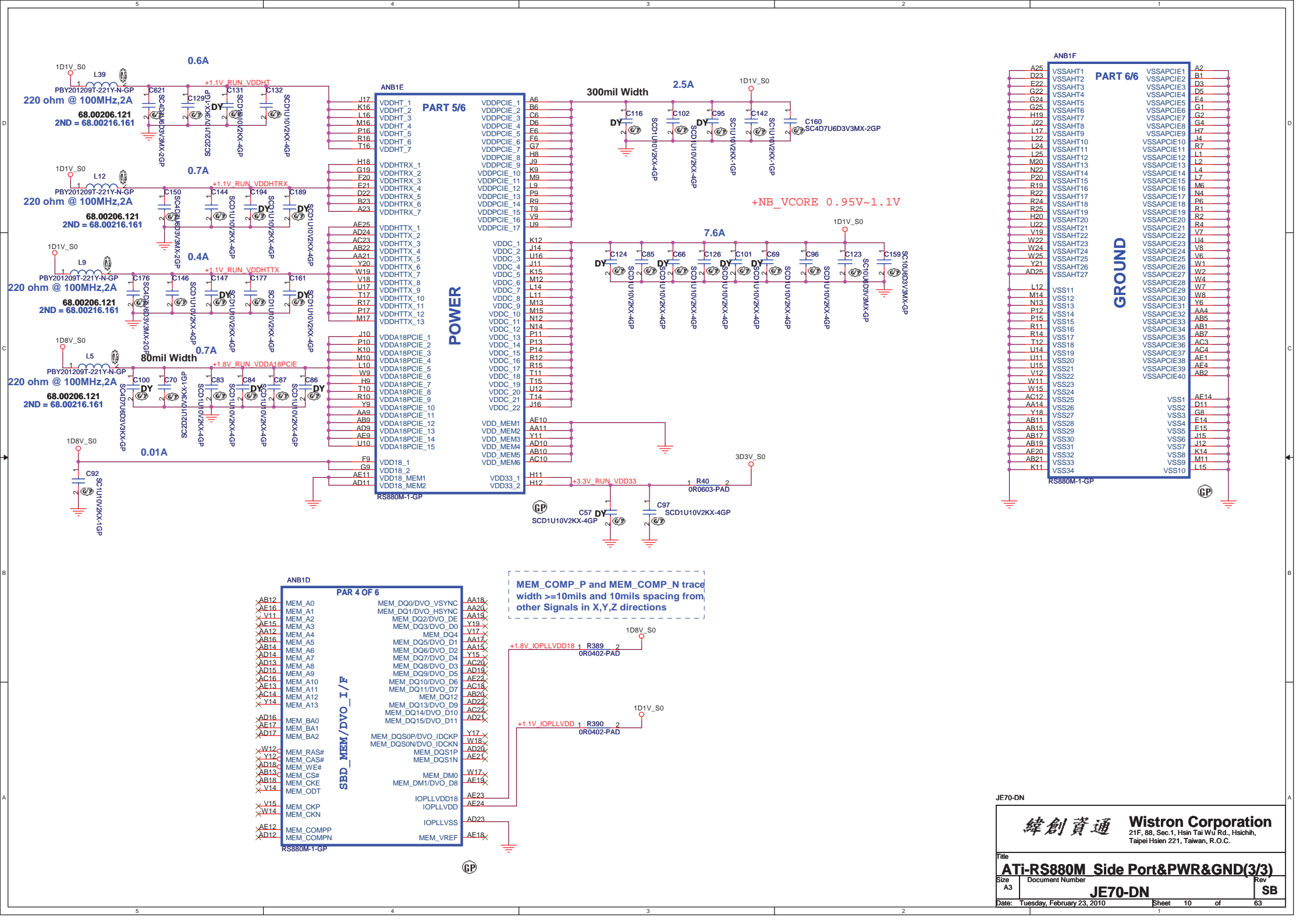
VDDLTP18	A13	>>>	1D8V_S0_VDDLTP18
VSSLTP18	B13	>>>	1D8V_S0_VDDLTP18
VDDL18_1	A15	>>>	1D8V_S0_VDDLTP18
VDDL18_2	B15	>>>	1D8V_S0_VDDLTP18
VDDL33_1	A14	>>>	1D8V_S0_VDDLTP18
VDDL33_2	B14	>>>	1D8V_S0_VDDLTP18
VSSLT1	C14	>>>	1D8V_S0_VDDLTP18
VSSLT2	D15	>>>	1D8V_S0_VDDLTP18
VSSLT3	C16	>>>	1D8V_S0_VDDLTP18
VSSLT4	C18	>>>	1D8V_S0_VDDLTP18
VSSLT5	C20	>>>	1D8V_S0_VDDLTP18
VSSLT6	E20	>>>	1D8V_S0_VDDLTP18
VSSLT7	C22	>>>	1D8V_S0_VDDLTP18

CLOCKS PM

LVDS_DIGON	E9	>>>	GMCH_LCDVDD_ON 19
LVDS_BLON	F7	>>>	GMCH_BL_PWM 19
LVDS_ENA_BL	G12	>>>	LVDS_ENA_BL 18
TMDS_HPD	D9	>>>	NB_DVI_HPD
HPD	D10	>>>	NB_DVI_HPD
SUS_STAT#	D12	>>>	NB_SUS_STAT# 12
THERMALDIODE_P	AE8	>>>	RS780_DXP3_1
THERMALDIODE_N	AD8	>>>	RS780_DXP3_1
TESTMODE	D13	>>>	TESTMODE_NB

MIS.

I2C_CLK	B9	>>>	AUXON
I2C_DATA	A9	>>>	AUXON
DDC_CLK0/AUXON	B8	>>>	DDC_DATA0/AUXON
DDC_CLK1/AUXON	B7	>>>	DDC_DATA1/AUXON
DDC_CLK0/AUXON	B7	>>>	DDC_CLK0/AUXON
DDC_CLK1/AUXON	B7	>>>	DDC_CLK1/AUXON
STRP_DATA	B10	>>>	STRP_DATA
AUX_CAL	C8	>>>	RS780_AUX_CAL



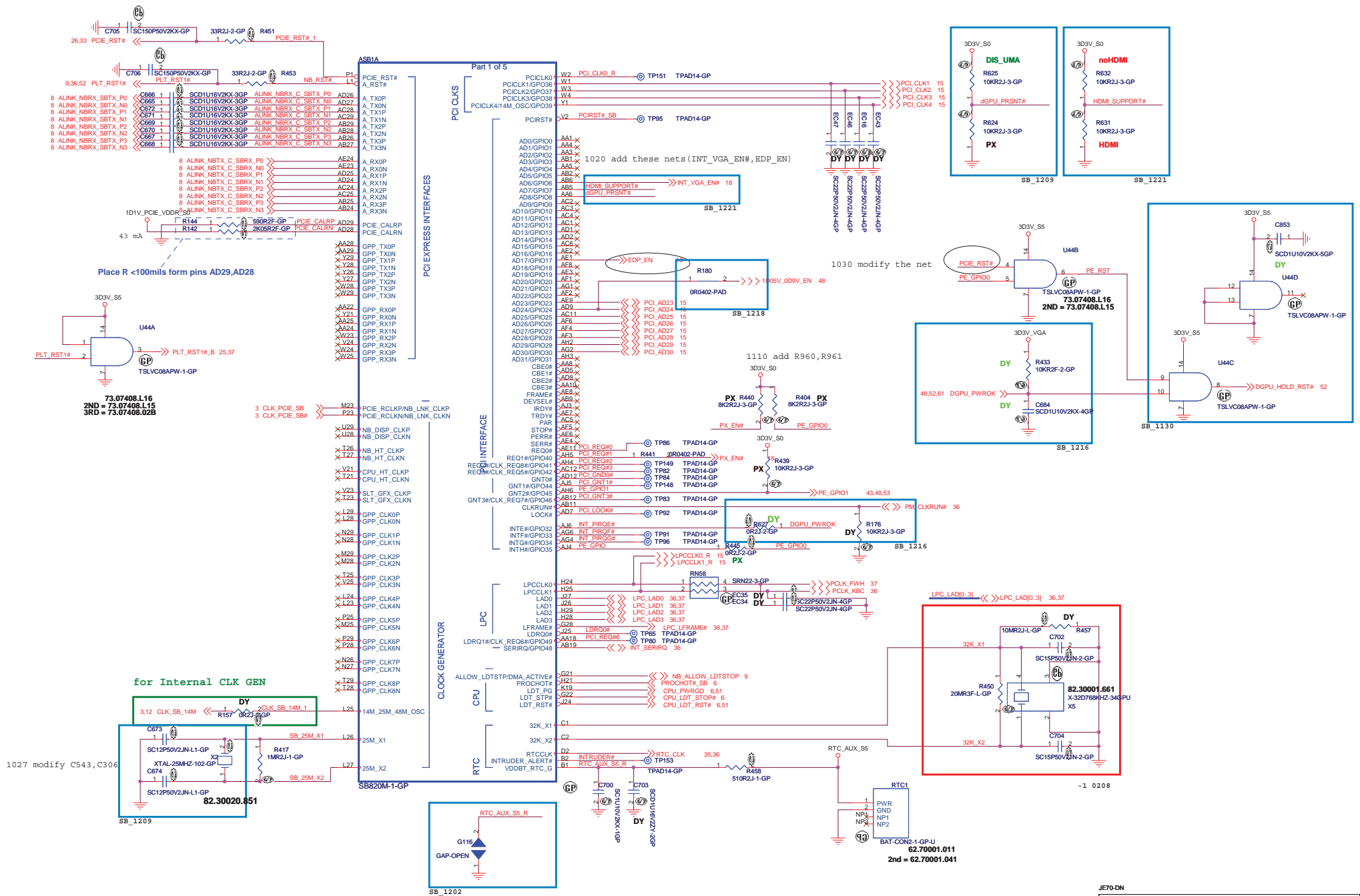
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Taipei Hsien 221, Taiwan, R.O.C.

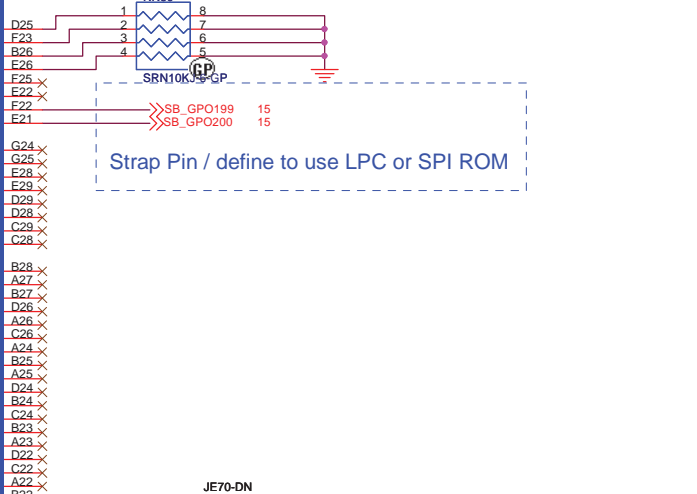
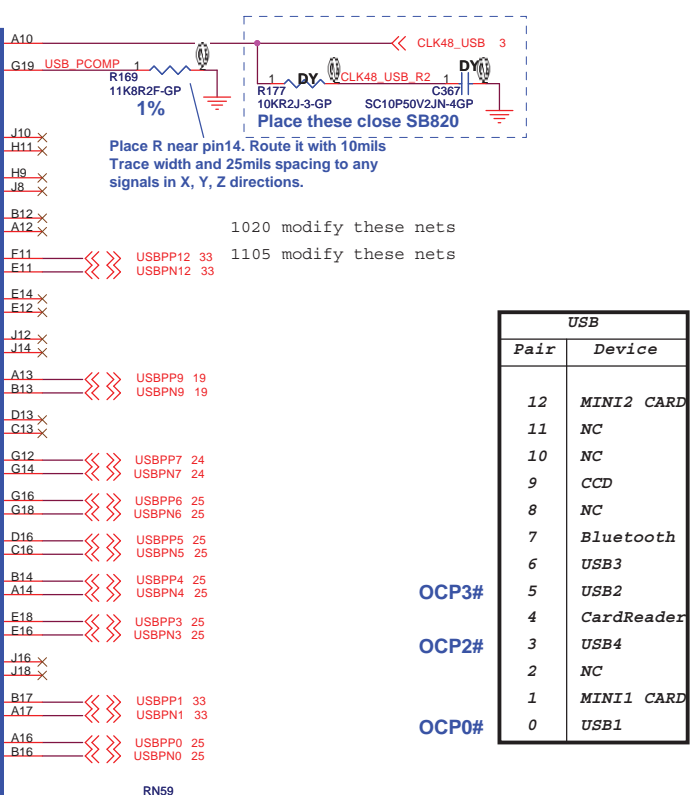
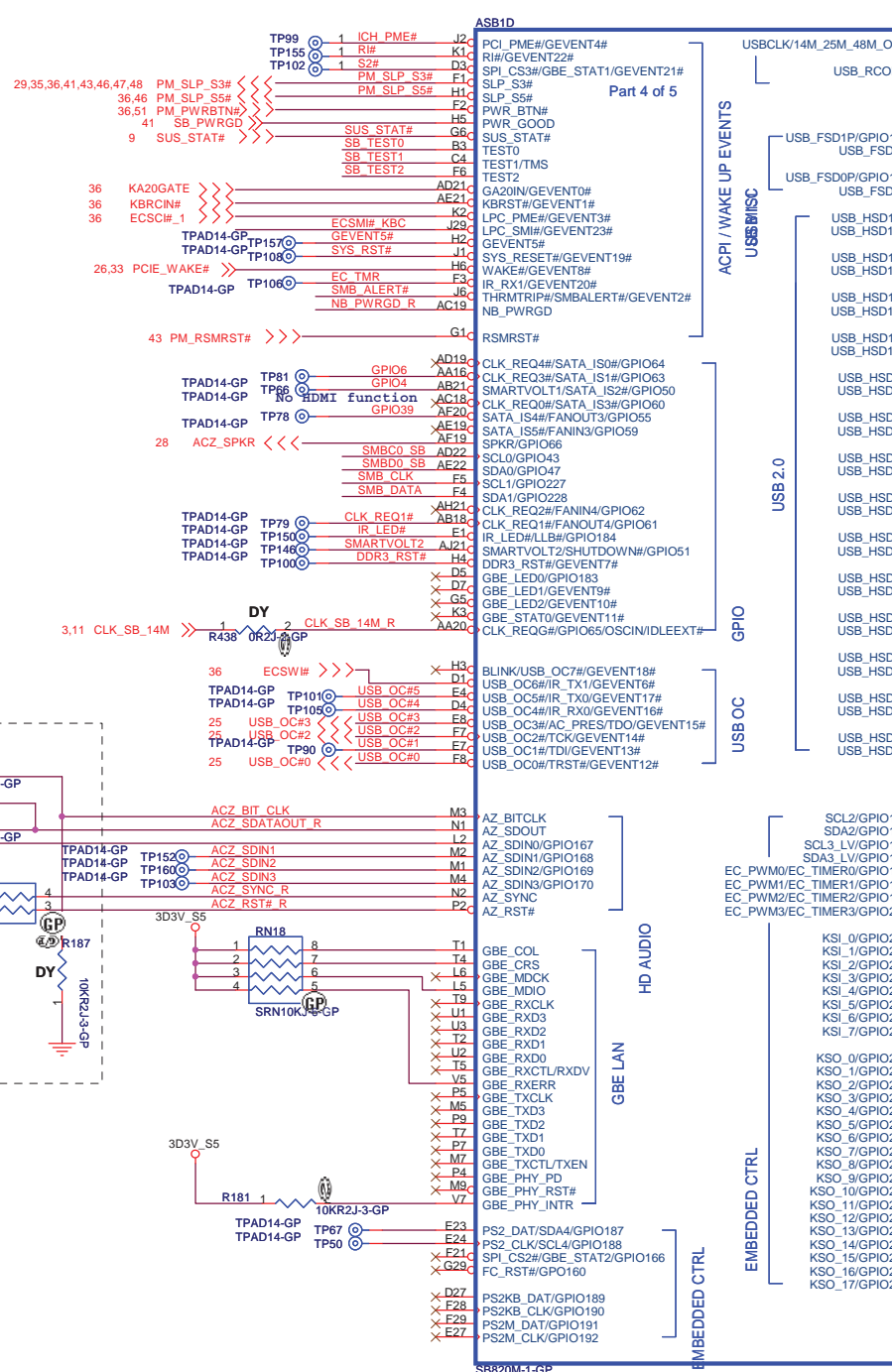
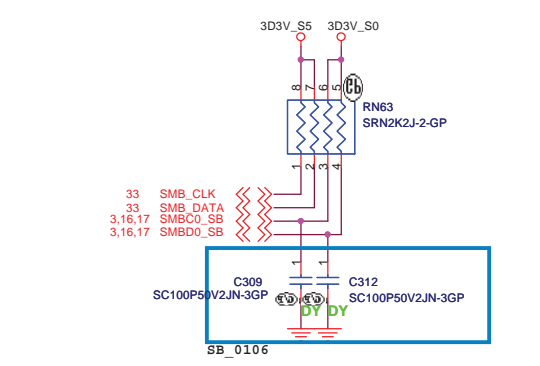
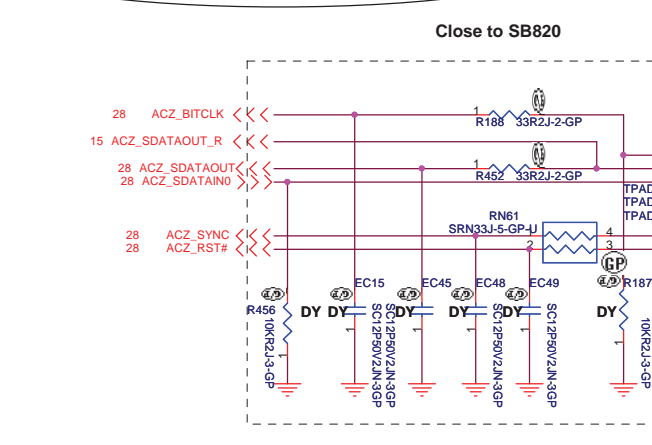
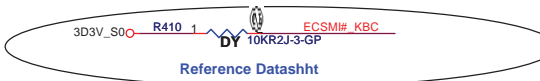
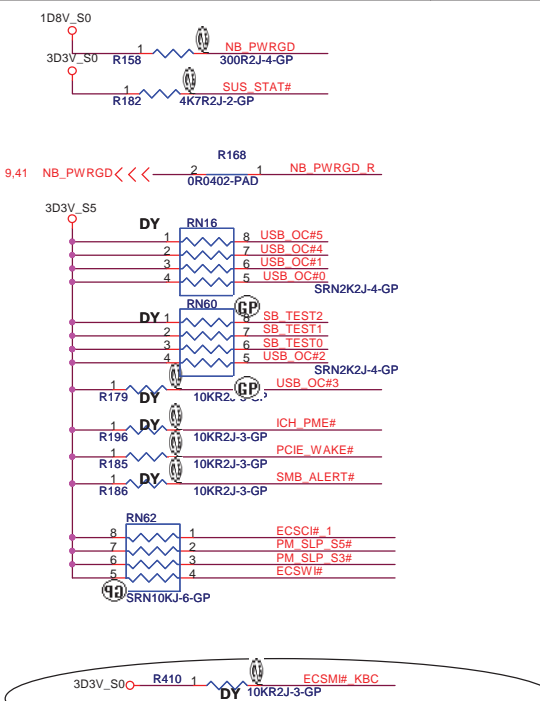
Title
ATI-RS880M Side Port&PWR&GND(3/3)

Size A3 Document Number **JE70-DN** Rev **SB**

Date: Tuesday, February 23, 2010 Sheet 10 of 63

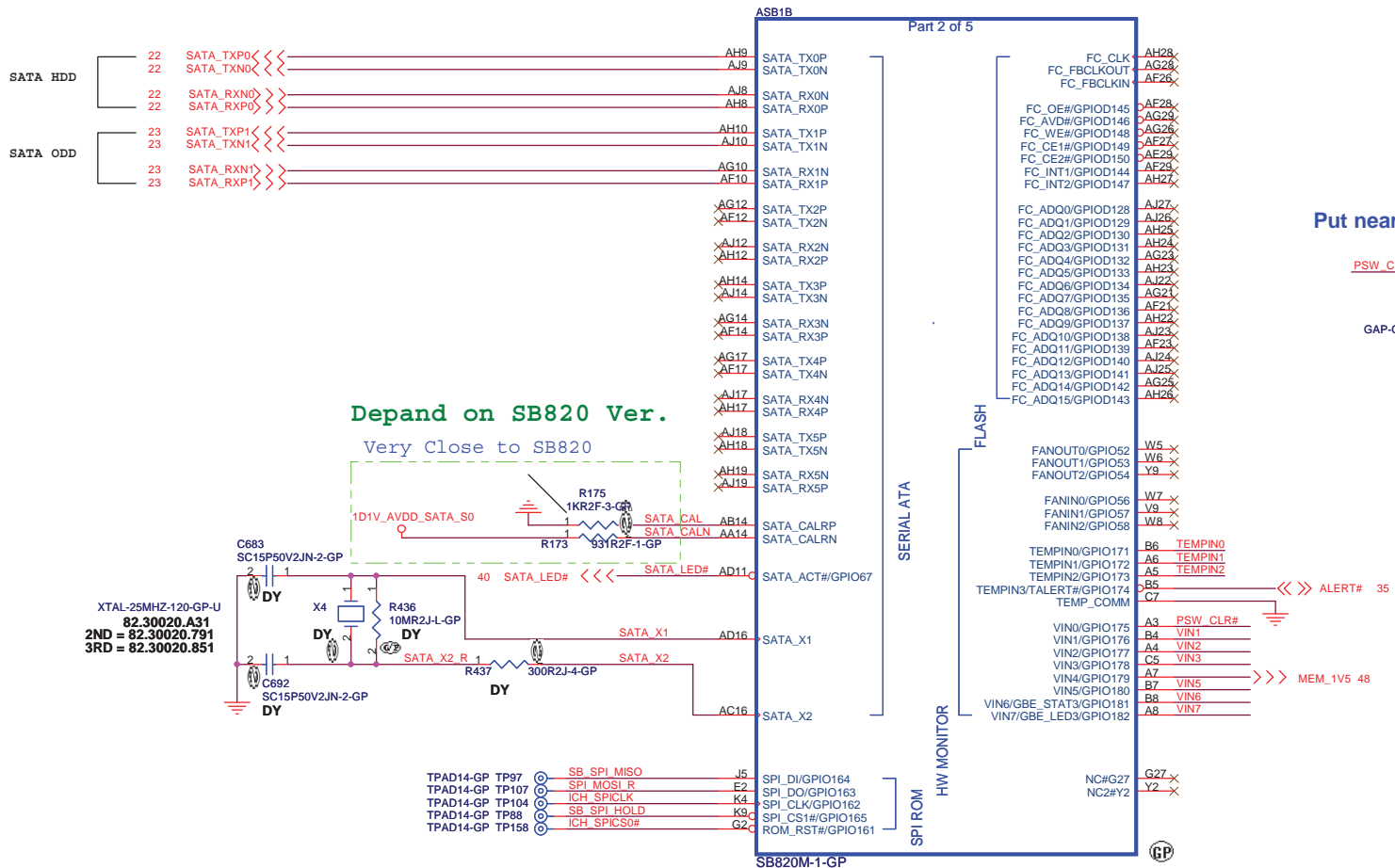


PX_EN : Power Xpress enable
 PE_GPI01 : use to turn on the power of Discrete VGA
 PE_GPI00 : use to reset the MXM module when enables Power Xpress



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ATI-SB820 USB&GPIO (2/5)
 JE70-DN
 Title: _____
 Size: A3 Document Number: _____ Rev: **SB**
 Date: Tuesday, February 23, 2010 Sheet 12 of 63

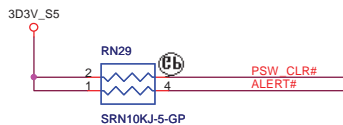
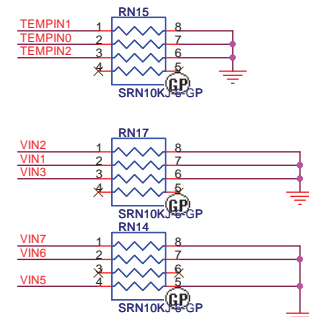
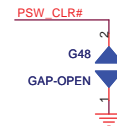


Depand on SB820 Ver.
Very Close to SB820

XTAL-25MHz-120-GP-U
82.30020.A31
2ND = 82.30020.791
3RD = 82.30020.851

TPAD14-GP	TP97	SB SPI_MISO	J5	SPI_DI#/GPIO164
TPAD14-GP	TP107	SPI_MOSI_R	F2	SPI_DO#/GPIO163
TPAD14-GP	TP104	ICH_SPICLK	K4	SPI_CLK#/GPIO162
TPAD14-GP	TP89	SB_SPI_HOLD	K9	SPI_CS1#/GPIO165
TPAD14-GP	TP158	ICH_SPICSO#	G2	ROM_RST#/GPIO161

Put near Dimm Door



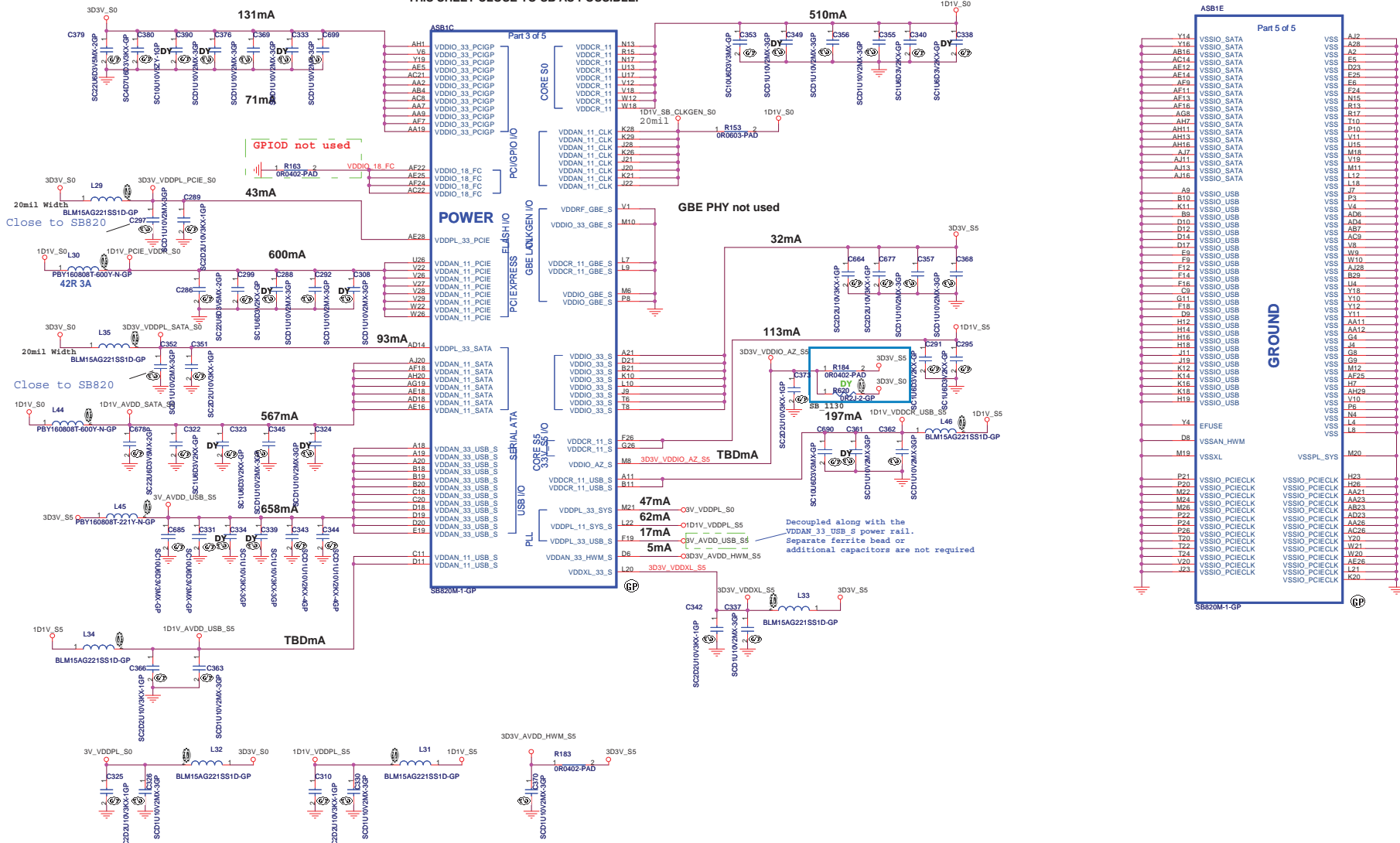
1029 modify the net (SATA_LED#)



JE70-DN

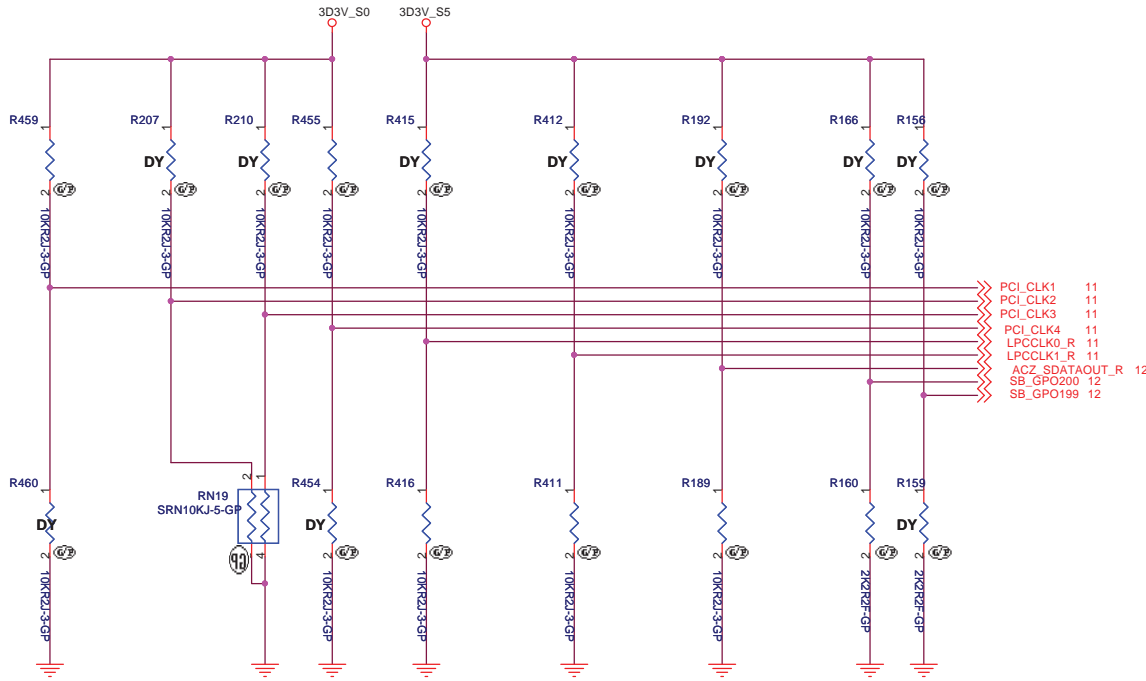
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ATI-SB820 SATA-IDE (3/5)			
Size	Document Number	Rev	SB
A3	JE70-DN		
Date:	Tuesday, February 23, 2010	Sheet	13 of 63

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



1118 modify R412,R411

	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200	GPIO199
PULL HIGH	ALLOW PCIe Gen2 <small>DEFAULT</small>	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE <small>DEFAULT</small>	EC ENABLED	CLKGEN ENABLED	LOW POWER MODE	H,H = Reserved H,L = SPI ROM	
PULL LOW	FORCE PCIe Gen1	Watchdog Timer Disabled <small>DEFAULT</small>	IGNORE DEBUG STRAP <small>DEFAULT</small>	FUSION CLOCK MODE	EC DISABLED <small>DEFAULT</small>	CLKGEN DISABLED <small>DEFAULT</small>	PERFORMANCE MODE <small>DEFAULT</small>	L,H = LPC ROM (Default) L,L = FWH ROM	

NOTE: SB820 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS

TPAD14-GP TP89	PCI_AD23	11
TPAD14-GP TP87	PCI_AD24	11
TPAD14-GP TP85	PCI_AD25	11
TPAD14-GP TP93	PCI_AD26	11
TPAD14-GP TP98	PCI_AD27	11
TPAD14-GP TP156	PCI_AD28	11
TPAD14-GP TP159	PCI_AD29	11
TPAD14-GP TP154	PCI_AD30	11

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL <small>DEFAULT</small>	DISABLE ILA AUTORUN <small>DEFAULT</small>	USE FC PLL <small>DEFAULT</small>	USE DEFAULT PCIe STRAPS <small>DEFAULT</small>	DISABLE PCI MEM BOOT <small>DEFAULT</small>
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT

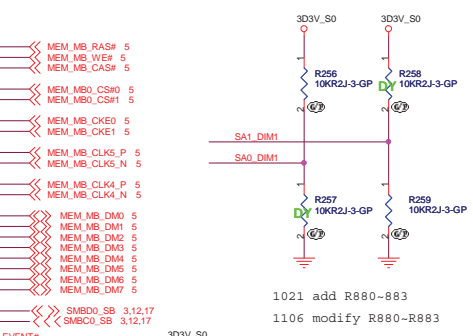
Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

JE70-DN

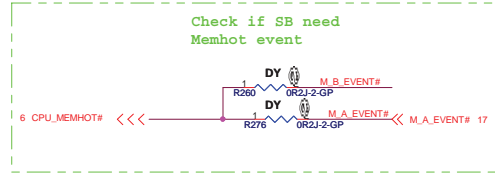
Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
ATi-SB820 STRAPPING (5/5)	
Size	Document Number
A3	JE70-DN
Date: Tuesday, February 23, 2010	Sheet 15 of 63
Rev SB	

ADM1		ADM1	
5 MEM_MB_ADD0	96	A0	NP1
5 MEM_MB_ADD1	97	A1	NP2
5 MEM_MB_ADD2	98	A2	
5 MEM_MB_ADD3	99	A3	RAS#
5 MEM_MB_ADD4	100	A4	WE#
5 MEM_MB_ADD5	101	A5	CAS#
5 MEM_MB_ADD6	102	A6	
5 MEM_MB_ADD7	103	A7	CS0#
5 MEM_MB_ADD8	104	A8	CS1#
5 MEM_MB_ADD9	105	A9	
5 MEM_MB_ADD10	106	A10/AP	CKE0#
5 MEM_MB_ADD11	107	A11	CKE1#
5 MEM_MB_ADD12	108	A12	
5 MEM_MB_ADD13	109	A13	CK0#
5 MEM_MB_ADD14	110	A14	CK1#
5 MEM_MB_ADD15	111	A15	CK1#
5 MEM_MB_BANK2	112	A16/BA2	CK1#
	113		
5 MEM_MB_BANK0	114	BA0	DM0
5 MEM_MB_BANK1	115	BA1	DM1
	116		
5 MEM_MB_DATA0	117	D00	DM2
5 MEM_MB_DATA1	118	D01	DM2
5 MEM_MB_DATA2	119	D02	DM3
5 MEM_MB_DATA3	120	D03	DM4
5 MEM_MB_DATA4	121	D04	DM4
5 MEM_MB_DATA5	122	D05	DM5
5 MEM_MB_DATA6	123	D06	DM6
5 MEM_MB_DATA7	124	D07	DM7
5 MEM_MB_DATA8	125	D08	DM7
5 MEM_MB_DATA9	126	D09	
5 MEM_MB_DATA10	127	D10	
5 MEM_MB_DATA11	128	D11	
5 MEM_MB_DATA12	129	D12	
5 MEM_MB_DATA13	130	D13	
5 MEM_MB_DATA14	131	D14	
5 MEM_MB_DATA15	132	D15	
5 MEM_MB_DATA16	133	D16	
5 MEM_MB_DATA17	134	D17	
5 MEM_MB_DATA18	135	D18	
5 MEM_MB_DATA19	136	D19	
5 MEM_MB_DATA20	137	D20	
5 MEM_MB_DATA21	138	D21	
5 MEM_MB_DATA22	139	D22	
5 MEM_MB_DATA23	140	D23	
5 MEM_MB_DATA24	141	D24	
5 MEM_MB_DATA25	142	D25	
5 MEM_MB_DATA26	143	D26	
5 MEM_MB_DATA27	144	D27	
5 MEM_MB_DATA28	145	D28	
5 MEM_MB_DATA29	146	D29	
5 MEM_MB_DATA30	147	D30	
5 MEM_MB_DATA31	148	D31	
5 MEM_MB_DATA32	149	D32	
5 MEM_MB_DATA33	150	D33	
5 MEM_MB_DATA34	151	D34	
5 MEM_MB_DATA35	152	D35	
5 MEM_MB_DATA36	153	D36	
5 MEM_MB_DATA37	154	D37	
5 MEM_MB_DATA38	155	D38	
5 MEM_MB_DATA39	156	D39	
5 MEM_MB_DATA40	157	D40	
5 MEM_MB_DATA41	158	D41	
5 MEM_MB_DATA42	159	D42	
5 MEM_MB_DATA43	160	D43	
5 MEM_MB_DATA44	161	D44	
5 MEM_MB_DATA45	162	D45	
5 MEM_MB_DATA46	163	D46	
5 MEM_MB_DATA47	164	D47	
5 MEM_MB_DATA48	165	D48	
5 MEM_MB_DATA49	166	D49	
5 MEM_MB_DATA50	167	D50	
5 MEM_MB_DATA51	168	D51	
5 MEM_MB_DATA52	169	D52	
5 MEM_MB_DATA53	170	D53	
5 MEM_MB_DATA54	171	D54	
5 MEM_MB_DATA55	172	D55	
5 MEM_MB_DATA56	173	D56	
5 MEM_MB_DATA57	174	D57	
5 MEM_MB_DATA58	175	D58	
5 MEM_MB_DATA59	176	D59	
5 MEM_MB_DATA60	177	D60	
5 MEM_MB_DATA61	178	D61	
5 MEM_MB_DATA62	179	D62	
5 MEM_MB_DATA63	180	D63	
	181		
5 MEM_MB_DQS0_N	182	DQS0#	VSS
5 MEM_MB_DQS1_N	183	DQS1#	VSS
5 MEM_MB_DQS2_N	184	DQS2#	VSS
5 MEM_MB_DQS3_N	185	DQS3#	VSS
5 MEM_MB_DQS4_N	186	DQS4#	VSS
5 MEM_MB_DQS5_N	187	DQS5#	VSS
5 MEM_MB_DQS6_N	188	DQS6#	VSS
5 MEM_MB_DQS7_N	189	DQS7#	VSS
	190		
5 MEM_MB_DQS0_F	191	DQS0	VSS
5 MEM_MB_DQS1_F	192	DQS1	VSS
5 MEM_MB_DQS2_F	193	DQS2	VSS
5 MEM_MB_DQS3_F	194	DQS3	VSS
5 MEM_MB_DQS4_F	195	DQS4	VSS
5 MEM_MB_DQS5_F	196	DQS5	VSS
5 MEM_MB_DQS6_F	197	DQS6	VSS
5 MEM_MB_DQS7_F	198	DQS7	VSS
	199		
5 MEM_MB_ODT0	200	ODT0	VSS
5 MEM_MB_ODT1	201	ODT1	VSS
	202		
	203		
	204		
	205		
	206		

REVERSE TYPE

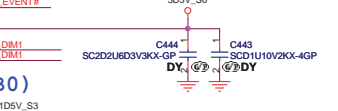


Note:
If SA0_DIMM0 = 1, SA1_DIMM0 = 0
SO-DIMMA SPD Address is
SO-DIMMA TS Address is



1021 add R880-883
1106 modify R880-R883

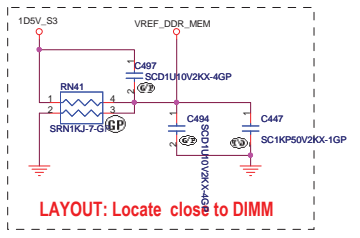
1029 delete C338,C331



(B0)

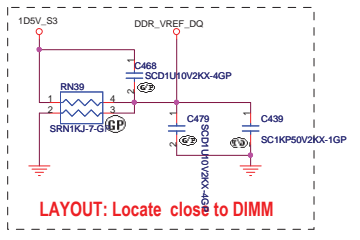


VREF_DDR_MEM



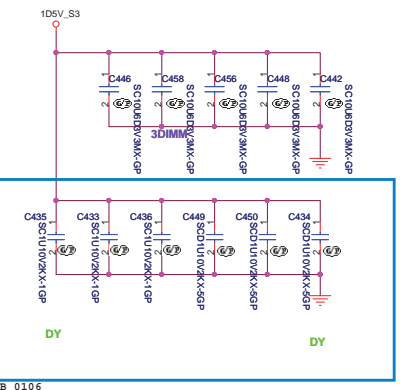
LAYOUT: Locate close to DIMM

DDR_VREF_DQ

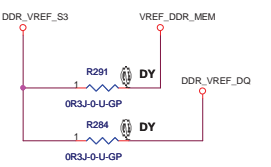


LAYOUT: Locate close to DIMM

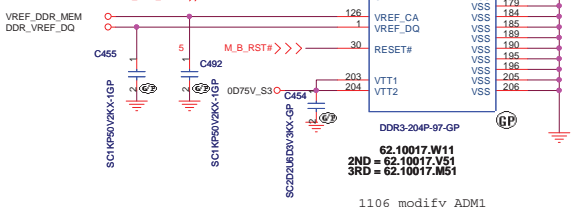
SODIMM A DECOUPLING



Layout Note:
Place these Caps near
SO-DIMMA0.



1029 add R934,R935
1105 modify R934,R935



1106 modify ADM1

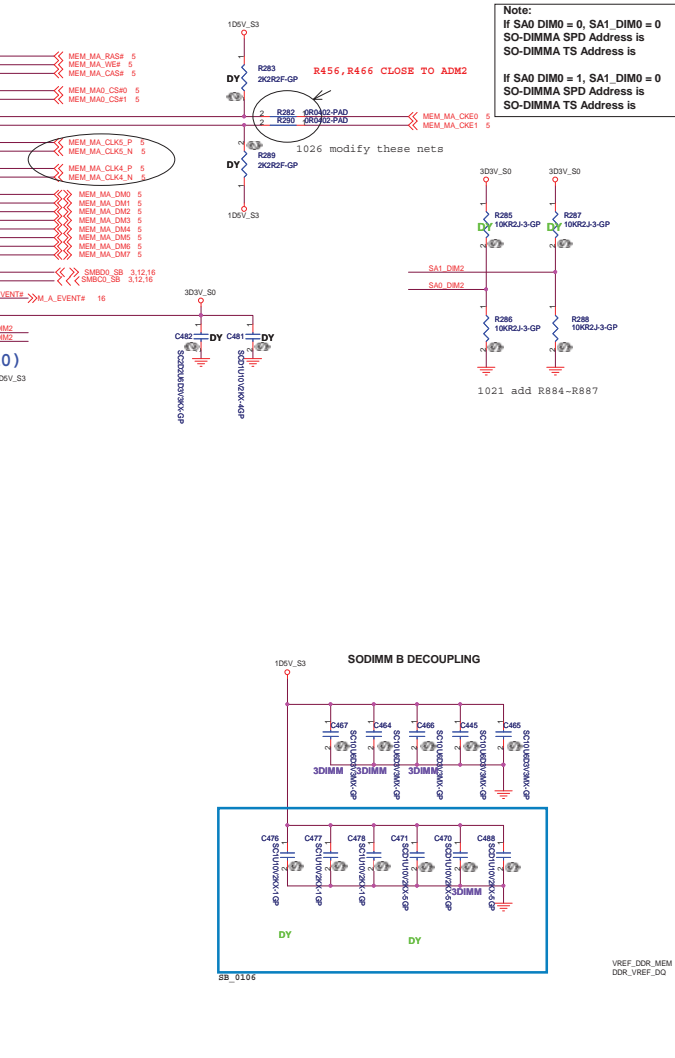
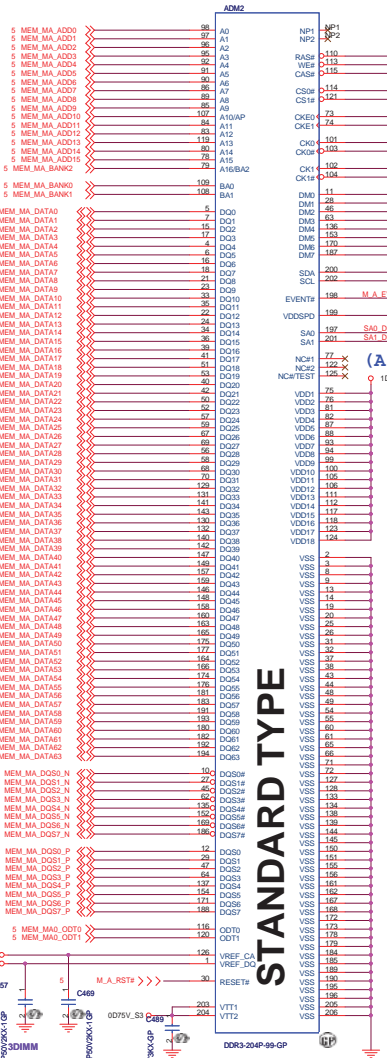
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Title: **DDRIII SO-DIMM SKT 1**

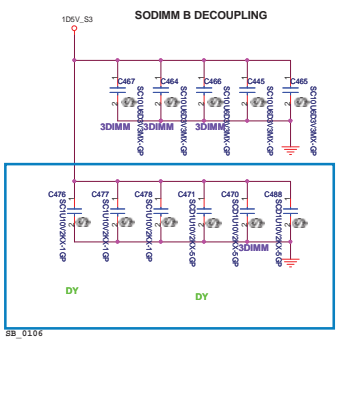
Size: Custom Document Number: **JE70-DN** Rev: **SB**

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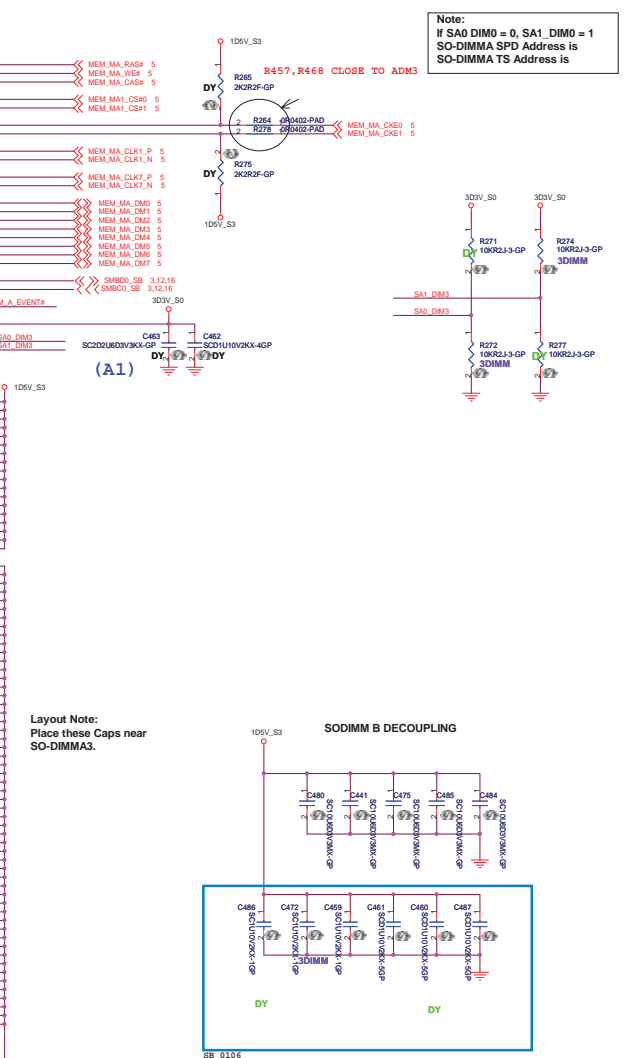
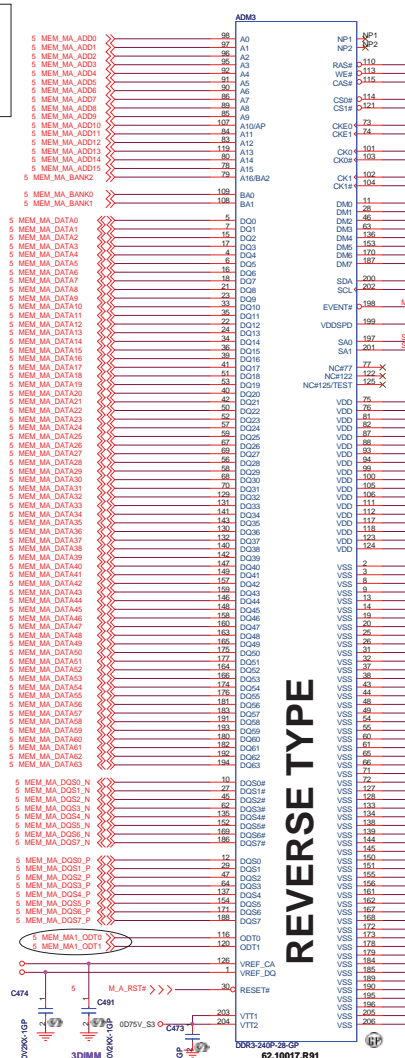
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is
SO-DIMMA TS Address is

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is
SO-DIMMA TS Address is

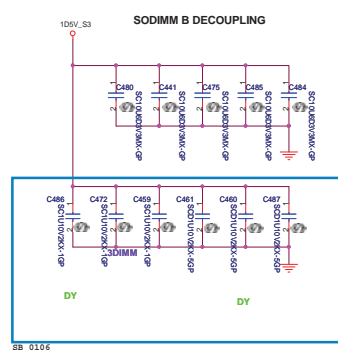


STANDARD TYPE

1106 modify ADM2



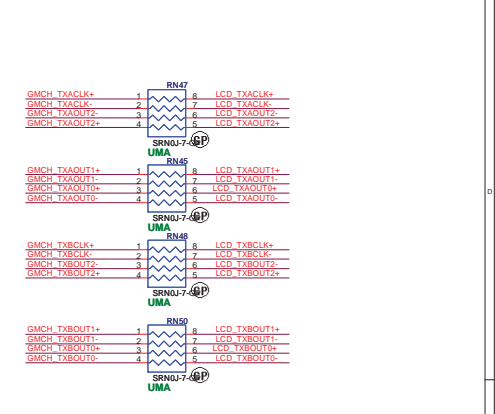
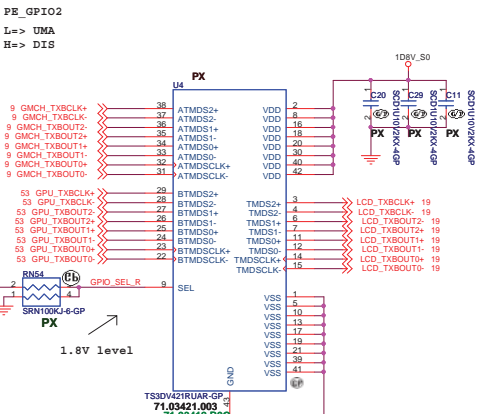
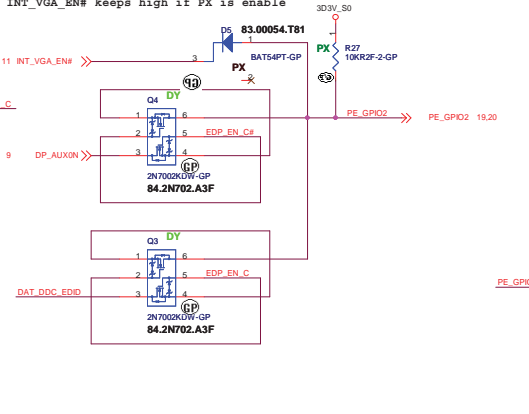
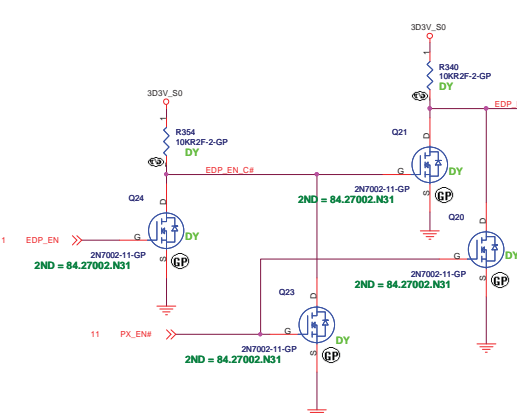
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is
SO-DIMMA TS Address is



REVERSE TYPE

Layout Note:
Place these Caps near
SO-DIMMA3.

1021 modify ADM3



DISPLAY SUPPORT TABLE

	PX_EN#	DP_AUXON EDP disabled	I2C_DATA EDP disabled	INT_VGA_EN#	DISPLAY OUTPUT
IGP only mode	1	X	X	0	IGP (LVDS, EDP, VGA, DP)
MXM only mode	1	X	X	1	MXM (LVDS, EDP, VGA, DP)
Power Express (muxed)	0	0/1	0/1	1	MXM/IGP (LVDS, EDP, VGA) ; MXM (DP)
Power Express (muxless)	0	X	X	0	IGP (LVDS, EDP, VGA, DP)

PX mode display device auto detection method:
VGA: I2C interface to NB
DP:HPD

LVDS

Function	SEL
An to nB1	L
An to nB2	H

CRT

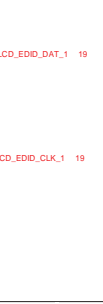
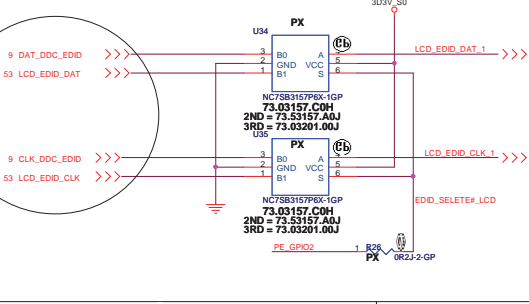
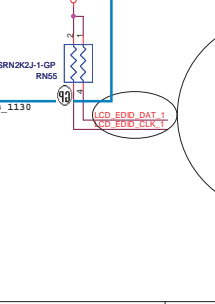
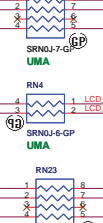
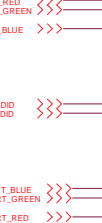
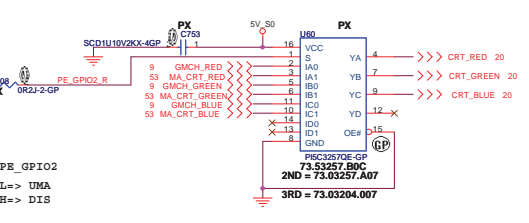
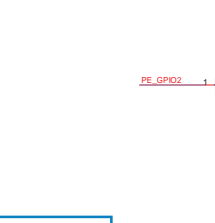
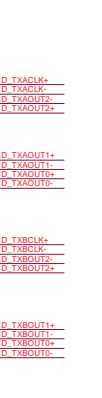
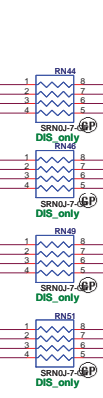
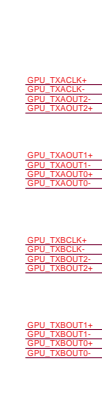
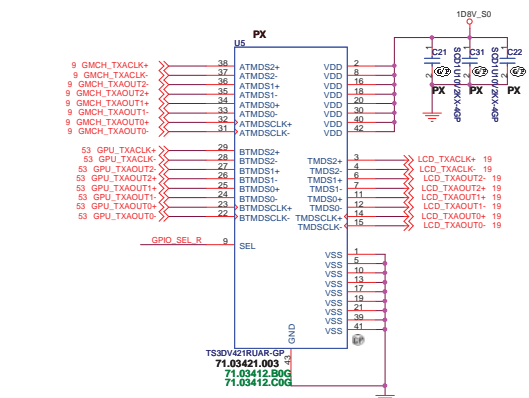
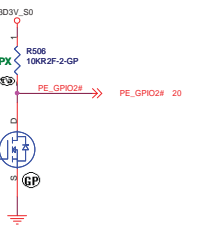
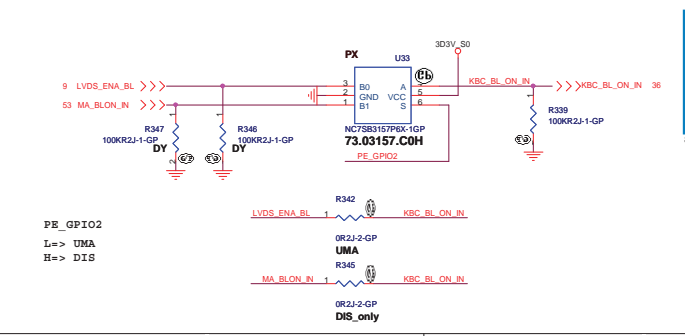
\bar{E}	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S=0
L	H	IA1	IB1	IC1	ID1	S=1

EDID

Function Table

Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

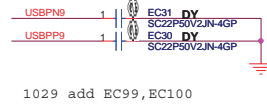
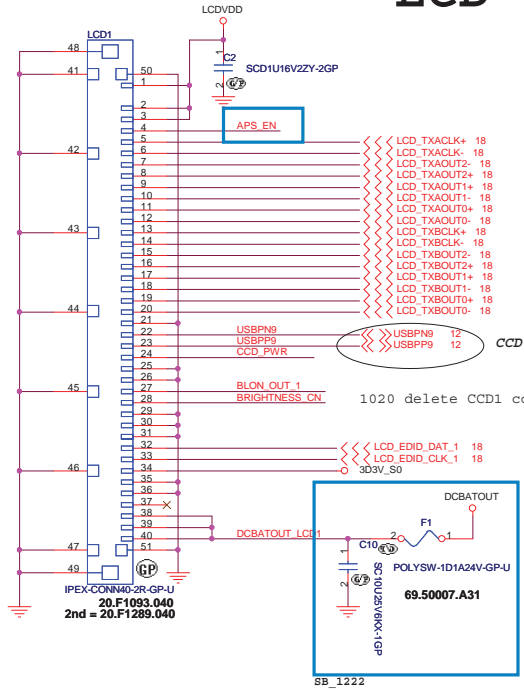
H = HIGH Logic Level L = LOW Logic Level



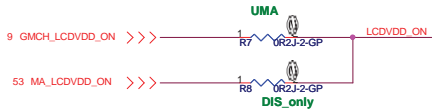
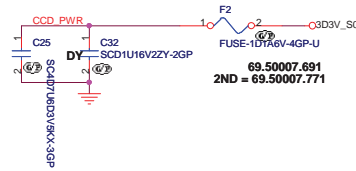
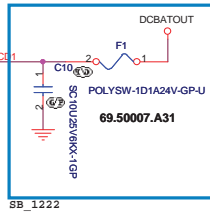
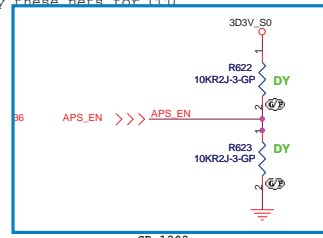
LCD CONN

Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

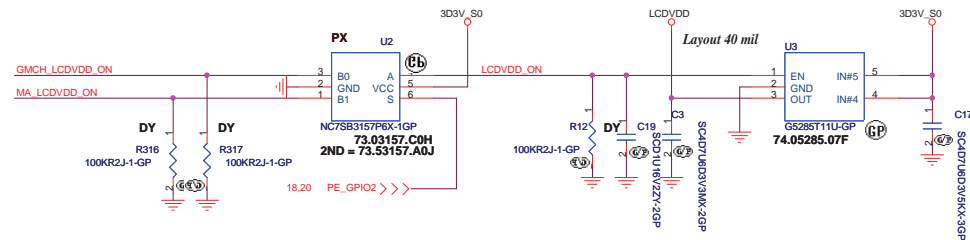
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



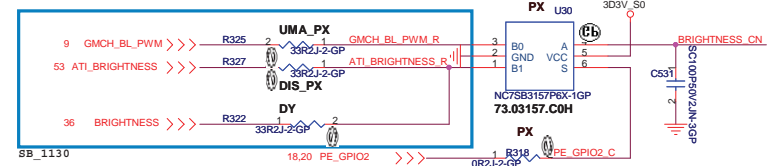
1020 delete CCD1 conn and modify these nets for CCD



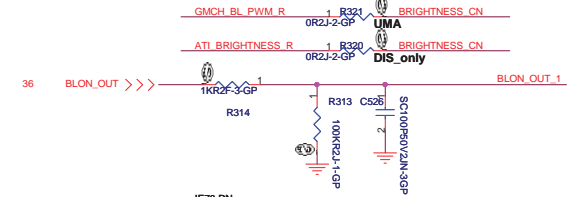
PE_GPIO2
L=> UMA
H=> DIS



Reserve direct connector to KBC



PE_GPIO2
L=> UMA
H=> DIS

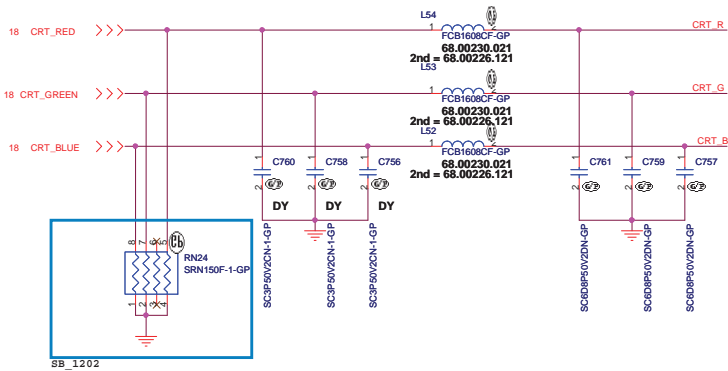


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LCD CONN	
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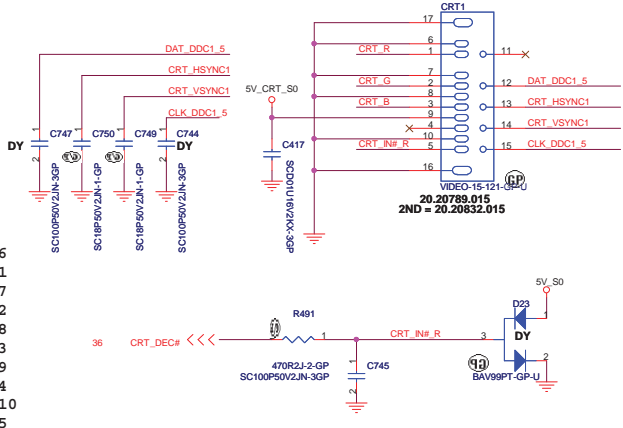
Layout Note:
Place these resistors
close to the CRT-out
connector

Ferrite bead impedance: 10 ohm@100MHz



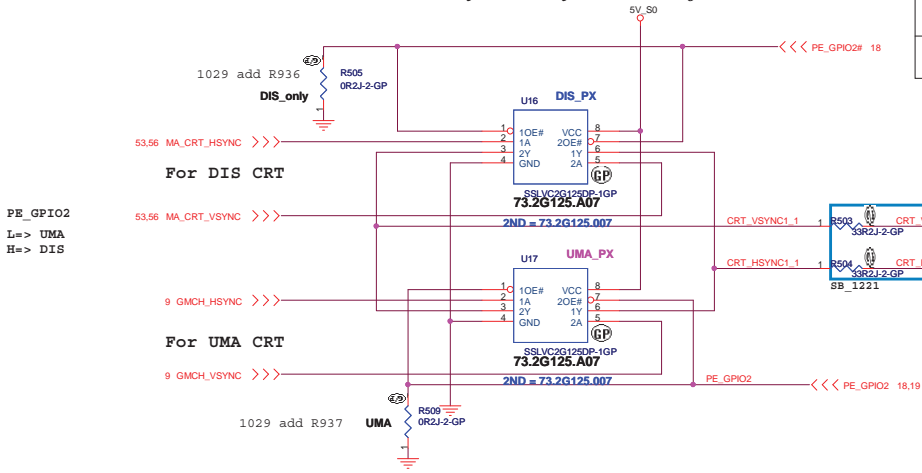
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR

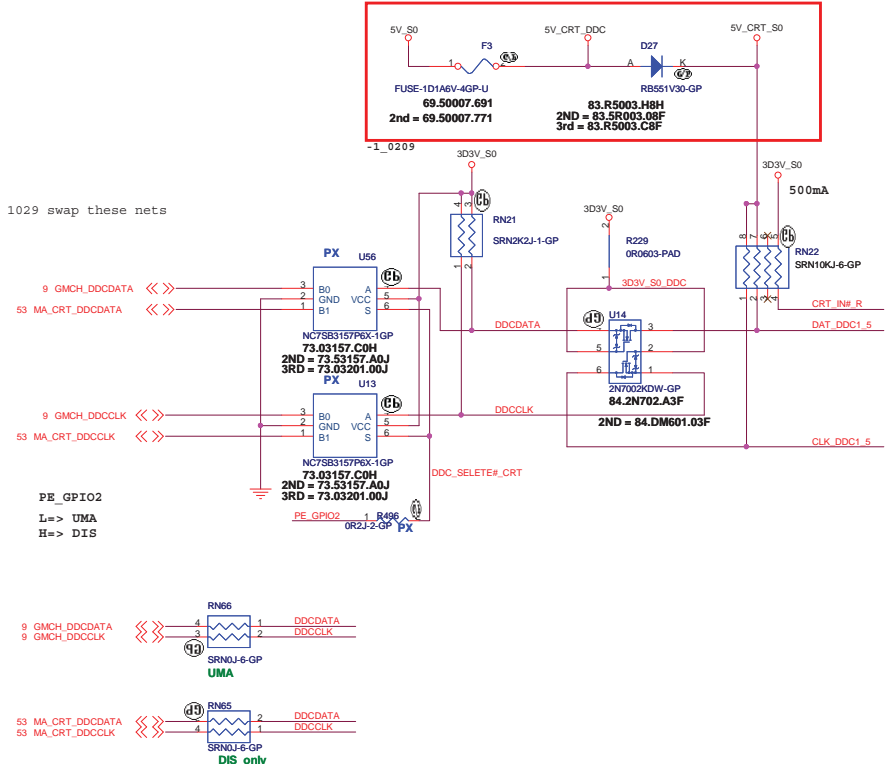


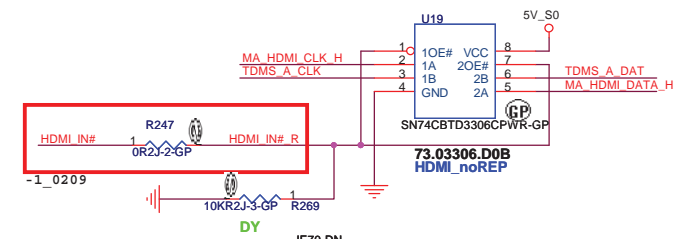
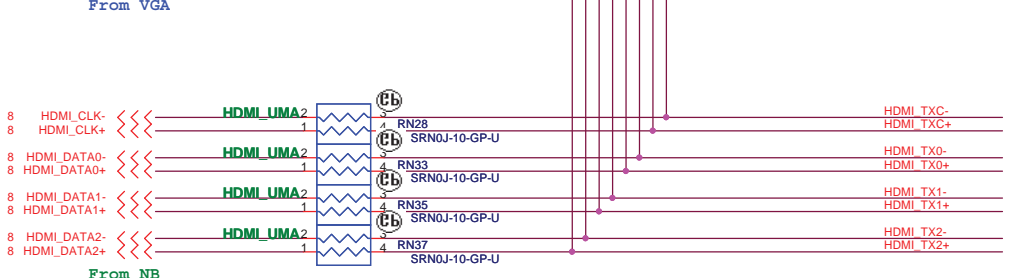
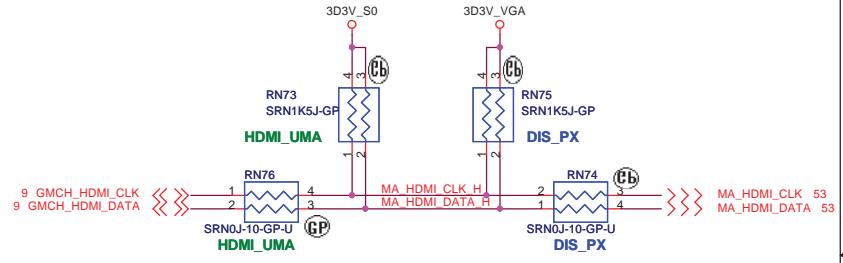
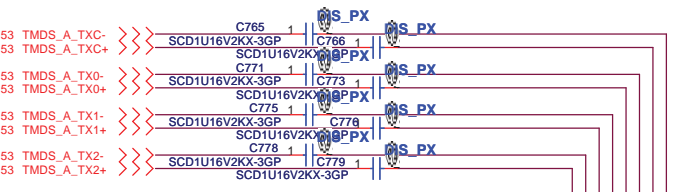
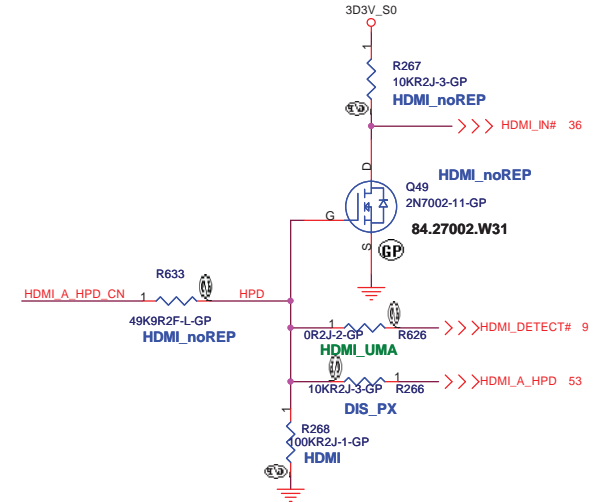
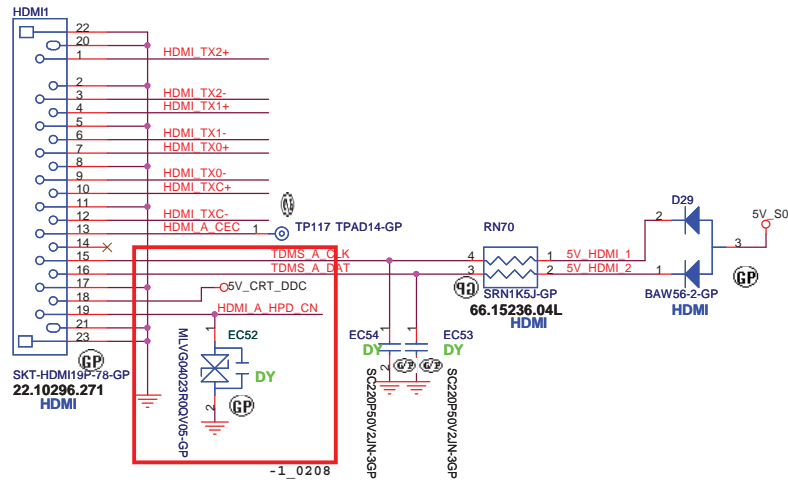
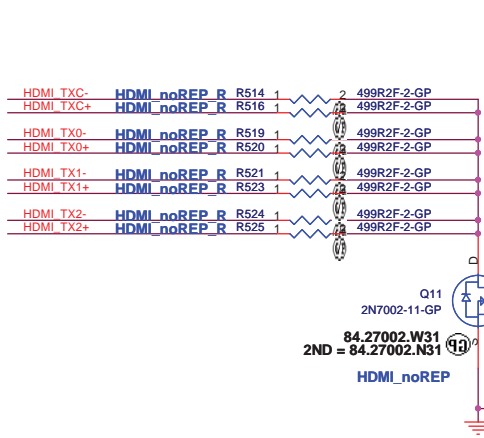
Hsync & Vsync level shift

Function	OE#
nA to nY	L
X	H



DDC_CLK & DATA level shift





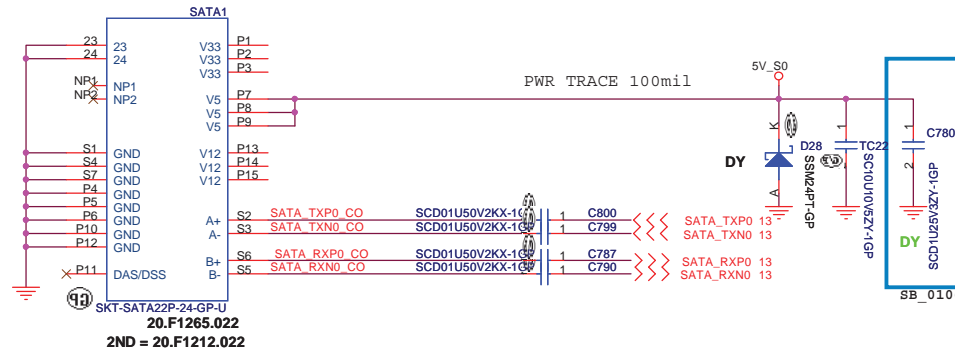
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI Connector**


Size: JE70-DN Document Number: **JE70-DN** Rev: **SB**

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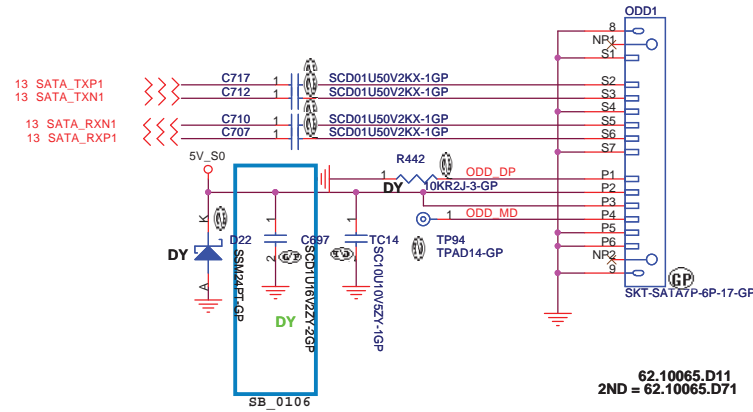
SATA Connector




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Title	
HDD	
Size	Document Number
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ODD Connector

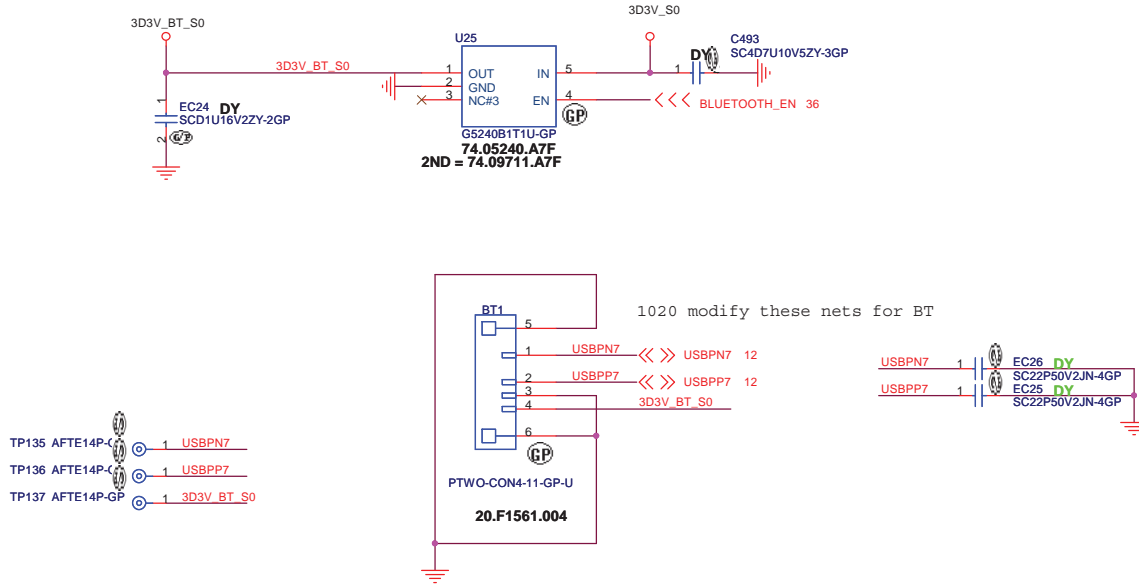


JE70-DN


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Title	
ODD	
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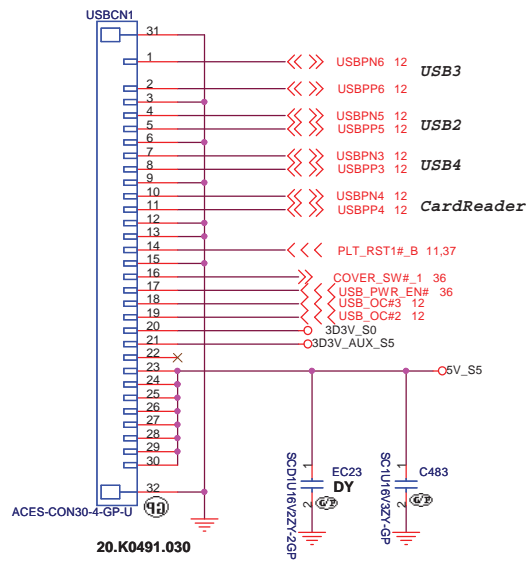
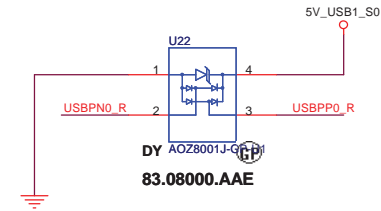
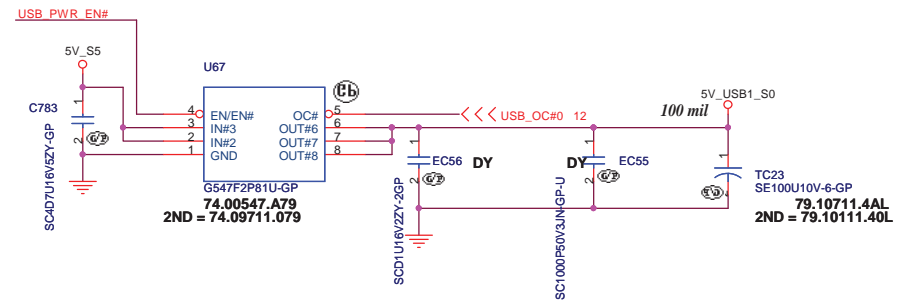
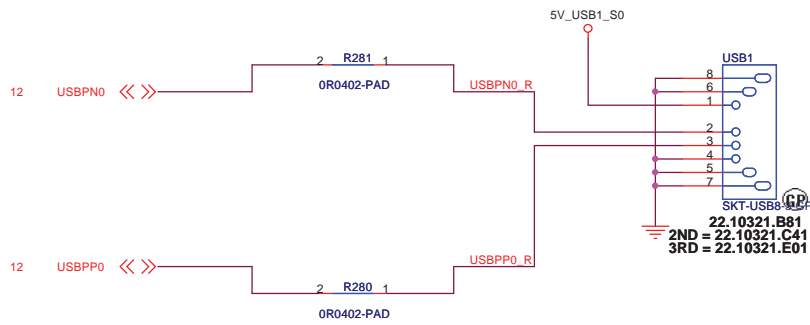
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



JE70-DN

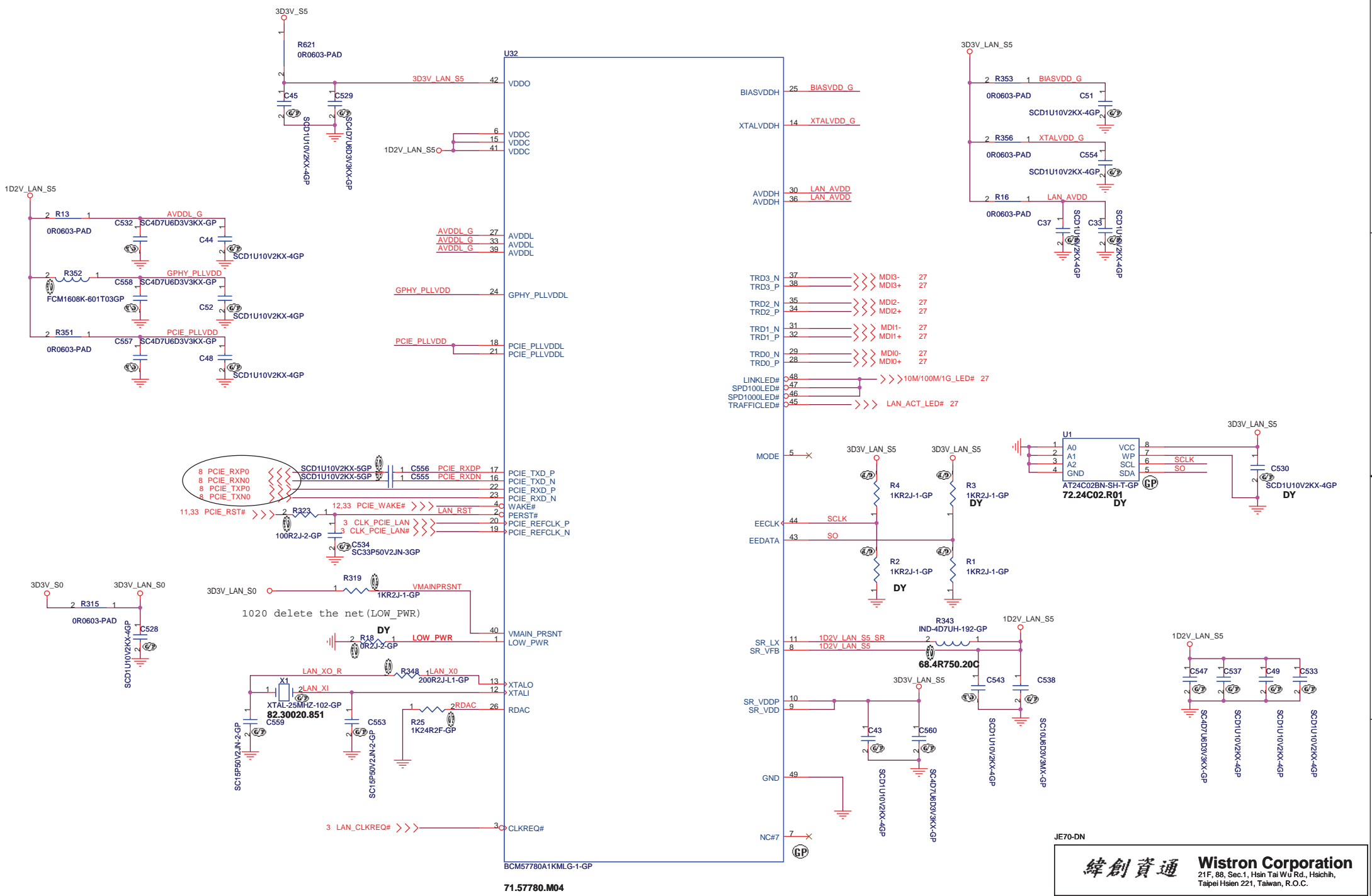
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
BLUETOOTH	
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USBPN6	1	TE14P-GP	TP120
USBPP6	1	TE14P-GP	TP121
USBPN5	1	TE14P-GP	TP122
USBPP5	1	TE14P-GP	TP123
USBPN3	1	TE14P-GP	TP124
USBPP3	1	TE14P-GP	TP125
USBPN4	1	TE14P-GP	TP126
USBPP4	1	TE14P-GP	TP127
PLT_RST1#_B	1	TE14P-GP	TP31
COVER_SW#_1	1	TE14P-GP	TP128
USB_PWR_EN#	1	TE14P-GP	TP129
USB_OC#3	1	TE14P-GP	TP130
USB_OC#2	1	TE14P-GP	TP131
3D3V_S0	1	TE14P-GP	TP133
3D3V_AUX_S5	1	TE14P-GP	TP132
5V_S5	1	TE14P-GP	TP134

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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: USB			
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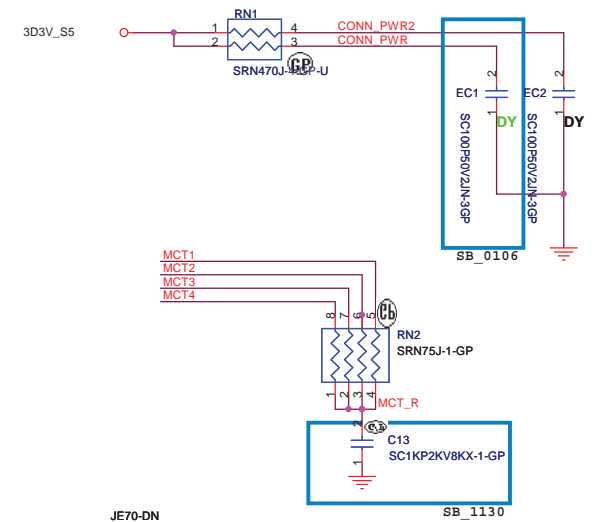
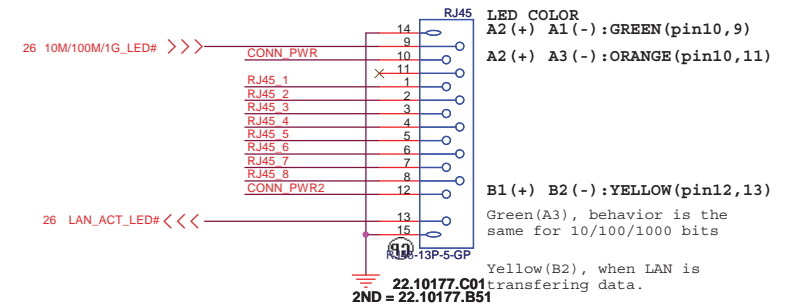
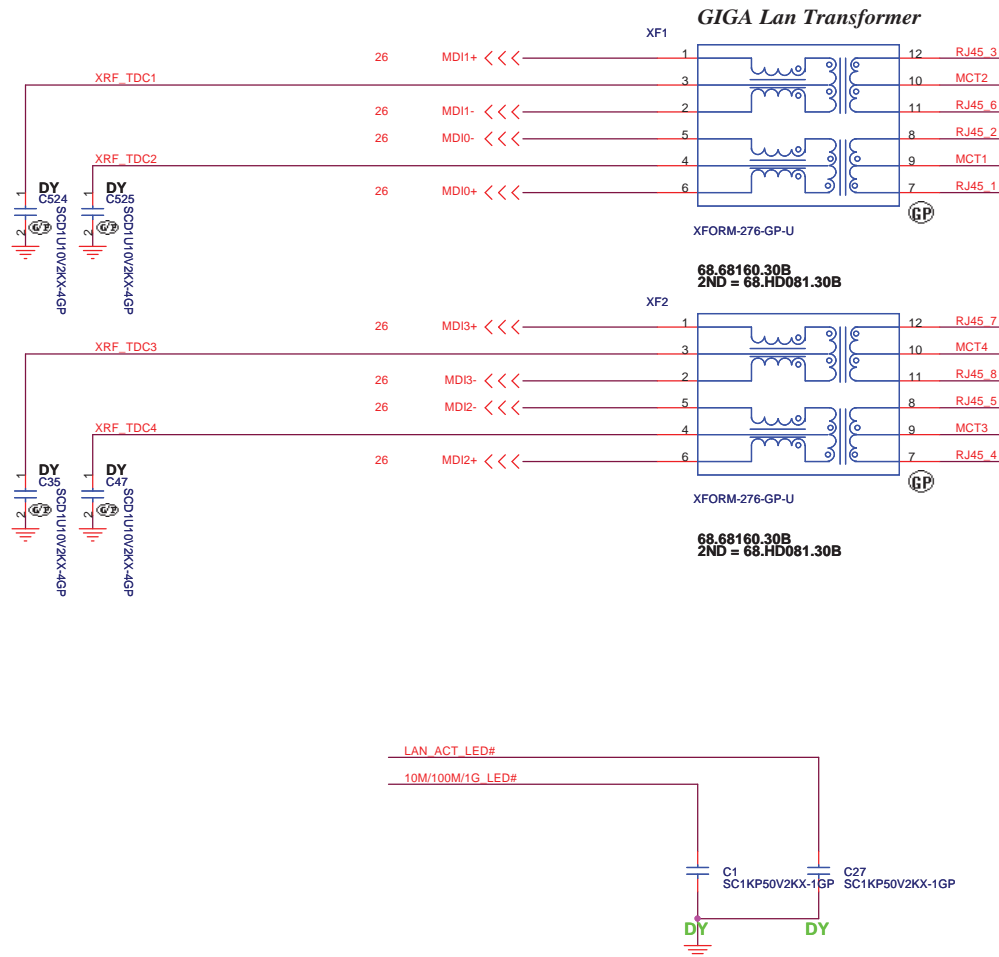
JE70-DN

緯創資通		Wistron Corporation	
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BCM57780			
Title	BCM57780		Rev
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LAN Connector

LAN Connector

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

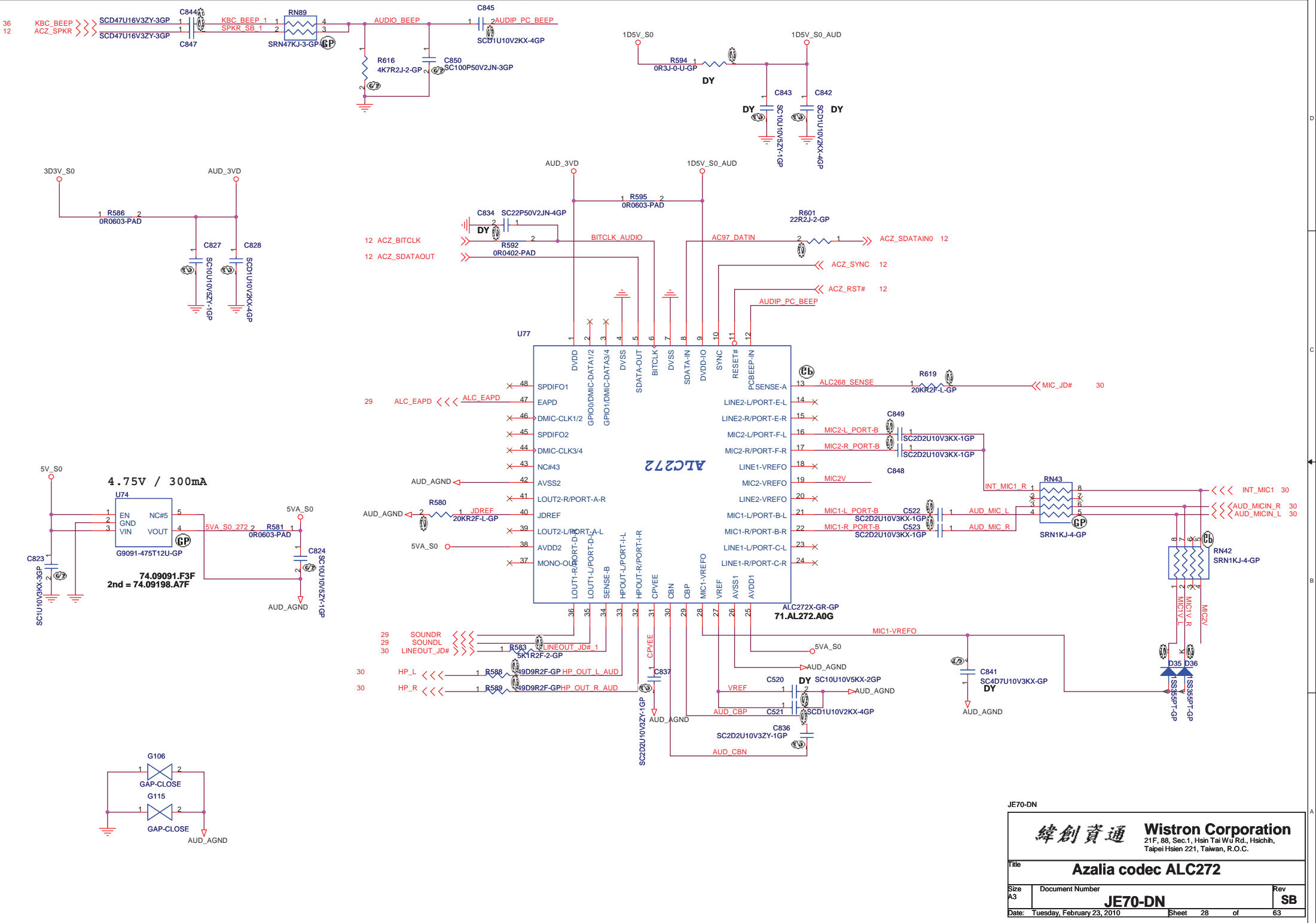


JE70-DN

SB_1130

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title LAN CONN		
Size A3	Document Number JE70-DN	Rev SB
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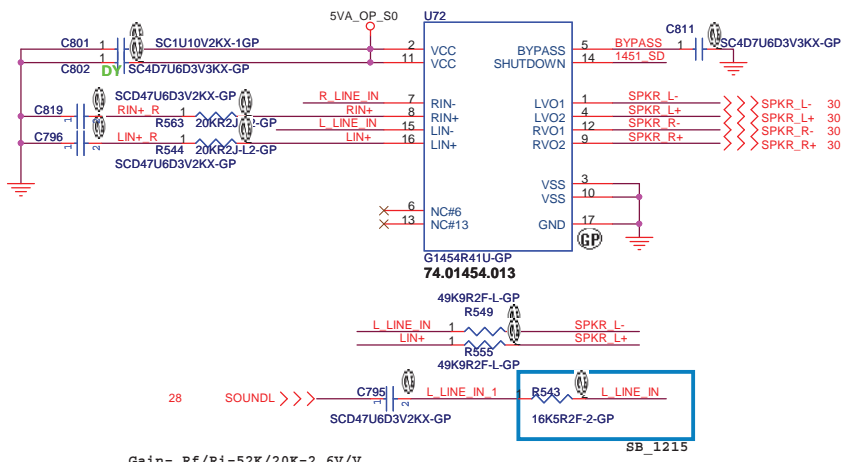
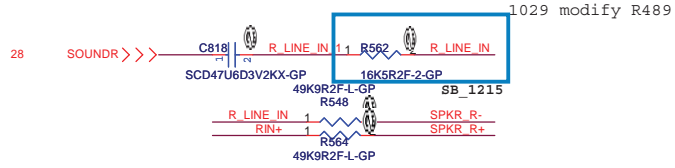
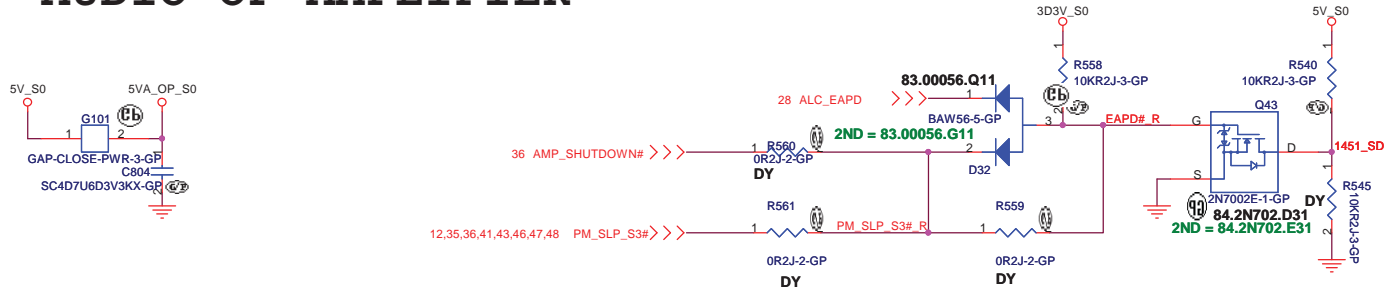
JE70-DN

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Azalia codec ALC272**

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AUDIO OP AMPLIFIER



Gain = $R_f/R_i = 52K/20K = 2.6V/V$
 $f(HP) = 1/(2 \pi * 20K * 0.47\mu f) = 16.9Hz$
 If $V_{IN} = 1.54V$ Gain = $2.6V/V$ $R_L = 4\Omega$ $V_O(peak) = 4V$ $V(rms) = 2.828V$
 Power = $2.828^2/4 = 1.999W$

JE70-DN

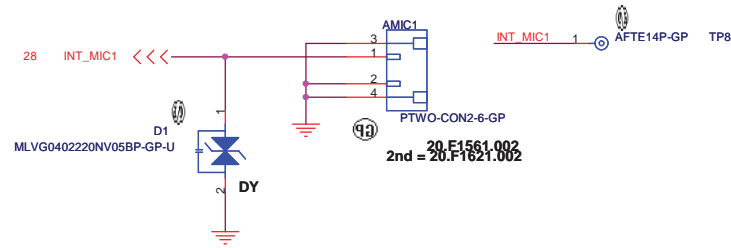
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP**

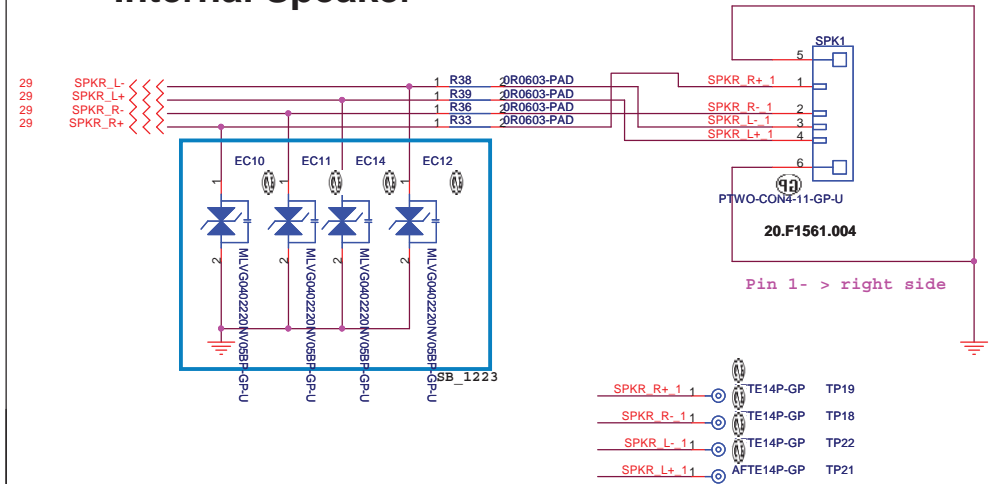
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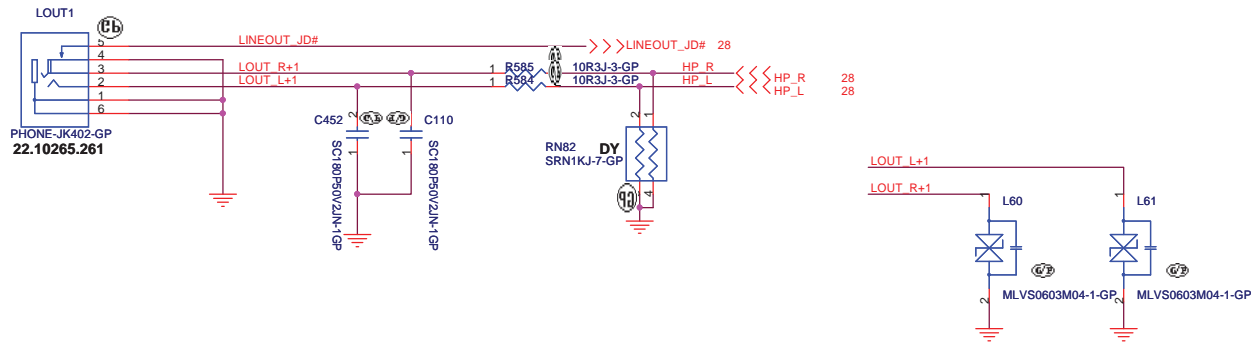
Internal Mic



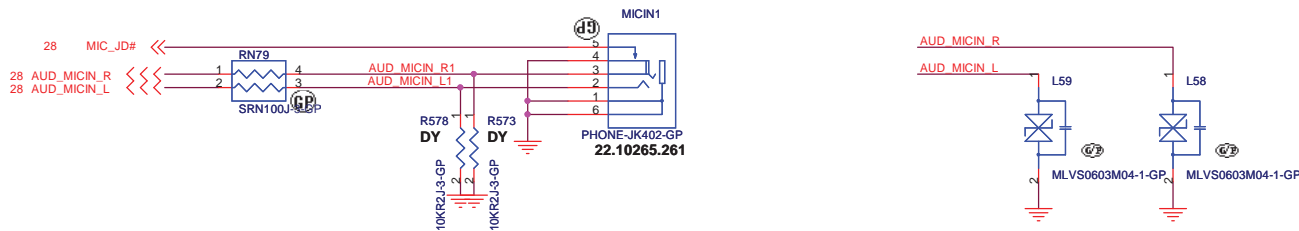
Internal Speaker



LINE OUT



MIC IN



JE70-DN

緯創資通 Wistron Corporation
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Title: **AUDIO JACK**

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No Modem Function

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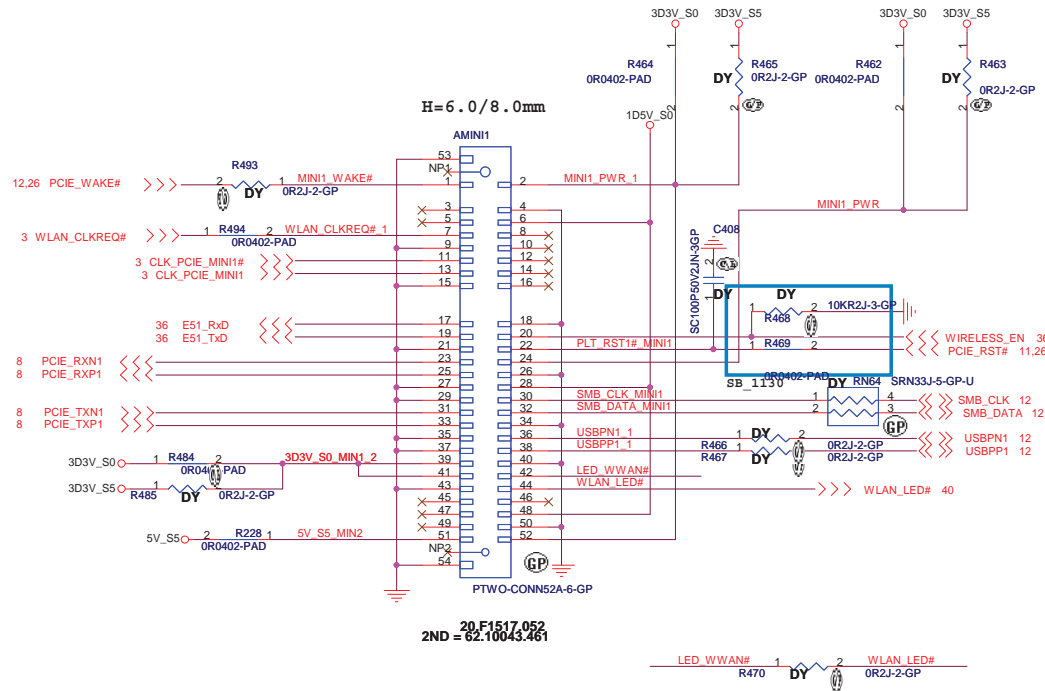
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MDC			
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5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD) on USB board

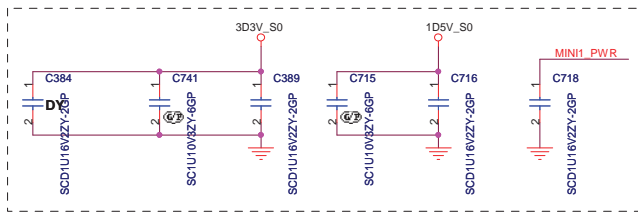
JE70-DN

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CARDREADER			
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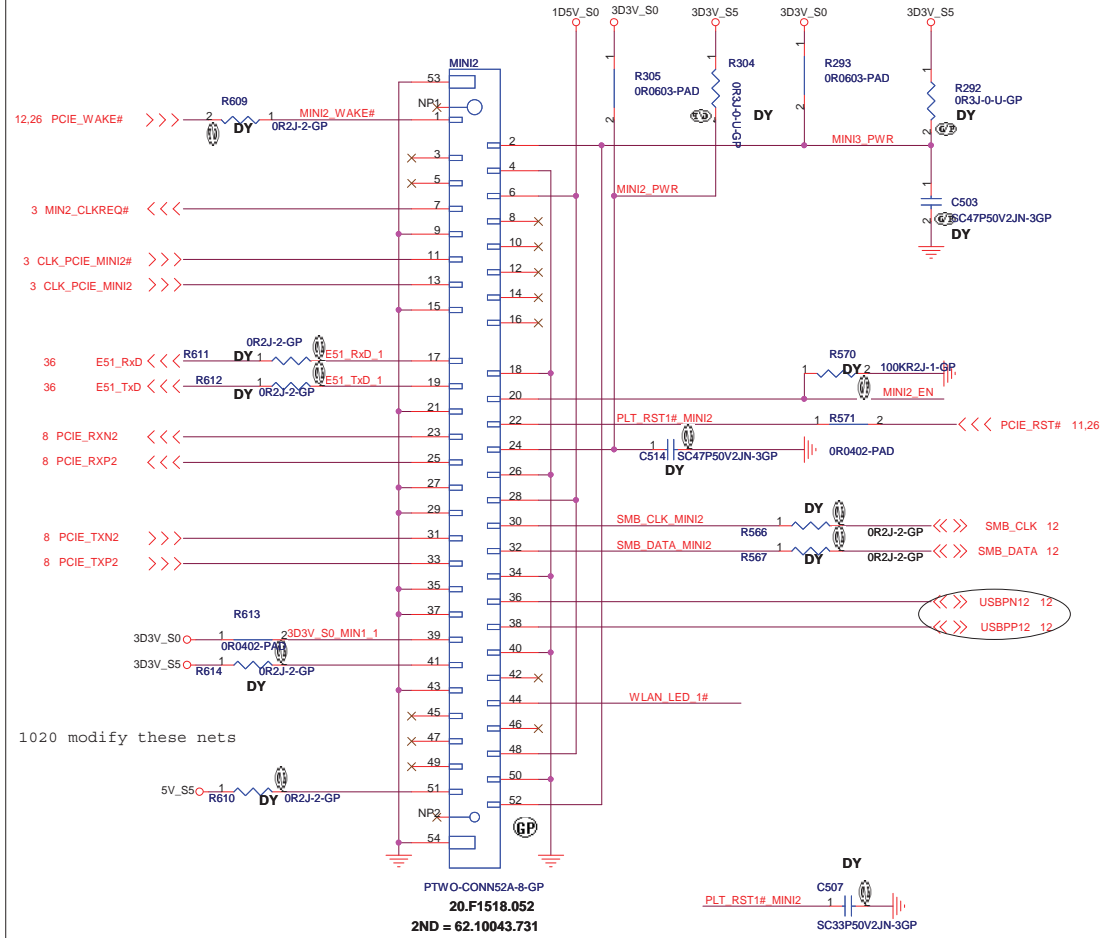
Mini Card Connector(WLAN)



Place near AMINI1

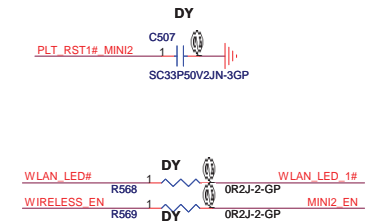
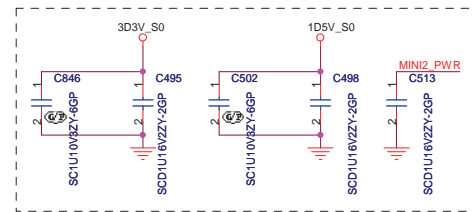


Mini Card Function



1020 modify these nets

Place near MINIC2



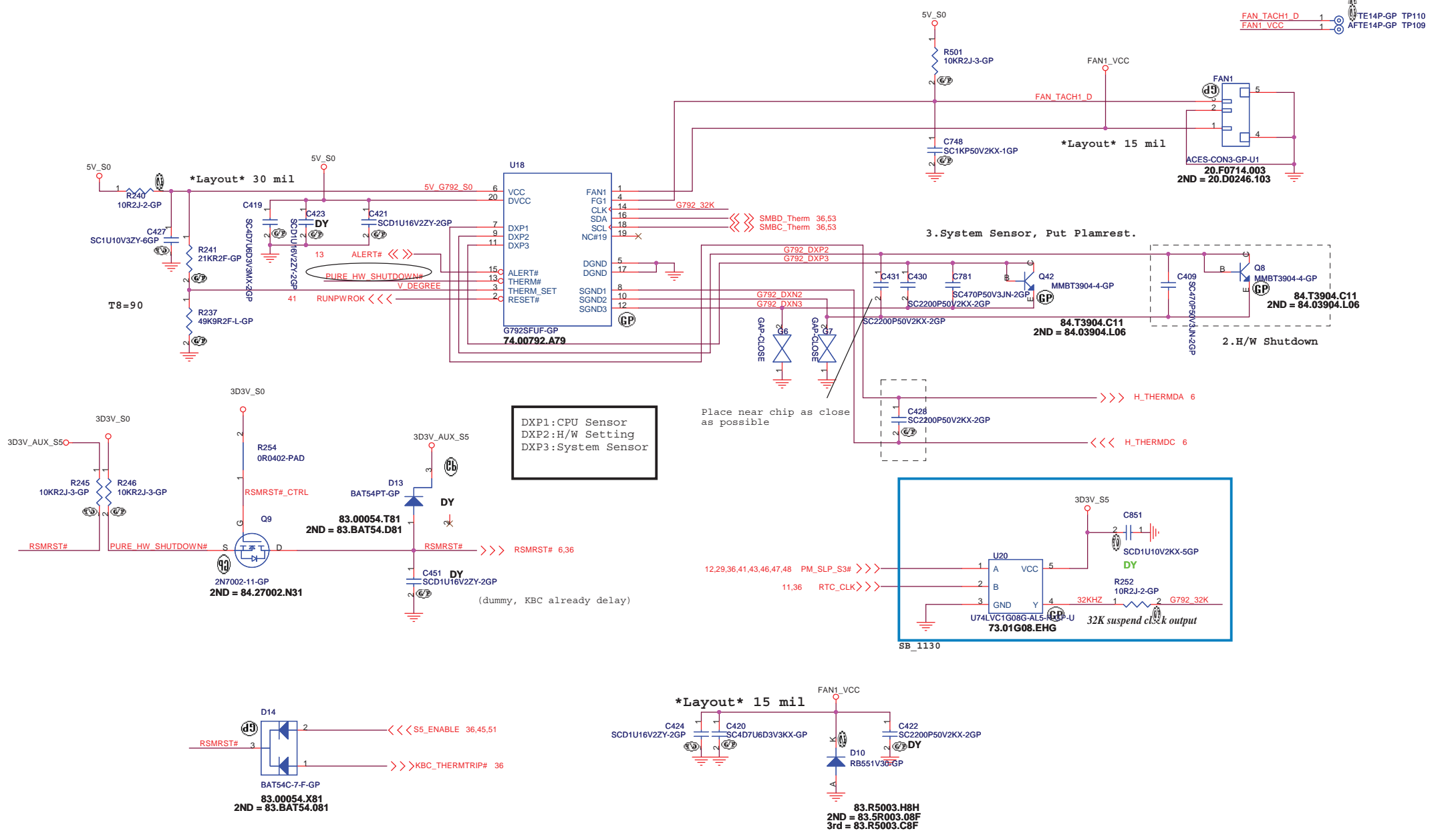
JE70-DN

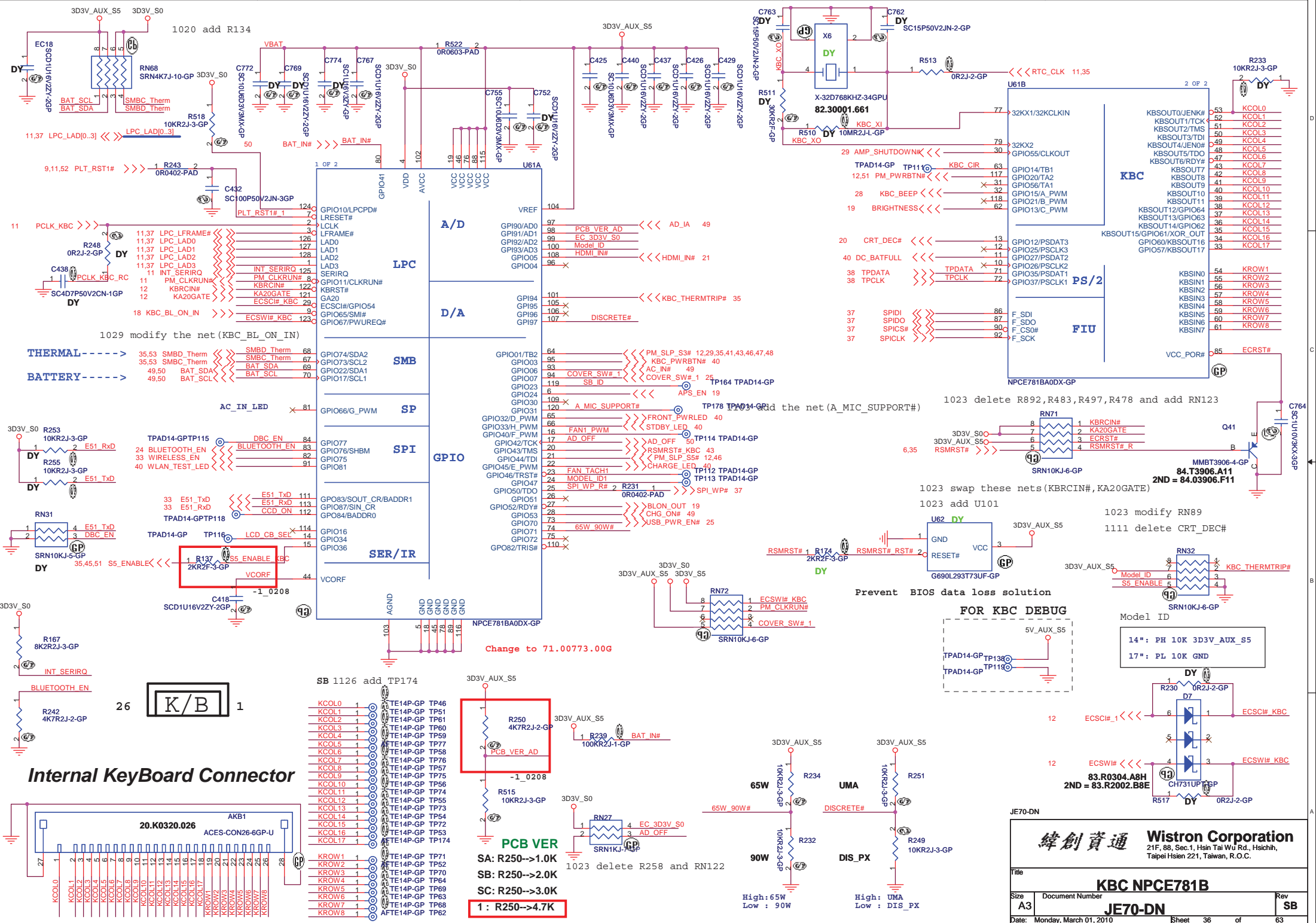
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
MINI CARD			
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No NEWCARD Function

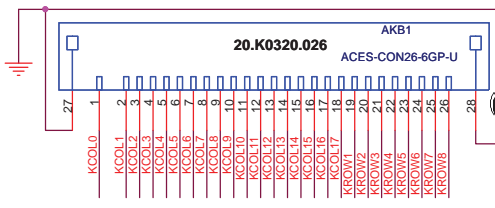
JE70-DN

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
NEW CARD			
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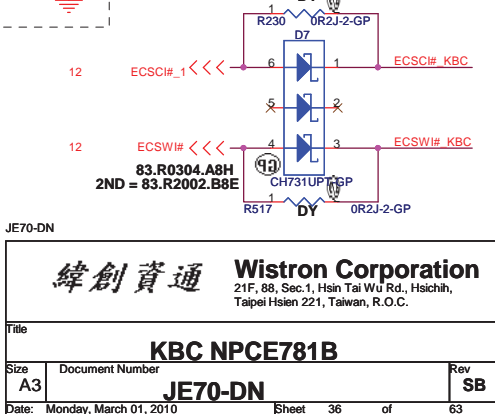
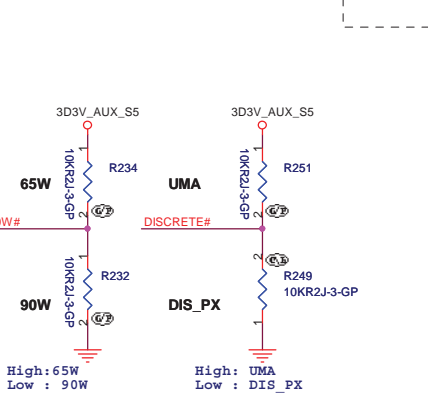
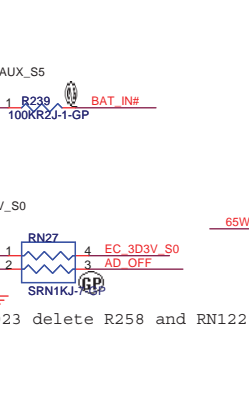
Internal KeyBoard Connector



SB 1126 add TP174

KCOL0	1	TE14P-GP	TP46
KCOL1	1	TE14P-GP	TP51
KCOL2	1	TE14P-GP	TP61
KCOL3	1	TE14P-GP	TP60
KCOL4	1	TE14P-GP	TP59
KCOL5	1	TE14P-GP	TP77
KCOL6	1	TE14P-GP	TP58
KCOL7	1	TE14P-GP	TP76
KCOL8	1	TE14P-GP	TP57
KCOL9	1	TE14P-GP	TP75
KCOL10	1	TE14P-GP	TP56
KCOL11	1	TE14P-GP	TP74
KCOL12	1	TE14P-GP	TP55
KCOL13	1	TE14P-GP	TP73
KCOL14	1	TE14P-GP	TP54
KCOL15	1	TE14P-GP	TP72
KCOL16	1	TE14P-GP	TP53
KCOL17	1	TE14P-GP	TP174
KROW1	1	TE14P-GP	TP71
KROW2	1	TE14P-GP	TP52
KROW3	1	TE14P-GP	TP70
KROW4	1	TE14P-GP	TP64
KROW5	1	TE14P-GP	TP69
KROW6	1	TE14P-GP	TP63
KROW7	1	TE14P-GP	TP68
KROW8	1	TE14P-GP	TP62

PCB VER
 SA: R250-->1.0K
 SB: R250-->2.0K
 SC: R250-->3.0K
 1: R250-->4.7K



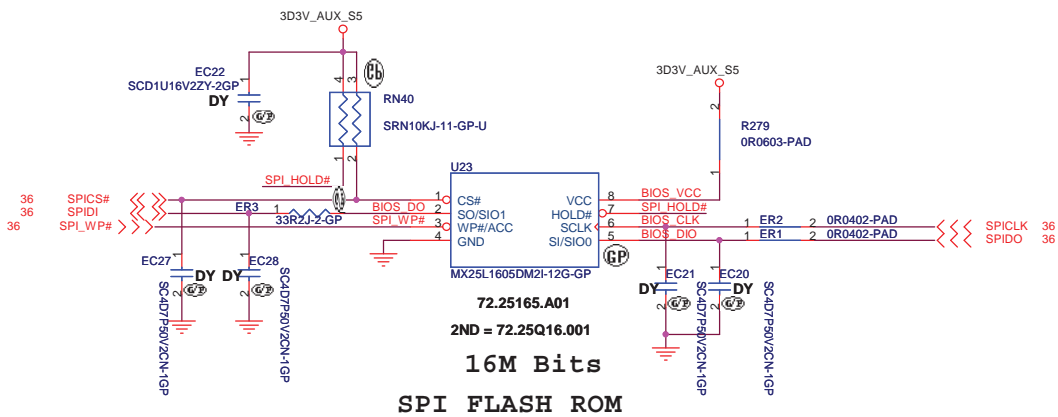
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KBC NPCE781B

JE70-DN

File	Document Number	Rev
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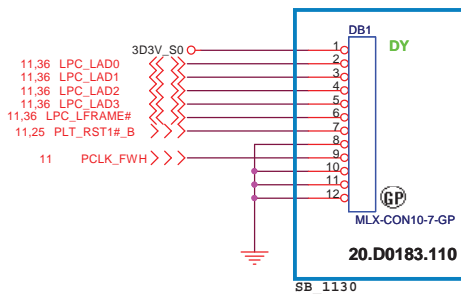
Date: Monday, March 01, 2010 Sheet 36 of 63



**16M Bits
SPI FLASH ROM**

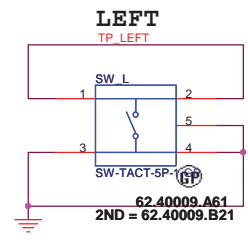
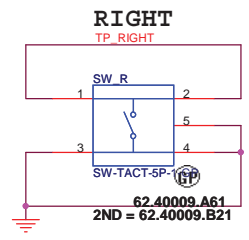
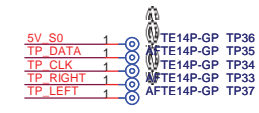
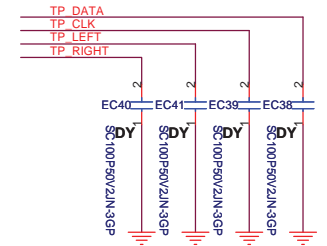
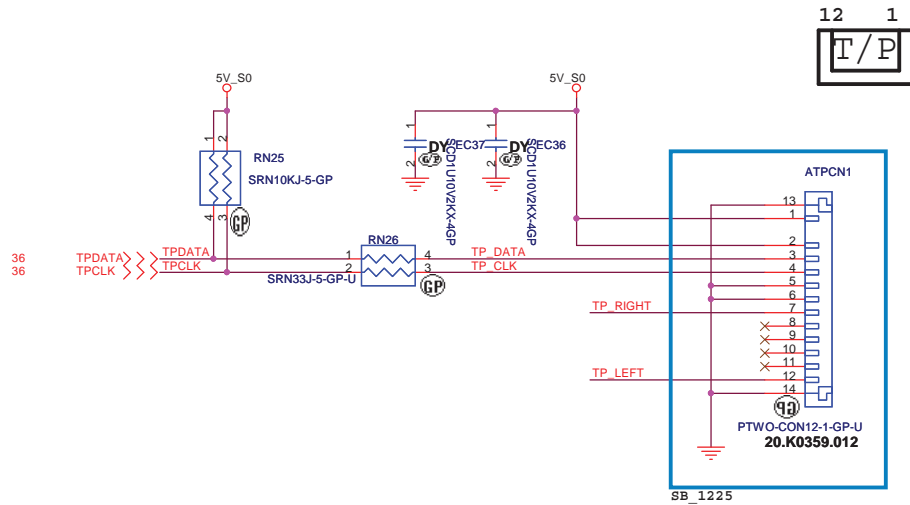
GOLDEN FINGER FOR DEBUG BOARD

11.36 LPC_LAD[0..3] <<< LPC_LAD[0..3]



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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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BIOS			
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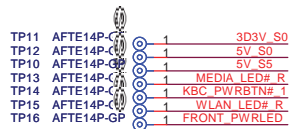
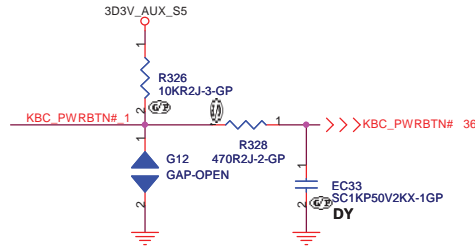
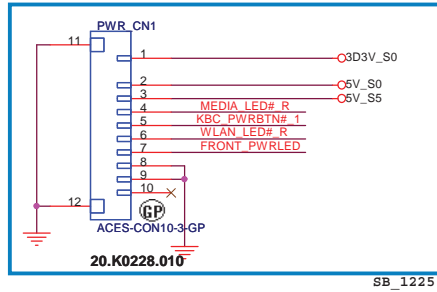
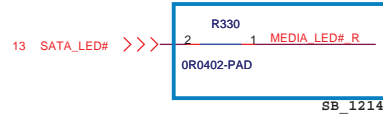
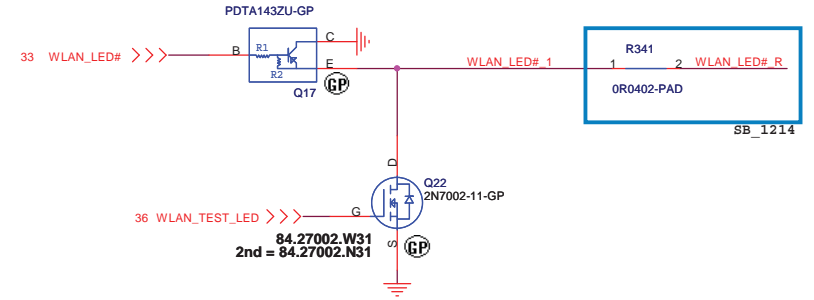
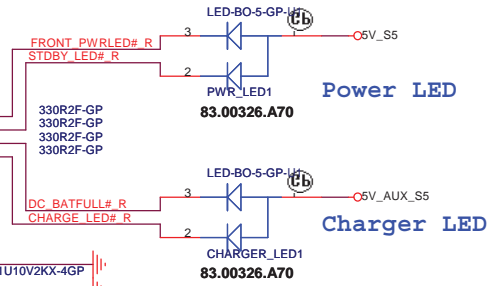
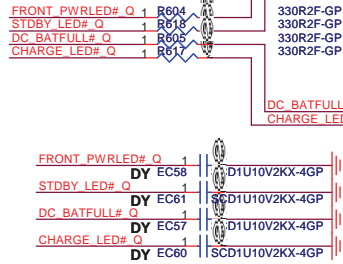
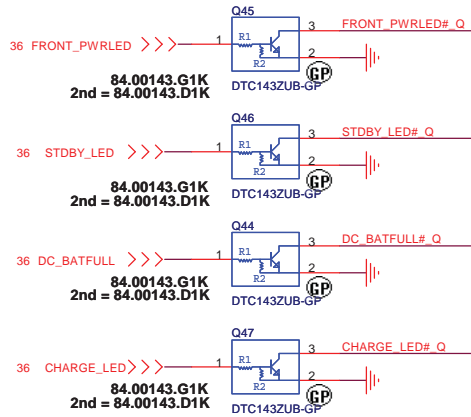
JE70-DN

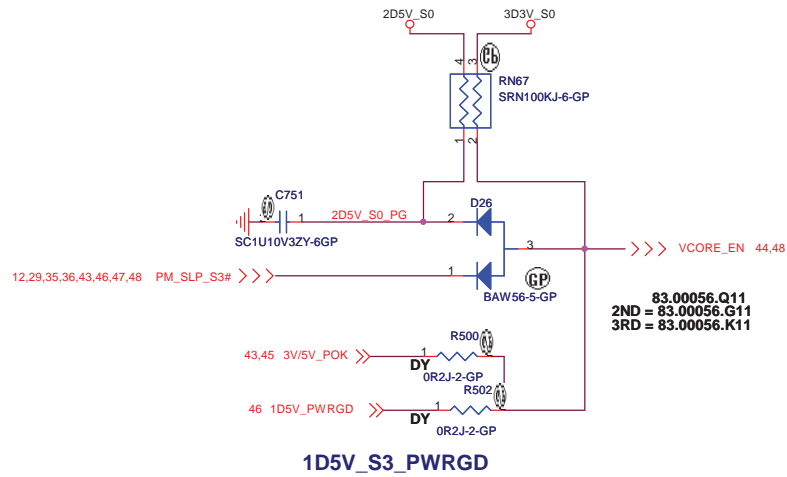
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Touch PAD		
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NONE BOARD

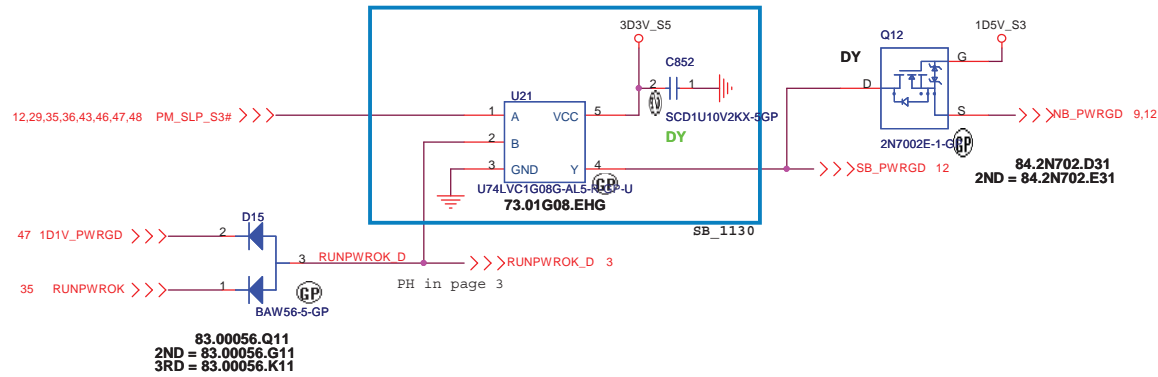
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
NONE BOARD			
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LED



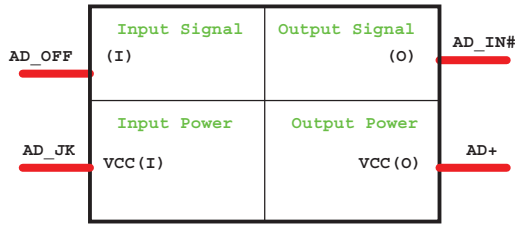


P/H @ 1D8V_S3 PAGE

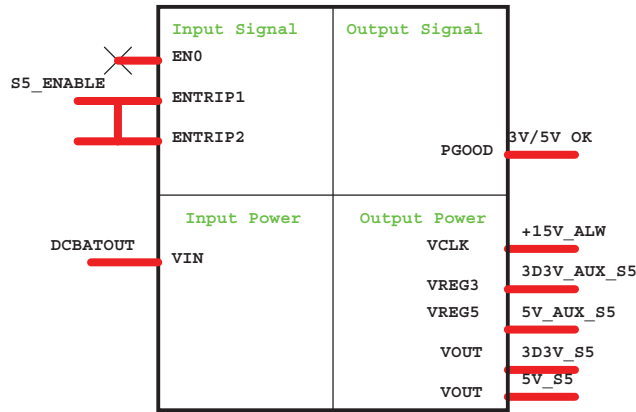


JE70-DN

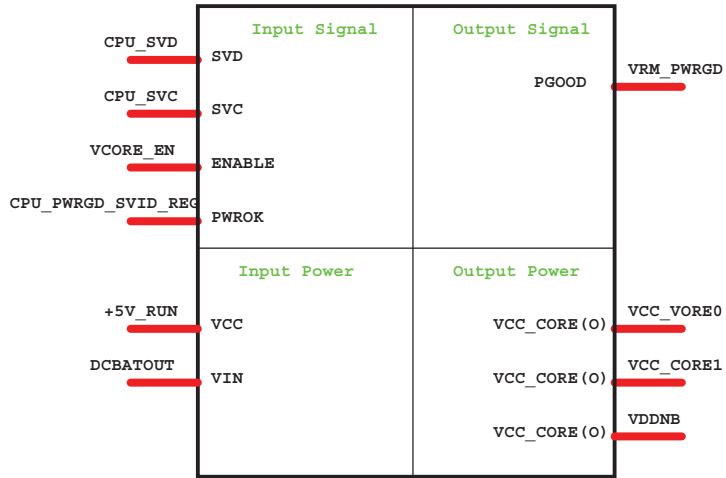
Adapter



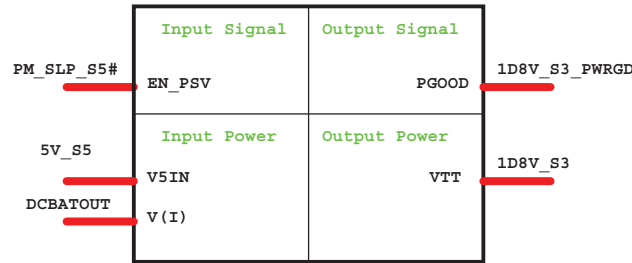
DCDC 5V/3D3V(RT8205A)



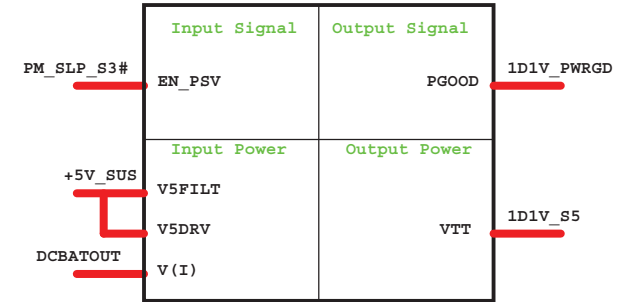
CPU_CORE ISL6265HRTZ



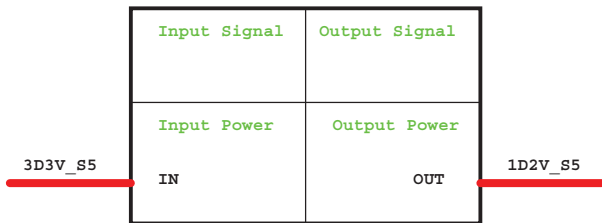
DCDC 1D8V(RT8209B)



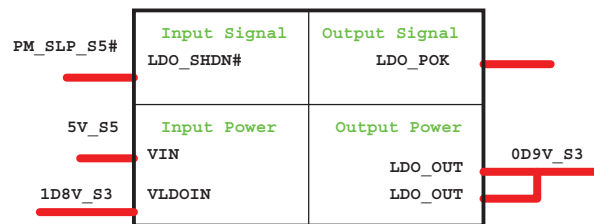
DCDC 1D1V(RT8209)



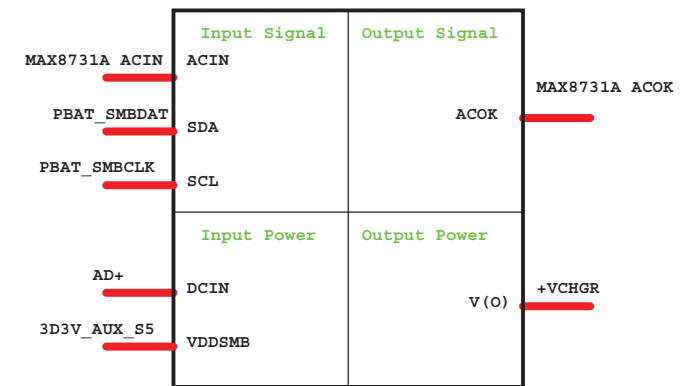
1D2V LDO G9161



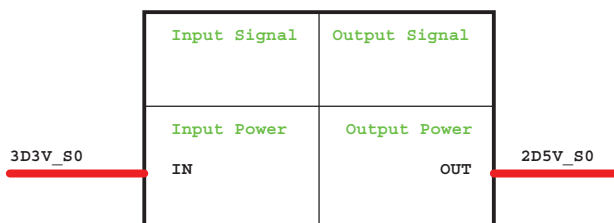
0D9V LDO RT9026



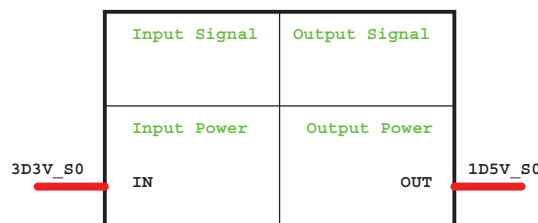
CHARGER MAX8731




2D5V LDO R9161

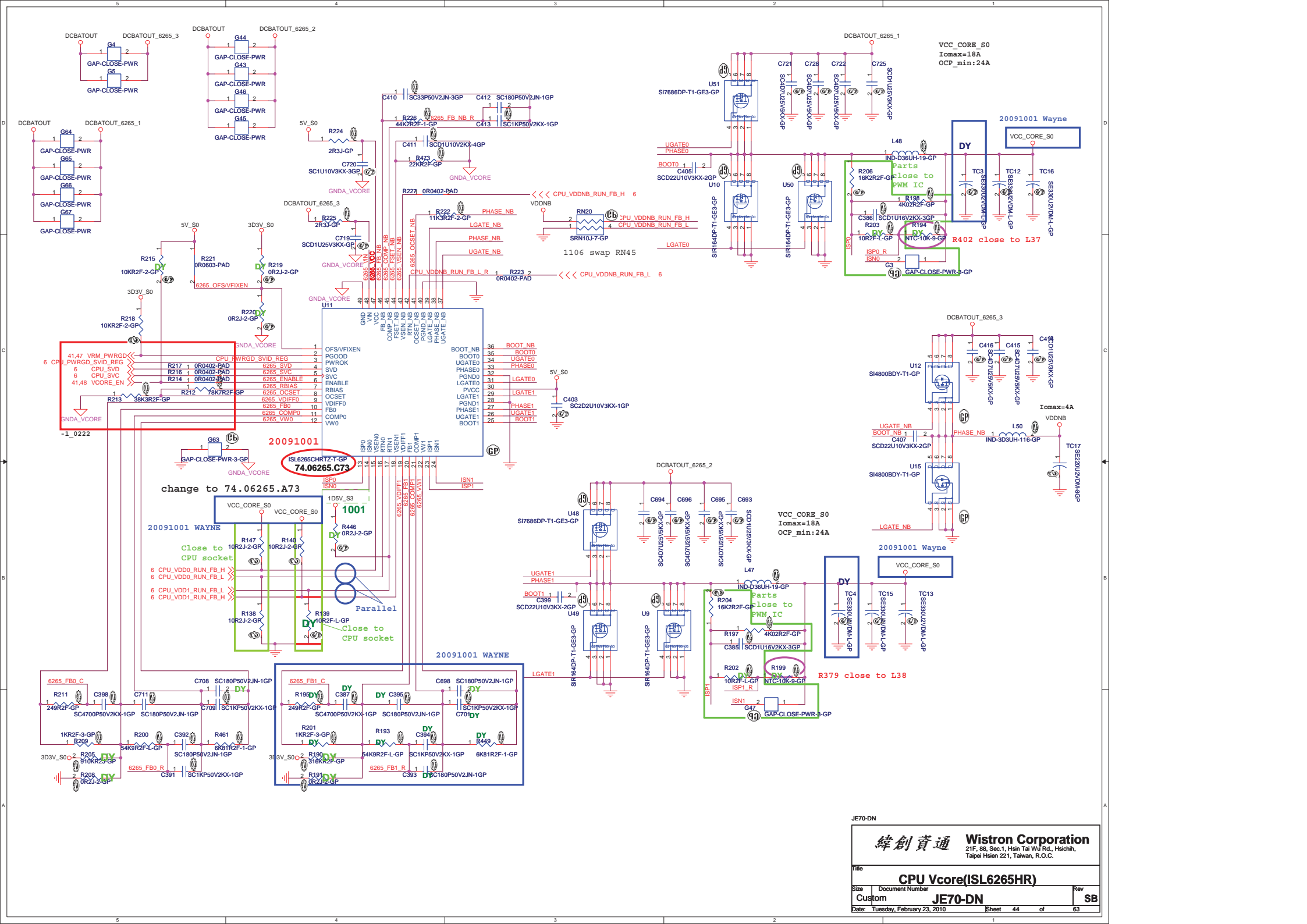


1D5V LDO G9571



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Title Power Block Diagram	
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VCC_CORE_S0
Iomax=18A
OCP_min:24A

VCC_CORE_S0
Iomax=4A

VCC_CORE_S0
Iomax=18A
OCP_min:24A

VCC_CORE_S0
Iomax=18A
OCP_min:24A

change to 74.06265.A73

20091001
ISL6265CHRTZ-T-GP
74.06265.C73

VCC_CORE_S0

VCC_CORE_S0

Close to CPU socket

6 CPU_VDD0_RUN_FB_H
6 CPU_VDD0_RUN_FB_L
6 CPU_VDD1_RUN_FB_L
6 CPU_VDD1_RUN_FB_H

Parallel

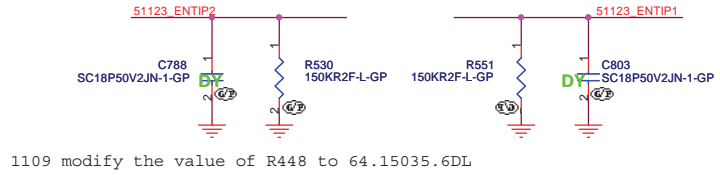
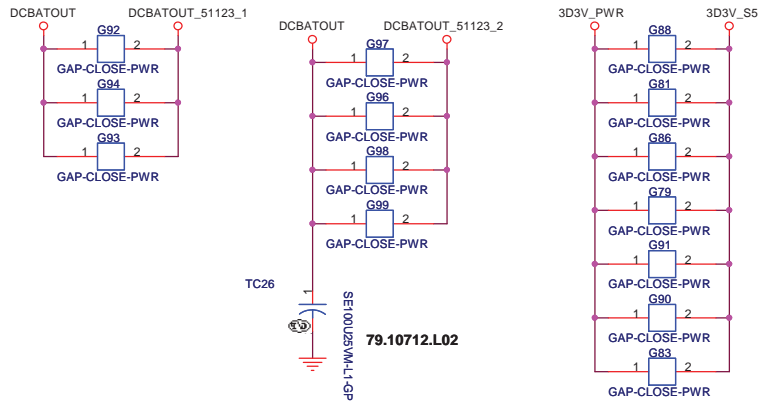
Close to CPU socket

20091001 WAYNE

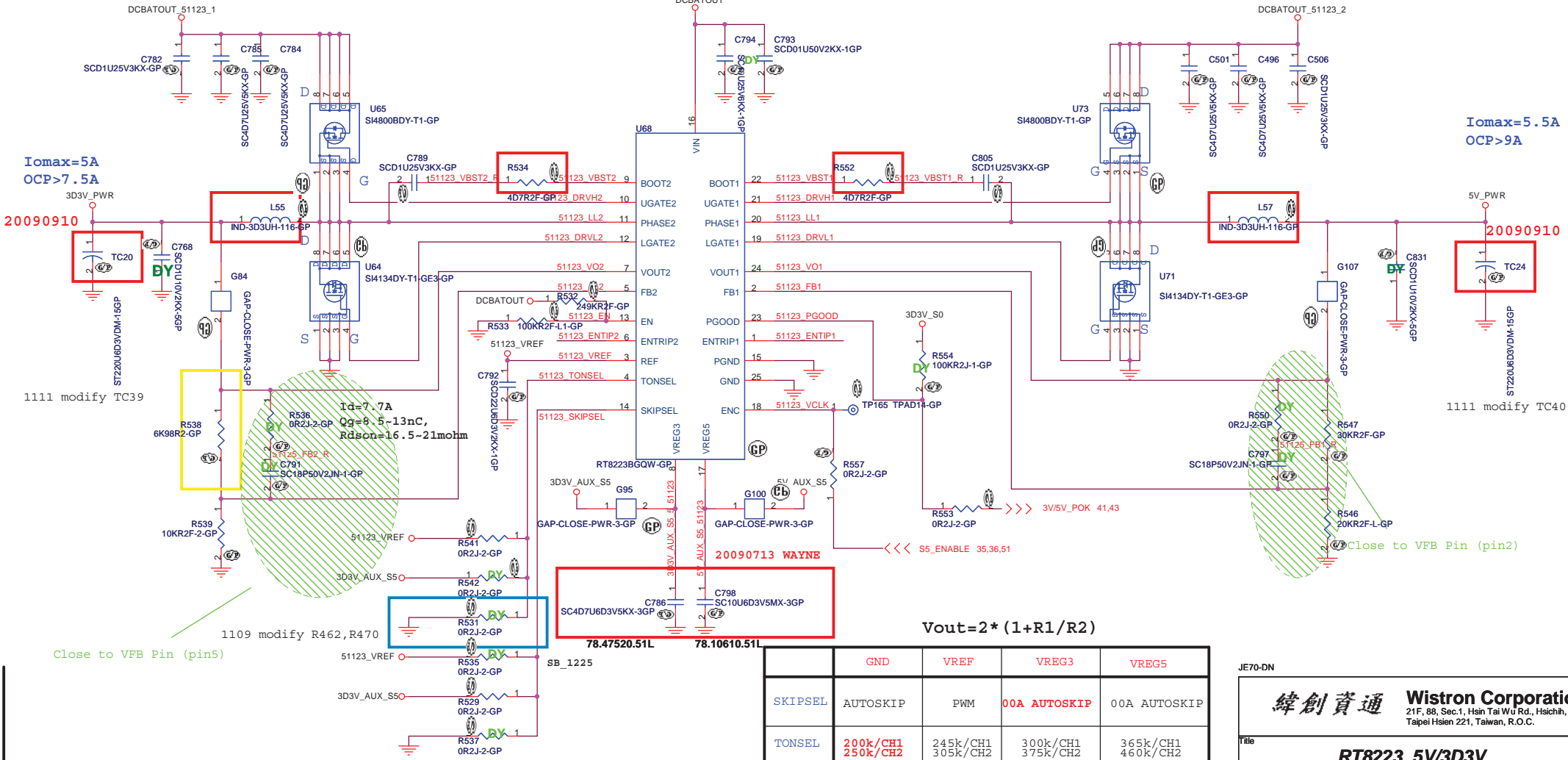
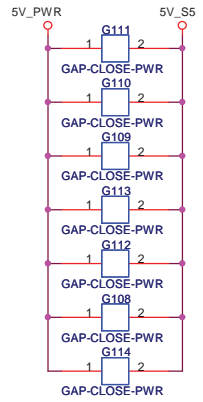
JE70-DN

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Taipei Hsien 221, Taiwan, R.O.C.

File				CPU Vcore(ISL6265HR)			
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1109 modify the value of R448 to 64.15035.6DL



Iomax=5A
OCP>7.5A
20090910

Iomax=5.5A
OCP>9A

1111 modify TC39

1111 modify TC40

1109 modify R462, R470

Close to VFB Pin (pin5)

$$V_{out} = 2 * (1 + R1/R2)$$

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

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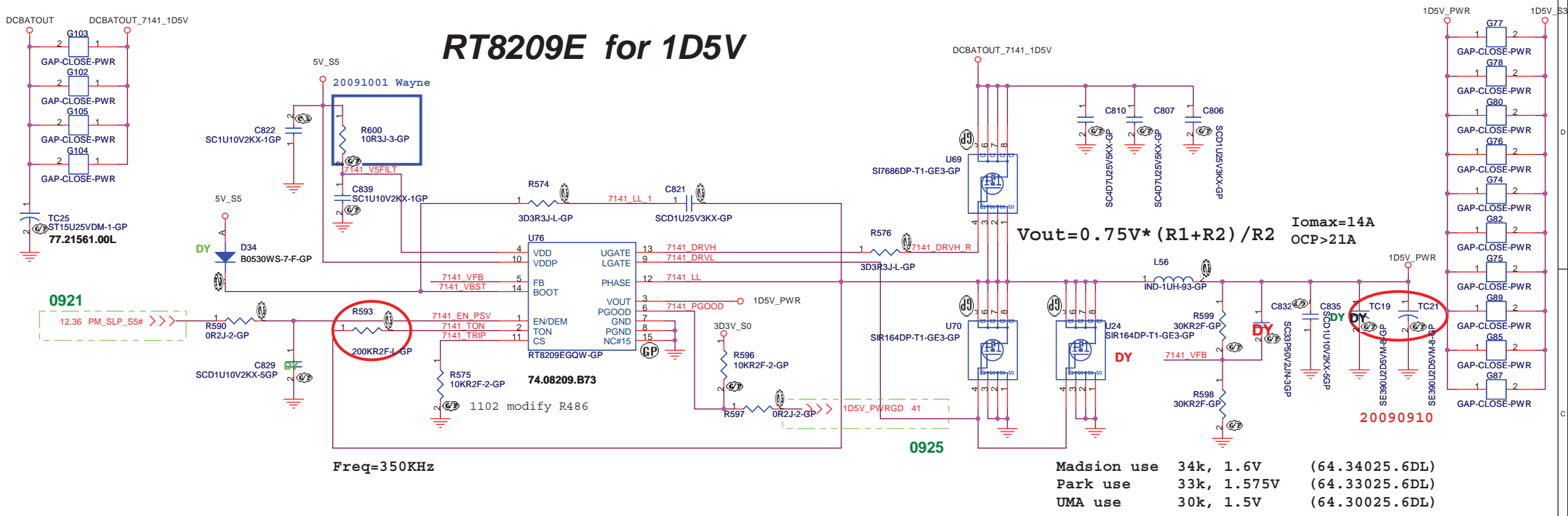
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8223 5V/3D3V**

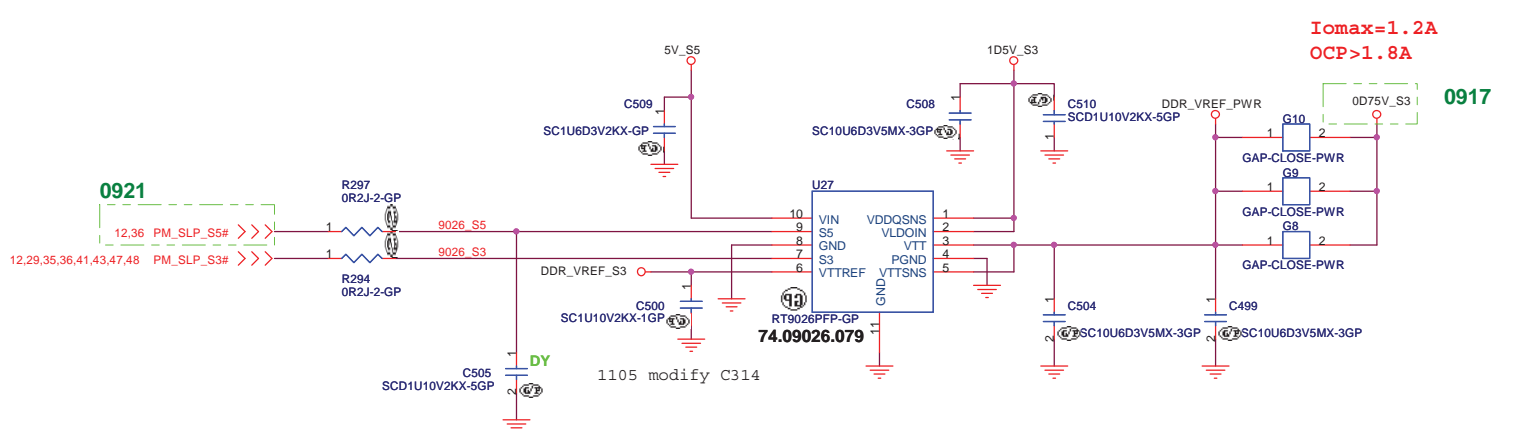
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RT8209E for 1D5V



RT9026 for 0D75V_S3



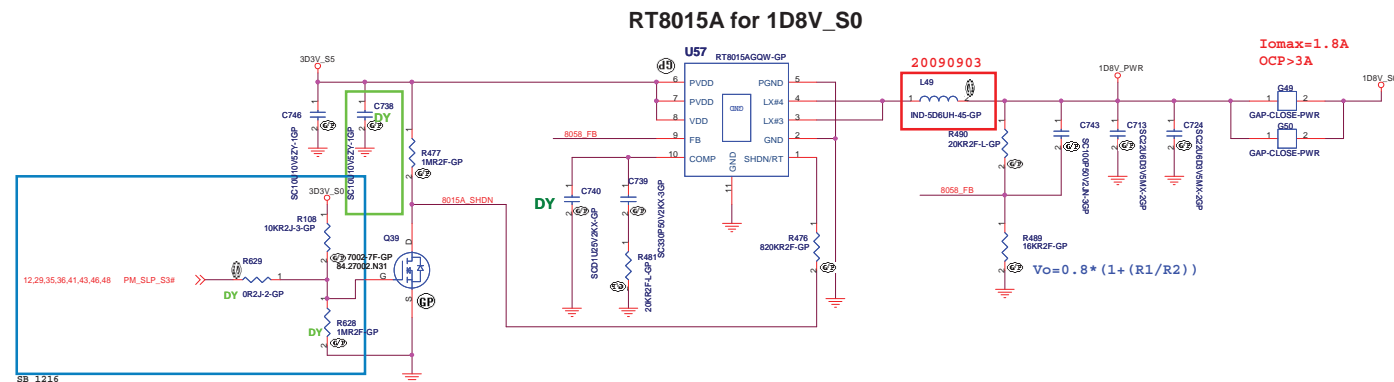
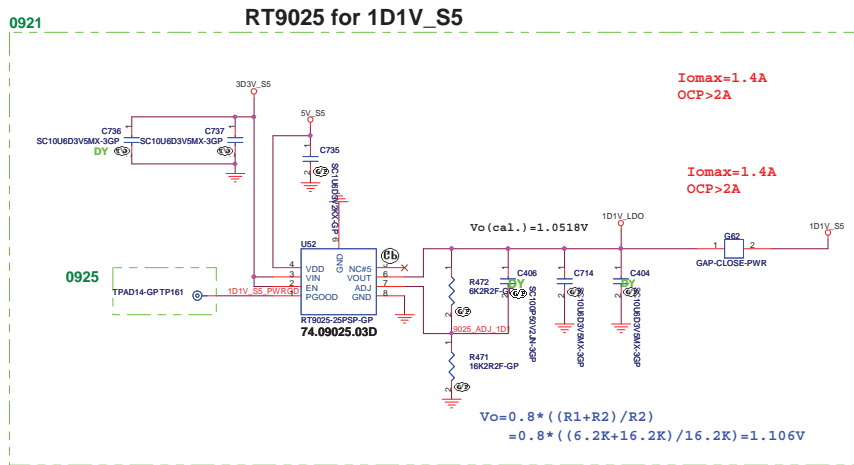
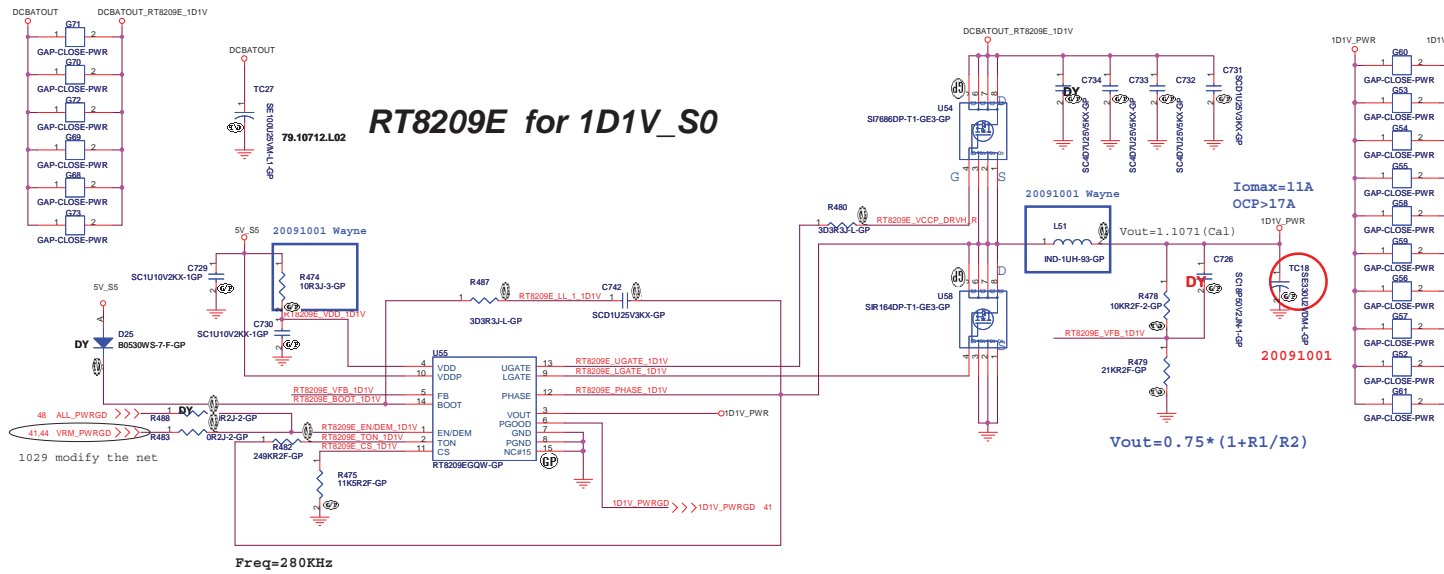
JE70-DN

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

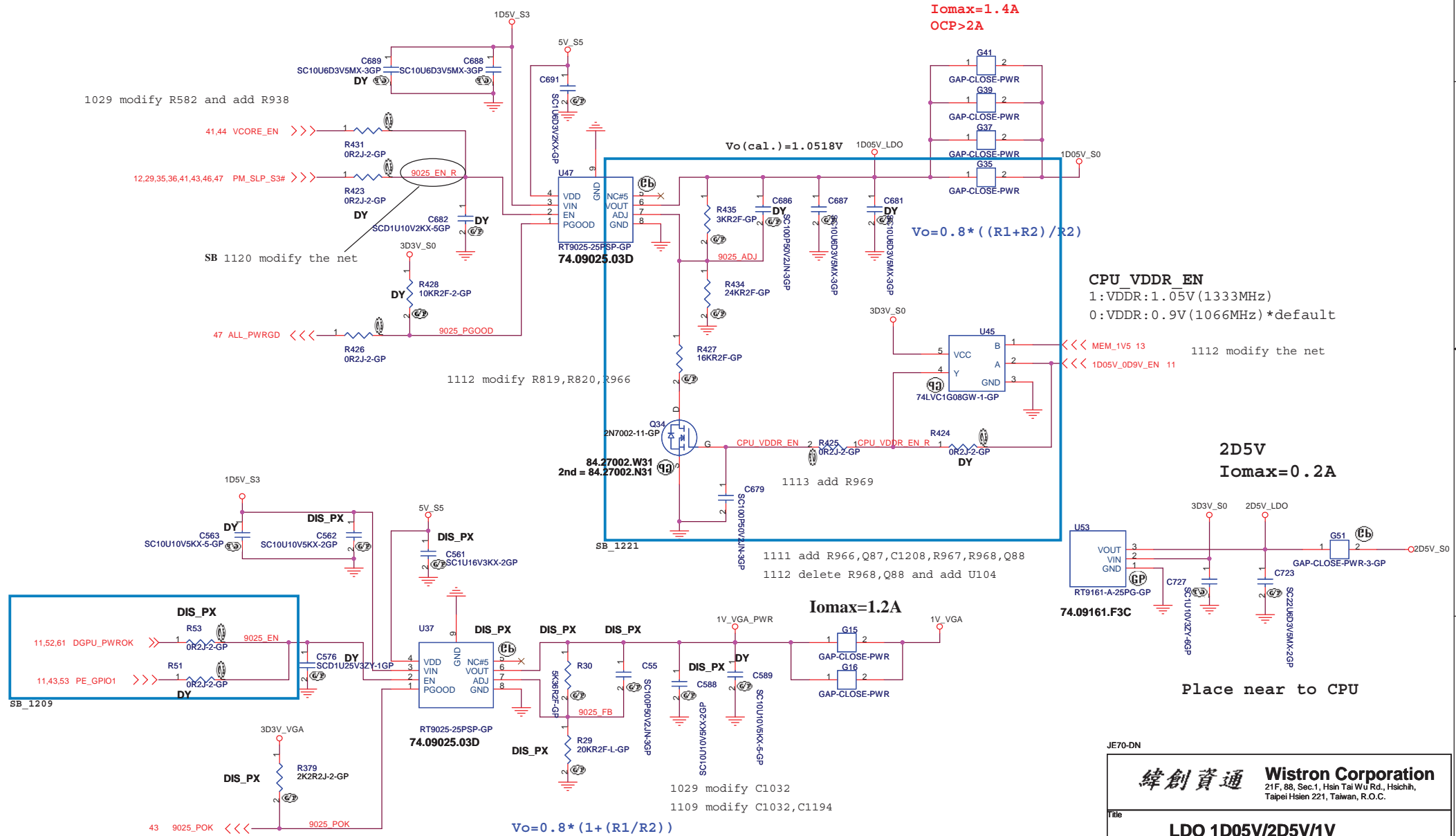
Title: RT8209E 1D5V

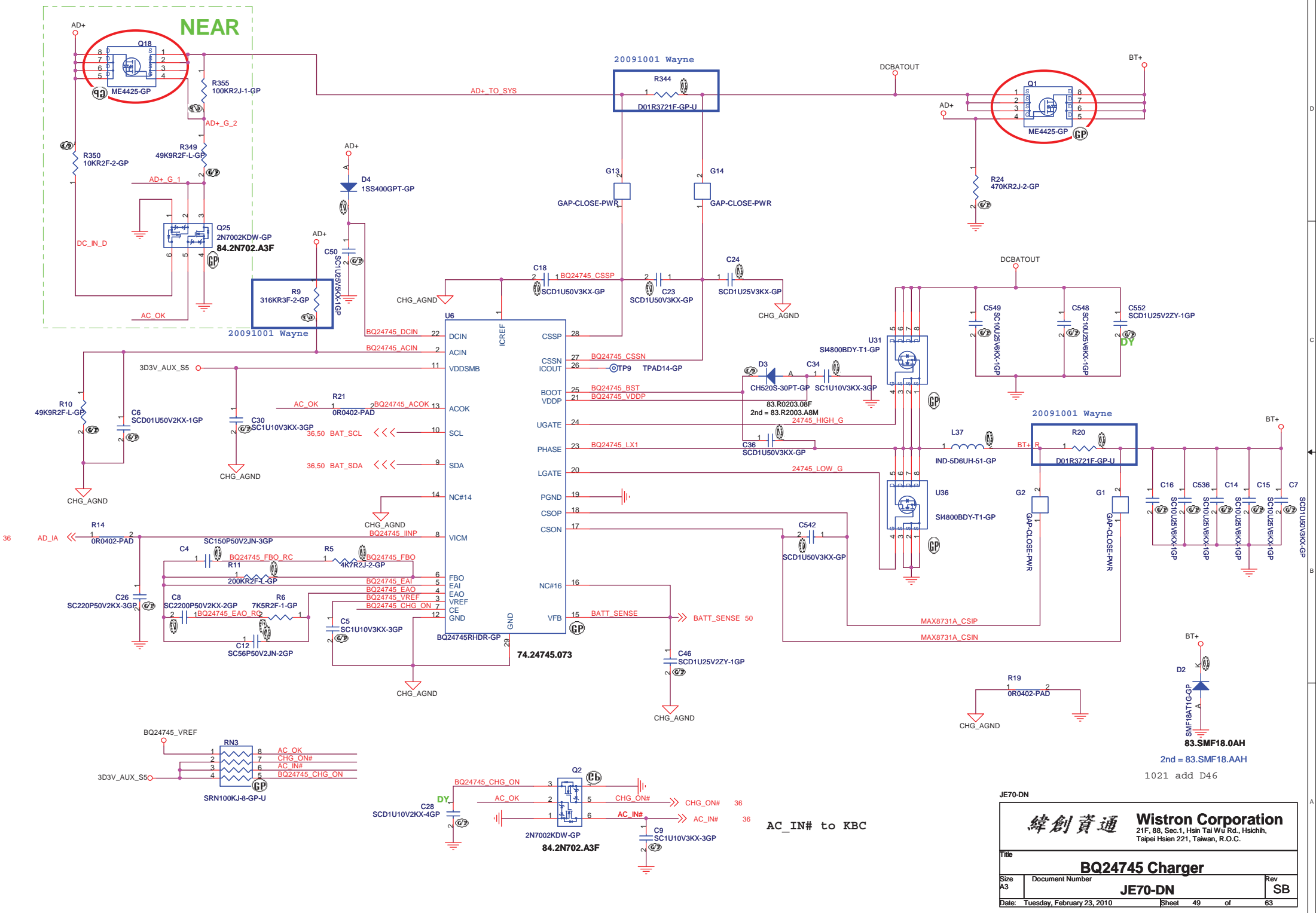
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RT9025 for 1D05V_S0





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緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

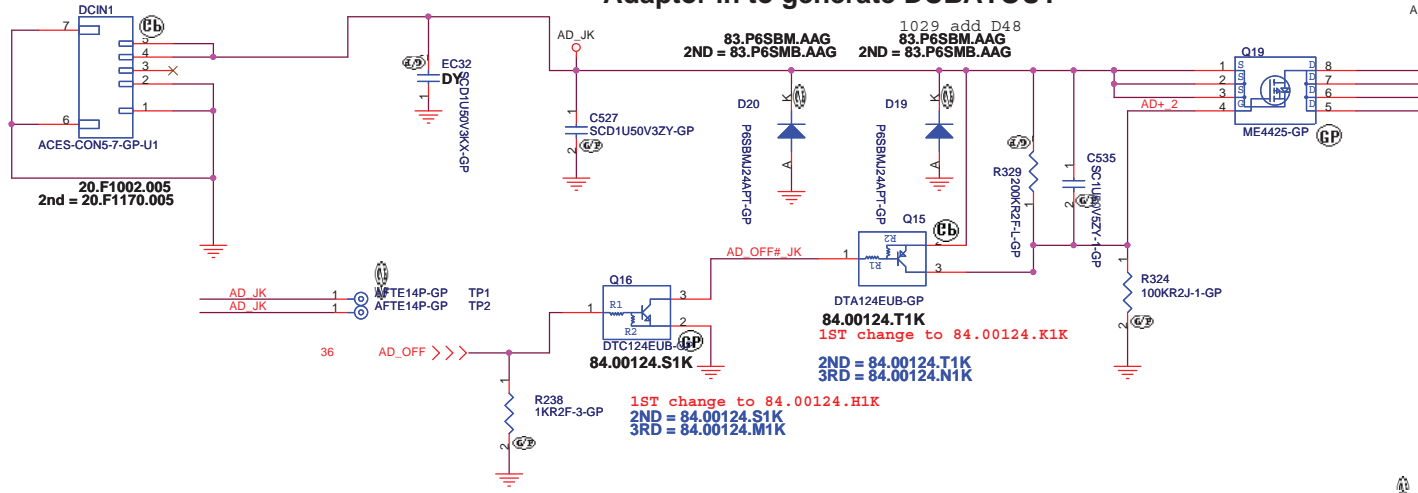
BQ24745 Charger

Title	BQ24745 Charger	
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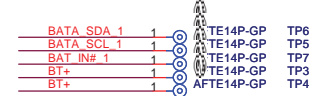
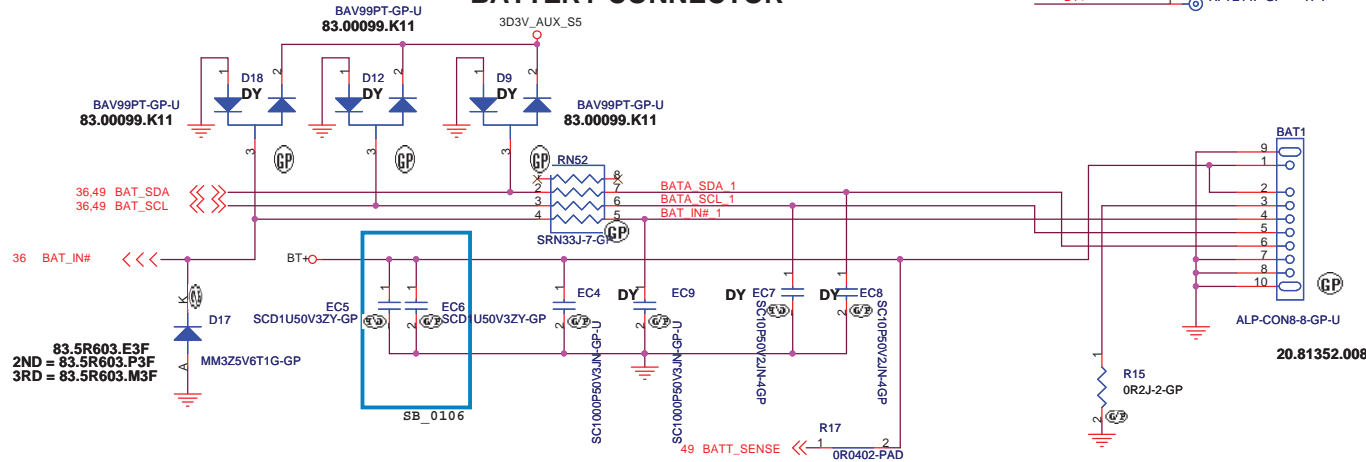
1021 modify DCIN1

1Pin=3A

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



Pin NO	Symbol
1	GND
2	GND
3	SMD
4	SMC
5	TS
6	B/I
7	BT+
8	BT+

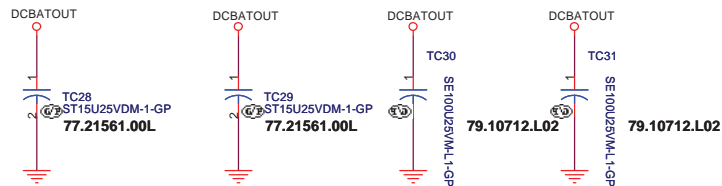
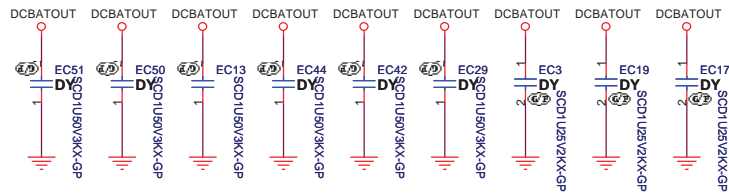
JE70-DN

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

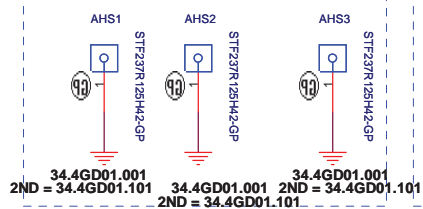
Title: **AD/BATT CONN**

Size: Document Number **JE70-DN** Rev: **SB**

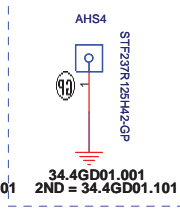
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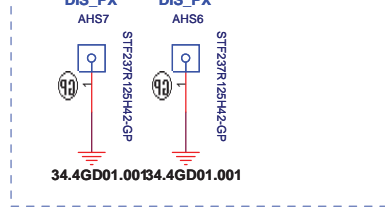
CPU



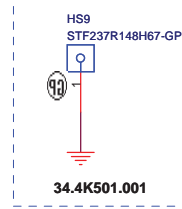
NB



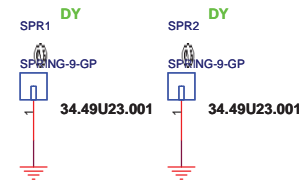
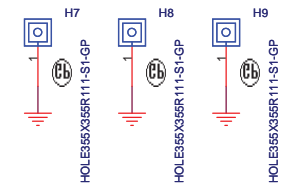
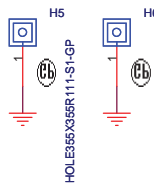
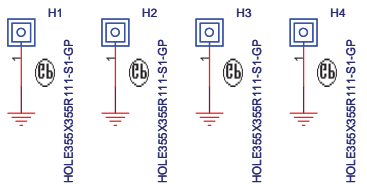
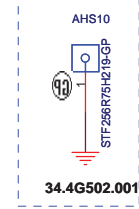
VGA



MEDIA PROCESSOR



MINICARD



Check test point

3D3V_S0	TP171	TPAD14-GP
3D3V_AUX_S5	TP170	TPAD14-GP
3D3V_S5	TP172	TPAD14-GP
5V_S5	TP167	TPAD14-GP
12.36 PM_PWRBTN#	TP169	TPAD14-GP
6.11 CPU_PWRGD	TP163	TPAD14-GP
35.36,45 SS_ENABLE	TP173	TPAD14-GP
6.11 CPU_LDT_RST#	TP162	TPAD14-GP

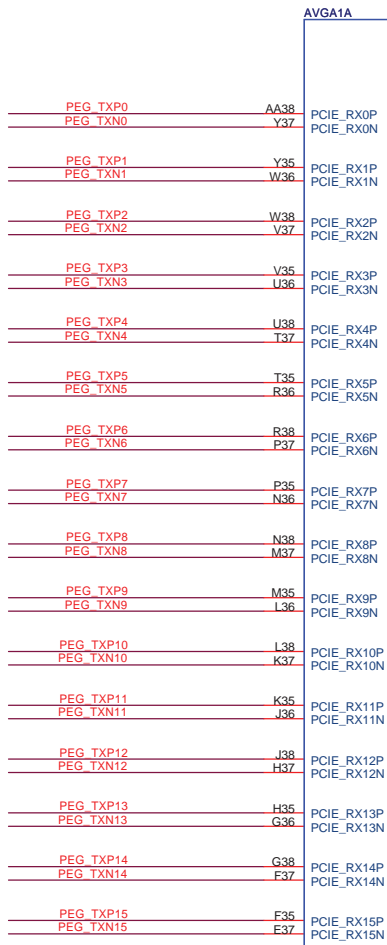
Test Point放在Dimm Door打開可量測處

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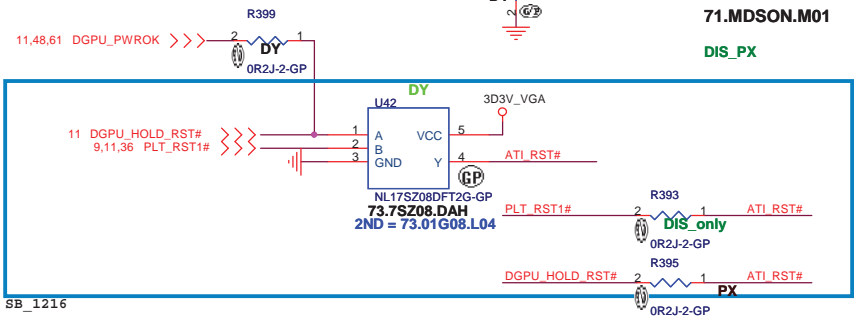
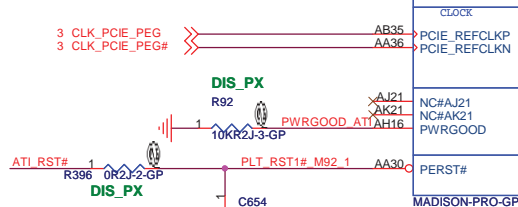
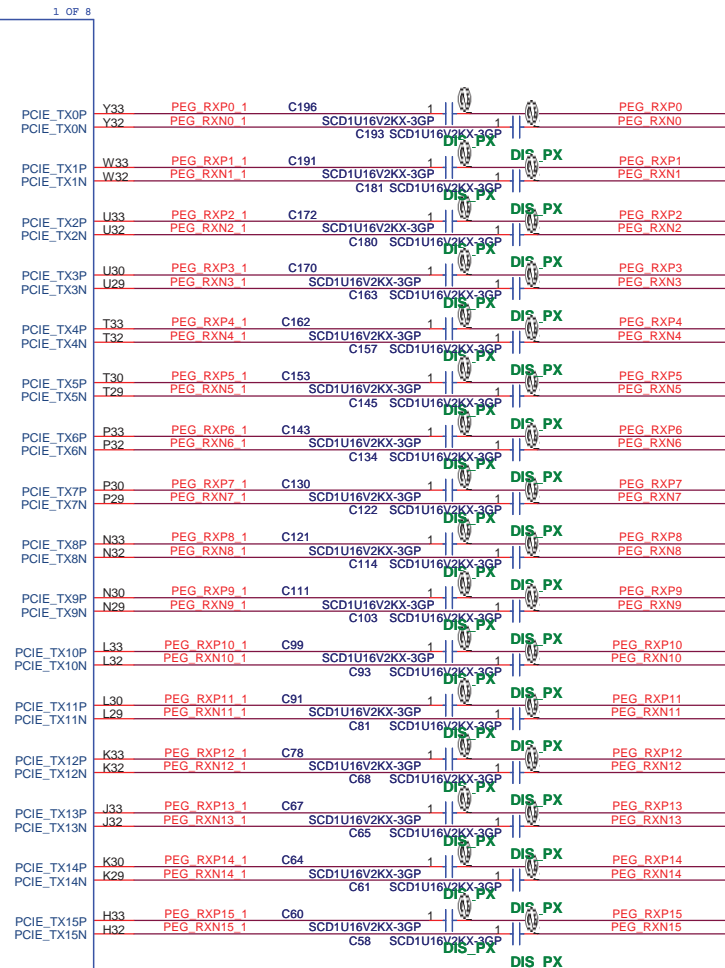
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
EMI/Spring/Boss	
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8 PEG_TXP[15..0] << PEG_TXP[15..0]
8 PEG_TXN[15..0] << PEG_TXN[15..0]

8 PEG_RXP[15..0] << PEG_RXP[15..0]
8 PEG_RXN[15..0] << PEG_RXN[15..0]



PCI EXPRESS INTERFACE



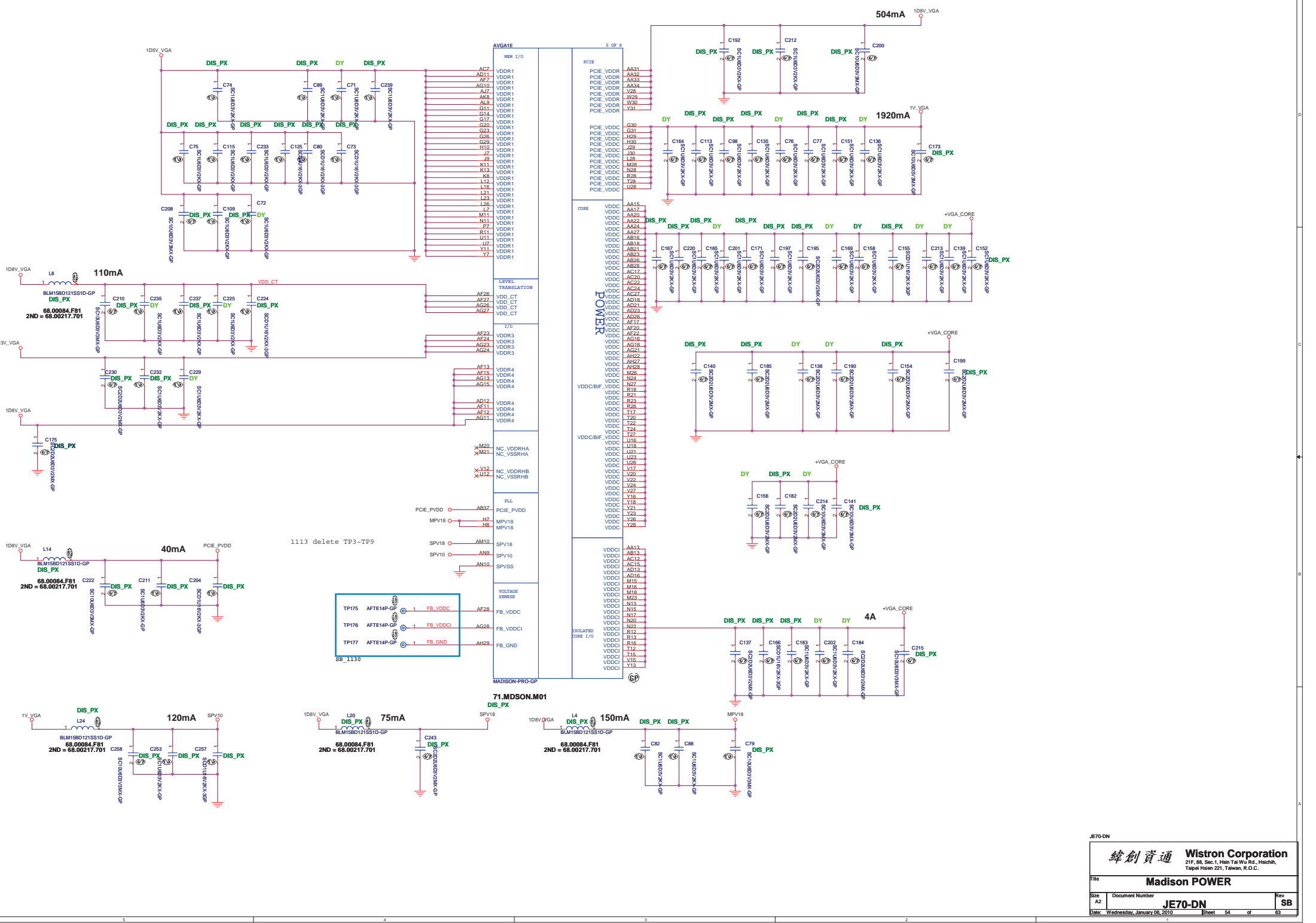
JE70-DN

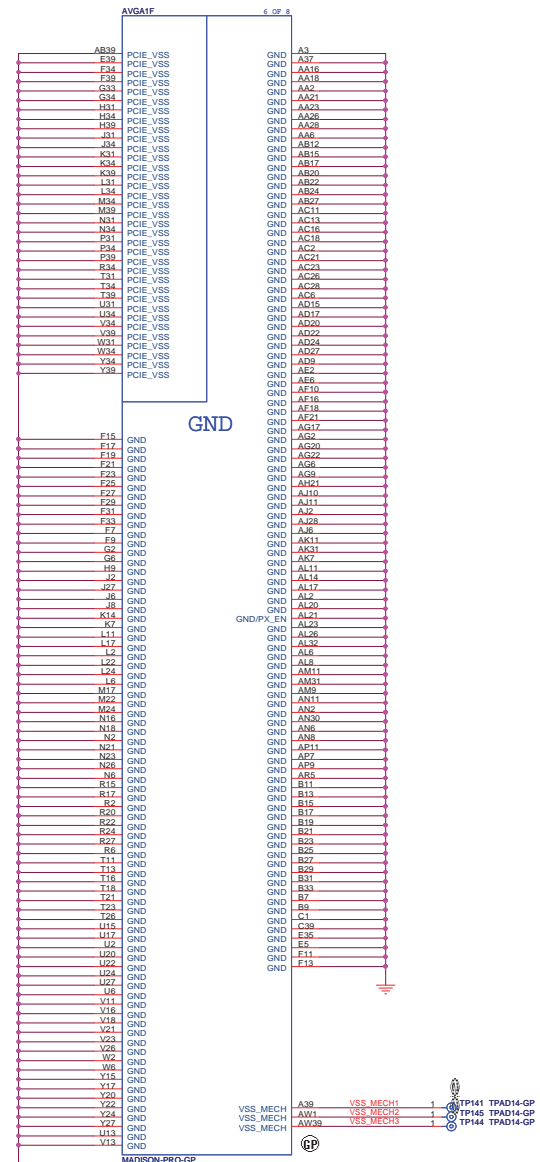
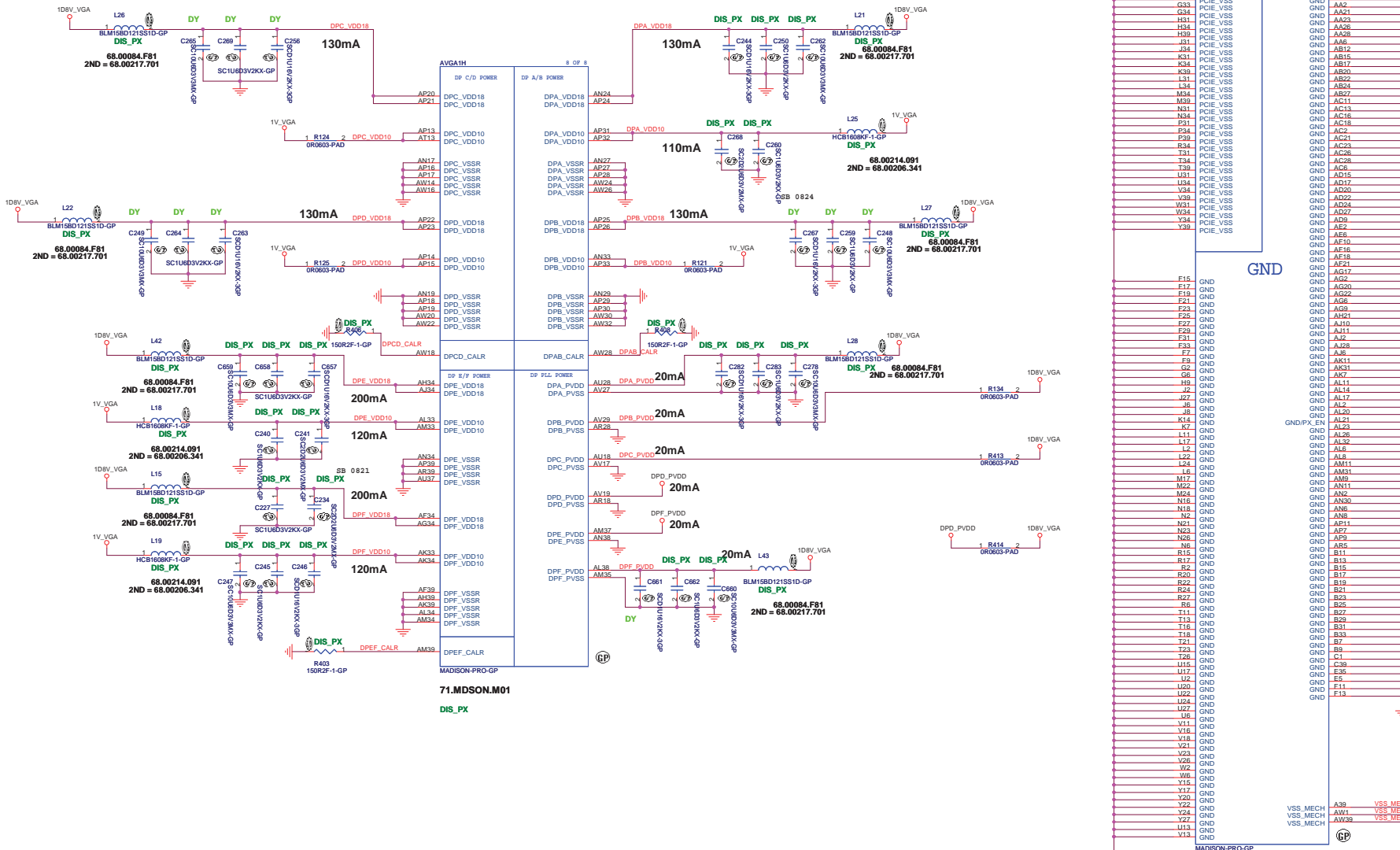
緯創資通 Wistron Corporation
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Title: **Madison PCIE**

Size	Document Number	Rev
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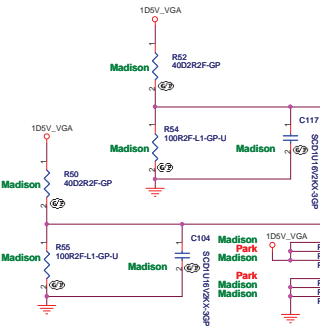
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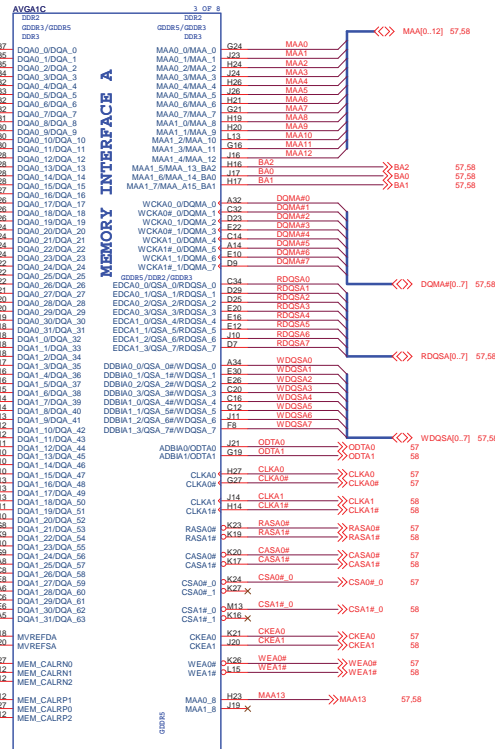


For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



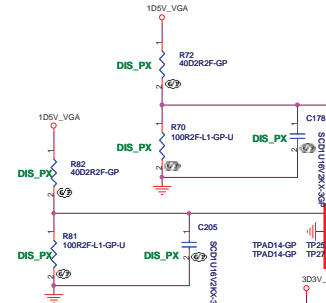
Madison: MEM_CALRP[0,2] signals are used.
Park: MEM_CALRP1 and MEM_CALRN1 are used



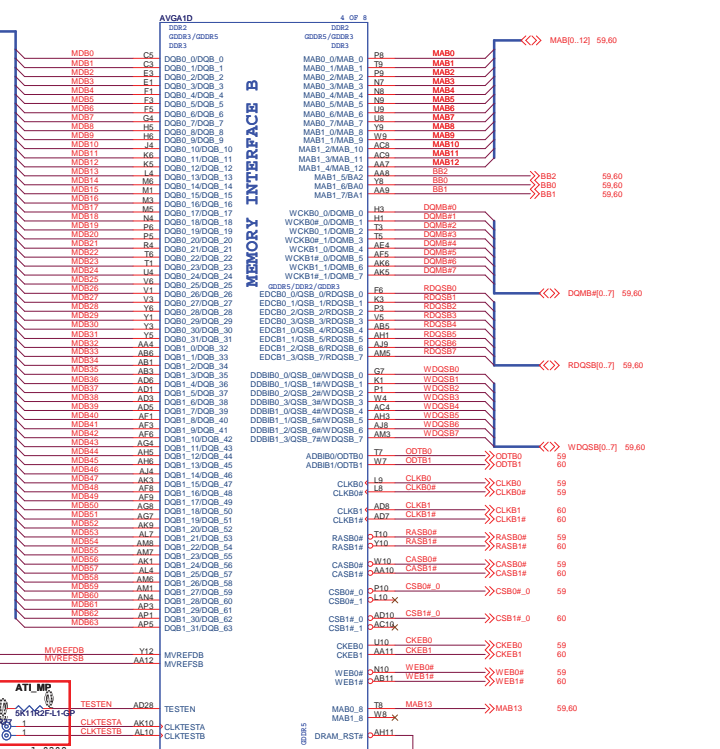
71.MDS0N.M01
DIS_PX

For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



71.MDS0N.M01
DIS_PX



71.MDS0N.M01
DIS_PX

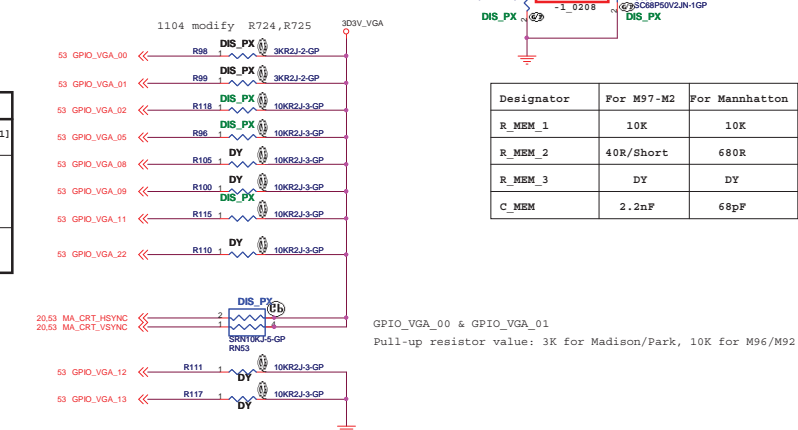
71.MDS0N.M01
DIS_PX

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS
TX_PWRS_ENB (Internal PD)	GPIO0	PCIe FULL TX OUTPUT SWING Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	x
TX_DERMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	x
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
Bios_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size	x x x
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI if adapter is detected 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	x x

AMD RESERVED CONFIGURATION STRAPS

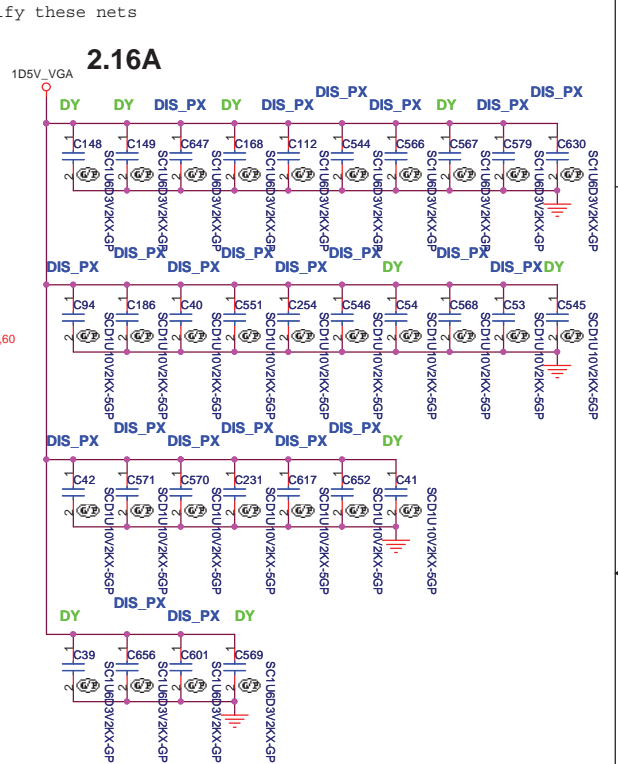
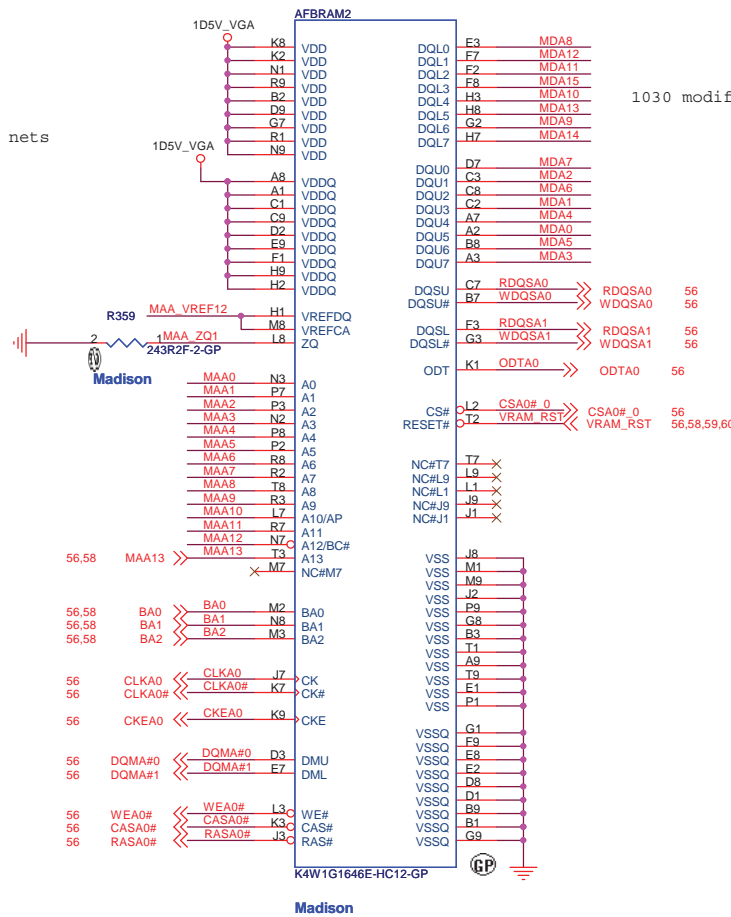
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x	Chingris (formerly PMC)	Fm25LV512A	0100
1GB	x		Fm25LV010A	0101
2GB	x			
4GB	x			



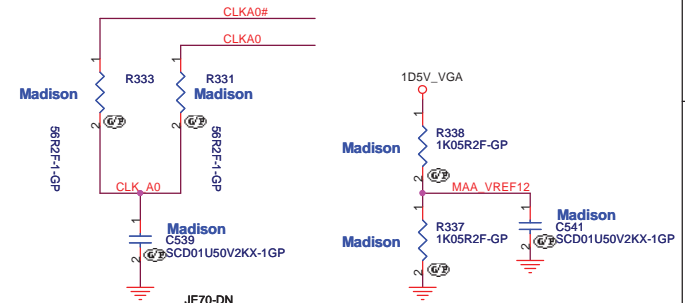
GPIO_VGA_00 & GPIO_VGA_01
Pull-up resistor value: 3K for Madison/Park, 10K for M96/M92

DDR3

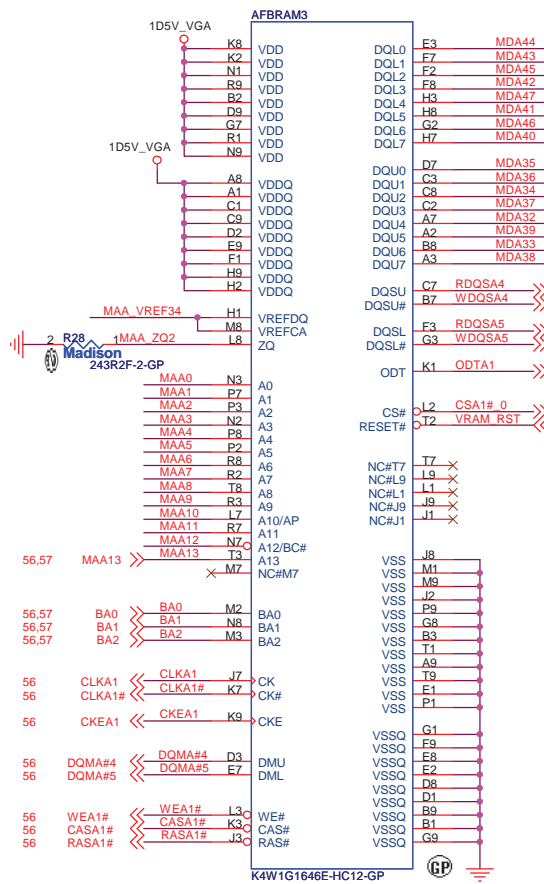


SAMSUNG: 72.41164.H0U (VR.1GB0B.006)
 HYNIX: 72.51G63.C0U (VR.1GB0G.004)

- 56.58 DQMA#[0..7] <<>
- 56.58 RDQSA#[0..7] <<>
- 56.58 WQSA#[0..7] <<>
- 56.58 MAA#[0..12] <<
- 56.58 MDA#[0..63] <<>



DDR3

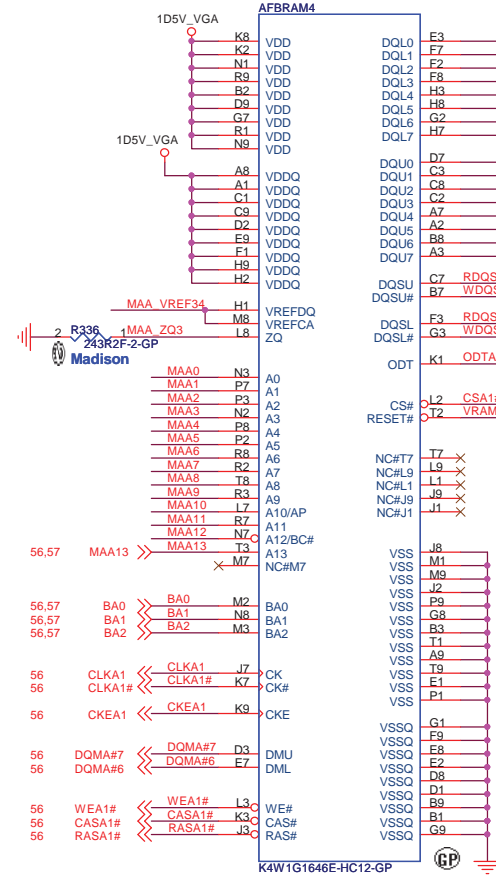


Madison
72.41164.H0U
2ND = 72.51G63.C0U

SAMSUNG: 72.41164.H0U (VR.1GB0B.006)
HYNIX: 72.51G63.C0U (VR.1GB0G.004)

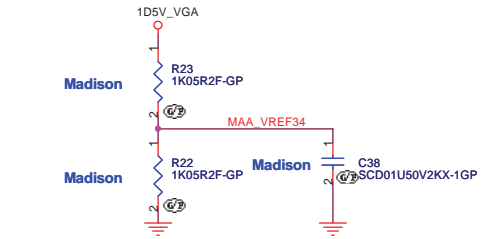
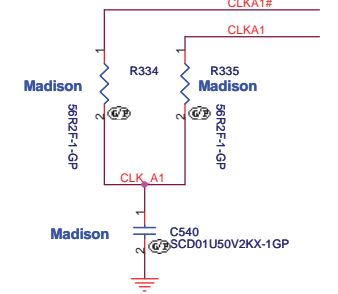
- 56,57 DQMA#[0..7] <<>
- 56,57 RDQSA#[0..7] <<>
- 56,57 WDQSA#[0..7] <<>
- 56,57 MAA#[0..12] <<<
- 56,57 MDA#[0..63] <<>

1030 modify these nets



Madison
72.41164.H0U
2ND = 72.51G63.C0U

1030 modify these nets



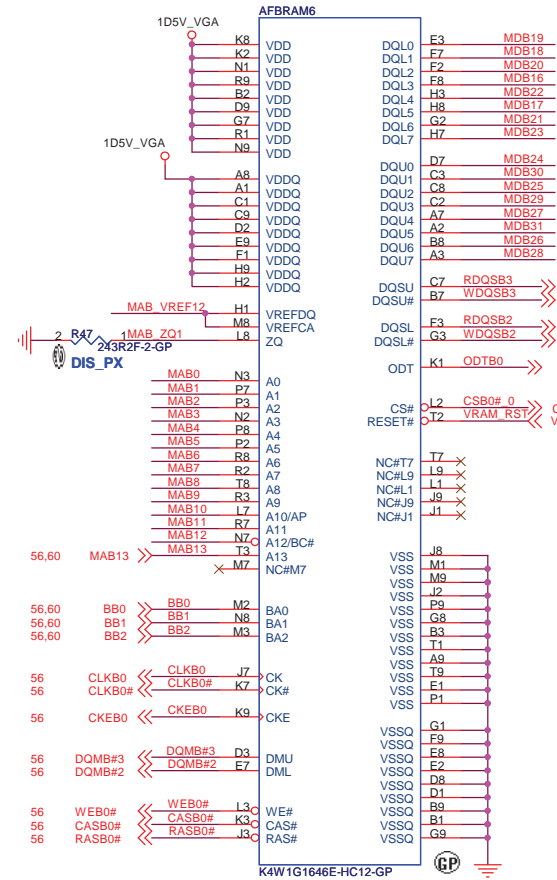
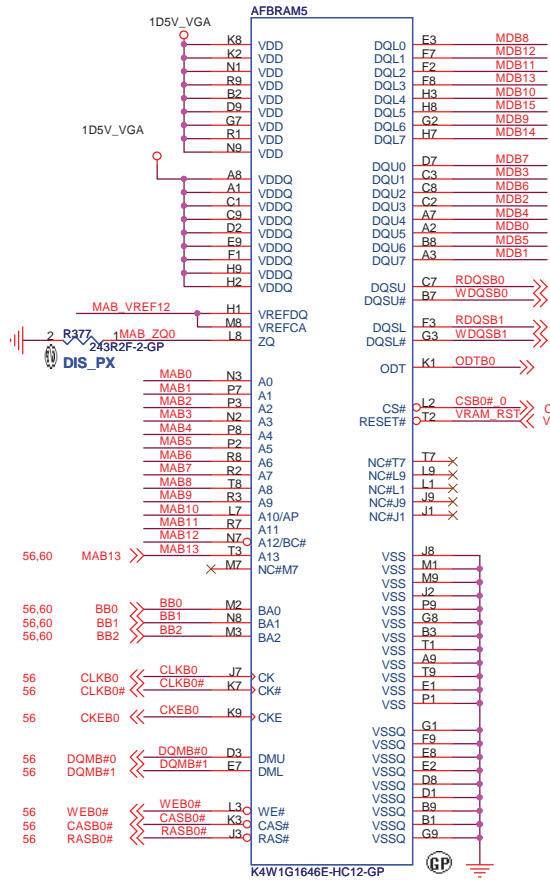
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Title: **VRAM(2/4)**

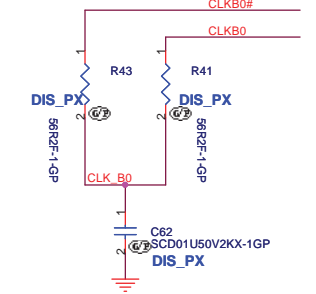
Size: A3	Document Number: JE70-DN	Rev: SB
Date: Tuesday, February 23, 2010	Sheet: 58 of 63	

DDR3



SAMSUNG: 72.41164.H0U (VR.1GB0B.006)
 HYNIX: 72.51G63.C0U (VR.1GB0G.004)

- 56.60 DQMB#[0..7] <<>
- 56.60 RDQSB#[0..7] <<>
- 56.60 WDQSB#[0..7] <<>
- 56.60 MAB#[0..12] <<
- 56.60 MDB#[0..63] <<>



JE70-DN

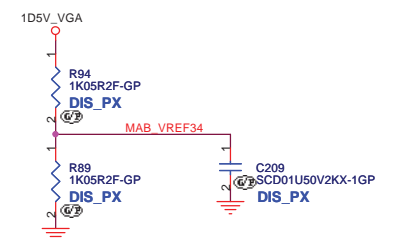
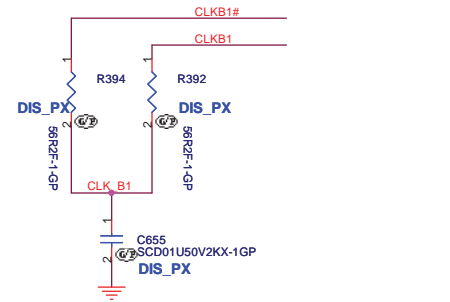
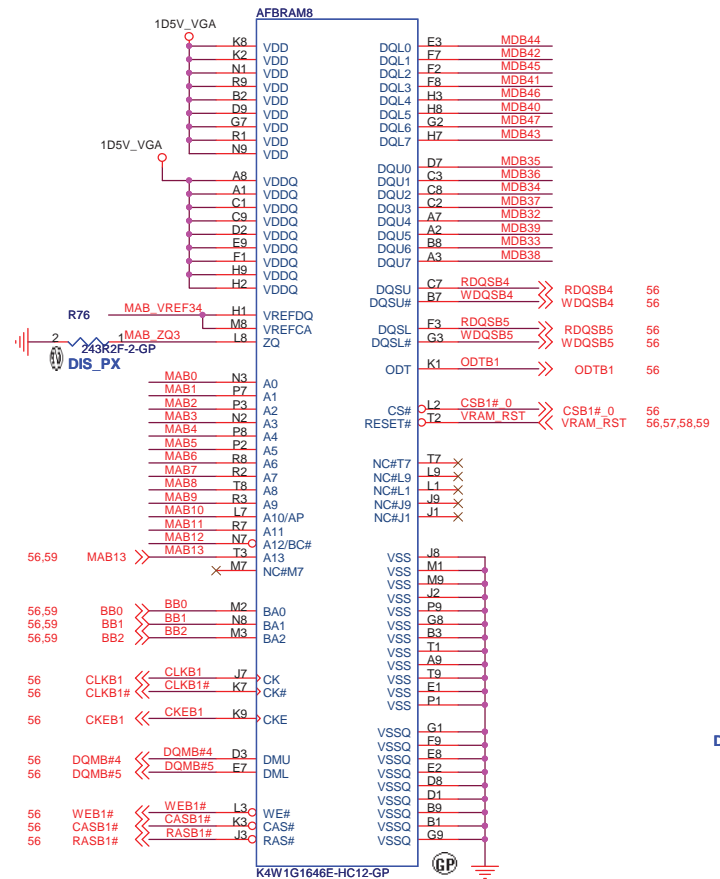
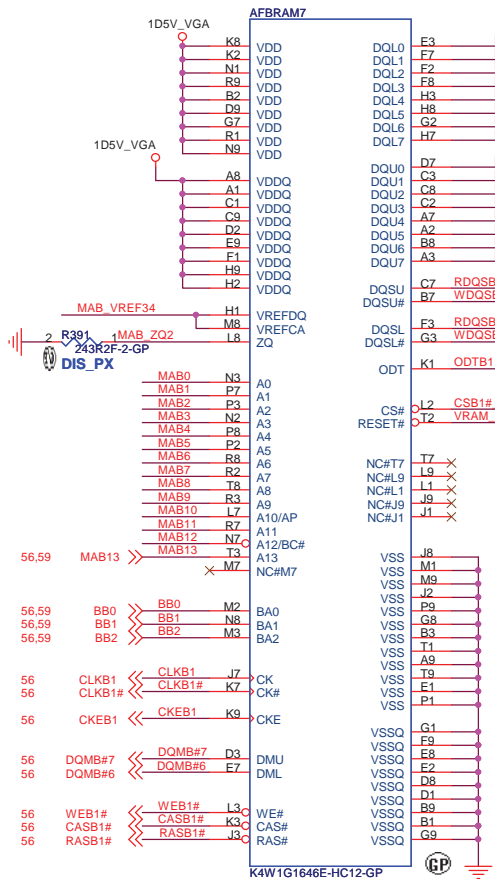
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM(3/4)**

Size: A3 Document Number: **JE70-DN** Rev: **SB**

Date: Tuesday, February 23, 2010 Sheet 59 of 63

DDR3



72.41164.H0U
2ND = 72.51G63.C0U

SAMSUNG: 72.41164.H0U (VR.1GB0B.006)
HYNIX: 72.51G63.C0U (VR.1GB0G.004)

72.41164.H0U
2ND = 72.51G63.C0U

- 56,59 DQMB#[0..7] <<>
- 56,59 RDQSB#[0..7] <<>
- 56,59 WDQSB#[0..7] <<>
- 56,59 MAB#[0..12] <<> MAB#[0..12]
- 56,59 MDB#[0..63] <<> MDB#[0..63]

JE70-DN

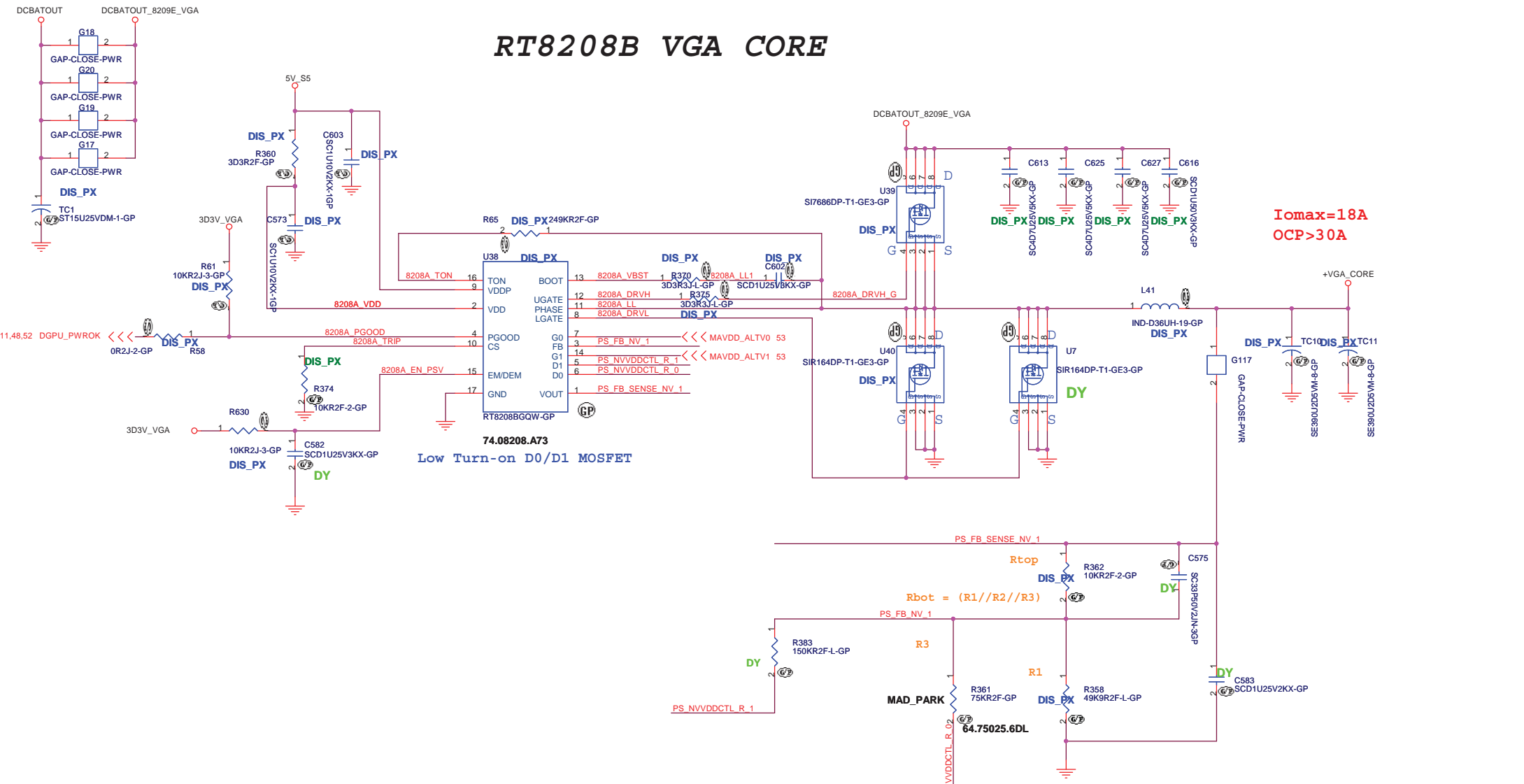
緯創資通 Wistron Corporation
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Title: **VRAM(4/4)**

Size: A3 Document Number: **JE70-DN** Rev: **SB**

Date: Tuesday, February 23, 2010 Sheet 60 of 63

RT8208B VGA CORE



**Iomax=18A
OCP>30A**

**74.08208.A73
Low Turn-on D0/D1 MOSFET**

Madsion : 64.75025.6DL 75k-ohm
Park : 64.34025.6DL 34K-ohm

MAVDD_ALTIVO	Madison Pro	Park XT
0	1.00V	1.12V
1	0.90V	0.90V

JE70-DN

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Title: **RT8209E VGA CORE**

Size: A3	Document Number: JE70-DN	Rev: SB
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1020

Page8: modify these nets for PCIE ports
Page11: add these nets (INT_VGA_EN#,BDP_EN)
Page11: add the net(PX_EN#) and R861
Page11: delete D41,R437,R435
Page12: modify these nets for USB ports
Page14: modify L45,L48,L52,L57,L58,L60
Page18: delete RN95,R423 and add Q73-Q76,R862-R864,D45
Page19: delete CCD1 conn and modify these nets for CCD
Page19: add R865,R866,U100
Page20: add Q77,R867
Page24: add modify these nets for BT
Page25: add modify these nets for USB board
Page26: modify these nets for PCIE port (LAN)
Page26: delete the net(LOW_PWR)
Page33: modify these nets for PCIE ports(MINI1,MINI2)
Page33: modify these part's names
Page33: modify these nets for USB port(MINI2)
Page40: 1020 modify PWR_LED1,CHARGER_LED1
Page51: add screw holes

1021

Page5: modify these nets
Page6: delete HDT1 conn and add TP246-255
Page16: modify these nets of ADM1
Page16: add R880-883
Page17: modify these nets of ADM2 and ADM3
Page17: add R884-R891
Page18: add RN114-117
Page23: modify ODD1
Page25: modify the net(COVER_SW# 1)
Page30: modify LOUT1,AMIC1 and MICIN1
Page33: modify AMINI1 and MINI2
Page36: modify these nets and add R873-878
Page38: modify these devices(ATPCN1_SW_R,SW_L)
Page40: modify PWR_LED1,CHARGER_LED1
Page49: add D46
Page50: modify DCIN1, BAT1 and add R879

1021

Page26: modify U6 (LAN IC)

1023

Page12: delete R538,R539 and add RN118
Page12: delete R442,R443,R445 and add RN119
Page12: delete R570-R572 and add RN120
Page12: delete C368-C371,C446,C449,C686,C687
Page18: swap these nets
Page21: add R892-R900,Q78
Page25: delete TC29,TC24,EC79,EC83
Page25: modify the net of USB_CN1 pin32
Page36: delete R258 and RN89,RN122
Page36: delete R382 and add U101
Page36: delete R892,R483,R497,R478 and add RN123
Page36: delete R410,R416 and add RN121,R892
Page37: add R901,R902
Page40: modify the pin5 define of PWR_CN1 and Q11
Page43: add TC53,TC54,U44
Page61: modify TC52, R295 and add R903,Q79

1026

Page3: add R904 and modify C509,R232,R235
Page6: add R913,RN124
Page6: modify RN42,RN84,R612,R611,R364
Page17: modify these nets
Page19: modify R588
Page21: modify U73 and delete R504
Page22: modify SATA1
Page35: delete R311 and modify FAN1
Page36: modify RN121
Page36: modify AKB1
Page37: modify RN94 and the net(SPI_WP#)
Page43: add R097-R911,D47,Q80
Page53: add R905,R906

1027

Page10: delete C651,R320,R316
Page11: modify C543,C306,C424,C433
Page11: delete R148
Page12: modify the net(PM_RSMRST#)
Page43: modify the net(PM_RSMRST#)

1028

Page3: add the net(LAN_CLKREQ#) to RN70
Page4: modify C704-C706
Page4: modify R401
Page9: delete R576,R578
Page10: modify C62,C91
Page11: delete R207,C337,D5,R208
Page11: delete the net(PCI_REQ#6)
Page12: delete RN120 and add R570
Page13: modify the net(SATA_LED#)
Page14: add C1198,C1199 and modify C815,C811
Page16: add R934,R935
Page18: add U102,R915-R919
Page18: modify R432,U3,U8
Page19: add U103,R920-R922 and delete D35
Page20: add R936,R937 and modify R325,R323,R354
Page21: delete RN8,RN13,RN15,RN19
Page21: modify C819-C821,C823,C824,C826-C828
Page25: add L82,R924,R925
Page29: modify R489
Page30: modify R622,R619 and add RN125
Page36: delete R384 and modify the net(KBC_BL_ON_IN)
Page36: add R926
Page43: delete R583,D33,U74,R340,Q34,R584
Page43: add R930-R933,Q84,Q85,C1197
Page43: add R927-R929,Q8-Q83
Page43: delete R591-R595
Page48: modify these nets(DGPU_PWROK,9025_POK)

1029

Page6: delete R364,R612 and add RN127,R946
Page6: delete C331,C338
Page17: delete C348,C340,C350,C342
Page18: modify these nets
Page19: add EC99,EC100
Page24: add EC101,EC102
Page25: add L82,R924,R925,R939,EC103
Page35: delete D17,D18,U39,U43,R298,R322,R330,R338,R337,C646,C656
Page35: delete U38,R321,R308,R309,R314,C645
Page36: add R945,RN126
Page43: delete U44,R342,C675
Page47: modify the net
Page48: modify R582 and add R938
Page50: add D48
Page53: add R940-R943
Page61: add R944,Q86

1030

Page3: modify these nets
Page8: modify these nets
Page11: modify the net
Page12: add R949
Page14: delete C760,C721,C805,C800,C769,L64 and add R948
Page18: modify these nets
Page30: add R950-R953 and modify EC24,EC51
Page57: swap these nets
Page58: swap these nets
Page59: swap these nets
Page60: swap these nets

1102

Page3: swap these nets
Page6: swap these nets
Page12: swap these nets
Page13: swap these nets
Page18: swap these nets
Page25: modify USB_CN1
Page30: modify these names of these nets

1103

Page3: modify X5,C508,C509
Page11: modify R164
Page14: modify L51,L59
Page21: modify these names of nets
Page21: add RN8,RN13,RN15,RN19
Page36: add the net(A_MIC_SUPPORT#)

1104

Page6: delete TP246-255 and add HDT1
Page9: modify the value of RN11
Page24: add AFTP (TP256-TP258)
Page24: add AFTP (TP259-TP263)
Page25: add AFTP (TP264-TP280)
Page35: add AFTP (TP281,TP282)
Page36: add AFTP (TP283-TP307)
Page38: add AFTP (TP308-TP312)
Page40: add AFTP (TP313-TP319)
Page56: modify these values of R724,R725

1105

Page3: delete R191-R194,R198-R200,R204-R206
Page3: delete R214,R213,R187-R190,R220,R222
Page3: add RN128-RN136
Page3: modify R215,R197,R238,R229
Page6: delete R104,R105,R108,R110
Page6: add RN137,RN138,R954
Page6: modify R366
Page6: modify Q8,R81,R375,C205
Page8: delete TP16,TP17,TP20,TP21
Page9: add R955,R956 and modify R29
Page11: delete R144,R141,R137,R138
Page12: add the net(SUS_STAT#) and R957
Page12: modify these nets
Page21: swap these nets
Page28: modify C713,R634 and delete R626
Page33: modify these nets
Page33: modify R879

1106

Page3: modify these values of R169,R170
Page12: add R957,R958
Page12: add these nets(USB_OC#0,USB_OC#2,USB_OC#3)
Page16: modify R880-R883,ADM1
Page17: modify R888,R890,ADM2
Page21: add R959
Page35: modify FAN1
Page35: modify PWR_CN1
Page35: modify ATPCN1
Page36: swap these nets(KBCRCIN#,KA20GATE)
Page37: swap RN94
Page44: swap RN45
Page51: add EC104-EC112 for EMI demand

1107

Page3: swap RN129,RN130,RN132
Page6: swap RN137
Page51: add EC104-EC112 for EMI demand

1109

Page45: modify the value of R448 to 64.15035.6DL for Power team demand
Page45: modify R462,R470 for Power team demand
Page46: modify L25 for Power team demand
Page48: modify C1032,C1194

1110

Page5: swap RN48
Page7: add C1200-C1207
Page11: add R960,R961
Page25: modify USB1
Page43: add TC55,TC56
Page52: add R962

1111

Page11: add R965
Page21: modify HDM11
Page28: add R626
Page33: delete C550,C549 and add R963
Page36: delete RN121 and add R964
Page45: modify TC39,TC40
Page48: add R966,Q87,C1208,R967,R968,Q88

1112

Page13: modify the net
Page48: delete R968,Q88
Page48: modify R819,R820,R966
Page48: modify the net

1113

Page3: delete R170,EC50
Page25: delete R939,TP272,EC103
Page46: modify TC43
Page48: add R969
Page53: add R968
Page53: delete TP103,TP122,TP160,TP178
Page53: delete these TP (TP157,TP145...))
Page54: delete TP3-TP9

1117 (Rename)

Page18: swap these nets
Page22: delete D29-D31,D33
Page36: modify RN31
Page61: delete G24-G29
Page61: modify the net

1118

Page14: add R620 and modify R184
Page15: modify R412,R411
Page36: swap AKB1 pin1-pin26

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File		HISTORY(1/2)	
Size	Document Number	JE70-DN	
K2		Rev SB	
Date:	Thursday, November 19, 2009	Sheet	62 of 63

SA to SB

1120

Page19: modify these nets

Page48: modify the net(9025_EN)

1124

Page38: modify ATPCN1

1126

Page25: modify these nets

Page36: add TP174

JE70-DN

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Title		HISTORY(2/2)		Rev	SB
Size	42	Document Number	JE70-DN		
Date	Friday, December 25, 2009	Sheet	63	of	63