Page	Title of schematic page	Rev.	Date
01	Page List	1A	
02	Block Diagram	1A	
03	Change List	1A	
04	SNB 1/4(HOST&PCIE)	1A	
05	SNB 2/4(DDR3 I/F)	1A	
06	SNB 3/4(POWER)	1A	
07	SNB 4/4(GND/Strap)	1A	
08	PCH 1/6(DMI/FDI/VIDEO)	1A	
09	PCH 2/6(SATA/RTC/HDA/LPC)	1A	
10	PCH 3/6(PCIE/USB/CLK/NV)	1A	
11	PCH 4/6(GPIO/CPU/STRAP)	1A	
12	PCH 5/6(POWER)	1A	
13	PCH 6/6 (GND)	1A	
14	DDR3 DIMM-0-STD	1A	
15	DDR3 DIMM-1-STD	1A	
16	WPCE791L & FLASH	1A	
17	CRT/LVDS/CAMERA	1A	
18	CARD READER(RTS5209)	1A	
19	HDMI/THERMAL	1A	
20	USB	1A	
21	LAN (RTL8111F)	1A	
22	WLAN/KB-BL	1A	
23	HDD/ODD/G-SENSOR/TP/FAN	1A	
24	Audio ALC258-GR	1A	
25	LED/RF/PS	1A	
26	POWER +VCC_CORE (ISL95835)	1A	
27	POWER 3VPCU&RVCC5(PM6686)	1A	
28	POWER 1.5VSUS/VTT_MEM	1A	
29	POWER +1.05V(G5602R41U)-15A	1A	
30	POWER VCCSA/VCCIO	1A	
31	POWER VCC1.8/Thermal	1A	
32	POWER(BAT IN / ADA IN/ UL)	1A	
33	POWER CHARGER (ISL88731C)	1A	
34	POWER VGA_CORE(OZ8117)	1A	
35	POWER VGA_VCC1.8/VCC1.0	1A	
36	Thames_PCIE I/F/DP Power	1A	
37	Thames_IO & STRAP	1A	
38	Thames_MEMORY/THERM	1A	
39	Thames_POWER	1A	

Page	Title of schematic page	Rev.	Date
40	Thames_DDR3_A_512M	1A	
41	Thames_DDR3_B_512M	1A	
42	HOLE/EMI/KB	1A	
43	IO PORT LIST	1A	

* : No mount
E@ : For DIS GFX only
I@ : For INT GFX only

ZS/HK5 Chief River BLOCK DIAGRAM

02

DDR3 : 1.5V

Dual Channel

P14~P15

DDR3 : 1066/1333/1600 MHz

intel

Ivy Bridge

PCI-E X16

DDR SYSTEM MEMORY

rPGA 988

(37.5mm X 37.5mm)

FDI DMI

P4~P7

PCIE2

5GT/s

AMD

Thames-Pro

Package type : GB1b-128 P36 ~ P39

VRAM 1GB / 2GB P40 ~ P41

VRAM 1GB / 2GB P40 ~ P41

X8 2.7GT/s FDI

DMI X4 5GT/s

INT_CRT

P17

INT_LVDS

P17

INT_HDMI

P19

Camera P17

PORT10

WiMax/BT P21

PORT12

USB I/O P20

PORT3

USB I/O P20

PORT1

USB I/O P20

PORT2

USB I/O P20

PORT0

USB 2.0

USB 3.0

P21 HDD SATA0 6Gb/s

P21 ODD SATA3 3Gb/s

FDI DMI

SATA Gen3

SATA Gen2

intel

<PCH>

iGFX Interfaces

Panther Point

USB

mBGA 989

(25mm X 25mm)

HDA

SPI

P8~P13

5GT/s PCI-Express Gen2

PCIE6 PCIE1 PCIE4

Giga-LAN

RTL8111F P21

RJ45

P21

WLAN/Widi/BT P21

BT Combo : Atheros WB195

WiMAX : Kelsey Peak KSP(612BNXHWG)

802.11bgn/Intel/KsP_1x2_BT

Card Reader

RTS5209

P18

MS SD-XC

Audio CODEC

ALC258-GR

P24

Azalia

HP Jack MIC Jack SPK DMIC

P24

P24

P24

P24

SPI ROM 8MB P9

LPC

EC

NPCE885L

P16

Touch Pad P20

Keyboard P25

Power LED
Sleep LED
SATA LED
Battery LED
RF LED
SCROLED
CAPSLED
NUMLED
CARD LED

Button
QWA#
VAIO#
ASSIST#
Power SW

Note:
HM65 does not support USB 6 & 7
HM65 does not support SATA 2 & 3

Change List

HK5_MB_SCH_PVT_001

P21--Add LQ2[CHT2301PT],LR18[47K],LC27[0.01UF],LC26[1U].

P21--No mount LR15[0 ohm].

P21--LR16 pin1 connect to "+3V_S5".

Reason : Modify circuit for LAN power Rise time.
Possible Risk: No.

HK5_MB_SCH_PVT_002

P22--Delete R409[3.01K].

P22--U29 value change to "G5240/TPS2051".

Reason : Modify circuit for K/B Backlight protect.
Possible Risk: No.

HK5_MB_SCH_PVT_003

P4--Delete R332[0 ohm].

P5--Delete R171[0 ohm].

P6--Delete R189,R186,R197[0 ohm].

P8--Delete R438,R38,R37,R439[0 ohm].

P9--Delete R121,R67,R65,R122[0 ohm].

P10--Delete R73[0 ohm].

P12--Delete R102,R126,R299,R302[0 ohm]

P14--Delete R312[0 ohm]

P15--Delete R309[0 ohm]

P16--Delete KR39,KR60,KR6,KR30[0 ohm]

P18--Delete ML1,MR5[0 ohm]

P21--Delete LR12[0 ohm]

P22--Delete R96[0 ohm]

P23--Delete R461 ,R462 [0 ohm]

P24--Delete AL1,AR21,AR8,AR23,AR24,AR25,AR22,AR15,AR16,AR17,AL3,AL4,R418,AR20[0 ohm]

P27--Delete PR490,PR502[0 ohm]

P31--Delete PR504[0 ohm]

Reason : Cancel 0 ohm.
Possible Risk: No.

HK5_MB_SCH_PVT_004

P27--Delete PR513.

Reason : Cancel 0 ohm.
Possible Risk: No.

HK5_MB_SCH_PVT_005

P26--PR100,PR108,PR109 change to short PAD.

P27--PR325,PR318,PR324,PR326 change to short PAD.

P28--PR352,PR356,PR360,PR357,PR358 change to short PAD.

P30--PR388,PR390,PR392 change to short PAD.

P31--PR413,PR429,PR430,PR440,PR441 change to short PAD.

P33--PR271 change to short PAD.

Reason : Cancel 0 ohm.
Possible Risk: No.

HK5_MB_SCH_PVT_006

P23--reserve D9 and D10

Reason : reserve ESD diode
Possible Risk: No.

HK5_MB_SCH_PVT_007

P25--change CON1 form 12Pin to 10pin

Reason : delete samll board LID fuction
Possible Risk: No.

HK5_MB_SCH_PVT_008

P42-- Del J5,J6,J7,J8,J9,J10 for EMI request

Reason : For EMI
Possible Risk:
No.

HK5_MB_SCH_PVT_009

P23-- Delete reserve ESD diode D23 ,D24

Reason : ESD test PASS , we don't need to reserve
Possible Risk: No.

HK5_MB_SCH_PVT_010

P23-- change ODD ESD diode form Rclamp0502n to SR05

Reason : for SMT issue , Rclamp0502n easy to short , we change to SR05 and still reserve it
Possible Risk: No.

HK5_MB_SCH_PVT_011

P25-- change R225 form 150ohm to 40.2ohm

Reason : for W/L LED dark issue
Possible Risk: No.

HK5_MB_SCH_PVT_012

P25-- change R224 R226 R349 form 150ohm to 75ohm

Reason : for HDD ,Battery and card reader LED dark issue
Possible Risk: No.

HK5_MB_SCH_PVT_013

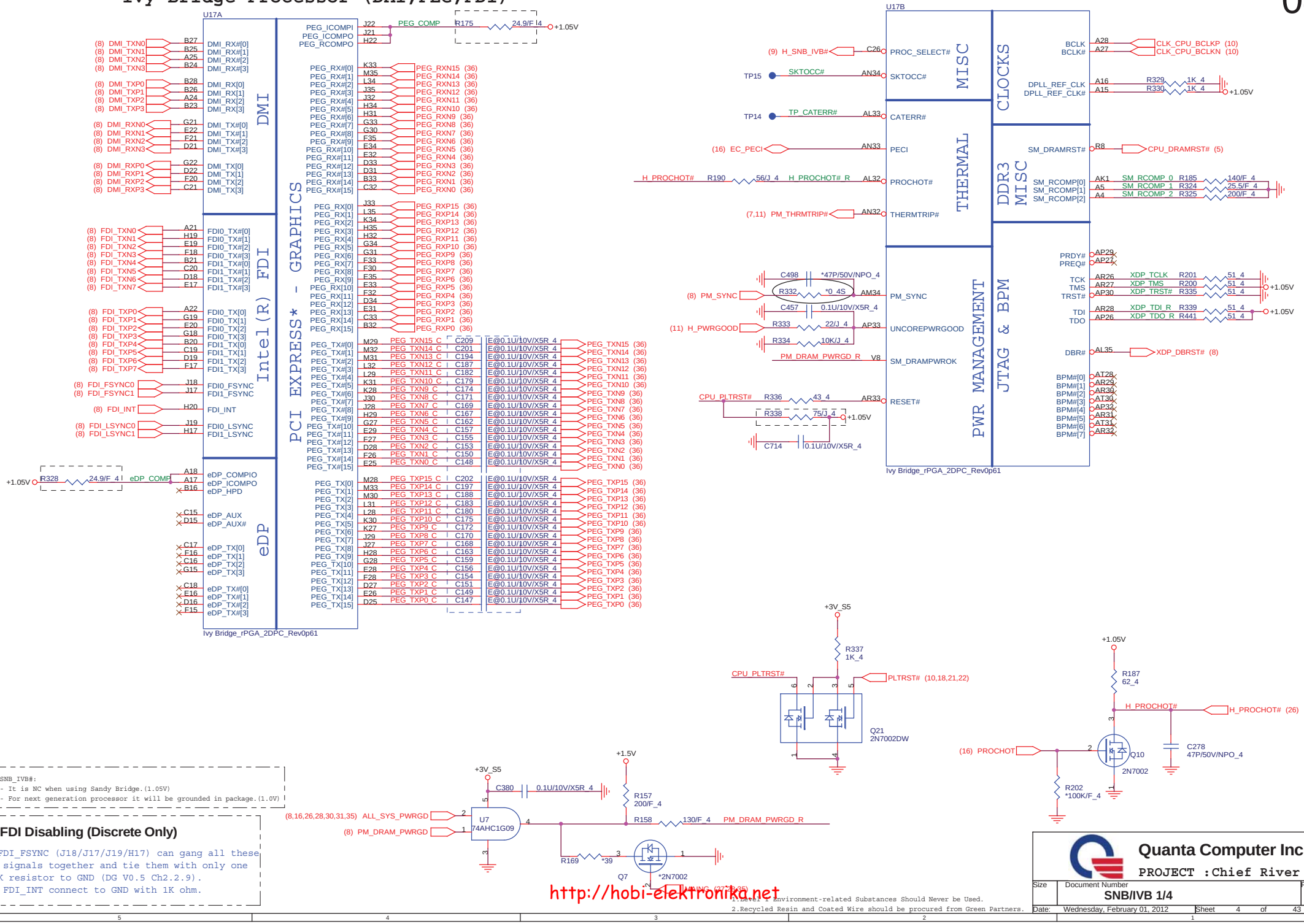
P23-- add R461 ,R462 [0ohm]

Reason : customer requirement for TP SMBUS signal
Possible Risk: No.

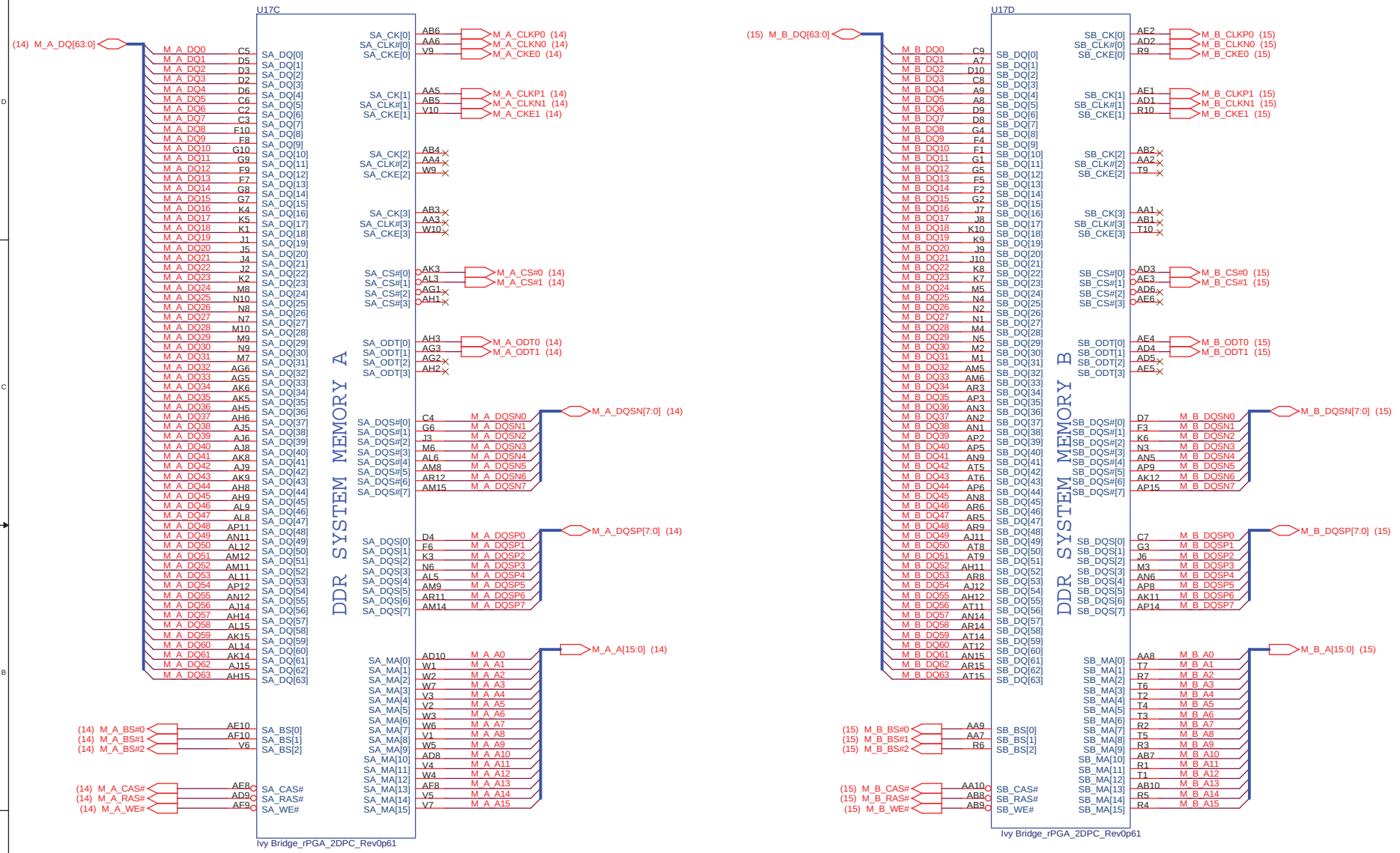
Ivy Bridge Processor (DMI,PEG,FDI)

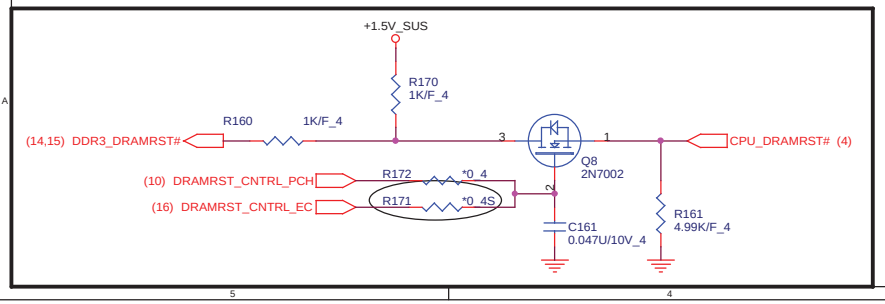
Ivy Bridge Processor (CLK,MISC,JTAG)

04



Ivy Bridge Processor (DDR3)





1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

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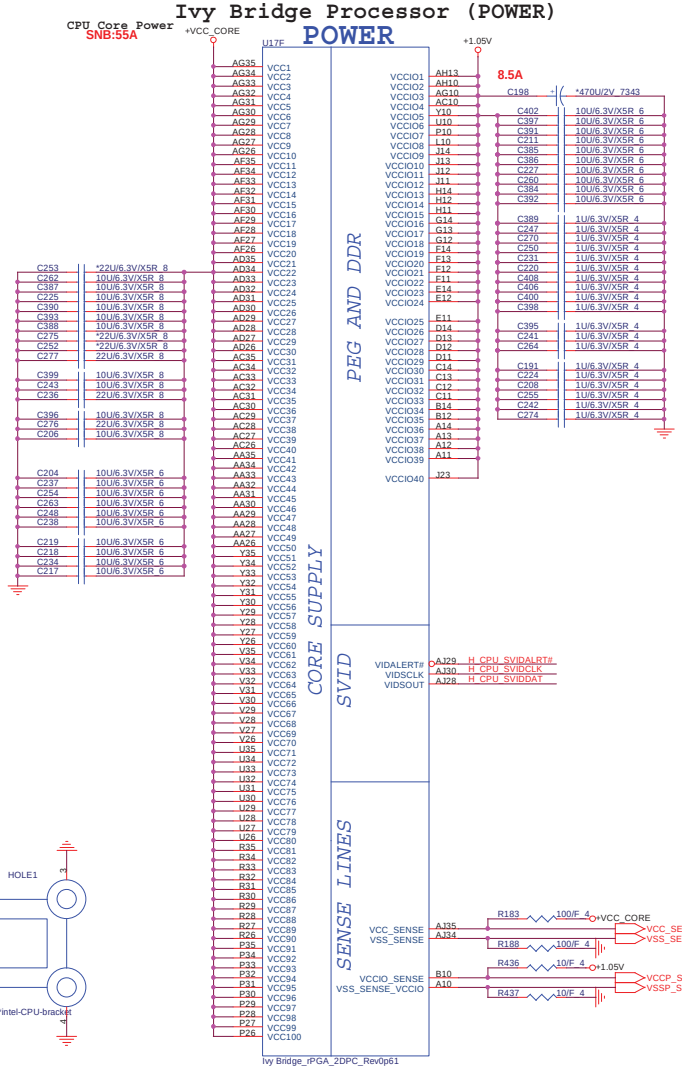
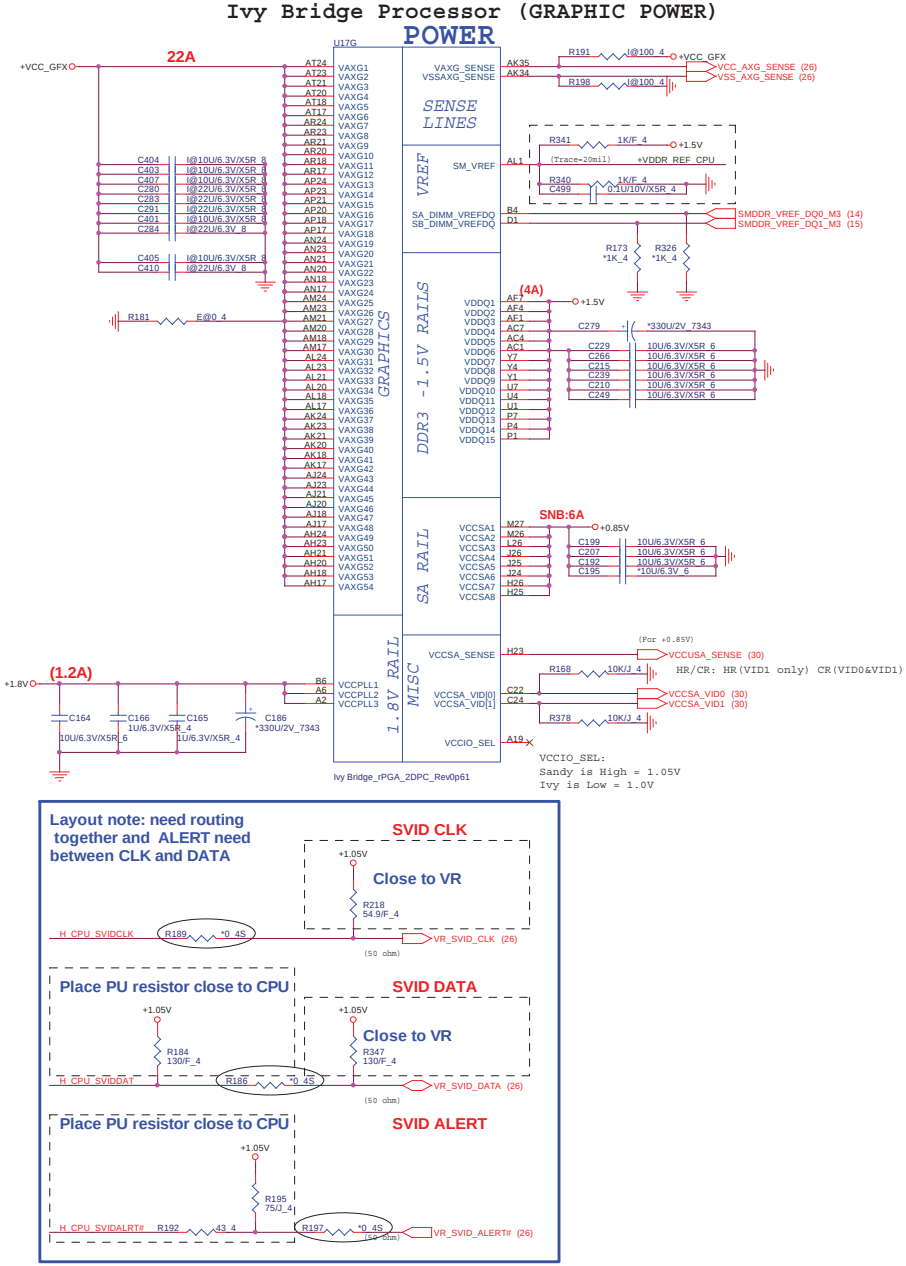
PROJECT :Chief River

Size	Document Number	Rev
	SNB/IVB 2/4	1A
Date: Wednesday, February 01, 2012	Sheet 5 of 43	

Ivy Bridge Processor (POWER)



Ivy Bridge Processor (GRAPHIC POWER)



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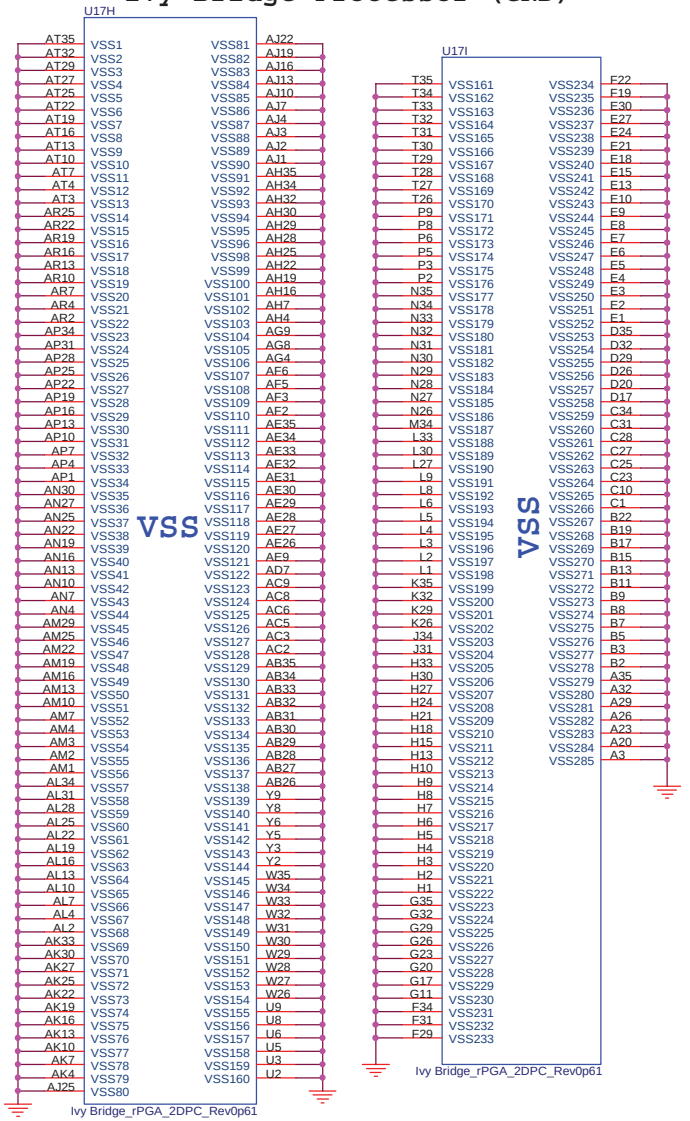
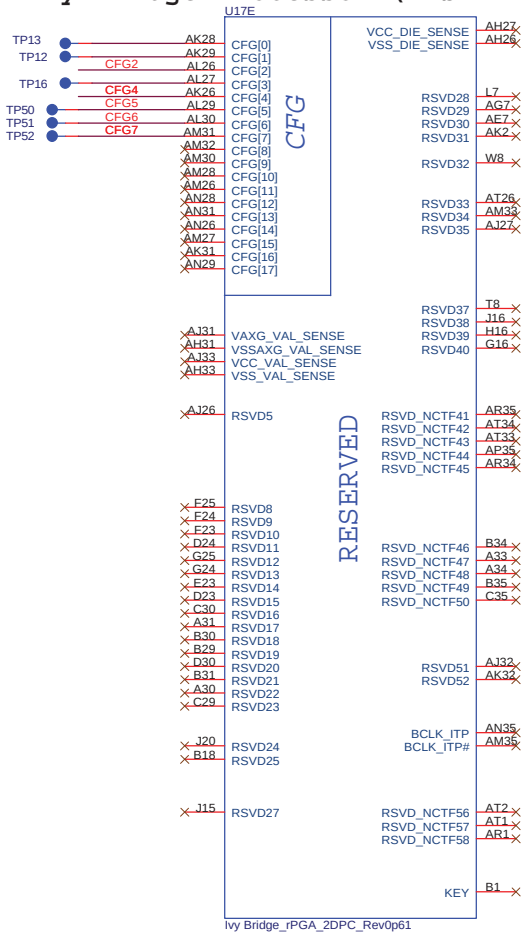
Size	Document Number	Rev
	SNB/IVB 3/4	1A

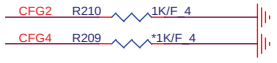
Date: Wednesday, February 01, 2012 Sheet 6 of 43

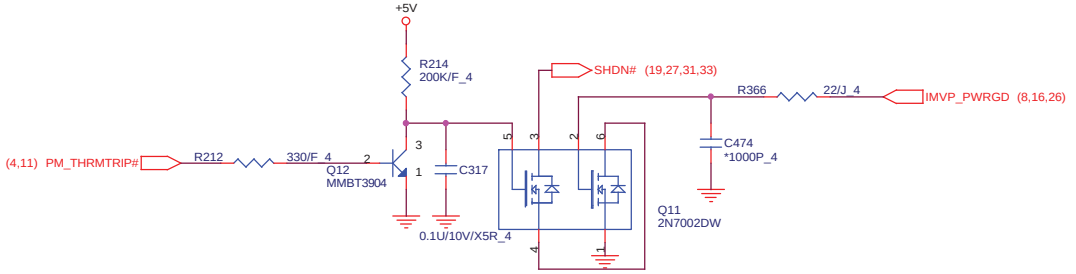
Ivy Bridge Processor (GND)



Ivy Bridge Processor (RESERVED, CFG)







Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	**Lane Reversed**
CFG4 (DP Presence Strap)	**Disable; No physical DP attached to eDP**	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	**PEG train immediately following xxRESETB de assertion**	PEG wait for BIOS training

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - X16 PEG interface
10: PEG x8 x8 bifurcation enableddisabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Size	Document Number	Rev
	SNB/IVB 4/4	1A
Date: Wednesday, February 01, 2012	Sheet 7 of 43	

CPT/PPT (DMI,FDI,PM)

U16C

DMI0RXN BC24 ← (4) DMI_RXN0
DMI1RXN BE20 ← (4) DMI_RXN1
DMI2RXN BG18 ← (4) DMI_RXN2
DMI3RXN BG20 ← (4) DMI_RXN3
DMI0RXP BE24 ← (4) DMI_RXP0
DMI1RXP BC20 ← (4) DMI_RXP1
DMI2RXP BJ18 ← (4) DMI_RXP2
DMI3RXP BJ20 ← (4) DMI_RXP3
DMI0TXN AW24 → (4) DMI_TXN0
DMI1TXN AW20 → (4) DMI_TXN1
DMI2TXN BB18 → (4) DMI_TXN2
DMI3TXN AV18 → (4) DMI_TXN3
DMI0TXP AY24 → (4) DMI_TXP0
DMI1TXP AY20 → (4) DMI_TXP1
DMI2TXP AY18 → (4) DMI_TXP2
DMI3TXP AU18 → (4) DMI_TXP3
DMI_ZCOMP BJ24 — R321 49.9/F_4 DMI_COMP BG25 DMI_IRCOMP — +1.05V
DMI2RBIAS BH21 — R145 750/F_4 DMI2RBIAS

DMI

FDI_RXN0 BJ14 → FDI_TXN0 (4)
FDI_RXN1 AY14 → FDI_TXN1 (4)
FDI_RXN2 BE14 → FDI_TXN2 (4)
FDI_RXN3 BH13 → FDI_TXN3 (4)
FDI_RXN4 BC12 → FDI_TXN4 (4)
FDI_RXN5 BJ12 → FDI_TXN5 (4)
FDI_RXN6 BG10 → FDI_TXN6 (4)
FDI_RXN7 BG9 → FDI_TXN7 (4)
FDI_RXP0 BG14 → FDI_TXP0 (4)
FDI_RXP1 BB14 → FDI_TXP1 (4)
FDI_RXP2 BF14 → FDI_TXP2 (4)
FDI_RXP3 BG13 → FDI_TXP3 (4)
FDI_RXP4 BE12 → FDI_TXP4 (4)
FDI_RXP5 BG12 → FDI_TXP5 (4)
FDI_RXP6 BJ10 → FDI_TXP6 (4)
FDI_RXP7 BH9 → FDI_TXP7 (4)
FDI_INT AW16 → FDI_INT (4)
FDI_FSYNC0 AV12 → FDI_FSYNC0 (4)
FDI_FSYNC1 BC10 → FDI_FSYNC1 (4)
FDI_LSYNC0 AV14 → FDI_LSYNC0 (4)
FDI_LSYNC1 BB10 → FDI_LSYNC1 (4)

FDI

System Power Management

DSWVRMEN A18 ← DSWVREN
DPWROK E22 ← DPWROK (16)
WAKE# B9 ← PCIE_WAKE# 1 — R439 *0_4S — PCIE_WAKE# (16,21)
CLKRUN# / GPIO32 N3 → CLKRUN#
SUS_STAT# / GPIO61 G8 → T8
SUSCLK / GPIO62 N14 → T10
SLP_S5# / GPIO63 D10 → T3
SLP_S4# H4 → T6 → SLP_S4# (16)
SLP_S3# F4 → T4 → SLP_S3# (16)
SLP_A# G10 → T9
SLP_SUS# G16 → SLP_SUS# (16)
PMSYNCH AP14 ← PM_SYNC (4)
SLP_LAN# / GPIO29 K14

DSW DSW

(16) SUSACK# — R438 *0_4S — SUSACK# C12
SUSWARN# — R255 *0_4 — SUSACK# R
(4) XDP_DBRST# — XDP_DBRST# K3 — SYS_RESET#
(7,16,26) IMVP_PWRGD — R365 22/J_4 — C473 1000P/50V/X7R/10% — SYS_PWROK P12
PWROK_R — PWROK L22
(16) PCH_PWROK_EC — R37 0_4S — R28 *0_4 — APWROK L10
(4,16,26,28,30,31,35) ALL_SYS_PWRGD
(4) PM_DRAM_PWRGD — PM_DRAM_PWRGD B13 — DRAMPWROK
(16) RSMRST# — RSMRST# C21
(16) SUSWARN# — SUSWARN# K16 — SUSWARN#/SUSPWRDNACK/GPIO30
(16) EC_PWRBTN# — PWRBTN# E20
(16) AC_PRESENT — AC_PRESENT H20 — ACPRESENT / GPIO31
PM_BATLOW# — BATLOW# / GPIO72 E10
PM_RI# — RI# A10

+3V_S5 +3V +3V_S5 +3V_S5 +3V_S5 +3V_S5 +3V_S5 +3V_S5

CPT_PPT_Rev_0p5

R54 2.2K_4 INT_EDIDCLK
R50 2.2K_4 INT_EDIDDAT
+3V

CPT/PPT (LVDS,DDI)

U16D

L_BKLTEN J47 ← (16) INT_LVDS_BLON
L_VDD_EN M45 ← (17) INT_LVDS_VDDEN
L_BKLTCTL P45 ← (17) INT_LVDS_BRIGHT
L_DDC_CLK T40 ← (17) INT_EDIDCLK — INT_EDIDCLK
L_DDC_DATA K47 ← (17) INT_EDIDDAT — INT_EDIDDAT
L_CTRL_CLK T45 ← R92 2.2K_4 — +3V
L_CTRL_DATA P39 ← R94 2.2K_4 — +3V
LVD_IBG AF37 — R116 I@2.37K/F_4 — LVDS_IBG
LVD_VBG AF36 — T7
LVD_VREFH AE48
LVD_VREFL AE47

LVDS

LVDSA_CLK# AK39 ← (17) INT_TXLCLKOUTN — INT_TXLCLKOUTN
LVDSA_CLK AK40 ← (17) INT_TXLCLKOUTP — INT_TXLCLKOUTP
LVDSA_DATA#0 AN48 ← (17) INT_TXLOUT0 — INT_TXLOUT0
LVDSA_DATA#1 AM47 ← (17) INT_TXLOUT1 — INT_TXLOUT1
LVDSA_DATA#2 AK47 ← (17) INT_TXLOUT2 — INT_TXLOUT2
LVDSA_DATA#3 AJ48
LVDSA_DATA0 AN47 → (17) INT_TXLOUTP0 — INT_TXLOUTP0
LVDSA_DATA1 AM49 → (17) INT_TXLOUTP1 — INT_TXLOUTP1
LVDSA_DATA2 AK49 → (17) INT_TXLOUTP2 — INT_TXLOUTP2
LVDSA_DATA3 AJ47
LVDSB_CLK# AF40
LVDSB_CLK AF39
LVDSB_DATA#0 AH45
LVDSB_DATA#1 AH47
LVDSB_DATA#2 AF49
LVDSB_DATA#3 AF45
LVDSB_DATA0 AH43
LVDSB_DATA1 AH49
LVDSB_DATA2 AF47
LVDSB_DATA3 AF43

Digital Display Interface

CRT_BLUE N48 ← (17) INT_CRT_BLU — INT_CRT_BLU
CRT_GREEN P49 ← (17) INT_CRT_GRE — INT_CRT_GRE
CRT_RED T49 ← (17) INT_CRT_RED — INT_CRT_RED
CRT_DDC_CLK T39 ← (17) INT_DDCCLK
CRT_DDC_DATA M40 ← (17) INT_DDCDAT
CRT_HSYNC M47 ← (17) INT_CRT_HSYNC
CRT_VSYNC M49 ← (17) INT_CRT_VSYNC
DAC_IREF T43 — R103 1K/D_4
CRT_IRTN T42

CRT

SDVO_TVCLKINN AP43
SDVO_TVCLKINP AP45
SDVO_STALLN AM42
SDVO_STALLP AM40
SDVO_INTN AP39
SDVO_INTP AP40
SDVO_CTRLCLK P38 → INT_HDMI_SCL (19)
SDVO_CTRLDATA M39 → INT_HDMI_SDA (19)
DDPB_AUXN AT49
DDPB_AUXP AT47
DDPB_HPD AT40 → INT_HDMI_HPD_Q (19)
DDPB_0N AV42 → C378 I@0.1U/10V/X5R_4 → INT_HDMI_TXDN2 (19)
DDPB_0P AV40 → C379 I@0.1U/10V/X5R_4 → INT_HDMI_TXDP2 (19)
DDPB_1N AV45 → C365 I@0.1U/10V/X5R_4 → INT_HDMI_TXDN1 (19)
DDPB_1P AV46 → C366 I@0.1U/10V/X5R_4 → INT_HDMI_TXDP1 (19)
DDPB_2N AU48 → C368 I@0.1U/10V/X5R_4 → INT_HDMI_TXDN0 (19)
DDPB_2P AU47 → C369 I@0.1U/10V/X5R_4 → INT_HDMI_TXDP0 (19)
DDPB_3N AV47 → C375 I@0.1U/10V/X5R_4 → INT_HDMI_TXCN (19)
DDPB_3P AV49 → C373 I@0.1U/10V/X5R_4 → INT_HDMI_TXCP (19)

INT. HDMI

DDPC_CTRLCLK P46
DDPC_CTRLDATA P42
DDPC_AUXN AP47
DDPC_AUXP AP49
DDPC_HPD AT38
DDPC_0N AY47
DDPC_0P AY49
DDPC_1N AY43
DDPC_1P AY45
DDPC_2N BA47
DDPC_2P BA48
DDPC_3N BB47
DDPC_3P BB49

INT. DP

DDPD_CTRLCLK M43
DDPD_CTRLDATA M36
DDPD_AUXN AT45
DDPD_AUXP AT43
DDPD_HPD BH41
DDPD_0N BB43
DDPD_0P BB45
DDPD_1N BF44
DDPD_1P BE44
DDPD_2N BF42
DDPD_2P BE42
DDPD_3N BJ42
DDPD_3P BG42

CPT_PPT_Rev_0p5

R place close to PCH
R90 I@150/F_4 INT_CRT_BLU
R95 I@150/F_4 INT_CRT_GRE
R100 I@150/F_4 INT_CRT_RED

PCH Pull-high/low(CLG)

+3V
CLKRUN# R93 8.2K/J_4
XDP_DBRST# R78 1K_4
RSMRST# R70 *47K_4
PWROK_R R30 47K_4

+3V_S5
PM_RI# R256 10K/J_4
SUSWARN# R34 10K/J_4
PM_BATLOW# R35 8.2K/J_4
R440 *8.2K/J_4 — +3V_S5_DSW
PCIE_WAKE# R253 *10K/J_4 — +3V_SUS
AC_PRESENT R13 *10K/J_4 — +3V_S5_DSW
PM_DRAM_PWRGD R7 200/F_4 — +3V_SUS
PCIE_WAKE# 1 R448 10K/J_4 — +3V_S5

+3V_RTC
R241 330K/J_4
DSWVREN

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

+3V_S5
C475 *0.1U/10V/X5R_4
(7,16,26) IMVP_PWRGD — R367 *22/J_4 — (16) PCH_PWROK_EC
U25 TC7SH08FU
4 SYS_PWROK

FDI_INT R132 E@1K_4
FDI_FSYNC0 R139 E@1K_4
FDI_FSYNC1 R144 E@1K_4
FDI_LSYNC0 R131 E@1K_4
FDI_LSYNC1 R138 E@1K_4

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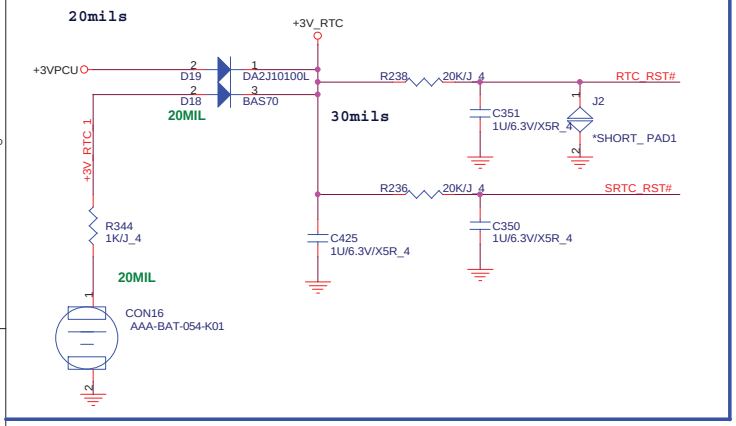
PROJECT :Chief River

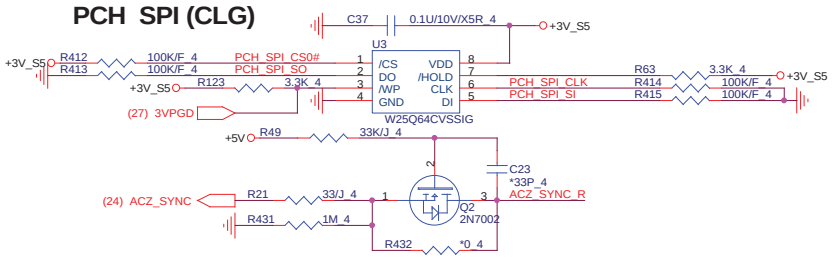
Size	Document Number	Rev
	CPT/PTT 1/6	1A
Date: Wednesday, February 01, 2012	Sheet 8 of 43	

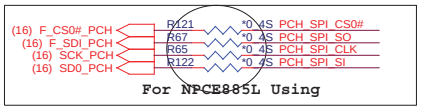
RTC Circuitry(RTC)



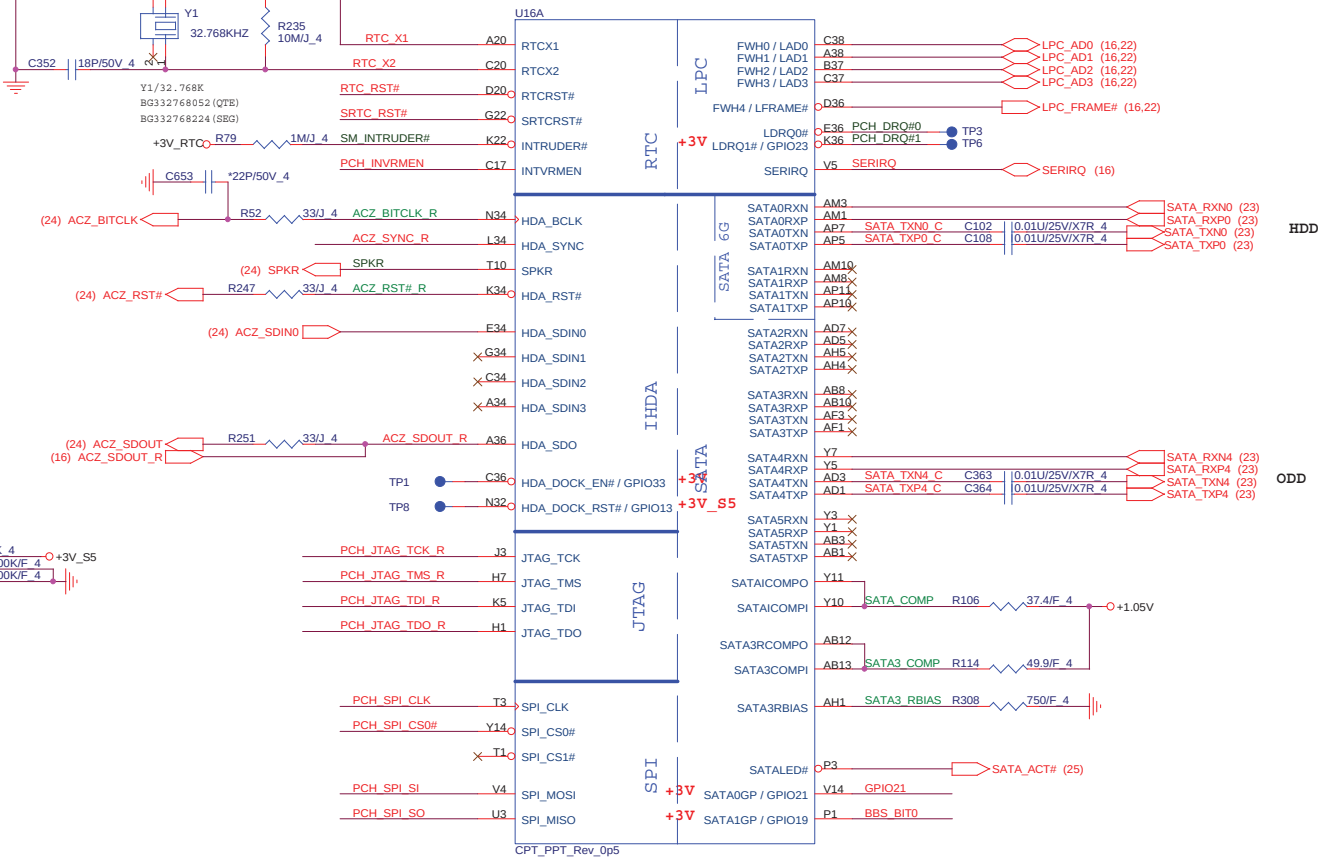
MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00

PCH SPI (CLG)





CPT/PPT (HDA,JTAG,SATA)



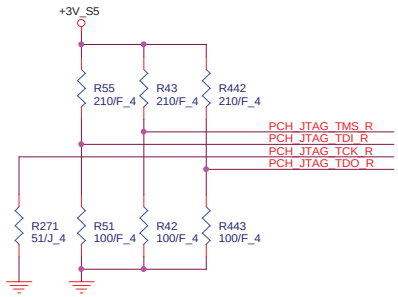
CPT_PPT_Rev_0p5

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	HK1/HK2 note
SPKR	No reboot mode setting	PWROK	**0 = Default (weak pull-down 20K)** 1 = Setting to No-Reboot mode	SPKR
PCI_GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R270 *1K_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+3V_RTC R242 330K/J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC	**Default weak pull-up on GNT0/1#** **[Need external pull-down for LPC BIOS]**
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		TP47 BBS_BIT1 (10) TP43 BBS_BIT0
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Enabled	ACZ_SDOUT_R
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss for Ivy Bridge 1 = Set to Vcc for Sandy Bridge (weak pull-down 20K)	R140 2.2K_4 +1.8V R320 1K_4 NV_CLE (11) H_SNB_IVB# (4)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	TP44 PLL_ODVR_EN (11)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	R49 1K_4 ACZ_SYNC_R

HR/CR: PROCSEL#

PCH JTAG Debug (CLG)



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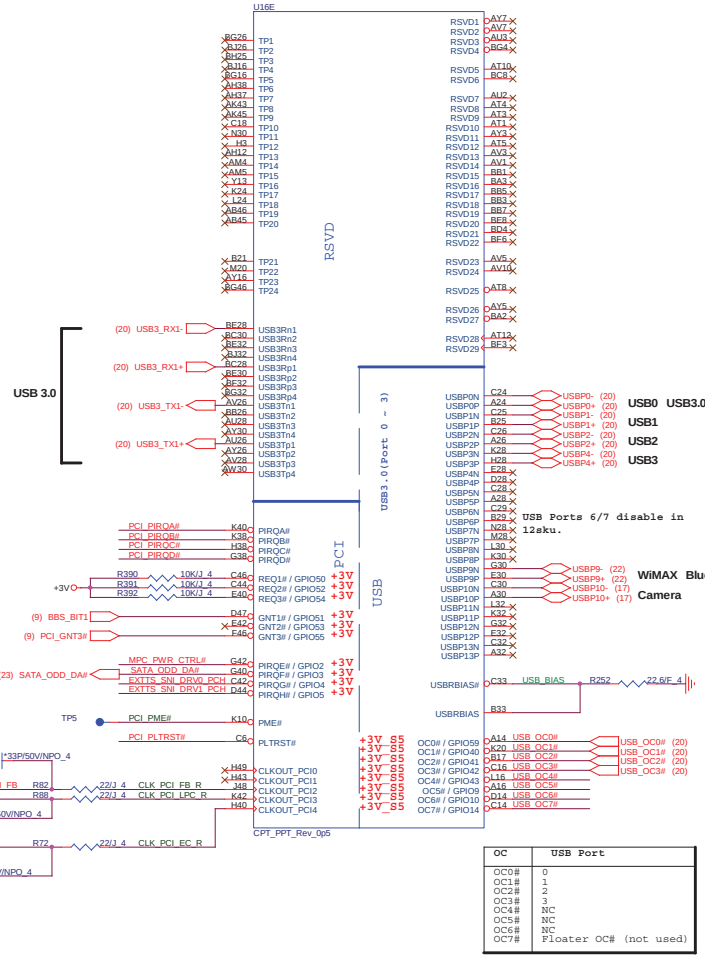
Size	Document Number	Rev
	CPT/PPT 2/6	1A

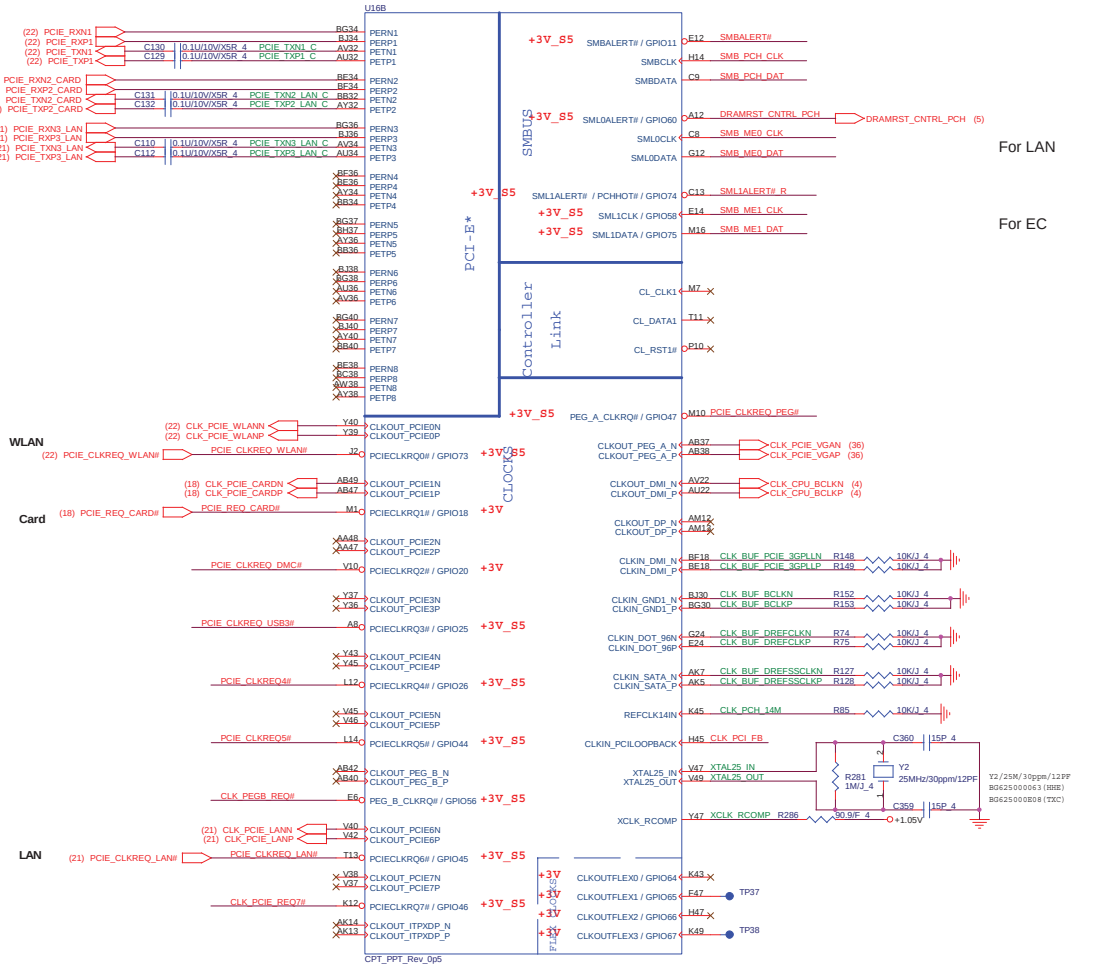
Date: Wednesday, February 01, 2012 Sheet 9 of 43

CPT/PPT (PCI,USB,NVRAM)

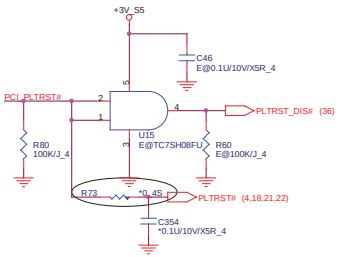


OC	USB Port
OC0#	0
OC1#	1
OC2#	2
OC3#	3
OC4#	NC
OC5#	NC
OC6#	NC
OC7#	Floater OC# (not used)

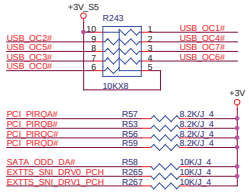
CPT/PPT (PCI-E,SMBUS,CLK)



PLTRST#(CLG)

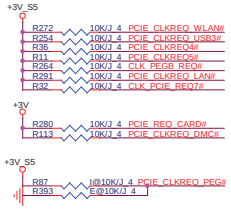


PCI/USBOC# Pull-up(CLG)

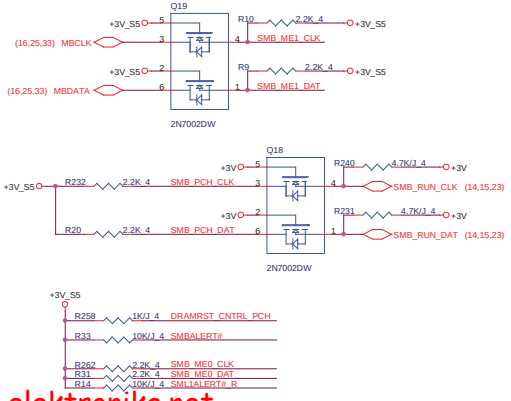


MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



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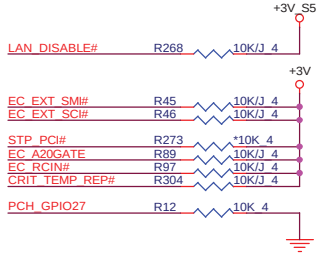
Size	Document Number	Rev
	CPT/PPT 3/6	1A

Date: Wednesday, February 01, 2012 Sheet 10 of 43

CPT/PPT (GPIO,VSS_NCTF,RSVD)

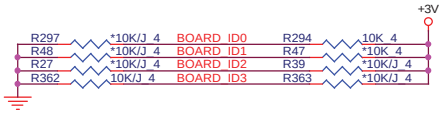
GPIO Pull-up/Pull-down(CLG)



	R363 (High) R362 (Low) Board ID3	R294 (High) R297 (low) Board ID0
14"/HK6/HK76	0	0
14"/HK6/HK70	1	0
15"/HK5/HM76	0	1
15"/HK5/HM70	1	1

Board ID1 (VRAM Vendor)	Samaung(1)	Hynix(0)
R47 (High)	Stuff	No Stuff
R48 (Low)	No Stuff	Stuff

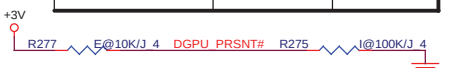
Board ID2		
14" 4PCS	1G	512M
15" 8PCS	1G	2G
R39 (High)	Stuff	No Stuff
R27 (Low)	No Stuff	Stuff



SV_SET_UP
High = Strong (Default)

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

PCBA SKU	Discrete	UMA
R277 (Pull High)	Stuff	No Stuff
R275 (Pull Low)	No Stuff	Stuff



FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST

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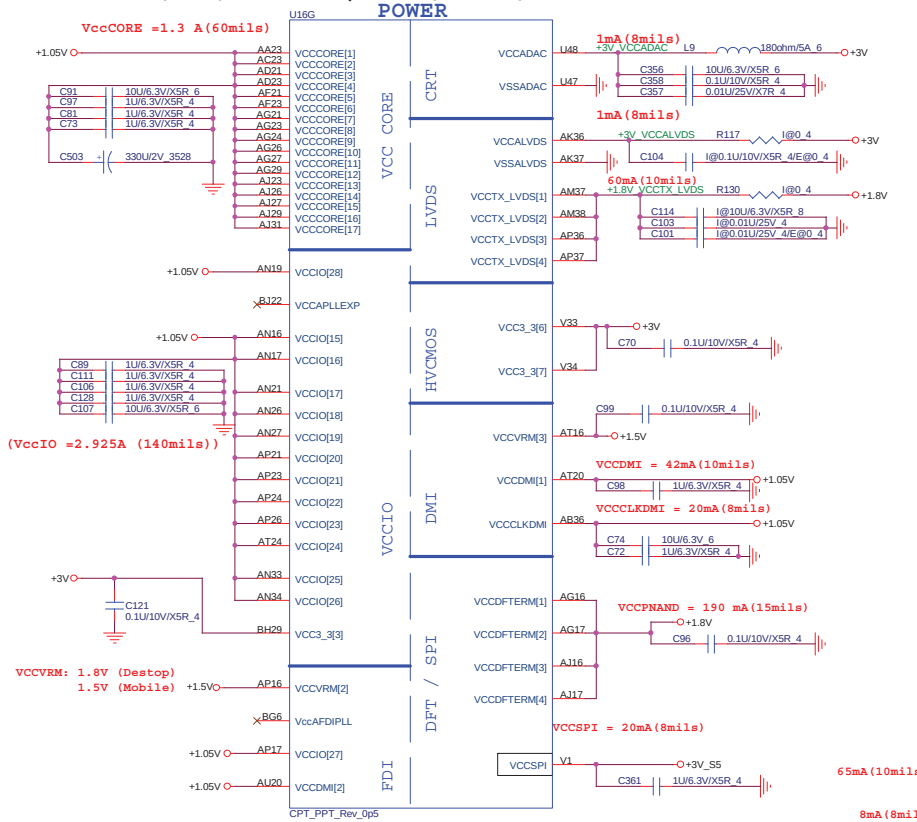
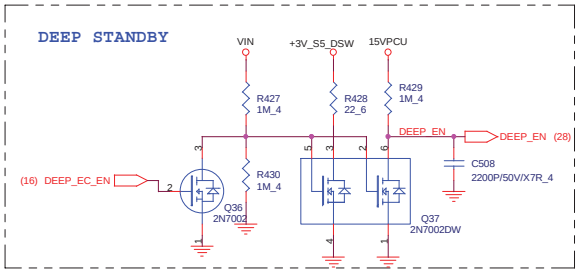
Size	Document Number	Rev
	CPT/PPT 4/6	1A

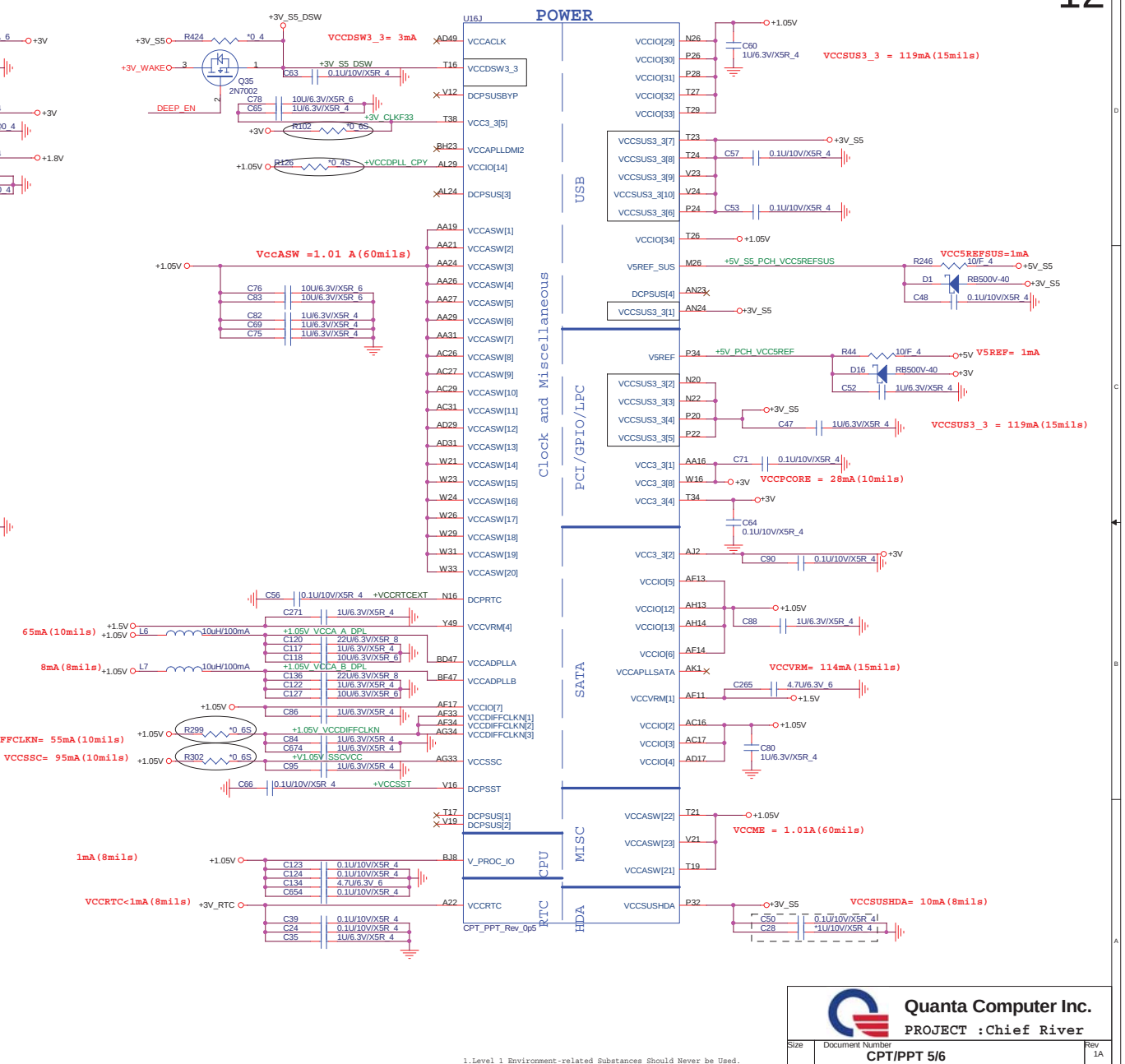
Date: Wednesday, February 01, 2012 Sheet 11 of 43

PCH5 (CLG) CPT/PPT (POWER)





CPT/PPT (POWER)



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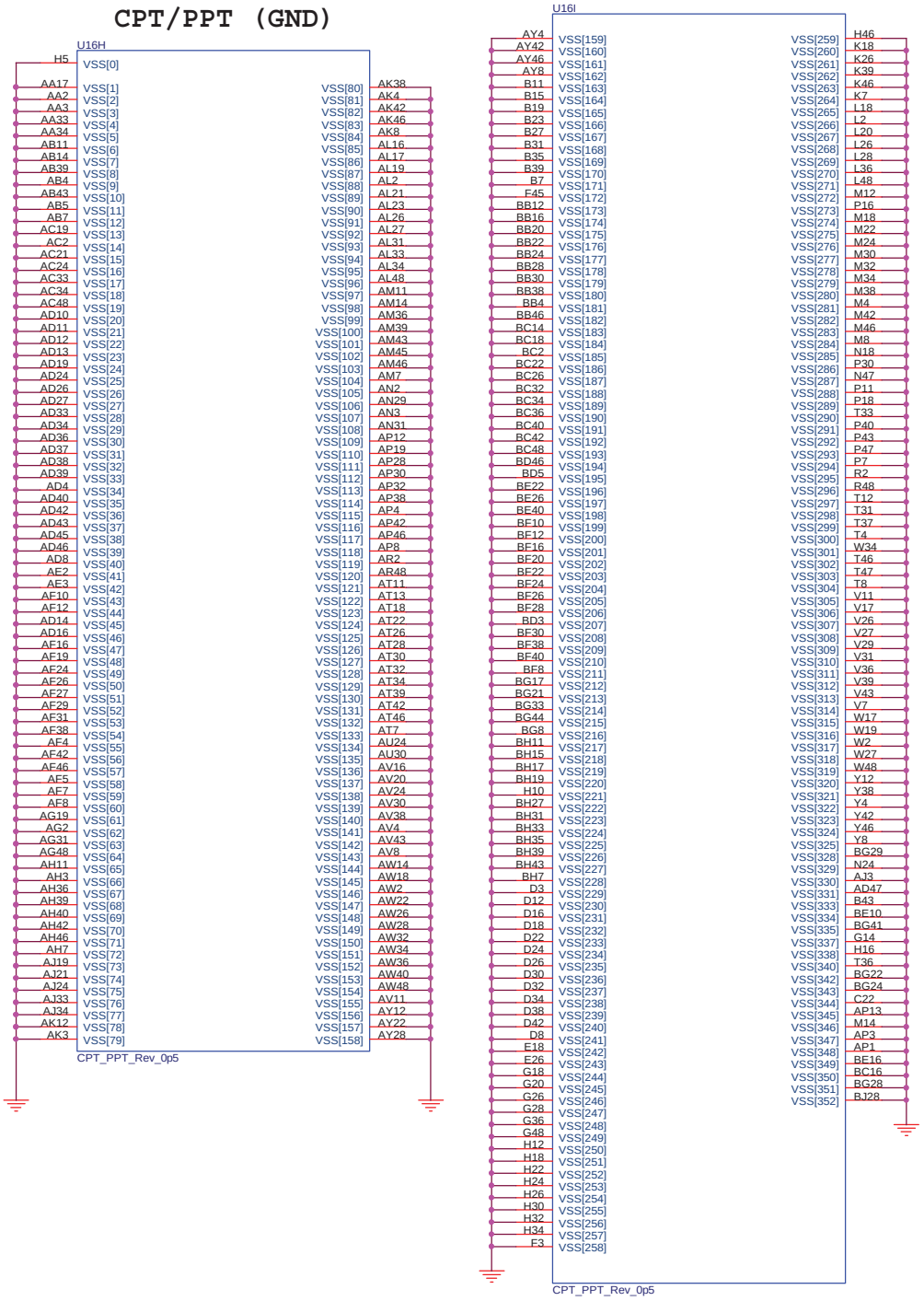
Size	Document Number		Rev
	CPT/PPT 5/6		1A
Date:	Wednesday, February 01, 2012	Sheet 12 of 43	

CPT/PPT (GND)



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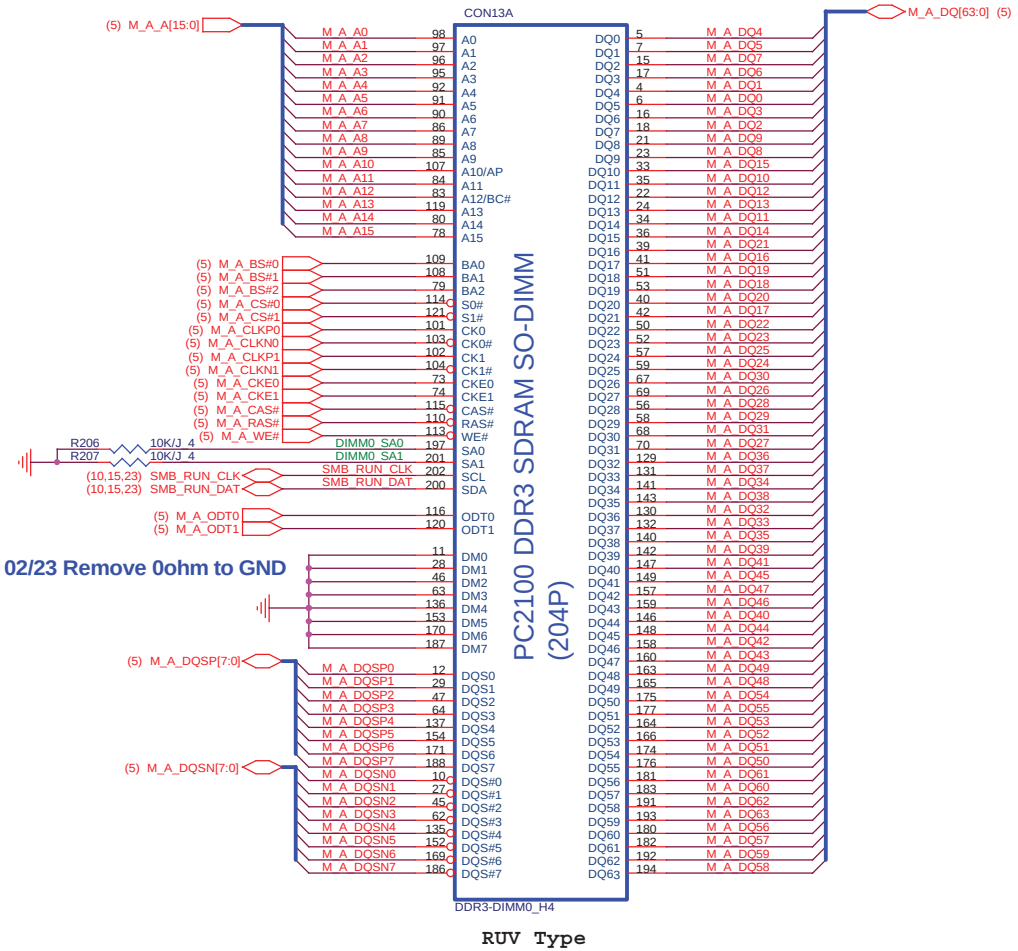
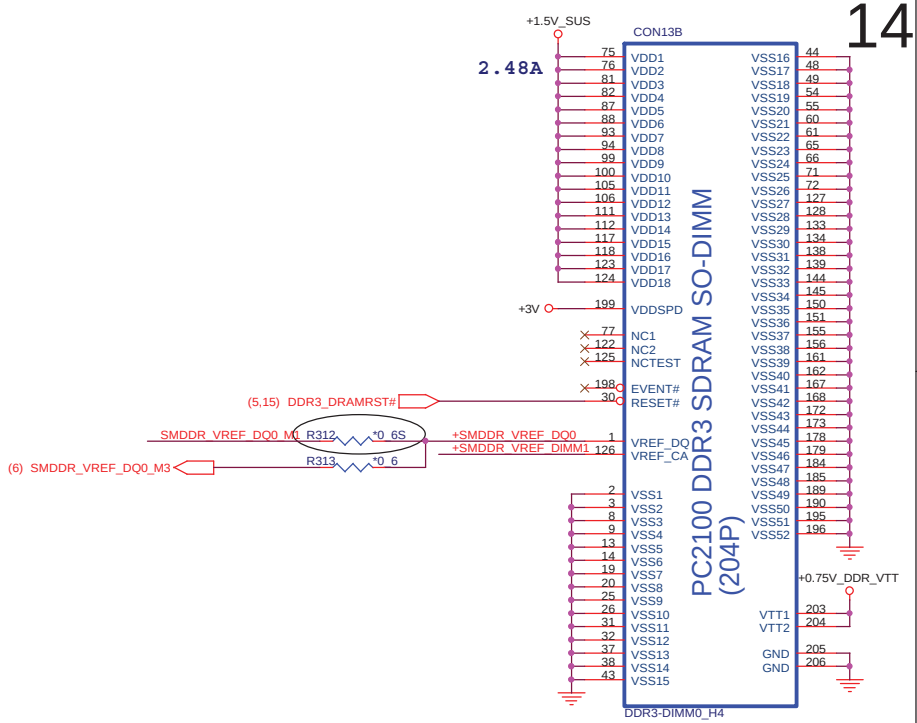
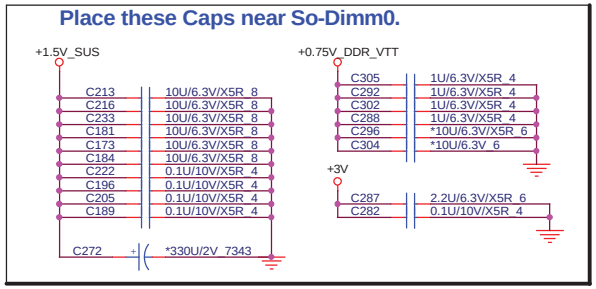
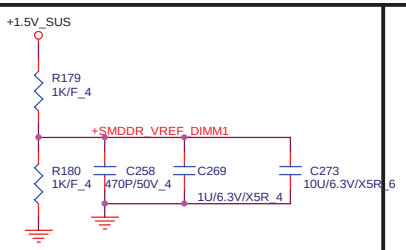
Size	Document Number	Rev
	CPT/PPT 6/6	1A
Date: Wednesday, February 01, 2012	Sheet 13 of 43	



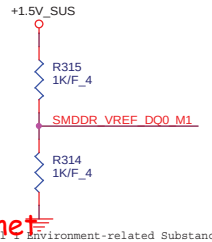
02/23 Remove 0ohm to GND

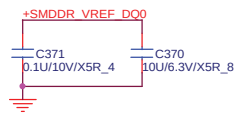






VREF DQ0 M1 Solution





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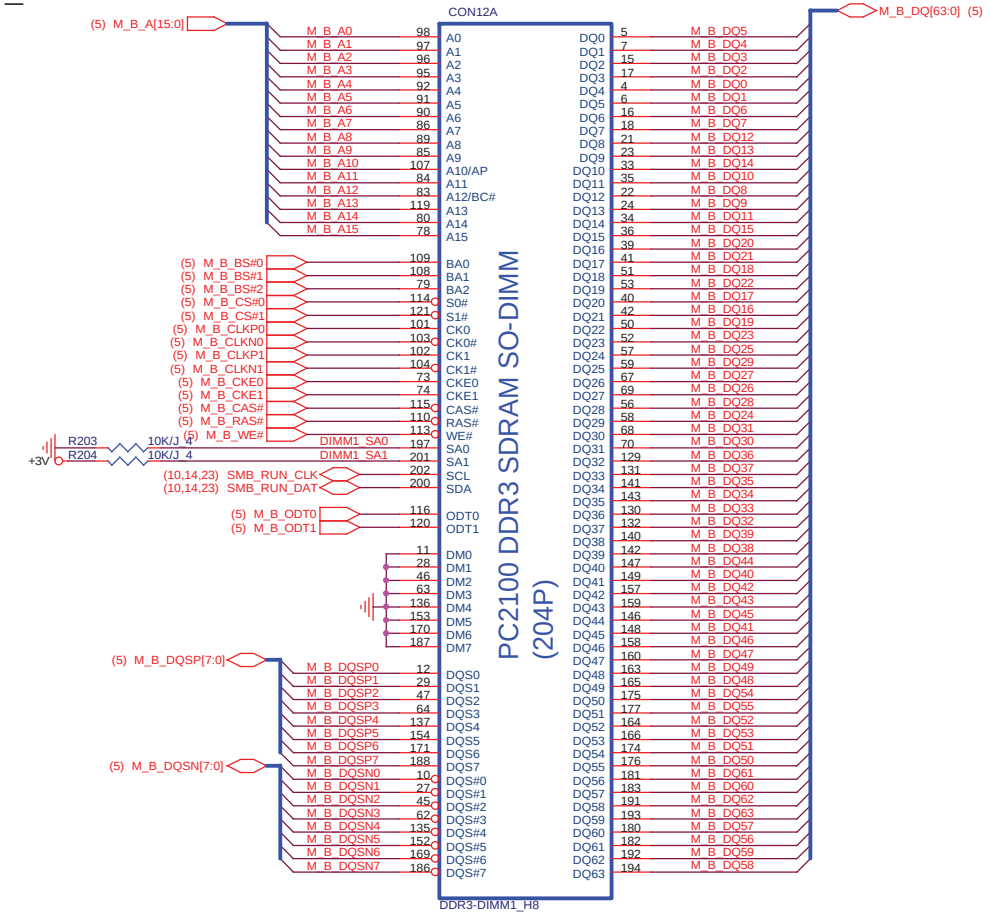
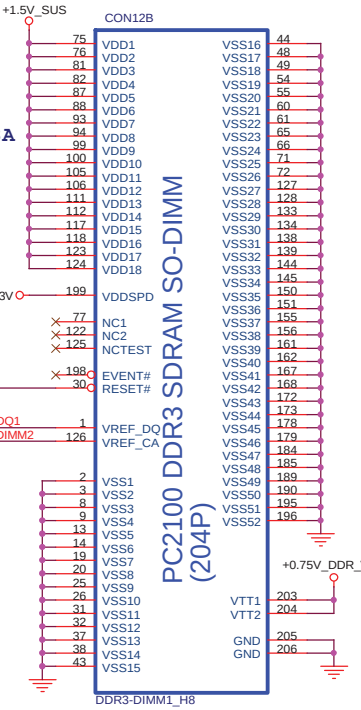
Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A
Date: Wednesday, February 01, 2012	Sheet 14 of 43	

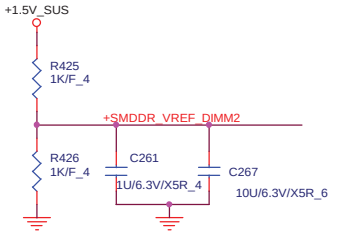
DDR_RVS(DDR)



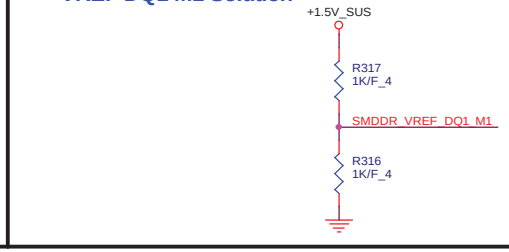
RUV Type



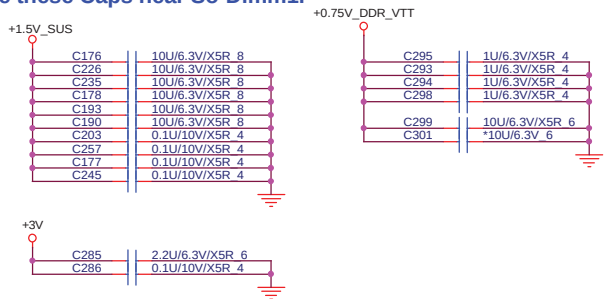
RUV Type



VREF DQ1 M1 Solution



Place these Caps near So-Dimm1.



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Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
Date: Wednesday, February 01, 2012	Sheet 15 of 43	

**** Straping Pin,Can not pull low.**
Note the input leakage current to the strap pins must be less than 10uA.

Since ECSCI is OD, no need for a back-drive protection diode on this signal. But note there is internal PU in chipset at default

Magnetic Lid Switch

KU4 E-CMOS: +3VPCU, IN, OUT → LID#, GND

E-CMOS :AL002618001/EC2618NLB1GR
PROLIFIC : AL003661003/PT3661-BB
BCD : AL009249000/AH9249NTR-G1

35001

+3VPCU, KD4 RB501V-40, KR23 1K/F_4, KR27 4.7K_4, KR16 2.2K_4, KR19 2.2K_4, KR20 *100K_4, KU2 R5G05000N753NF (PGM, PIO, RSET, SDA, VSS, SCK, VCC, GND, CNVSS), BATT_RST#, BATT_ID (32), 35001_SDA, 35001_SCK, KC7 *1000P/50V/X7R/10%_4, KC9 *1000P/50V/X7R/10%_4

NPCE885L

KU1

LPC: LAD0/GPIOF1 … LAD3/GPIOF4, LRESET#/GPIOF7, LCLK/GPIOF5, LFRAME#/GPIOF6
- (9,22) LPC_AD0 … LPC_AD3
- (10) CLK_PCI_EC ← +3V, KR25 10K/F_4, KC18 *33P/50V/NPO_4
- (9,22) LPC_FRAME#

GA20/GPIO85, SERIRQ/GPIOF0, SMI#/GPIO65, ECSCI#/GPIO54, KBRST#/GPIO86
- (11) EC_A20GATE
- (9) SERIRQ
- (11) EC_EXT_SMI#
- (11) EC_EXT_SCI#
- (11) EC_RCIN#

GPIO67/PWUREQ#
- (8) RSMRST# ← KR29 2.2K_4, KR57 10K/J_4

SPI: F_SDI/F_SDIO1, F_SDIO/F_SDIO0, F_SCK, F_CS0#
- (9) F_SDI_PCH
- (9) SD0_PCH
- (9) SCK_PCH
- (9) F_CS0#_PCH

A/D: AD0/GPIO90 … AD7/GPIO07
- MBATV (33), ISENS_IN (33), BAT_PRS# (32), FUN_ASSIST# (25), NBSWON# (25), SLP_S3# (8), BT_PEN (22), SLP_SUS# (8)

D/A: DA0/GPIO94 … DA3/GPIO97
- VFAN (23), HDD_UNLOAD (23), CRIT_TEMP_REP# (11), EC_WAKE_ON (27)

PWM: A_PWM0/GPIO15, B_PWM0/GPIO21, C_PWM0/GPIO13, D_PWM0/GPIO32, H_PWM0/GPIO33, G_PWM0/GPIO66, E_PWM0/GPIO45, F_PWM0/GPIO40
- KB_BACKLIGHT (22), NUMLED# (25), CAPSLED# (25), SCROLED# (25), SLEEPLED# (25), BATLED1# (25), PWRLED# (25), RF_LED# (25)

LPCPD#/GPIO10, CLKRUN#/GPIO11
- S5_ON ← WLAN_LED# (22), S5_ON (27)

K/B: KBSIN0/GPIOA0/N2TCK … KBSIN7/GPIOA7
- (42) MX0 … MX7

KBSOUT0/GPOB0/JENK#** … KBSOUT17/GPIO57
- (42) MY0 … MY17

GPIO: GPIO02, GPIO16, GPIO30/F_WP#, GPIO36, GPIO41/F_WP#, GPIO70, GPIO71, GPIO72, GPIO81/F_WP#
- SUSACK# (8), SLP_S4# (8), DEEP_EC_EN ← DEEP_EC_EN (12), SUS_ON (17,20,27,28), RUN_ON (27,28,29,31,33,34,35), RUN_ON_5V (23)
- KD2 RB501V-40 → EC_PWRBTN# (8)
- KR35 2.2K_4 ← BATT_RST#
- PCH_PWROK_EC → PCH_PWROK_EC (8)

GPIO24/HGPIO01, TA1/GPIO56
- DRAMRST_CNTRL_EC (5), SUSWARN# (8)

TMS/SDA3B/GPIO43
- ALL_SYS_PWRGD ← ALL_SYS_PWRGD (4,8,26,28,30,31,35)

**SOUT_CR/GPO83/TRIST#, TDI/SCL4B/GPIO44
- KR39 *0_4S → AMPMUTE# (24), DISPON
- KR46 E@2.2K_4 → DISPON (17), EXT_LVDS_BLON (37)
- KR49 I@2.2K_4 → INT_LVDS_BLON (8)
- KR41 100K/F_4

GPIO51
- 2540A_CTL3 (20)

CIR: RDY#/GPIO52/PSDAT3, TDO/GPIO50/PSCLK3, PSDAT2/GPIO27, PSCLK2/GPIO26, PSDAT1/GPIO35, PSCLK1/GPIO37
- (25) FUN_WEB#, (9) ACZ_SDOUT_R, (8) AC_PRESENT
- KR6 *0_4S, KR13 10K/F_4 ← +3VPCU
- LID#, TBDATA, TBCLK
- (23) TBDATA, (23) TBCLK

CIRRXL/GPIO34, CIRRXM/SDA4B/TRST#/GPIO46, SIN_CR/CIRRXM/GPIO87
- 2540A_CTL2 (20), WLAN_RF_ON (22), PCH_GPIO27 (11)

PECI, VTT, TCK/SCL4B/GPIO42/Thermal Alarm
- KR9 43_4 → EC_PECI (4)
- KC6 1U/6.3V/X5R_4 → +1.05V
- KR56 *0_4, KR60 *0_4S → PCIE_WAKE# (8,21), IMVP_PWRGD (7,8,26)

SPI_DI/GPIO77, **SPI_DO/GPO76, SPI_SCK/GPIO75
- ODD_PWEN (23), DC/-C (32,33)
- KR7 *10K/F_4

TA2/GPIO20/IOX_DIN_DIO, TB1/GPIO14, TB2/GPIO01
- (23) HDD_INTERRUPT1, (23) FAN-SIG, (21,33) ACIN

SM BUS / I/O Expansion: SCL1/GPIO17/N2TCK, SDA1/GPIO22/N2TMS; SCL2/GPIO73, SDA2/GPIO74; SCL3A/GPIO23, SDA3A/GPIO31; SCL4A/GPIO47, SDA4A/GPIO53
- (32) MBCLK_BAT, (32) MBDATA_BAT
- 35001_SCK, 35001_SDA
- (10,25,33) MBCLK, (10,25,33) MBDATA
- (20) 2540A_CTL1, (4) PROCHOT

GPIO06/IOX_DOUT, **TEST#GPO82/IOX_LDSH, **XORTR#GPO84/IOX_SCLK, CLKOUT/GPIO55/IOX_DIM_DIO
- USB_WAKE# (20) ← KR55 100K/F_4 → +3VPCU
- USB_CHRG_ON (20)
- BT_LED# (22), FUN_VAIO# (25) ← KR54 *0_4 → CHGEN# (33)

VREF ← KC15 0.1U/10V/X5R_4

VCC_POR# ← KR8 4.7K_4 → +3VPCU
VCC POWER ON RESET

VCORF ← KC1 1U/6.3V/X5R_4

GPIO00/EXTCLK
- (8) DPWROK ← KR59 100K/F_4

GND, GND, GND, GND, GND, GND, AGND → KR30 *0_4S

KD9 RB501V-40: DPWROK
KD8 RB501V-40: RSMRST#
KD7 RB501V-40: PCH_PWROK_EC
(27) 5VPGD

+3VPCU: KC17 *10U/6.3V/X5R_8, KC5 0.1U/10V/X5R_4, KC2 0.1U/10V/X5R_4, KC14 0.1U/10V/X5R_4, KC8 0.1U/10V/X5R_4, KC3 0.1U/10V/X5R_4, KC10 0.1U/10V/X5R_4, KC16 *10U/6.3V/X5R_8, KC13 0.1U/10V/X5R_4
+3V: KC10 0.1U/10V/X5R_4

TBCLK KR51 4.7K_4 → +3V
TBDATA KR52 4.7K_4 → +3V

+3VPCU: KR31 3.3K_4 MBCLK, KR32 3.3K_4 MBDATA, KR3 4.7K_4 MBCLK_BAT, KR1 4.7K_4 MBDATA_BAT

ALL_SYS_PWRGD KR2 1K/F_4 → +3V

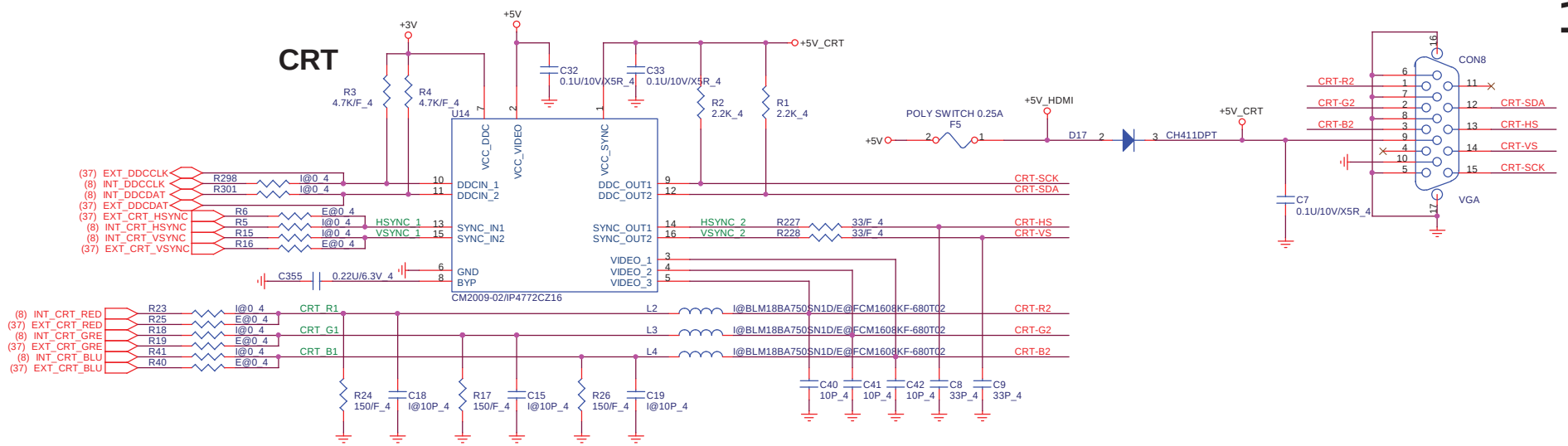
MBATV KC11 0.01U/25V/X7R_4
ISENS_IN KC12 0.01U/25V/X7R_4

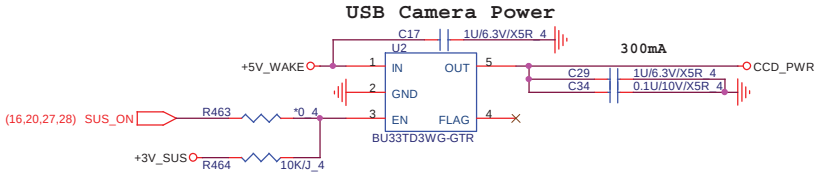
EC_WAKE_ON KR50 100K/F_4
S5_ON KR18 100K/F_4
DEEP_EC_EN KR58 100K/F_4
→ +3VPCU

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

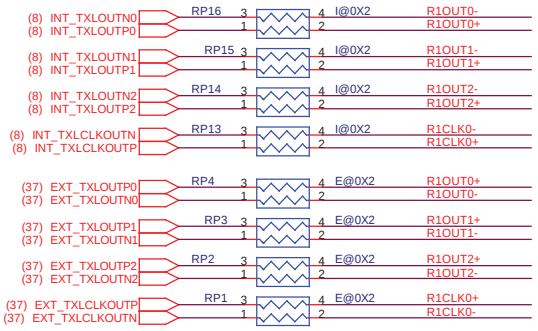
Quanta Computer Inc.
PROJECT :Chief River

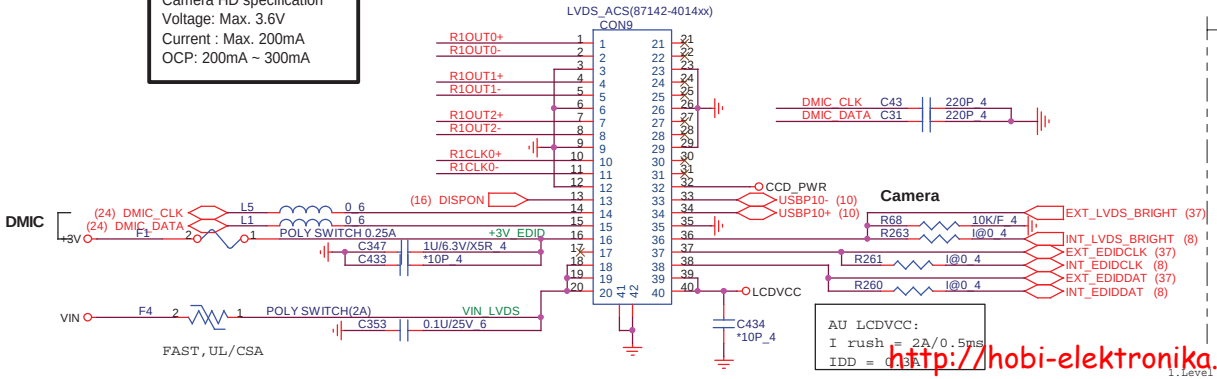
Size	Document Number	Rev
	NPCE885L	1A
Date: Wednesday, February 01, 2012	Sheet 16 of 43	

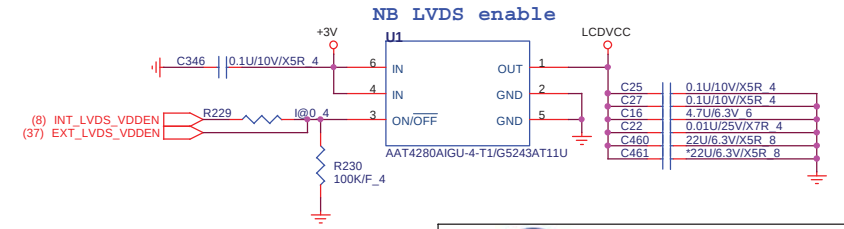




Camera HD specification
Voltage: Max. 3.6V
Current : Max. 200mA
OCP: 200mA ~ 300mA



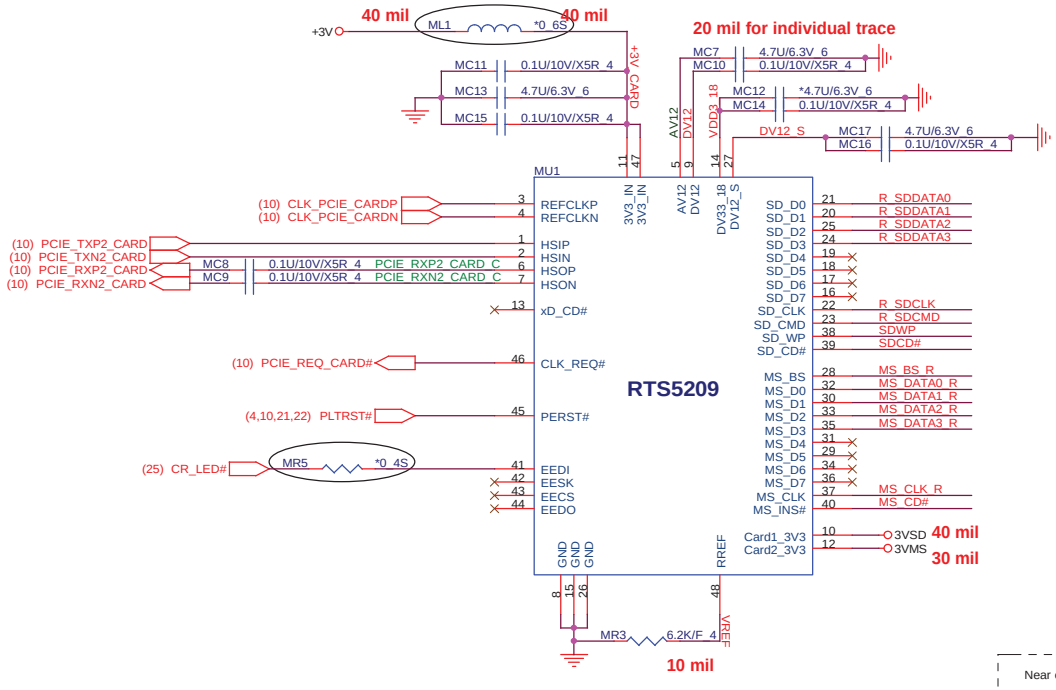


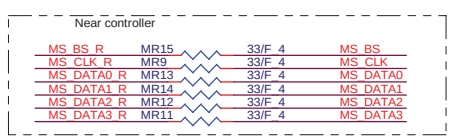


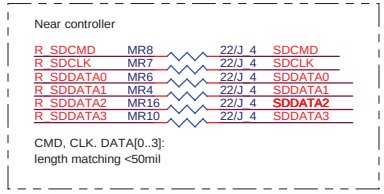
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

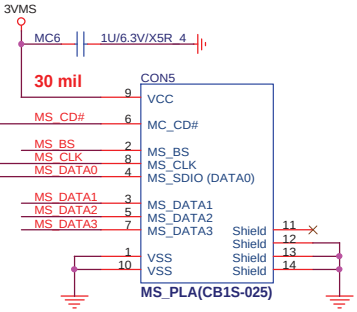
Quanta Computer Inc.
PROJECT :Chief River

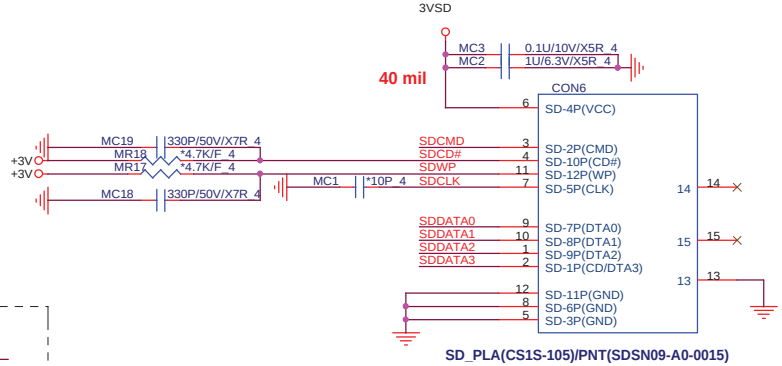
Size	Document Number	Rev
	CRT/LVDS	1A
Date: Wednesday, February 01, 2012	Sheet 17 of 43	











1.Never 1 Environment-related Substances Should Never be Used.
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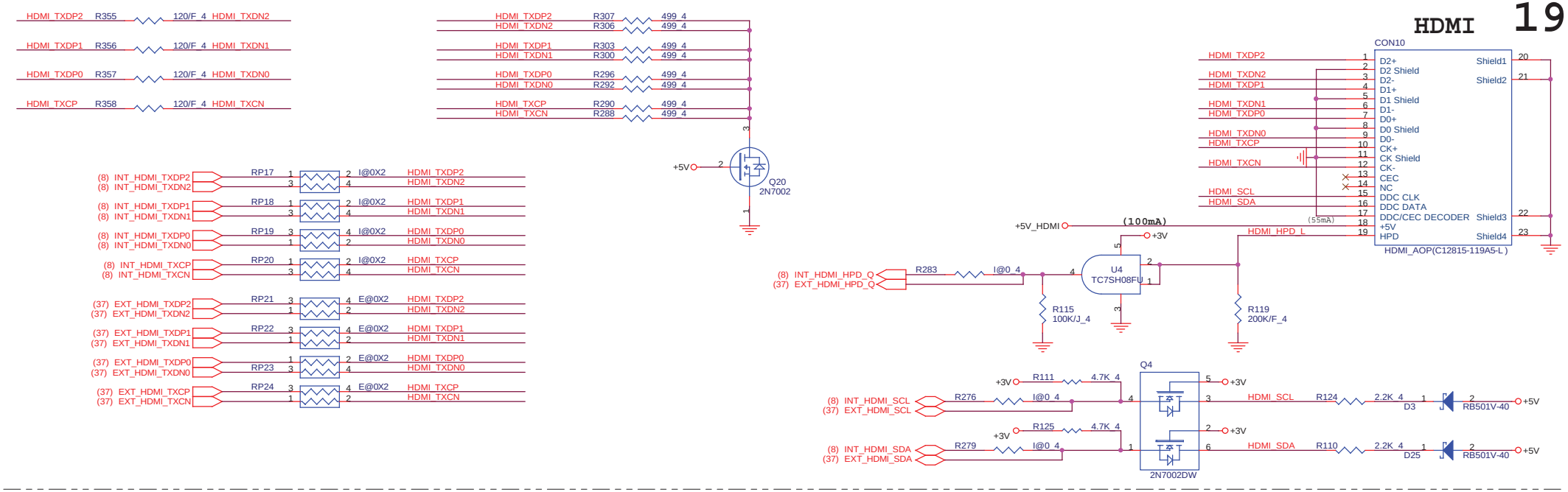
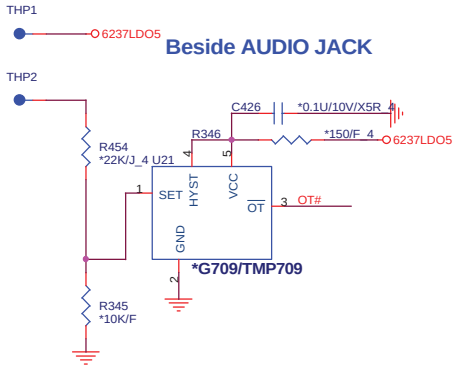
Quanta Computer Inc.
PROJECT :Chief River

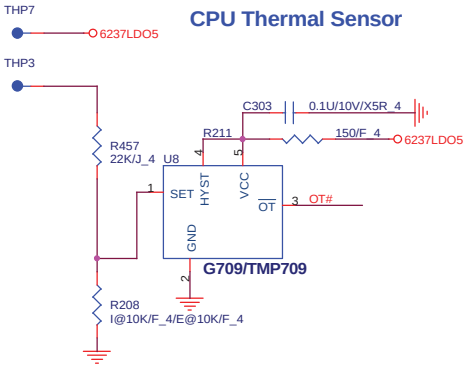
Size	Document Number	Rev
	CARD	1A
Date:	Wednesday, February 01, 2012	Sheet 18 of 43

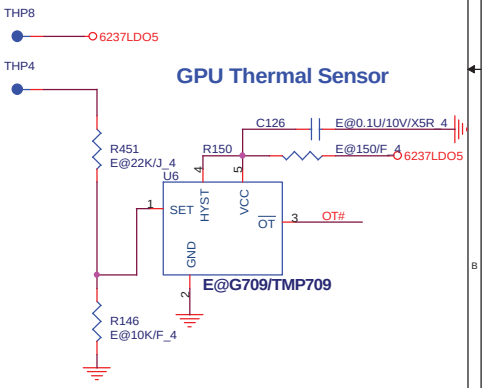
HDMI



H/W Thermal Protect

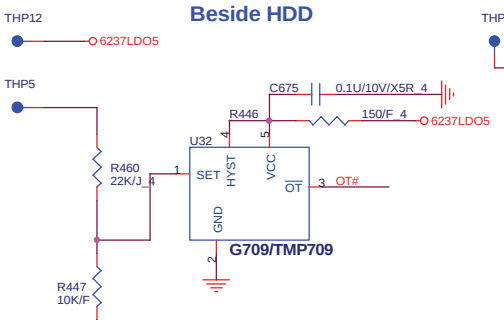


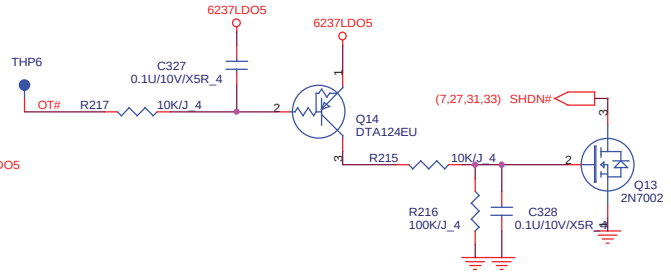




RSET(kΩ) = 0.0012T2 – 0.9308T + 96.147

95	18.5K
100	15K
107	10.3K
110	8.2K





DIS SKU

Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	73	R208=34.59K	34.8K	73.2	72.2
Near GFX sensor temp	73	R146=34.59K	34.8K	73.2	72.2
Near AUDIO sensor temp	55	R345=48.58K	48.7K	55.5	54.2

UMA SKU

Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	82	R208=27.89K	27.4K	83.1	82.2
Near AUDIO sensor temp	55	R345=48.58K	48.7K	55.5	54.2

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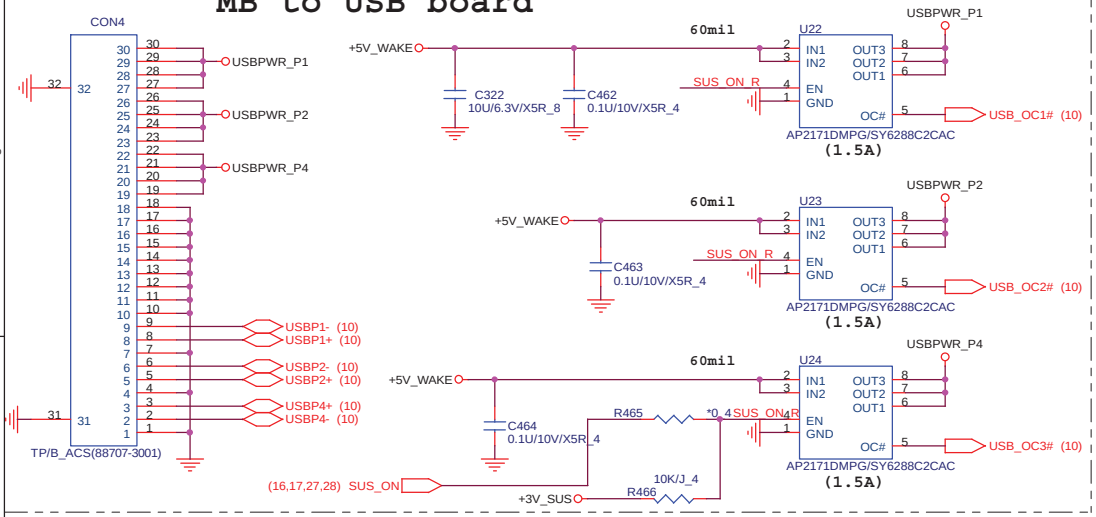
Quanta Computer Inc.
PROJECT : Chief River

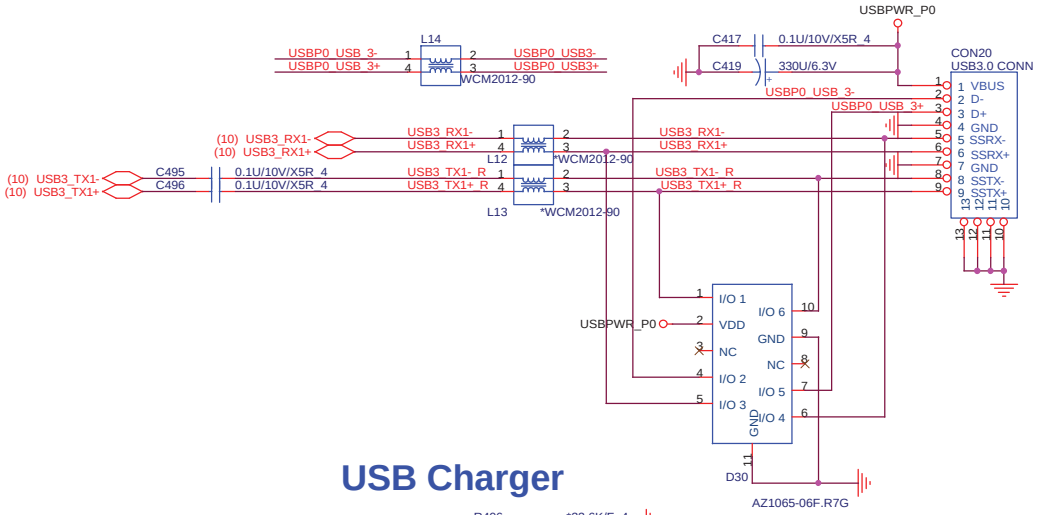
Size	Document Number	Rev
	HDMI/Thermal IC	1A

Date: Friday, February 03, 2012 Sheet 19 of 43

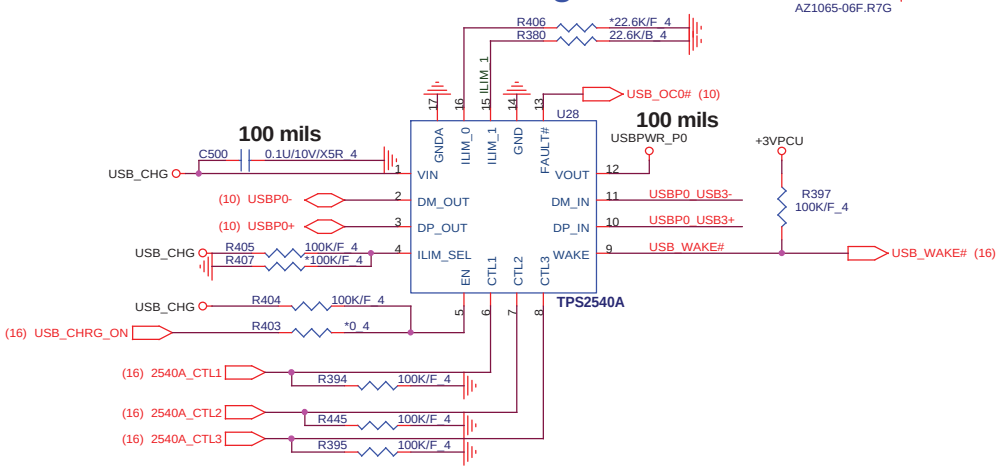
MB to USB board



USB 3.0 PORT0



USB Charger



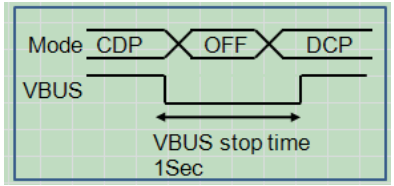
System State	USB Battery Charging Setting	
	Disable	Enable
S0	SDP	CDP
S3	SDP	DCP
Deep Standby	SDP (VBUS OFF)	DCP
S4	SDP (VBUS OFF)	DCP
S5	SDP (VBUS OFF)	DCP

SDP : Standard Downstream Port
CDP : Charging downstream port
DCP : Dedicated Charging Port
Enable/Disable : setting by BIOS

CTL_1	CTL_2	CTL_3	TPS 2540A/2543 Truth Table
0	0	0	OUT discharge, power switch OFF
0	X	1	DCP,Auto-detect(S3/S4/S5, 1.5A)
X	1	0	SDP, USB2.0 mode(S0, 0.5A)
1	0	0	DCP, BC SPEC1.2 only(S3/Deep standby/S4/S5, 1.5A)
1	0	1	DCP, Divider mode only(S3/S4/S5, 1.5A)
1	1	1	CDP (S0, 1.5A)

TPS-2540A	TPS-2543	MODE	AC/DC Mode C1	C2	C3	ILIM_SEL
S0	S0	SDP	X(1)	1	0	X
S0	S0	CDP	1	1	1	1
S3(Wake Enable)	X	SDP	1	1	0	1
S3(Charger Mode)	S3	DCP	1	X(0)	0	1
S4	S4	DCP	1	X(0)	0	1
S5	S5	DCP	1	X(0)	0	1
Discharge	Discharge	DIS	0	0	0	X

DCP: BC 1.2 only.



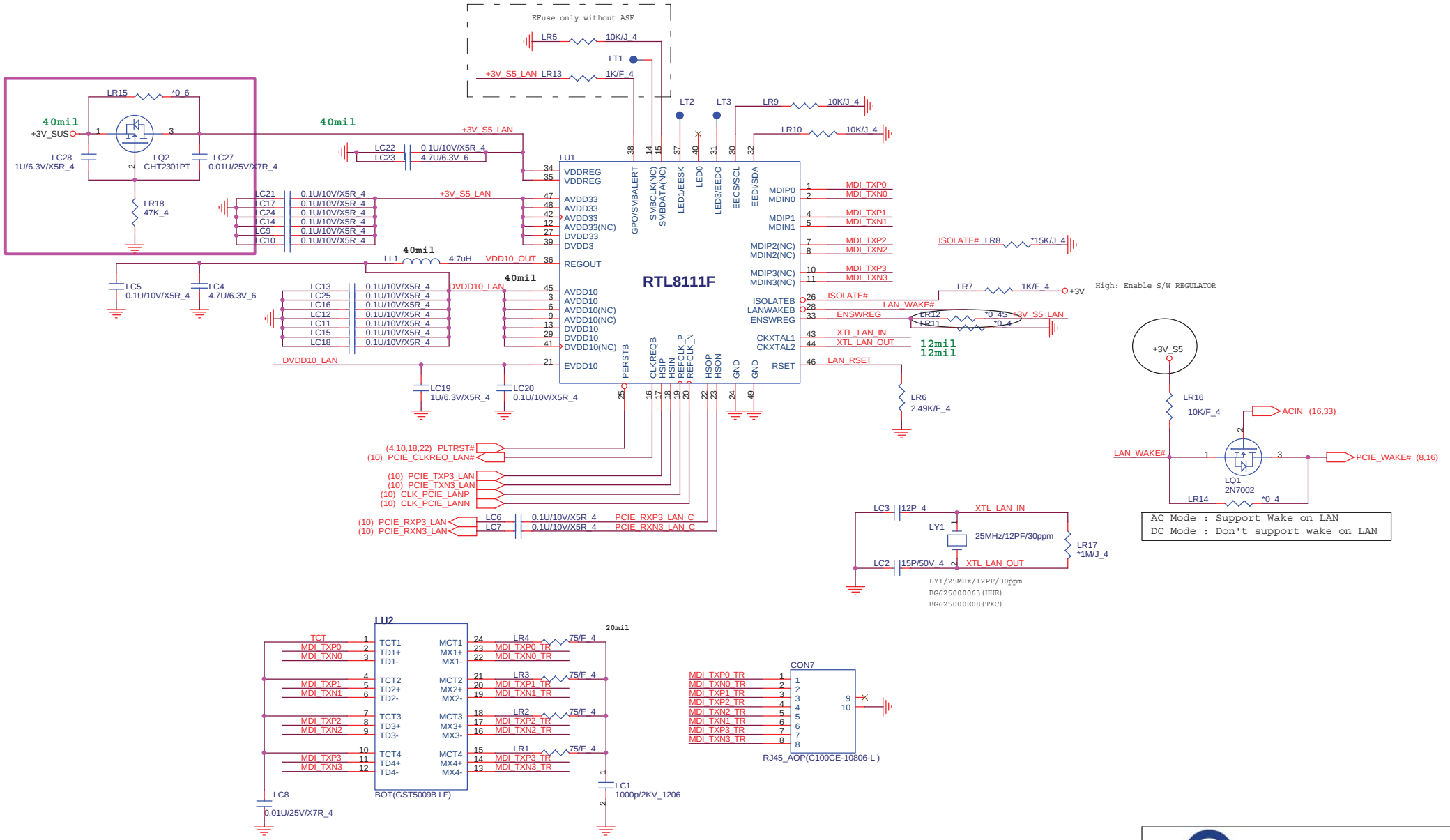
USB WAKE	
1	No device plug(LDO)
0	Device plug(Switch Power)

ILIM_SEL	(I LIMIT(A)= 48000/R)	
HI	I_LIM_1	
LO	I_LIM_0	48000/22.6K=2.123A

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT :Chief River

Size	Document Number	Rev
	USB/USB Charger	1A
Date: Thursday, February 02, 2012	Sheet 20 of 43	

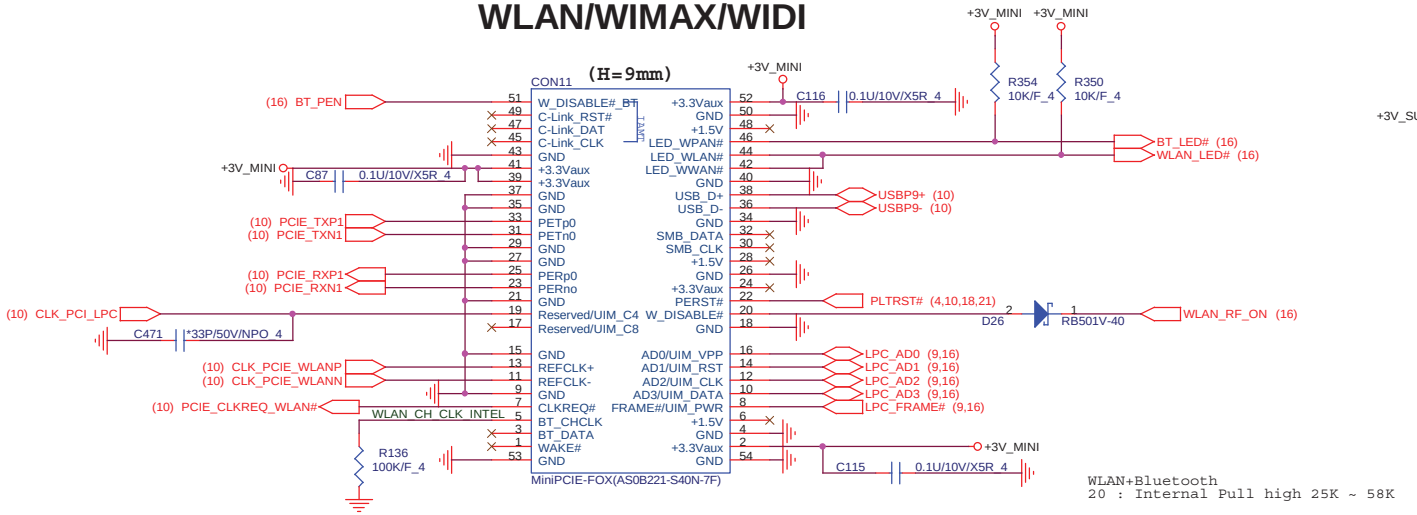


1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

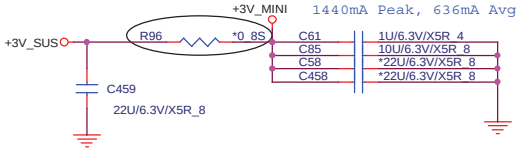
Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	LAN RTL8111E	1A
Date: Wednesday, February 01, 2012	Sheet 21 of 43	

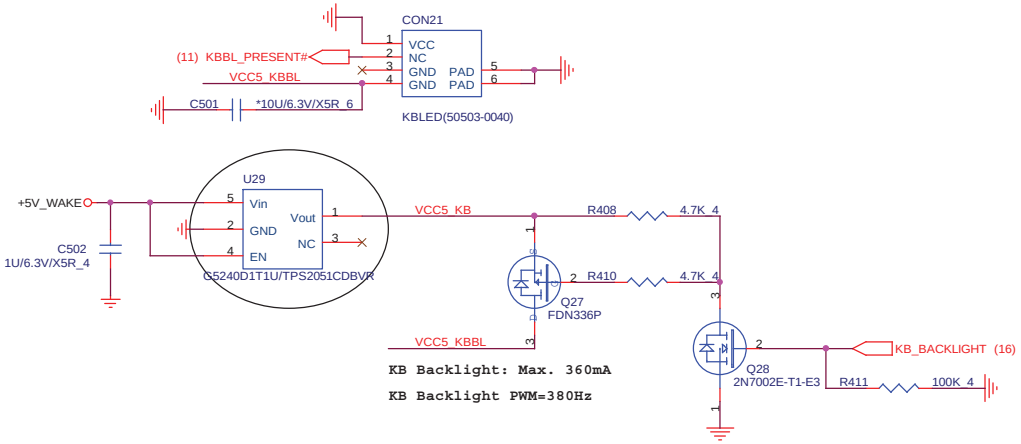
WLAN/WIMAX/WIDI

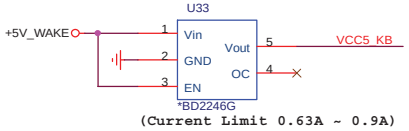


WLAN+Bluetooth
20 : Internal Pull high 25K ~ 58K



KB BACKLIGHT



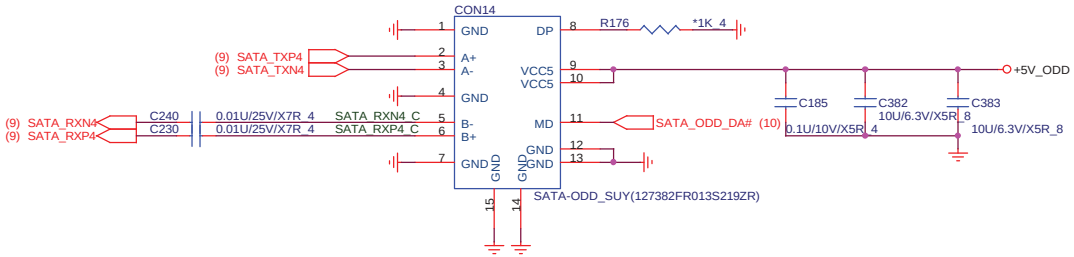


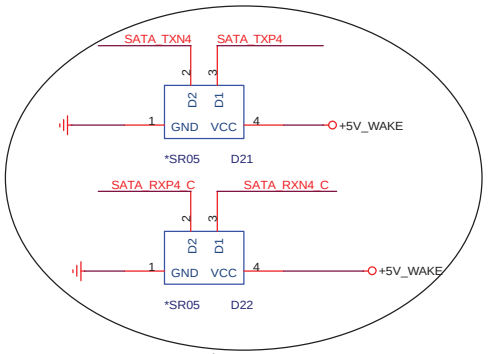
1.Lever 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

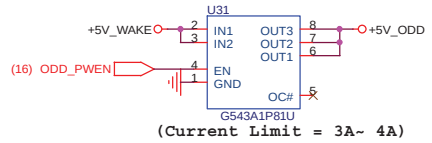
Quanta Computer Inc.
PROJECT :Chief River

Size	Document Number	Rev
	WLAN/KB BL	1A
Date: Wednesday, February 01, 2012	Sheet 22 of 43	

ODD CONNECTOR

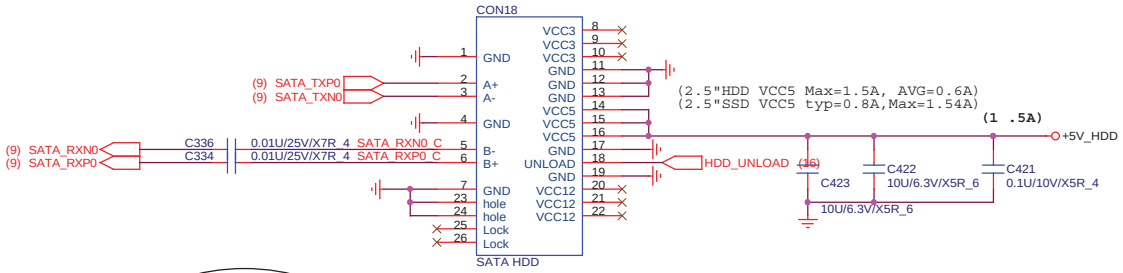


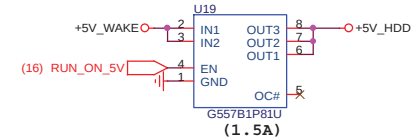


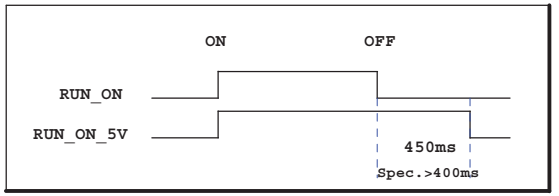


0130-- change ODD ESD diode form Rclamp0502n to SR05

HDD CONNECTOR

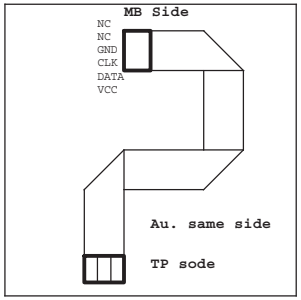


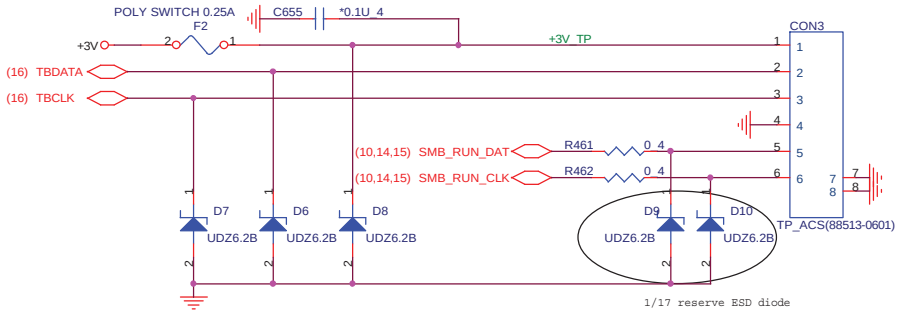




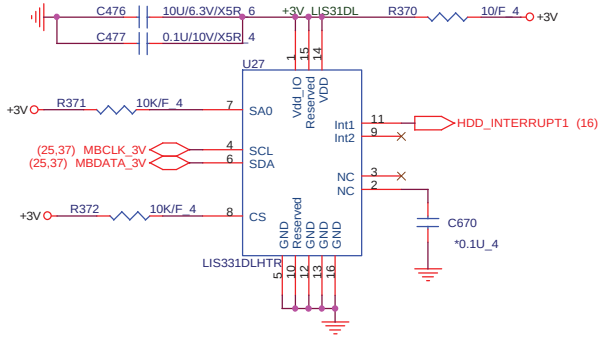
01/30 del D23 , D24 ESD diode

T/P Board to T/P

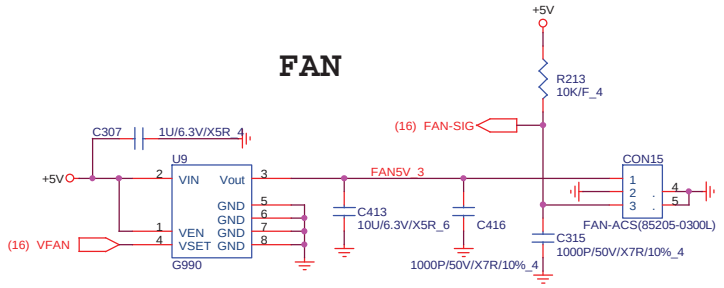




HDD PROTECT



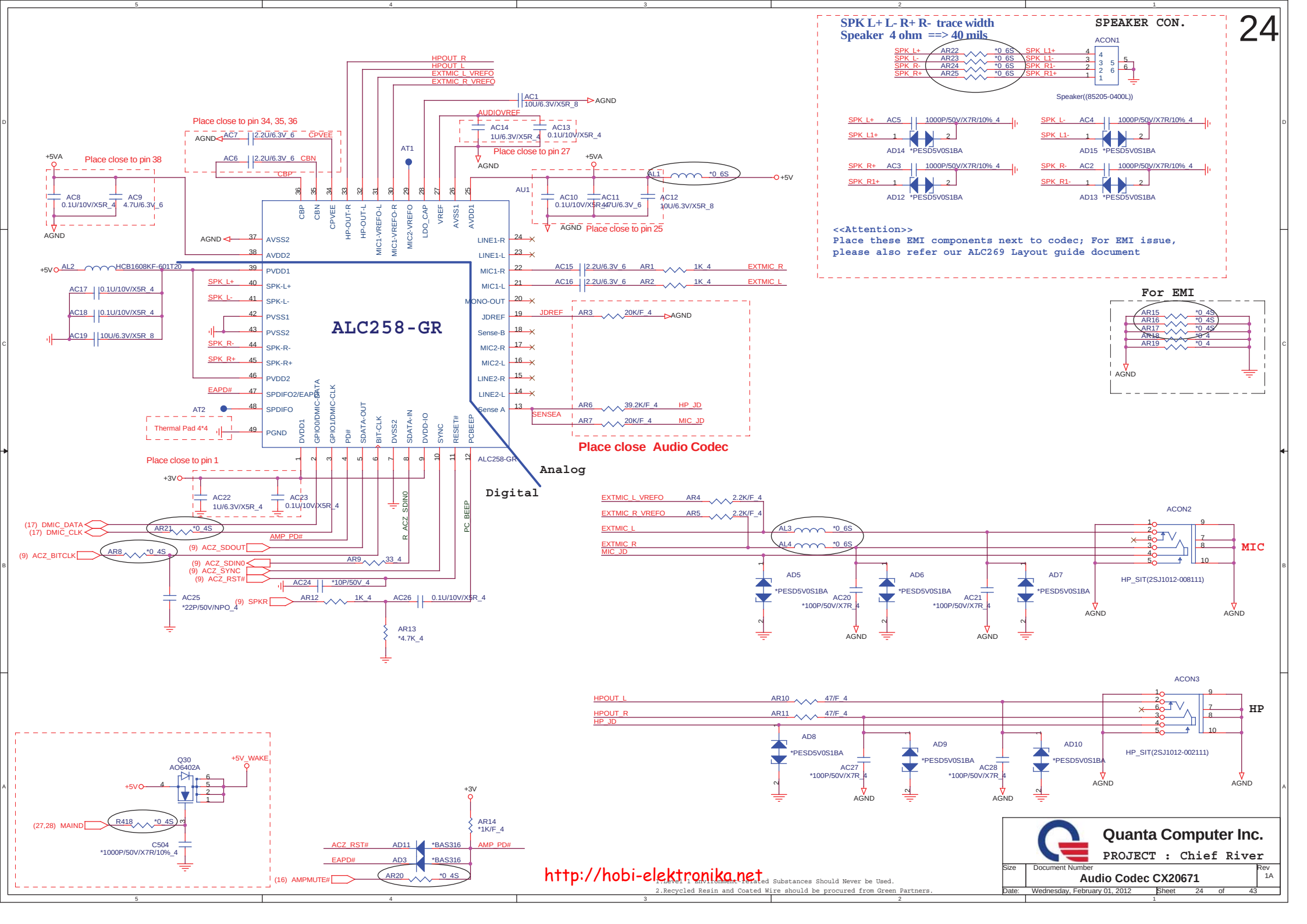
FAN

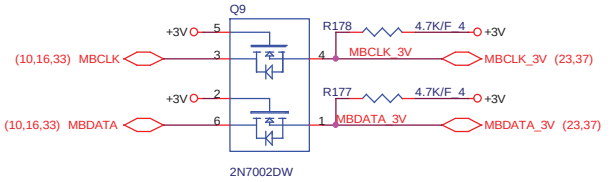


1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

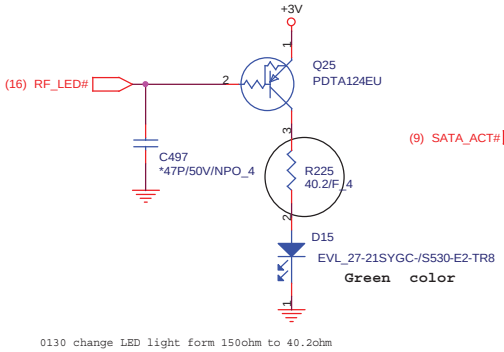
Quanta Computer Inc.
PROJECT :Chief River

Size	Document Number	Rev
	HDD/ODD/TP/FAN	1A
Date: Thursday, February 02, 2012	Sheet 23 of 43	


SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 40 mils
SPEAKER CON.
ACON1
Speaker((85205-0400L))
<<Attention>>
Place these EMI components next to codec; For EMI issue,
please also refer our ALC269 Layout guide document
For EMI
ALC258-GR
Analog
Digital
Place close to pin 34, 35, 36
Place close to pin 38
Place close to pin 27
Place close to pin 25
Place close to pin 1
Place close Audio Codec
Thermal Pad 4*4
MIC
HP
HP_SIT(2SJ1012-008111)
HP_SIT(2SJ1012-002111)
http://hobi-elektronika.net
1.Level 1 Environment Related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.
Quanta Computer Inc.
PROJECT : Chief River
Audio Codec CX20671
Wednesday, February 01, 2012
Sheet 24 of 43

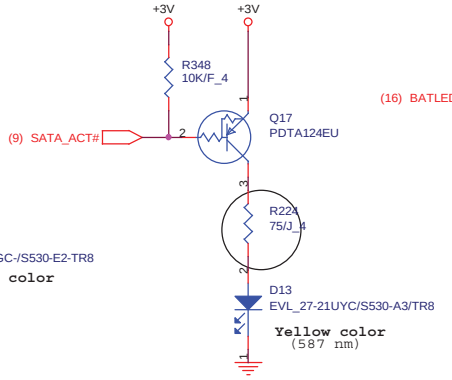


RF LED



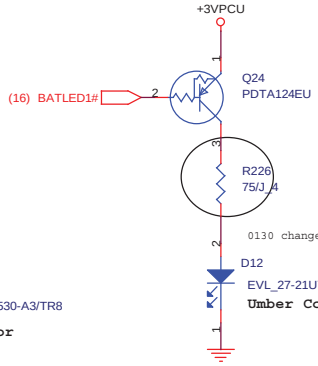
0130 change LED light form 150ohm to 40.2ohm

SATA LED



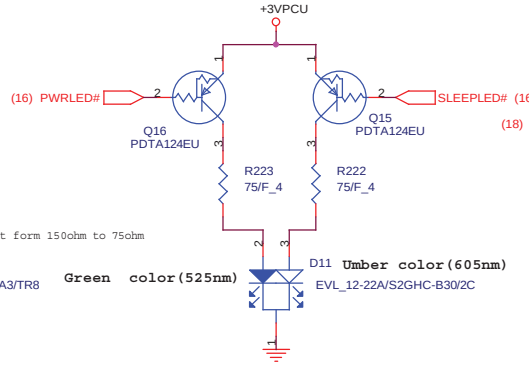
0130 change LED light form 150ohm to 75ohm

BATTERY LED

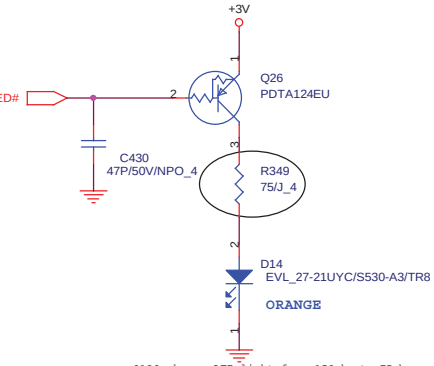


0130 change LED light form 150ohm to 75ohm

Power/Sleep LED

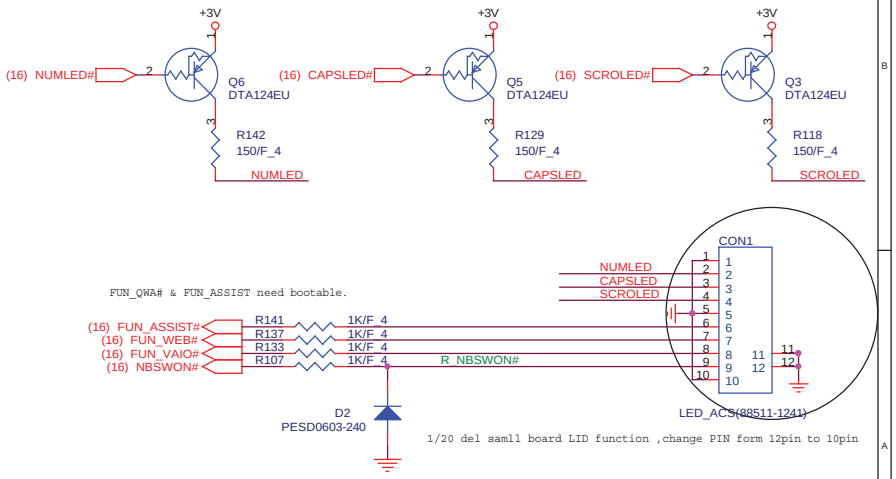


CARD LED



0130 change LED light form 150ohm to 75ohm

Power SW Board Connector

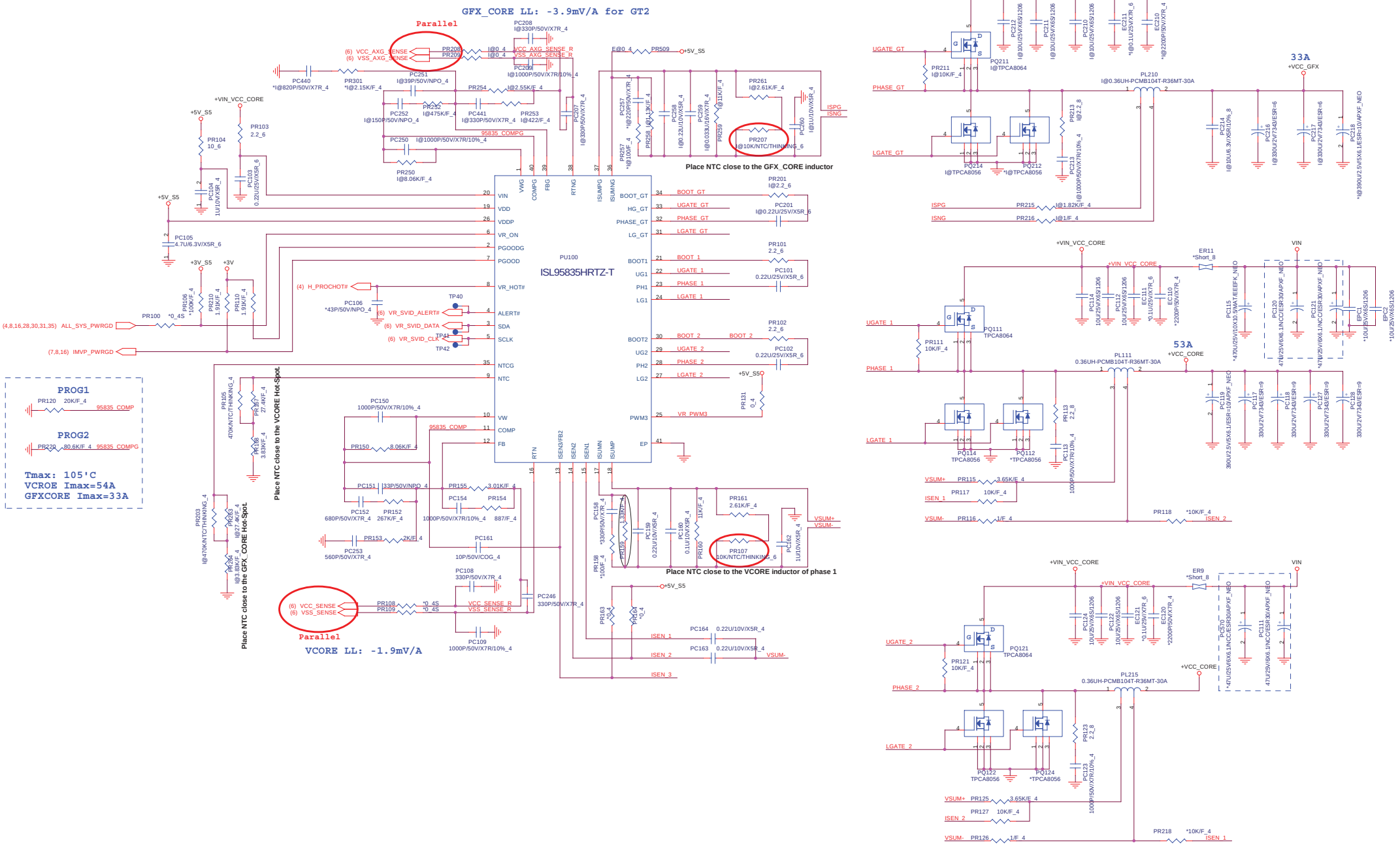


1/20 del samll board LID function ,change PIN form 12pin to 10pin

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT :Chief River

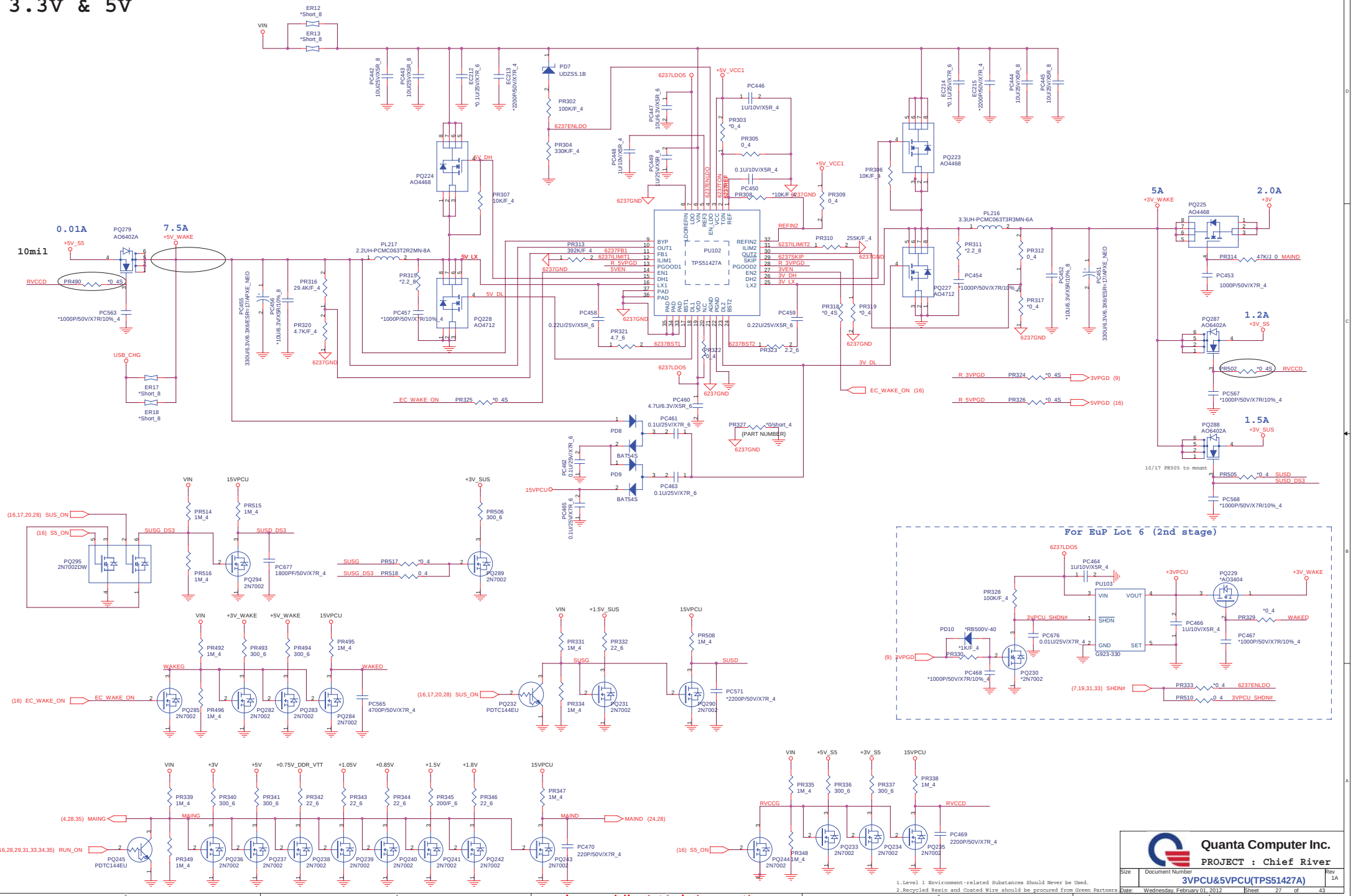
Size	Document Number	Rev
	LED/RF/KB/PS	1A
Date: Wednesday, February 01, 2012	Sheet 25 of 43	



Quanta Computer Inc.
PROJECT :Chief River

Size	Document Number	Rev
	+VCC_CORE (ISL95835)	ES1
Date: Wednesday, February 01, 2012	Sheet 26 of 43	

3.3V & 5V



1.Level 1 Environment-related Substances Should Never be Used.
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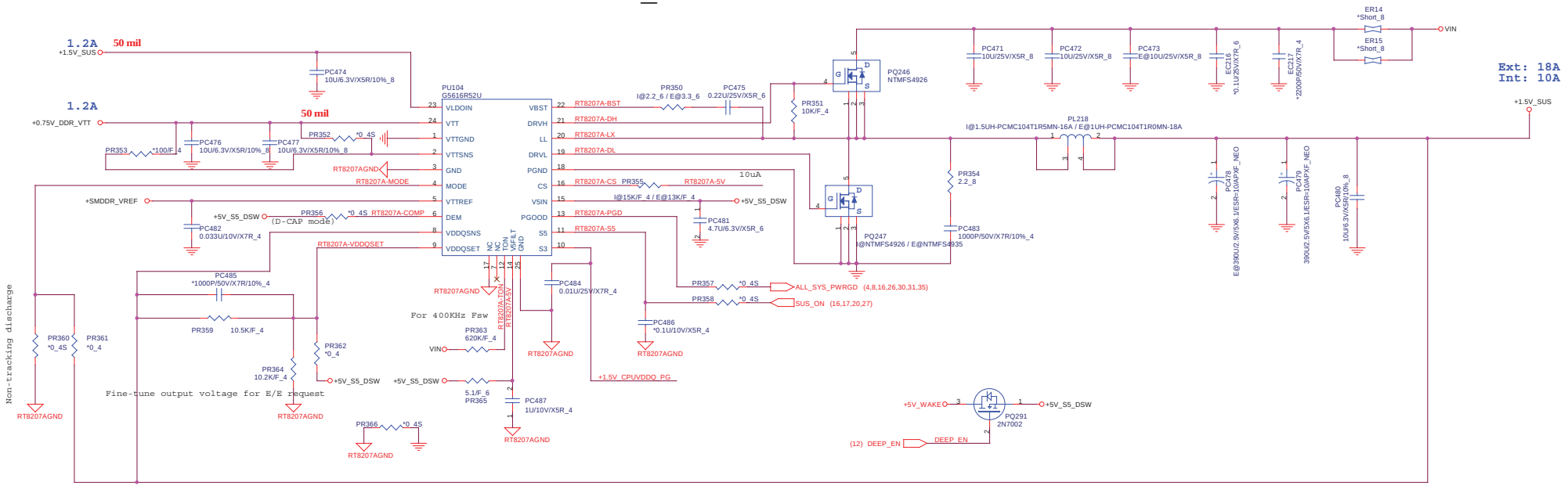
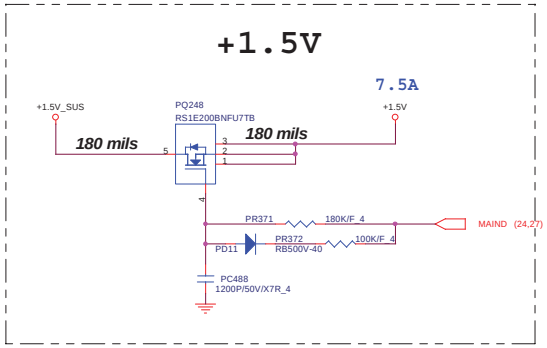
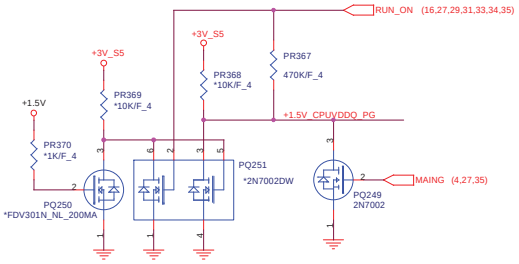
Quanta Computer Inc.
PROJECT : Chief River

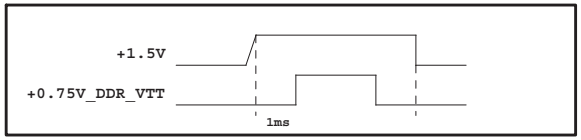
Size	Document Number	Rev
	3VPCU&5VPCU(TPS51427A)	1A
Date: Wednesday, February 01, 2012	Sheet 27 of 43	

1.5VSUS & VTT_MEM









MODE	DISCHARGE MODE
+5V	No discharge
+1.5V	Tracking discharge
GND	Non-tracking discharge

VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	1.5 fixed	VDDQSNS/2	DDR3
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

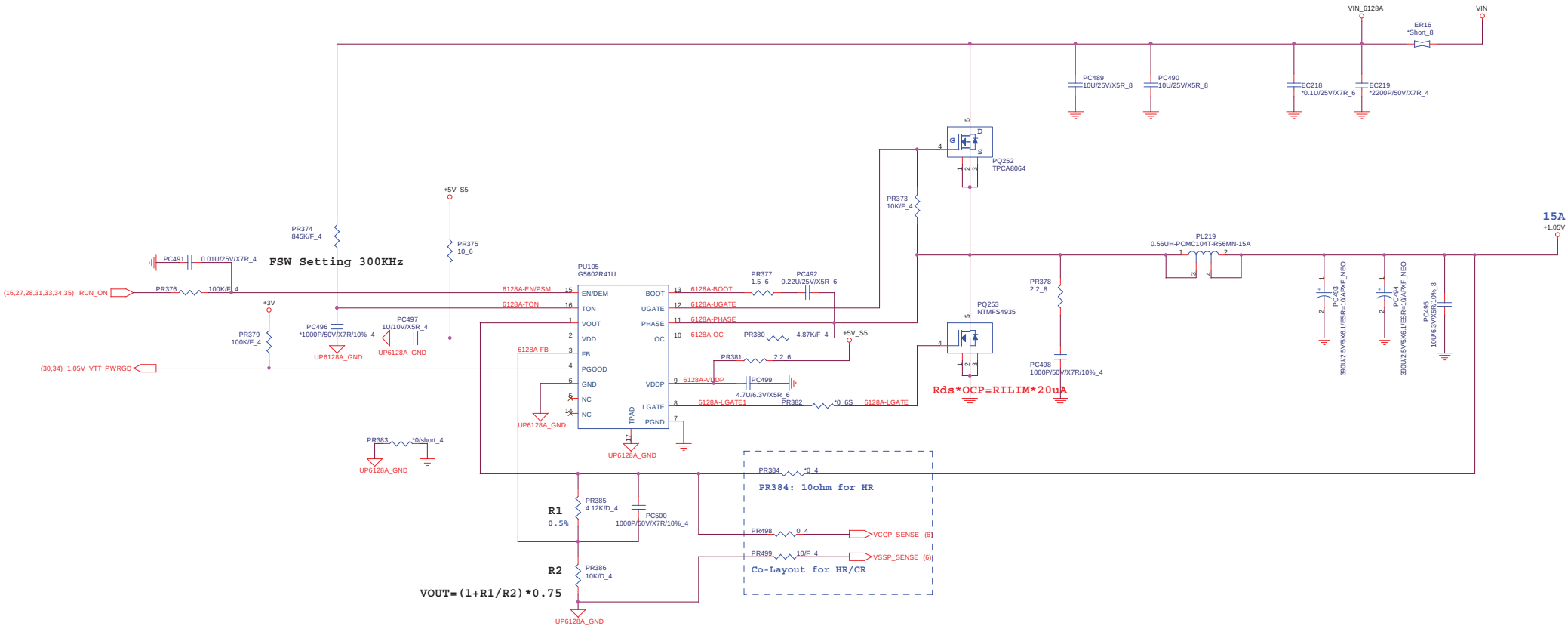
VTT = VTTREF = VDDQSNS/2 = 0.75V

STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : Chief River

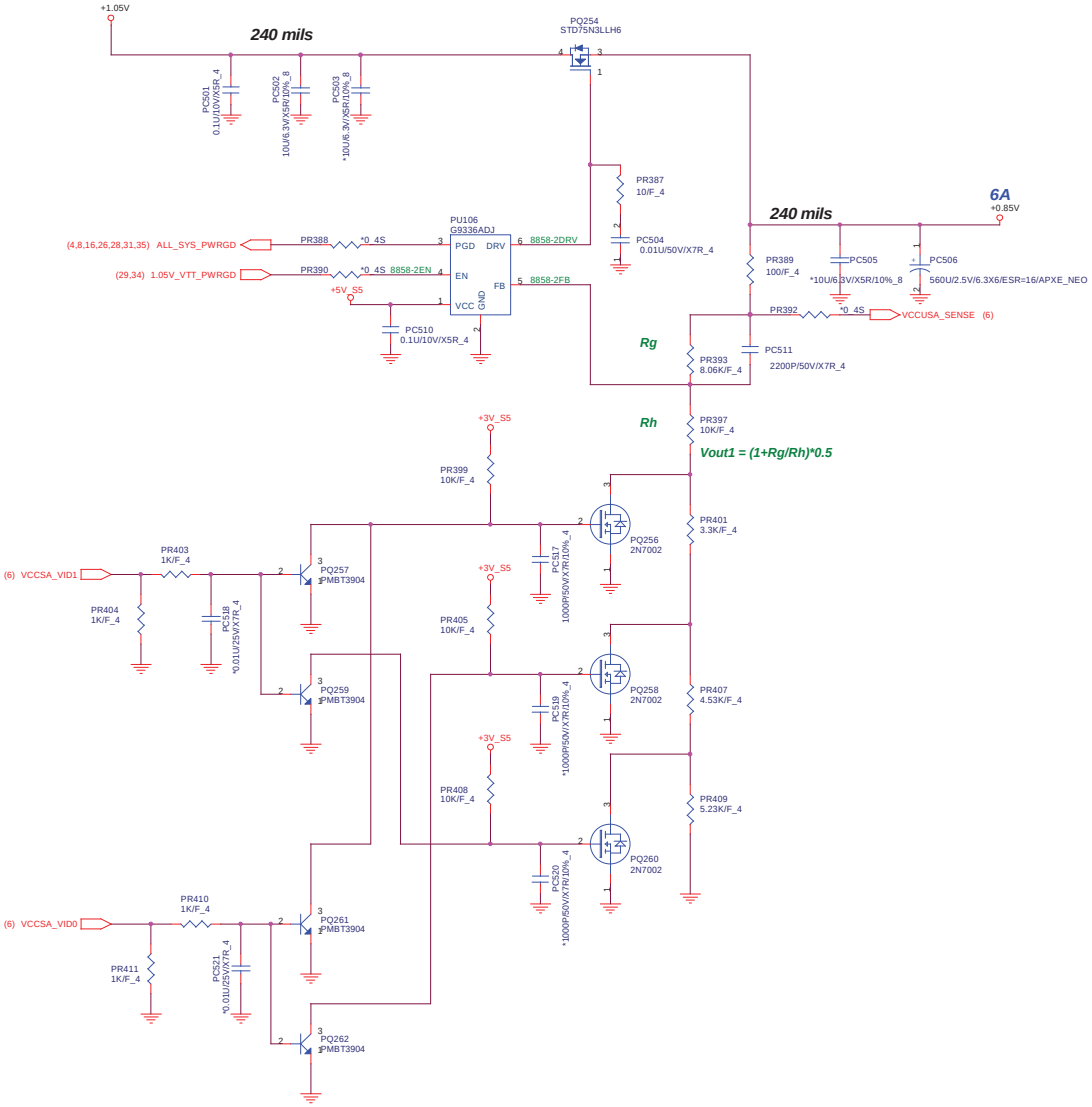
Size	Document Number	Rev
	1.5VSUS/VTT_MEM	1A
Date: Wednesday, February 01, 2012	Sheet 28 of 43	



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.		
PROJECT : Chief River		
Size	Document Number	Rev
	+1.05V (UP1522RQDD)-15A	1A
Date: Thursday, February 02, 2012	Sheet 29 of 43	

VCCSA



VID 0	VID 1	+0.85V
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

VCCIO

1.Level 1 Environment-related Substances Should Never be Used.
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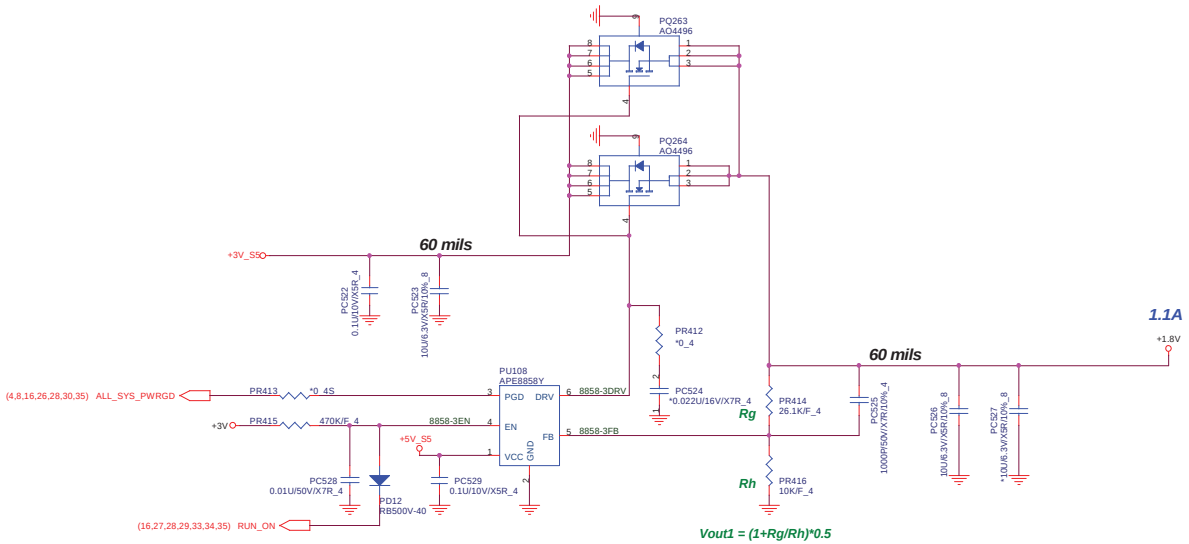
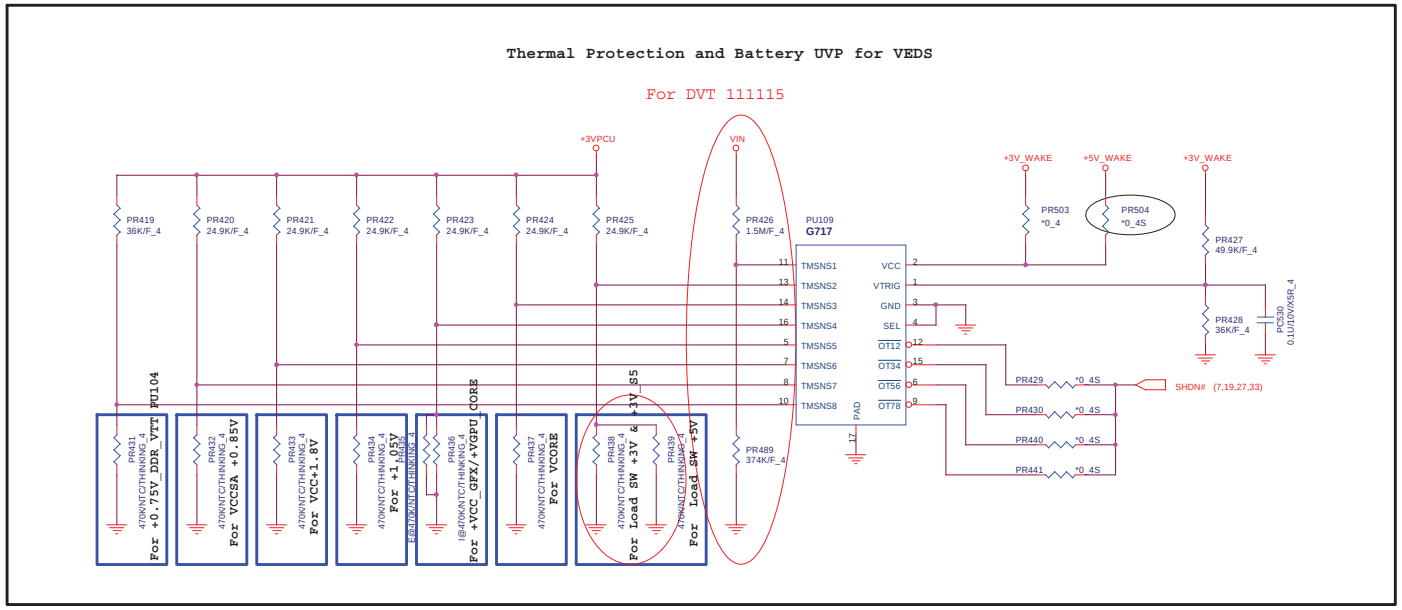
Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	VCCSA / VCCIO	1A
Date: Wednesday, February 01, 2012	Sheet 30 of 43	

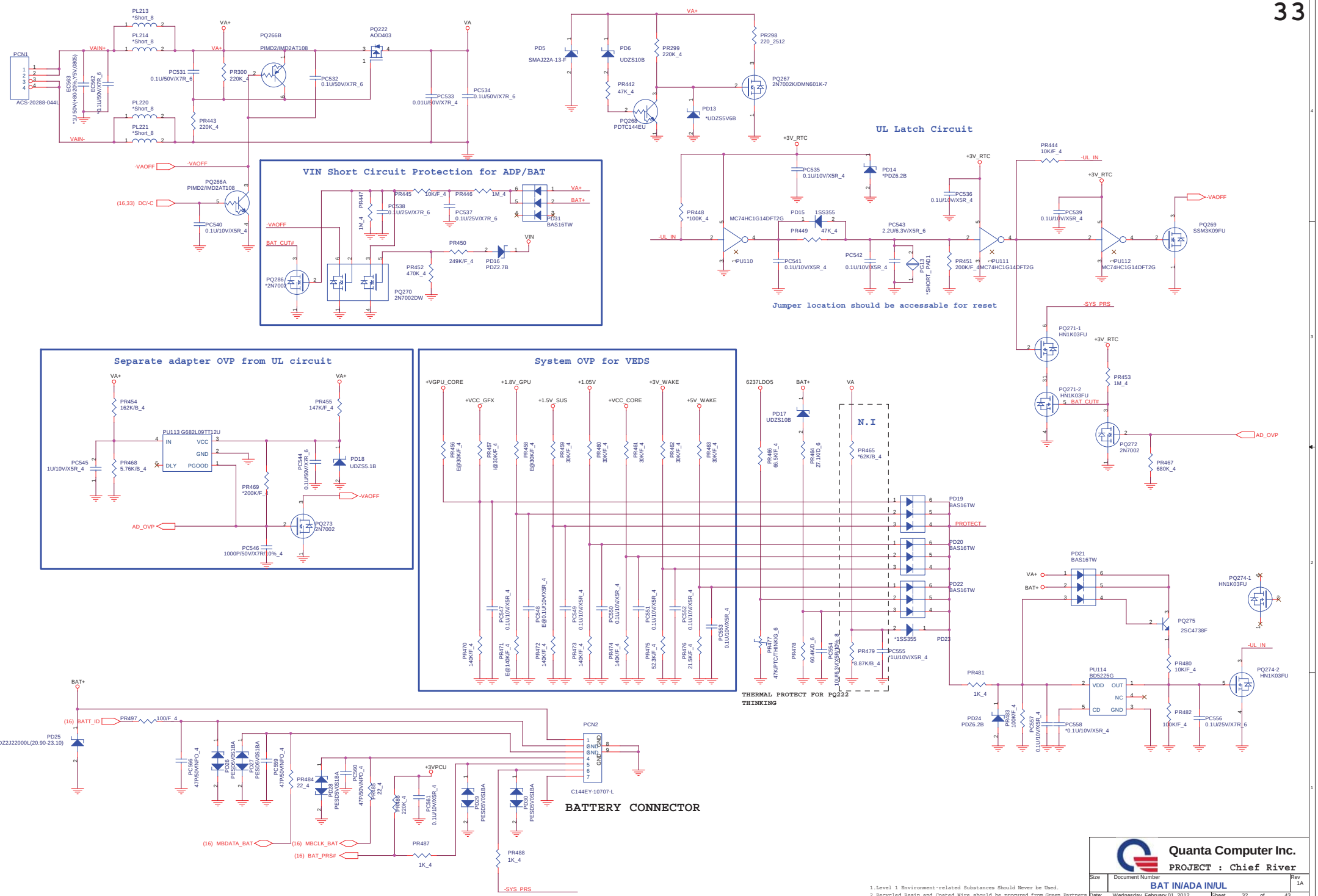
VCC1.8





Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	VCC1.8	1A
Date:	Wednesday, February 01, 2012	Sheet 31 of 43



1.Level 1 Environment-related Substances Should Never be Used.
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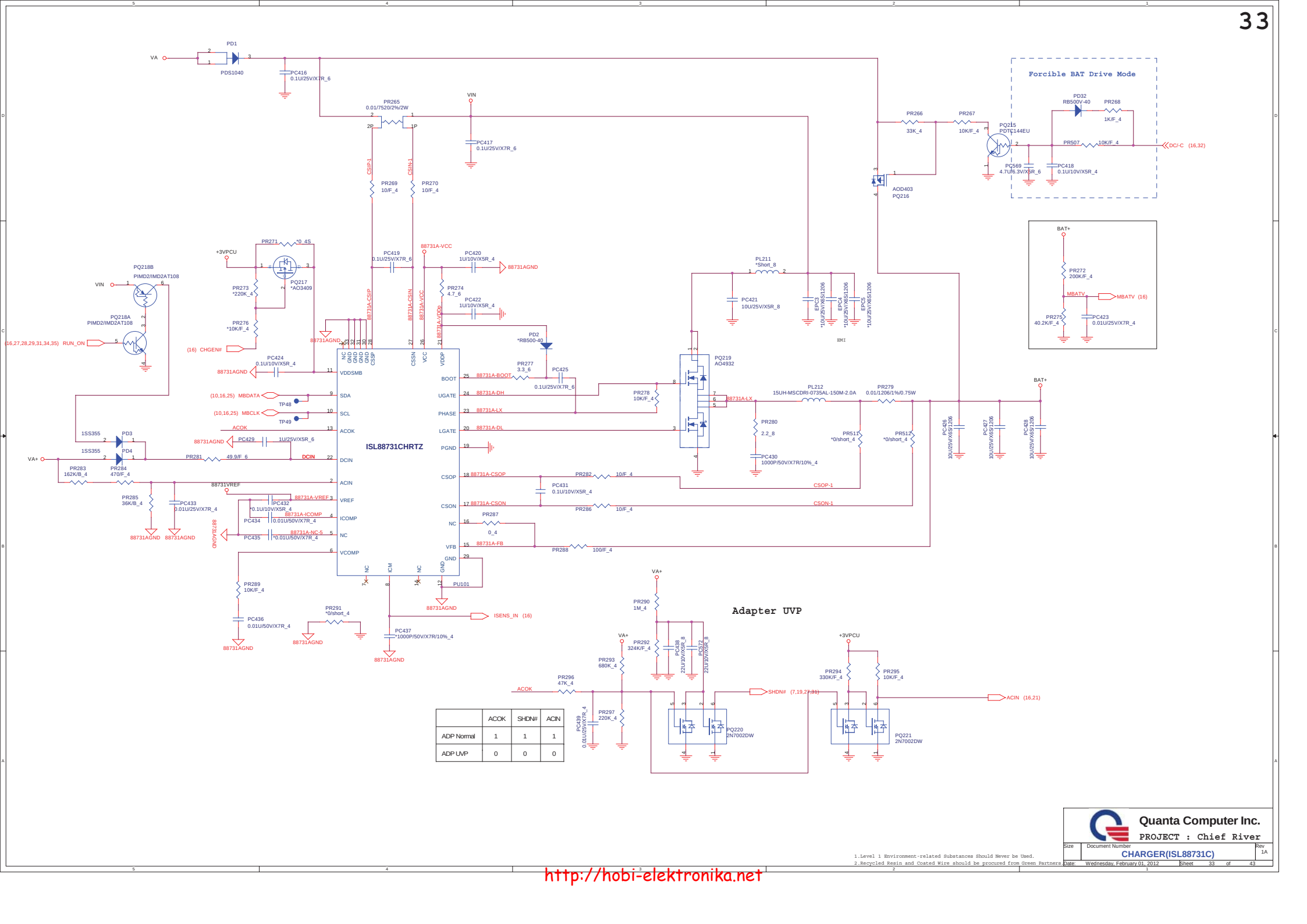
Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	BAT IN/ADA IN/UL	1A
Date: Wednesday, February 01, 2012	Sheet 32 of 43	



	ACOK	SHDN#	ACIN
ADP Normal	1	1	1
ADP UVP	0	0	0

1.Level 1 Environment-related Substances Should Never be Used.
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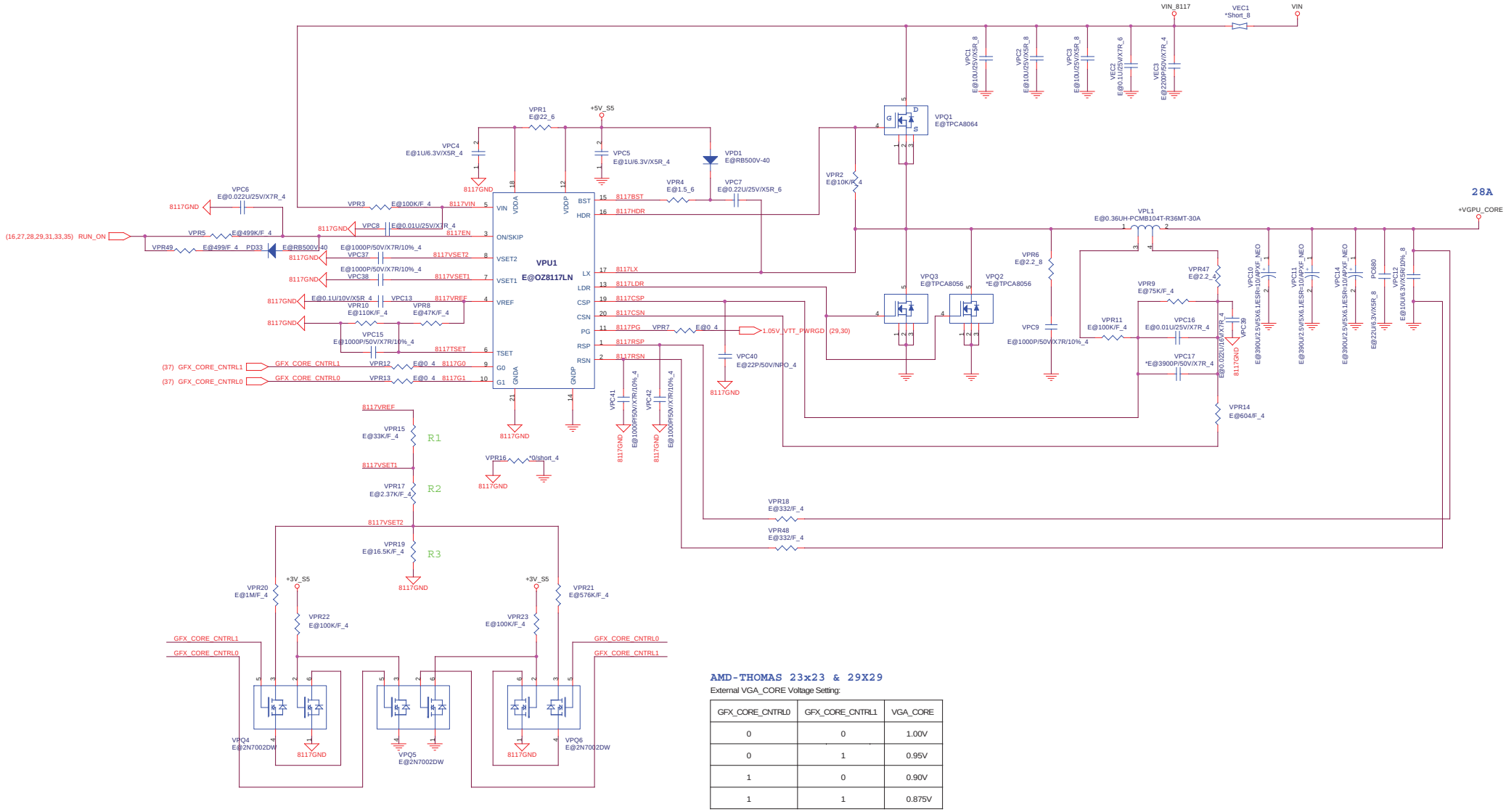
Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	CHARGER(ISL88731C)	1A
Date: Wednesday, February 01, 2012	Sheet 33 of 43	



AMD-THOMAS 23x23 & 29X29

External VGA_CORE Voltage Setting:

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	VGA_CORE
0	0	1.00V
0	1	0.95V
1	0	0.90V
1	1	0.875V

1.Level 1 Environment-related Substances Should Never be Used.
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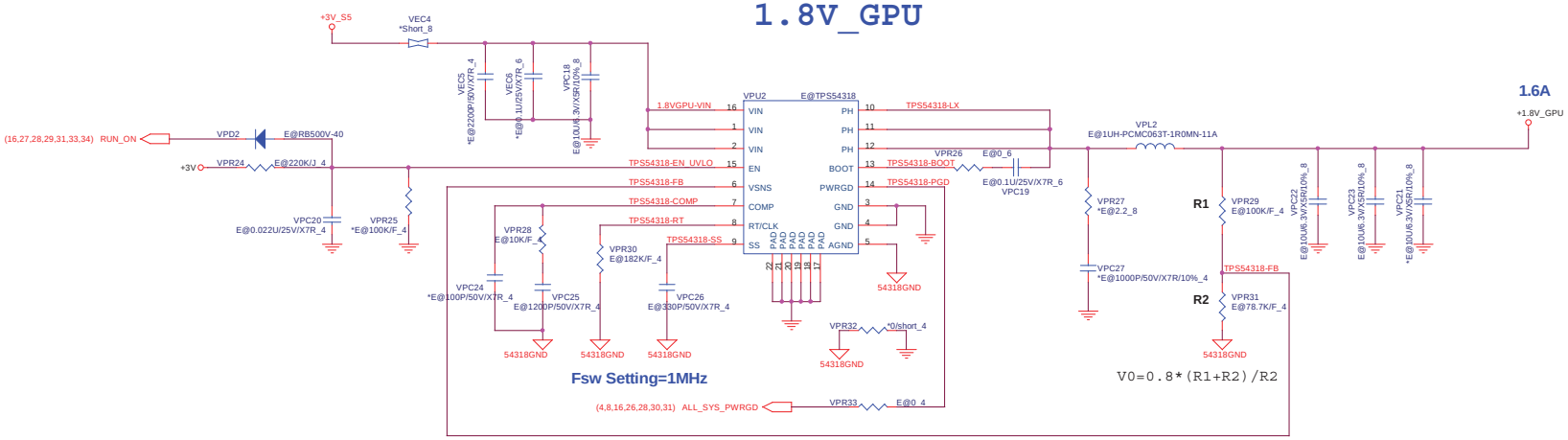
Quanta Computer Inc.
PROJECT : Chief River

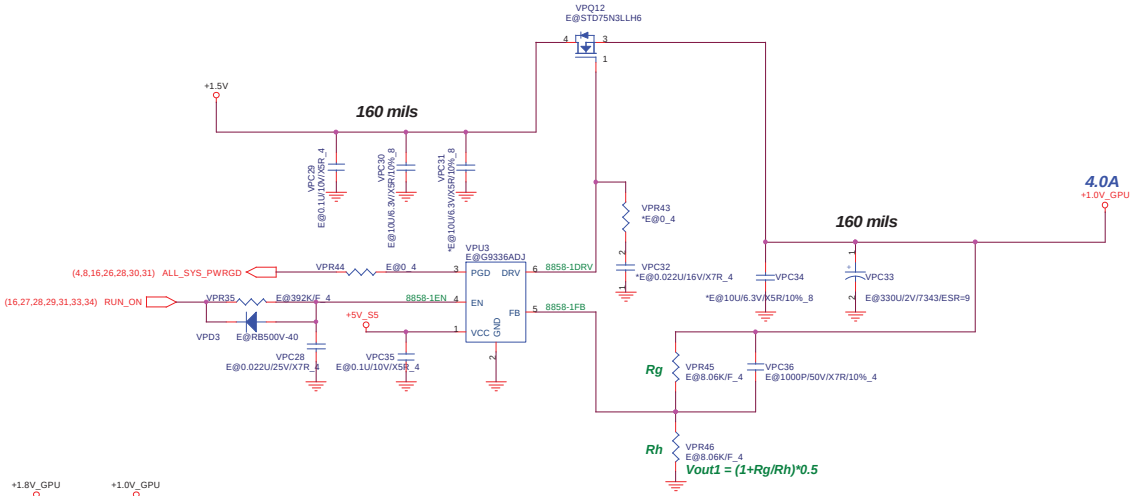
Size	Document Number	Rev
	VGA_CORE (OZ8117)	1A

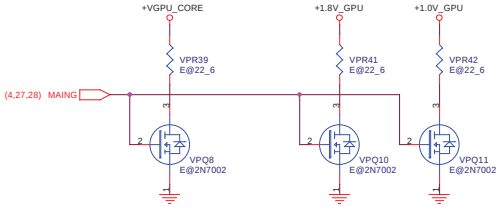
Date: Wednesday, February 01, 2012 Sheet 34 of 43

1.8V_GPU



+1.0V_GPU (Support VRAM 900MHz)





1.Level 1 Environment-related Substances Should Never be Used.
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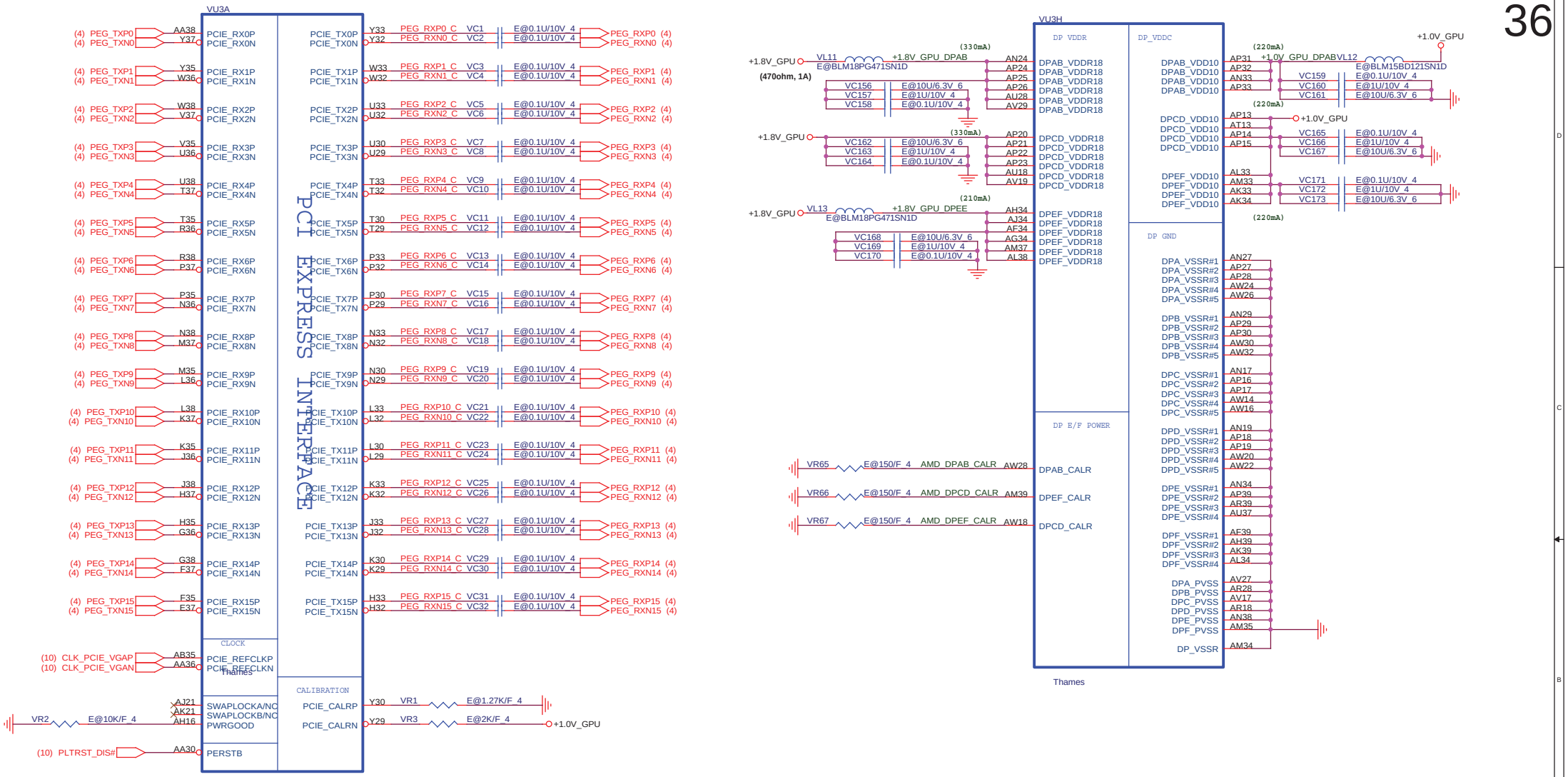
Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	1.8_GPU / 1.0_GPU	1A
Date: Wednesday, February 01, 2012	Sheet 35 of 43	



Thames necessary Power-on sequence

All power rails reach nominal within 20ms

1 => +3V_GPU
2 => +VDDC_CORE
3 => +1.0V_GPU
3 => +1.8V_GPU

1.Lever 1 Environment-related Substances Should Never be Used.
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Quanta Computer Inc.
PROJECT : HK5

Size	Document Number	Rev
	Thames/PCIE	1A
Date: Wednesday, February 01, 2012	Sheet 36 of 43	

VRAM TYPE

+1.8V_GPU

VR4	E@10K/J_4	RAM_TYPE_CFG0	VR5	*E@10K/J_4	
VR6	*E@10K/J_4	RAM_TYPE_CFG1	VR7	*E@10K/J_4	
VR8	*E@10K/J_4	RAM_TYPE_CFG2	VR9	*E@10K/J_4	
VR10	*E@10K/J_4	RAM_TYPE_CFG3	VR11	*E@10K/J_4	

Note : Required Frequency = 900 MHz

Memory Straps	MCLK:900Mhz	RAM_TYPE_CFG3	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0
900 MHz 2Gb(128M*16) Hynix_Vega die	H5TQ2G63BFR-11C	0	0	0	0
900 MHz 2Gb(128M*16) Samsung_C die	K4W2G1646C-HC11	0	0	0	1
900 MHz 1Gb(64M*16) Hynix_Vega die	H5TQ1G63DFR-11C	0	0	1	0
900 MHz 1Gb(64M*16) Samsung_G die	K4W1G1646G-BC11	0	0	1	1

VU3B

MUTI GFX

DPA: TXCAP_DPA3P / TXCAM_DPA3N, TX0P_DPA2P / TX0M_DPA2N, TX1P_DPA1P / TX1M_DPA1N, TX2P_DPA0P / TX2M_DPA0N, TXCBP_DPB3P / TXCBM_DPB3N

DPB: TX3P_DPB2P / TX3M_DPB2N, TX4P_DPB1P / TX4M_DPB1N, TX5P_DPB0P / TX5M_DPB0N, TXCCP_DPC3P / TXCCM_DPC3N

DPC: TX0P_DPC2P / TX0M_DPC2N, TX1P_DPC1P / TX1M_DPC1N, TX2P_DPC0P / TX2M_DPC0N, TXCDP_DPD3P / TXCDM_DPD3N

DPD: TX3P_DPD2P / TX3M_DPD2N, TX4P_DPD1P / TX4M_DPD1N, TX5P_DPD0P / TX5M_DPD0N

AU24	EXT_HDMI_TXCP_C	VC33	E@0.1U/10V/X5R_4
AV24	EXT_HDMI_TXCN_C	VC34	E@0.1U/10V/X5R_4
AT25	EXT_HDMI_TXDP0_C	VC39	E@0.1U/10V/X5R_4
AR24	EXT_HDMI_TXDN0_C	VC40	E@0.1U/10V/X5R_4
AU26	EXT_HDMI_TXDP1_C	VC37	E@0.1U/10V/X5R_4
AV25	EXT_HDMI_TXDN1_C	VC38	E@0.1U/10V/X5R_4
AT27	EXT_HDMI_TXDP2_C	VC35	E@0.1U/10V/X5R_4
AR26	EXT_HDMI_TXDN2_C	VC36	E@0.1U/10V/X5R_4

EXT_HDMI_TXCP (19), EXT_HDMI_TXCN (19), EXT_HDMI_TXDP0 (19), EXT_HDMI_TXDN0 (19), EXT_HDMI_TXDP1 (19), EXT_HDMI_TXDN1 (19), EXT_HDMI_TXDP2 (19), EXT_HDMI_TXDN2 (19)

DVPCNTL_MVP_0 (AR8), DVPCNTL_MVP_1 (AU8), DVPCNTL_0 (AP8), DVPCNTL_1 (AW8), DVPCNTL_2 (AR3), DVPCLK (AR1)

RAM_TYPE_CFG0 (AU1), RAM_TYPE_CFG1 (AU3), RAM_TYPE_CFG2 (AW3), RAM_TYPE_CFG3 (AP6)

DVPDATA_0 (AW5), DVPDATA_1 (AU5), DVPDATA_2 (AR6), DVPDATA_3 (AW6), DVPDATA_4 (AU6), DVPDATA_5 (AT7), DVPDATA_6 (AV7), DVPDATA_7 (AN7), DVPDATA_8 (AV9), DVPDATA_9 (AT9), DVPDATA_10 (AR10), DVPDATA_11 (AW10), DVPDATA_12 (AU10), DVPDATA_13 (AP10), DVPDATA_14 (AV11), DVPDATA_15 (AT11), DVPDATA_16 (AR12), DVPDATA_17 (AW12), DVPDATA_18 (AU12), DVPDATA_19 (AP12), DVPDATA_20, DVPDATA_21, DVPDATA_22, DVPDATA_23

I2C: SCL (AK26), SDA (AJ26)

(17) EXT_EDIDCLK, (17) EXT_EDIDDAT, +3V, VR13 E@2.2K/F_4, VR12 E@2.2K/F_4

GENERAL PURPOSE I/O

GPIO_0 (AH20), GPIO_1 (AH18), GPIO_2 (AN16), GPIO_3_SMBDATA (AH23), GPIO_4_SMBCLK (AJ23), GPIO_5_AC_BATT (AH17), GPIO_6 (AJ17), GPIO_7_BLON (AK17), GPIO_8_ROMSO (AJ13), GPIO_9_ROMSI (AH15), GPIO_10_ROMSCK (AJ16), GPIO_11 (AK16), GPIO_12 (AL16), GPIO_13 (AM16), GPIO_14_HPD2 (AM14), GPIO_15_PWRCNTL_0 (AM13), GPIO_16_SSIN (AK14), GPIO_17_THERMAL_INT (AG30), GPIO_18_HPD3 (AN14), GPIO_19_CTF (AM17), GPIO_20_PWRCNTL_1 (AL13), GPIO_21_BB_EN (AJ14), GPIO_22_ROMCSB (AK13), GPIO_23_CLKREQB (AN13), JTAG_TRSTB (AM23), JTAG_TDI (AN23), JTAG_TCK (AK23), JTAG_TMS (AL24), JTAG_TDO (AM24), GENERICA (AJ19), GENERICB (AK19), GENERICC (AJ20), GENERICD (AK20), GENERICE_HPD4 (AJ24), GENERICF (AH26), GENERICG (AH24)

(23,25) MBDATA_3V, (23,25) MBCLK_3V, (16) EXT_LVDS_BLON, (34) GFX_CORE_CNTRL0, (34) GFX_CORE_CNTRL1, TEMP_FAIL, GPIO22_SCS#, VT13–VT17

DAC1: R (AD39), RB (AD37), G (AE36), GB (AD35), B (AE37), BB (AE38), HSYNC (AC36), VSYNC (AC38), RSET (AB34), AVDD (AD34), AVSSQ (AE34), VDD1DI (AC33), VSS1DI (AC34)

VR16 E@150/F_4 EXT_CRT_RED (17); VR19 E@150/F_4 EXT_CRT_GRE (17); VR20 E@150/F_4 EXT_CRT_BLU (17)

EXT_CRT_HSYNC (17), EXT_CRT_VSYNC (17)

AMD_RSET, VR21 E@499/F_4, +1.8V_GPU_AVDD_Q 1.8V(70mA), VL1 E@BLM15BD121SN1D, VC41 E@0.1U/10V_4, VC43 E@10U/6.3V_6, +1.8V_GPU

1.8V(45mA VDD1DI), +1.8V_GPU, VC44 E@0.1U/10V_4, VC45 E@1U/10V/X5R_4

NC/R2 (AC39), NC/R2B (AC31), NC/G2 (AD39), NC/G2B (AD33), NC/B2 (AE39), NC/B2B (AE33), NC/C (AC32), NC/Y (AD32), NC/COMP (AE32)

DAC2: GENLK_CLK/H2SYNC (AD29), GENLK_VSYNC/V2SYNC (AC29) — VT25, VT26

NC/VDD2DI (AG31), NC/VSS2DI (AG32), NC/A2VDD (AG33), NC/A2VDDQ (AD33), TSVSSQ/A2VSSQ (AE33), NC/R2SET (AA29)

DDC/AUX: DDC1CLK (AM26), DDC1DATA (AN26) — EXT_HDMI_SCL (19), EXT_HDMI_SDA (19)

AUX1P (AM27), AUX1N (AL27), DDC2CLK (AM19), DDC2DATA (AL19), AUX2P (AN28), AUX2N (AM28), DDCCLK_AUX3P (AL30), DDCDATA_AUX3N (AM30), DDCCLK_AUX4P (AL29), DDCDATA_AUX4N (AM29), DDCCLK_AUX5P (AN21), DDCDATA_AUX5N (AM21), DDC6CLK (AJ30), DDC6DATA (AJ31) — EXT_DDCCLK (17), EXT_DDCDAT (17), DDCCLK_AUX7P (AK30), DDCDATA_AUX7N (AK29)

(19) EXT_HDMI_HPD_Q, HPD1 (AK24)

VREFG (AH13): VR33 E@499/F_4, VR34 E@249/F_4, VC46 E@0.1U/10V_4, +1.8V_GPU

DPLL_PVDD (AM32), DPLL_PVSS (AN32), DPLL_VDDC (AN31)

+1.8V_GPU, VL2 E@BLM15BD121SN1D, 120ohm, 300mA, (1.8V @ 120mA DPLL_PVDD), VC48 E@1U/10V_4, VC49 E@10U/6.3V_6, +DPLL_PVDD

+1.0V_GPU, VL3 E@BLM15BD121SN1D, 1.0V @ 150mA DPLL_VDDC, VC50 E@10U/6.3V_6, VC51 E@1U/10V_4, +DPLL_VDDC

XTALIN (AV33), XTALOUT (AU34), XTAIN_AMD, XTAOUT_AMD

VY1 27MHZ/20PF/20PPM (BG627000289 (HKE), BG627000505 (TXC)), E@27MHZ/20PF/20PPM, VR39 E@1M_4, VC53 E@27P_4, VC54 E@27P_4

XO_IN (AW34), SS_IN (AW35)

DPLUS (AF29), DMINUS (AG29), THERMAL

TS_FDO (AK32), NC (AL31)

TSVDD (AJ32), TSVSS (AJ33)

+1.8V_GPU, VL4 E@BLM15BD121SN1D, +1.8V_GPU_TSVDD (5mA), VC55 E@10U/6.3V_6, VC56 E@1U/10V_4

VU3G

LVDS CONTROL: VARY_BL (AK27), DIGON (AJ27) — EXT_LVDS_BRIGHT (17), EXT_LVDS_VDDEN (17)

TXCLK_UP_DPF3P (AK35), TXCLK_UN_DPF3N (AL35), TXOUT_U0P_DPF2P (AJ38), TXOUT_U0N_DPF2N (AK37), TXOUT_U1P_DPF1P (AH35), TXOUT_U1N_DPF1N (AJ36), TXOUT_U2P_DPF0P (AG38), TXOUT_U2N_DPF0N (AH37), TXOUT_U3P (AF35), TXOUT_U3N (AG36)

LVTMDP: TXCLK_LP_DPE3P (AP34), TXCLK_LN_DPE3N (AR34), TXOUT_L0P_DPE2P (AW37), TXOUT_L0N_DPE2N (AU35), TXOUT_L1P_DPE1P (AR37), TXOUT_L1N_DPE1N (AU39), TXOUT_L2P_DPE0P (AP35), TXOUT_L2N_DPE0N (AR35), TXOUT_L3P (AN36), TXOUT_L3N (AP37)

EXT_TXLCLKOUTP (17), EXT_TXLCLKOUTN (17), EXT_TXLOUTP0 (17), EXT_TXLOUTN0 (17), EXT_TXLOUTP1 (17), EXT_TXLOUTN1 (17), EXT_TXLOUTP2 (17), EXT_TXLOUTN2 (17)

Thames

	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	1.0V
M	0	1	0.95V
H	1	0	0.9V
TBD	1	1	0.875V

APERTURE SIZE

Databook mean : 512MB 1GMB memory setting should be 256MB

+3V; VR14 E@10K/J_4 RAM_CFG0, VR15 *E@10K/J_4 RAM_CFG1, VR17 *E@10K/J_4 RAM_CFG2, VR18 *E@10K/J_4 GPIO22_SCS#

MEMORY APERTURE SIZE SELECT

MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

+3V; VR24 *E@10K/J_4 GPIO0, VR25 *E@10K/J_4 GPIO1, VR26 E@10K/J_4 GPIO2, VR27 *E@10K/J_4 GPIO5, VR28 *E@10K/J_4 GPIO6, VR29 *E@10K/J_4 GPIO8_SOUT, VR30 *E@10K/J_4 GPIO9_SIN, VR31 *E@10K/J_4 GPIO10_SCLK, VR120 E@10K/J_4 EXT_CRT_HSYNC, VR121 E@10K/J_4 EXT_CRT_VSYNC

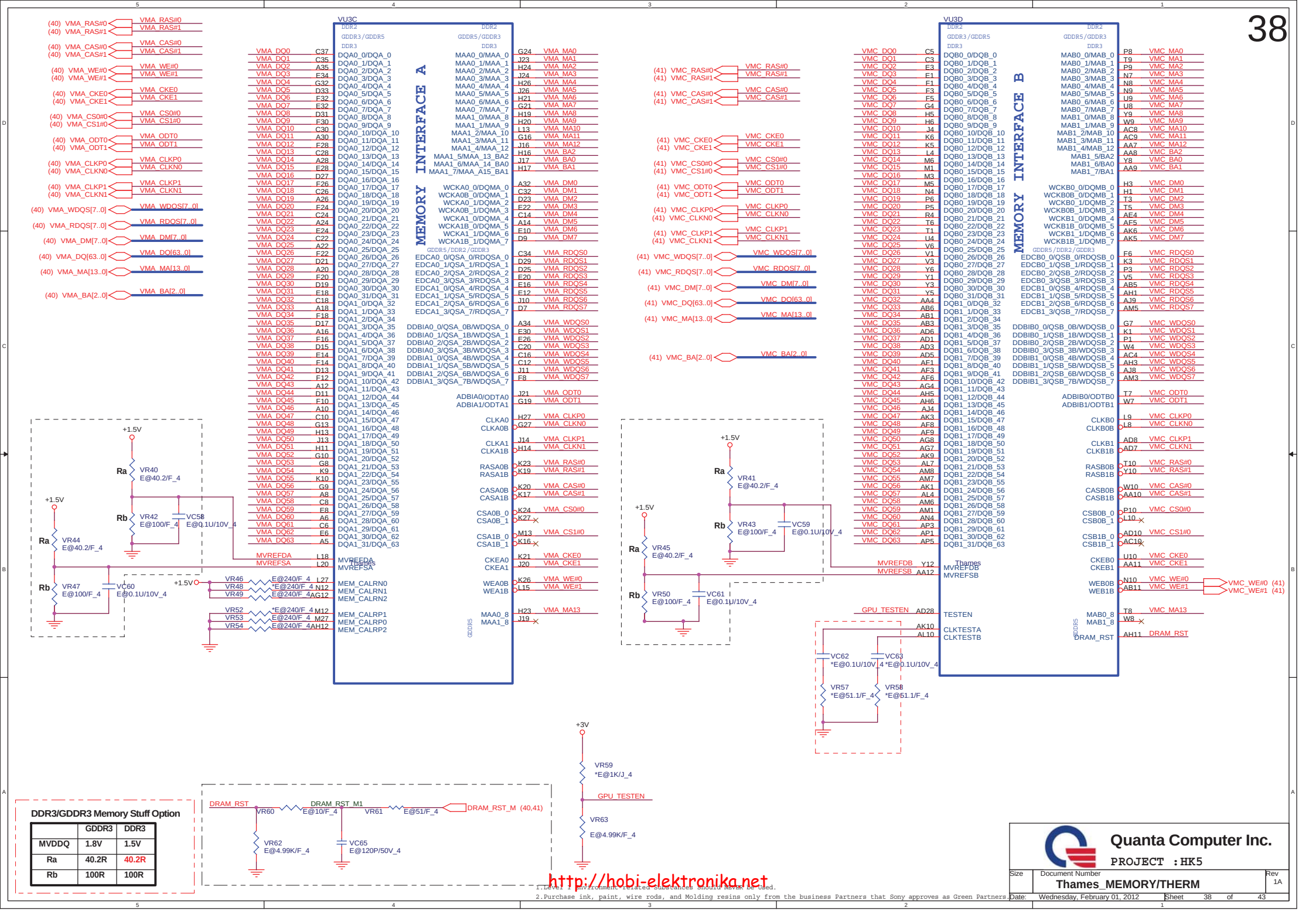
CONFIGURATION STRAPS

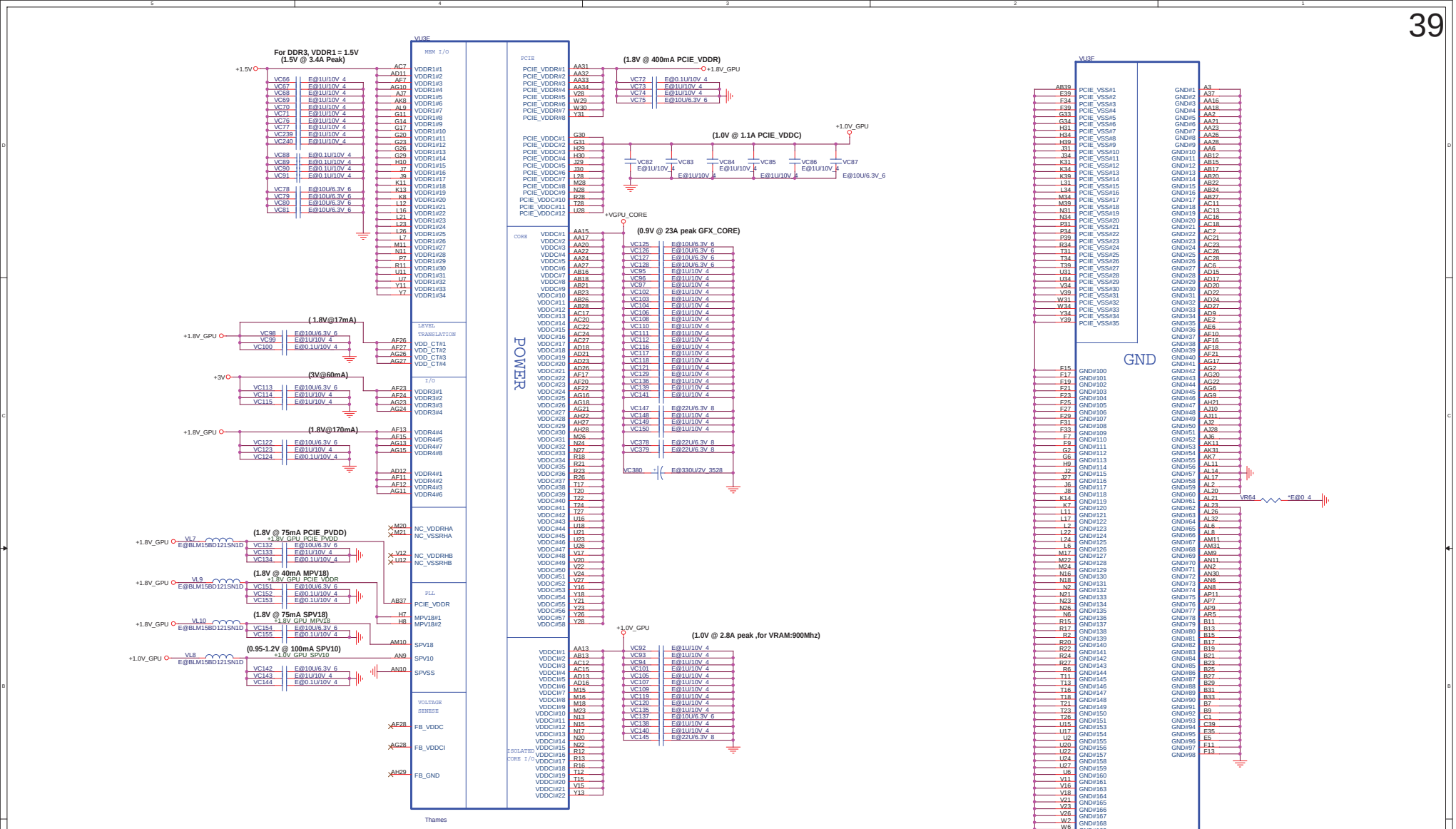
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	0
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	1
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	1
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	11
VIP_DEVICE_STRAP_EN	BIOS_ROM_EN	ViP Device Strap Enable 0 = Disable ; 1 = Enable	0

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : HK5

Size	Document Number	Rev
	Thames_IO&STRAP	1A
Date: Wednesday, February 01, 2012	Sheet 37 of 43	


VU3C
MEMORY INTERFACE A
DDR2
GDDR3/GDDR5
DDR3
GDDR5/DDR2/GDDR3
VU3D
MEMORY INTERFACE B
Thames_MEMORY/THERM
Quanta Computer Inc.
PROJECT :HK5
Size
Document Number
Rev
1A
Date: Wednesday, February 01, 2012
Sheet 38 of 43
DDR3/GDDR3 Memory Stuff Option
MVDDQ 1.8V 1.5V
Ra 40.2R 40.2R
Rb 100R 100R
1.Level 1 environment related substances should NEVER be used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.
http://hobi-elektronika.net



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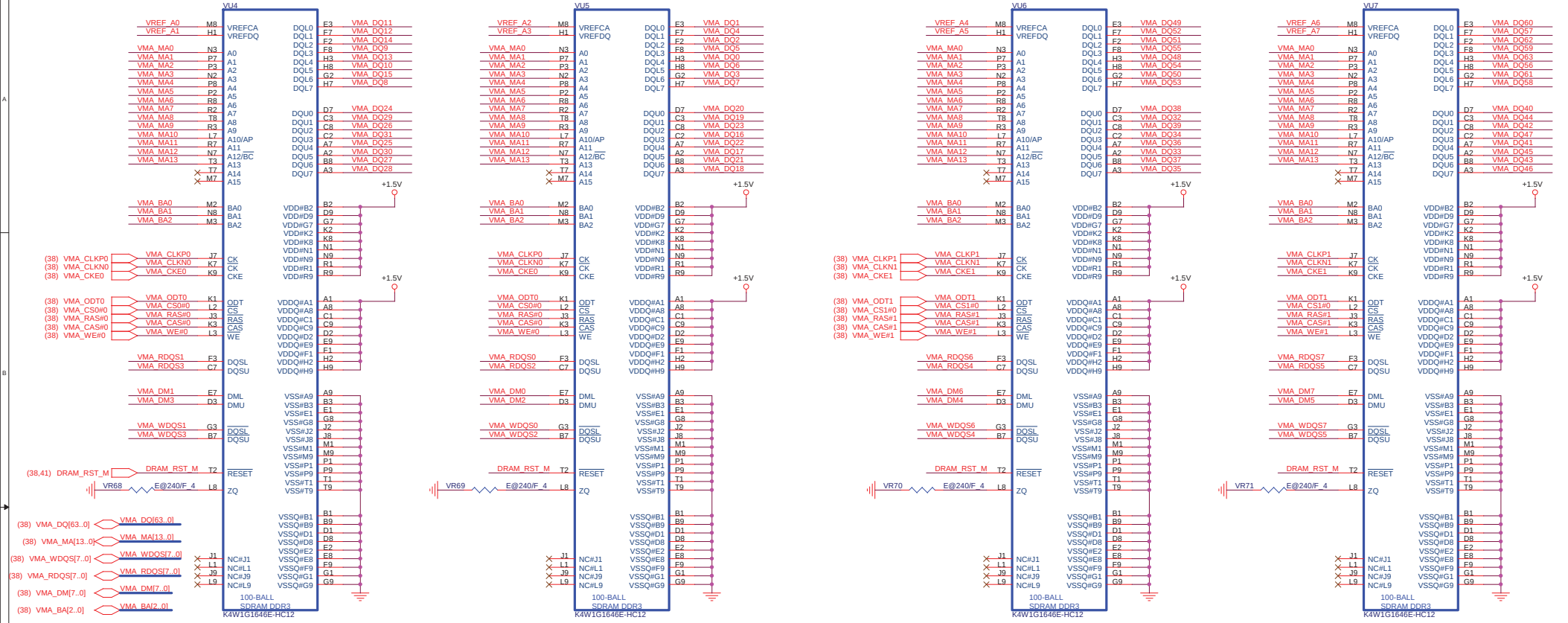
Quanta Computer Inc.
PROJECT :HK5

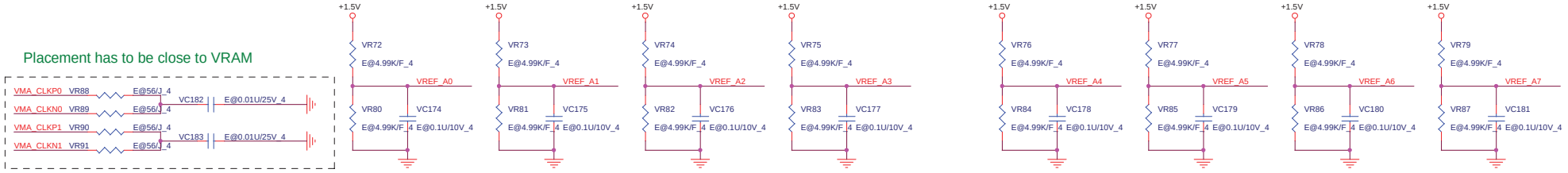
Size	Document Number	Rev
	Thames_POWER	1A

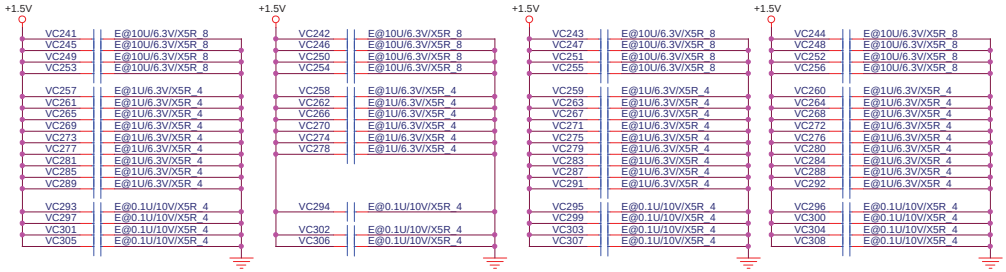
Date: Wednesday, February 01, 2012 Sheet 39 of 43

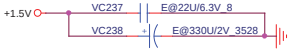
DDR3 64MX16, CH A : 512MB



Placement has to be close to VRAM





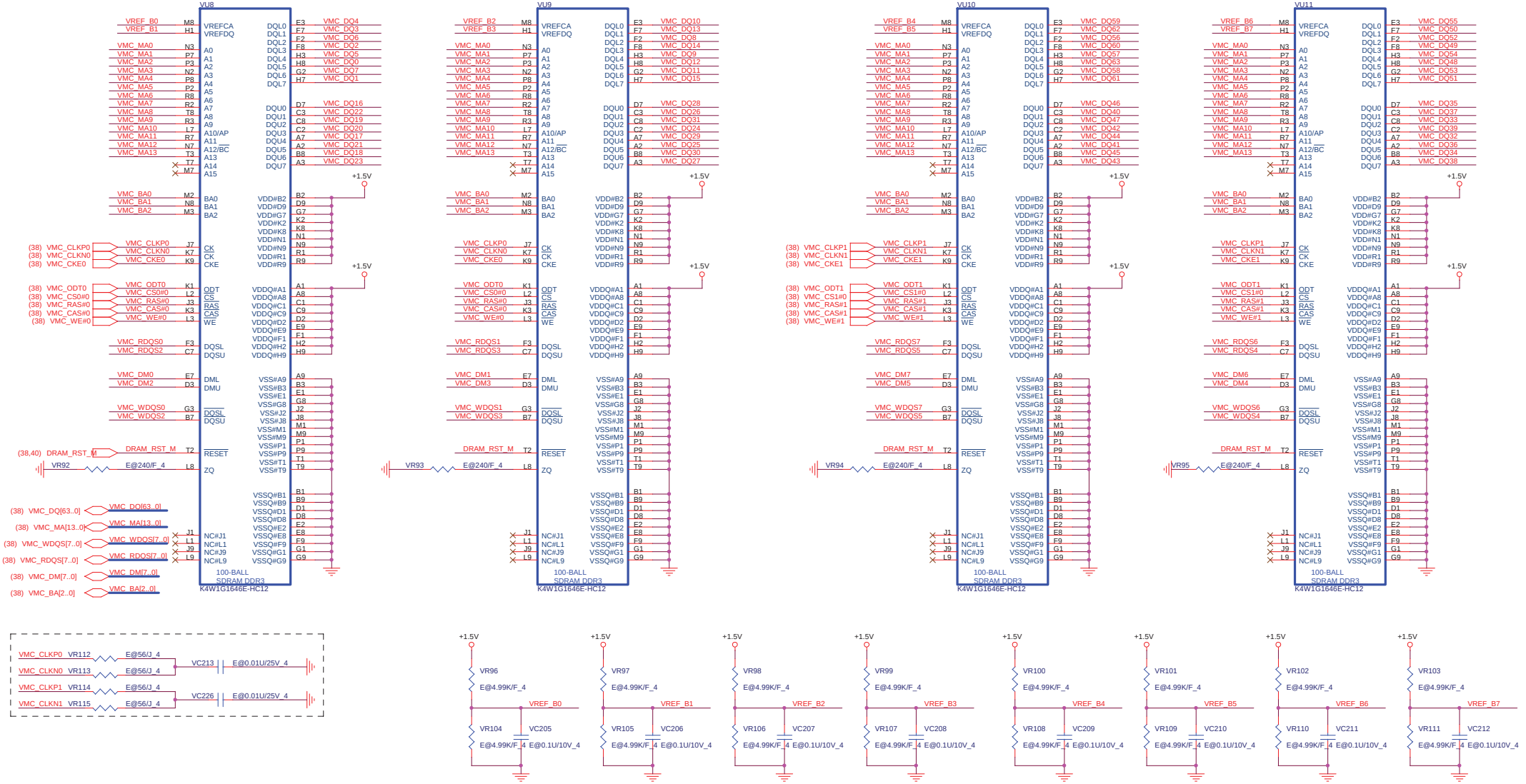


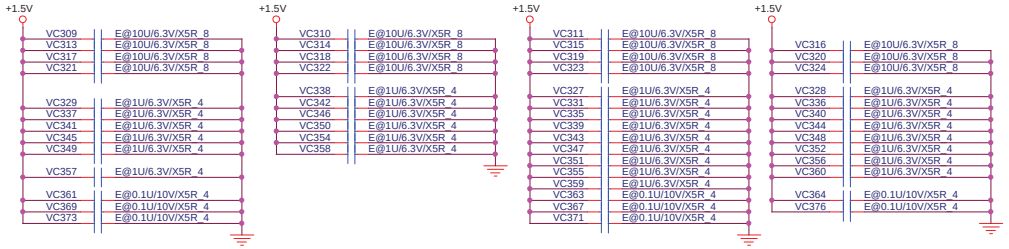
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT :HK5

Size	Document Number	Rev
	Thames_DDR3_A_512M	1A
Date:	Wednesday, February 01, 2012	Sheet 40 of 43

DDR3 64MX16, CH B : 512MB





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PROJECT :HK5

Size	Document Number	Rev
	Thames_DDR3_B_512M	1A
Date:	Wednesday, February 01, 2012	Sheet 41 of 43

WLAN PCH

42

H8 *H-C197D158P2
H-C197D158P2
H27 h-tc5_5bc4i3d3p2
H56 h-tc5_5bc4i3d3p2
H10 *O-HK1-3
H19 *HG-C236D102P2
H16 *O-HK1-3
H7 *O-HK1-12
H18 *o-hk5-1
H23 *O-HK1-5
H25 *O-HK1-6
H24 *O-HK1-7
H44 *HK1-F
H42 *HK1-D
H41 *HK1-C
H60 *h-tsbc207d157p2-1
H61 *h-tsbc207d157p2-2
H4 *O-HK1-11
H34 *HG-TSBSD102P2
H13 *O-HK1-17
H54 *HK1-N
H55 *H-C91D91N
H62 *h-tsbsd102p2-0
H9 *O-HK1-10
H11 *O-HK1-9
H15 *O-HK1-8
H26 *H-C197D158P2
H14 *O-HK1-16
H12 *O-HK1-15
H3 *H-C177D91PT
H2 *H-C177D91PT
H20 *O-HK1-14
H17 *O-HK1-13
H30 *SPAD-RE177X79
H32 *SPAD-RE177X79

KEY BOARD Connector

CON2
KB_ACS(88513-260N)
(16) MY15 (16) MY14 (16) MY13 (16) MY12 (16) MY11 (16) MX7 (16) MY10 (16) MX6 (16) MX5 (16) MY9 (16) MX4 (16) MY8 (16) MY7 (16) MY6 (16) MY5 (16) MY4 (16) MY3 (16) MX3 (16) MY2 (16) MY1 (16) MY0 (16) MX2 (16) MX1 (16) MX0 (16) MY17 (16) MY16
RP6 RP8 RP9 RP10 RP11 RP12 22X4
R164 22_4
R166 22_4
27
28
+3VPCU
MX0 R163 10K/J_4
MX1 R162 10K/J_4
MX2 R159 10K/J_4
MX3 R156 10K/J_4
MX4 R154 10K/J_4
MX5 R151 10K/J_4
MX6 R147 10K/J_4
MX7 R143 10K/J_4

VIN +1.5V
C550 1000P/50V/X7R/10%_4
C551 1000P/50V/X7R/10%_4
VIN +1.5V_SUS
C552 1000P/50V/X7R/10%_4
C553 1000P/50V/X7R/10%_4
C557 1000P/50V/X7R/10%_4
VIN +1.05V
C554 1000P/50V/X7R/10%_4
C556 1000P/50V/X7R/10%_4
C560 1000P/50V/X7R/10%_4
C561 1000P/50V/X7R/10%_4
+5V_WAKE C565 C566 C567 1000P/50V/X7R/10%_4 +1.05V
+5V C555 C558 C559 1000P/50V/X7R/10%_4
+1.05V C616 C617 C618 C619 1000P/50V/X7R/10%_4

VIN C585 C587 C588 0.1U/25V/X7R_6
C643 C644 C645 0.1U/25V/X7R_6
C646 1000P/50V/X7R/10%_4
C647 0.1U/25V/X7R_6
+3V_S5 C589 0.1U/10V/X5R_4
+5V C593 1000P/50V/X7R/10%_4 +5V_WAKE
+5V C595 C596 C597 1000P/50V/X7R/10%_4 USB_CHG
+1.05V C563 C620 C660 C661 C662 C663 C664 C665 C666 C667 C668 C669 0.1U/10V/X5R_4

+3V_S5 C601 C602 C603 1000P/50V/X7R/10%_4 +3V
+1.05V C605 C606 C607 1000P/50V/X7R/10%_4 +3V
+3V_S5 C612 1000P/50V/X7R/10%_4 USB_CHG
+1.05V C621 C622 1000P/50V/X7R/10%_4 +1.5V_SUS
+5V_WAKE C638 C639 C648 C649 C583 1000P/50V/X7R/10%_4 C640 C641 0.1U/10V/X5R_4

+VCC_CORE C613 C614 C615 1000P/50V/X7R/10%_4
+VCC_GFX C625 1000P/50V/X7R/10%_4
+1.5V_SUS C626 C671 C672 C673 1000P/50V/X7R/10%_4 +1.5V
+VGPU_CORE C630 1000P/50V/X7R/10%_4 +1.5V
+VGPU_CORE C631 C632 1000P/50V/X7R/10%_4
+1.5V C627 C633 C634 C635 C636 C637 1000P/50V/X7R/10%_4 0.1U/10V/X5R_4
+3V_WAKE C642 1000P/50V/X7R/10%_4

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Quanta Computer Inc.
PROJECT :HK5

Size	Document Number	Rev
	HOLE/EMI/KB	1A
Date: Wednesday, February 01, 2012	Sheet 42 of 43	

USB PORT Architecture	
PORT 0	USB3.0
PORT 1	USN2.0
PORT 2	USN2.0
PORT 3	USB2.0
PORT 4	N/A
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A
PORT 9	WiMax/BT
PORT 10	Camera
PORT 11	N/A
PORT 12	N/A
PORT 13	N/A

PCIE BUS	
PORT 1	WLAN Port
PORT 2	CARD READER
PORT 3	GLAN(RTL8111E)
PORT 4	N/A
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A

SATA BUS	
PORT 0	HDD
PORT 1	N/A
PORT 2	N/A
PORT 3	N/A
PORT 4	ODD
PORT 5	N/A

SM BUS	MBCLK/MBDATA	WRITE	READ	Function
ISL88731CHRTZ	0001 001X	0001 0010	0001 0011	Charger
AMD Thames	0100 0001	-	0100 0001	Graphice
LIS331DL	0011 101X	0011 1010	0011 1011	G Sensor

SM BUS	MBCLK_BAT/MBDATA_BAT	WRITE	READ	Function
VGP-BPS26	0001 011X	0001 0110	0001 0111	Battery

SM BUS	SMB_PCH_CLK/SMB_PCH_DAT	WRITE	READ	Function
DIMM Module0	1010 000X	1010 0000	1010 0001	DDRIII
DIMM Module 1	1010 010X	1010 0100	1010 0101	DDRIII
Synaptics	0010 110X	0010 1100	0010 1101	Click PAD

R363(High) R362(Low) / R294(High) R297(low)

	Board ID3	Board ID0
14"/HK6	0	0
15"/HK5	0	1
17"/HK7	1	0

Board ID1 (VRAM Vendor)	Samaung(1)	Hynix(0)
R47(High)	Stuff	No Stuff
R48(Low)	No Stuff	Stuff

Board ID2		
14" 4PCS	1G	512M
15" 8PCS	1G	2G
R39(High)	Stuff	No Stuff
R27(Low)	No Stuff	Stuff

PCBA SKU	Discrete	UMA
R277(Pull High)	Stuff	No Stuff
R275(Pull Low)	No Stuff	Stuff

	S0	S3	DS3	S4	S5 (Charger Enable)	S5 (Charger Disable)
RUN_ON	H	L	L	L	L	L
+3V	H	L	L	L	L	L
+5V	H	L	L	L	L	L
+0.75V_DDR_VTT	H	L	L	L	L	L
+1.05V	H	L	L	L	L	L
+0.85V	H	L	L	L	L	L
+1.5V	H	L	L	L	L	L
+1.8V	H	L	L	L	L	L
+1.8V_GPU	H	L	L	L	L	L
+1.0V_GPU	H	L	L	L	L	L
+VGPU_CORE	H	L	L	L	L	L
+VCC_GFX	H	L	L	L	L	L
+VCC_CORE	H	L	L	L	L	L
SUS_ON	H	H	H	L	L	L
+1.5V_SUS	H	H	H	L	L	L
S5_ON	H	H	L	H	L	L
+5V_S5	H	H	L	H	L	L
+3V_S5	H	H	L	H	L	L
EC_WAKE_ON	H	H	H	H	H	L
+3V_WAKE	H	H	H	H	H	L
+5V_WAKE	H	H	H	H	H	L
DEEP_EC_EN	H	H	H	H	L	L
+3V_S5_DSW	H	H	H	H	L	L
+3V_SUS	H	H	L	L	L	L