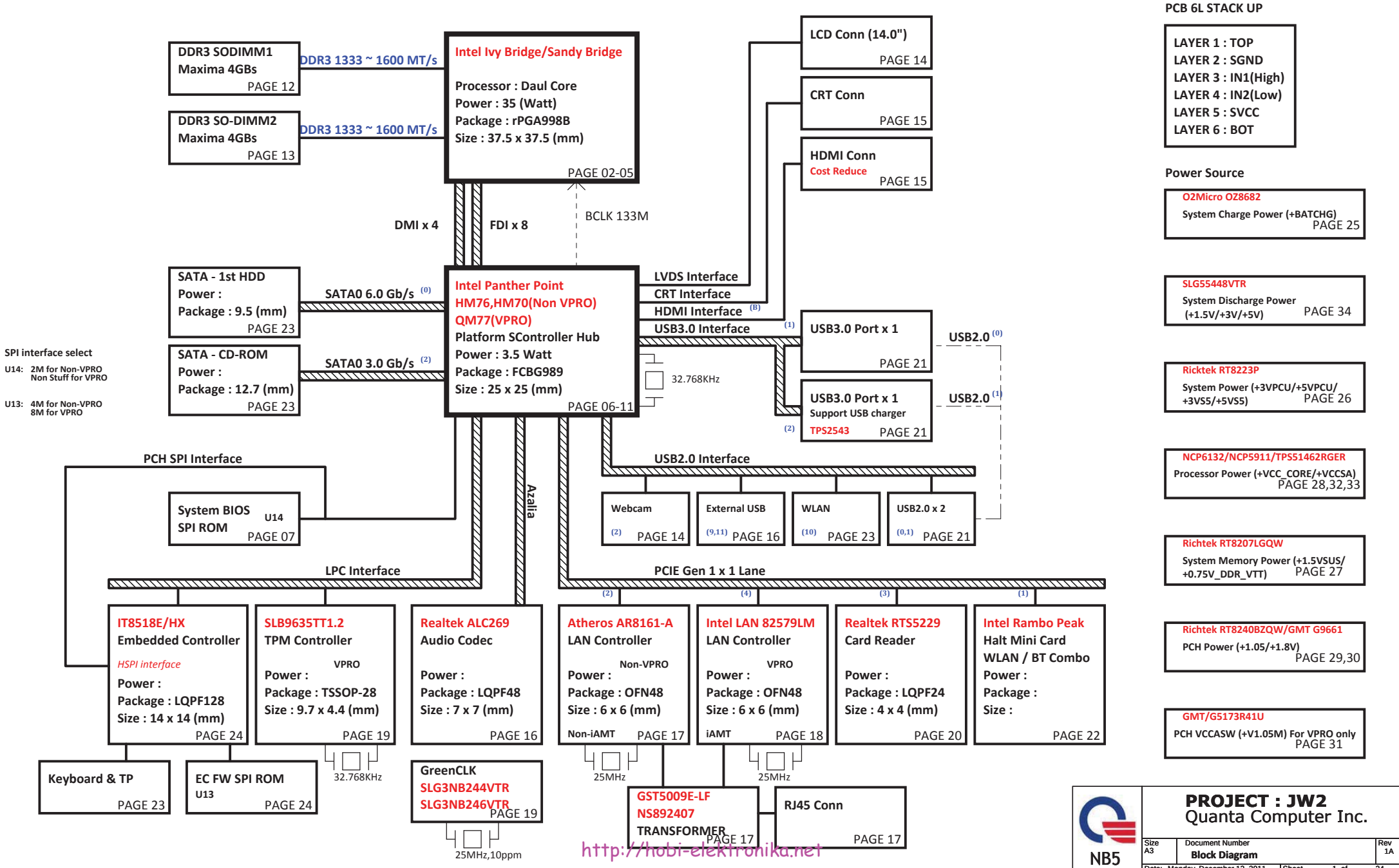
# JW2 UMA (14.0") Intel Chief River Block Diagram

01




PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

O2Micro OZ8682
System Charge Power (+BATCHG) PAGE 25

SLG55448VTR
System Discharge Power (+1.5V/+3V/+5V) PAGE 34

Ricktek RT8223P
System Power (+3VPCU/+5VPCU/ +3VS5/+5VS5) PAGE 26

NCP6132/NCP5911/TPS51462RGER
Processor Power (+VCC_CORE/+VCCSA) PAGE 28,32,33

Richtek RT8207LGQW
System Memory Power (+1.5VSUS/ +0.75V_DDR_VTT) PAGE 27

Richtek RT8240BZQW/GMT G9661
PCH Power (+1.05/+1.8V) PAGE 29,30

GMT/G5173R41U
PCH VCCASW (+V1.05M) For VPRO only PAGE 31



NB5

**PROJECT : JW2**
Quanta Computer Inc.

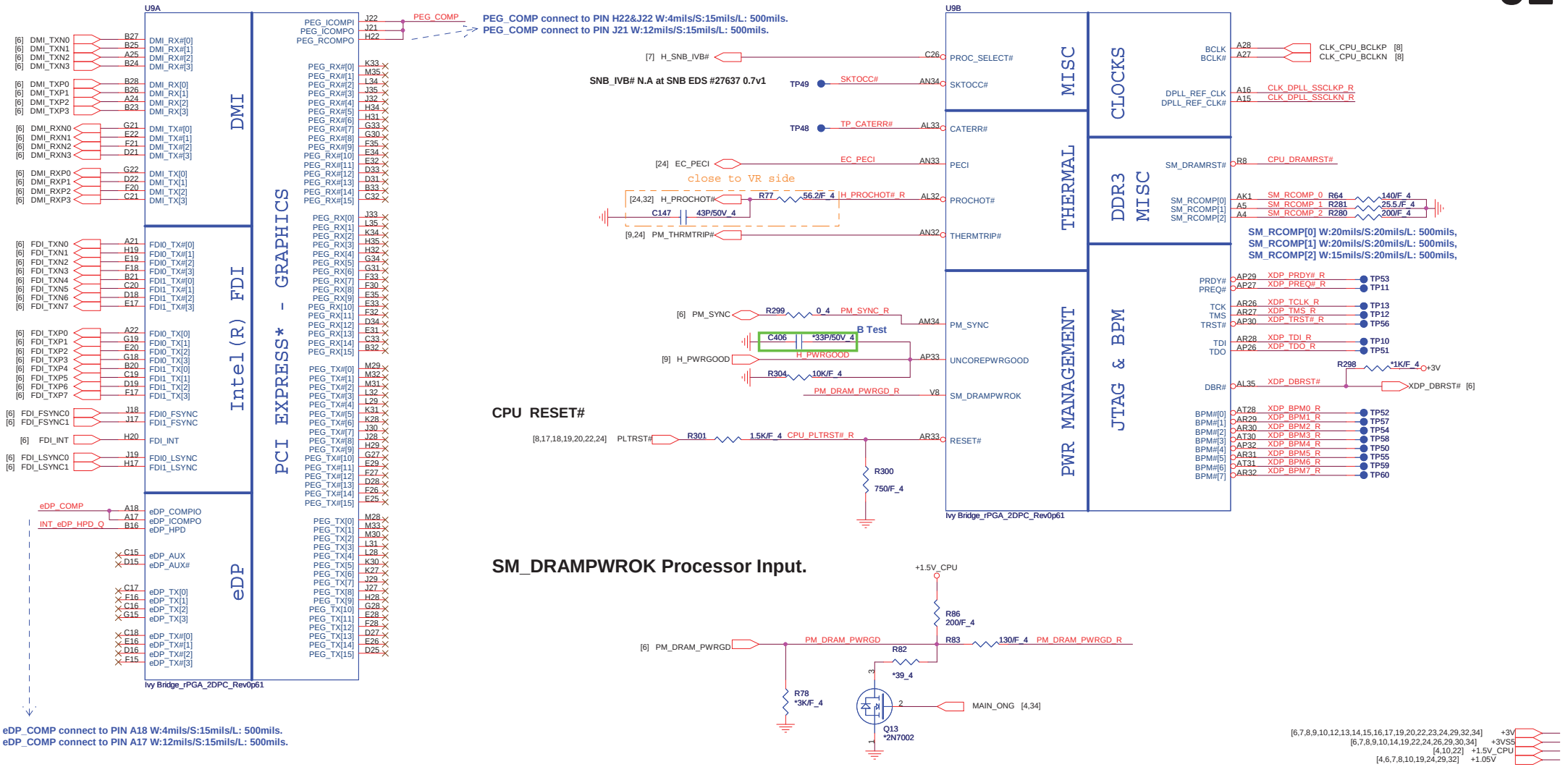
| Size | Document Number | Rev |
|---|---|---|
| A3 | Block Diagram | 1A |

Date: Monday, December 12, 2011 Sheet 1 of 34

# Ivy Bridge Processor (DMI,PEG,FDI)

# Ivy Bridge Processor (CLK,MISC,JTAG)

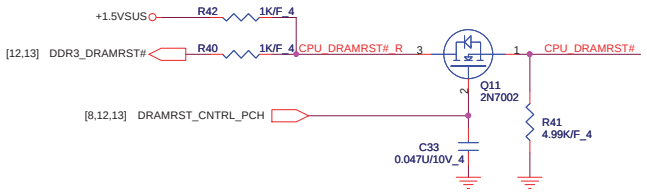
02




## FDI disable (DIS only stuff)

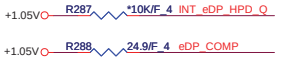
FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

## DDR3 DRAM RESET




## Embedded Display PLL Clock

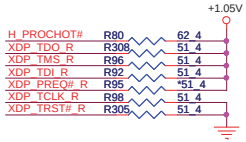

## DP & PEG Compensation




eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms


PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

## Processor pull-up (CPU)



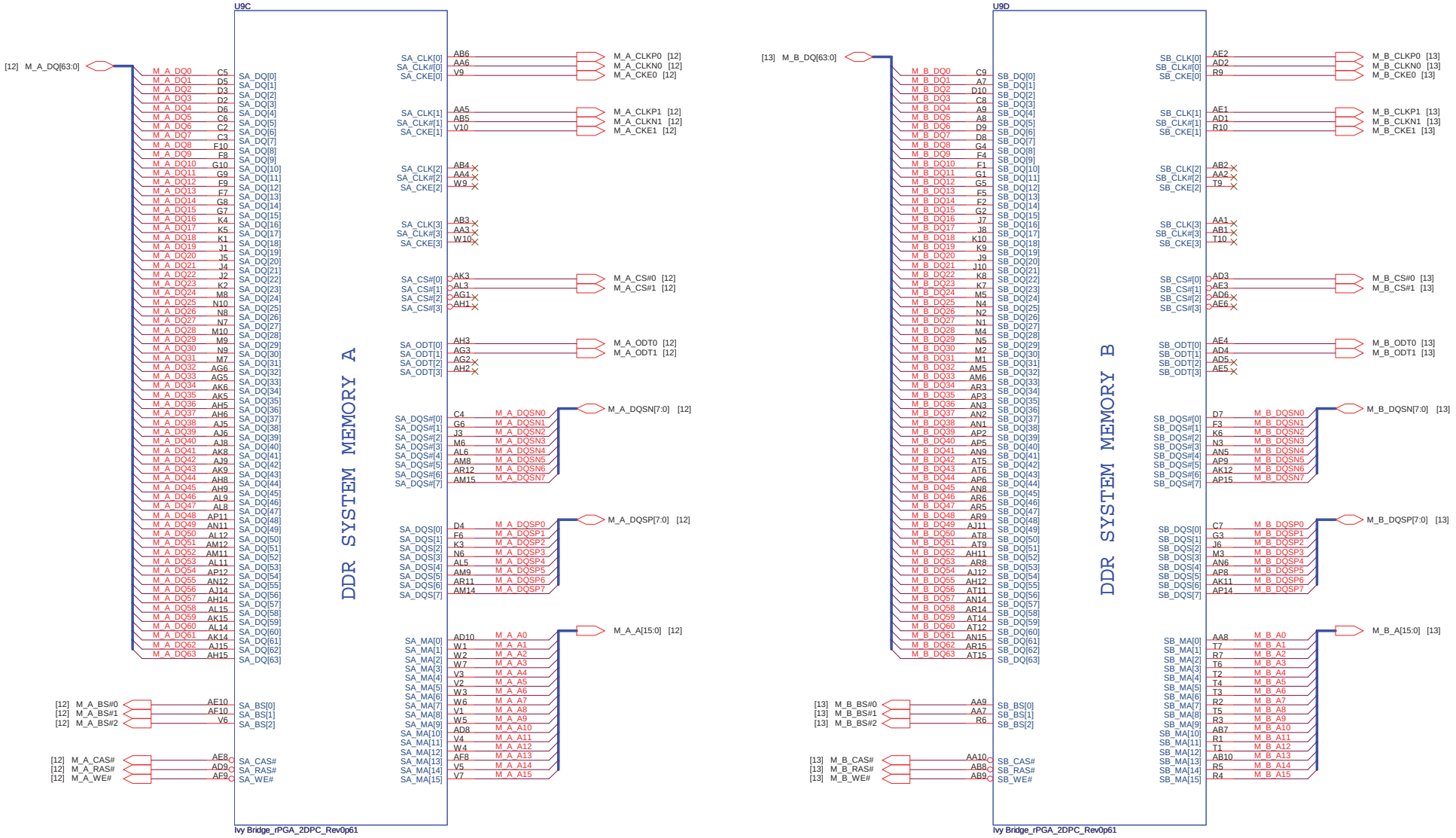

NB5

**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Processor 1/4 (Host/GPU) | 1A |
| Date: Tuesday, February 07, 2012 | Sheet 2 of 34 | |

# Ivy Bridge Processor (DDR3)






NB5

**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Processor 2/4 (Memory) | 1A |

Date: Tuesday, February 07, 2012 | Sheet 3 of 34

# Ivy Bridge Processor

04

## POWER

U9F

SNB: 55A
IVY: 55A

+VCC_CORE

C387 22U/6.3VS_8 C395 22U/6.3VS_8 C31 22U/6.3VS_8
C371 22U/6.3VS_8 C370 22U/6.3VS_8 C369 22U/6.3VS_8
C385 22U/6.3VS_8 C39 22U/6.3VS_8 C113 22U/6.3VS_8
C131 22U/6.3VS_8 C54 22U/6.3VS_8 C382 22U/6.3VS_8
C57 22U/6.3VS_8 C394 *22U/6.3VS_8 C69 22U/6.3VS_8
C400 22U/6.3VS_8 C80 22U/6.3VS_8 C126 22U/6.3VS_8
C94 22U/6.3VS_8 C50 22U/6.3VS_8 C399 22U/6.3VS_8
C30 *22U/6.3VS_8 C389 *22U/6.3VS_8 C95 22U/6.3VS_8
C388 22U/6.3VS_8 C61 22U/6.3VS_8 C390 22U/6.3VS_8
C45 22U/6.3VS_8 C401 22U/6.3VS_8 C32 *22U/6.3VS_8

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

### CORE SUPPLY

### PEG AND DDR

SNB: 8.5A
IVY: 8.5A

+1.05V

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

C62 22U/6.3VS_8 C64 22U/6.3VS_8 C383 22U/6.3VS_8
C107 22U/6.3VS_8 C65 22U/6.3VS_8 C130 22U/6.3VS_8
C63 *22U/6.3VS_8 C78 22U/6.3VS_8 C393 22U/6.3VS_8
C398 *22U/6.3VS_8 C66 22U/6.3VS_8 C53 *22U/6.3VS_8
C375 22U/6.3VS_8 C51 *22U/6.3VS_8 C122 *22U/6.3VS_8
C376 *22U/6.3VS_8 C386 22U/6.3VS_8 C88 *22U/6.3VS_8
C392 *22U/6.3VS_8 C391 22U/6.3VS_8 C46 22U/6.3VS_8

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

### SVID

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 VR_SVID_CLK
VIDSOUT AJ28 VR_SVID_DATA

### SENSE LINES

VCC_SENSE AJ35
VSS_SENSE AJ34
VCCIO_SENSE B10
VSS_SENSE_VCCIO A10

R63 100_4 +VCC_CORE
R65 100_4
VCC_SENSE [32]
VSS_SENSE [32]
VCCP_SENSE [29]
VSSP_SENSE [29]

Trace Route to Power IC area.

+1.05V
VCCP_SENSE R283 10/F_4
VSSP_SENSE R282 10/F_4

[7,10,30] +1.8V
[28] +VCCSA
[2,12,13,27] +1.5VSUS
[33] +VCC_GFX
[2,10,22] +1.5V_CPU
[2,6,7,8,10,19,24,29,32] +1.05V
[33] +VCC_CORE

Ivy Bridge_rPGA_2DPC_Rev0p61

## POWER

U9G

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

SNB: 21.5A
IVY: 38A

+VCC_GFX

C397 22U/6.3VS_8 C100 22U/6.3VS_8
C125 22U/6.3VS_8 C133 22U/6.3VS_8
C124 22U/6.3VS_8 C155 22U/6.3VS_8
C132 22U/6.3VS_8 C99 22U/6.3VS_8
C152 22U/6.3VS_8 C102 22U/6.3VS_8
C101 22U/6.3VS_8 C396 22U/6.3VS_8

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

### GRAPHICS

### SENSE LINES

VAXG_SENSE AK35
VSSAXG_SENSE AK34

R295 100/F_4 +VCC_GFX
R296 100/F_4
VCC_AXG_SENSE [32]
VSS_AXG_SENSE [32]

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

### VREF

SM_VREF AL1

+VDDR_REF_CPU
Q12 2N7002
R66 100K/F_4
DDR_VTTREF [12,13,27]
MAIND [34]

SA_DIMM_VREFDQ B4
SB_DIMM_VREFDQ D1

SMDDR_VREF_DQ0_M3 [12]
SMDDR_VREF_DQ1_M3 [13]

R279 *1K/F_4 R278 *1K/F_4

### DDR3 -1.5V RAILS

VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

SNB: 5A
IVY: 5A

+1.5V_CPU

C129 10U/6.3VS_6 C121 10U/6.3V_8 C110 10U/6.3VS_6 C139 10U/6.3VS_6

330uF x1, 10uF_8 x6 Socket BOT edge.

C142 10U/6.3VS_6 C138 10U/6.3VS_6 C407 *100U 16V/6.3*5.8

### SA RAIL

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

SNB: 6A
IVY: 6A

+VCCSA

C377 10U/6.3V_8 C349 10U/6.3V_8 C42 10U/6.3V_8 C348 *10U/6.3V_8

330uF x1, 10uF_8 x1 Socket BOT edge,
10uF_8 x2 Socket BOT cavity.

### 1.8V RAIL

+1.8V

SNB: 1.5A
IVY: 1.5A

C26 10U/6.3V_8 C27 10U/6.3V_4 C28 1U/6.3V_4 C25 *330U/2V_7343

VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

330uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.

### MISC

VCCSA_SENSE H23 VCCUSA_SENSE_R R286 0_4 VCCUSA_SENSE [28]
VCCSA_VID[0] C22 R290 10K/F_4 VCCSA_SEL0 [28]
VCCSA_VID[1] C24 VCCSA_SEL [28]
R291 10K/F_4
VCCIO_SEL A19 R289 0_4 H_VTTVID1 [29]

Ivy Bridge_rPGA_2DPC_Rev0p61

Layout note: need routing together and ALERT need between CLK and DATA.

### SVID CLK

Place PU resistor close to VR
R75 *54.9/F_4 +1.05V
VR_SVID_CLK
VR_SVID_CLK [32]

### SVID DATA

+1.05V
Place PU resistor close to CPU
R68 130/F_4
VR_SVID_DATA
B Test
Del R67
VR_SVID_DATA [32]

### SVID ALERT

Place PU resistor close to CPU
+1.05V R74 75/F_4
H_CPU_SVIDALRT# R72 43_4
VR_SVID_ALERT# [32]

+1.5VSUS
+1.5V_CPU
+1.5VSUS
Q23 QM3002N3
R105 220_8
C75 0.1U/10V_4
C83 0.1U/10V_4
C92 0.1U/10V_4
C68 0.1U/10V_4
Placement close to CPU.
MAIND
C145 *470P/50V_4
Q14 2N7002
MAIN_ONG [2,34]

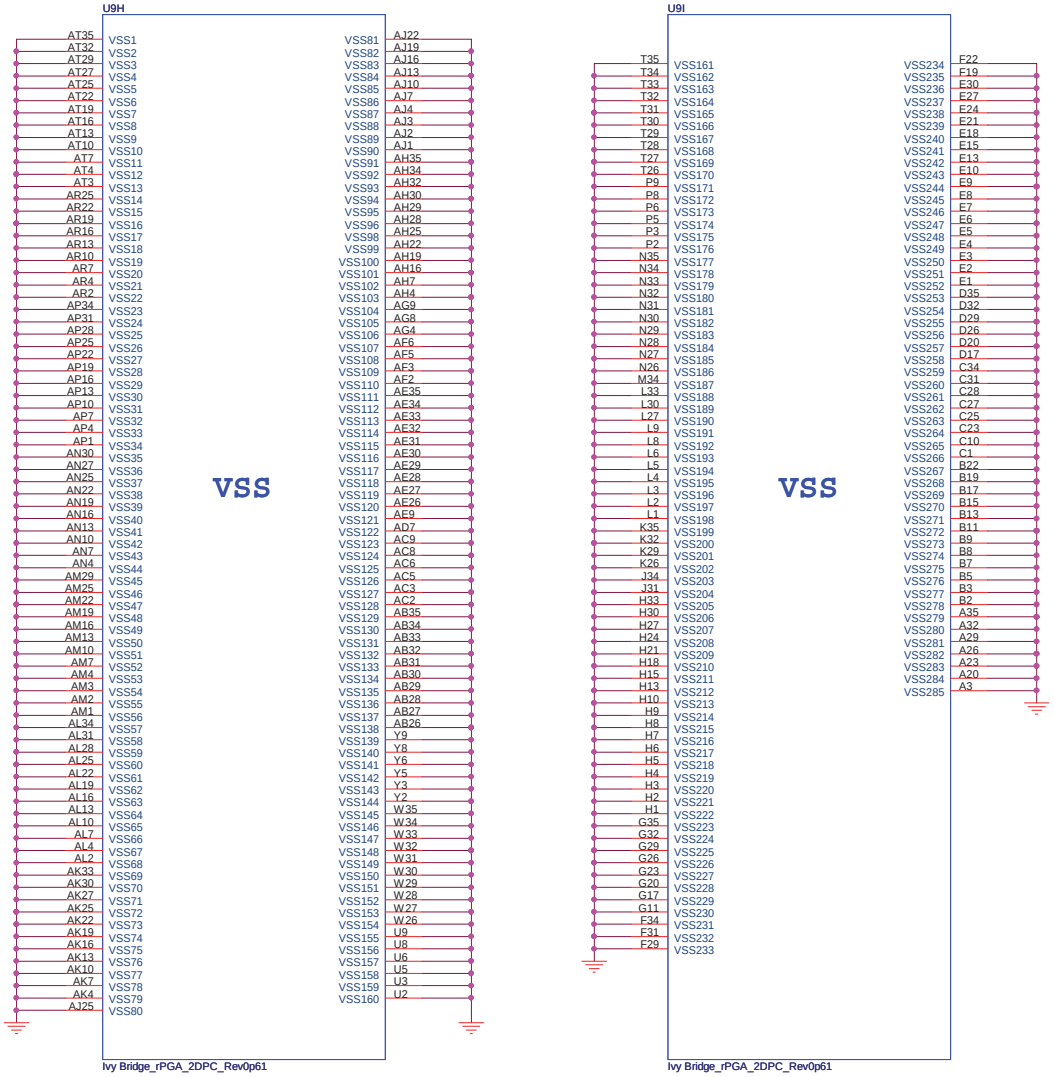
### CPU VDDQ

NB5

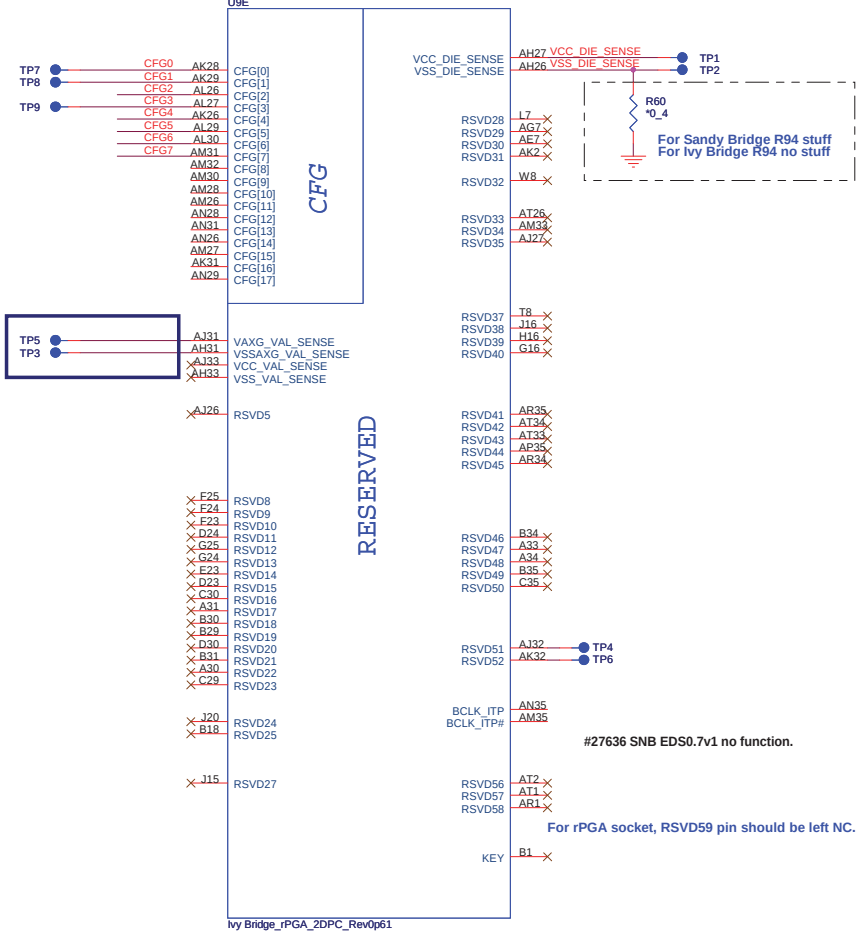
PROJECT : JW2
Quanta Computer Inc.

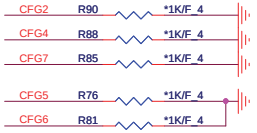
| Size | Document Number | Rev |
|---|---|---|
| Custom | Processor 3/4 (Power) | 1A |
| Date: Tuesday, February 07, 2012 | Sheet 4 of 34 | |

# Ivy Bridge Processor (GND)




# Ivy Bridge Processor (RESERVED, CFG)




## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

| | 1 | 0 |
|---|---|---|
| CFG2<br>(PEG Static Lane Reversal) | Normal Operation | Lane Reversed |
| CFG4<br>(DP Presence Strap) | Disable; No physical DP attached to eDP | Enable; An ext DP device is connected to eDP |
| CFG7<br>(PEG Defer Training) | PEG train immediately following xxRESETB de assertion | PEG wait for BIOS training |

**CFG[6:5] (PCIE Port Bifurcation Straps)**

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

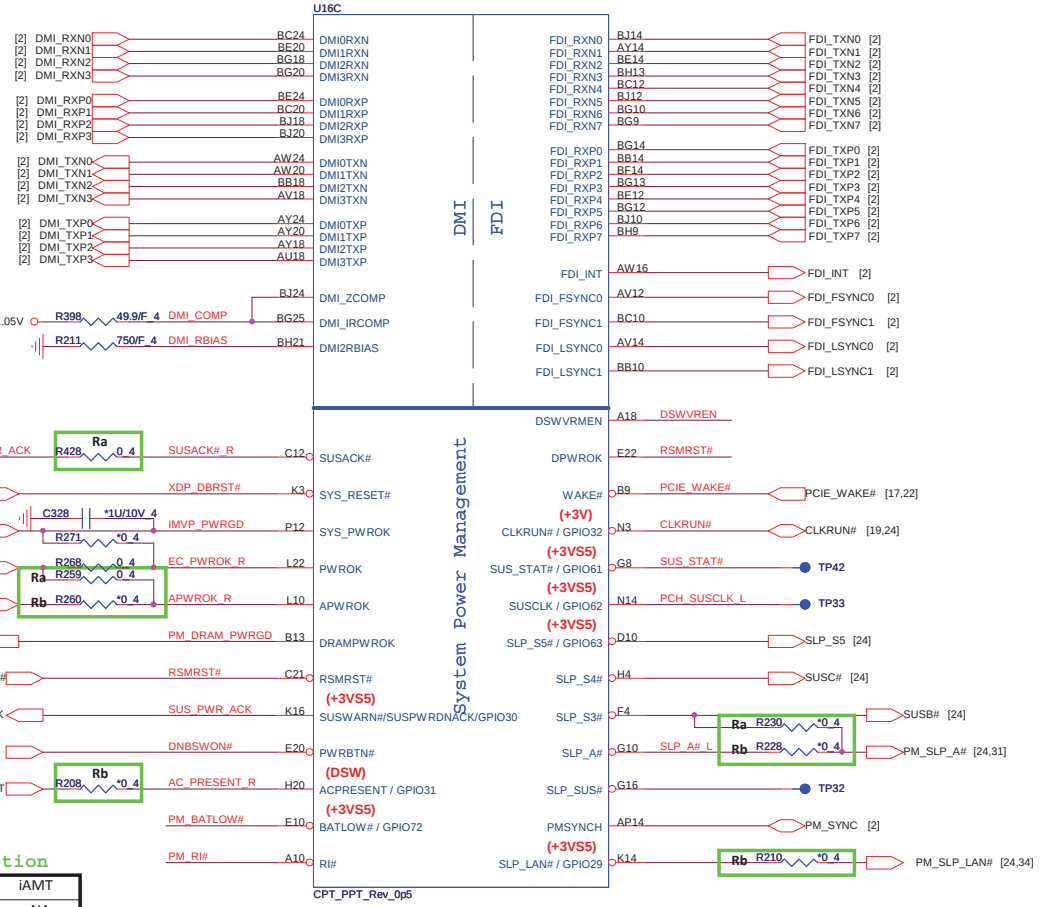
NB5

**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Processor 4/4 (Ground) | 1A |

Date: Thursday, December 08, 2011 | Sheet 5 of 34

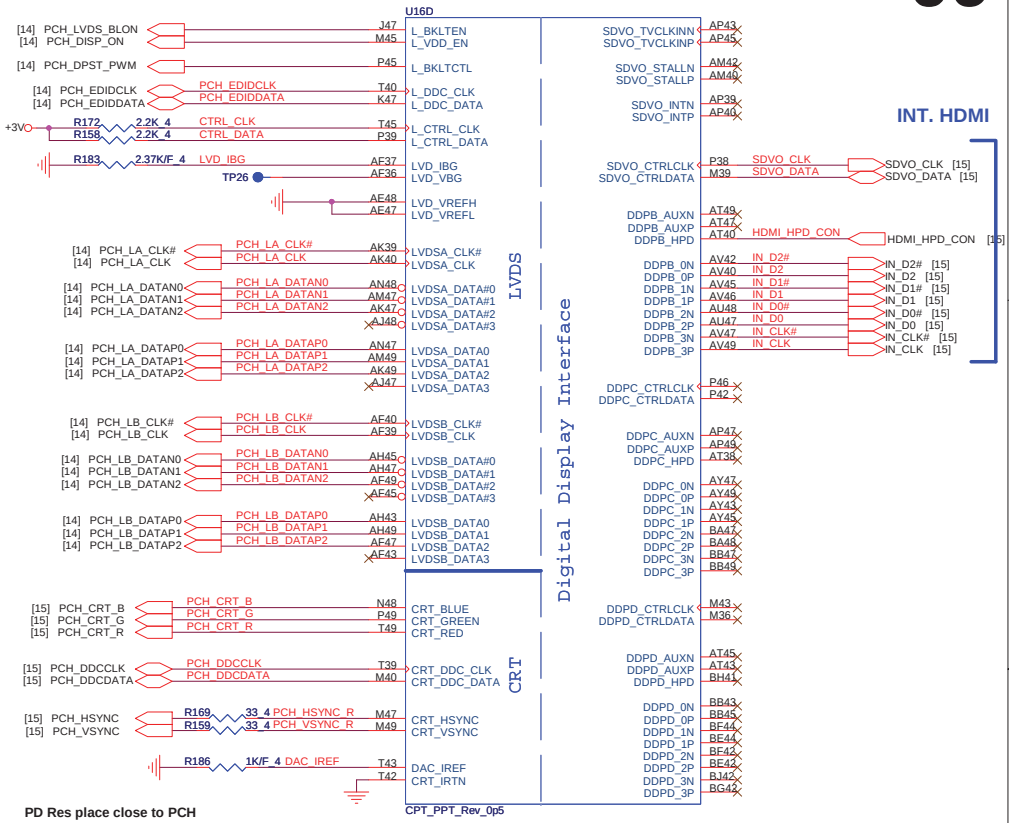
# Cougar Point/Panther Point (DMI,FDI,PM)




FOR iAMT option

| | Non-iAMT | iAMT |
|---|---|---|
| Ra | Stuff | NA |
| Rb | NA | Stuff |

# Cougar Point/Panther Point (LVDS,DDI)

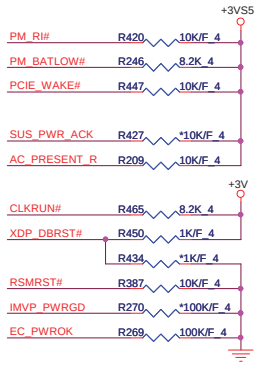



INT. HDMI

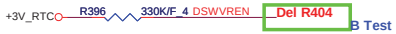
PD Res place close to PCH

PCH to Res routeing 50 ohm Impedance.
Res to connector filter routeing 37.5ohm Impedance.


## PCH Pull-high/low(CLG)




## System PWR_OK(CLG)




B Test

| On Die DSW VR Enable |
|---|
| High = Enable (Default)<br>Low = Disable |

[2,7,8,9,10,12,13,14,15,16,17,19,20,22,23,24,29,32,34] +3V
[7,10,14,15,16,22,23,34] +5V
[7,8,9,10,14,19,22,24,26,29,30,34] +3VS5
[2,4,7,8,10,19,24,29,32] +1.05V
[7,10,19] +3V_RTC

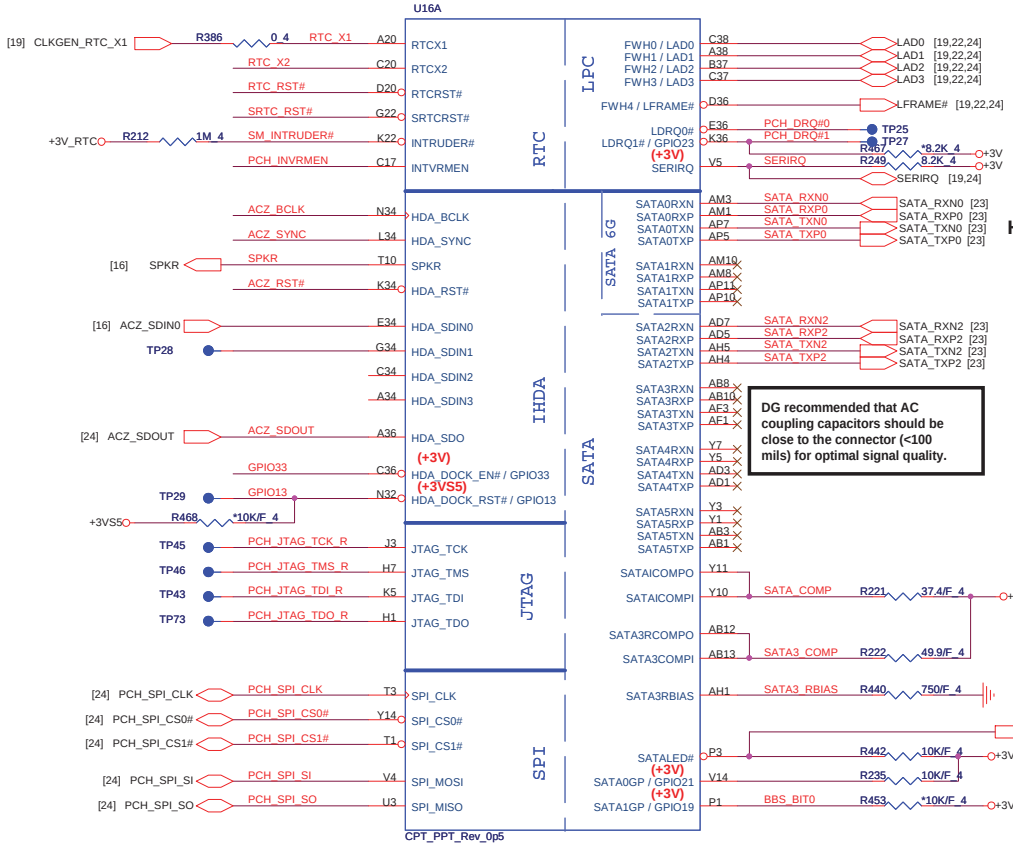
NB5

**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 1/6 (Host/Display) | 1A |

Date: Tuesday, February 07, 2012 Sheet 6 of 34

# Cougar Point/Panther Point (HDA,JTAG,SATA)




HDD (SATA3 6.0 Gb/s)

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

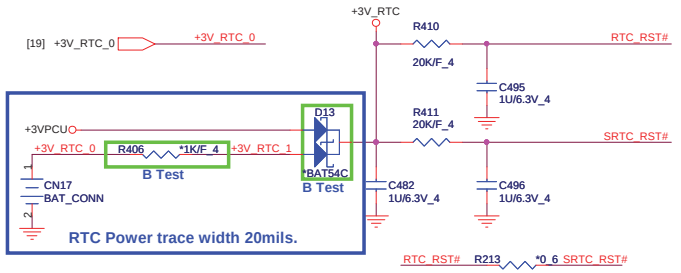
## PCH Strap Table

| Pin Name | Strap description | Sampled | Configuration | Circuit |
|---|---|---|---|---|
| SPKR Different from Calpella | No reboot mode setting | PWROK | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode | SPKR R238 *1K/F_4 +3V |
| GNT3# / GPIO55 | Top-Block Swap Override | PWROK | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 20K) | +3V R339 *1K/F_4 R348 10K/F_4 PCI_GNT3# [8] |
| INTVRMEN | Integrated 1.05V VRM enable | ALWAYS | Should be always pull-up | PCH_INVRMEN R395 330K/F_4 +3V_RTC |
| HDA_DOCK_EN#/GPIO33 | Flash Descriptor Security Only for Interposer | PWROK | 0 = Override<br>1 = Default (weak pull-up 20K) | GPIO33 R383 *1K/F_4 ACZ_SDOUT |
| GNT1# / GPIO51 | Boot BIOS Selection 1 [bit-1] | PWROK | GNT1# 1 0 / GNT0# 1 0 / Boot Location SPI LPC | [Need external pull-down for LPC BIOS]<br>Default weak pull-up on GNT0/1#<br>R437 *1K/F_4 BBS_BIT0<br>R344 *1K/F_4 BBS_BIT1 [8] |
| GPIO19 Different from Calpella | Boot BIOS Selection 0 [bit-0] | PWROK | | |
| GNT2# / GPIO53 | ESI strap (Server only) | PWROK | Should not be pull-down (weak pull-up 20K) | USE GPIO PIN |
| NV_ALE | Intel Anti-Theft HDD protection Only for Interposer | PWROK | 0 = Disable (Internal pull-down 20kohm) | +1.8V R232 *1K/F_4 NV_ALE [8] |
| NV_CLE | DMI Termination voltage | PWROK | weak pull-down 20kohm | +1.8V R426 2.2K_4 R425 1K/F_4 NV_CLE [9] H_SNB_IVB# [2] sandy/ivy bridge |
| HDA_SYNC | On-Die PLL VR Voltage Select | RSMRST | 0 = Support by 1.8V (weak pull-down)<br>1 = Support by 1.5V | +3VS5 R354 1K/F_4 ACZ_SYNC |
| HDA_SDO | Flash Descriptor Security | PWROK | 0 = Override<br>1 = Default (weak pull-up 20K) | ACZ_SDOUT R382 *1K/F_4 +3VS5 |
| GPIO8 | Integrated Clock Chip Enable | RSMRST# | Should be pull-down (weak pull-up 20K) | R446 *1K/F_4 ICC_EN# [9] |
| GPIO28 Different from Calpella | On-die PLL Voltage Regulator | RSMRST# | 0 = Disable<br>1 = Enable (Default) | R265 *1K/F_4 PLL_ODVR_EN [9] |
| SPI_MOSI | iTPM function Disable | APWROK | 0 = Default (weak pull-down 20K)<br>1 = Enable | PCH_SPI_SI R438 *1K/F_4 +3V |

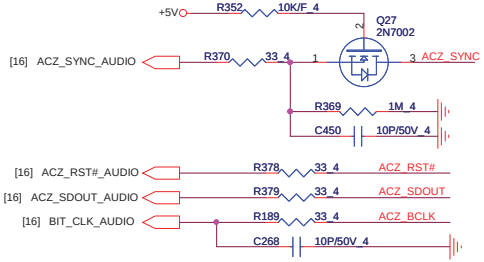
+3V [2,6,8,9,10,12,13,14,15,16,17,19,20,22,23,24,29,32,34]
+5V [10,14,15,16,22,23,34]
+1.8V [4,10,30]
+1.05V [2,4,6,8,10,19,24,29,32]
+3VS5 [6,8,9,10,14,19,22,24,26,29,30,34]
+3VPCU [14,19,22,23,24,25,26]
+3V_RTC [6,10,19]

07

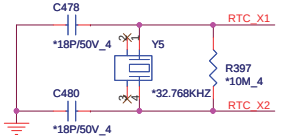
## RTC Circuitry(RTC)




## HDA Bus(CLG)

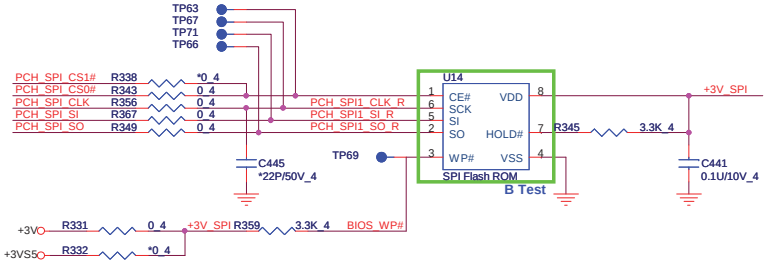



## RTC Clock 32.768KHz




## PCH SPI ROM(CLG)

| Vender | Size | P/N |
|---|---|---|
| EON | 2MB | AKE38ZN0Q00 (EN25QH16-104HIP |
| AMIC | 2MB | AKE38ZN0802 (A25LQ16M-F/Q) |
| Socket | | DFHS08FS023 |



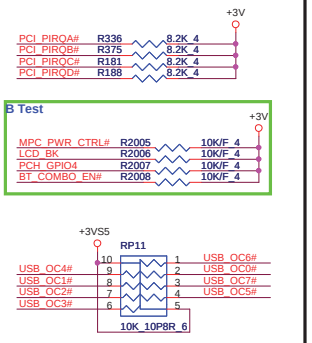

| | | | |
|---|---|---|---|
| NB5 | PROJECT : JW2<br>Quanta Computer Inc. | | |
| | Size: Custom | Document Number: PCH 2/6 (HDA/RTC/SATA/SPI) | Rev: 1A |
| | Date: Tuesday, February 07, 2012 | Sheet 7 of 34 | |

# Cougar Point-M/Panther Point (PCI,USB,NVRAM)

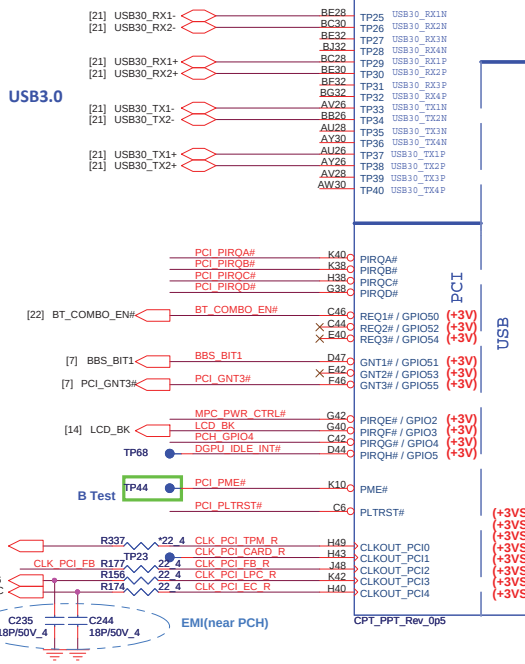
# Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)

08

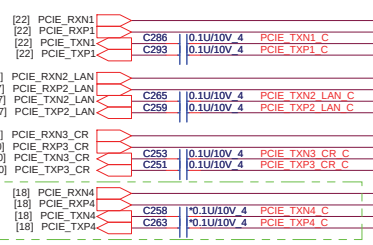
## PCI/USBOC# Pull-up(CLG)



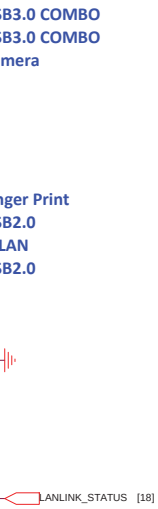

## USB3.0



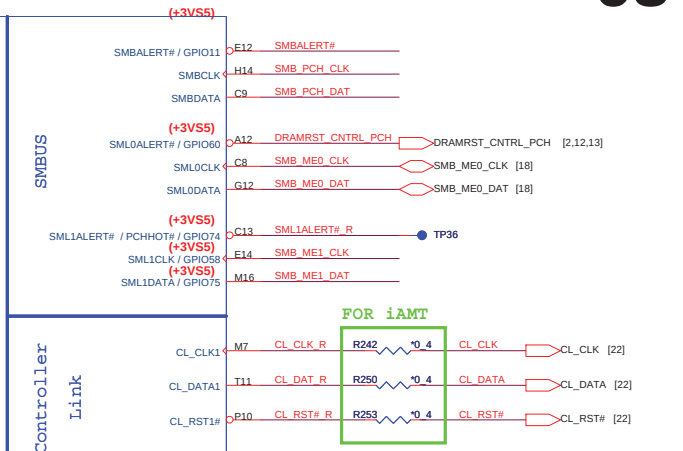

## WLAN / LAN / Cardreader / vPro



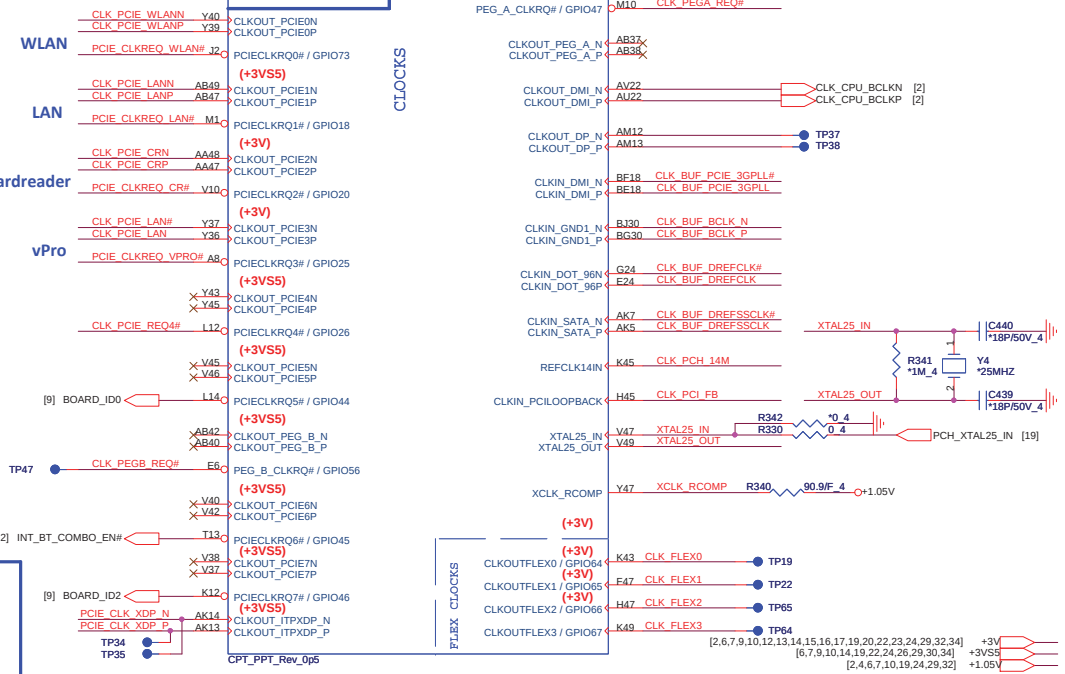

## USB3.0 COMBO / Finger Print / USB2.0 / WLAN / Camera




## SMBUS / Controller Link




## CLOCKS

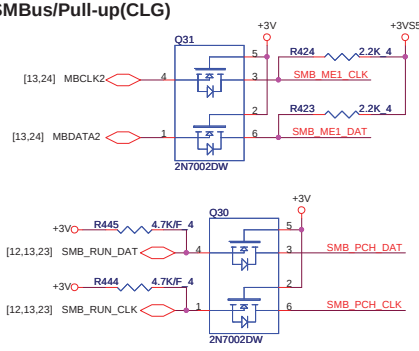



## MPC Switch Control

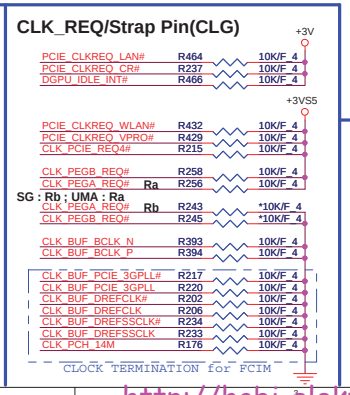
| | |
|---|---|
| MPC_PWR_CTRL# | Low = MPC ON<br>High = MPC OFF (Default) |

MPC_PWR_CTRL# R353 *1K/F_4

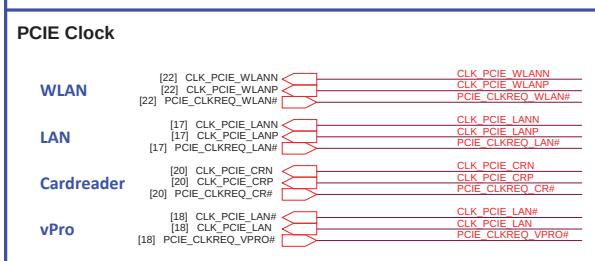
## SMBus/Pull-up(CLG)



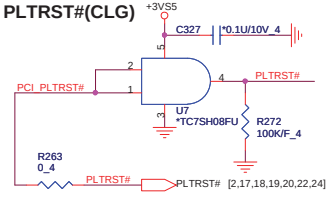

## CLK_REQ/Strap Pin(CLG)



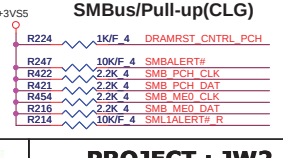

## PCIE Clock




## PLTRST#(CLG)




## SMBus/Pull-up(CLG)



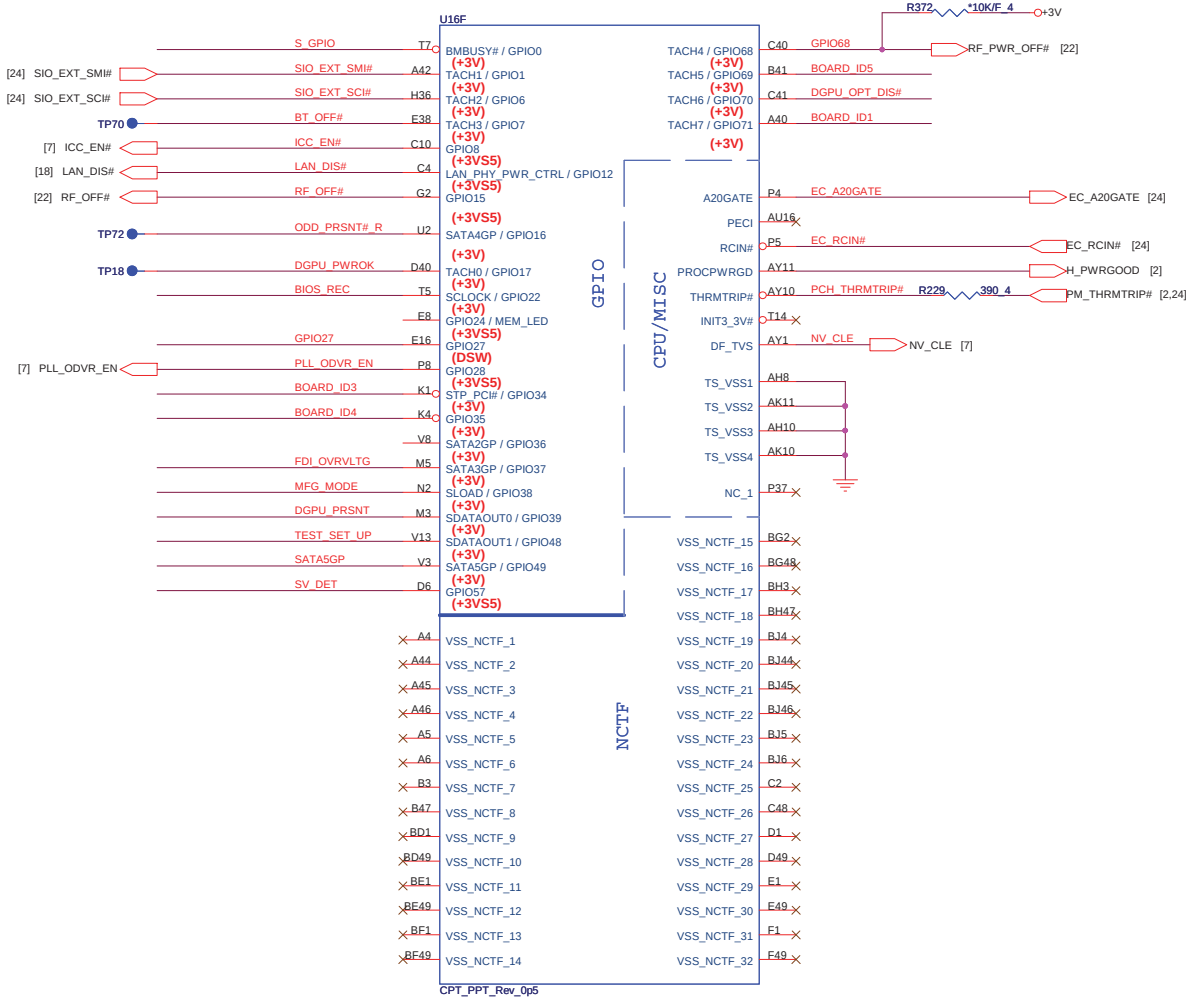

NB5

**PROJECT : JW2**
Quanta Computer Inc.

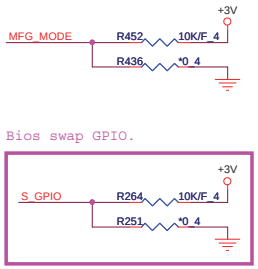
| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 3/6 (Clock/PCI/PCIE/USB) | 1A |
| Date: Tuesday, February 07, 2012 | Sheet 8 of 34 | |

# Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

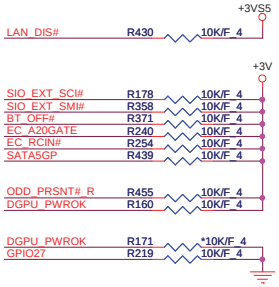
09

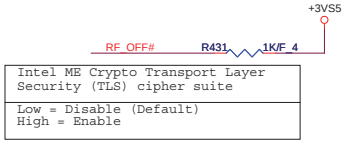


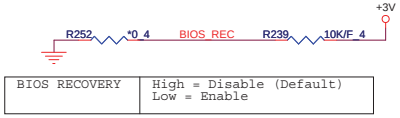

## MFG-TEST

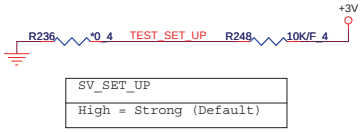


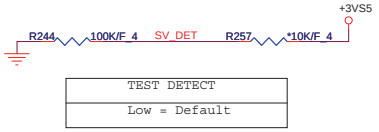

## GPIO Pull-up/Pull-down(CLG)



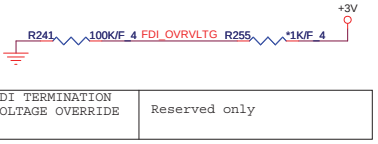




上DGPU_PWR_EN_R pull high
+3V 200K，200K 是不上件。

| | |
|---|---|
| DMI TERMINATION VOLTAGE OVERRIDE | Reserved only |



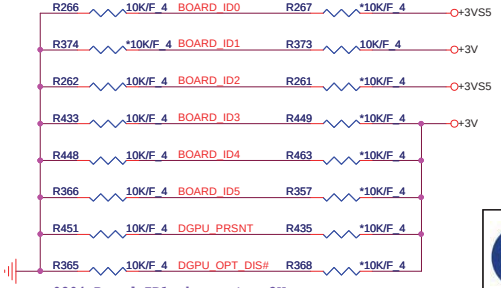

| BOARD_ID[3:0] | Model Name |
|---|---|
| 0000 | QLGA |
| 0001 | TWC |
| 0010 | JW2 |
| 0011 | TBD |
| 0100 | LG3 |
| 0101 | LG5 |
| 0110 | LG2C |
| 0111 | LG4C |

## Chief River BOARD ID SETTING

| | | |
|---|---|---|
| BOARD_ID0 | GPIO44 | MODEL BIT0 |
| BOARD_ID1 | GPIO71 | MODEL BIT1 |
| BOARD_ID2 | GPIO46 | MODEL BIT2 |
| BOARD_ID3 | GPIO34 | MODEL BIT3 |
| BOARD_ID4 | GPIO35 | No Dolby=0, Dolby=1 |
| BOARD_ID5 | GPIO69 | HM76=0, HM70=1 |
| DGPU_PRSNT | GPIO39 | Optimus=1, UMA=0 |
| DGPU_OPT_DIS# | GPIO70 | Optimus=0, Dis only=1 |

C Test
B Test

20110816 Define BRD_ID[3:0]


0804 Board_ID1 change to +3V
Board_ID5 change to +3V

[2,6,7,8,10,12,13,14,15,16,17,19,20,22,23,24,29,32,34] +3V
[6,7,8,10,14,19,22,24,26,29,30,34] +3VS5

NB5

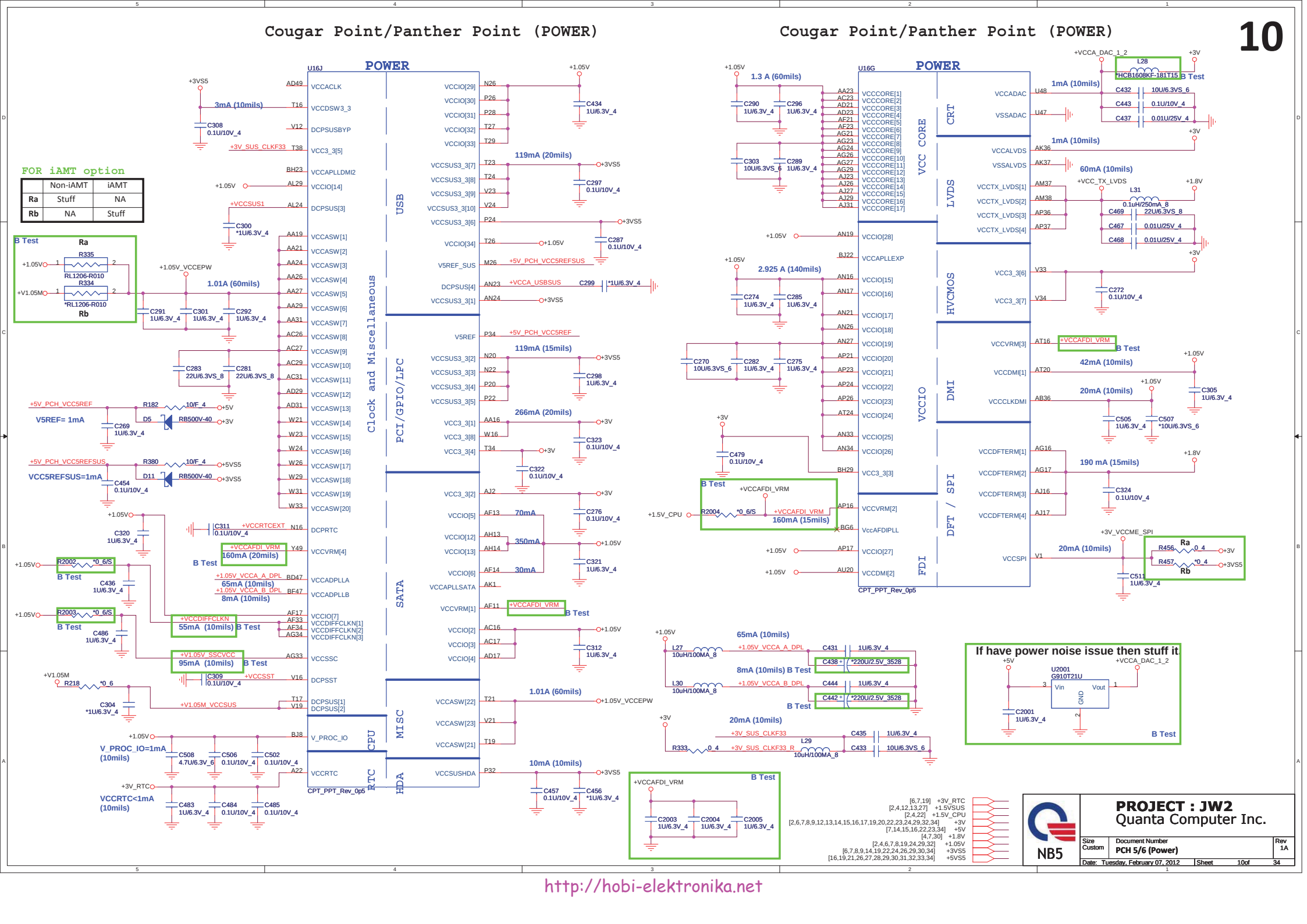
**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 4/6 (GPIO) | 1A |

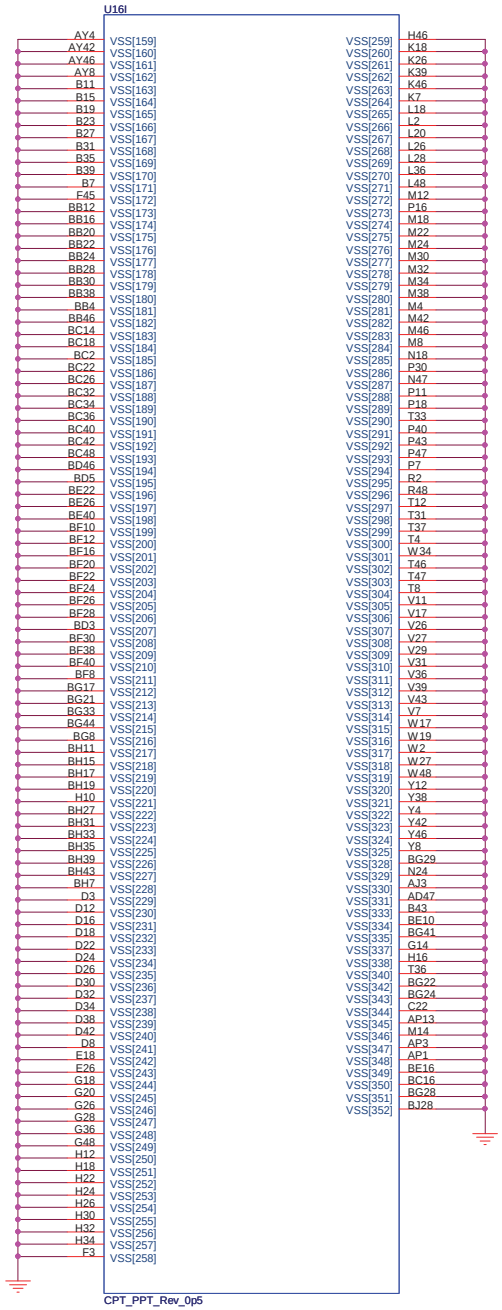
Date: Tuesday, February 07, 2012 | Sheet 9 of 34

Cougar Point/Panther Point (POWER)

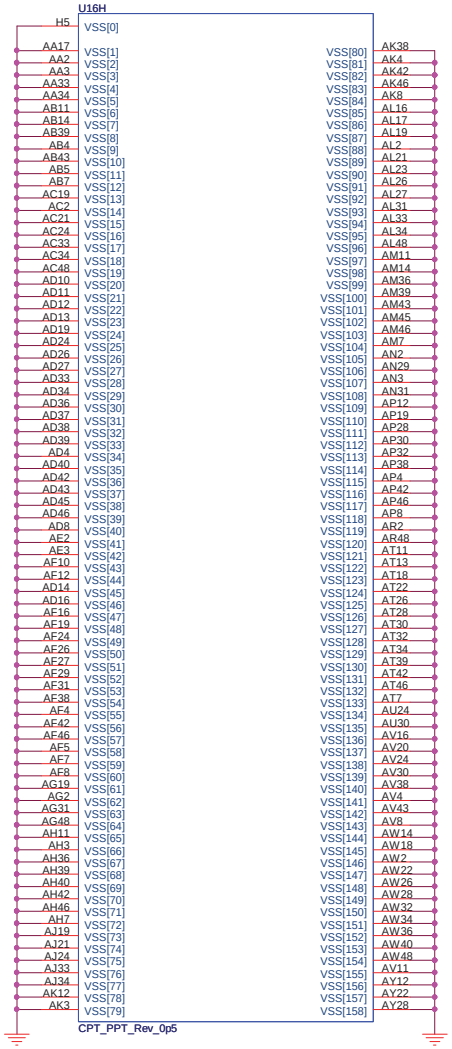




## Cougar Point/Panther Point (GND)



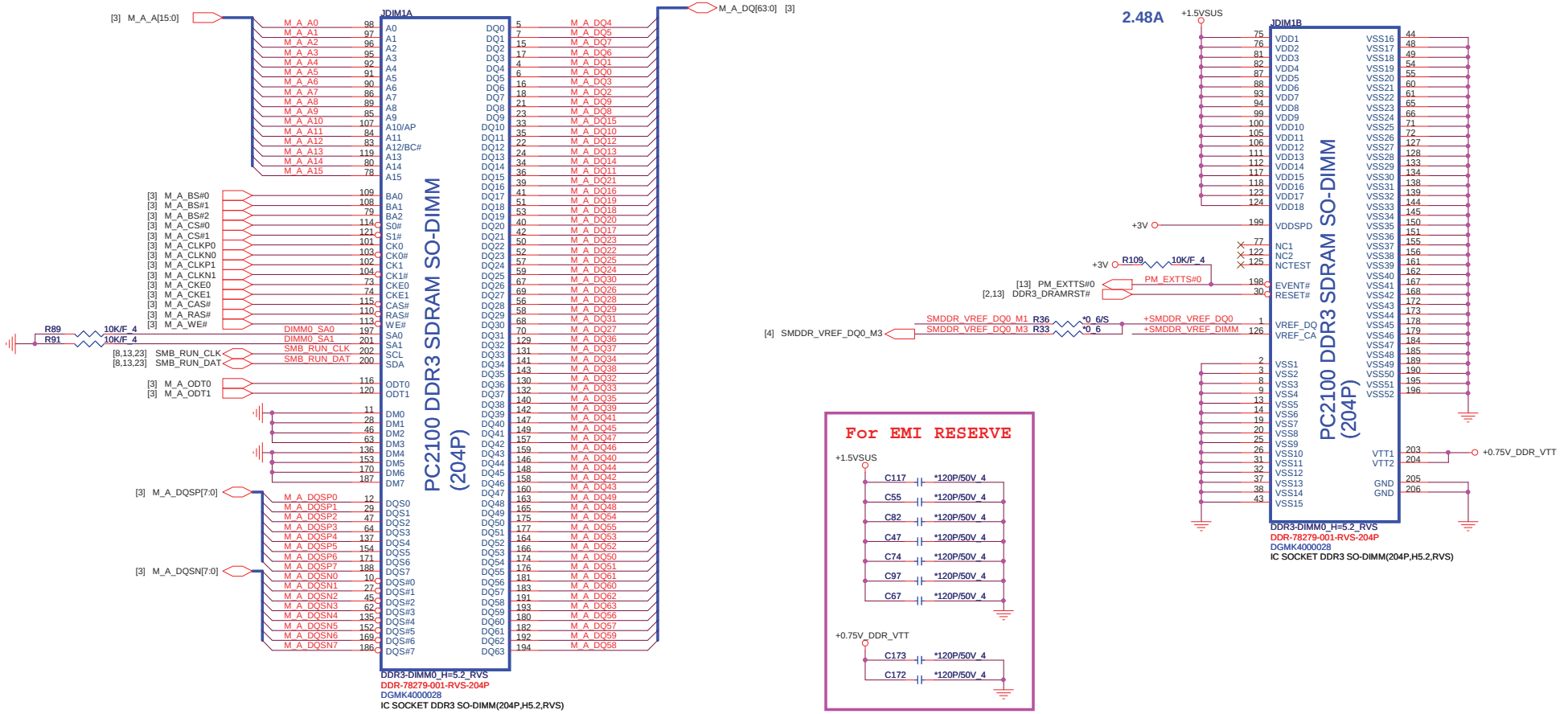

## Cougar Point/Panther Point (GND)



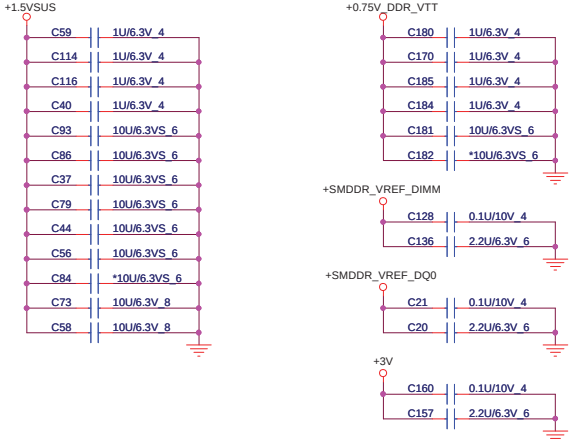

**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | PCH 6/6 (Ground) | 1A |
| Date: Thursday, January 12, 2012 | Sheet 11of 34 | |

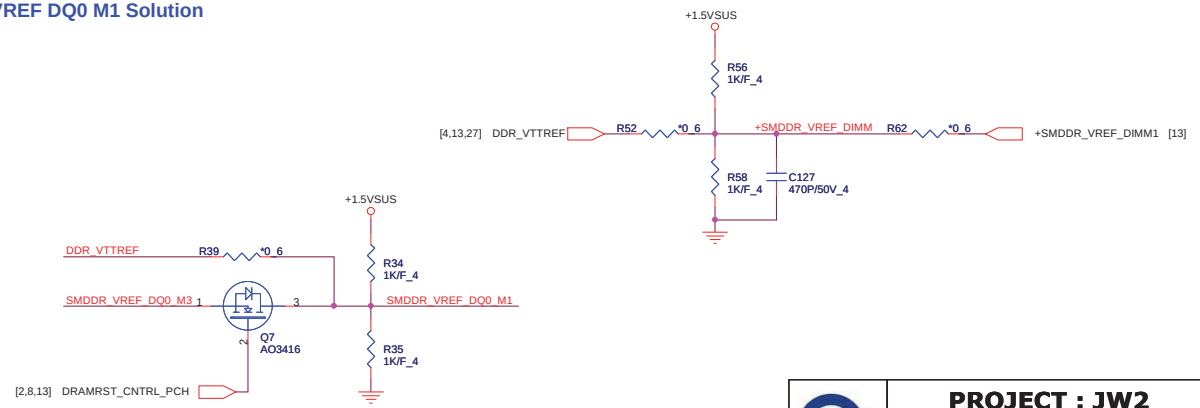
NB5




## Place these Caps near So-Dimm0.



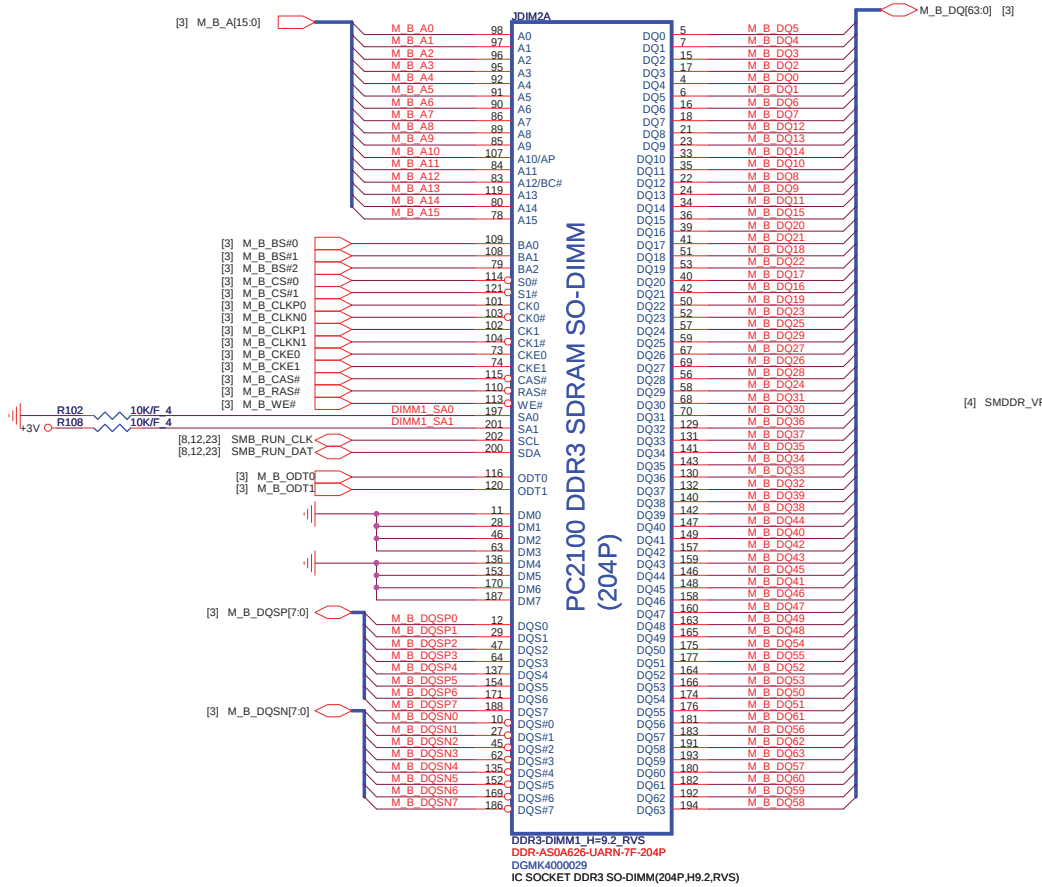

## VREF DQ0 M1 Solution

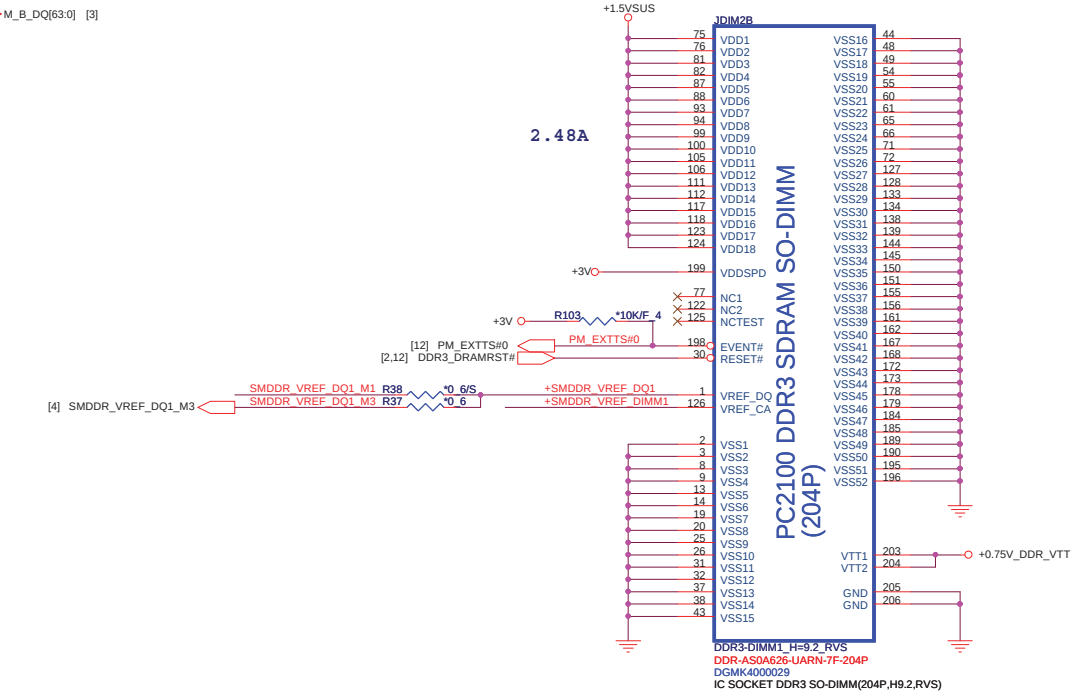



**PROJECT : JW2**
Quanta Computer Inc.

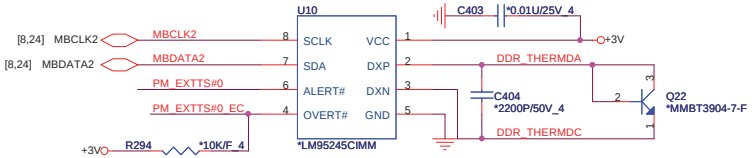
| Size | Document Number | Rev |
|---|---|---|
| Custom | System Memory 1/2 (5.2H) | 1A |
| Date: Tuesday, February 07, 2012 | Sheet 12of 34 | |

NB5

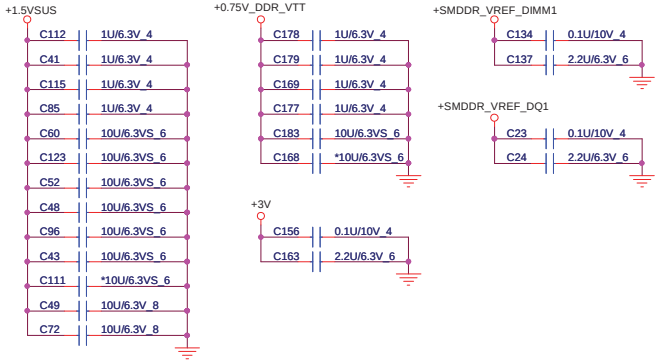


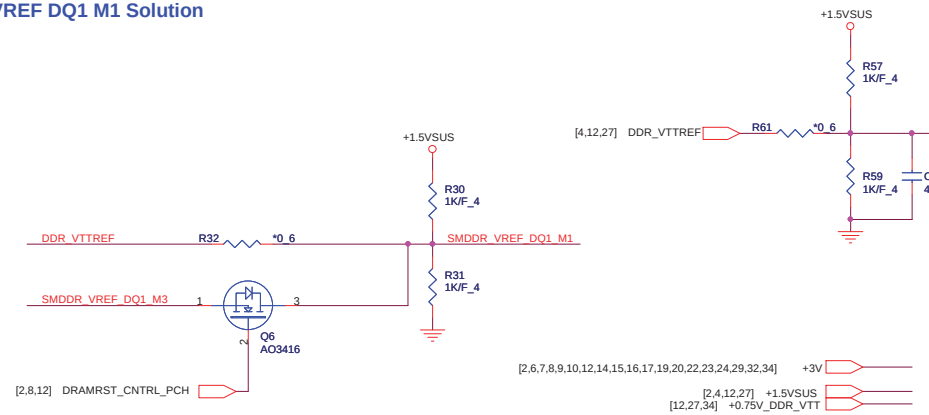

## DDR3 Thermal Sensor



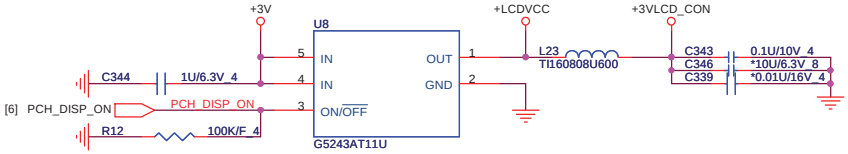

## Place these Caps near So-Dimm1.

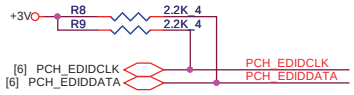


## VREF DQ1 M1 Solution

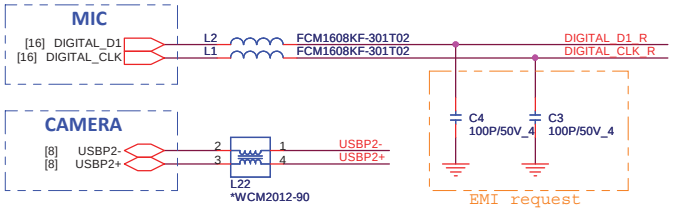



| | | | |
|---|---|---|---|
| NB5 | PROJECT : JW2<br>Quanta Computer Inc. | | |
| | Size: Custom | Document Number: System Memory 2/2 (9.2H) | Rev: 1A |
| | Date: Tuesday, February 07, 2012 | Sheet: 13of | 34 |

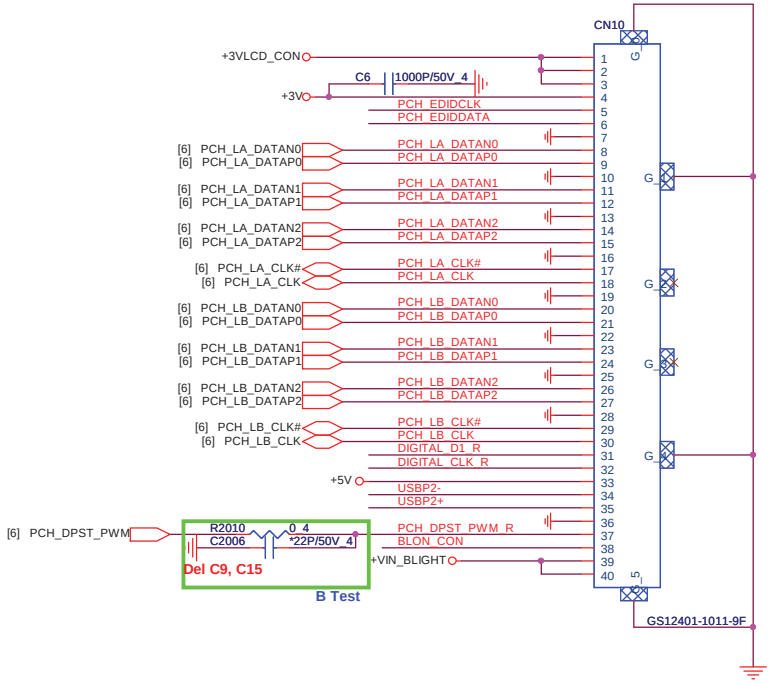


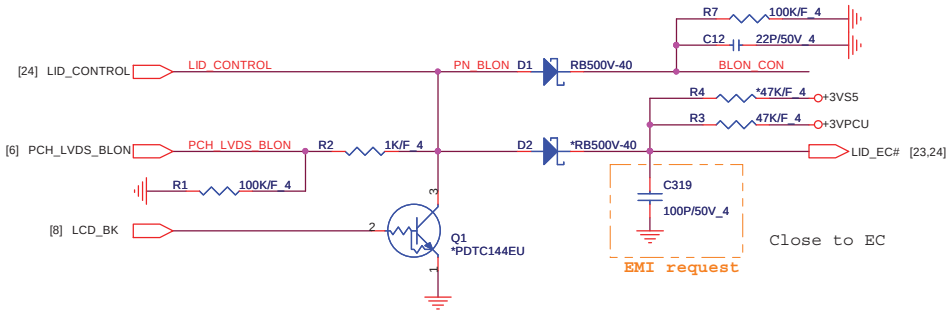




## USB Camera Connector









[2,6,7,8,9,10,12,13,15,16,17,19,20,22,23,24,29,32,34] +3V
[7,10,15,16,22,23,34] +5V
[19,25,26,27,29,33,34] +VIN
[7,19,22,23,24,25,26] +3VPCU

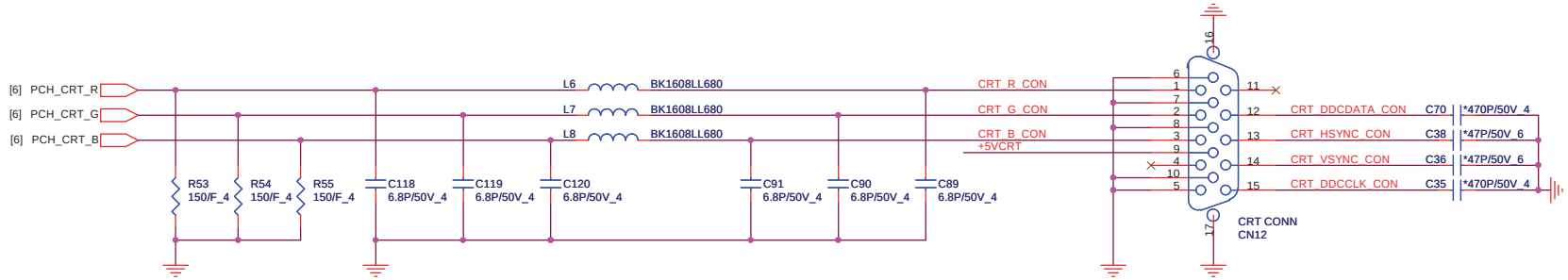


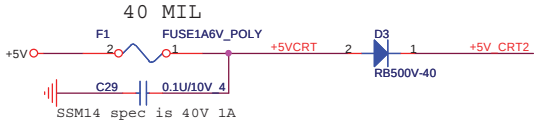
NB5

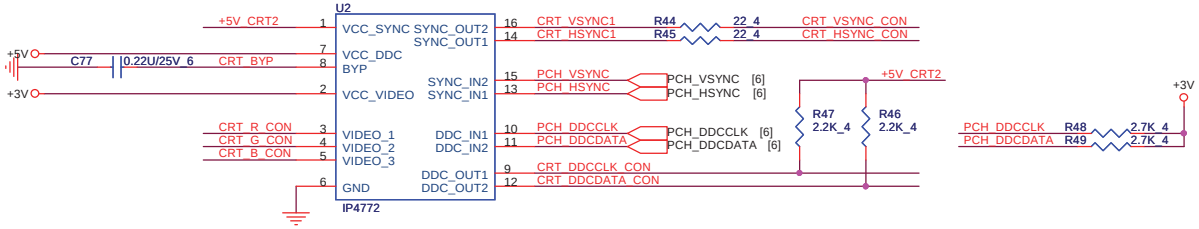
**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | LCD Connector (LVDS) | 1A |
| Date: Tuesday, February 07, 2012 | Sheet 14 of 34 | |

# CRT PORT

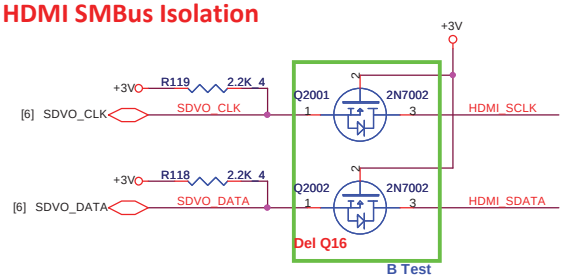


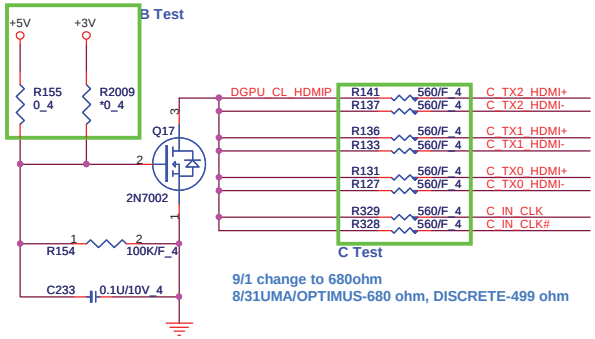



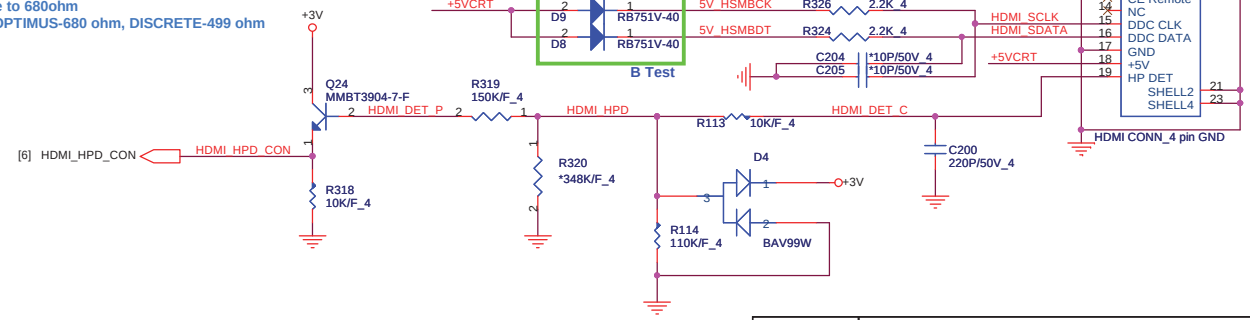

# HDMI PORT

## HDMI SMBus Isolation

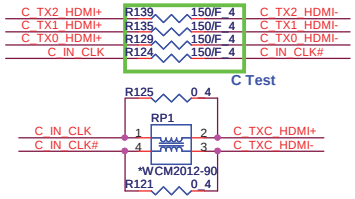


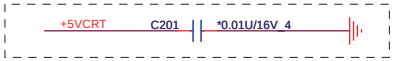




9/1 change to 680ohm
8/31UMA/OPTIMUS-680 ohm, DISCRETE-499 ohm




## EMI Solution



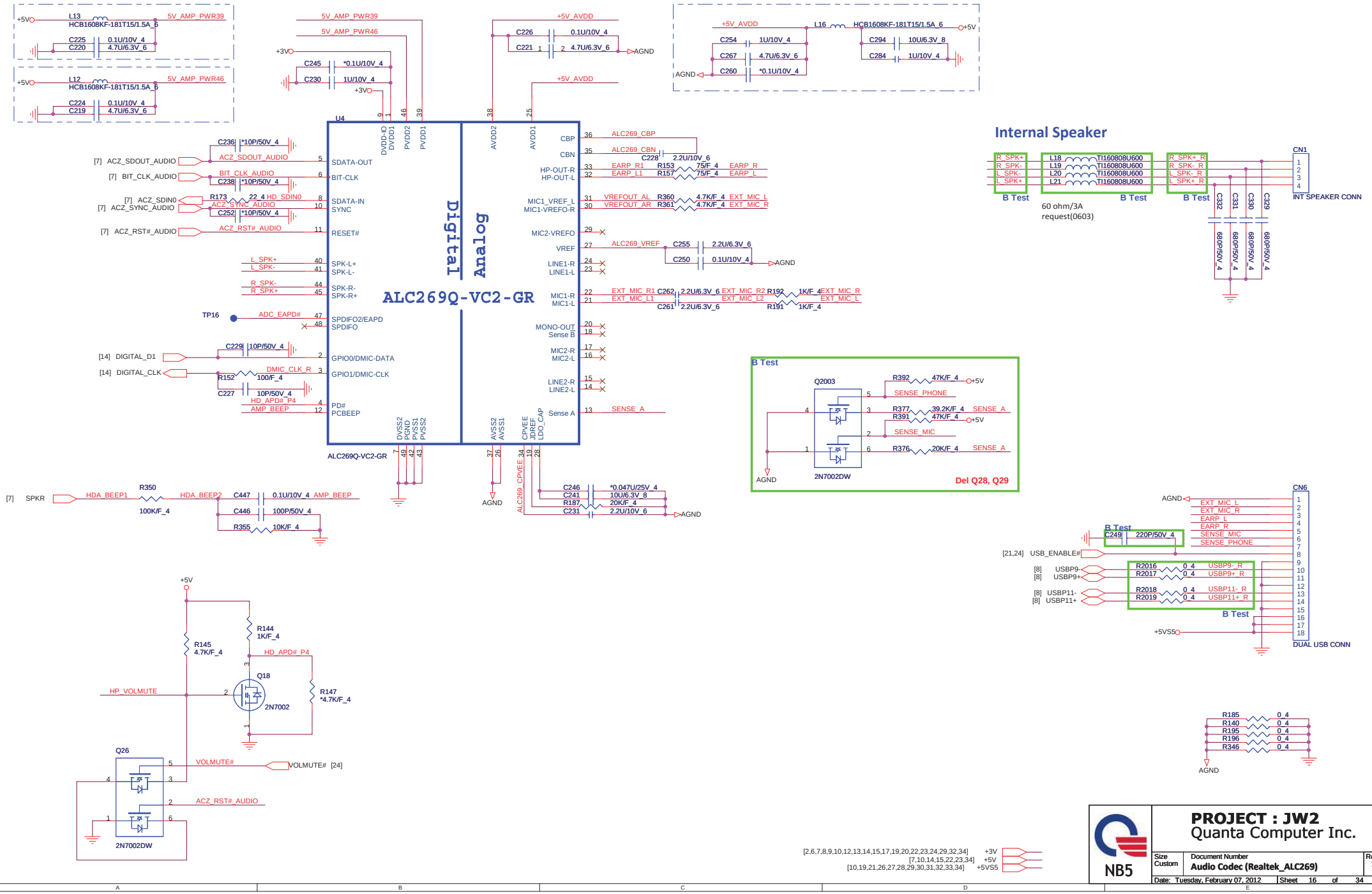

[2,6,7,8,9,10,12,13,14,16,17,19,20,22,23,24,29,32,34] +3V
[7,10,14,16,22,23,34] +5V



NB5

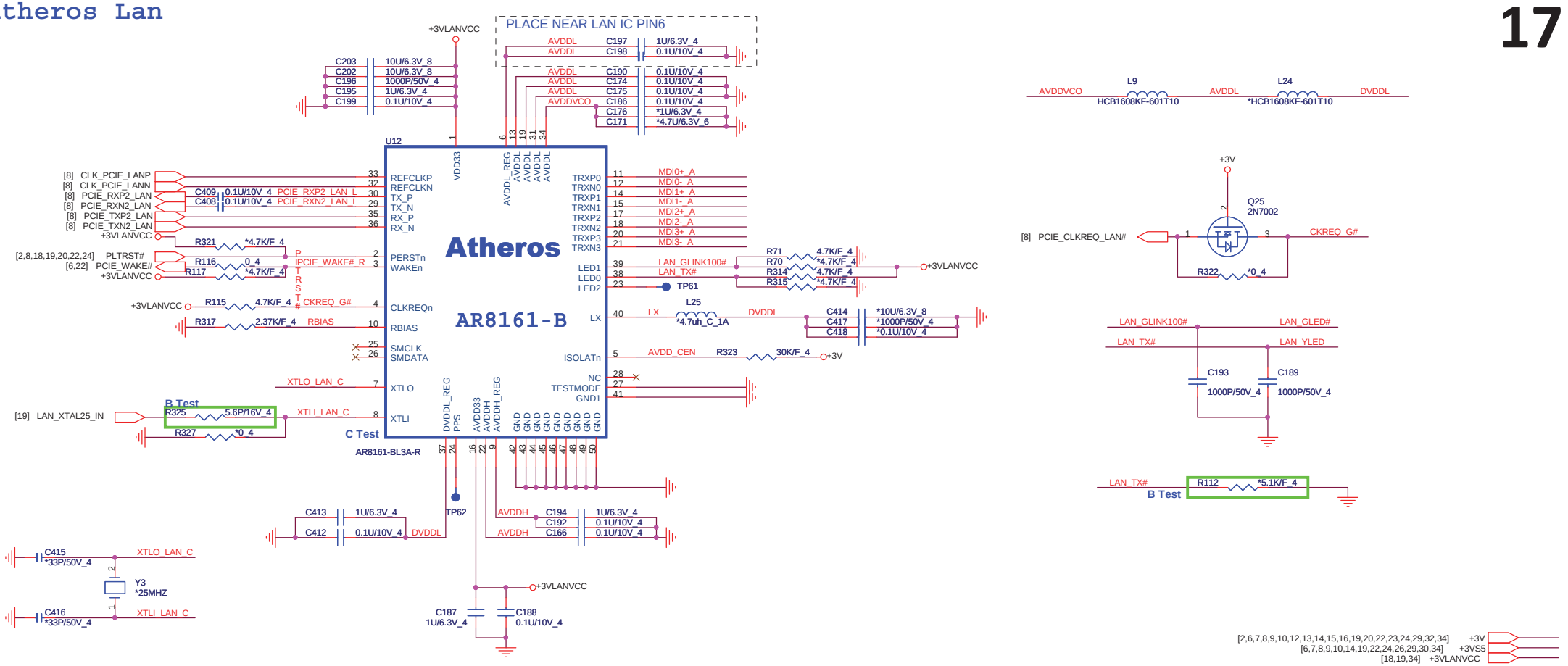
**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | CRT/HDMI Connector | 1A |
| Date: Tuesday, February 07, 2012 | Sheet 15 of 34 | |

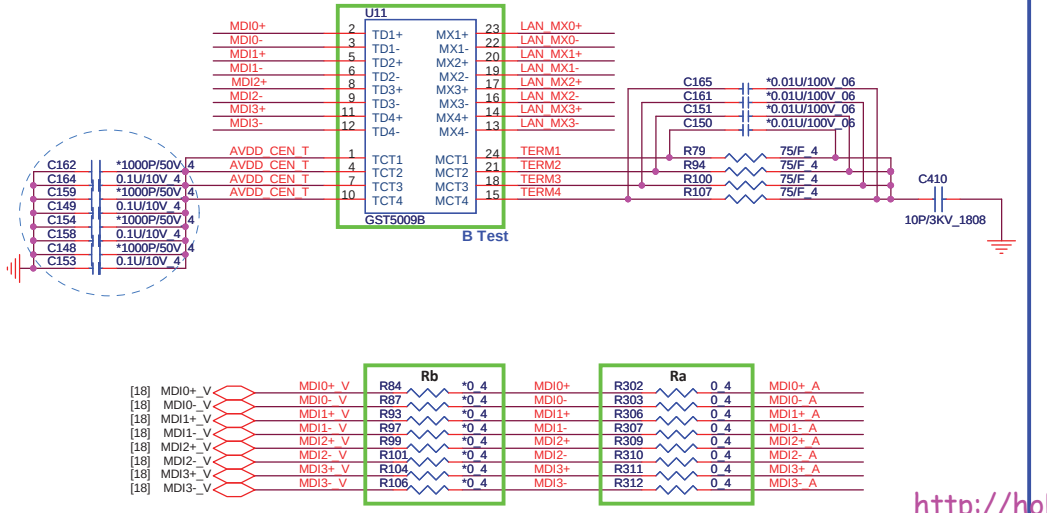


# Atheros Lan

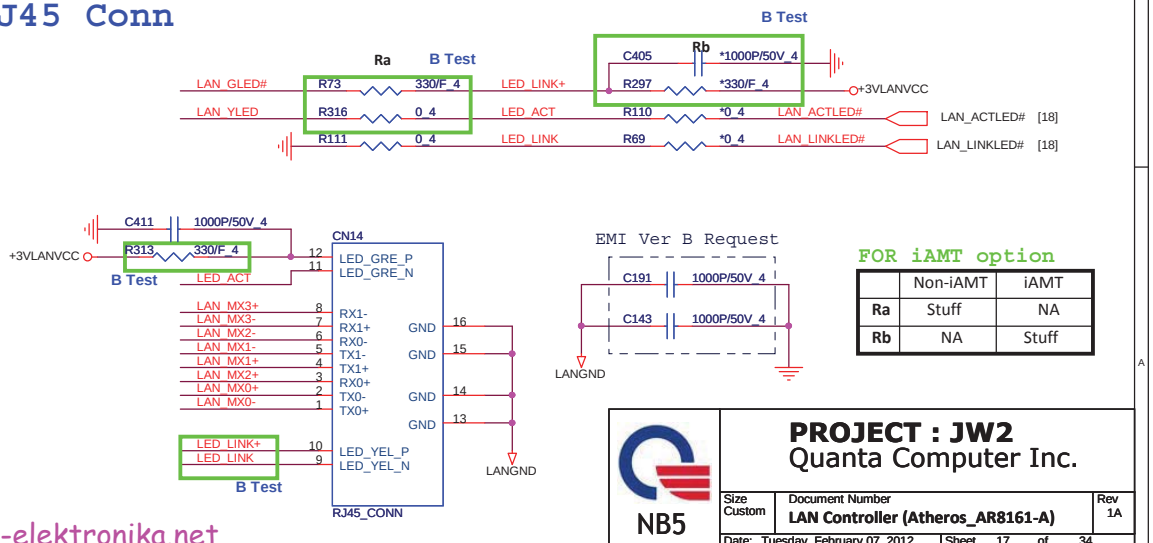





# TRANSFORMER




# RJ45 Conn



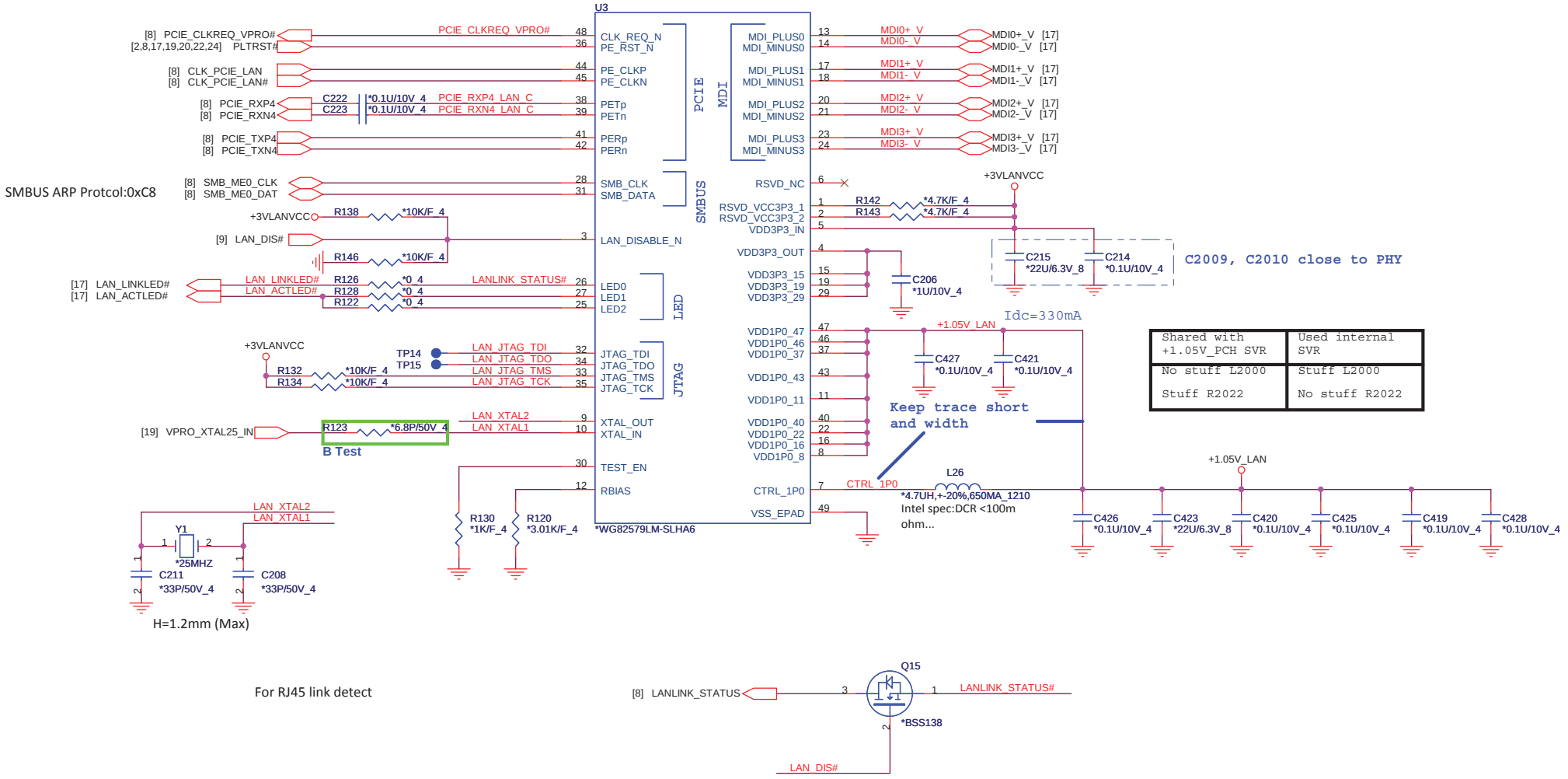



NB5

**PROJECT : JW2**
Quanta Computer Inc.

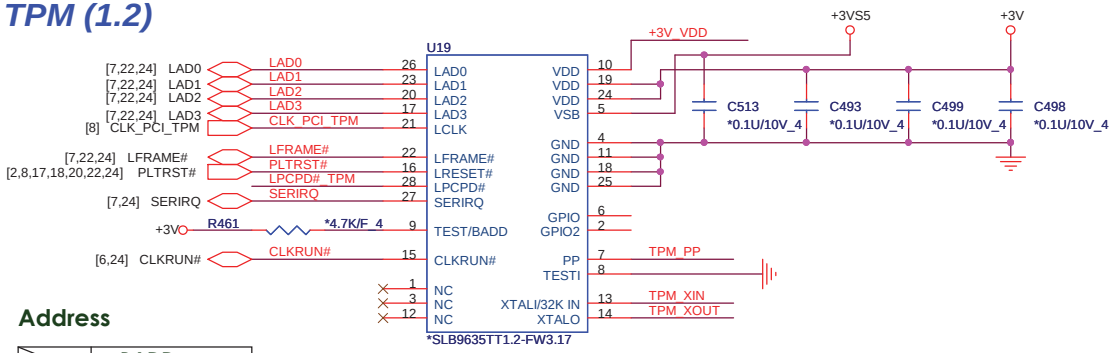
| Size | Document Number | Rev |
|---|---|---|
| Custom | LAN Controller (Atheros_AR8161-A) | 1A |

Date: Tuesday, February 07, 2012 | Sheet 17 of 34




| | |
|---|---|
| PROJECT : JW2 | |
| Quanta Computer Inc. | |
| NB5 | Size B / Document Number: Intel Lewisville 82579LM / Rev 1A |
| Date: Tuesday, February 07, 2012 | Sheet 18 of 34 |

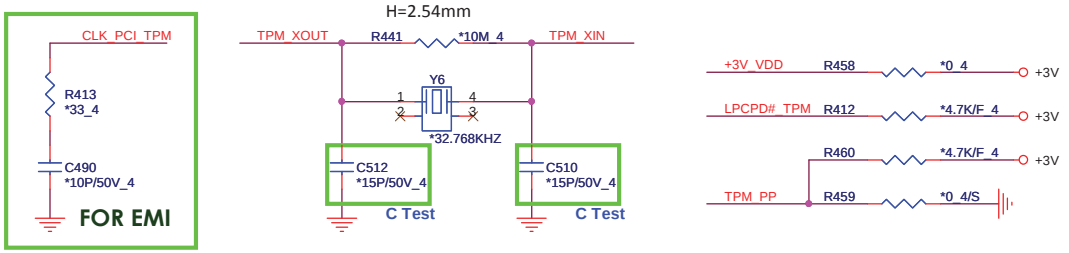
# TPM (1.2)

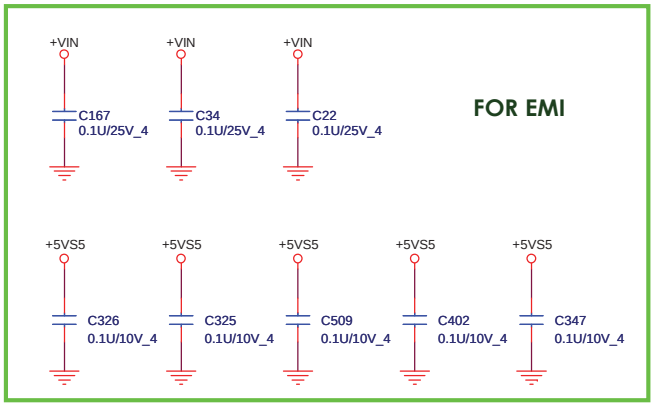



## Address

| | BADD |
|---|---|
| HIGH | 4EH/4F |

(default)



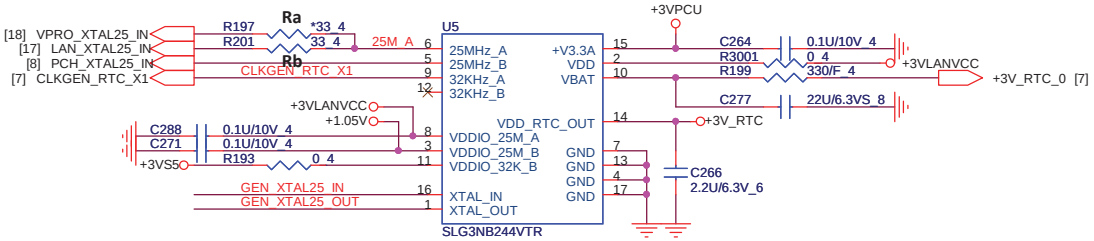

# Green CLK

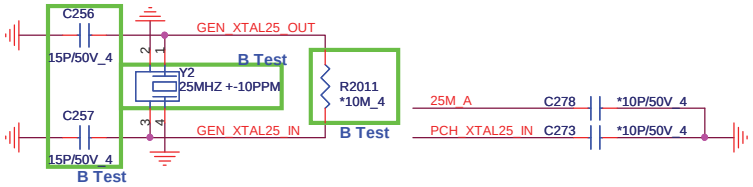
FOR LAN CLK option

| | Atheros | vPRO |
|---|---|---|
| Ra | NA | Stuff |
| Rb | Stuff | NA |

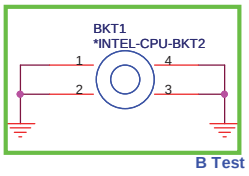
FOR TPM option

| | TPM | Non-TPM |
|---|---|---|
| R419 | Stuff | NA |
| U5 | AL3NB246000 | AL3NB244000 |

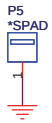


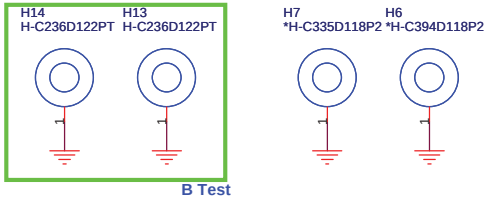

## CPU Bracket



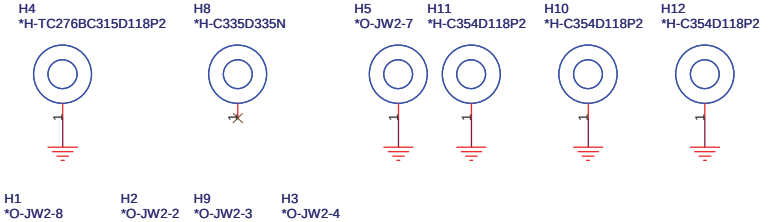

## MINI PCI Pad

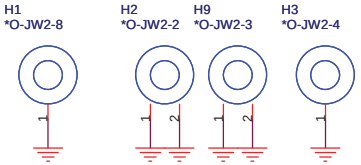



## PCH NU Screw Hold




## System Screw Hold



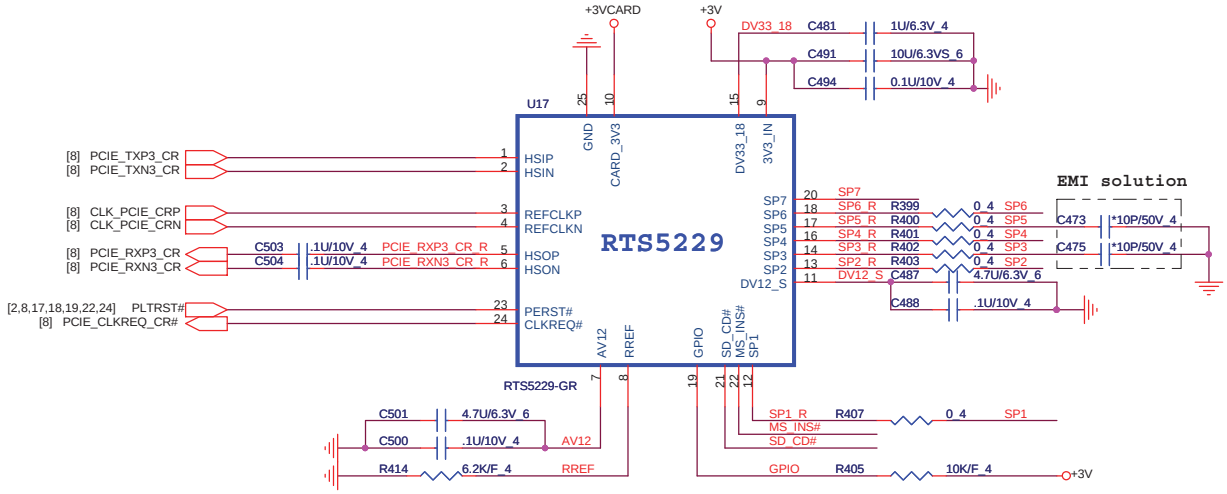

NB5

**PROJECT : JW2**
Quanta Computer Inc.

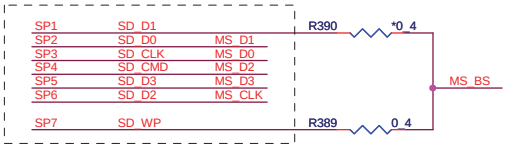
| Size | Document Number | Rev |
|---|---|---|
| B | TPM&Green CLK | 1A |

Date: Tuesday, February 07, 2012 Sheet 19 of 34

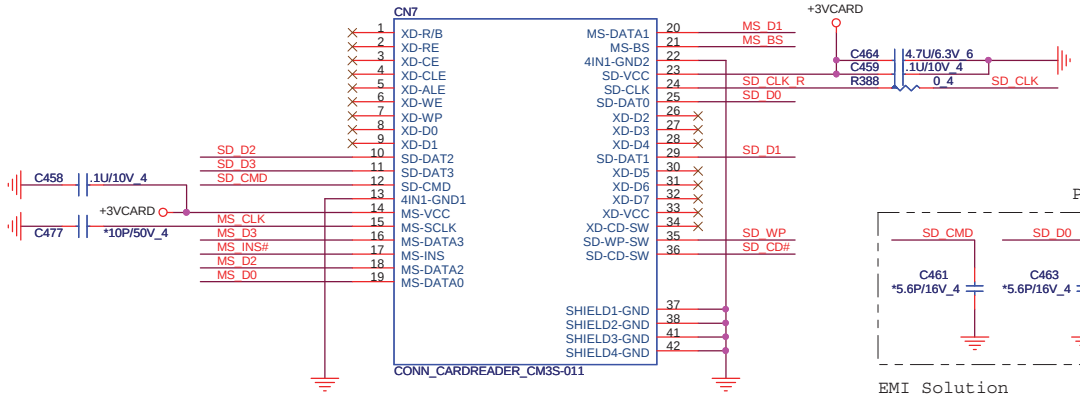
## RTS5229



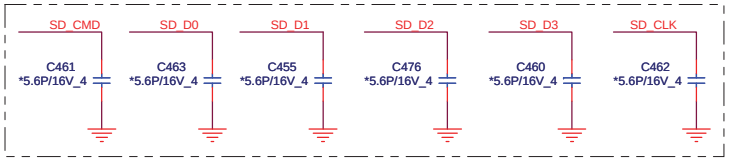

## Share Pin




## CR Socket




Please help to close to connector




EMI Solution

**Note:**

1. R5194, R5196, R5197, R5198, R5199, R5200 close to U37 pin
2. C5265, C5202 close to U37 pin7
3. C1021, C1022 close to U37 pin11
4. C1089, C1090 close to U37 pin9
5. C1019 close to U37 pin15
6. C1026, C1027 close to CN27 pin11
7. C1025 close to CN27 pin4

[2,6,7,8,9,10,12,13,14,15,16,17,19,22,23,24,29,32,34] +3V

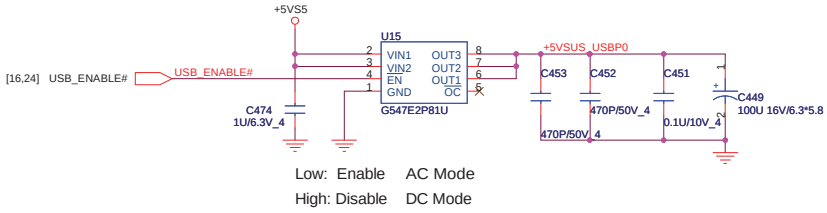


NB5

**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | RTS5229 & CR SOCKET | 1A |
| Date: Tuesday, February 07, 2012 | Sheet 20 of 34 | |

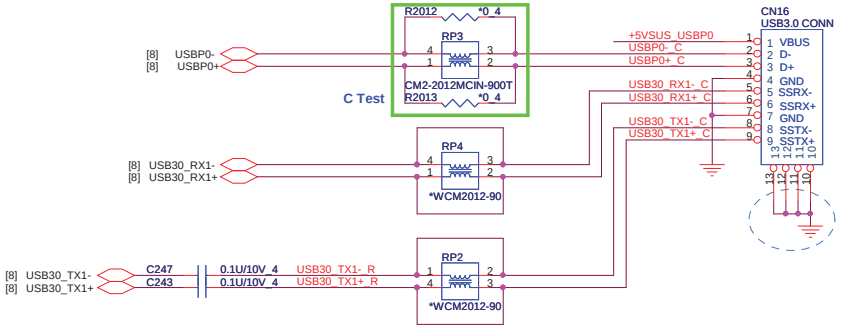
# USB3.0 / USB2.0 COMBO X 2



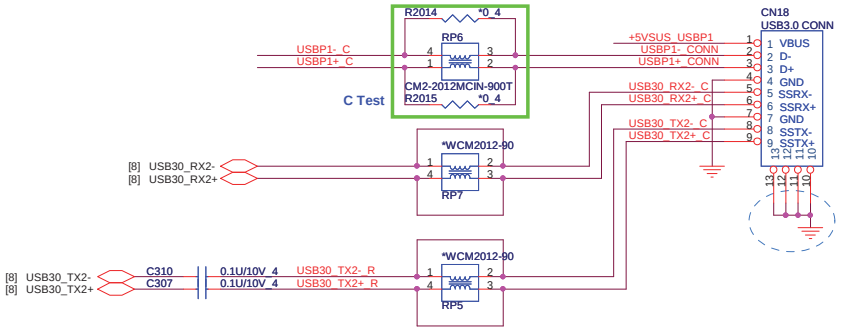

Low: Enable AC Mode

High: Disable DC Mode

## USB 3.0




## USB 3.0

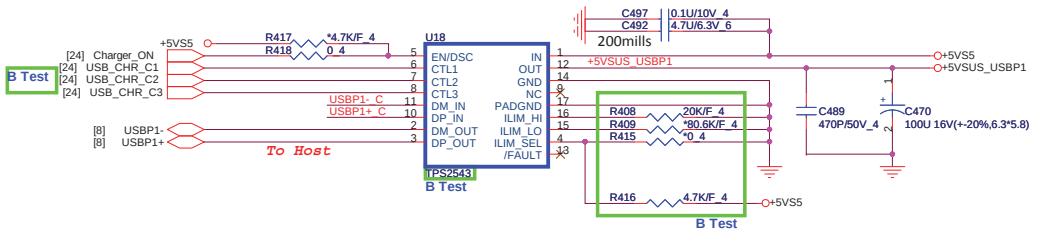


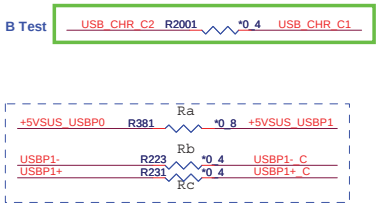

# USB Charger



high active
80 mils (Iout=2A)

Ios = 48000/RILIM0
default: Auto-detect




TPS2543/45 Control Truth Table

| CTL1 | CTL2 | CTL3 | ILIM_SEL | Charging Mode | Current Limit Setting | TPS2543 STATUS Output (active low) |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | Discharge | NA | off |
| 0 | 0 | 1 | 1 | DCP/auto | IOS_PW & ILIM_HI (1) | DCP load present |
| 0 | 1 | 0 | 1 | SDP | ILIM_HI | off |
| 0 | 1 | 1 | 1 | DCP/auto | ILIM_HI | DCP load present |
| 1 | 1 | 0 | 1 | SDP | ILIM_HI | off |
| 1 | 1 | 1 | 1 | CDP | ILIM_HI | CDP load present |

(1) ILIM_HI: 20K(R408), 2.4A

USB Charger option

| U18 | Ra | Rb | Rc |
|---|---|---|---|
| stuff | unstuff | unstuff | unstuff |
| unstuff | stuff | stuff | stuff |

| LGE SPEC | S0/S3 | | S4/S5 | |
|---|---|---|---|---|
| | AC Mode | DC Mode | AC Mode | DC Mode |
| charge mode | CDP | CDP | DCP | DCP |
| user define and wake up | | SDP | | OFF |

+3V [2,6,7,8,9,10,12,13,14,15,16,17,19,20,22,23,24,29,32,34]
+5VS5 [10,16,19,26,27,28,29,30,31,32,33,34]

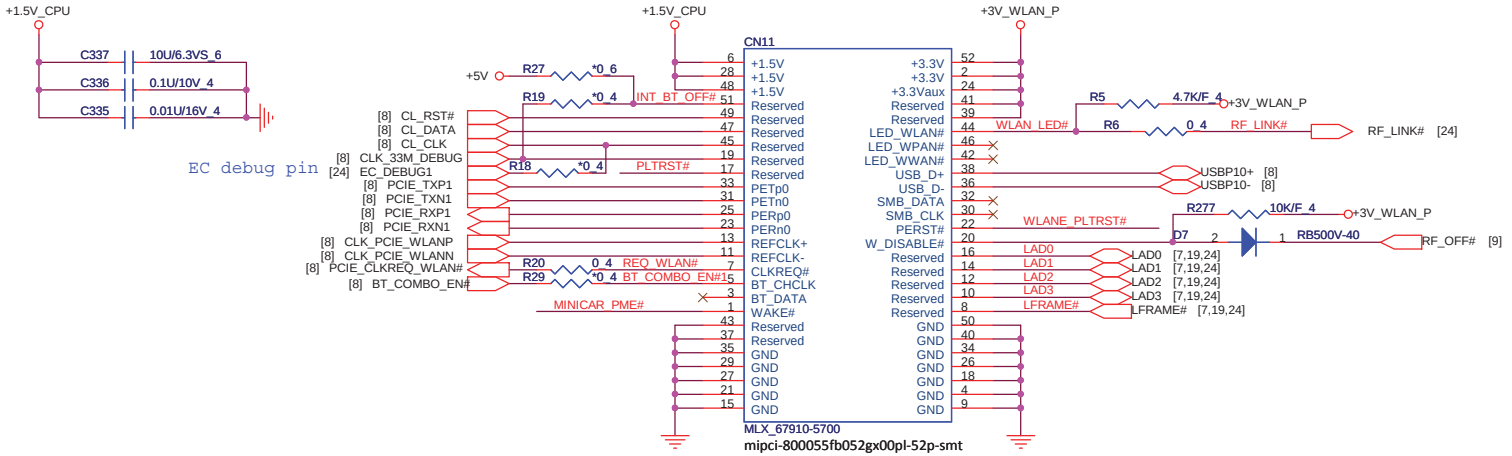
NB5

**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | USB 3.0 Connector | 1A |

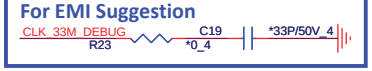
Date: Tuesday, February 07, 2012 Sheet 21 of 34

# Mini Card/WLAN/BT(Option)



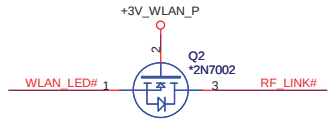

| LGE mini-pcie power status | | |
|---|---|---|
| WLAN | Bluetooth | +3V_WLAN_P |
| Radio-ON | Radio-ON | Power-ON |
| Radio-ON | Radio-OFF | Power-ON |
| Radio-OFF | Radio-ON | Power-ON |
| Radio-OFF | Radio-OFF | Power-OFF |

**For EMI Suggestion**

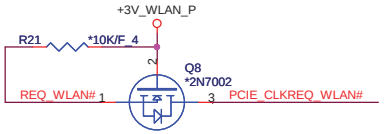



**Avoid leakage issue**

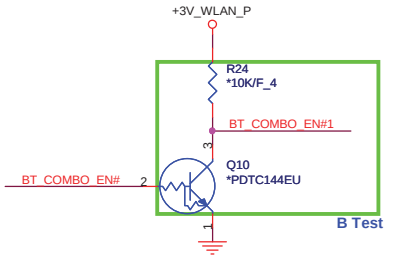
**PIN44**



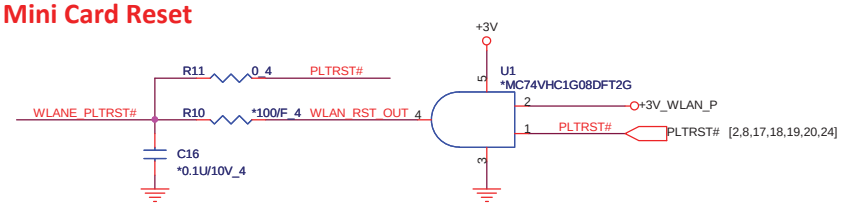

**PIN7**




**PIN5**

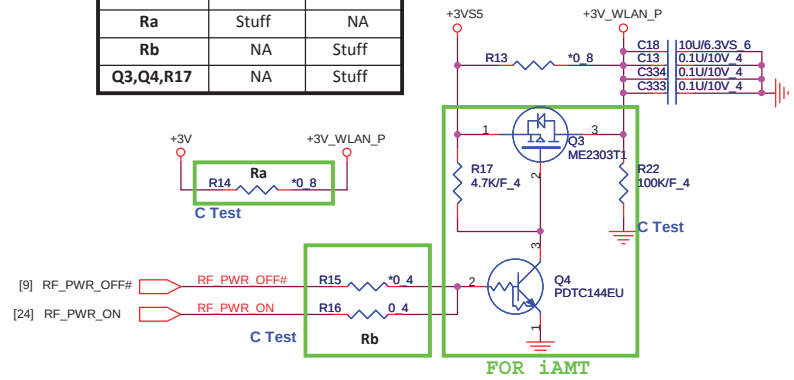



# Mini Card Reset

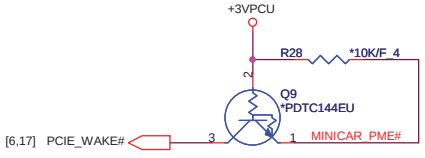



**FOR iAMT option**

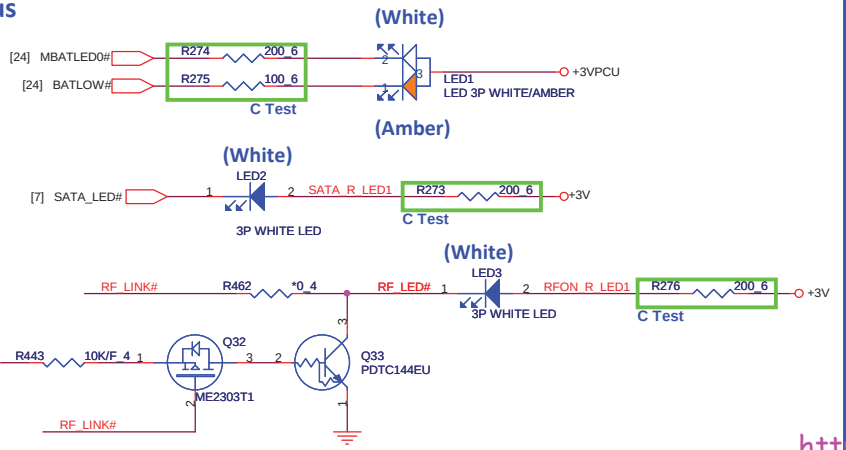
| | Non-iAMT | iAMT |
|---|---|---|
| Ra | Stuff | NA |
| Rb | NA | Stuff |
| Q3,Q4,R17 | NA | Stuff |



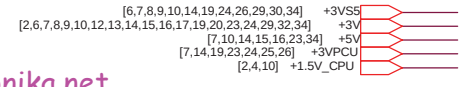

# Support Wake Function(Reserve)



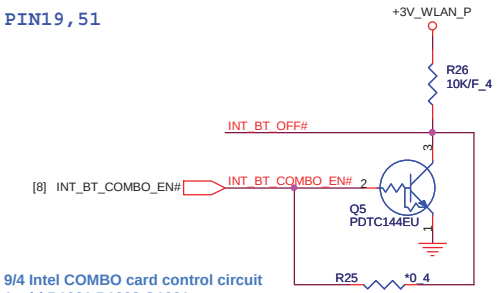

# LED Status




# Capacity module Connector


**PIN19,51**




9/4 Intel COMBO card control circuit
1.add R1001,R1002,Q1001
2.add net name"INT_BT_COMBO_EN#" -> "INT_BT_OFF#"

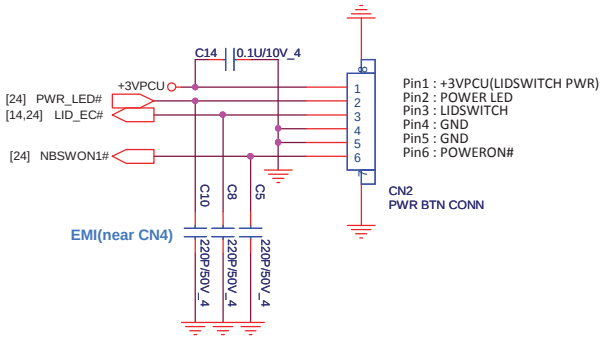


NB5

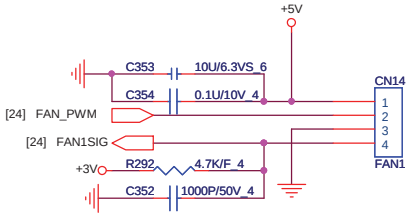
**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | MINI PCIE CONN/LED | 1A |
| Date: Tuesday, February 07, 2012 | Sheet 22 of 34 | |

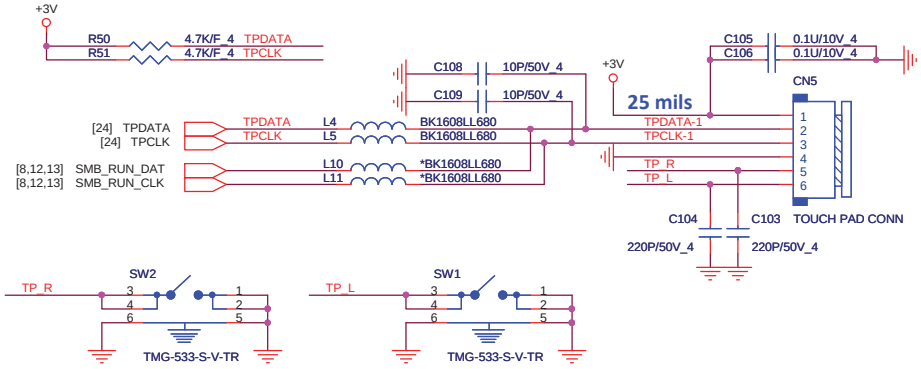
## Power Botton Connector



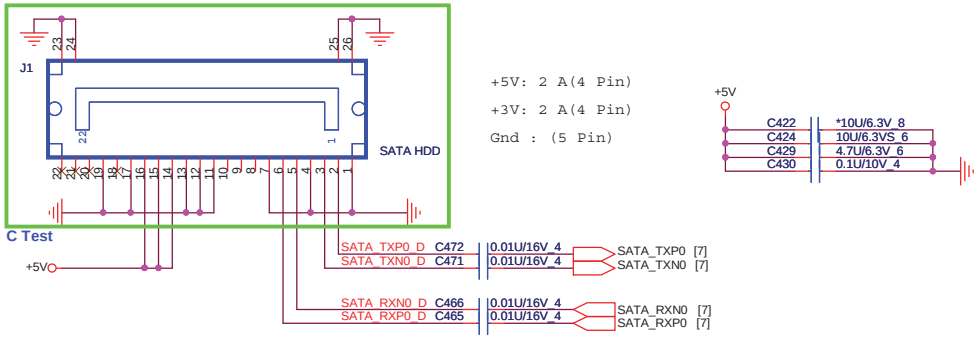

## CPU FAN




## Touch Pad Connector

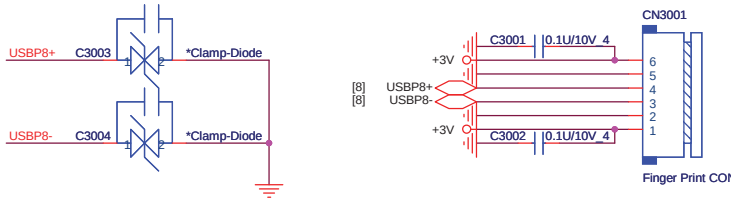



## SATA HDD Connector

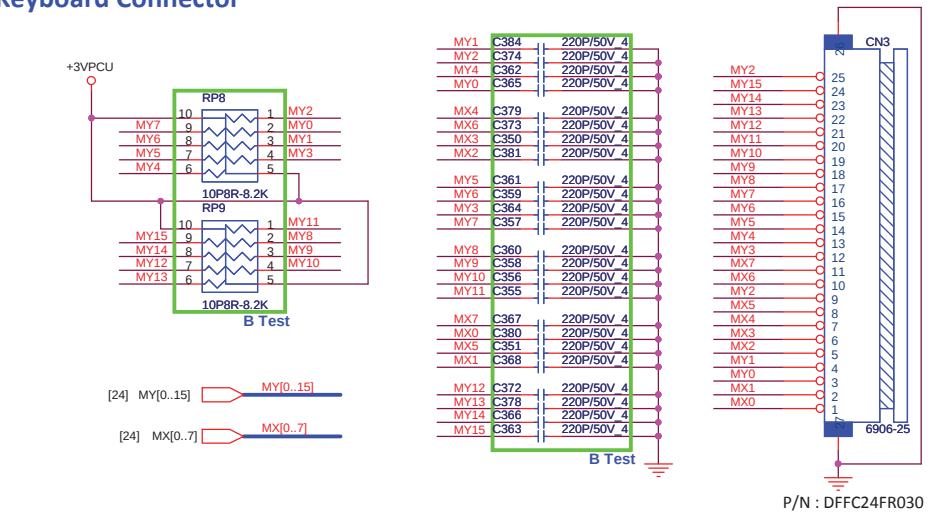



DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

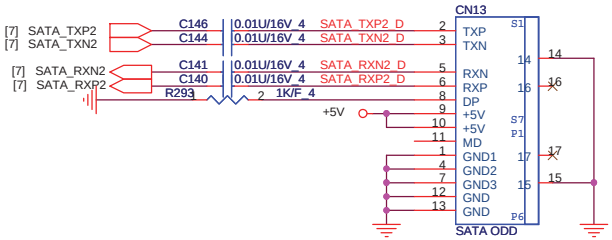
## Finger Print Connector

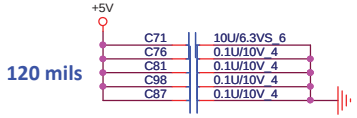



## Keyboard Connector




## SATA ODD Connector




[2,6,7,8,9,10,12,13,14,15,16,17,19,20,22,24,29,32,34] +3V
[7,10,14,15,16,22,34] +5V
[7,14,19,22,24,25,26] +3VPCU

NB5

**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | HDD/ODD/FAN/KEY CONN | 1A |

Date: Tuesday, February 07, 2012 | Sheet 23 of 34

[2,6,7,8,9,10,12,13,14,15,16,17,19,20,22,23,29,32,34] +3V
[6,7,8,9,10,14,19,22,26,29,30,34] +3VS5
[7,14,19,22,23,25,26] +3VPCU
[2,4,6,7,8,10,19,29,32] +1.05V

Del C316
B Test

Layout Note:
Place all capacitors close to IT8518E.

+3VPCU
12 MILS
C314 0.1U/10V_4
C279 0.1U/10V_4
C313 0.1U/10V_4
C295 0.1U/10V_4
C280 0.1U/10V_4
C239 0.1U/10V_4

Select Pin
Rb R167 10K/F_4 CB/LG Ra R166 *10K/F_4

| | CB/LG select |
|---|---|
| LG project | Ra |
| CB project | Rb |

FOR iAMT option

| | Non-iAMT | iAMT |
|---|---|---|
| Ra | Stuff | NA |
| Rb | NA | Stuff |

Ra R163 0_4 PCH_SPI_CS1# [7]
Rb R164 *0_4 PCH_SPI_CS0# [7]

Q19 2N7002DW
H_PROCHOT# EC R165 100K/F_4
H_PROCHOT# Q R150 0_4 H_PROCHOT# [2,32]
BATLOW
BATLOW# [22]

Q21 2N7002DW
PWR_LED
PWR_LED# [23]
MBATLED0
MBATLED0# [22]

+3VPCU
R227 470K_4
EC_WRST
C315 0.1U/10V_4

+3V_ECACC L15 HCB1608KF-181T15 +3VPCU
C242 1U/6.3V_4
C237 1000P/50V_4
IT8502_AGND IT8502_AGND
+3v_STBY L17 HCB1608KF-181T15 +3VPCU
C306 0.1U/10V_4
C317 0.1U/10V_4
+3V +3VPCU
Del R225, R226
B Test

U6 IT8518E/HX

LPC
[7,19,22] LAD0
[7,19,22] LAD1
[7,19,22] LAD2
[7,19,22] LAD3
[2,8,17,18,19,20,22] PLTRST#
[8] CLK_33M_KBC
[7,19,22] LFRAME#
[6] SLP_S5
LAD0
LAD1
LAD2
LAD3
LPCRST#/WUI4/GPD2
LPCCLK
LFRAME#
LPCPD#/WUI6/GPE6

GPIO
[9] EC_A20GATE D6 RB500V-40
[7,19] SERIRQ D15 RB500V-40
[9] SIO_EXT_SMI# D14 RB500V-40
[9] SIO_EXT_SCI#
EC_WRST
[9] EC_RCIN# D16 RB500V-40
TP41
GA20/GPB5
SERIRQ
ECSMI#/GPD4
ECSCI#/GPD3
WRST#
KBRST#/GPB6
PWUREQ#/BBO/GPC7
EGCLK/WUI27/GPE3 BATLOW
EGCS#/WUI26/GPE2 VRON [32]
EGAD/WUI25/GPE1 PM_SLP_A# [6,31]
KSO16/SMOSI/GPC3 EC_PWROK [6]
KSO17/SMISO/GPC5 M_PWROK [6,31]
L80HLAT/BAO/WUI24/GPE0 SUSON [27]
L80LLAT/WUI7/GPE7 PM_SLP_LAN# [6,34]
SBUSY/GPG1/ID7 MBATLED0
HMOSIGPH6/ID6 H_SI R184 0_4 PCH_SPI_SI [7]
HMISO/GPH5/ID5 H_SO R180 0_4 PCH_SPI_SO [7]
HSCK/GPH4/ID4 H_CLK R179 0_4 PCH_SPI_CLK [7]
HSCE#/WUI19/GPH3/ID3 H_SCE#
CTX1/WUI18/GPH2/SMDAT3/ID2 MAINON [25,27,29,30,34]
CRX1/WUI17/GPH1/SMCLK3/ID1 RF_LINK# [22]
CLKRUN#/WUI16/GPH0/ID0 CLKRUN# [6,19]

[25] D/C#
[6] RSMRST#
GPC0
TMA0/GPB2

IT8518E/HX

H_PROCHOT# EC
[21] Charger_ON
Charger_ON
PS2DAT0/TMB1/GPF1
PS2CLK0/TMB0/GPF0

PS/2
[23] TPDATA TPDATA
[23] TPCLK TPCLK
PS2DAT2/WUI21/GPF5
PS2CLK2/WUI20/GPF4

SM_BUS
SMCLK2/WUI22/GPF6/PECI EC_PECI_R R205 43_4 EC_PECI [2]
SMDAT2/WUI23/GPF7
SMCLK0/GPB3 MBCLK MBCLK [25]
SMDAT0/GPB4 MBDATA MBDATA [25]
SMCLK1/GPC1 MBCLK2 MBCLK2 [8,13]
SMDAT1/GPC2 MBDATA2 MBDATA2 [8,13]

For Battery charge/charge
For PCH SMB/DDR Thermal IC/VGA/cap board

CB/LG
[21] USB_CHR_C3
[26,27,28,29,30] HWPG
[14] LID_CONTROL
[22] RF_PWR_ON
[7] ACZ_SDOUT
D12 RB500V-40
[22] EC_DEBUG1
DAC4/DCD0#/GPJ4
DSR0#/GPG6
GINT/CTS0#/GPD5
PS2DAT1/RTS0#/GPF3
DAC5/RIG0#/GPJ5
PS2CLK1/DTR0#/GPF2
RXD/SIN0/GPB0
TXD/SOUT0/GPB1

UART
PWM0/GPA0 LAN_POWER [34]
PWM1/GPA1 Num LK TP40 AC_PRESENT [6]
PWM2/GPA2 SATA5GP_EC TP39 FAN_PWM [23]
PWM3/GPA3 SUS_PWR_ACK [6]
PWM4/GPA4 VOLMUTE# [16]
PWM5/GPA5
PWM6/SSCK/GPA6
PWM7/GPA7

PWM
TACH0/GPD6 USB_CHR_C2 [21] B Test
TACH1/TMA1/GPD7 R204 *10K/F_4 +3V
R200 0_4 FAN1SIG [23]
TMR0/WUI2/GPC4 3VS5_ON [26]
TMR1/WUI3/GPC6 SUSC# [6]
5VS5_ON [26]

[16,21] USB_ENABLE#
EC_SCK
GPG0
FSCK
EC_SO
EC_SI
EC_CE#
FMISO
FMOSI
FSCE#
SSCE0#/GPG2

FLASH

TP24
[23] MY[0..15]
MY0 MY1 MY2 MY3 MY4 MY5 MY6 MY7 MY8 MY9 MY10 MY11 MY12 MY13 MY14 MY15
KSO0/PD0
KSO1/PD1
KSO2/PD2
KSO3/PD3
KSO4/PD4
KSO5/PD5
KSO6/PD6
KSO7/PD7
KSO8/ACK#
KSO9/BUSY
KSO10/PE
KSO11/ERR#
KSO12/SLCT
KSO13
KSO14
KSO15
KSI0/STB#
KSI1/AFD#
KSI2/INIT#
KSI3/SLIN#
KSI4
KSI5
KSI6
KSI7

KBMX
WAKE UP
PWRSW/GPE4 NBSWON1# NBSWON1# [23]
RI1#/WUI0/GPD0 LID_EC# [14,23]
RI2#/WUI1/GPD1 ACIN [25]
WUI5/GPE5 SUSB# [6]
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7 PWR_LED

[23] MX[0..7]
MX0 MX1 MX2 MX3 MX4 MX5 MX6 MX7

A/D D/A
ADC0/GPI0 EC_GPI0
ADC1/GPI1 GFX_HWPG_EC TP21 SYS_I [25]
ADC2/GPI2 AD_AIR [25]
ADC3/GPI3 TEMP_MBAT [25]
ADC4/WUI28/GPI4
ADC5/WUI29/GPI5
ADC6/WUI30/GPI6 SETVPRO TP20
ADC7/WUI31/GPI7

CLOCK
CK32K
CK32KE
DAC0/GPJ0 USB_CHR_C1 USB_CHR_C1 [21]
DAC1/GPJ1
DAC2/GPJ2 VFAN TP17
DAC3/GPJ3 D10 RB500V-40 DNBSWON# [6]
R385 10K/F_4 +3VS5

VSS VSS VSS VSS VSS VSS AVSS VCORE
C318 0.1U/10V_4
IT8502_AGND

IT8518E/HX

L14 HCB1608KF-181T15
EE
IT8502_AGND

thermal shutdown circuit

+3VPCU
MBCLK R190 10K/F_4
MBDATA R194 10K/F_4
+3V
MBCLK2 R198 10K/F_4
MBDATA2 R203 10K/F_4

+3VPCU
R207 10K/F_4
NBSWON1#
C302 0.1U/10V_4

EC_CT_UP R170 *4.7K/F_4 +1.05V
C248 220P/50V_4
EC_WRST Q20 *MMBT3904-7-F PM_THRMTRIP# [2,9]

| | |
|---|---|
| Non-iAMT | 4MB |
| iAMT | 8MB |

| Platform | ADC |
|---|---|
| JW2 | 0.00 V |
| TWC | 0.75 V |
| SW6C | 1.50 V |
| CB3 | 2.25 V |
| CB4 | 3.00 V |

+3VPCU
R175 10K/F_4 EC_GPI0 R162 *10K/F_4

Select Pin
Rd R161 10K/F_4 SETVPRO R151 *10K/F_4 Rc +3VPCU

| | VPRO Select |
|---|---|
| VPRO | Rc |
| Non-VPRO | Rd |

| Vender | Size | P/N |
|---|---|---|
| EON | 4MB | AKE39ZN0Q02 (EN25Q32B-104HIP) |
| AMIC | 4MB | AKE39F-0800 (A25LQ32AM-F/Q) |
| Socket | | DFHS08FS023 |

U13 SPI Flash ROM
EC_CE# EC_SCK R363 47_4 EC_SCK_R
EC_SI R362 47_4 EC_SI_R
EC_SO R351 15_4 EC_SO_R
CE# SCK SI SO WP# VDD HOLD# VSS
+3VPCU R347 10K/F_4
R364 10K/F_4 C448 0.1U/10V_4
B Test



NB5

PROJECT : JW2
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | Embedded Controller (ITE_IT8518E/HX) | 1A |

Date: Tuesday, February 07, 2012 Sheet 24 of 34

TOP DC_JACK
90W/4.75A

Place this ZVS close to idea diode

Do Not add test point on BATDIS_G signal

Kelvin Connections for the Current-Sense Resistors

New Battery Pack
3S2P (2200mAH)

Parallel routing

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

include charger boost function

Using Kevin connection for layout

Place this cap close to IC

Place this cap close to EC

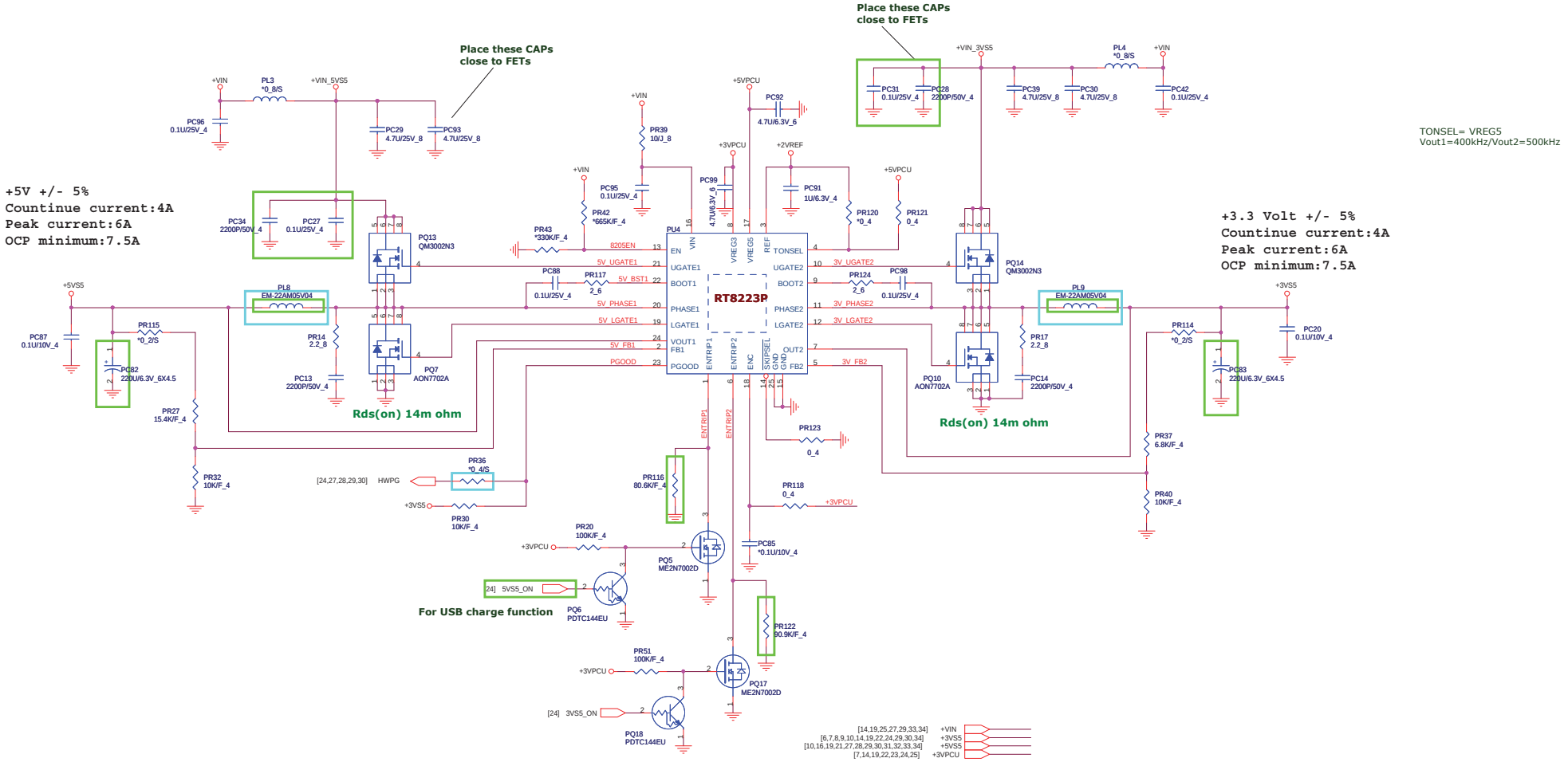
Place this cap close to EC

PU1
OZ8682

EMI Suggestion

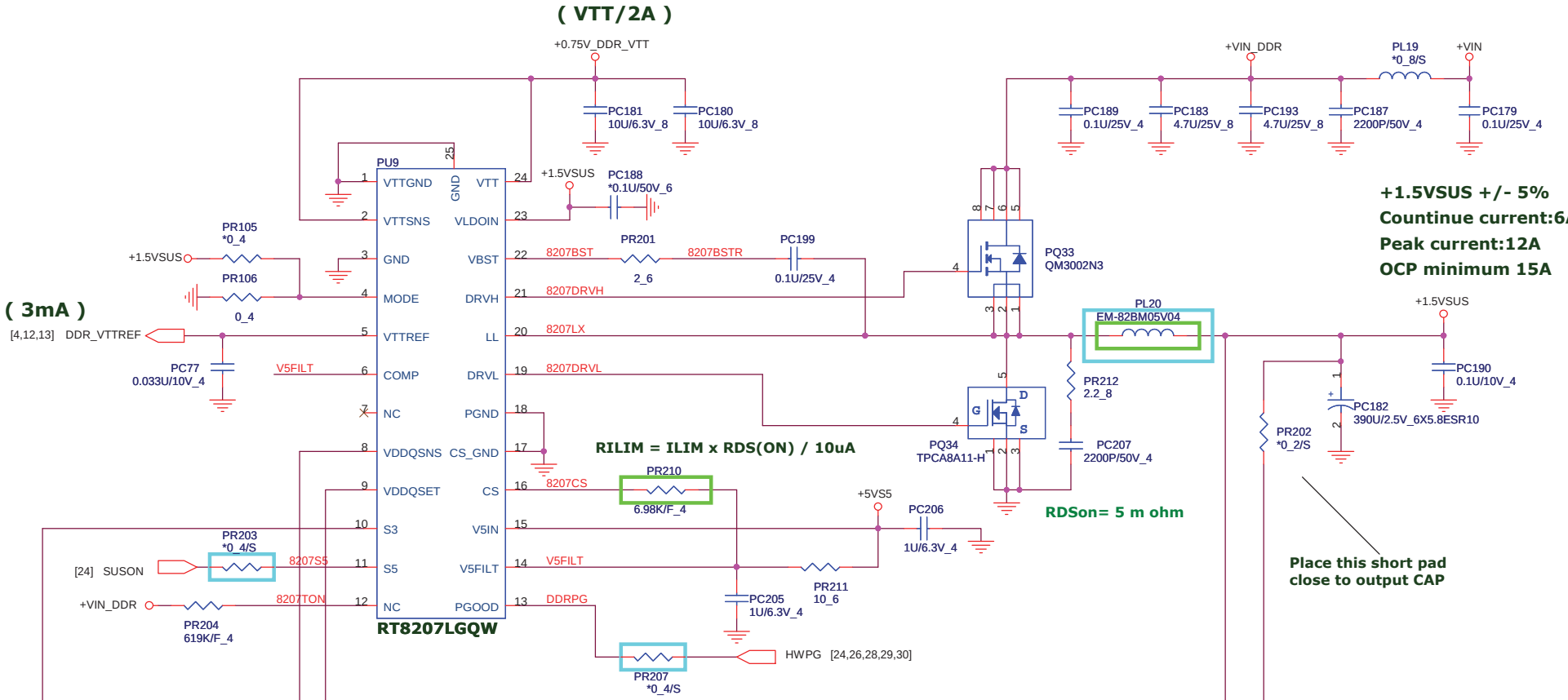


| | |
|---|---|
| PROJECT : JW2 | Quanta Computer Inc. |
| NB5 | Size: Custom; Document Number: 25 -- Charger (OZ8682); Rev: 1A |
| Date: Tuesday, February 07, 2012 | Sheet 25 of 34 |





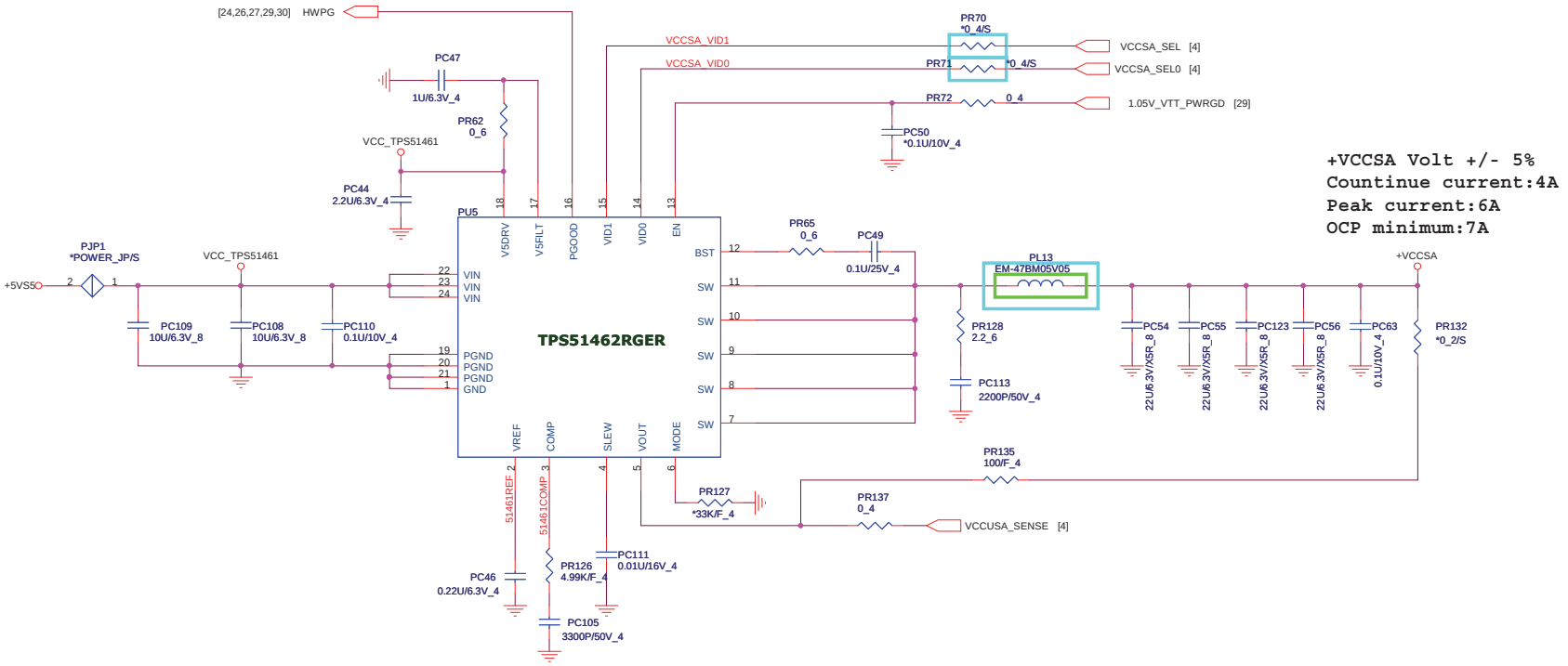

| | | |
|---|---|---|
| NB5 | PROJECT : JW2<br>Quanta Computer Inc. | |
| Size C | Document Number 26 -- 3/5VS5 (RT8223P) | Rev 1A |
| Date: Tuesday, February 07, 2012 | Sheet 26 of 34 | |




| | | |
|---|---|---|
| NB5 | PROJECT : JW2<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: 27 -- DDR3 (RT8207) | Rev: 1A |
| Date: Tuesday, February 07, 2012 | Sheet 27 of 34 | |

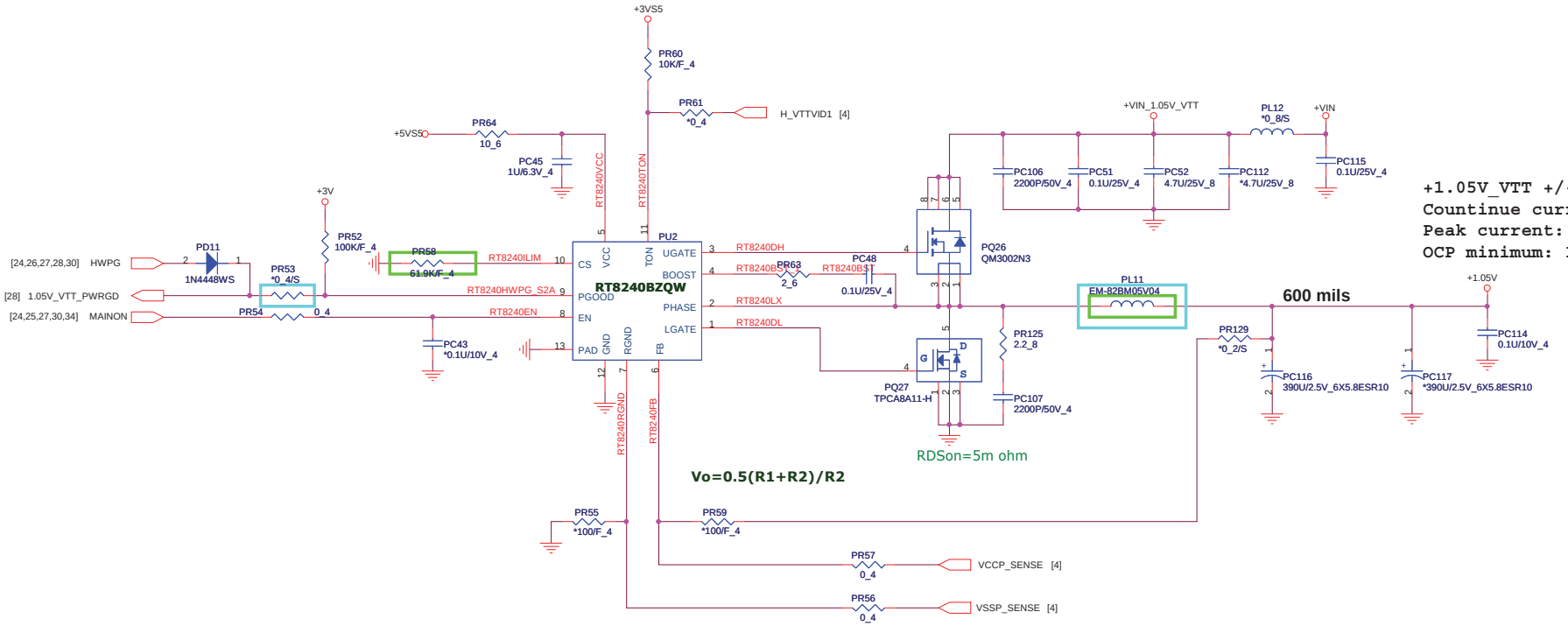
**CPU system agent**
**voltage slew rate of 0.5 -10 mV/µs**

| SEL0 | SEL1 | +VCCSA |
|---|---|---|
| 0 | 0 | 0.9V |
| 0 | 1 | 0.8V |
| 1 | 0 | 0.725V |
| 1 | 1 | 0.675V |



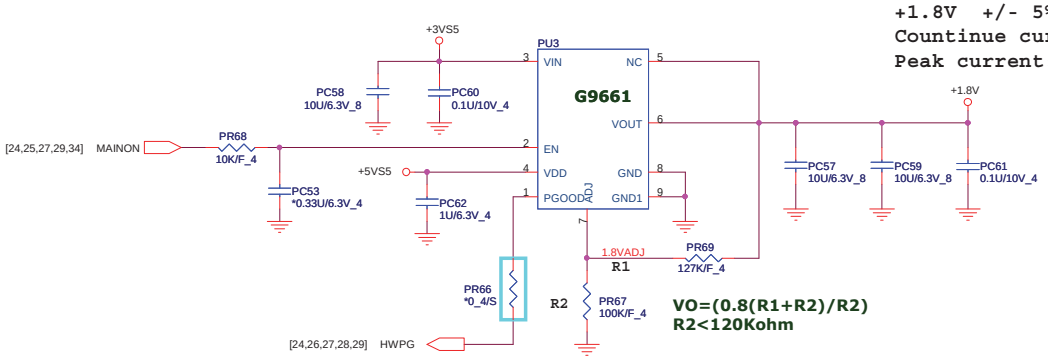

+VCCSA Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7A

| | | |
|---|---|---|
| NB5 | **PROJECT : JW2**<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: 28 – +VCCSA (TPS51462RGER) | Rev: 1A |
| Date: Tuesday, February 07, 2012 | Sheet 28 of 34 | |



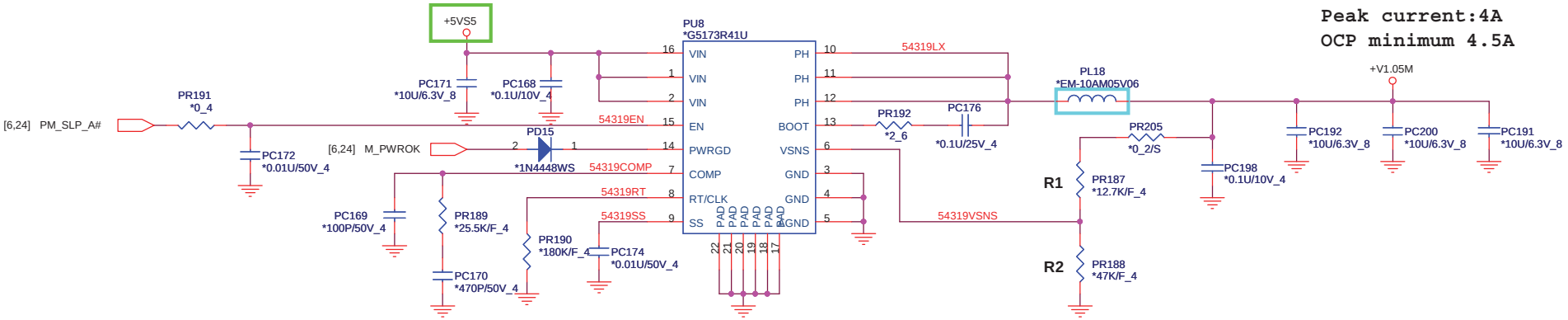

+1.05V_VTT +/- 5%
Countinue current:10A
Peak current: 12A
OCP minimum: 14.5A

| | | |
|---|---|---|
| NB5 | **PROJECT : JW2**<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: 29 -- +1.05V_VTT(RT8240B) | Rev: 1A |
| Date: Tuesday, February 07, 2012 | Sheet 29 of 34 | |




| | | |
|---|---|---|
| NB5 | PROJECT : JW2<br>Quanta Computer Inc. | |
| Size: Custom | Document Number: 30 – +1.8V (G9661) | Rev: 1A |
| Date: Tuesday, February 07, 2012 | Sheet 30 of 34 | |

+V1.05M +/- 5%
Countinue current:3A
Peak current:4A
OCP minimum 4.5A



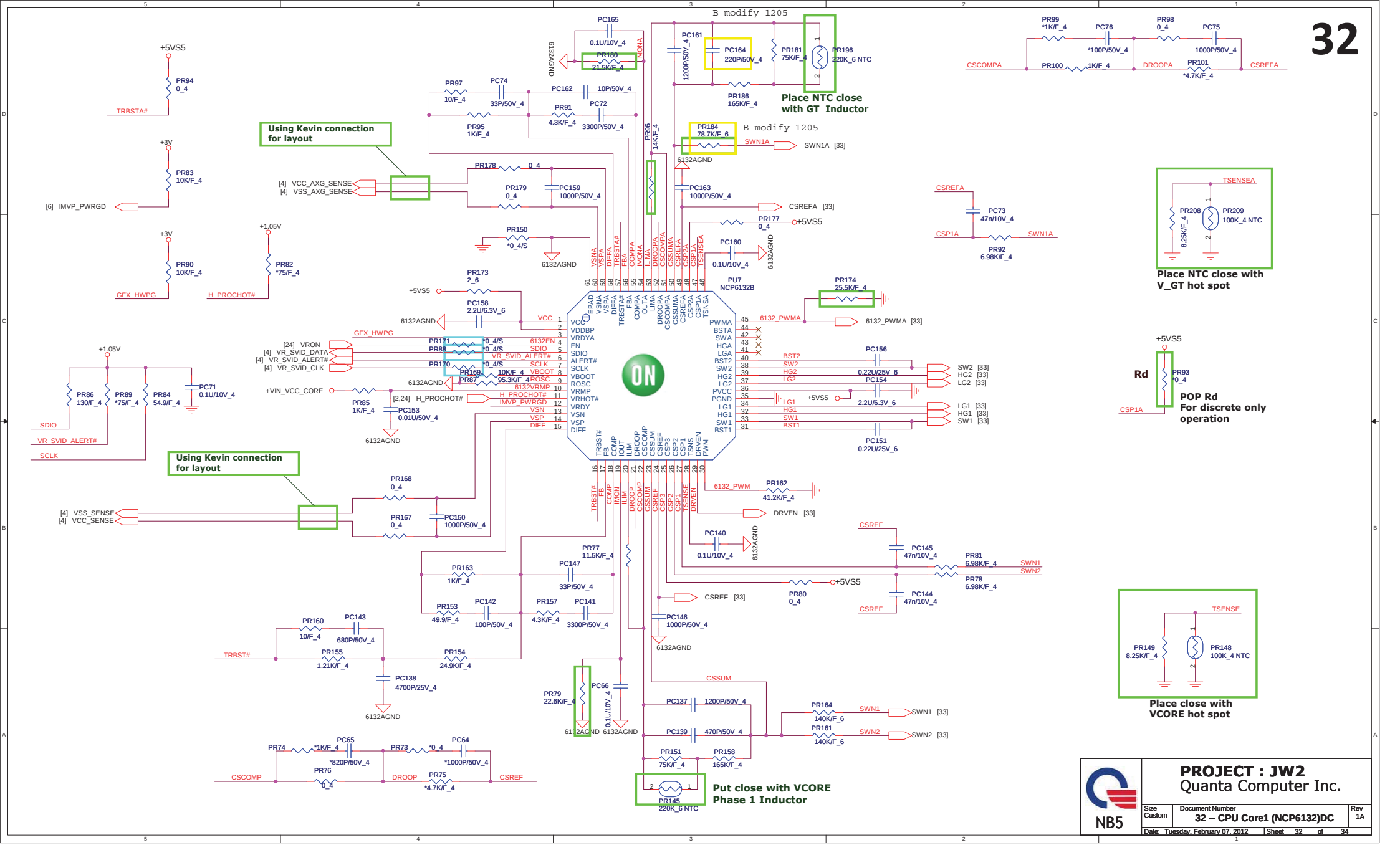

V0=0.827*(R1+R2)/R2

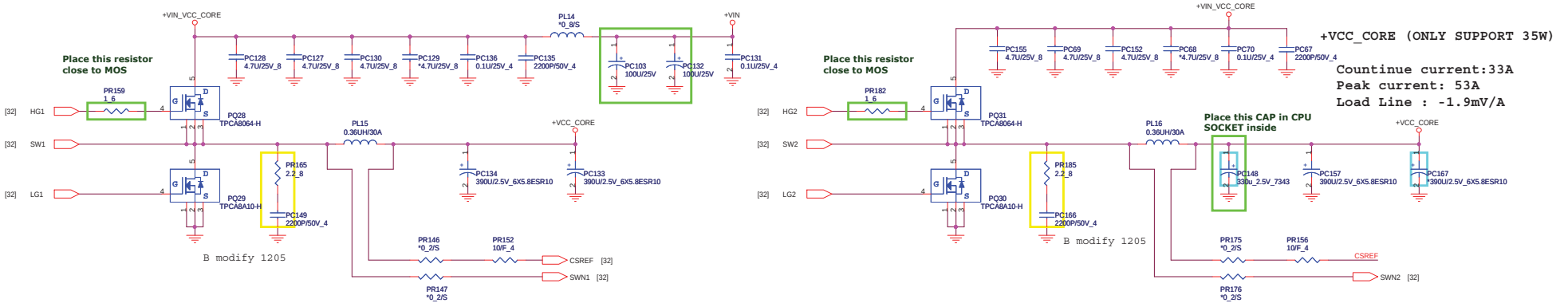
**PROJECT : JW2**
Quanta Computer Inc.

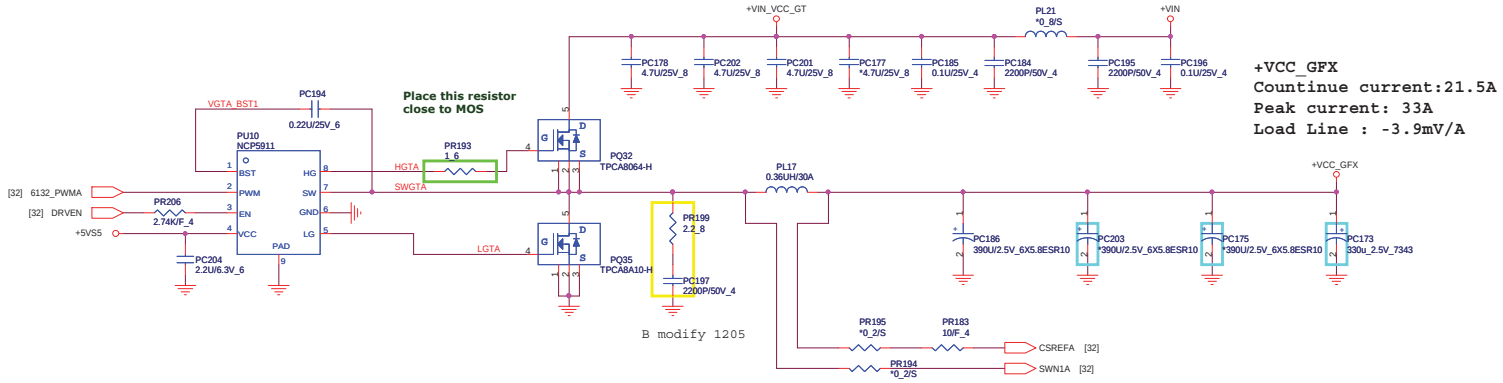
NB5

| Size | Document Number | Rev |
|---|---|---|
| B | 31 -- +V1.05M (G5173) | 1A |

Date: Tuesday, February 07, 2012 | Sheet 31 of 34

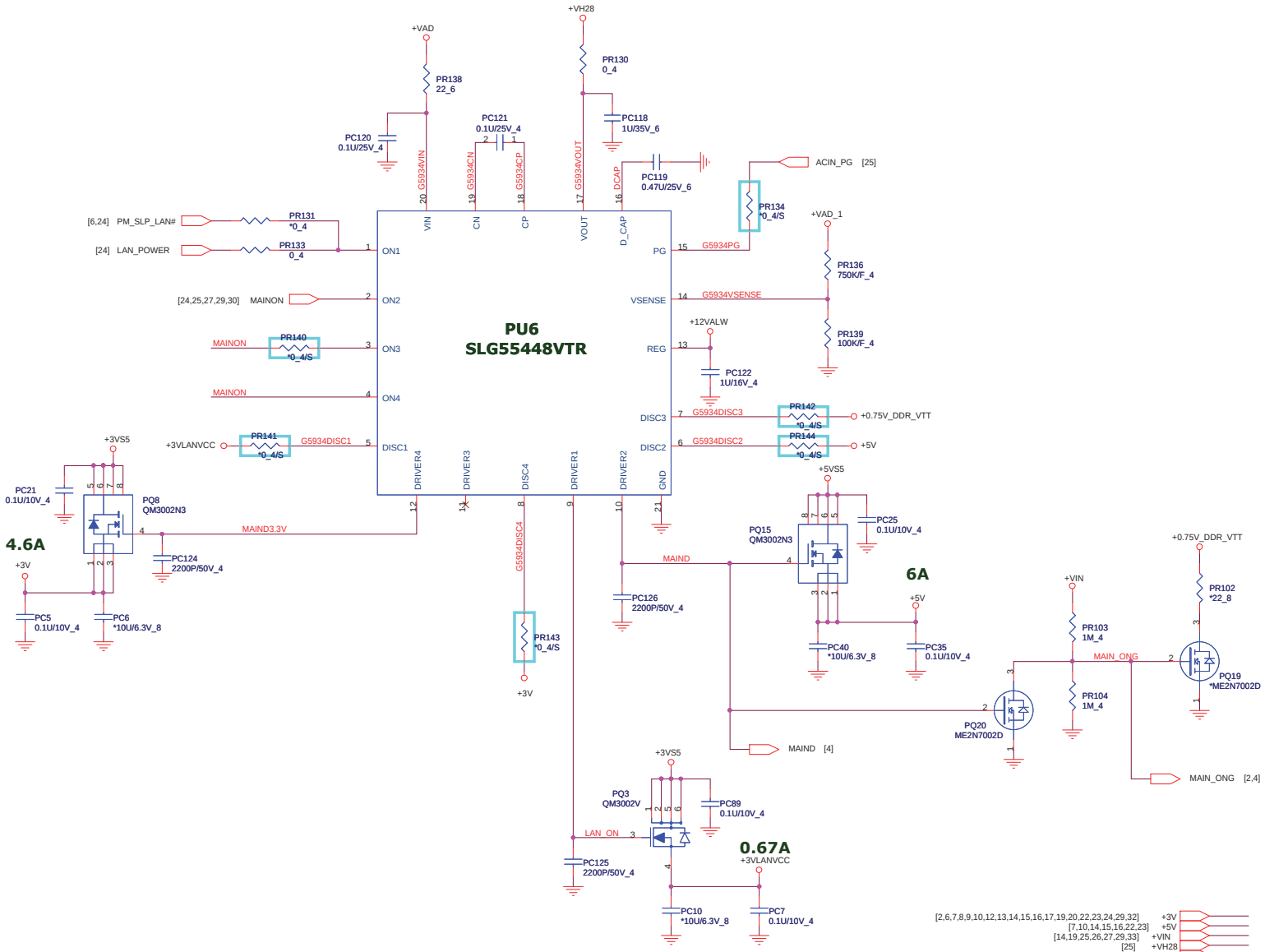







| | | |
|---|---|---|
| NB5 | PROJECT : JW2<br>Quanta Computer Inc. | |
| Size C | Document Number<br>33 -- CPU Core2 (NCP5911)DC | Rev 1A |
| Date: Tuesday, February 07, 2012 | Sheet 33 of 34 | |






NB5

**PROJECT : JW2**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| Custom | 34 -- Dis-charge IC (SLG55448V) | 1A |
| Date: Tuesday, February 07, 2012 | Sheet 34 of 34 | |