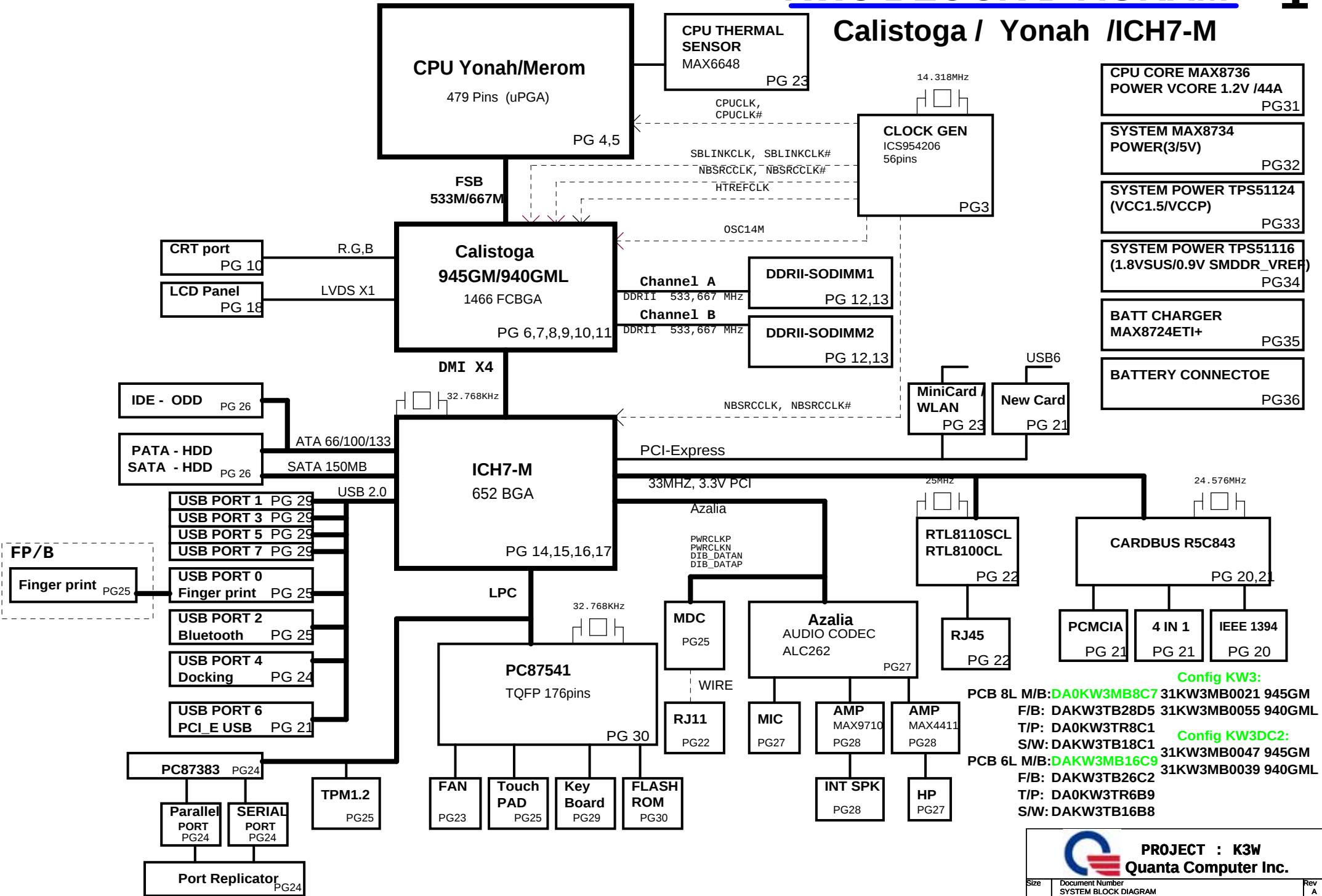


1

Calistoga / Yonah / ICH7-M



Voltage Rails

Voltage Rails		ON S0-S2	ON S3	ON S4	ON S5	Ctl Signal
VCC_CORE	Core voltage for Processor	X				VR_ON
GMCH_VTT	Core voltage for CPU / NB	X				MAINON
SMDDR_VREF	0.9V for DDR2 Termination voltage	X				MAINON
VMEM_VTT	1.25V for VRAM Termination voltage	X				MAINON
RVCC3		X	X	X		RVCCD
VCC1.5		X				MAINON
VCC1.8		X				MAINON
VCC2.5		X				MAINON
VCC3		X				MAIND
VCC5		X				MAIND
1.8VSUS		X	X			SUSON
3VSUS		X	X			SUSD
5VSUS		X	X			SUSD
3VPCU		X	X	X	X	VL
5VPCU		X	X	X	X	VL
9VPCU		X	X	X	X	5VPCU

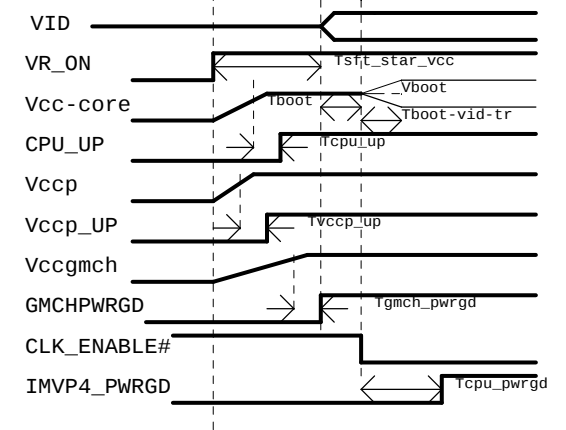
PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 6 : SVCC
LAYER 6 : BOT

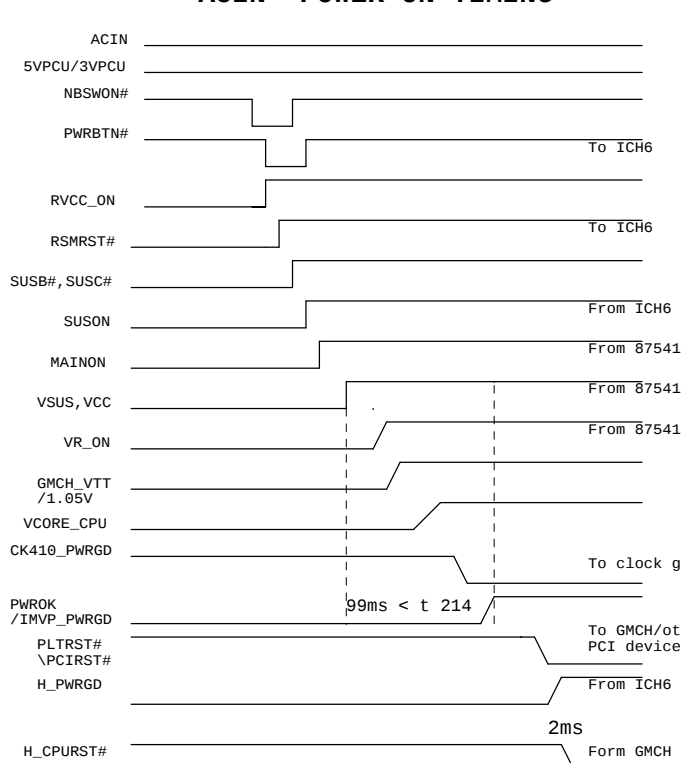
PCI DEVICES IRQ ROUTING

K3W PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
RTL Lan	AD16	REQ0# / GNT0#	INT D#
R5C843	AD23	REQ1# / GNT1#	INT A/B/C#

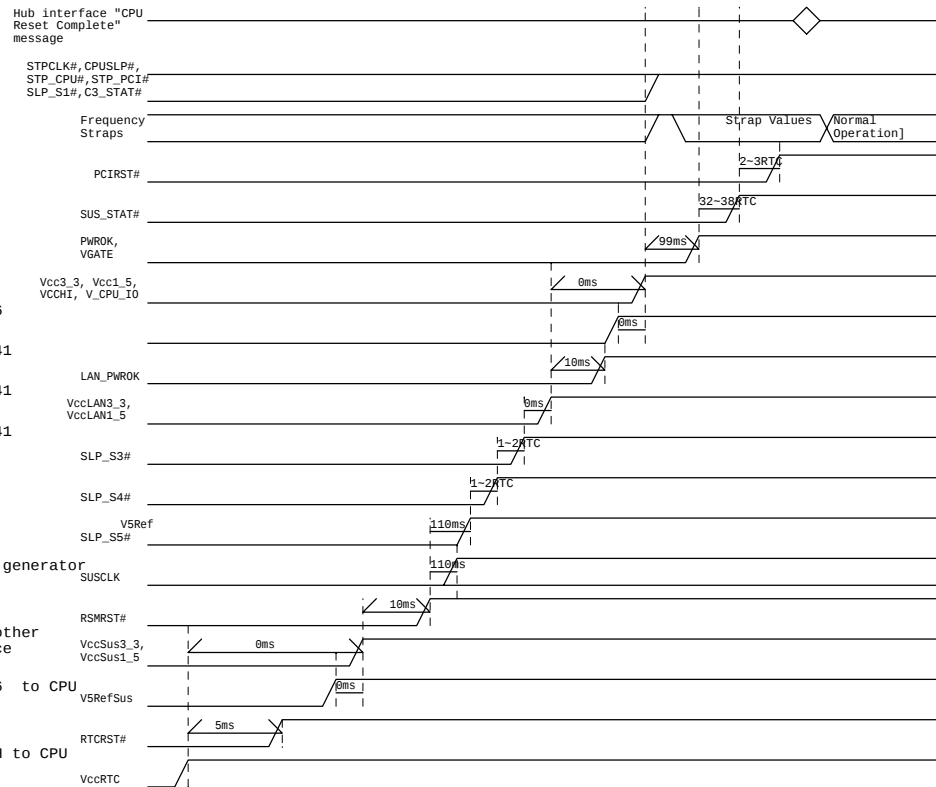
CPU Power On Sequence



ACIN POWER ON TIMING



Power Sequencing and Reset Signal Timings



Default

25 mils

VCC3

120 ohms@100Mhz

VDD_SRC_CPU

C74 0.1U/10V

C83 0.1U/10V

C82 0.1U/10V

C64 0.1U/10V

C87 10U

R69 2.2F VDD_A

C73 0.1U/10V

C80 10U

VCC3 (8,9,10,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,30,31,32)

GMCH_VTT (4,5,6,9,10,14,17,33)

Close to IC <500mils

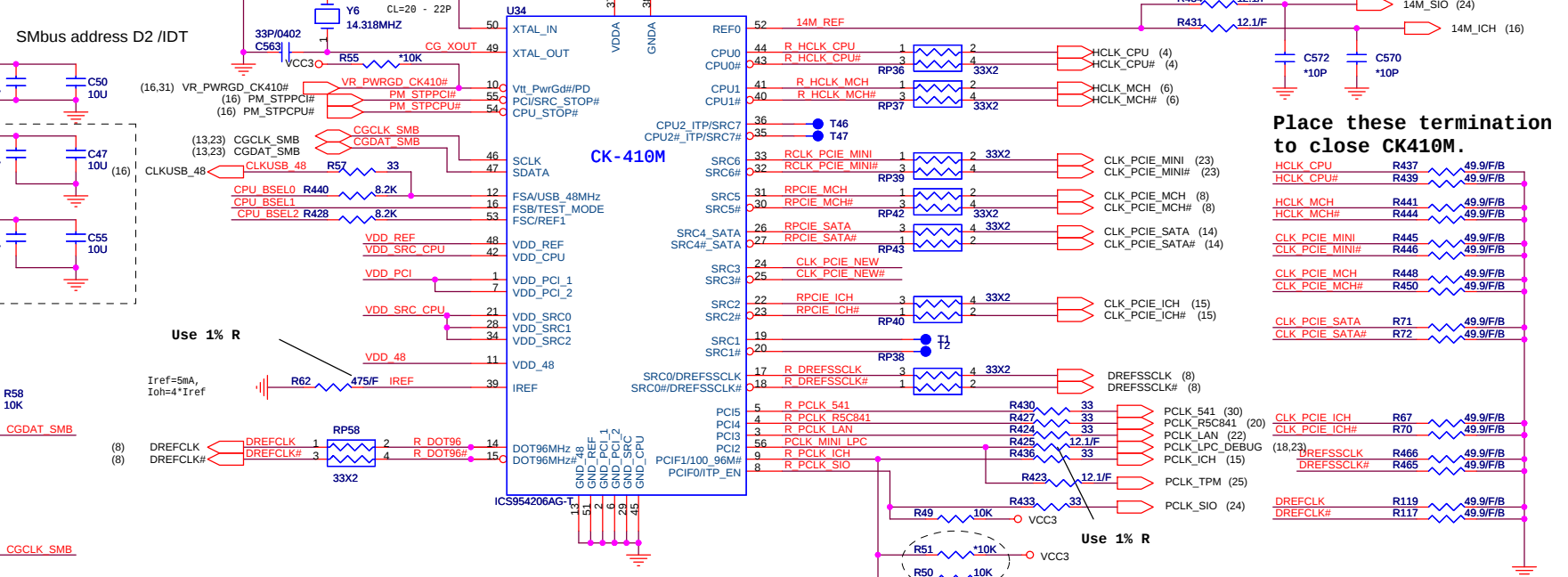
33P/0402 C564

CG_XIN

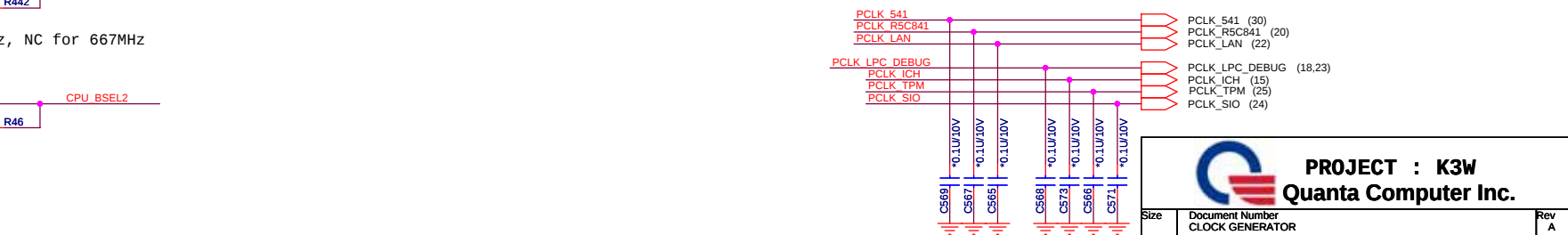
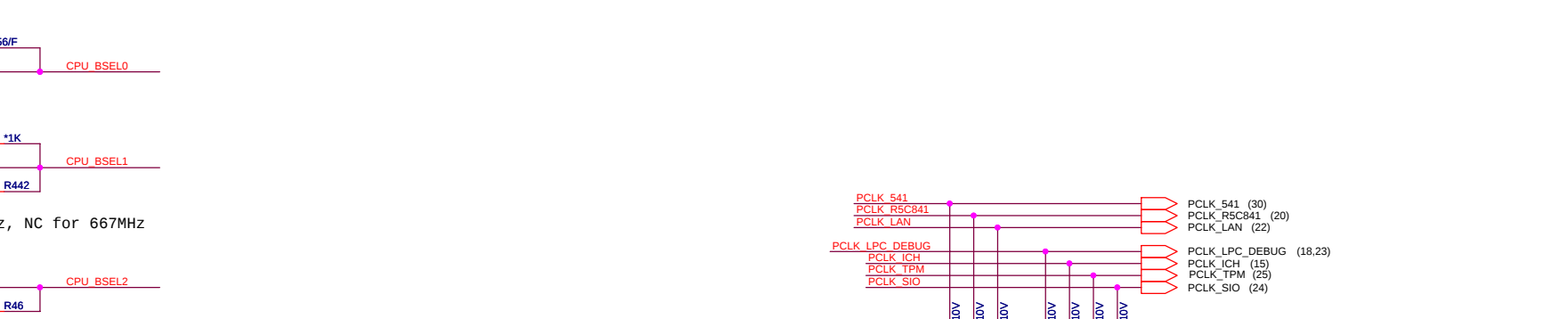
VDD_A

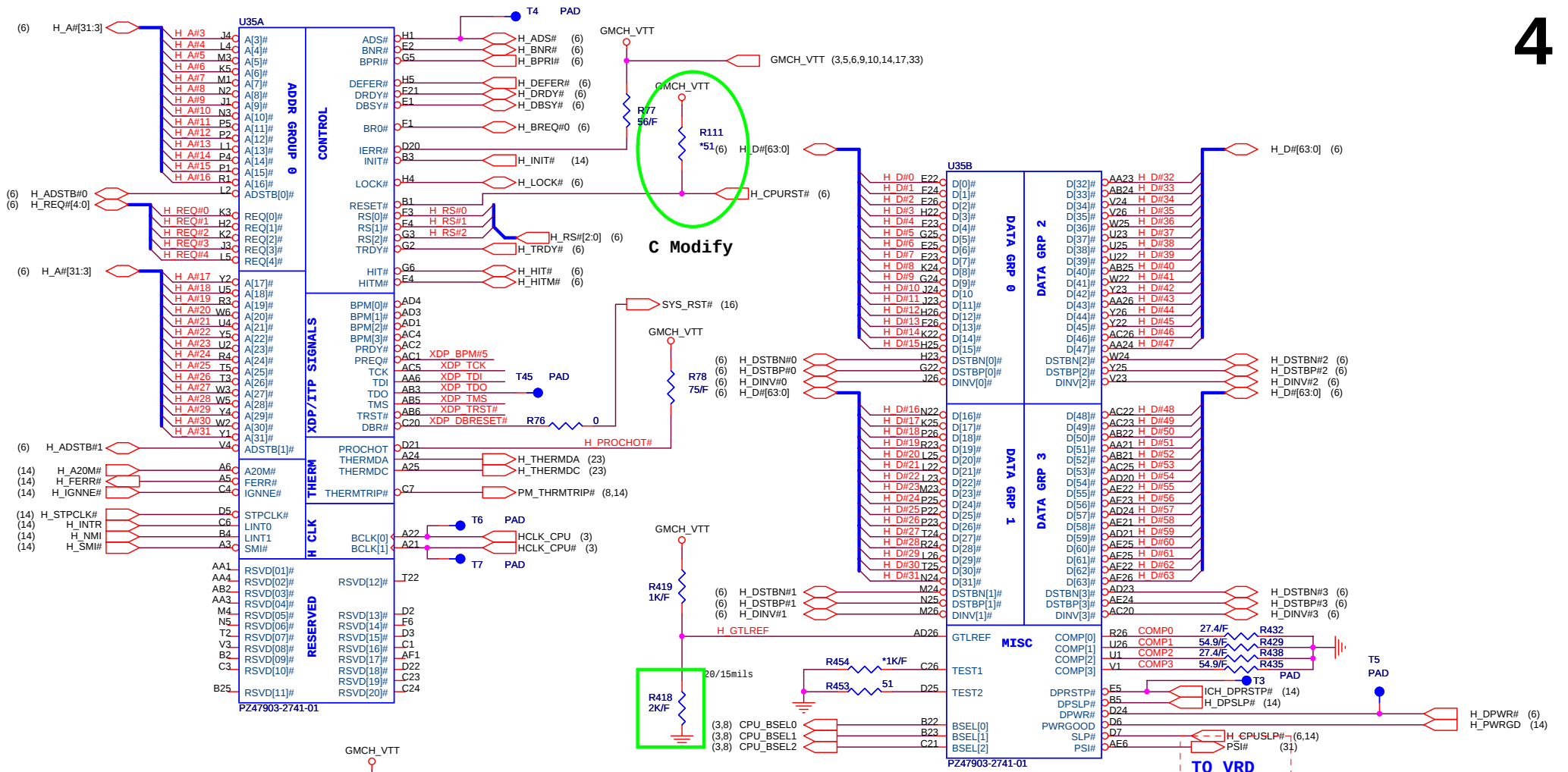
Place these termination to close CK410M.

R434 12 1/F



or 533MHz Moby Dick (Intel®915GM + Calistoga Interposer
7MHz board).





XDP PU_R < 0.2"

Why BMP5 need PH ?

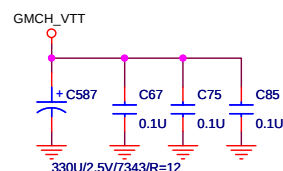
XDP_TCK PD 27.4/1% ?
 XDP_TRST PD 510ohm /5% ?
 XDP_TDI PU 150ohm /1.05V
 XDP_TMS PU 39.2/1%?
 XDP_TDO PU 54.9ohm?
 For ITP700

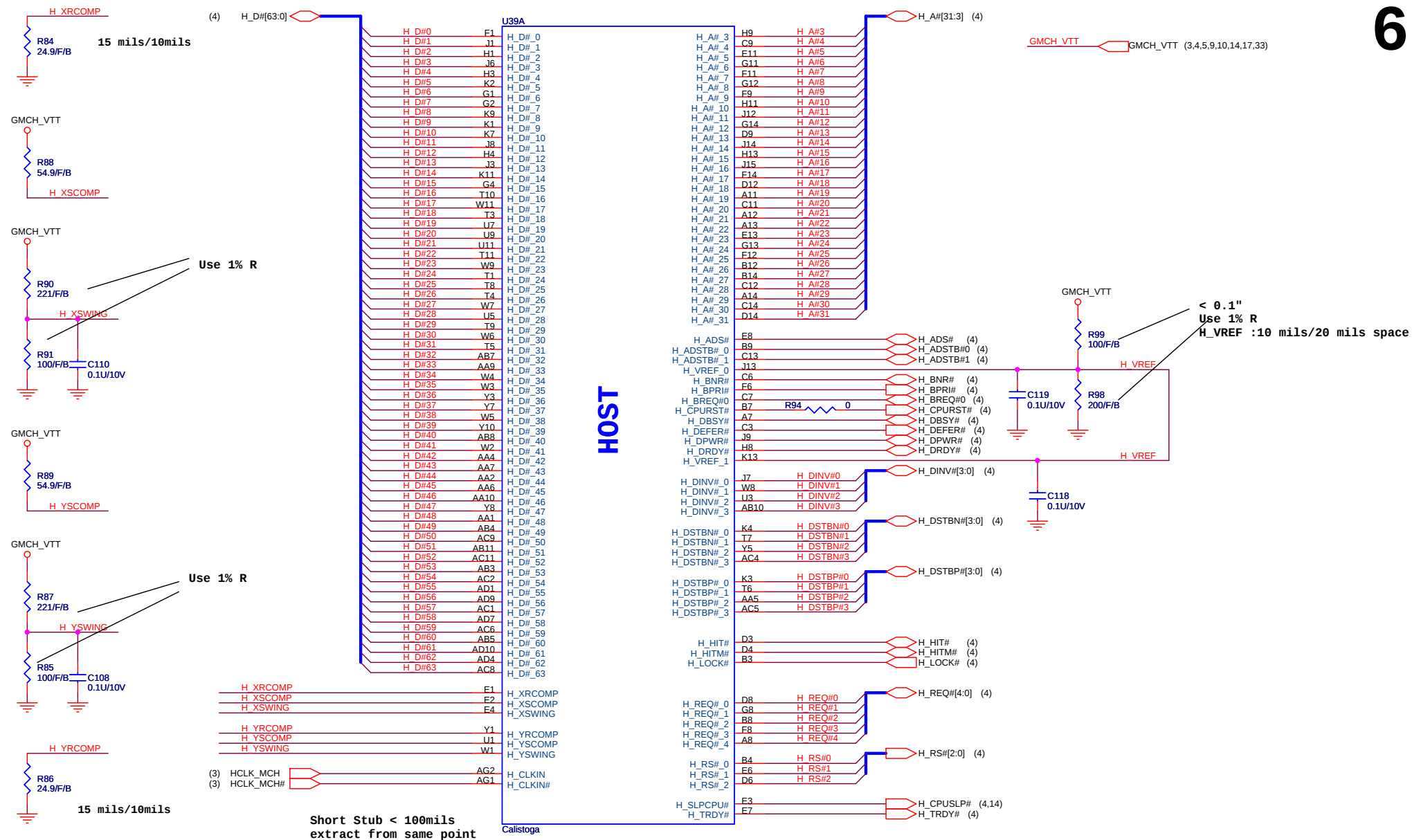
H_PWRGD is CMOS driving by ICH

PROJECT : K3W

Quanta Computer Inc.

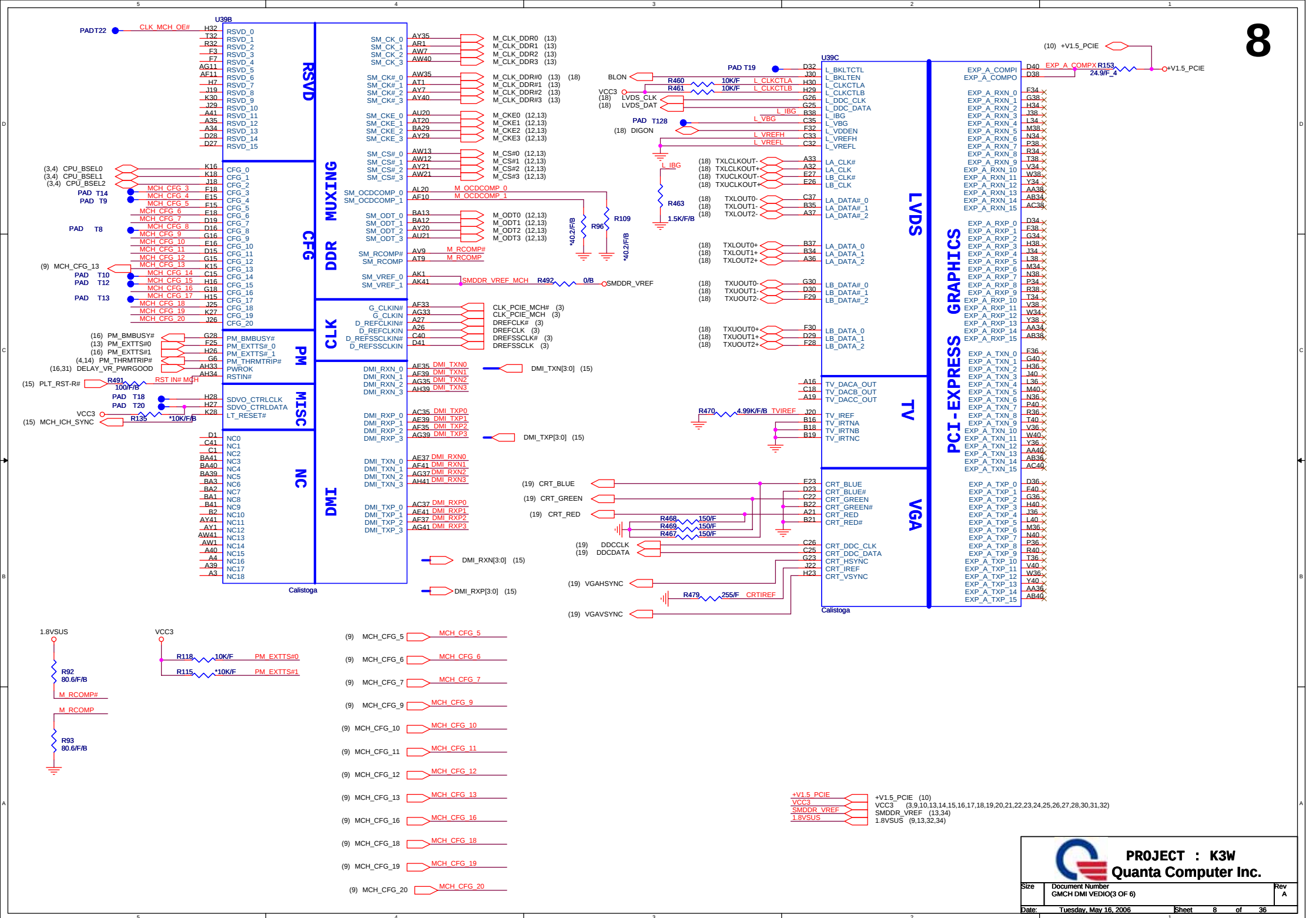
Size	Document Number CPU(HOST BUS)	Rev A
Date:	Tuesday, May 16, 2006	Sheet 4 of 36

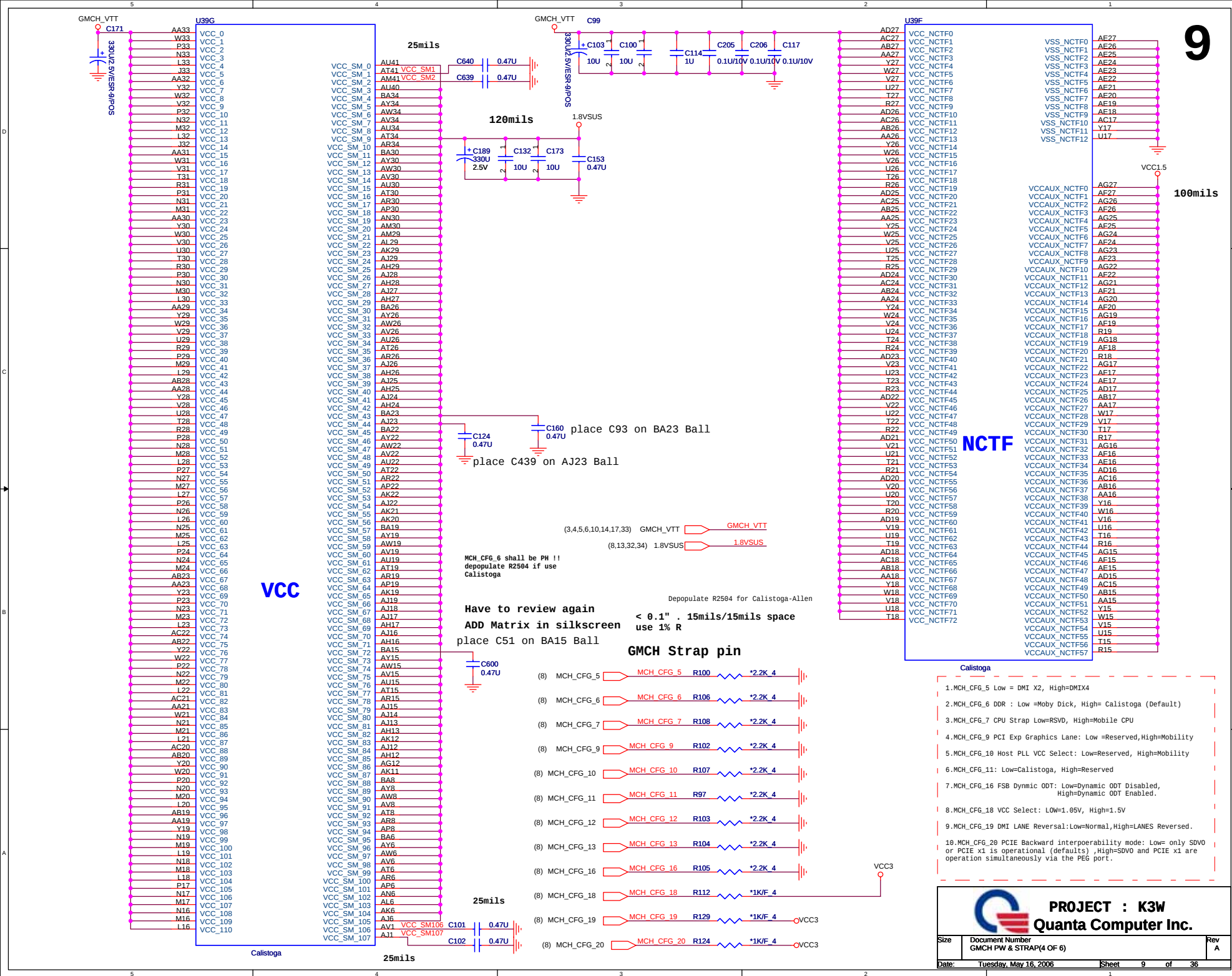


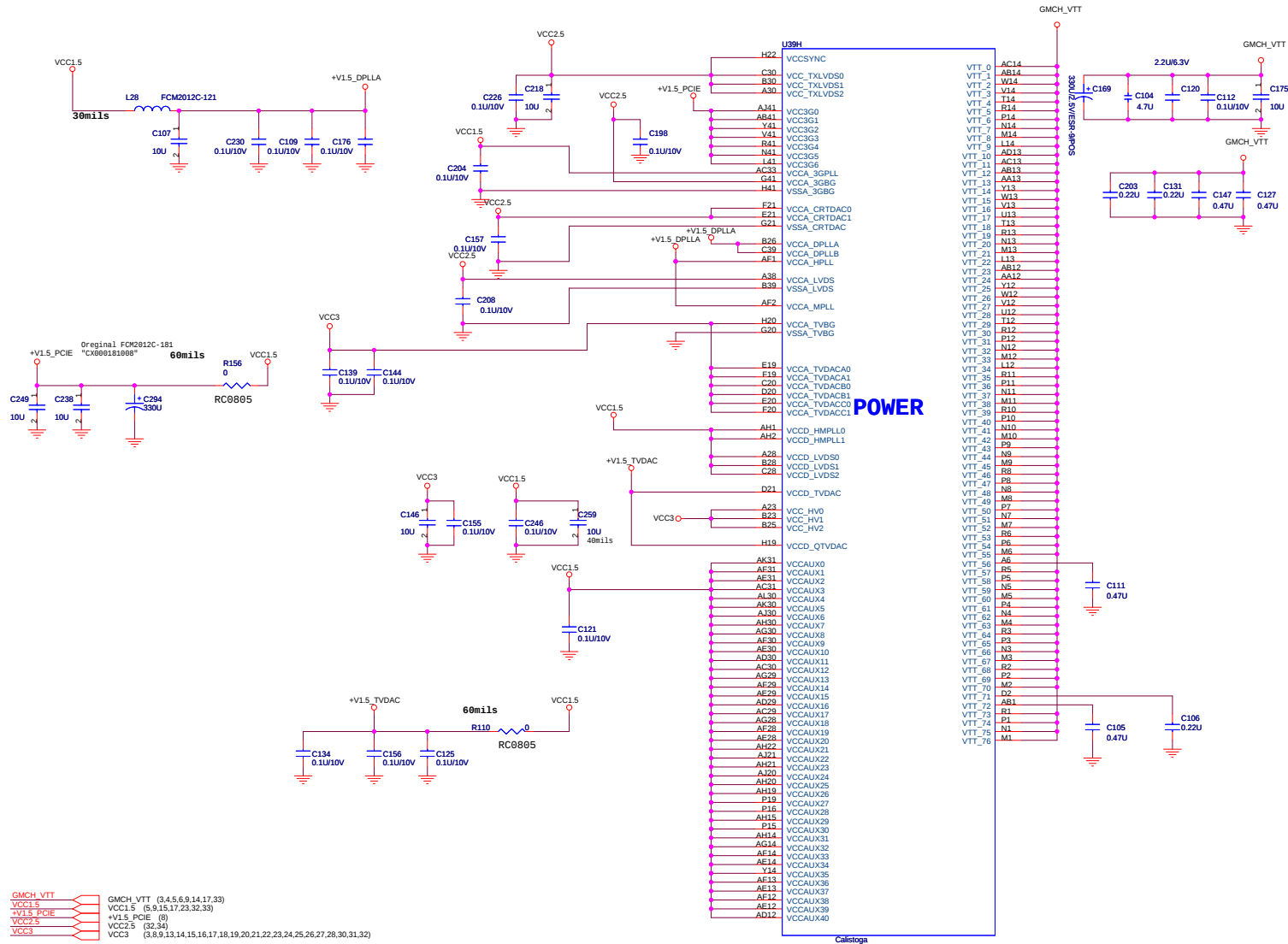


PROJECT : K3W
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH HOST(1 OF 6)	A
Date:	Tuesday, May 16, 2006	Sheet 6 of 36





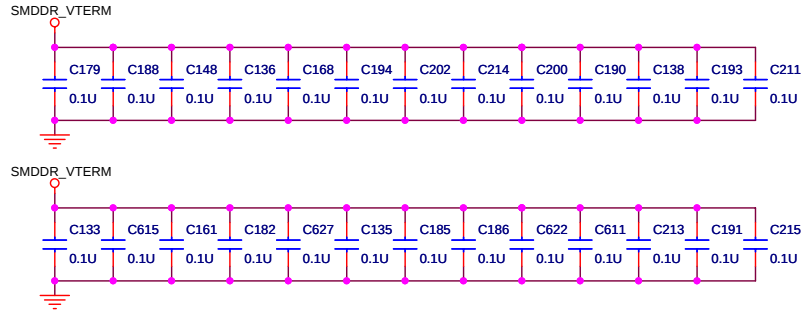
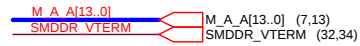




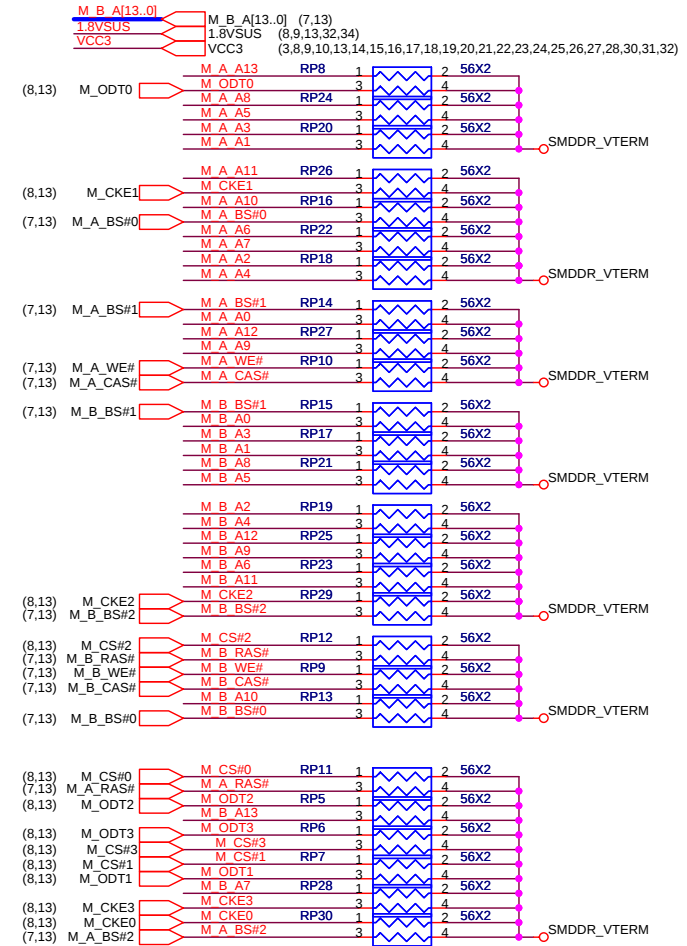
DDRII DUAL CHANNEL A, B.

12

DDRII A CHANNEL

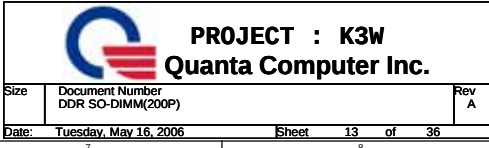


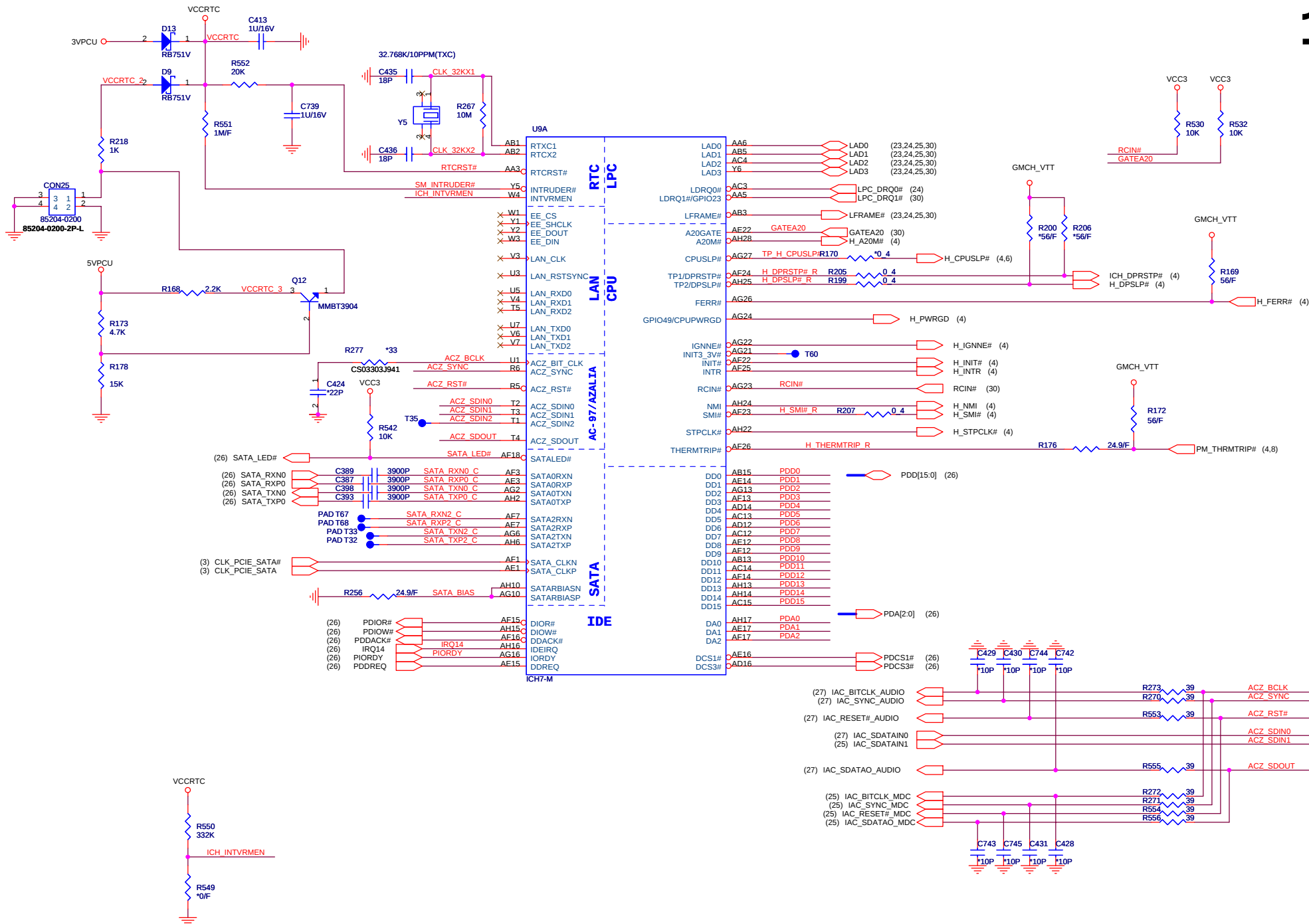
DDRII B CHANNEL



PROJECT : K3W
Quanta Computer Inc.

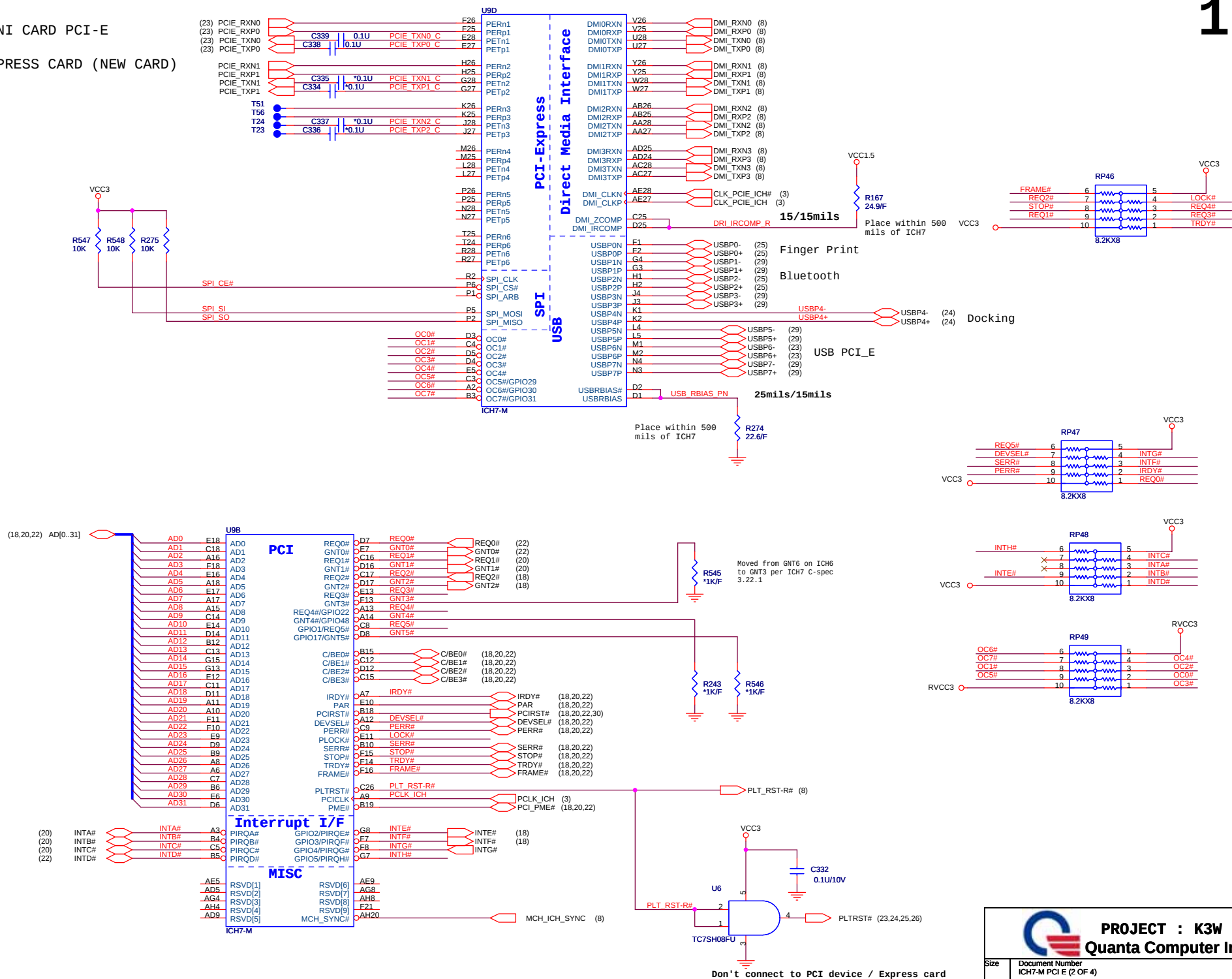
Size	Document Number DDR RES. ARRAY	Rev A
Date:	Tuesday, May 16, 2006	Sheet 12 of 36

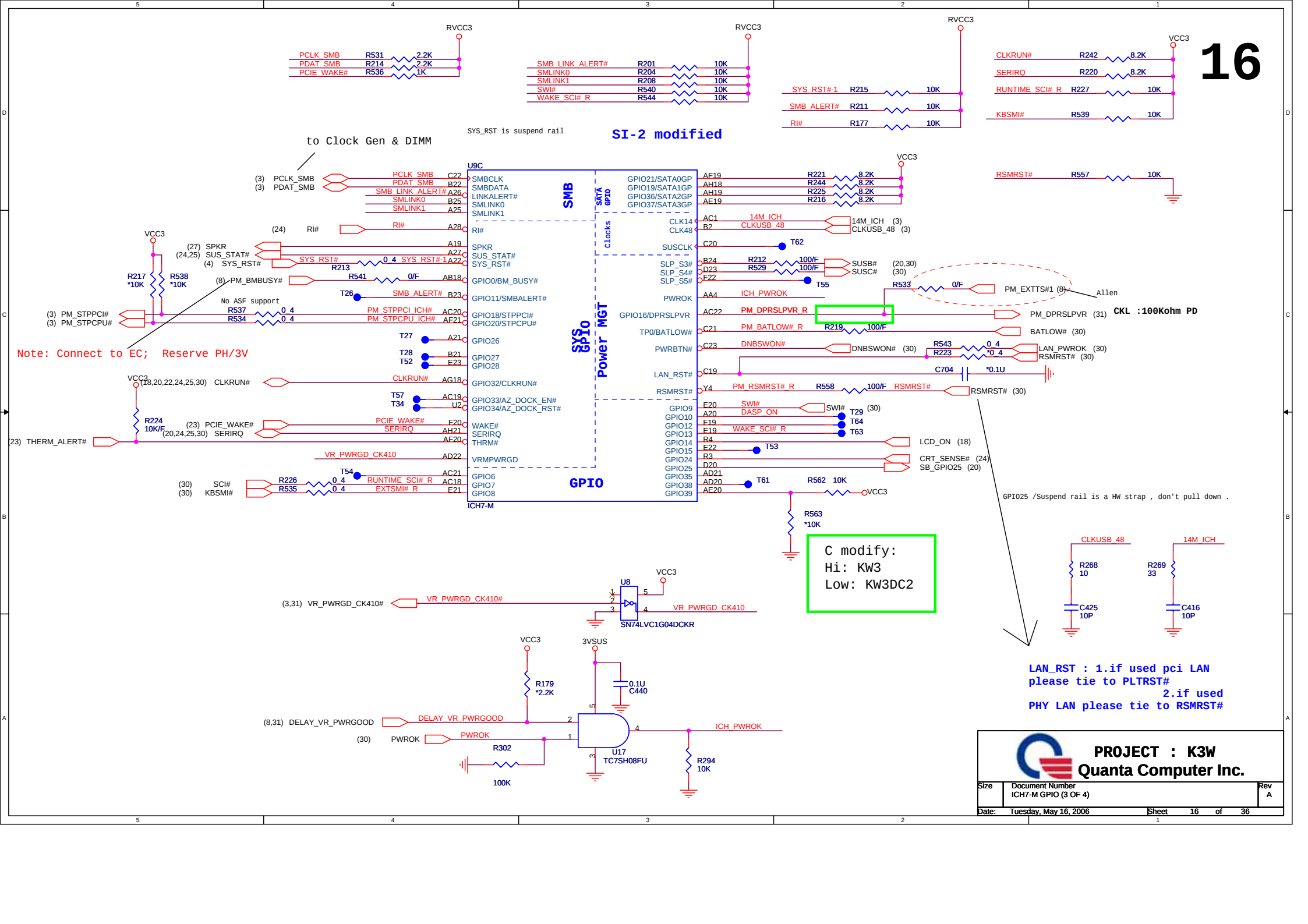


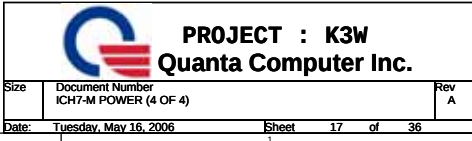


MINI CARD PCI-E

EXPRESS CARD (NEW CARD)

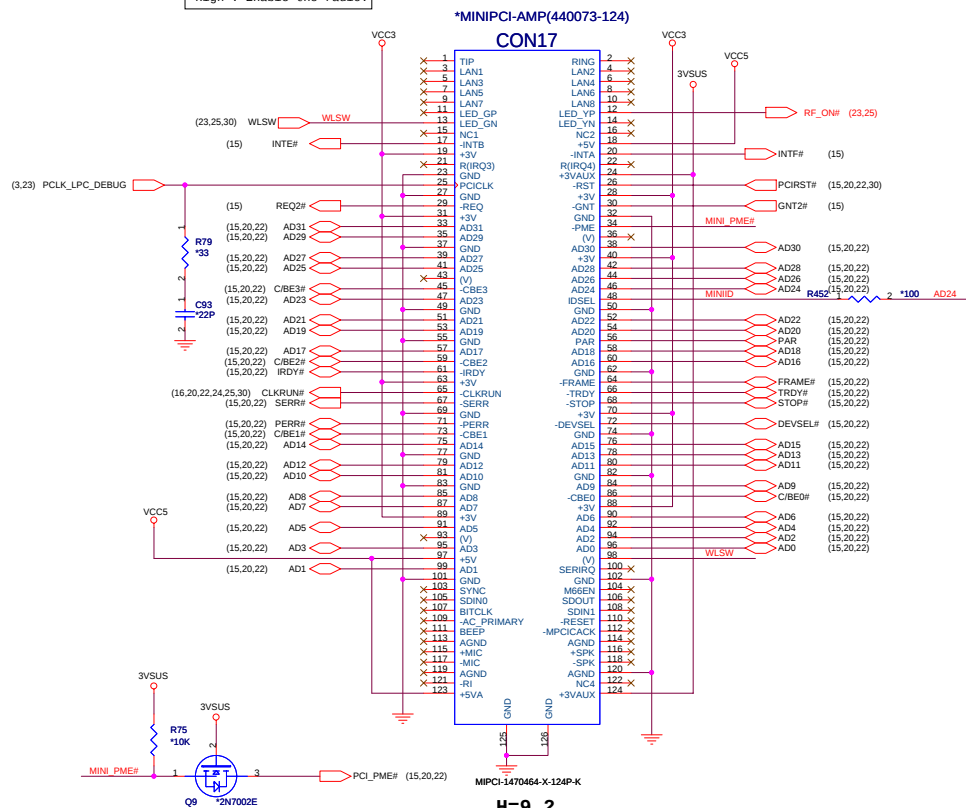




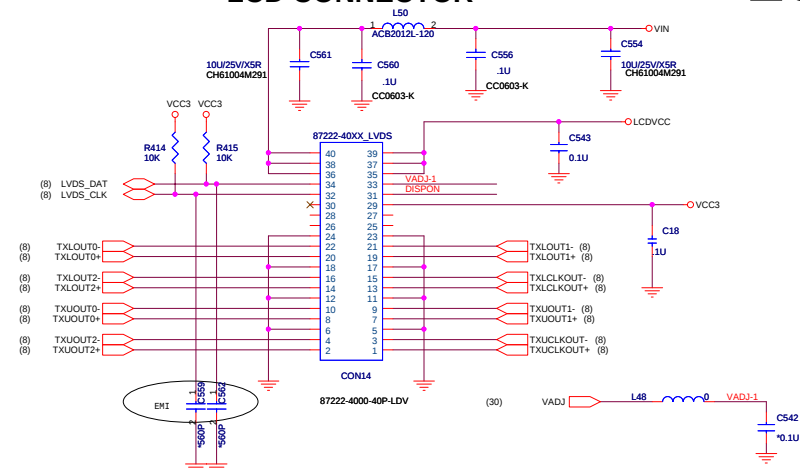


ID Select : AD24
 Interrupt Pin : INTE#, INTF#
 Request indicates : REQ2#
 Grant indicates : GNT2#

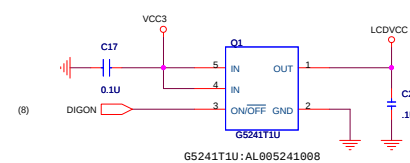
WLSW:
 Low : disable the radio.
 High : Enable the radio.



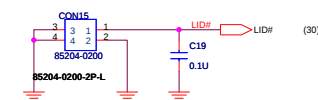
LCD CONNECTOR



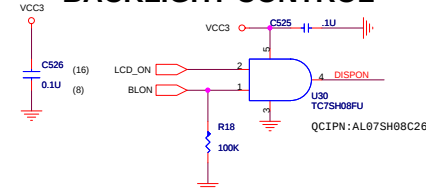
PANEL VCC CONTROL

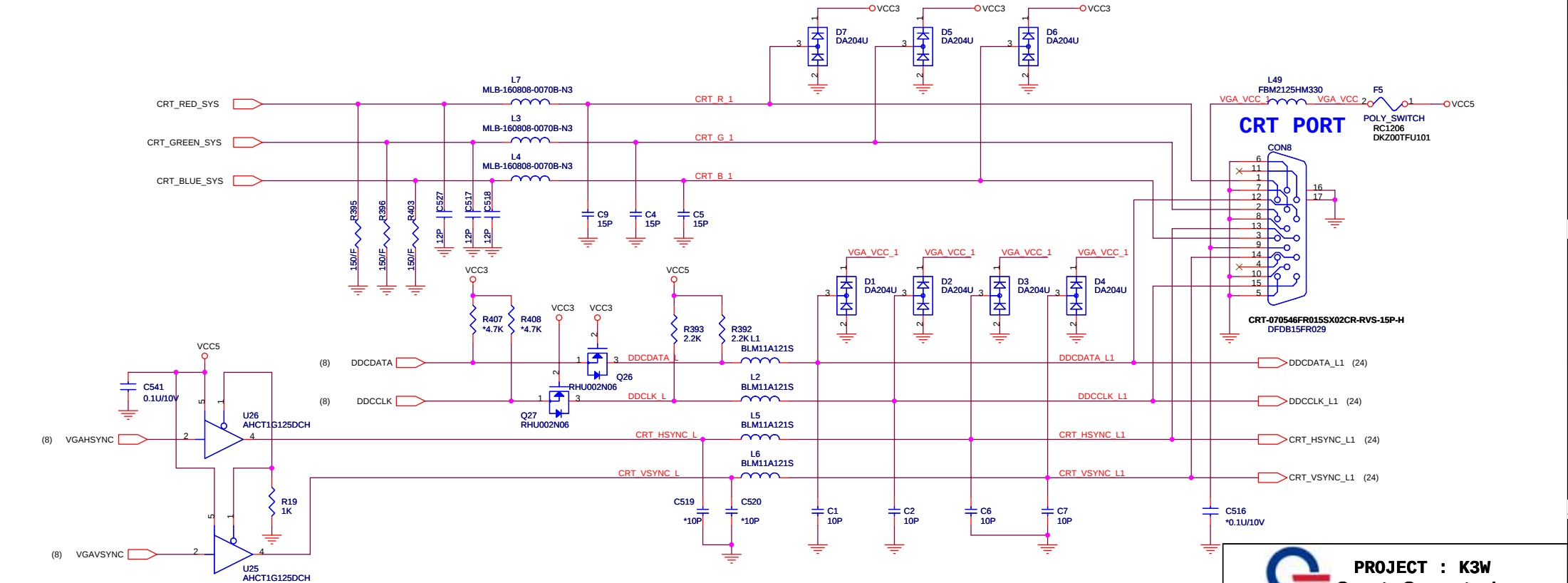
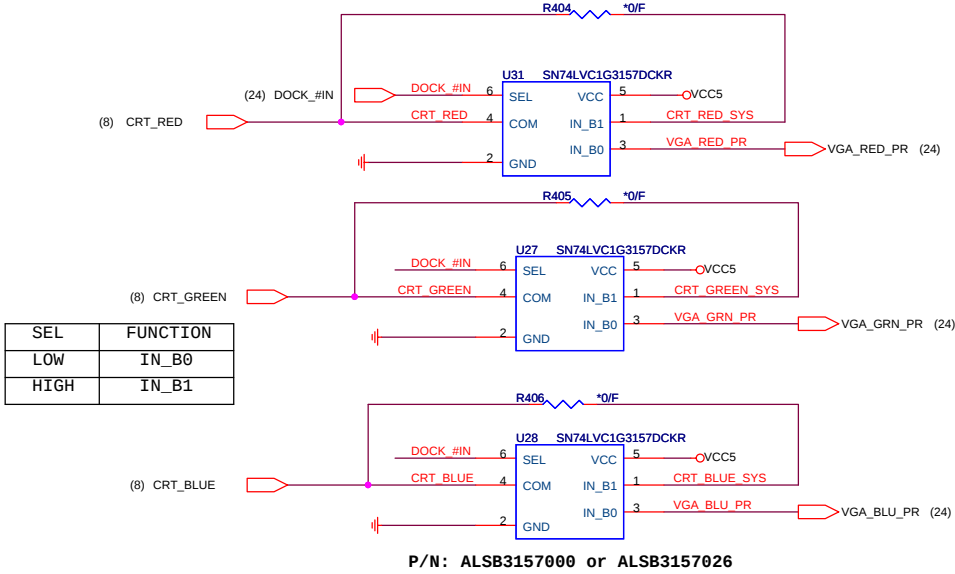


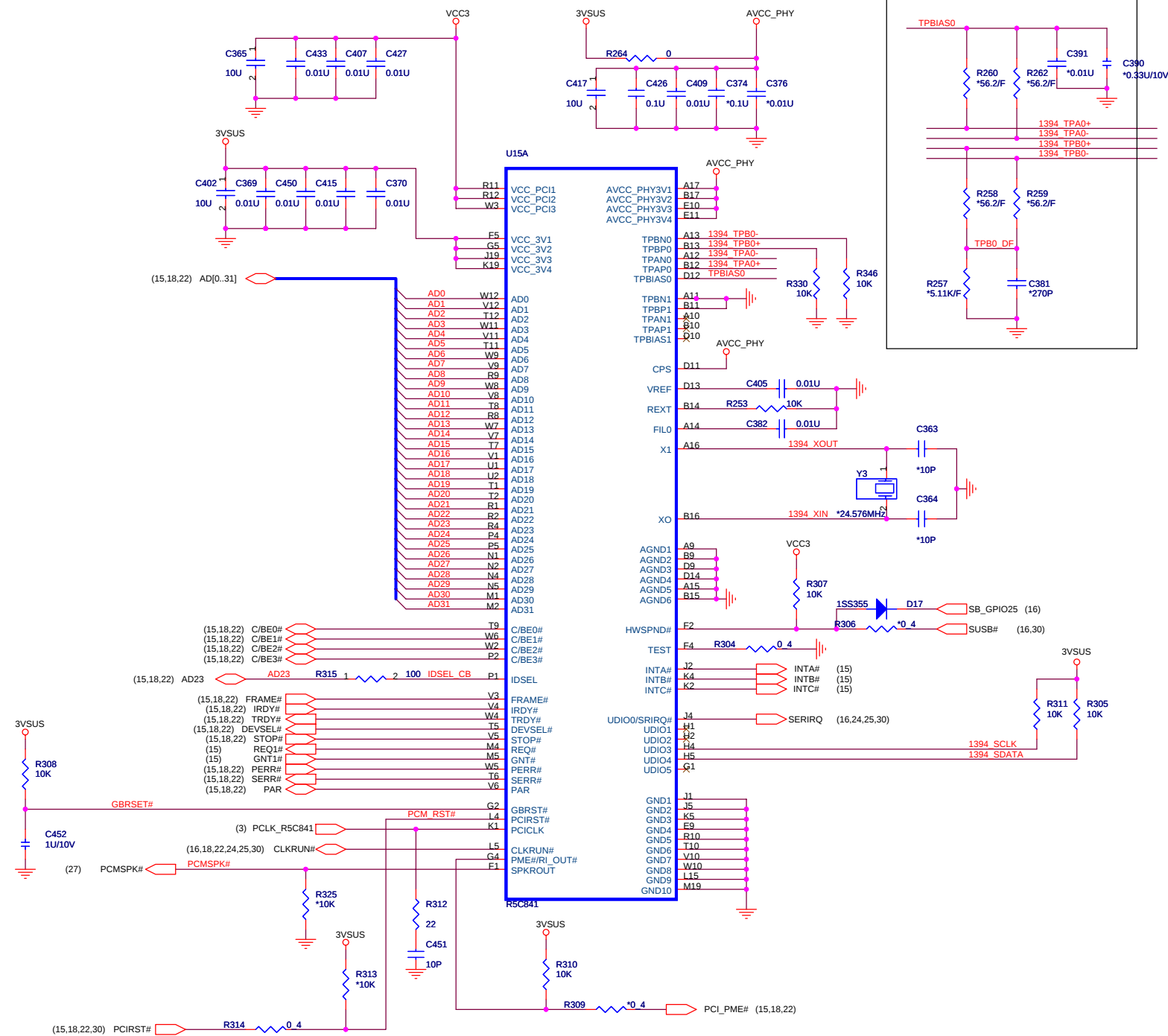
LID



BACKLIGHT CONTROL

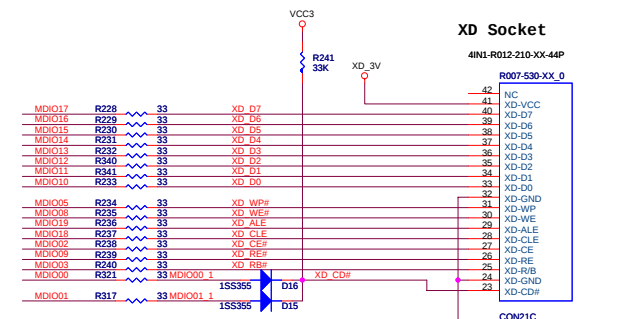
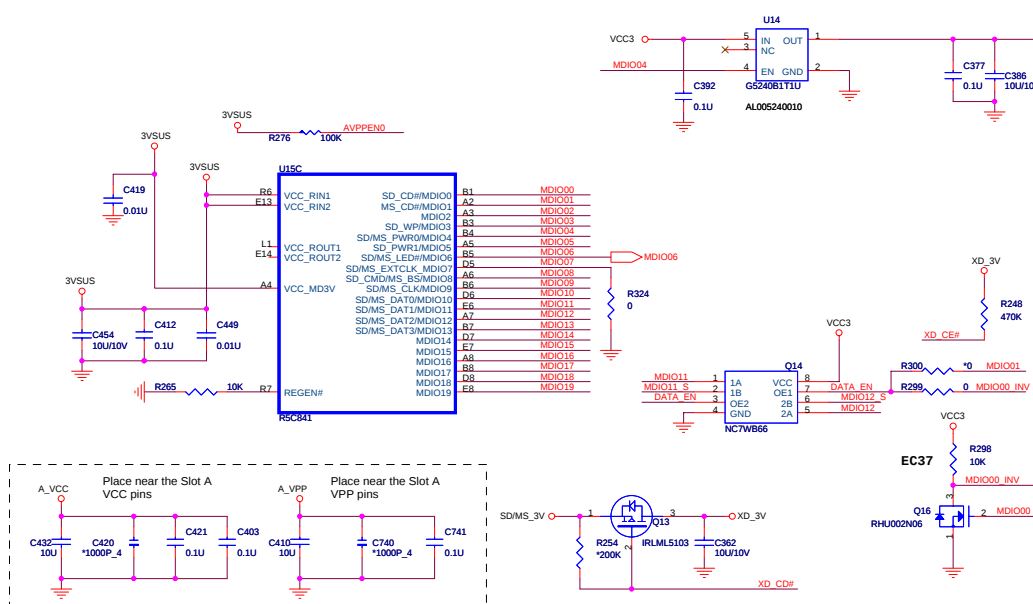
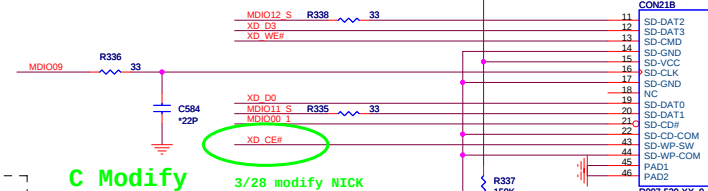
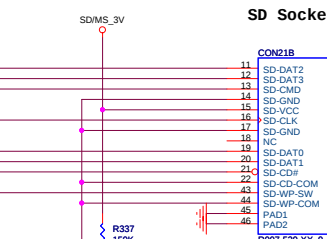
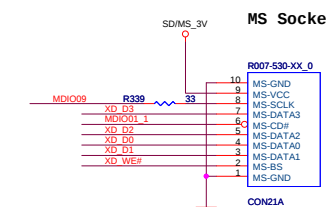
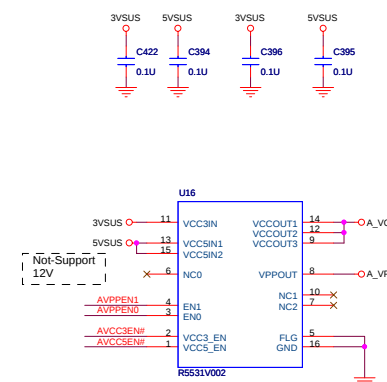
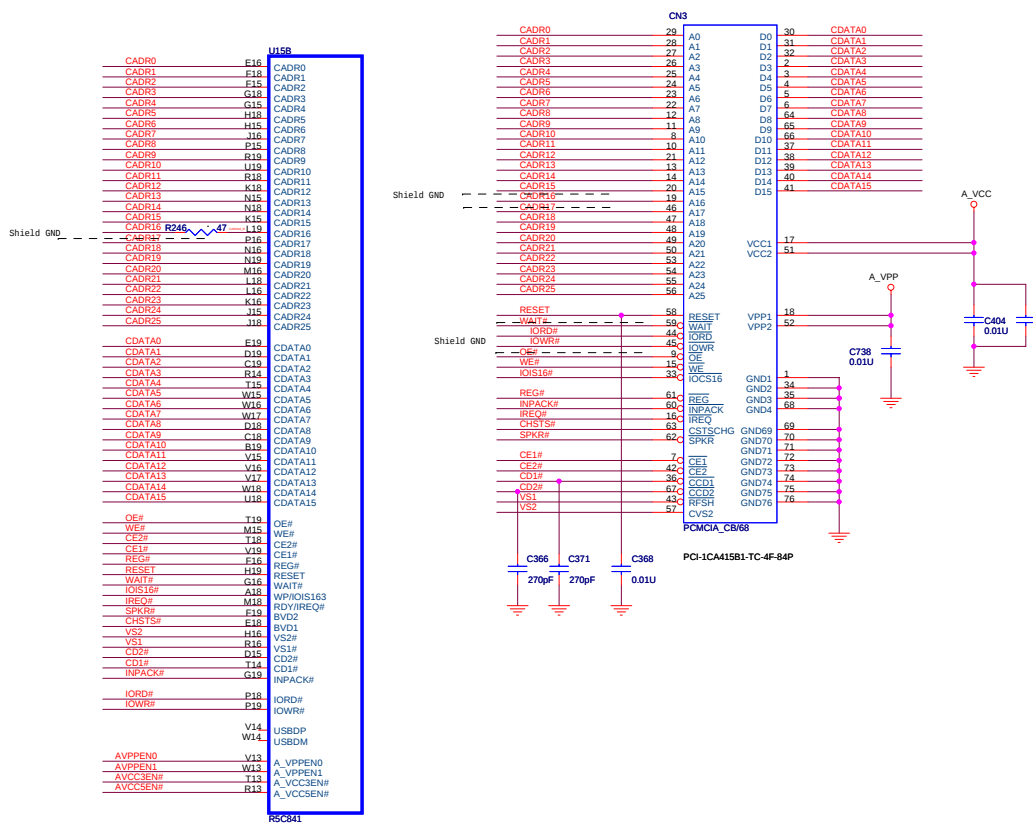


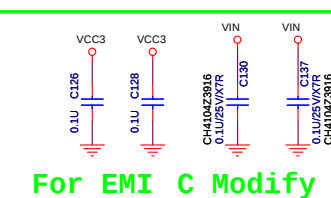
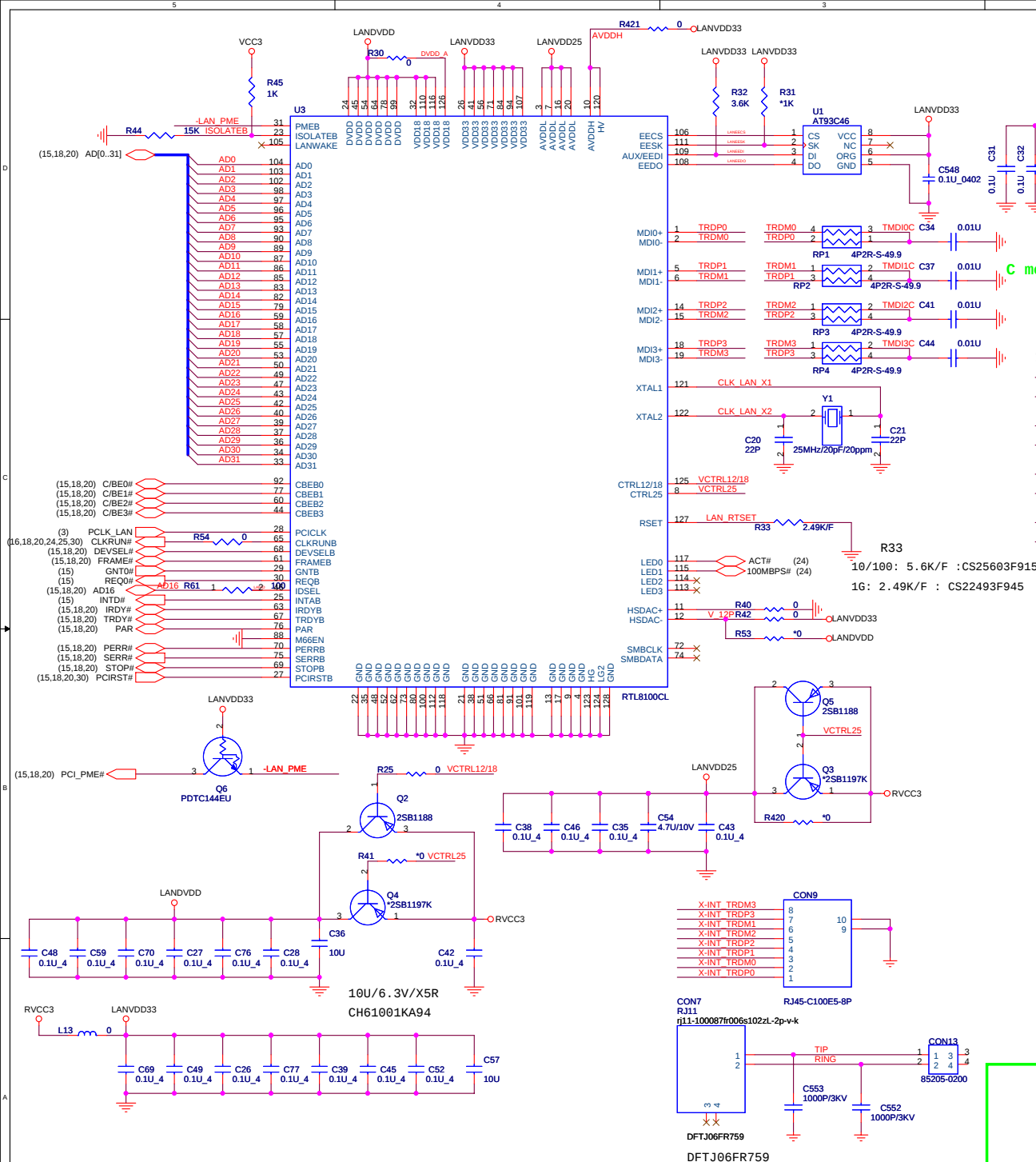




PCMCIA Conn.

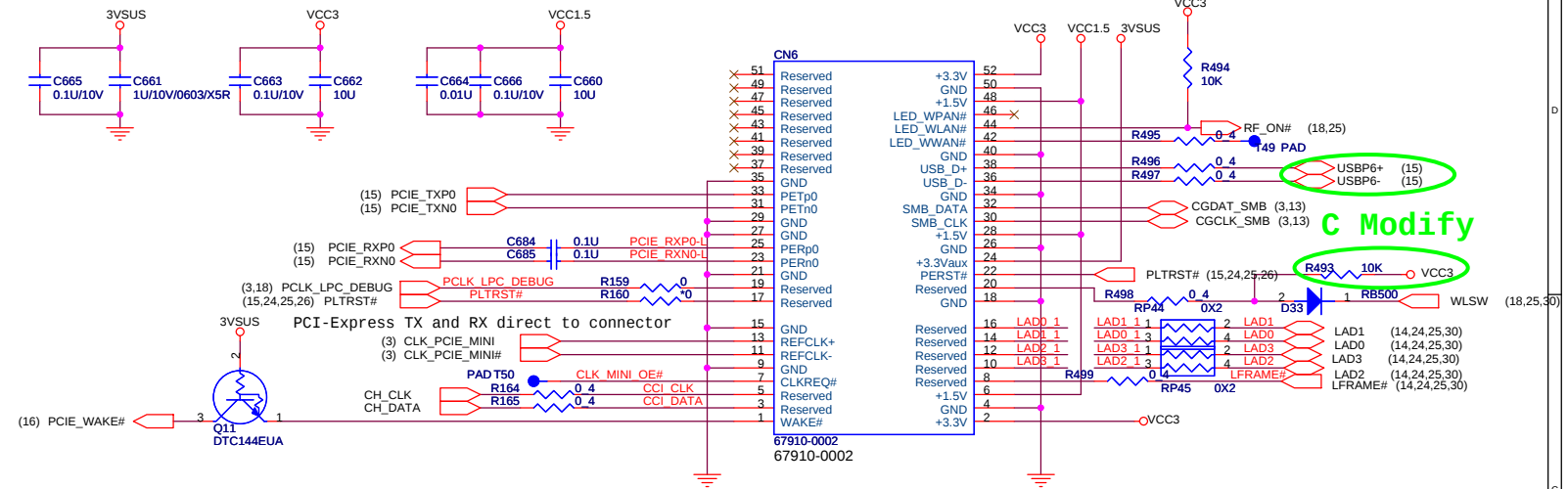
21



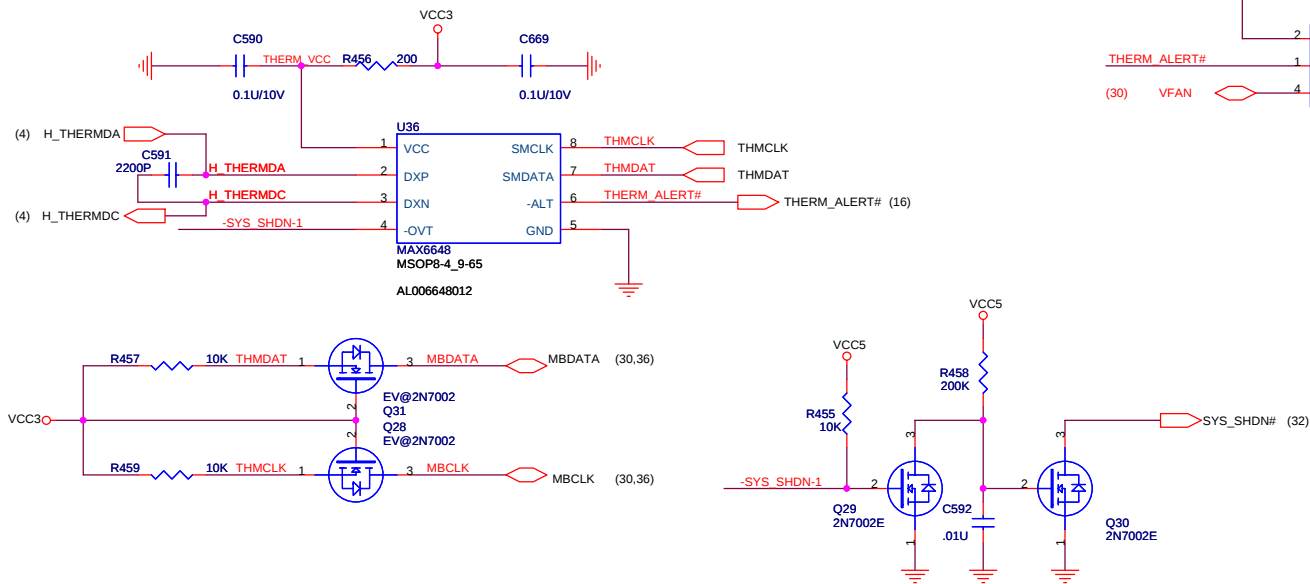


	RTL8100CL	RTL8110SCL	RTL8110SB
AVDDH	Remove R421	Keep R421	Keep R421
LANVDD25	Keep R420 Remove Q5	Keep Q5 Remove R420	Keep Q5 Remove R420
V12_P	Keep R53 Remove R42	Keep R42 Remove R53	Keep R42 Remove R53
DVDD_A	Remove R30	Keep R30	Keep R30
DVDD	Keep R41, Q4 Remove R25, Q2	Keep R25, Q2 Remove R41, Q4	Keep R25, Q2 Remove R41, Q4
V_DAC	Remove R34	Remove R34	Keep R34
	Remove R60	Keep R60	Keep R60
		Remove RP1, 2, 3, 4 C34, 37, 41, 44	

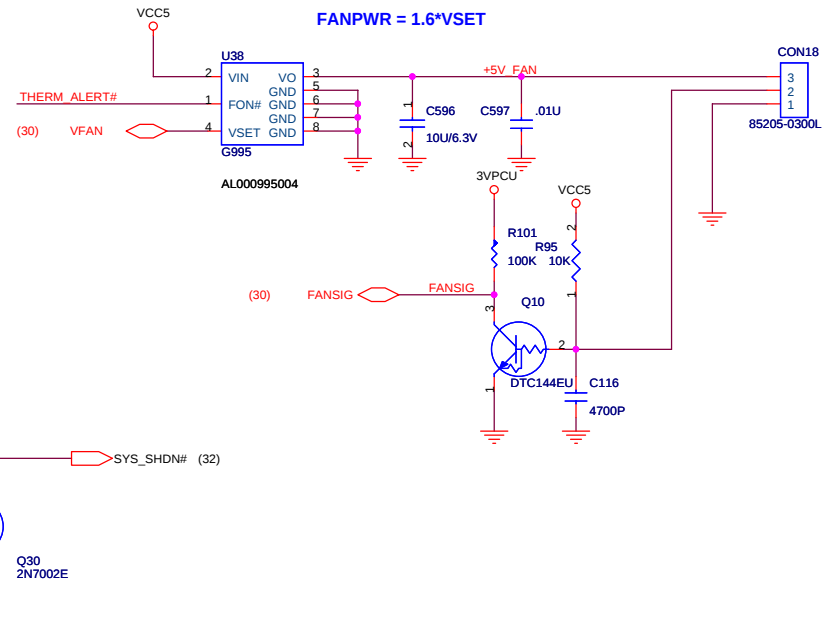
Mini PCI-E Card

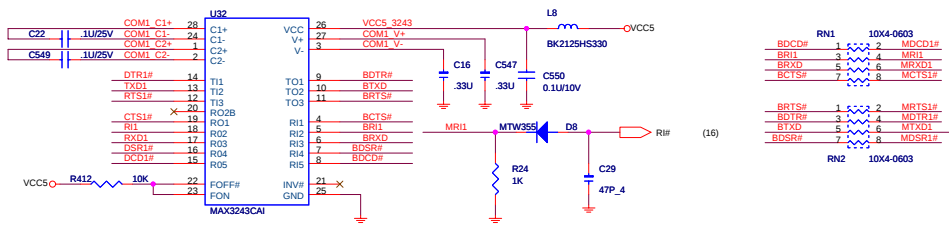
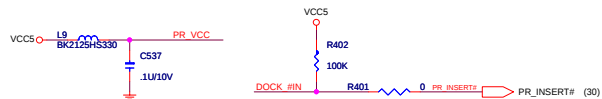
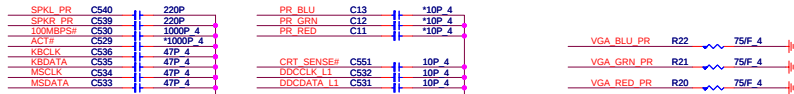
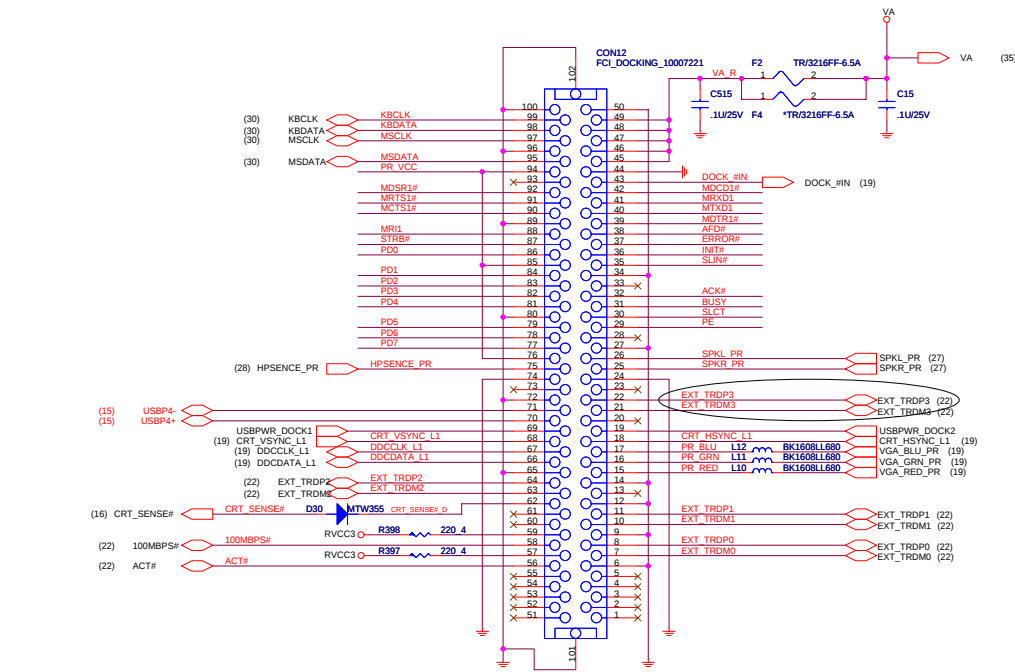


Thermal Sensor

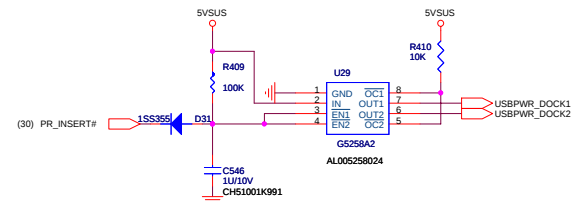
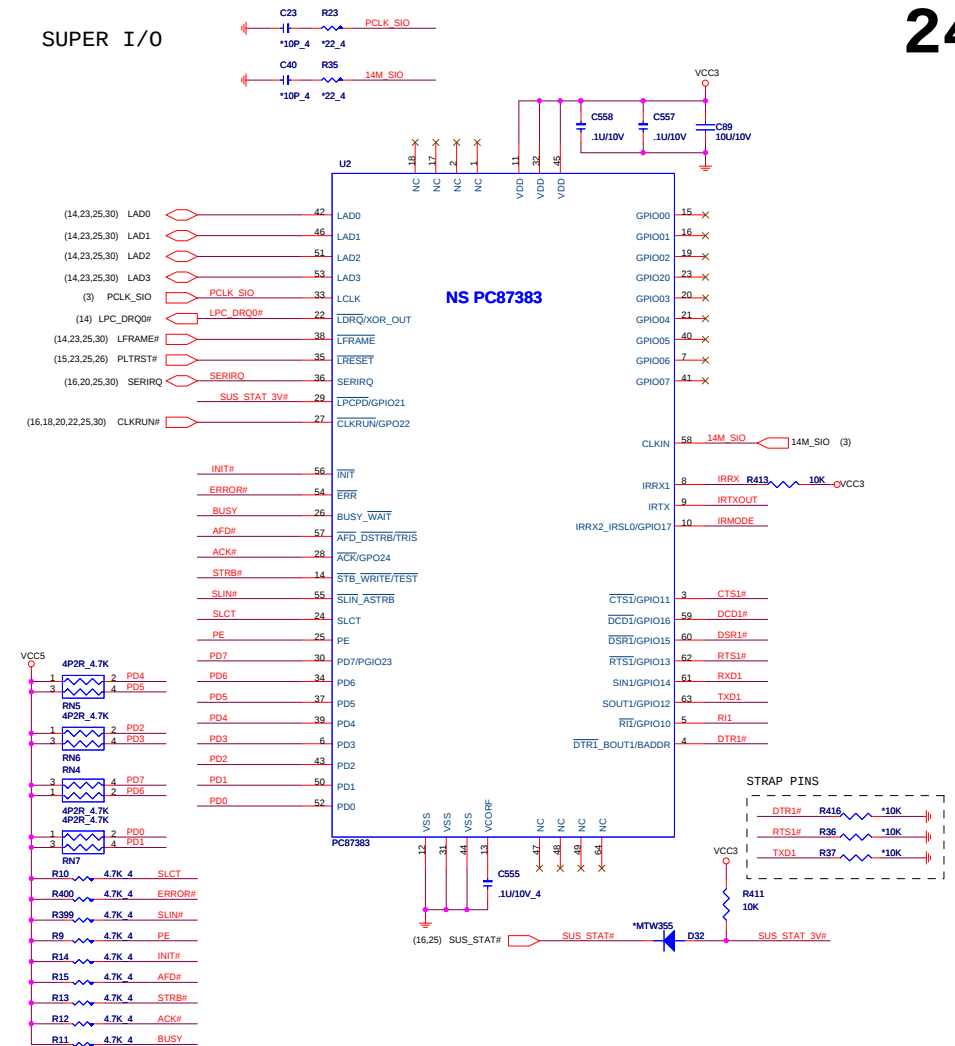


FAN CONN

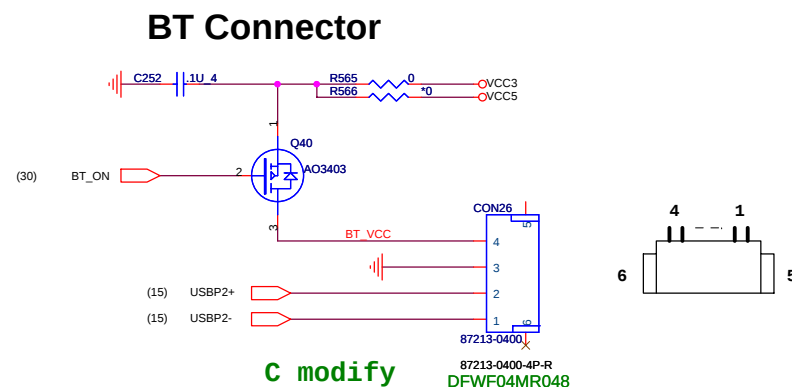
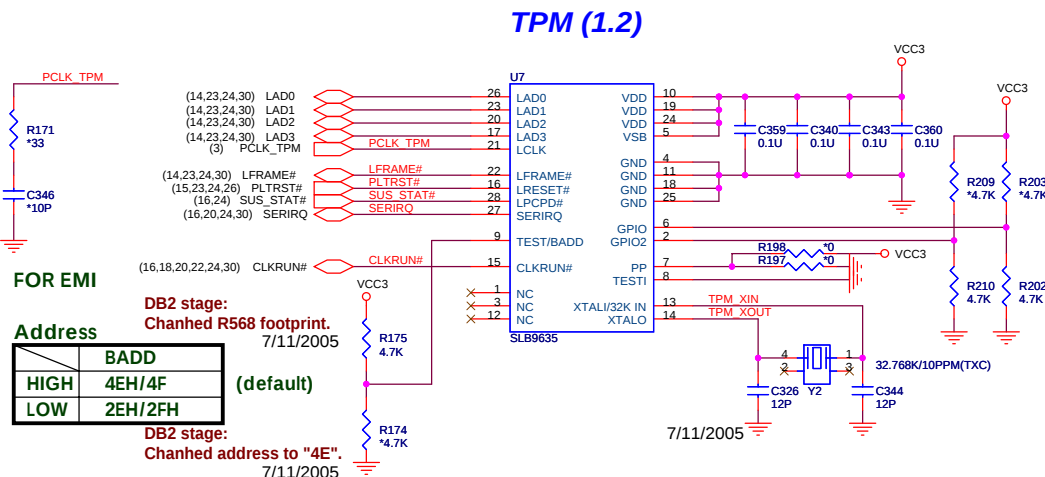
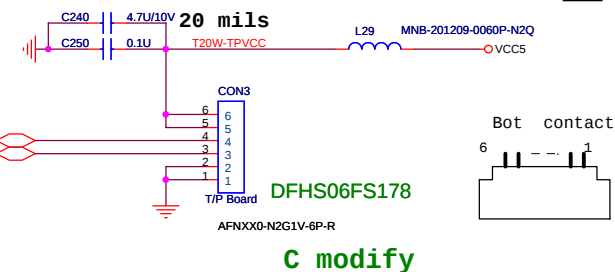




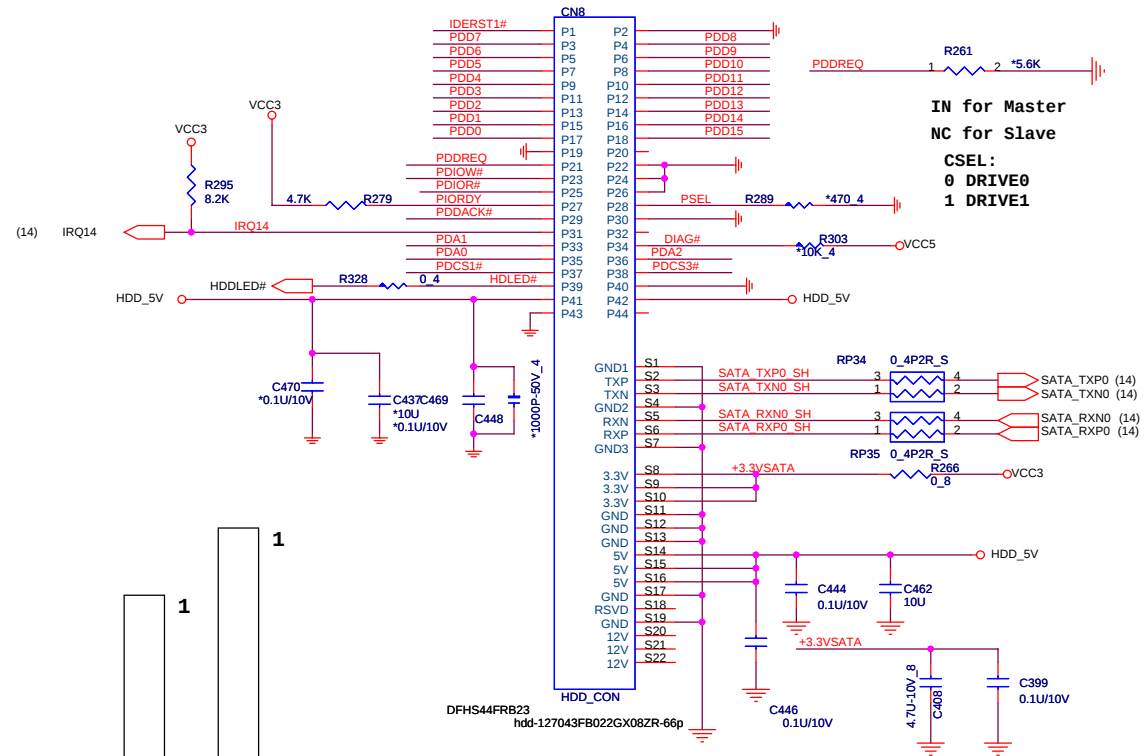
SUPER I/O



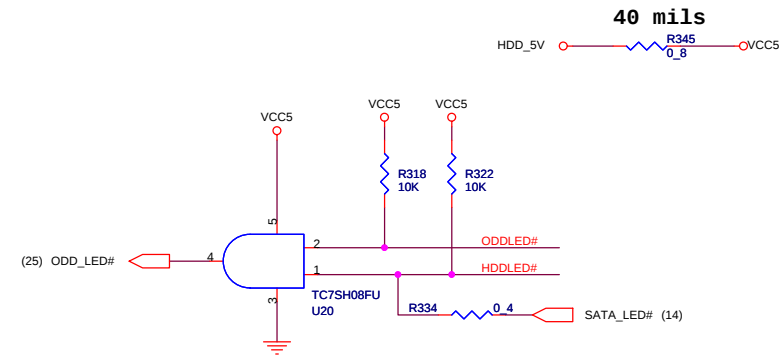
25



PATA HDD CONNECTOR

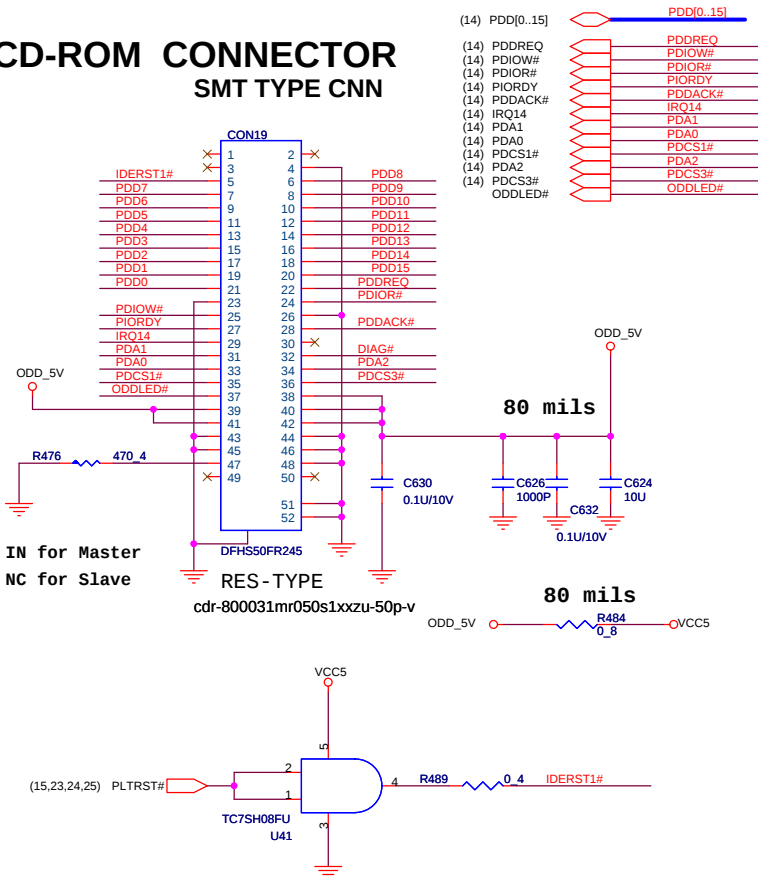


SATA HDD CONNECTOR



CD-ROM CONNECTOR

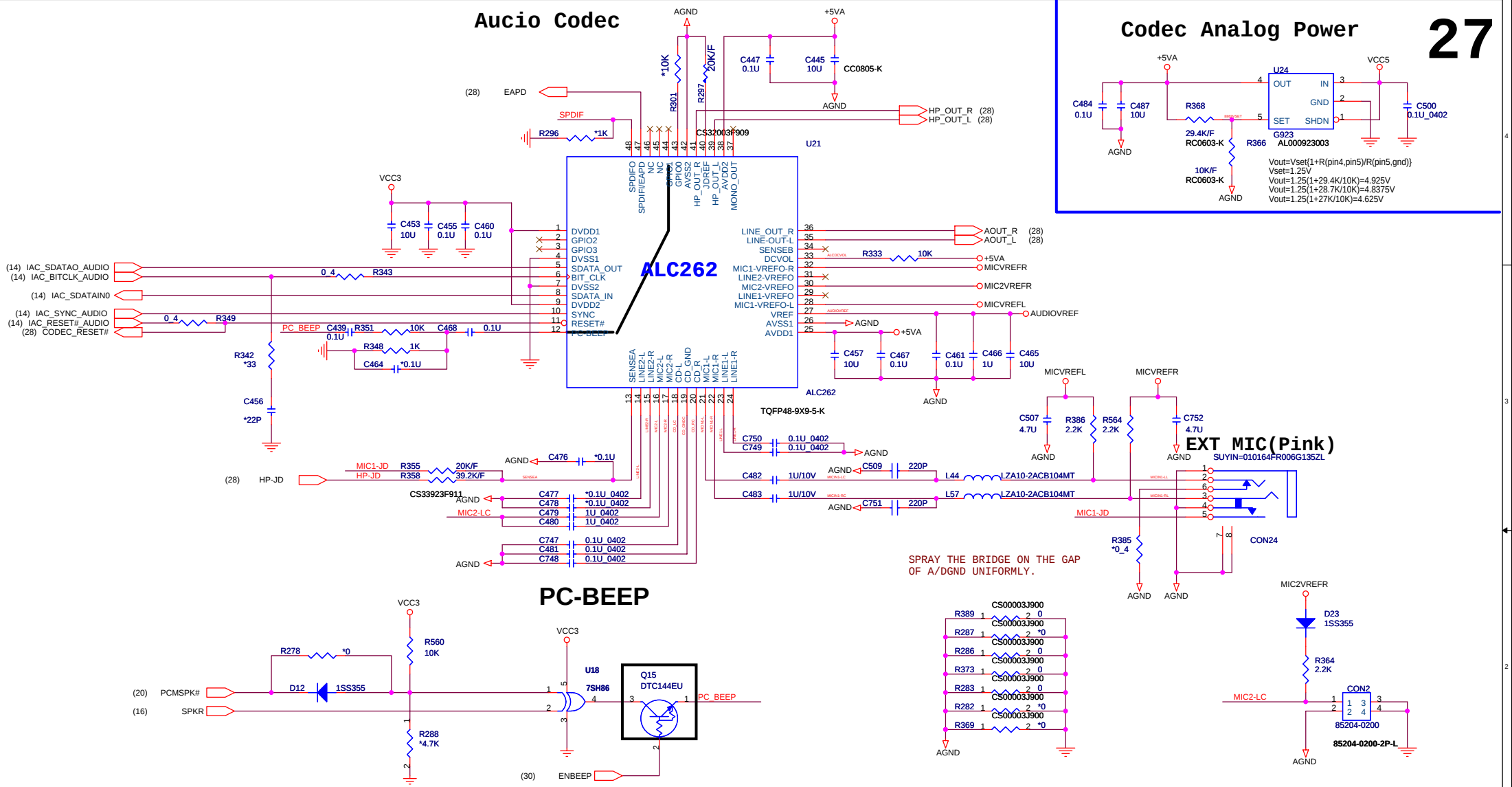
SMT TYPE CNN



Aucio Codec

Codec Analog Power

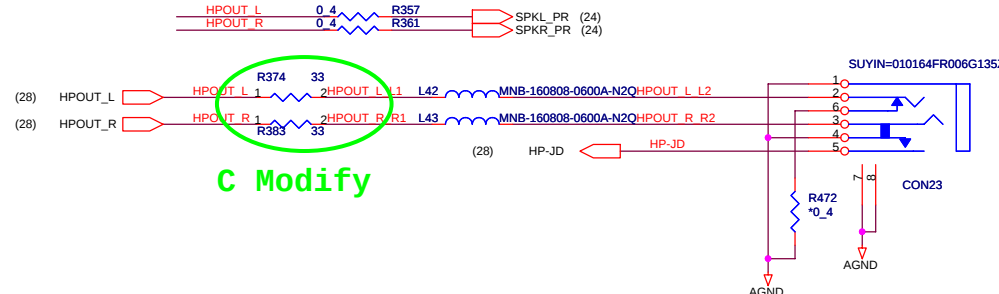
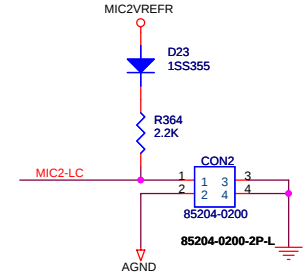
27



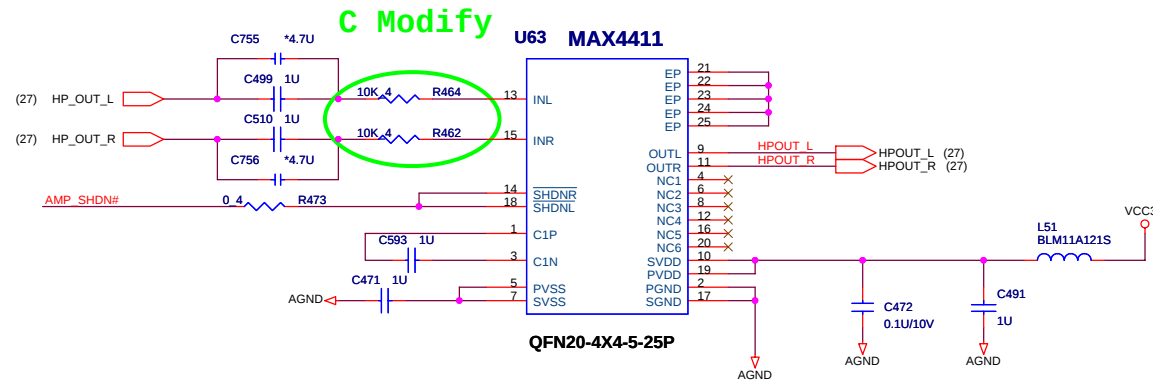
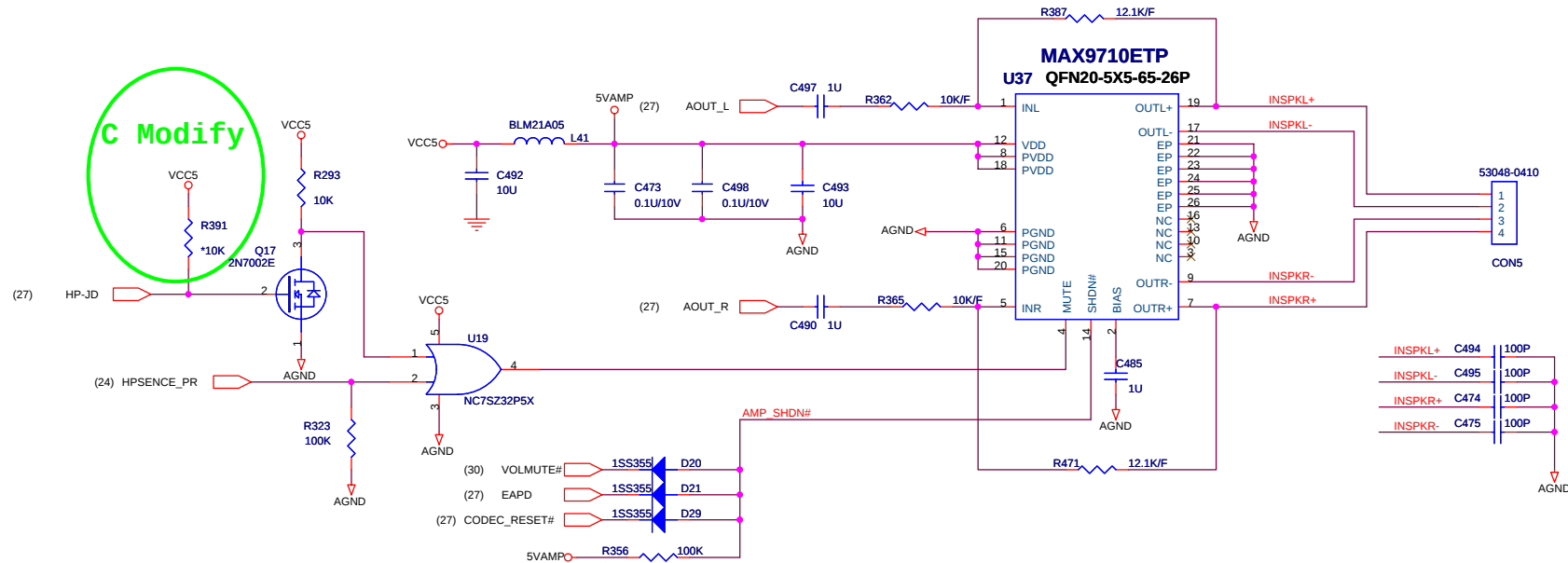
EXT MIC(Pink)

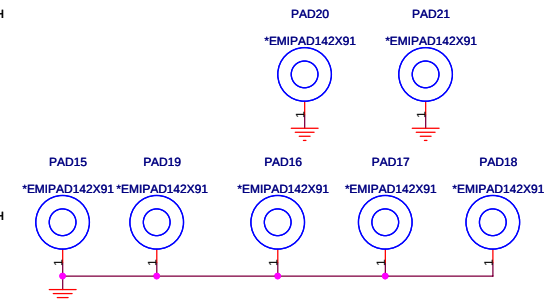
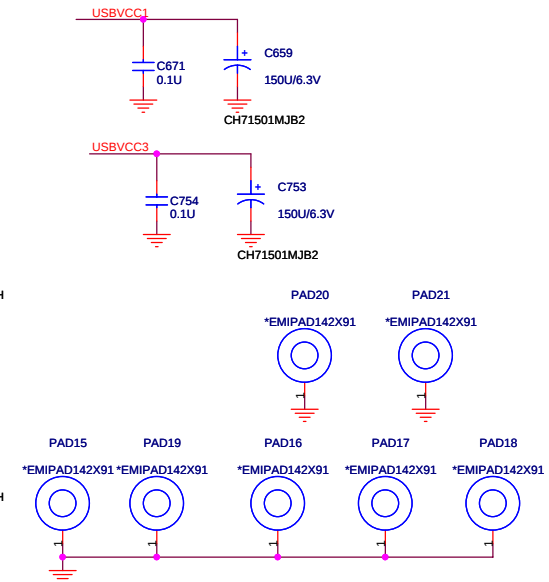
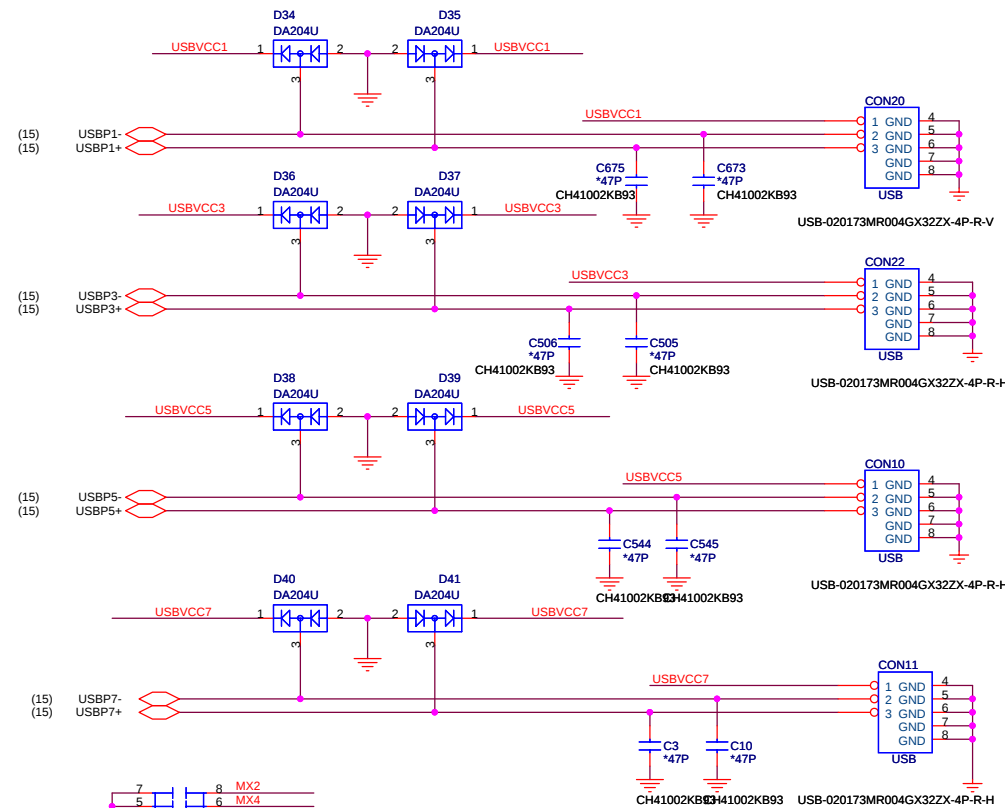
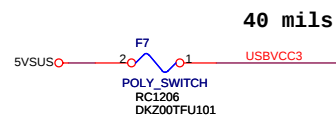
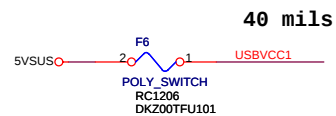
SPRAY THE BRIDGE ON THE GAP OF A/DGND UNIFORMLY.

PC-BEEP

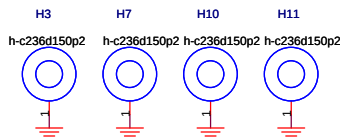


C Modify

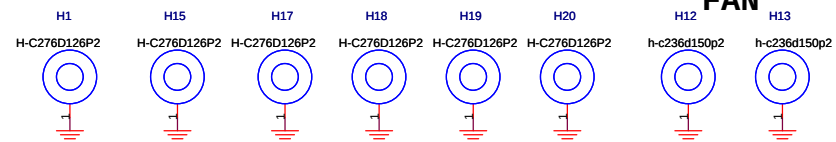




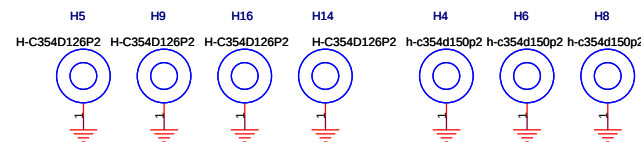
MDC, PCI_E



FAN



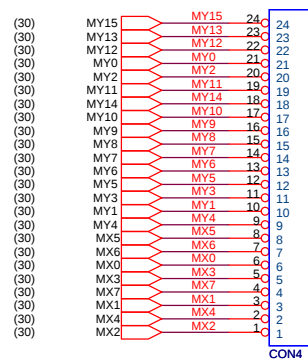
CPU



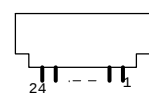
DC_IN



AFN240-A2G1T-24P-L
AFN240-A2G1T-24P-L

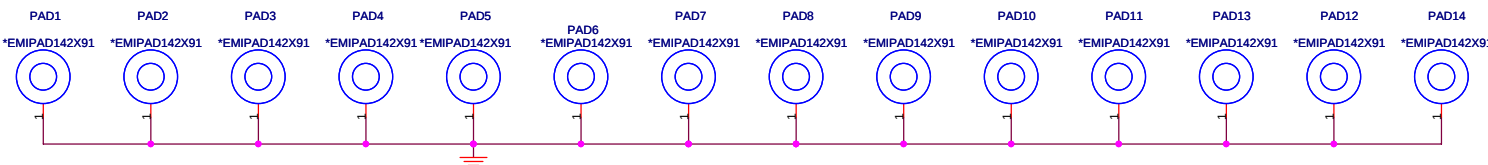


Bot contact



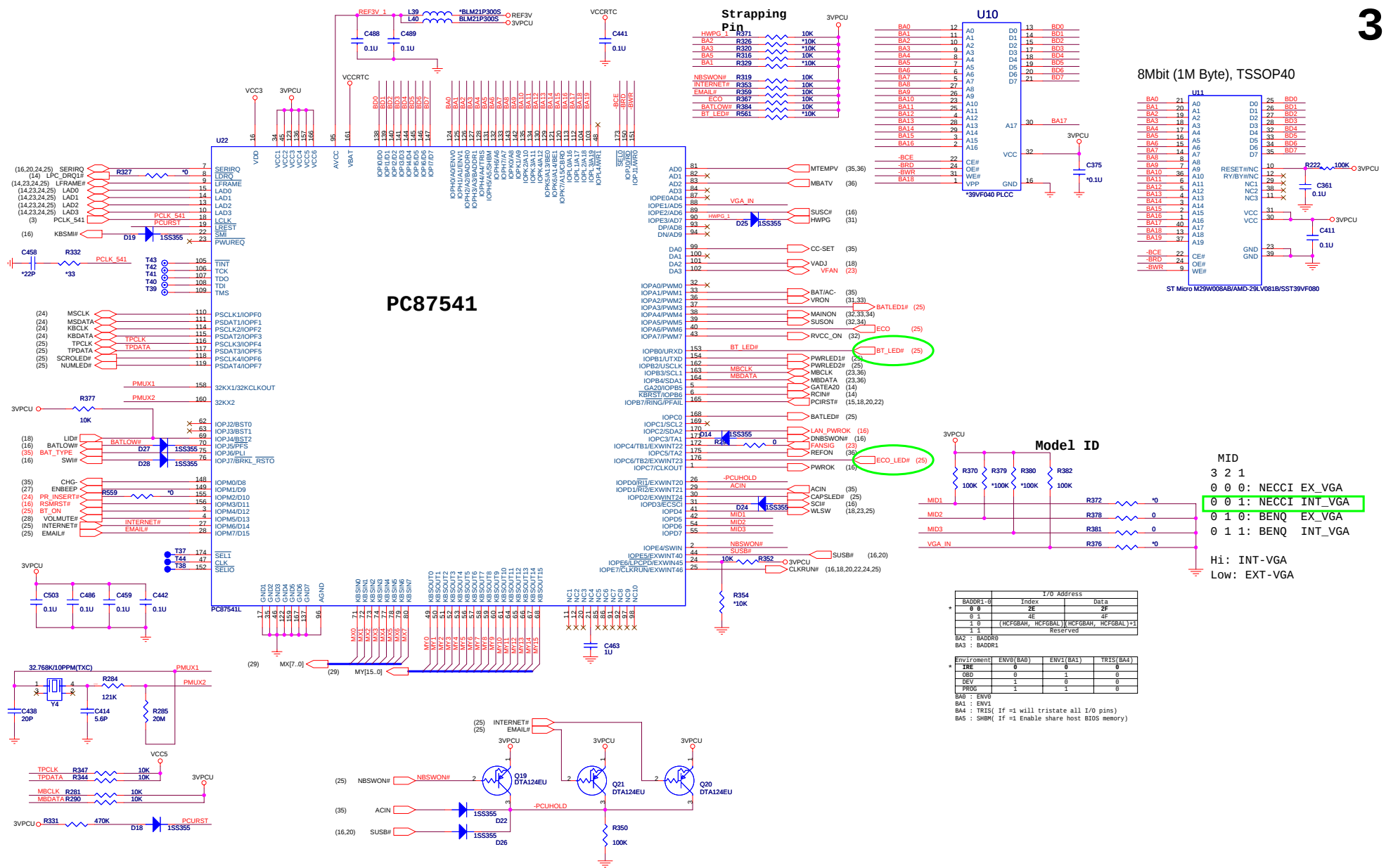
P/N:DFHS24FR180

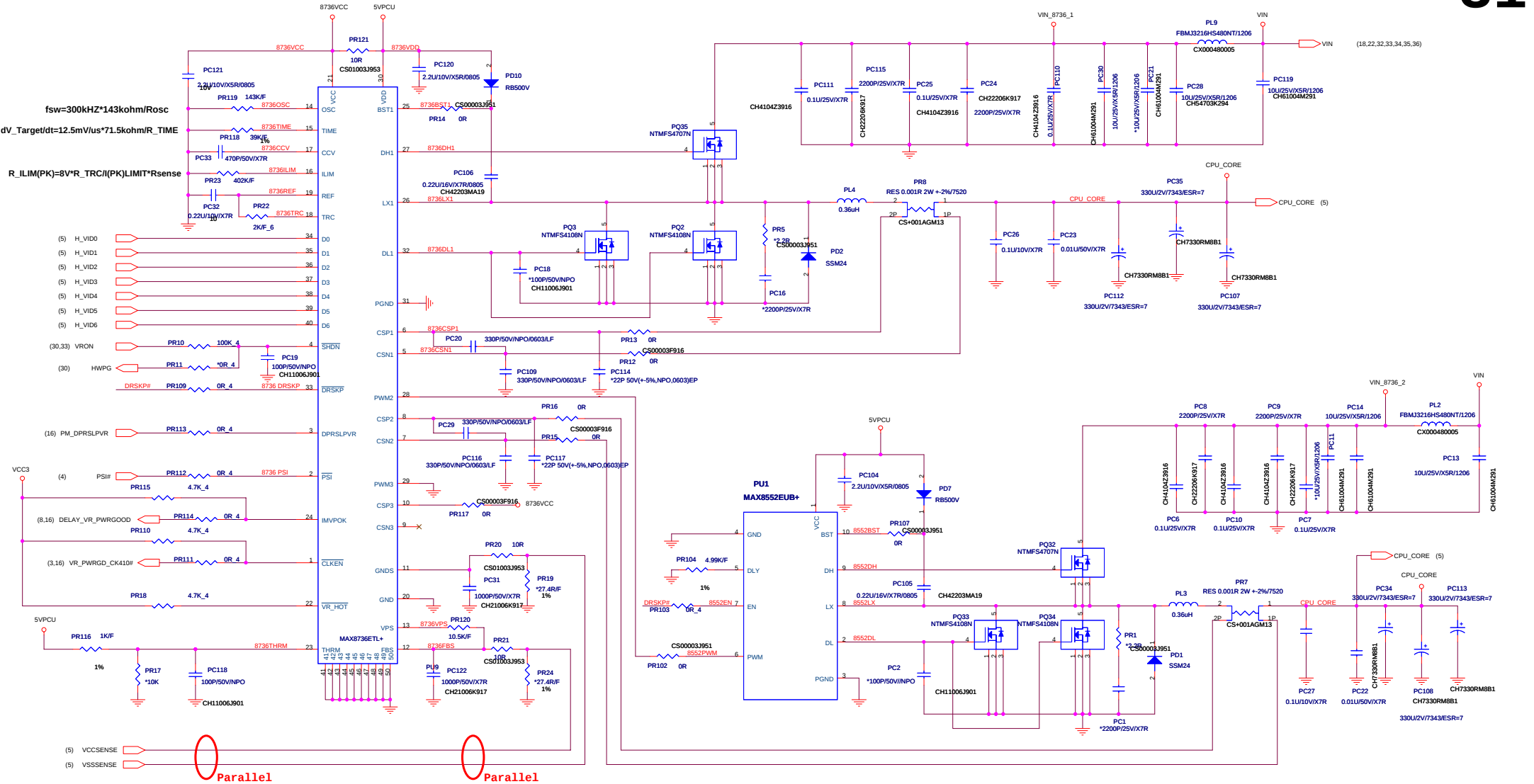
C modify



PROJECT : K3W
Quanta Computer Inc.

8Mbit (1M Byte), TSSOP40

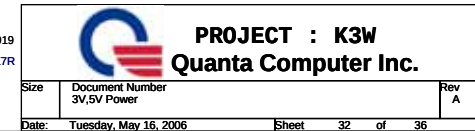


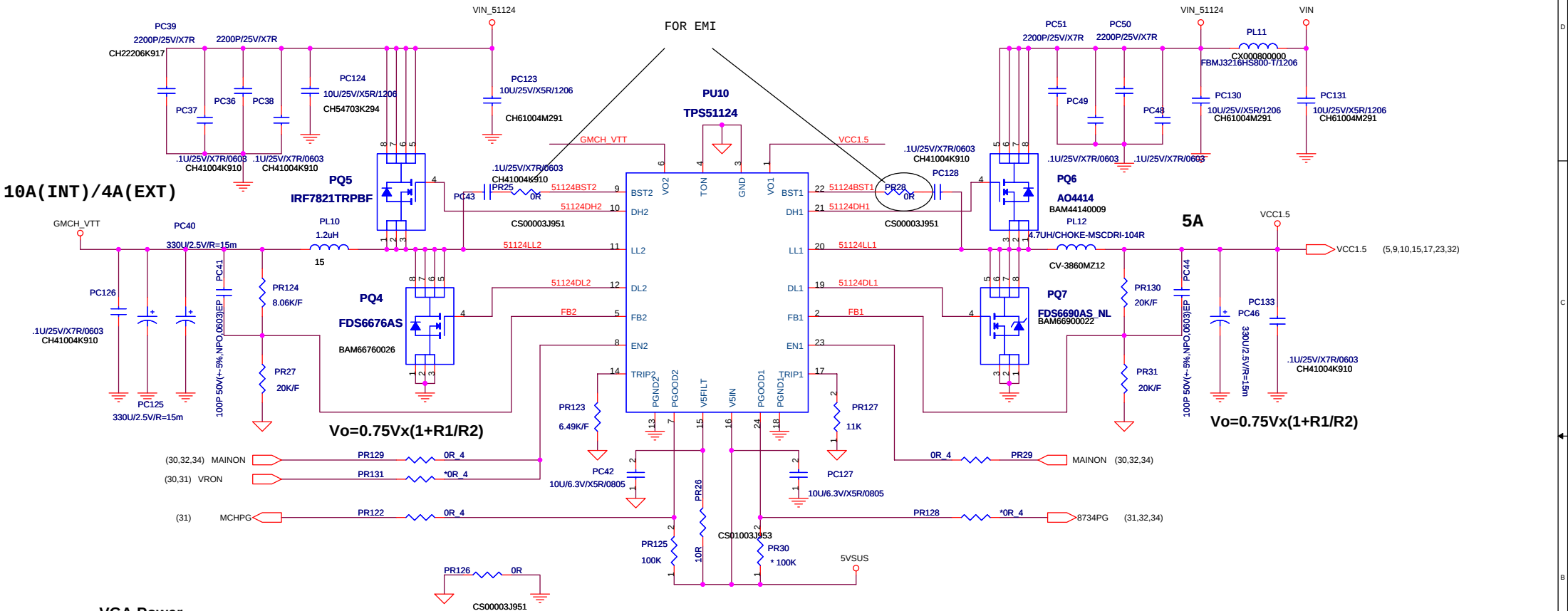


DPRSLPVR	DPRSKP#	-PSI	State	CPU Current
1	0	0	Deeper Sleep	< 3A
1	0	1	Deeper Sleep	> 3A
0	1	0	Active Mode	< 18A
0	1	1	Active Mode	> 15A

DPRSLPVR	PSI#	
1	X	1-phase pulse-skipping mode(low power)
0	0	1-phase forced-PWM mode(inteermidiate power)
0	1	All phase active,forced-PWM mode(full powr)

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VGA Power

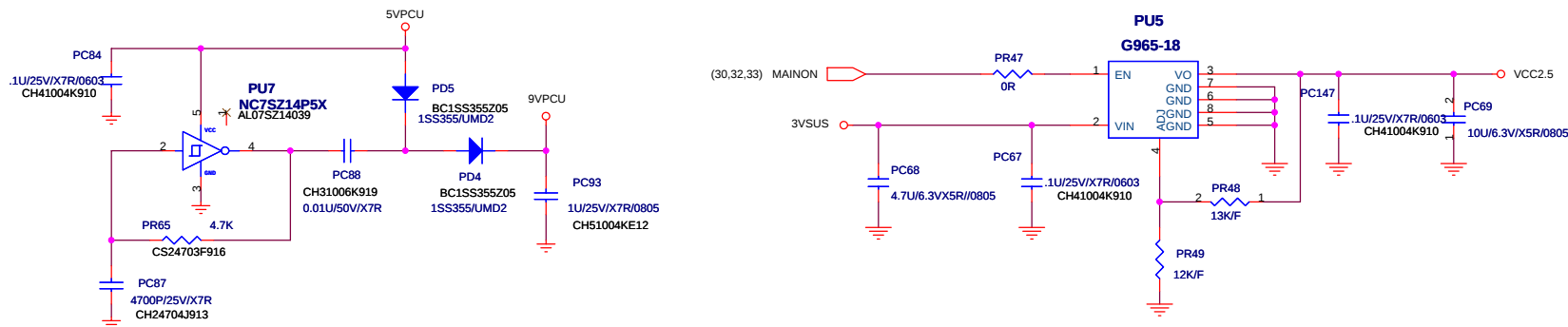
+VCCP	PL8	Current	R_TRIP2	PQ35
INT. Gfx	1.2uH	10A	6.49K	FDS6676S
EXT. Gfx	2uH	4A	11K	FDS6690AS

	INT. Gfx	EXT. Gfx
+VCCP	10A	4A
VCC1.5	3A	5.2A

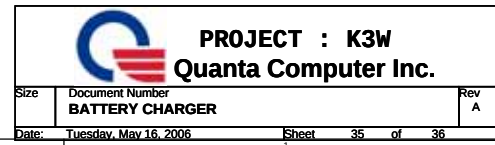
(3,4,5,6,9,10,14,17) GMCH_VTT

(5,9,10,15,17,23,32) VCC1.5

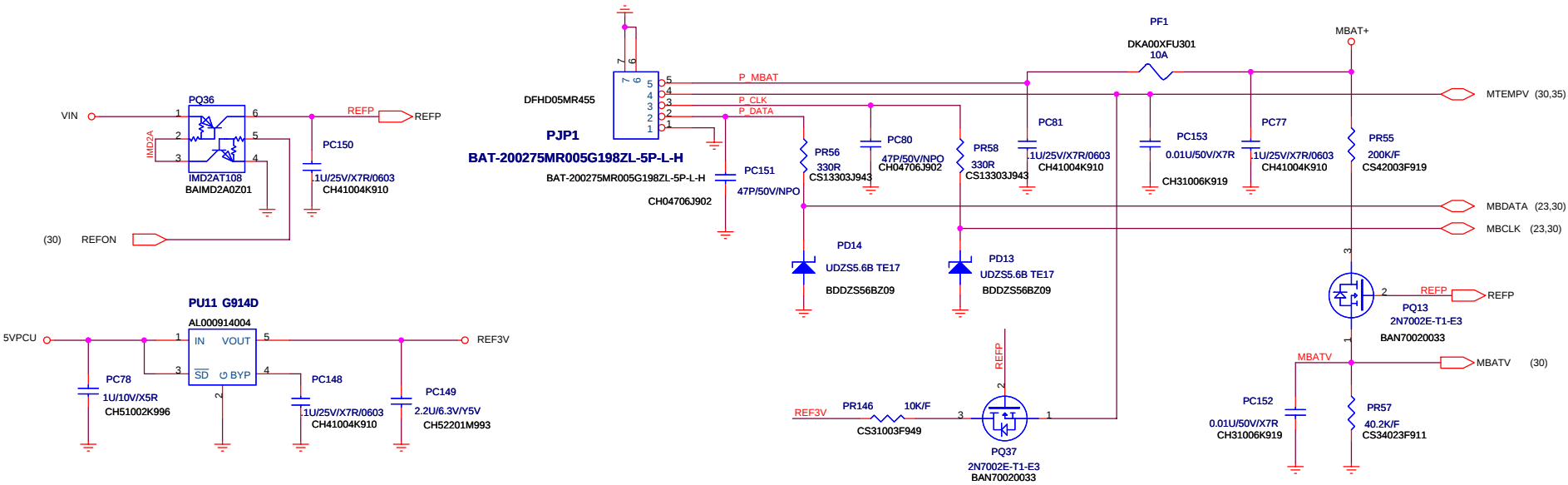
34



35



Battery Connector



MTEMPV voltage :		
	System Off	System On
Battery	0V	1.6V
Adapter	3.3V	3.3V
Battery+Adapter	1.6V	1.6V

MBATV voltage :

$16.8V \times 40.2 / (200 + 40.2) = 2.812V$

$12.0V \times 40.2 / (200 + 40.2) = 2.008V$

$8.0V \times 40.2 / (200 + 40.2) = 1.34V$