BOM MARK
E@ EXT VGA POPULATE
I@ INV VGA POPULATE
F@ FIR MODULE POPULATE
4@ 4401 10/100M POPULATE
5@ 5788 1G POPULATE

LE4 BLOCK DIAGRAM

Yonah /Calistoga /ICH-7m

1

VGA NVIDA G72M (64 Bit B/W)
16M*16(128MB)
(Bank*4)
PG 18,19,20,21

CPU Yonah/Merom
31W/35W
(478 Micro-FCPGA)
PG 4,5

CPU THERMAL SENSOR
PG 5

14.318MHz
CLOCK GEN
IDTXXX/ ICSXXXX
56pins
PG 3

CPUCLK,
CPUCLK#
SBLINKCLK, SBLINKCLK#
NBSRCCLK, NBSRCCLK#
HTREFCLK
OSC14M

HyperThansport I/O BUS
16X PCI-E
Link 16x16

NORTH BRIDGE
Calistoga
945GM/ 945PM / 940GML
INTEGRADED VGA FUNCTION
1466 BGA
PG 6,7,8,9,10,11

DDRII
266,333 MHz
DDRII-SODIMM1
PG 16,17
DDRII
266,333 MHz
DDRII-SODIMM2
PG 16,17

EXT_CRT
EXT_LVDS
EXT_TV-OUT
INT_CRT
INT_LVDS
INT_TV-OUT
SWITCH CIRCUIT
CRT port PG 23
LCD Panel PG 22
S-VIDEO PG 23

DMI LINK
2X
PCI-E

32.768KHz
NBSRCCLK, NBSRCCLK#
33MHZ, 3.3V PCI

USB PORT 0,2,6
PG 31
USB 2.0
SATA-HDD
PG 32
PATA-CDROM
PG 32
ATA 66/100/133

ICH7-M
652 BGA
PG 12,13,14,15

Azalia
MIC IN
PG 28

Conexant Audio
CX20549-12
PG 28

LAN
BCM4401/5788
PG 33

24.576MHz
CARDREADER / IEEE 1394
CONTROLLER/CF
TI 8412
PG 24,25

25MHz

3 IN 1
CARD READER SD, SM, MS,
PG 25

CARDBUS SOCKET
PG 25

1394 CONN
PG 24

LPC
3.3V LPC, 33MHz
PCLK_E

32.768KHz
PC87551L
PG 30

IO/B
CON.
SIO (87383)
PG 26

Express Card x1
MINI PICE CARD
USB PORT 1
PG 27

AMP
MAX9755
PG 29

MDC CONN
PG 27

WIRE

SPEKER
PG 29
INT_SPK
PG 29

IO/B
RJ11
JACK
PG 24

RJ45
JACK
PG 34

IR module PG 26
FAN PG 31
Touchpad PG 31
Keyboard PG 26
FLASH PG 30

SYSTEM POWER MAX1993
(1.2V/NB_CORE/1.25V)
PG 41

CPU CORE MAX8771
POWER VCORE 1.2V /44A
PG 38

SYSTEM MAX8734
POWER(3/5V)
PG 39

SYSTEM POWER MAX8632
(1.8VSUS/0.9V SMDDR_VREF)
PG 36

BATT CHARGER
MAX8724
PG 35

DISCHARGE
PG 40

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : VCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

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Quanta Computer Inc.

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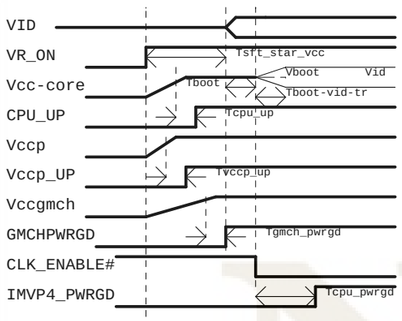
Board Stack up Description

PCB Layers

Layer 1		TOP(Component,Other)
Layer 2		Ground Plane
Layer 3		IN1
Layer 4		Power Plane
Layer 5		IN2
Layer 6		IN3
Layer 7		Ground Plane
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



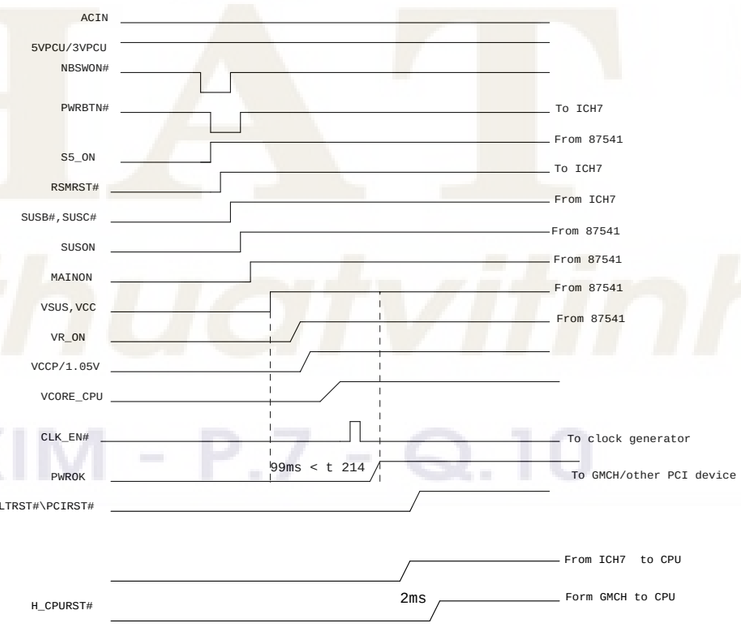
Dothan Power-up Timing Specifications

Ta=VCC and VCCP asseration to VID[5:0] vaild
Tb=VID[5:0] stable to VCC vaild
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=Vcc,boot vaild to PWRGOOD assertion time

Voltage Rails

Voltage Rails		ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	Core voltage for Processor	X				VR_ON 0.726V~0.94V
VCCP	Core voltage for CPU / NB	X				VR_ON
SMDDR_VTERM	0.9V for DDR2 Termination voltage	X				MAINON
RVCC1.5		X	X	X		RVCC_ON
RVCC3		X	X	X		RVCCD
VCC1.5		X				MAIND
VCC2.5		X				MAINON
VCC3		X				MAIND
VCC5		X				MAIND
1.8VSUS		X	X			SUSON
3VSUS		X	X			SUSD
5VSUS		X	X			SUSD
3VPCU		X	X	X	X	VL
5VPCU		X	X	X	X	VL
9VPCU		X	X	X	X	5VPCU

ACIN POWER ON TIMING



Voltage Rails		ON S0~S1	ON S3	ON S4	ON S5	Control signal
VCC_CORE	Core voltage for Processor	X				VRON
GMCH_VTT	Core voltage for GMCH 1.05V	X				MAINON
SMDDR_VTERM	0.9V for DDR II Termination voltage	X				MAINON
SMDDR_VREF	0.9V for DDR II Reference Voltage	X				MAINON
GMCH_1.5V		X				MAINON
1.8VSUS	1.8V for DDR II voltage	X	X			SUSON
+2.5V		X				MAINON
3VPCU		X	X	X	X	VL
3VSUS		X	X			SUSON
+3V		X				MAINON
5VPCU		X	X	X	X	VL
5VSUS		X	X			SUSON
+5V		X				MAINON
VIN	POWER SOURCE	X	X	X	X	

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7402	AD25	REQ1# / GNT1#	PIRQ B/C/D

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FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.

R199 1 2 49.9/F_4
R200 1 2 49.9/F_4
R196 1 2 49.9/F_4
R197 1 2 49.9/F_4

C323 33P_4 XIN <500mil
C324 33P_4 XOUT
Y2 14.318MHZ BG614318081

U17 CK-410M

XTAL_IN 50
XTAL_OUT 49
VDD_A 37
VSS_A 38
REF 52 14M_REF
CPU0 44 R_HCLK_CPU
CPU0# 43 R_HCLK_CPU#
CPU1 41 R_HCLK_MCH
CPU1# 40 R_HCLK_MCH#
CPU2_ITP/SRC7 36 R_PCIE_VGA
CPU2#_ITP/SRC7# 35 R_PCIE_VGA#
SRC6 33
SRC6# 32
SRC5 31 R_MCH_3GPLL
SRC5# 30 R_MCH_3GPLL#
SRC4 26 R_PCIE_SATA
SRC4# 27 R_PCIE_SATA#
SRC3 24 R_PCIE_ICH
SRC3# 25 R_PCIE_ICH#
SRC2 22 R_PCIE_MINI
SRC2# 23 R_PCIE_MINI#
SRC1 19
SRC1# 20
SRC0 17 R_DREFSSCLK
SRC0# 18 R_DREFSSCLK#
PCI5 5 R_PCLK_LAN
PCI4 4 R_PCLK_LPC
PCI3 3 R_PCLK_LPC_DEBUG
PCI2 56 R_PCLK_PCM
PCIF1 9 R_PCLK_SIO
PCIF0/ITP_EN 8 PCIF0
VTT_PWRGD#/PD 10 CLK_EN#
PCI_STOP# 55 PM_STPPCI#
CPU_STOP# 54 PM_STPCPU#
SCLK 46 CGCLK_SMB
SDATA 47 CGDAT_SMB
FSA/USB_48 12 FSA
FSB/TEST_MODE 16 FSB
FSC/TEST_SEL 53 FSC
VDD_REF 48 VDDREF_CR
VDD_CPU 42 CLKVDD
VDD_PCI_1 1 CLKVDD1
VDD_PCI_2 7
VDD_SRC0 21 CLKVDD
VDD_SRC1 28
VDD_SRC2 34
VDD_48 11 VDD48_CR
IREF 39 IREF
DOT96 14 R_DOT96
DOT96# 15 R_DOT96#
GND_48 13
GND_REF 51
GND_PCI_1 2
GND_PCI_2 6
GND_SRC 29
GND_CPU 45

ICS954206AGLFT
250mA (MAX.)

R201 1 2 475/F_4
Iref=5mA,
Ioh=4*Iref

RP34 4P2R-S-33
RP39 4P2R-S-33
RP43 4P2R-S-33
RP47 4P2R-S-33
RP48 4P2R-S-33
RP44 4P2R-S-33
RP40 4P2R-S-33
RP37 I@4P2R-S-33
RP35 I@4P2R-S-33

R192 1 2 33_4 14M_SIO (26)
R188 1 2 33_4 14M_ICH (14)
C366 *10P_4
C361 *10P_4

CLK_CPU_BCLK (4)
CLK_CPU_BCLK# (4)
CLK_MCH_BCLK (6)
CLK_MCH_BCLK# (6)
CLK_PCIE_VGA (18)
CLK_PCIE_VGA# (18)
CLK_PCIE_3GPLL (7)
CLK_PCIE_3GPLL# (7)
CLK_PCIE_SATA (12)
CLK_PCIE_SATA# (12)
CLK_PCIE_ICH (13)
CLK_PCIE_ICH# (13)
CLK_PCIE_MINI (27)
CLK_PCIE_MINI# (27)
DREFSSCLK (7)
DREFSSCLK# (7)
0816a

R186 1 2 33_4 PCLK_LAN
R181 1 2 33_4 PCLK_LPC
R178 1 2 33_4 PCLK_LPC_DEBUG
R182 1 2 33_4 PCLK_PCM
R194 1 2 33_4 PCLK_541
PCLK_LAN (33)
PCLK_LPC (26)
PCLK_LPC_DEBUG (27)
PCLK_PCM (24)
PCLK_541 (30)

R189 1 2 *10K_4 +3VRUN
R183 1 2 10K_4
R185 1 2 33_4 PCLK_ICH
PCLK_ICH (13)

PCIF1
1:100 Mhz
0:96
Mhz

(14,37) CLK_EN#
(14) PM_STPPCI#
(14) PM_STPCPU#
(25) TI_CLK48M
(14) CLKUSB_48
R195 1 2 10_4 TI_CLK48M
R190 1 2 10_4 CLKUSB_48

SMbus address D2

(4,7) CPU_MCH_BSEL0
(4,7) CPU_MCH_BSEL1
(4,7) CPU_MCH_BSEL2
R193 1 2 8.2K/F_4 FSA
R184 1 2 8.2K/F_4 FSC

LE4 A:
Changed new function

Solved sometimes can't power on

+3VRUN

LE4 B:

Add R566 pull high with FSA

R566 10K_4
R567 *10K_4

(7) DOT96
(7) DOT96#

+3VRUN

RP33 4P2R-S-10K

Q32 Q33

(14,33) PDAT_SMB
(14,33) PCLK_SMB
PDAT_SMB
PCLK_SMB
CGDAT_SMB
CGCLK_SMB
CGDAT_SMB (16,17,27)
CGCLK_SMB (16,17,27)
RHU002N06
RHU002N06

Connect ICH6 SMB

Connect DDR Module's SMB

These are for backdrive issue

CT_0505: Change footprint to TSSOP56-8_1-5 from TSSOP56-240

CT_0229: Change MOS to RHU002N06 due to layout concern.

Bypass CAPs need to follow Bypass CAP. Routing Rule, no vias between CAP to CHIPSET VCC Pin or GND.

Tie to VCC (Logic 1) is for ITP using.
Tie to GND (Logic 0) is for PCIE using.

120 ohms@100Mhz
L31 HB-1T2012-121JT_8
+3VRUN
C387 0.047U/10V_4
C573 0.047U/10V_4
C383 0.047U/10V_4
C579 0.047U/10V_4
C388 4.7U/10V_8
CLKVDD

R204 2.2
C578 0.047U/10V_4
C393 4.7U/10V_8
VDDA_CR

120 ohms@100Mhz
L25 HB-1T2012-121JT_8
+3VRUN
C351 0.047U/10V_4
C565 0.047U/10V_4
C326 4.7U/10V_8
CLKVDD1

R177 2.2
C374 0.047U/10V_4
C340 4.7U/10V_8
VDD48_CR

R191 1R_6
C564 0.047U/10V_4
VDDREF_CR

CLK_PCIE_VGA
CLK_PCIE_VGA# RP42 49.9_4P2R
CLK_PCIE_MINI
CLK_PCIE_MINI# RP41 49.9_4P2R
CLK_MCH_3GPLL
CLK_MCH_3GPLL# RP46 49.9_4P2R
CLK_PCIE_SATA
CLK_PCIE_SATA# RP49 49.9_4P2R
CLK_PCIE_ICH
CLK_PCIE_ICH# RP45 49.9_4P2R
DREFSSCLK
DREFSSCLK# RP38 I@49.9_4P2R
DOT96
DOT96# RP36 I@49.9_4P2R

Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.

PCLK_LAN C359 *10P_4
PCLK_PCM C432 *10P_4
PCLK_541 C566 *10P_4
PCLK_LPC_DEBUG C350 *10P_4
PCLK_LPC C355 *10P_4
PCLK_ICH C442 *10P_4

LE4 A:
Add Cap 10p reserve for EMI E-mail 093020051211

LE4 A:
Del this function desgin

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ADDR GROUP 0 / CONTROL / XDP/ITP SIGNALS / THERM / H CLK / RESERVED

(6) H_A#[31:3] → H_A#[31:3]
H_A#3 J4 … H_A#16 R1
(6) H_ADSTB#0
(6) H_REQ#[4:0] → H_REQ#0 K3 … H_REQ#4 L5
H_A#[31:3] → H_A#17 Y2 … H_A#31 Y1
(6) H_ADSTB#1 → V4
(12) H_A20M# → A6
(12) H_FERR# → A5
(12) H_IGNNE# → C4
(12) H_STPCLK# → H_STPCLK# D5
(12) H_INTR → C6
(12) H_NMI → B4
(12) H_SMI# → A3

A[3]# J4 … A[16]# L2
ADSTB[0]#
REQ[0]# K3 … REQ[4]# L5
A[17]# Y2 … A[31]# Y1
ADSTB[1]# V4
A20M# A6
FERR# A5
IGNNE# C4
STPCLK# D5
LINT0 C6
LINT1 B4
SMI# A3

RSVD[01]# AA1
RSVD[02]# AA4
RSVD[03]# AB2
RSVD[04]# AA3
RSVD[05]# M4
RSVD[06]# N5
RSVD[07]# T2
RSVD[08]# V3
RSVD[09]# B2
RSVD[10]# C3
RSVD[11]# B25

T188 TP_A32# AA1
T187 TP_A33# AA4
T189 TP_A34# AB2
T186 TP_A35# AA3
T44 TP_A36# M4
T48 TP_A37# N5
T49 TP_A38# T2
T47 TP_A39# V3
T59 TP_APM0# B2
T51 TP_APM1# C3
T208 TP_HFPLL B25

ADS# H1 → H_ADS# (6)
BNR# E2 → H_BNR# (6)
BPRI# G5 → H_BPRI# (6)
DEFER# H5 → H_DEFER# (6)
DRDY# F21 → H_DRDY# (6)
DBSY# F1 → H_DBSY# (6)
BR0# → H_BREQ#0 (6)
IERR# D20
INIT# B3 → H_INIT# (12) → T195
LOCK# H4 → H_LOCK# (6)
H_CPURST# (6)
RESET# B1
RS[0]# E3 → H_RS#0
RS[1]# F4 → H_RS#1
RS[2]# G3 → H_RS#2
H_RS#[2:0] (6)
TRDY# G2 → H_TRDY# (6) → T56
HIT# G6 → H_HIT# (6)
HITM# E4 → H_HITM# (6)

BPM[0]# AD4 XDP_BPM#0 → T70
BPM[1]# AD3 XDP_BPM#1 → T67
BPM[2]# AD1 XDP_BPM#2 → T64
BPM[3]# AC4 XDP_BPM#3 → T65
PRDY# AC2 XDP_BPM#4 → T55
PREQ# AC1 XDP_BPM#5
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 XDP_TDO → T191
TMS AB5 XDP_TMS
TRST# AB6 XDP_TRST#
DBR# C20 XDP_DBRESET#

PROCHOT D21 H_PROCHOT#
THERMDA A24 H_THERMDA
THERMDC A25 H_THERMDC → H_THERMDA (5) H_THERMDC (5)
THERMTRIP# C7 PM_THRMTRIP# → PM_THRMTRIP# (7,12)

BCLK[0] A22 → T228 CLK_CPU_BCLK (3)
BCLK[1] A21 → T224 CLK_CPU_BCLK# (3)

RSVD[12]# T22 TP_EXTBREF → T75
RSVD[13]# D2 TP_SPARE0 → T57
RSVD[14]# F6 TP_SPARE1 → T61
RSVD[15]# D3 TP_SPARE2 → T53
RSVD[16]# C1 TP_SPARE3 → T190
RSVD[17]# AF1 TP_SPARE4 → T193
RSVD[18]# D22 TP_SPARE5 → T76
RSVD[19]# C23 TP_SPARE6 → T77
RSVD[20]# C24 TP_SPARE7 → T207

PZ47903-2741-01

+1.05V → +1.05V (5,6,7,9,10,12,15,38,40)
R458 56/F_4 — Near to MCH <500mils

LE4 A: Modfiy circuit

+1.05V → R198 75_4 — XDP PU_R < 0.2"

LE4 A: Modfiy circuit

(6) H_D#[63:0] → H_D#[63:0]

U38B

DATA GRP 0 / DATA GRP 2 / DATA GRP 1 / DATA GRP 3 / MISC

H_D#0 F22 … H_D#15 H25 → D[0]# … D[15]# (DATA GRP 0)
H_D#16 N22 … H_D#31 M24 → D[16]# … D[31]# (DATA GRP 1)
D[32]# AA23 H_D#32 … D[47]# W24 (DATA GRP 2)
D[48]# AC22 H_D#48 … D[63]# AD23 (DATA GRP 3)

(6) H_DSTBN#0 → DSTBN[0]#
(6) H_DSTBP#0 → DSTBP[0]#
(6) H_DINV#0 → DINV[0]#
DSTBN[2]# W24 → H_DSTBN#2 (6)
DSTBP[2]# Y25 → H_DSTBP#2 (6)
DINV[2]# V23 → H_DINV#2 (6)
(6) H_DSTBN#1 → DSTBN[1]# M24
(6) H_DSTBP#1 → DSTBP[1]# N25
(6) H_DINV#1 → DINV[1]# M26
DSTBN[3]# AE24 → H_DSTBN#3 (6)
DSTBP[3]# AE25 → H_DSTBP#3 (6)
DINV[3]# AC20 → H_DINV#3 (6)

GTLREF AD26
TEST1 C26
TEST2 D25
BSEL[0] B22
BSEL[1] B23
BSEL[2] C21
DPRSTP# E5
DPSLP# B5
DPWR# D24
PWRGOOD D6
SLP# D7
PSI# AE6

PZ47903-2741-01

+1.05V → R468 1K/F_4 → H_GTLREF
R213 *1K_4 / R212 51_4 — 20/15mils
R467 2K/F_4
(3,7) CPU_MCH_BSEL0
(3,7) CPU_MCH_BSEL1
(3,7) CPU_MCH_BSEL2
Use 1% R
Layout note: 0.5" max for GTLREF

LE4 A: Modify circuit

Trcae width : ? placement <0.5"
25/25mils

R26 COMP0 27.4/F_4 R465
U26 COMP1 54.9/F_4 R464
U1 COMP2 27.4/F_4 R151
V1 COMP3 54.9/F_4 R150

ICH_DPRSTP# (12,37)
H_DPSLP# (12)
H_DPWR# (6)
H_PWRGD (12)
H_CPUSLP# (6,12)
PSI# (37)
H_PWRGD is CMOS driving by ICH

TO VRD

LE4 A: Modify circuit

XDP_TMS R147 54.9/F_4
XDP_TDI R149 54.9/F_4
XDP_BPM#5 R145 54.9/F_4
XDP_TCK R146 54.9/F_4
XDP_TRST# R148 54.9/F_4

XDP PU_R < 0.2"

Why BMP5 need PH ?

XDP_TCK PD 27.4/1% ?
XDP_TRST PD 510ohm /5% ?
XDP_TDI PU 150ohm /1.05V
XDP_TMS PU 39.2/1%?
XDP_TDO PU 54.9ohm?
For ITP700

XDP_DBRESET# R454 *54.9/F_4 R235 0/F_4 +1.05V → SYS_RST# (14)

LE4 B: Add R235 in BOM

+1.05V → R455 *330_4 → H_PROCHOT# → Q10 *MMBT3904 → PH_PROCHOT# (37)

LE4 B: Change netname

+1.05V / +3V_S5 → R223 *1K_4 / R209 *10K_4 → PM_THRMTRIP# → Q13 *MMBT3904 → THERM_CPUDIE_L# → R463 *0_4 → THERM_CPUDIE# (30)

LE4 B: del R463 in BOM

+5VRUN → R456 100K_4 → Q12 DTC144EUA (30) FANLESS#
Q11 E@2N7002K → THERMATRIP_VGA# (19)
H_PROCHOT# → Q34 2N7002K

LE4 A: Add new circuit with

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+1.05V
C379 0.1U_4 C316 0.1U_4 C381 0.1U_4 C317 0.1U_4 C286 0.1U_4 C285 0.1U_4

VCC_CORE
CH6222M9A01
22UF/10V/X5R
C319 22U_8 C368 22U_8 C372 22U_8 C363 22U_8
C335 22U_8 C328 22U_8 C370 22U_8 C378 22U_8
C354 22U_8 C371 22U_8 C380 22U_8 C339 22U_8
C360 22U_8 C369 22U_8 C357 22U_8 C349 22U_8
C382 22U_8 C334 22U_8 C332 22U_8 C377 22U_8
C345 22U_8 C346 22U_8 C376 22U_8 C352 22U_8
C362 22U_8 C375 22U_8 C373 22U_8 C337 22U_8
C329 22U_8 C365 22U_8 C356 22U_8 C331 22U_8

U38C

A7	VCC[001]	VCC[068]	AB20		
A9	VCC[002]	VCC[069]	AB7		
A10	VCC[003]	VCC[070]	AC7		
A12	VCC[004]	VCC[071]	AC9		
A13	VCC[005]	VCC[072]	AC12		
A15	VCC[006]	VCC[073]	AC13		
A17	VCC[007]	VCC[074]	AC15		
A18	VCC[008]	VCC[075]	AC17		
A20	VCC[009]	VCC[076]	AC18		
B7	VCC[010]	VCC[077]	AD7		
B9	VCC[011]	VCC[078]	AD9		
B10	VCC[012]	VCC[079]	AD10		
B12	VCC[013]	VCC[080]	AD12		
B14	VCC[014]	VCC[081]	AD14		
B15	VCC[015]	VCC[082]	AD15		
B17	VCC[016]	VCC[083]	AD17		
B18	VCC[017]	VCC[084]	AD18		
B20	VCC[018]	VCC[085]	AE9		
C9	VCC[019]	VCC[086]	AE10		
C10	VCC[020]	VCC[087]	AE12		
C12	VCC[021]	VCC[088]	AE13		
C13	VCC[022]	VCC[089]	AE15		
C15	VCC[023]	VCC[090]	AE17		
C17	VCC[024]	VCC[091]	AE18		
C18	VCC[025]	VCC[092]	AE20		
D9	VCC[026]	VCC[093]	AF9		
D10	VCC[027]	VCC[094]	AF10		
D12	VCC[028]	VCC[095]	AF12		
D14	VCC[029]	VCC[096]	AF14		
D15	VCC[030]	VCC[097]	AF15		
D17	VCC[031]	VCC[098]	AF17		
D18	VCC[032]	VCC[099]	AF18		
E7	VCC[033]	VCC[100]	AF20		
E9	VCC[034]				
E10	VCC[035]	VCCP[01]	V6		
E12	VCC[036]	VCCP[02]	G21		
E13	VCC[037]	VCCP[03]	J6		
E15	VCC[038]	VCCP[04]	K6		
E17	VCC[039]	VCCP[05]	M6		
E18	VCC[040]	VCCP[06]	J21		
E20	VCC[041]	VCCP[07]	K21		
F7	VCC[042]	VCCP[08]	M21		
F9	VCC[043]	VCCP[09]	N21		
F10	VCC[044]	VCCP[10]	N6		
F12	VCC[045]	VCCP[11]	R21		
F14	VCC[046]	VCCP[12]	R6		
F15	VCC[047]	VCCP[13]	T21		
F17	VCC[048]	VCCP[14]	T6		
F18	VCC[049]	VCCP[15]	V21		
F20	VCC[050]	VCCP[16]	W21		
AA7	VCC[051]				
AA9	VCC[052]	VCCA	B26		
AA10	VCC[053]				
AA12	VCC[054]				
AA13	VCC[055]	VID[0]	AD6	H_VID0	H_VID0 (37)
AA15	VCC[056]	VID[1]	AE5	H_VID1	H_VID1 (37)
AA17	VCC[057]	VID[2]	AE5	H_VID2	H_VID2 (37)
AA18	VCC[058]	VID[3]	AF4	H_VID3	H_VID3 (37)
AA20	VCC[059]	VID[4]	AE3	H_VID4	H_VID4 (37)
AB9	VCC[060]	VID[5]	AF2	H_VID5	H_VID5 (37)
AC10	VCC[061]	VID[6]	AE2	H_VID6	H_VID6 (37)
AB10	VCC[062]				
AB12	VCC[063]				
AB14	VCC[064]				
AB15	VCC[065]	VCCSENSE	AF7	VCCSENSE	VCCSENSE (37)
AB17	VCC[066]				
AB18	VCC[067]	VSSSENSE	AE7	VSSSENSE	VSSSENSE (37)

PZ47903-2741-01

+1.05V
VCC_CORE
+1.5V
+1.05V (4,6,7,9,10,12,15,38,40)
VCC_CORE (37,40)
+1.5V (7,9,10,13,15,27,38,40)

+1.05V
C289 330U/2.5V/ESR-9/POS
ESR :12m ohm

+1.5V
C401 0.01U_4 C402 10U/10V_8

+1.5V
R167 100_4
VCCSENSE (37)
VSSSENSE (37)
Connect to PWM , special layout
R162 100_4
Use 1% R

U38D

A4	VSS[001]	VSS[082]	P6		
A8	VSS[002]	VSS[083]	P21		
A11	VSS[003]	VSS[084]	P24		
A14	VSS[004]	VSS[085]	R2		
A16	VSS[005]	VSS[086]	R5		
A19	VSS[006]	VSS[087]	R22		
A23	VSS[007]	VSS[088]	R25		
A26	VSS[008]	VSS[089]	T1		
B6	VSS[009]	VSS[090]	T4		
B8	VSS[010]	VSS[091]	T23		
B11	VSS[011]	VSS[092]	T26		
B13	VSS[012]	VSS[093]	U3		
B16	VSS[013]	VSS[094]	U6		
B19	VSS[014]	VSS[095]	U21		
B21	VSS[015]	VSS[096]	U24		
B24	VSS[016]	VSS[097]	V2		
C5	VSS[017]	VSS[098]	V5		
C8	VSS[018]	VSS[099]	V22		
C11	VSS[019]	VSS[100]	V25		
C14	VSS[020]	VSS[101]	W1		
C16	VSS[021]	VSS[102]	W4		
C19	VSS[022]	VSS[103]	W23		
C2	VSS[023]	VSS[104]	W26		
C22	VSS[024]	VSS[105]	Y3		
C25	VSS[025]	VSS[106]	Y6		
D1	VSS[026]	VSS[107]	Y21		
D4	VSS[027]	VSS[108]	Y24		
D8	VSS[028]	VSS[109]	AA2		
D11	VSS[029]	VSS[110]	AA5		
D13	VSS[030]	VSS[111]	AA8		
D16	VSS[031]	VSS[112]	AA11		
D19	VSS[032]	VSS[113]	AA14		
D23	VSS[033]	VSS[114]	AA16		
D26	VSS[034]	VSS[115]	AA19		
E3	VSS[035]	VSS[116]	AA22		
E6	VSS[036]	VSS[117]	AA25		
E8	VSS[037]	VSS[118]	AB1		
E11	VSS[038]	VSS[119]	AB4		
E14	VSS[039]	VSS[120]	AB8		
E16	VSS[040]	VSS[121]	AB11		
E19	VSS[041]	VSS[122]	AB13		
E21	VSS[042]	VSS[123]	AB16		
E24	VSS[043]	VSS[124]	AB19		
F5	VSS[044]	VSS[125]	AB23		
F8	VSS[045]	VSS[126]	AB26		
F11	VSS[046]	VSS[127]	AC3		
F13	VSS[047]	VSS[128]	AC6		
F16	VSS[048]	VSS[129]	AC8		
F19	VSS[049]	VSS[130]	AC11		
F2	VSS[050]	VSS[131]	AC14		
F22	VSS[051]	VSS[132]	AC16		
F25	VSS[052]	VSS[133]	AC19		
G4	VSS[053]	VSS[134]	AC21		
G1	VSS[054]	VSS[135]	AC24		
G23	VSS[055]	VSS[136]	AD2		
G26	VSS[056]	VSS[137]	AD5		
H3	VSS[057]	VSS[138]	AD8		
H6	VSS[058]	VSS[139]	AD11		
H21	VSS[059]	VSS[140]	AD13		
H24	VSS[060]	VSS[141]	AD16		
J2	VSS[061]	VSS[142]	AD19		
J5	VSS[062]	VSS[143]	AD22		
J22	VSS[063]	VSS[144]	AD25		
J25	VSS[064]	VSS[145]	AE1		
K1	VSS[065]	VSS[146]	AE4		
K4	VSS[066]	VSS[147]	AE8		
K23	VSS[067]	VSS[148]	AE11		
K26	VSS[068]	VSS[149]	AE14		
L3	VSS[069]	VSS[150]	AE16		
L6	VSS[070]	VSS[151]	AE19		
L21	VSS[071]	VSS[152]	AE23		
L24	VSS[072]	VSS[153]	AE26		
M2	VSS[073]	VSS[154]	AE3		
M5	VSS[074]	VSS[155]	AE6		
M22	VSS[075]	VSS[156]	AE8		
M25	VSS[076]	VSS[157]	AE11		
N1	VSS[077]	VSS[158]	AE13		
N4	VSS[078]	VSS[159]	AE16		
N23	VSS[079]	VSS[160]	AE19		
N26	VSS[080]	VSS[161]	AF21		
P3	VSS[081]	VSS[162]	AF24		

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LE4 C:

+3VRUN
Q16 2N7002K
(30,35) MBDATA — LM86_SMD — LM86_SMD (19)
Q15 2N7002K
(30,35) MBCLK — LM86_SMC — LM86_SMC (19)

change to 0805

CRB use 8.2k PH

LE4 B:

Solve can't power on isuue
So change R220 pull high and
R211 pull high to thermal
circuit.(12/12/2005)

+3VRUN
R220 200_4
25mils
R211 10K_4
LM86VCC
C406 0.1U_4 10/20mils
R232 10K_4 R231 10K_4
U19

SCLK	8	1	VCC
SDA	7	2	DXP
ALERT#	6	3	DXN
OVERT#	4	5	GND

MAX6657/GMT-781
ADDRESS: 98H
LM86_SMC
LM86_SMD
H_THERMDA — H_THERMDA (4)
C400 2200P/50V_4
H_THERMDC — H_THERMDC (4)
(14) THERM_ALERT# — THERM_ALERT#

LE4 C:

+3VRUN
R214 *10K_4
R208 *0_6
1999_SHDN# (39)

LE4 C:
Del R208

LE4 A:
Add new circuit
with H/W solution

LE4 B:
Del R224, C408, Q14
and Q17 in BOM

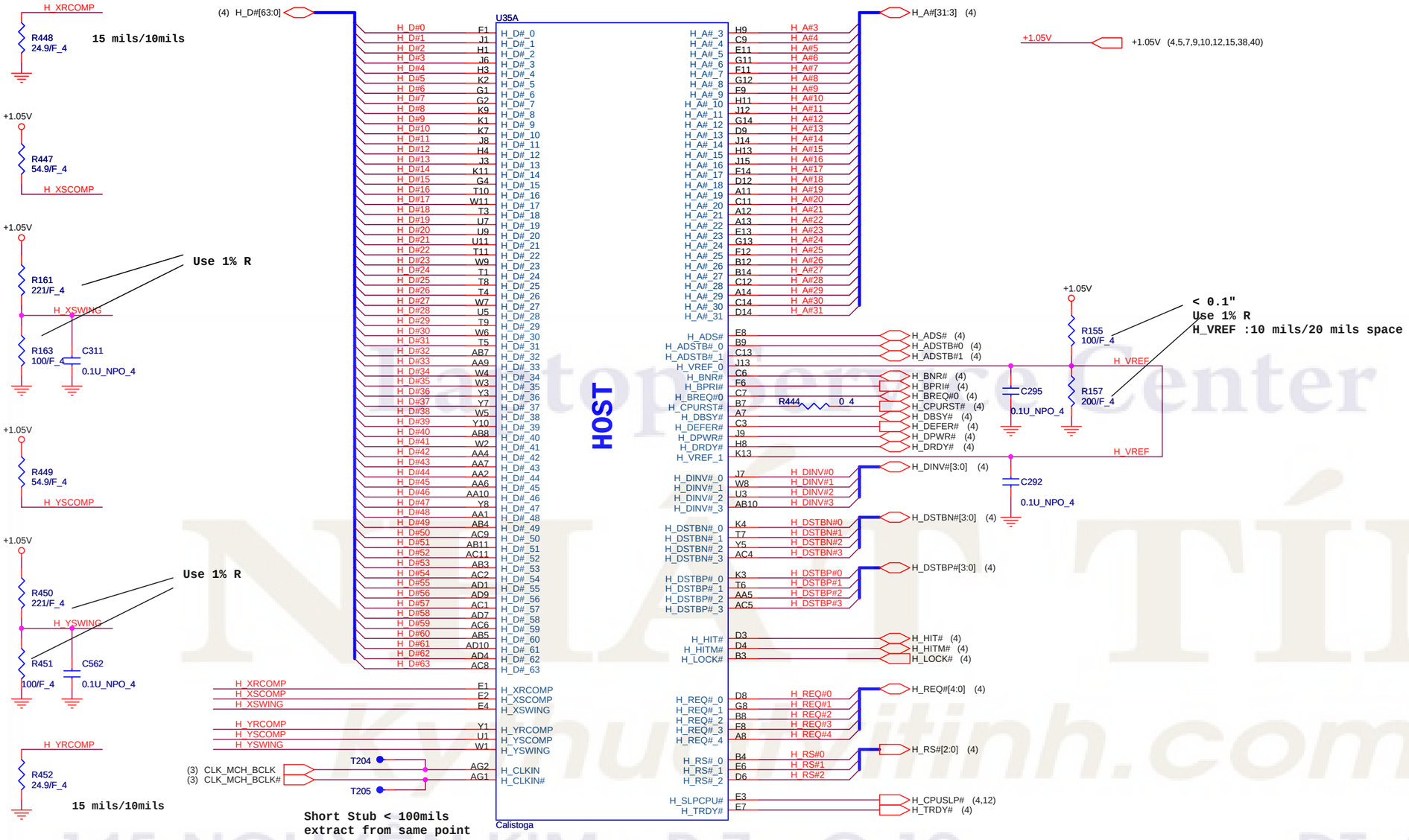
R224 *1M/F_4
Q17 *2N7002K
Q14 *2N7002K
C408 *0.1U_4
SYS_SHDN#

add hardware protect

Unstall R267 , Q28 , Q26 for Intel sighting -> CPU thermal die bug /0506

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	Yonah/Merom (Power/NC)	1A
Date: Tuesday, March 14, 2006	Sheet 5 of 42	



PROJECT : LE4		
Quanta Computer Inc.		
Size	Document Number: Calistoga_A (Host)	Rev: 1A
Date: Tuesday, March 14, 2006	Sheet 6 of 42	

Check

U35B

RSVD_0 RSVD_1 RSVD_2 RSVD_3 RSVD_4 RSVD_5 RSVD_6 RSVD_7 RSVD_8 RSVD_9 RSVD_10 RSVD_11 RSVD_12 RSVD_13 RSVD_14 RSVD_15

T21 MCH_RSVD_1 T32
T25 MCH_RSVD_2 R32
T24 MCH_RSVD_3 F3
T72 MCH_RSVD_4 F7
T68 MCH_RSVD_5 AG11
T63 MCH_RSVD_6 AF11
T60 MCH_RSVD_7 H7
T66 MCH_RSVD_8 J19
T42 MCH_RSVD_9 K30
T23 TV_DCONSEL0 J29
T31 TV_DCONSEL1 A41
T173 MCH_RSVD_11 A35
T183 MCH_RSVD_12 A34
T184 MCH_RSVD_13 D28
T180 MCH_RSVD_14 D27
T36 MCH_RSVD_15

RSVD

(3,4) CPU_MCH_BSEL0 MCH_BSEL0 K16
(3,4) CPU_MCH_BSEL1 MCH_BSEL1 K18
(3,4) CPU_MCH_BSEL2 MCH_BSEL2 J18
T43 MCH_CFG_3 F18
T62 MCH_CFG_4 E15
T50 MCH_CFG_5 F15
MCH_CFG_6 E18
MCH_CFG_7 D19
T46 MCH_CFG_8 D16
MCH_CFG_9 G16
MCH_CFG_10 E16
MCH_CFG_11 D15
MCH_CFG_12 G15
(9) MCH_CFG_13 MCH_CFG_13 K15
T192 MCH_CFG_14 C15
T54 MCH_CFG_15 H16
MCH_CFG_16 G18
T194 MCH_CFG_17 H15
MCH_CFG_18 J25
MCH_CFG_19 K27
MCH_CFG_20 J26

CFG_0 CFG_1 CFG_2 CFG_3 CFG_4 CFG_5 CFG_6 CFG_7 CFG_8 CFG_9 CFG_10 CFG_11 CFG_12 CFG_13 CFG_14 CFG_15 CFG_16 CFG_17 CFG_18 CFG_19 CFG_20

CFG

(14) PM_BMBUSY# G28
(16,17) PM_EXTTS#0 F25
(14,17) PM_EXTTS#1 H26
(4,12) PM_THRMTRIP# G6
(14,37) DELAY_VR_PWRGOOD AH33
AH34
(13) PLT_RST-R# R82 100/F_4 RST IN# MCH

PM_BMBUSY# PM_EXTTS#_0 PM_EXTTS#_1 PM_THRMTRIP# PWROK RSTIN#

PM

T32 H28
T33 H27
+3VRUN R114 *10K/F_4 K28
(13) MCH_ICH_SYNC

SDVO_CTRLCLK SDVO_CTRLDATA LT_RESET#

MISC

T203 TP_MCH_NC0 D1
T178 TP_MCH_NC1 C41
T202 TP_MCH_NC2 C1
T179 TP_MCH_NC3 BA41
T181 TP_MCH_NC4 BA40
T182 TP_MCH_NC5 BA39
T71 TP_MCH_NC6 BA3
T73 TP_MCH_NC7 BA2
T201 TP_MCH_NC8 BA1
T177 TP_MCH_NC9 B41
T197 TP_MCH_NC10 B2
T176 TP_MCH_NC11 AY41
T200 TP_MCH_NC12 AY1
T175 TP_MCH_NC13 AW41
T199 TP_MCH_NC14 AW1
T174 TP_MCH_NC15 A40
T196 TP_MCH_NC16 A4
T180 TP_MCH_NC17 A39
T198 TP_MCH_NC18 A3

NC0 NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11 NC12 NC13 NC14 NC15 NC16 NC17 NC18

NC

Calistoga

SM_CK_0 AY35 M_CLK_DDR0 (16)
SM_CK_1 AR1 M_CLK_DDR1 (16)
SM_CK_2 AW7 M_CLK_DDR2 (16)
SM_CK_3 AW40 M_CLK_DDR3 (16)

SM_CK#_0 AW35 M_CLK_DDR#0 (16)
SM_CK#_1 AT1 M_CLK_DDR#1 (16)
SM_CK#_2 AY7 M_CLK_DDR#2 (16)
SM_CK#_3 AY40 M_CLK_DDR#3 (16)

SM_CKE_0 AU20 M_CKE0 (16,17)
SM_CKE_1 AT20 M_CKE1 (16,17)
SM_CKE_2 BA29 M_CKE2 (16,17)
SM_CKE_3 AY29 M_CKE3 (16,17)

SM_CS#_0 AW13 M_CS#0 (16,17)
SM_CS#_1 AW12 M_CS#1 (16,17)
SM_CS#_2 AY21 M_CS#2 (16,17)
SM_CS#_3 AW21 M_CS#3 (16,17)

SM_OCDCOMP_0 AL20 M_OCDCOMP_0
SM_OCDCOMP_1 AF10 M_OCDCOMP_1

SM_ODT_0 BA13 M_ODT0 (16,17)
SM_ODT_1 BA12 M_ODT1 (16,17)
SM_ODT_2 AY20 M_ODT2 (16,17)
SM_ODT_3 AU21 M_ODT3 (16,17)

SM_RCOMP# AV9 M_RCOMP#
SM_RCOMP AT9 M_RCOMP

SM_VREF_0 AK1 SMDDR_VREF_MCH
SM_VREF_1 AK41

DDR MUXING

G_CLKIN# AF33
G_CLKIN AG33
D_REFCLKIN# A27 R_DOT96#
D_REFCLKIN A26 R_DOT96
D_REFSSCLKIN# C40 RDREFSSCLK#
D_REFSSCLKIN D41 RDREFSSCLK

CLK_PCIE_3GPLL# (3)
CLK_PCIE_3GPLL (3)
DOT96# (3)
DOT96 (3)
DREFSSCLK# (3)
DREFSSCLK (3)

CLK

DMI_RXN_0 AE35 DMI_TXN0
DMI_RXN_1 AE39 DMI_TXN1
DMI_RXN_2 AG35 DMI_TXN2
DMI_RXN_3 AH39 DMI_TXN3

DMI_RXP_0 AC35 DMI_TXP0
DMI_RXP_1 AE39 DMI_TXP1
DMI_RXP_2 AE35 DMI_TXP2
DMI_RXP_3 AG39 DMI_TXP3

DMI_TXN_0 AE37 DMI_RXN0
DMI_TXN_1 AF41 DMI_RXN1
DMI_TXN_2 AG37 DMI_RXN2
DMI_TXN_3 AH41 DMI_RXN3

DMI_TXP_0 AC37 DMI_RXP0
DMI_TXP_1 AE41 DMI_RXP1
DMI_TXP_2 AF37 DMI_RXP2
DMI_TXP_3 AG41 DMI_RXP3

DMI

SMDDR_VREF_MCH
R568 *0_4 V_DDR_MCH_REF
R173 0_4 SMDDR_VREF

LE4 B: add R568

0402
R172 10K/F_6 1.8VSUS
R171 10K/F_6 0402

Change R172 AND R171 SIZE from 0402 to 0603

(22) LCD_BKLTCTL R391 I@0_4 D32
(19,22,30) LCD_BLON_EC R89 I@0_4 J30
L_CLKCTLA H30
T38 L_CLKCTLB H29
T34 (22) EDIDCLK R119 I@0_4 G26
(22) EDIDDATA R115 I@0_4 G25
L_DDC_DATA
L_IBG B38
L_VBG C35
T22 (22) DISP_ON R81 I@0_4 VDDEN F32
L_VDDEN C33
R569 I@0_4 L_VREFH C32
L_VREFL

LE4 B: Use 1% R add R569

15mils/15mils

R156 *40.2/F_4
R120 *40.2/F_4

Layout as short as passable
NC from WW45

Shall be 10K divider of 1.8V_SUS

LA_CLK# A33
LA_CLK A32
T37 LB_CLK# E27
T39 LB_CLK E26

LA_DATAN0 C37
LA_DATAN1 B35
LA_DATAN2 A37

LA_DATAP0 B37
LA_DATAP1 B34
LA_DATAP2 A36

T30 G30
T28 LB_DATA#_1 D30
T26 LB_DATA#_2 F29

T29 F30
T27 LB_DATA_1 D29
T35 LB_DATA_2 F28

LVDS

LE4 A: As below

R591 I@0_6 TV_IRTN
R428 I@0_4 TV_COMP1
R423 I@0_4 TV_Y/G1
R419 I@0_4 TV_C/R1
R421 I@150/F_4
R425 I@150/F_4
R430 I@150/F_4
R124 I@4.99K/F_4 TVIREF J20

(23) TV_COMP
(23) TV_Y/G
(23) TV_C/R

TV_DACA_OUT A16
TV_DACB_OUT C18
TV_DACC_OUT A19
TV_IREF B16
TV_IRTNA B18
TV_IRTNB B19
TV_IRTNC

TV

< 0.1" . 15mils/15mils space

R590 I@0_6 CRT_RGB#
R406 I@0_4 CRT_BLUE
R411 I@0_4 CRT_GREEN
R415 I@0_4 CRT_RED
R416 I@150/F_4
R412 I@150/F_4
R407 I@150/F_4
R105 I@0_4 CRT_DDC_CLK
R98 I@0_4 CRT_DDC_DAT

(23) CRT_B_COM
(23) CRT_G_COM
(23) CRT_R_COM
(23) DDCCLK
(23) DDCDAT

CRT_BLUE F23
CRT_BLUE# D23
CRT_GREEN C22
CRT_GREEN# B22
CRT_RED A21
CRT_RED# B21
CRT_DDC_CLK C26
CRT_DDC_DATA C25
CRT_HSYNC G23
CRT_IREF J22
CRT_VSYNC H23

VGA

Calistoga

I@39/F_4
R116 HSYNC1
R126 I@255/F_4 CRTIREF
R112 I@39/F_4 VSYNC1

(23) HSYNC_COM
(23) VSYNC_COM

< 0.1" . 15mils/15mils space
use 1% R

DMI_TXP[3:0] (13)
DMI_TXN[3:0] (13)
DMI_RXP[3:0] (13)
DMI_RXN[3:0] (13)

U35C

L_BKLTCTL L_BKLTEN L_CLKCTLA L_CLKCTLB L_DDC_CLK L_DDC_DATA L_IBG L_VBG L_VDDEN L_VREFH L_VREFL

LA_CLK# LA_CLK LB_CLK# LB_CLK

LA_DATA#_0 LA_DATA#_1 LA_DATA#_2 LA_DATA_0 LA_DATA_1 LA_DATA_2

LB_DATA#_0 LB_DATA#_1 LB_DATA#_2 LB_DATA_0 LB_DATA_1 LB_DATA_2

TV_DACA_OUT TV_DACB_OUT TV_DACC_OUT TV_IREF TV_IRTNA TV_IRTNB TV_IRTNC

CRT_BLUE CRT_BLUE# CRT_GREEN CRT_GREEN# CRT_RED CRT_RED# CRT_DDC_CLK CRT_DDC_DATA CRT_HSYNC CRT_IREF CRT_VSYNC

Calistoga

+3VRUN

L_CLKCTLA R108 I@10K/F_4
L_CLKCTLB R102 I@10K/F_4

20mils/20mils space

+V1.5_PCIE

EXP_A_COMPI D40 EXP_A_COMPX R67 24.9/F_4
EXP_A_COMPO D38

EXP_A_RXN_0 F34 PCIE_MRX_GTX_N0
EXP_A_RXN_1 G38 PCIE_MRX_GTX_N1
EXP_A_RXN_2 H34 PCIE_MRX_GTX_N2
EXP_A_RXN_3 J38 PCIE_MRX_GTX_N3
EXP_A_RXN_4 L34 PCIE_MRX_GTX_N4
EXP_A_RXN_5 M38 PCIE_MRX_GTX_N5
EXP_A_RXN_6 N34 PCIE_MRX_GTX_N6
EXP_A_RXN_7 P38 PCIE_MRX_GTX_N7
EXP_A_RXN_8 R34 PCIE_MRX_GTX_N8
EXP_A_RXN_9 T38 PCIE_MRX_GTX_N9
EXP_A_RXN_10 V34 PCIE_MRX_GTX_N10
EXP_A_RXN_11 W38 PCIE_MRX_GTX_N11
EXP_A_RXN_12 Y34 PCIE_MRX_GTX_N12
EXP_A_RXN_13 AA38 PCIE_MRX_GTX_N13
EXP_A_RXN_14 AB34 PCIE_MRX_GTX_N14
EXP_A_RXN_15 AC38 PCIE_MRX_GTX_N15

PCIE_MRX_GTX_N[0..15] (18)

EXP_A_RXP_0 D34 PCIE_MRX_GTX_P0
EXP_A_RXP_1 F38 PCIE_MRX_GTX_P1
EXP_A_RXP_2 G34 PCIE_MRX_GTX_P2
EXP_A_RXP_3 H38 PCIE_MRX_GTX_P3
EXP_A_RXP_4 J34 PCIE_MRX_GTX_P4
EXP_A_RXP_5 L38 PCIE_MRX_GTX_P5
EXP_A_RXP_6 M34 PCIE_MRX_GTX_P6
EXP_A_RXP_7 N38 PCIE_MRX_GTX_P7
EXP_A_RXP_8 P34 PCIE_MRX_GTX_P8
EXP_A_RXP_9 R38 PCIE_MRX_GTX_P9
EXP_A_RXP_10 T34 PCIE_MRX_GTX_P10
EXP_A_RXP_11 V38 PCIE_MRX_GTX_P11
EXP_A_RXP_12 W34 PCIE_MRX_GTX_P12
EXP_A_RXP_13 Y38 PCIE_MRX_GTX_P13
EXP_A_RXP_14 AA34 PCIE_MRX_GTX_P14
EXP_A_RXP_15 AB38 PCIE_MRX_GTX_P15

PCIE_MRX_GTX_P[0..15] (18)

EXP_A_TXN_0 F36 PCIE_MTX_GRX_C_N0
EXP_A_TXN_1 G40 PCIE_MTX_GRX_C_N1
EXP_A_TXN_2 H36 PCIE_MTX_GRX_C_N2
EXP_A_TXN_3 J40 PCIE_MTX_GRX_C_N3
EXP_A_TXN_4 L36 PCIE_MTX_GRX_C_N4
EXP_A_TXN_5 M40 PCIE_MTX_GRX_C_N5
EXP_A_TXN_6 N36 PCIE_MTX_GRX_C_N6
EXP_A_TXN_7 P40 PCIE_MTX_GRX_C_N7
EXP_A_TXN_8 R36 PCIE_MTX_GRX_C_N8
EXP_A_TXN_9 T40 PCIE_MTX_GRX_C_N9
EXP_A_TXN_10 V36 PCIE_MTX_GRX_C_N10
EXP_A_TXN_11 W40 PCIE_MTX_GRX_C_N11
EXP_A_TXN_12 Y36 PCIE_MTX_GRX_C_N12
EXP_A_TXN_13 AA40 PCIE_MTX_GRX_C_N13
EXP_A_TXN_14 AB36 PCIE_MTX_GRX_C_N14
EXP_A_TXN_15 AC40 PCIE_MTX_GRX_C_N15

EXP_A_TXP_0 D36 PCIE_MTX_GRX_C_P0
EXP_A_TXP_1 F40 PCIE_MTX_GRX_C_P1
EXP_A_TXP_2 G36 PCIE_MTX_GRX_C_P2
EXP_A_TXP_3 H40 PCIE_MTX_GRX_C_P3
EXP_A_TXP_4 J36 PCIE_MTX_GRX_C_P4
EXP_A_TXP_5 L40 PCIE_MTX_GRX_C_P5
EXP_A_TXP_6 M36 PCIE_MTX_GRX_C_P6
EXP_A_TXP_7 N40 PCIE_MTX_GRX_C_P7
EXP_A_TXP_8 P36 PCIE_MTX_GRX_C_P8
EXP_A_TXP_9 R40 PCIE_MTX_GRX_C_P9
EXP_A_TXP_10 T36 PCIE_MTX_GRX_C_P10
EXP_A_TXP_11 V40 PCIE_MTX_GRX_C_P11
EXP_A_TXP_12 W36 PCIE_MTX_GRX_C_P12
EXP_A_TXP_13 Y40 PCIE_MTX_GRX_C_P13
EXP_A_TXP_14 AA36 PCIE_MTX_GRX_C_P14
EXP_A_TXP_15 AB40 PCIE_MTX_GRX_C_P15

PCI-EXPRESS GRAPHICS

+1.5V

TV_COMP1 R576 E@0_4
TV_Y/G1 R577 E@0_4
TV_C/R1 R578 E@0_4
TVIREF R579 E@0_4
TV_IRTN R580 E@0_4
TV_IRTN R581 E@0_4

+1.05V

CRT_BLUE R582 E@0_4
CRT_GREEN R583 E@0_4
CRT_RED R584 E@0_4
CRT_RGB# R585 E@0_4
CRT_RGB# R586 E@0_4
CRTIREF R587 E@0_4
HSYNC1 R588 E@0_4
VSYNC1 R589 E@0_4

LE4 B:
945PM contact power and GND plane
945GM/940GML Contact GND plane

1.8VSUS
R160 80.6/F_4
M_RCOMP#
15mils/10mils

+3VRUN
R106 10K/F_4 PM_EXTTS#0
R113 *10K/F_4 PM_EXTTS#1

M_RCOMP
R159 80.6/F_4

MCH_CFG_9 R125 *10K/F_4 +3VRUN

+V1.5_PCIE (10)
+3VRUN (3,5,9,10,12,13,14,15,16,17,18,19,20,22,23,26,27,28,30,31,32,33,36,40,41)
SMDDR_VREF (16)
1.8VSUS (9,16,36,40,41)

(9) MCH_CFG_[12:5] MCH_CFG_[12:5]
(9) MCH_CFG_[20:16] MCH_CFG_[20:16]

L_IBG R74 I@1.5K_4
L_VDDEN R86 I@100K_4

RP32 I@4P2R-S-0
(19,22) LCD_ACLK- 2 1 LA_CLK#
(19,22) LCD_ACLK+ 4 3 LA_CLK

RP29 I@4P2R-S-0
(19,22) LCD_A0- 2 1 LA_DATAN0
(19,22) LCD_A0+ 4 3 LA_DATAP0

RP31 I@4P2R-S-0
(19,22) LCD_A1- 2 1 LA_DATAN1
(19,22) LCD_A1+ 4 3 LA_DATAP1

RP30 I@4P2R-S-0
(19,22) LCD_A2- 2 1 LA_DATAN2
(19,22) LCD_A2+ 4 3 LA_DATAP2

PCIE_MTX_GRX_N[0..15] (18)

C187 E@0.1U_P_4 PCIE_MTX_GRX_C_N0 PCIE_MTX_GRX_N0
C525 E@0.1U_P_4 PCIE_MTX_GRX_C_N1 PCIE_MTX_GRX_N1
C189 E@0.1U_P_4 PCIE_MTX_GRX_C_N2 PCIE_MTX_GRX_N2
C527 E@0.1U_P_4 PCIE_MTX_GRX_C_N3 PCIE_MTX_GRX_N3
C191 E@0.1U_P_4 PCIE_MTX_GRX_C_N4 PCIE_MTX_GRX_N4
C529 E@0.1U_P_4 PCIE_MTX_GRX_C_N5 PCIE_MTX_GRX_N5
C193 E@0.1U_P_4 PCIE_MTX_GRX_C_N6 PCIE_MTX_GRX_N6
C531 E@0.1U_P_4 PCIE_MTX_GRX_C_N7 PCIE_MTX_GRX_N7
C195 E@0.1U_P_4 PCIE_MTX_GRX_C_N8 PCIE_MTX_GRX_N8
C533 E@0.1U_P_4 PCIE_MTX_GRX_C_N9 PCIE_MTX_GRX_N9
C197 E@0.1U_P_4 PCIE_MTX_GRX_C_N10 PCIE_MTX_GRX_N10
C519 E@0.1U_P_4 PCIE_MTX_GRX_C_N11 PCIE_MTX_GRX_N11
C199 E@0.1U_P_4 PCIE_MTX_GRX_C_N12 PCIE_MTX_GRX_N12
C521 E@0.1U_P_4 PCIE_MTX_GRX_C_N13 PCIE_MTX_GRX_N13
C201 E@0.1U_P_4 PCIE_MTX_GRX_C_N14 PCIE_MTX_GRX_N14
C523 E@0.1U_P_4 PCIE_MTX_GRX_C_N15 PCIE_MTX_GRX_N15

PCIE_MTX_GRX_P[0..15] (18)

C186 E@0.1U_P_4 PCIE_MTX_GRX_C_P0 PCIE_MTX_GRX_P0
C524 E@0.1U_P_4 PCIE_MTX_GRX_C_P1 PCIE_MTX_GRX_P1
C188 E@0.1U_P_4 PCIE_MTX_GRX_C_P2 PCIE_MTX_GRX_P2
C526 E@0.1U_P_4 PCIE_MTX_GRX_C_P3 PCIE_MTX_GRX_P3
C190 E@0.1U_P_4 PCIE_MTX_GRX_C_P4 PCIE_MTX_GRX_P4
C528 E@0.1U_P_4 PCIE_MTX_GRX_C_P5 PCIE_MTX_GRX_P5
C192 E@0.1U_P_4 PCIE_MTX_GRX_C_P6 PCIE_MTX_GRX_P6
C530 E@0.1U_P_4 PCIE_MTX_GRX_C_P7 PCIE_MTX_GRX_P7
C194 E@0.1U_P_4 PCIE_MTX_GRX_C_P8 PCIE_MTX_GRX_P8
C532 E@0.1U_P_4 PCIE_MTX_GRX_C_P9 PCIE_MTX_GRX_P9
C196 E@0.1U_P_4 PCIE_MTX_GRX_C_P10 PCIE_MTX_GRX_P10
C518 E@0.1U_P_4 PCIE_MTX_GRX_C_P11 PCIE_MTX_GRX_P11
C198 E@0.1U_P_4 PCIE_MTX_GRX_C_P12 PCIE_MTX_GRX_P12
C520 E@0.1U_P_4 PCIE_MTX_GRX_C_P13 PCIE_MTX_GRX_P13
C200 E@0.1U_P_4 PCIE_MTX_GRX_C_P14 PCIE_MTX_GRX_P14
C522 E@0.1U_P_4 PCIE_MTX_GRX_C_P15 PCIE_MTX_GRX_P15

DC Blocked Cap.

Near to North Bridge

+1.5V

R_DOT96# R95 E@0_4
R_DOT96 R107 E@0_4
RDREFSSCLK# R100 E@0_4
RDREFSSCLK R90 E@0_4

SMDDR_VREF_MCH
C333 0.1U_4
C536 0.1U_4

LE4 A:
940GML/945GM with clock signal
945PM with power and GND plan

LE4 B:
Change Netname

PROJECT : LE4
Quanta Computer Inc.

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	Calistoga_B (VGA,DMI)	1A
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(16) M_A_DQ[63:0]

U35D

DDR SYSTEM MEMORY A

M_A_DQ0	AJ35	SA_DQ0	
M_A_DQ1	AJ34	SA_DQ1	
M_A_DQ2	AM31	SA_DQ2	
M_A_DQ3	AM33	SA_DQ3	
M_A_DQ4	AJ36	SA_DQ4	
M_A_DQ5	AK35	SA_DQ5	
M_A_DQ6	AJ32	SA_DQ6	
M_A_DQ7	AH31	SA_DQ7	
M_A_DQ8	AN35	SA_DQ8	
M_A_DQ9	AP33	SA_DQ9	
M_A_DQ10	AR31	SA_DQ10	
M_A_DQ11	AP31	SA_DQ11	
M_A_DQ12	AN38	SA_DQ12	
M_A_DQ13	AM36	SA_DQ13	
M_A_DQ14	AM34	SA_DQ14	
M_A_DQ15	AN33	SA_DQ15	
M_A_DQ16	AK26	SA_DQ16	
M_A_DQ17	AL27	SA_DQ17	
M_A_DQ18	AM26	SA_DQ18	
M_A_DQ19	AN24	SA_DQ19	
M_A_DQ20	AK28	SA_DQ20	
M_A_DQ21	AL28	SA_DQ21	
M_A_DQ22	AM24	SA_DQ22	
M_A_DQ23	AP26	SA_DQ23	
M_A_DQ24	AP23	SA_DQ24	
M_A_DQ25	AL22	SA_DQ25	
M_A_DQ26	AP21	SA_DQ26	
M_A_DQ27	AN20	SA_DQ27	
M_A_DQ28	AL23	SA_DQ28	
M_A_DQ29	AP24	SA_DQ29	
M_A_DQ30	AP20	SA_DQ30	
M_A_DQ31	AT21	SA_DQ31	
M_A_DQ32	AR12	SA_DQ32	
M_A_DQ33	AR14	SA_DQ33	
M_A_DQ34	AP13	SA_DQ34	
M_A_DQ35	AP12	SA_DQ35	
M_A_DQ36	AT13	SA_DQ36	
M_A_DQ37	AT12	SA_DQ37	
M_A_DQ38	AL14	SA_DQ38	
M_A_DQ39	AL12	SA_DQ39	
M_A_DQ40	AK9	SA_DQ40	
M_A_DQ41	AN7	SA_DQ41	
M_A_DQ42	AK8	SA_DQ42	
M_A_DQ43	AK7	SA_DQ43	
M_A_DQ44	AP9	SA_DQ44	
M_A_DQ45	AN9	SA_DQ45	
M_A_DQ46	AT5	SA_DQ46	
M_A_DQ47	AL5	SA_DQ47	
M_A_DQ48	AY2	SA_DQ48	
M_A_DQ49	AW2	SA_DQ49	
M_A_DQ50	AP1	SA_DQ50	
M_A_DQ51	AN2	SA_DQ51	
M_A_DQ52	AV2	SA_DQ52	
M_A_DQ53	AT3	SA_DQ53	
M_A_DQ54	AN1	SA_DQ54	
M_A_DQ55	AL2	SA_DQ55	
M_A_DQ56	AG7	SA_DQ56	
M_A_DQ57	AF9	SA_DQ57	
M_A_DQ58	AG4	SA_DQ58	
M_A_DQ59	AF6	SA_DQ59	
M_A_DQ60	AG9	SA_DQ60	
M_A_DQ61	AH6	SA_DQ61	
M_A_DQ62	AF4	SA_DQ62	
M_A_DQ63	AF8	SA_DQ63	

SA_BS_0	AU12	M_A_BS#0	M_A_BS#0 (16,17)
SA_BS_1	AV14	M_A_BS#1	M_A_BS#1 (16,17)
SA_BS_2	BA20	M_A_BS#2	M_A_BS#2 (16,17)
			M_A_CAS# (16,17)
SA_CAS#	AY13	M_A_CAS#	
SA_DM_0	AJ33	M_A_DM0	M_A_DM[7:0] (16)
SA_DM_1	AM35	M_A_DM1	
SA_DM_2	AL26	M_A_DM2	
SA_DM_3	AN22	M_A_DM3	
SA_DM_4	AM14	M_A_DM4	
SA_DM_5	AL9	M_A_DM5	
SA_DM_6	AR3	M_A_DM6	
SA_DM_7	AH4	M_A_DM7	
SA_DQS_0	AK33	M_A_DQS0	M_A_DQS[7:0] (16)
SA_DQS_1	AT33	M_A_DQS1	
SA_DQS_2	AN28	M_A_DQS2	
SA_DQS_3	AM22	M_A_DQS3	
SA_DQS_4	AN12	M_A_DQS4	
SA_DQS_5	AN8	M_A_DQS5	
SA_DQS_6	AP3	M_A_DQS6	
SA_DQS_7	AG5	M_A_DQS7	
SA_DQS#_0	AK32	M_A_DQS#0	M_A_DQS#[7:0] (16)
SA_DQS#_1	AU33	M_A_DQS#1	
SA_DQS#_2	AN27	M_A_DQS#2	
SA_DQS#_3	AM21	M_A_DQS#3	
SA_DQS#_4	AM12	M_A_DQS#4	
SA_DQS#_5	AL8	M_A_DQS#5	
SA_DQS#_6	AN3	M_A_DQS#6	
SA_DQS#_7	AH5	M_A_DQS#7	
SA_MA_0	AY16	M_A_A0	M_A_A[13:0] (16,17)
SA_MA_1	AU14	M_A_A1	
SA_MA_2	AW16	M_A_A2	
SA_MA_3	BA16	M_A_A3	
SA_MA_4	BA17	M_A_A4	
SA_MA_5	AU16	M_A_A5	
SA_MA_6	AV17	M_A_A6	
SA_MA_7	AU17	M_A_A7	
SA_MA_8	AW17	M_A_A8	
SA_MA_9	AT16	M_A_A9	
SA_MA_10	AU13	M_A_A10	
SA_MA_11	AT17	M_A_A11	
SA_MA_12	AV20	M_A_A12	
SA_MA_13	AV12	M_A_A13	
SA_RAS#	AW14	TP_MA_RCVENIN#	M_A_RAS# (16,17)
SA_RCVENIN#	AK23	TP_MA_RCVENOUT#	T41
SA_RCVENOUT#	AK24		T40
SA_WE#	AY14		M_A_WE# (16,17)

Calistoga

(16) M_B_DQ[63:0]

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DDR SYSTEM MEMORY B

M_B_DQ0	AK39	SB_DQ0	
M_B_DQ1	AJ37	SB_DQ1	
M_B_DQ2	AP39	SB_DQ2	
M_B_DQ3	AR41	SB_DQ3	
M_B_DQ4	AJ38	SB_DQ4	
M_B_DQ5	AK38	SB_DQ5	
M_B_DQ6	AN41	SB_DQ6	
M_B_DQ7	AP41	SB_DQ7	
M_B_DQ8	AT40	SB_DQ8	
M_B_DQ9	AV41	SB_DQ9	
M_B_DQ10	AU38	SB_DQ10	
M_B_DQ11	AV38	SB_DQ11	
M_B_DQ12	AP38	SB_DQ12	
M_B_DQ13	AR40	SB_DQ13	
M_B_DQ14	AW38	SB_DQ14	
M_B_DQ15	AY38	SB_DQ15	
M_B_DQ16	BA38	SB_DQ16	
M_B_DQ17	AV36	SB_DQ17	
M_B_DQ18	AR36	SB_DQ18	
M_B_DQ19	AP36	SB_DQ19	
M_B_DQ20	BA36	SB_DQ20	
M_B_DQ21	AU36	SB_DQ21	
M_B_DQ22	AP35	SB_DQ22	
M_B_DQ23	AP34	SB_DQ23	
M_B_DQ24	AY33	SB_DQ24	
M_B_DQ25	BA33	SB_DQ25	
M_B_DQ26	AT31	SB_DQ26	
M_B_DQ27	AU29	SB_DQ27	
M_B_DQ28	AU31	SB_DQ28	
M_B_DQ29	AW31	SB_DQ29	
M_B_DQ30	AV29	SB_DQ30	
M_B_DQ31	AW29	SB_DQ31	
M_B_DQ32	AM19	SB_DQ32	
M_B_DQ33	AL19	SB_DQ33	
M_B_DQ34	AP14	SB_DQ34	
M_B_DQ35	AN14	SB_DQ35	
M_B_DQ36	AN17	SB_DQ36	
M_B_DQ37	AM16	SB_DQ37	
M_B_DQ38	AP15	SB_DQ38	
M_B_DQ39	AL15	SB_DQ39	
M_B_DQ40	AJ11	SB_DQ40	
M_B_DQ41	AH10	SB_DQ41	
M_B_DQ42	AJ9	SB_DQ42	
M_B_DQ43	AN10	SB_DQ43	
M_B_DQ44	AK13	SB_DQ44	
M_B_DQ45	AH11	SB_DQ45	
M_B_DQ46	AK10	SB_DQ46	
M_B_DQ47	AJ8	SB_DQ47	
M_B_DQ48	BA10	SB_DQ48	
M_B_DQ49	AW10	SB_DQ49	
M_B_DQ50	BA4	SB_DQ50	
M_B_DQ51	AW4	SB_DQ51	
M_B_DQ52	AY10	SB_DQ52	
M_B_DQ53	AY9	SB_DQ53	
M_B_DQ54	AW5	SB_DQ54	
M_B_DQ55	AY5	SB_DQ55	
M_B_DQ56	AV4	SB_DQ56	
M_B_DQ57	AR5	SB_DQ57	
M_B_DQ58	AK4	SB_DQ58	
M_B_DQ59	AK3	SB_DQ59	
M_B_DQ60	AT4	SB_DQ60	
M_B_DQ61	AK5	SB_DQ61	
M_B_DQ62	AJ5	SB_DQ62	
M_B_DQ63	AJ3	SB_DQ63	

SB_BS_0	AT24	M_B_BS#0	M_B_BS#0 (16,17)
SB_BS_1	AV23	M_B_BS#1	M_B_BS#1 (16,17)
SB_BS_2	AY28	M_B_BS#2	M_B_BS#2 (16,17)
		M_B_CAS#	M_B_CAS# (16,17)
SB_CAS#	AR24	M_B_DM0	M_B_DM[7:0] (16)
SB_DM_0	AK36	M_B_DM1	
SB_DM_1	AR38	M_B_DM2	
SB_DM_2	AT36	M_B_DM3	
SB_DM_3	BA31	M_B_DM4	
SB_DM_4	AL17	M_B_DM5	
SB_DM_5	AH8	M_B_DM6	
SB_DM_6	BA5	M_B_DM7	
SB_DM_7	AN4		
SB_DQS_0	AM39	M_B_DQS0	M_B_DQS[7:0] (16)
SB_DQS_1	AT39	M_B_DQS1	
SB_DQS_2	AU35	M_B_DQS2	
SB_DQS_3	AR29	M_B_DQS3	
SB_DQS_4	AR16	M_B_DQS4	
SB_DQS_5	AR10	M_B_DQS5	
SB_DQS_6	AR7	M_B_DQS6	
SB_DQS_7	AN5	M_B_DQS7	
SB_DQS#_0	AM40	M_B_DQS#0	M_B_DQS#[7:0] (16)
SB_DQS#_1	AU39	M_B_DQS#1	
SB_DQS#_2	AT35	M_B_DQS#2	
SB_DQS#_3	AP29	M_B_DQS#3	
SB_DQS#_4	AP16	M_B_DQS#4	
SB_DQS#_5	AT10	M_B_DQS#5	
SB_DQS#_6	AT7	M_B_DQS#6	
SB_DQS#_7	AP5	M_B_DQS#7	
SB_MA_0	AY23	M_B_A0	M_B_A[13:0] (16,17)
SB_MA_1	AW24	M_B_A1	
SB_MA_2	AY24	M_B_A2	
SB_MA_3	AR28	M_B_A3	
SB_MA_4	AT27	M_B_A4	
SB_MA_5	AT28	M_B_A5	
SB_MA_6	AU27	M_B_A6	
SB_MA_7	AV28	M_B_A7	
SB_MA_8	AY27	M_B_A8	
SB_MA_9	AW27	M_B_A9	
SB_MA_10	AV24	M_B_A10	
SB_MA_11	BA27	M_B_A11	
SB_MA_12	AY27	M_B_A12	
SB_MA_13	AR23	M_B_A13	
SB_RAS#	AU23	TP_MB_RCVENIN#	M_B_RAS# (16,17)
SB_RCVENIN#	AK16	TP_MB_RCVENOUT#	T52
SB_RCVENOUT#	AK18		T45
SB_WE#	AR27		M_B_WE# (16,17)

Calistoga

PROJECT : LE4

Quanta Computer Inc.

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	Calistoga_C (DDR)	1A
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U35G

+1.05V — C364 330U_2.5V_ESR12

VCC_0 VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_33 VCC_34 VCC_35 VCC_36 VCC_37 VCC_38 VCC_39 VCC_40 VCC_41 VCC_42 VCC_43 VCC_44 VCC_45 VCC_46 VCC_47 VCC_48 VCC_49 VCC_50 VCC_51 VCC_52 VCC_53 VCC_54 VCC_55 VCC_56 VCC_57 VCC_58 VCC_59 VCC_60 VCC_61 VCC_62 VCC_63 VCC_64 VCC_65 VCC_66 VCC_67 VCC_68 VCC_69 VCC_70 VCC_71 VCC_72 VCC_73 VCC_74 VCC_75 VCC_76 VCC_77 VCC_78 VCC_79 VCC_80 VCC_81 VCC_82 VCC_83 VCC_84 VCC_85 VCC_86 VCC_87 VCC_88 VCC_89 VCC_90 VCC_91 VCC_92 VCC_93 VCC_94 VCC_95 VCC_96 VCC_97 VCC_98 VCC_99 VCC_100 VCC_101 VCC_102 VCC_103 VCC_104 VCC_105 VCC_106 VCC_107 VCC_108 VCC_109 VCC_110

VCC

Calistoga

VCC_SM_0 VCC_SM_1 VCC_SM_2 VCC_SM_3 VCC_SM_4 VCC_SM_5 VCC_SM_6 VCC_SM_7 VCC_SM_8 VCC_SM_9 VCC_SM_10 VCC_SM_11 VCC_SM_12 VCC_SM_13 VCC_SM_14 VCC_SM_15 VCC_SM_16 VCC_SM_17 VCC_SM_18 VCC_SM_19 VCC_SM_20 VCC_SM_21 VCC_SM_22 VCC_SM_23 VCC_SM_24 VCC_SM_25 VCC_SM_26 VCC_SM_27 VCC_SM_28 VCC_SM_29 VCC_SM_30 VCC_SM_31 VCC_SM_32 VCC_SM_33 VCC_SM_34 VCC_SM_35 VCC_SM_36 VCC_SM_37 VCC_SM_38 VCC_SM_39 VCC_SM_40 VCC_SM_41 VCC_SM_42 VCC_SM_43 VCC_SM_44 VCC_SM_45 VCC_SM_46 VCC_SM_47 VCC_SM_48 VCC_SM_49 VCC_SM_50 VCC_SM_51 VCC_SM_52 VCC_SM_53 VCC_SM_54 VCC_SM_55 VCC_SM_56 VCC_SM_57 VCC_SM_58 VCC_SM_59 VCC_SM_60 VCC_SM_61 VCC_SM_62 VCC_SM_63 VCC_SM_64 VCC_SM_65 VCC_SM_66 VCC_SM_67 VCC_SM_68 VCC_SM_69 VCC_SM_70 VCC_SM_71 VCC_SM_72 VCC_SM_73 VCC_SM_74 VCC_SM_75 VCC_SM_76 VCC_SM_77 VCC_SM_78 VCC_SM_79 VCC_SM_80 VCC_SM_81 VCC_SM_82 VCC_SM_83 VCC_SM_84 VCC_SM_85 VCC_SM_86 VCC_SM_87 VCC_SM_88 VCC_SM_89 VCC_SM_90 VCC_SM_91 VCC_SM_92 VCC_SM_93 VCC_SM_94 VCC_SM_95 VCC_SM_96 VCC_SM_97 VCC_SM_98 VCC_SM_99 VCC_SM_100 VCC_SM_101 VCC_SM_102 VCC_SM_103 VCC_SM_104 VCC_SM_105 VCC_SM_106 VCC_SM_107

AU41 AT41 AM41 AU40 BA34 AY34 AW34 AV34 AU34 AT34 AR34 BA30 AY30 AW30 AV30 AU30 AT30 AR30 AP30 AN30 AM30 AM29 AL29 AK29 AJ29 AH29 AJ28 AH28 AJ27 AH27 BA26 AY26 AW26 AV26 AU26 AT26 AR26 AJ26 AH26 AJ25 AH25 AJ24 AH24 BA23 AJ23 BA22 AY22 AW22 AV22 AU22 AT22 AR22 AP22 AK22 AJ22 AK21 AK20 BA19 AY19 AW19 AV19 AU19 AT19 AR19 AP19 AK19 AJ19 AJ18 AJ17 AH17 AJ16 AH16 BA15 AY15 AW15 AV15 AU15 AT15 AR15 AJ15 AJ14 AJ13 AH13 AK12 AJ12 AH12 AG12 AK11 BA8 AY8 AW8 AV8 AT8 AR8 AP8 BA6 AY6 AW6 AV6 AT6 AR6 AP6 AN6 AL6 AJ6 AV1 AJ1

25mils

C214 VCC_SM1 0.47U_6
C222 VCC_SM2 0.47U_6

C344 330U_2.5V_ESR12

+1.05V — C242 10U_8 — C273 10U_8 — C237 1U_4 — C272 0.1U_4 — C288 0.1U_4 — C294 0.1U_4

10U to 1U-Allen

1.8VSUS

120mils

PC6 330U_2.5V_ESR12 2.5 — C274 10U_8 — C254 0.47U_6 — C282 0.1U_4 — C252 0.1U_4 — C302 0.1U_4

C253 0.47U_6
C255 0.47U_6 place C50 on BA23 Ball
place C49 on AJ23 Ball

LE4 B: del 1.5V_AUX power plane

(4,5,6,7,10,12,15,38,40) +1.05V → +1.05V
(7,16,36,40,41) 1.8VSUS → 1.8VSUS

Have to review again
ADD Matrix in silkscreen

place C51 on BA15 Ball

C269 0.47U_6

MCH_CFG_6 shall be PH !!
depopulate R2504 if use Calistoga

C325 VCC_SM106 0.47U_6
C310 VCC_SM107 0.47U_6

25mils

U35F

AD27 AC27 AB27 AA27 Y27 W27 V27 U27 T27 R27 AD26 AC26 AB26 AA26 Y26 W26 V26 U26 T26 R26 AD25 AC25 AB25 AA25 Y25 W25 V25 U25 T25 R25 AD24 AC24 AB24 AA24 Y24 W24 V24 U24 T24 R24 AD23 V23 U23 T23 R23 AD22 V22 U22 T22 R22 AD21 V21 U21 T21 R21 AD20 V20 U20 T20 R20 AD19 V19 U19 T19 AD18 AC18 AB18 AA18 Y18 W18 V18 U18 T18

VCC_NCTF0 VCC_NCTF1 VCC_NCTF2 VCC_NCTF3 VCC_NCTF4 VCC_NCTF5 VCC_NCTF6 VCC_NCTF7 VCC_NCTF8 VCC_NCTF9 VCC_NCTF10 VCC_NCTF11 VCC_NCTF12 VCC_NCTF13 VCC_NCTF14 VCC_NCTF15 VCC_NCTF16 VCC_NCTF17 VCC_NCTF18 VCC_NCTF19 VCC_NCTF20 VCC_NCTF21 VCC_NCTF22 VCC_NCTF23 VCC_NCTF24 VCC_NCTF25 VCC_NCTF26 VCC_NCTF27 VCC_NCTF28 VCC_NCTF29 VCC_NCTF30 VCC_NCTF31 VCC_NCTF32 VCC_NCTF33 VCC_NCTF34 VCC_NCTF35 VCC_NCTF36 VCC_NCTF37 VCC_NCTF38 VCC_NCTF39 VCC_NCTF40 VCC_NCTF41 VCC_NCTF42 VCC_NCTF43 VCC_NCTF44 VCC_NCTF45 VCC_NCTF46 VCC_NCTF47 VCC_NCTF48 VCC_NCTF49 VCC_NCTF50 VCC_NCTF51 VCC_NCTF52 VCC_NCTF53 VCC_NCTF54 VCC_NCTF55 VCC_NCTF56 VCC_NCTF57 VCC_NCTF58 VCC_NCTF59 VCC_NCTF60 VCC_NCTF61 VCC_NCTF62 VCC_NCTF63 VCC_NCTF64 VCC_NCTF65 VCC_NCTF66 VCC_NCTF67 VCC_NCTF68 VCC_NCTF69 VCC_NCTF70 VCC_NCTF71 VCC_NCTF72

NCTF

VSS_NCTF0 VSS_NCTF1 VSS_NCTF2 VSS_NCTF3 VSS_NCTF4 VSS_NCTF5 VSS_NCTF6 VSS_NCTF7 VSS_NCTF8 VSS_NCTF9 VSS_NCTF10 VSS_NCTF11 VSS_NCTF12

AE27 AE26 AE25 AE24 AE23 AE22 AE21 AE20 AE19 AE18 AC17 Y17 U17

+1.5V

LE4 B: change +1.5V_AUX to +1.5V
100mils

VCCAUX_NCTF0 VCCAUX_NCTF1 VCCAUX_NCTF2 VCCAUX_NCTF3 VCCAUX_NCTF4 VCCAUX_NCTF5 VCCAUX_NCTF6 VCCAUX_NCTF7 VCCAUX_NCTF8 VCCAUX_NCTF9 VCCAUX_NCTF10 VCCAUX_NCTF11 VCCAUX_NCTF12 VCCAUX_NCTF13 VCCAUX_NCTF14 VCCAUX_NCTF15 VCCAUX_NCTF16 VCCAUX_NCTF17 VCCAUX_NCTF18 VCCAUX_NCTF19 VCCAUX_NCTF20 VCCAUX_NCTF21 VCCAUX_NCTF22 VCCAUX_NCTF23 VCCAUX_NCTF24 VCCAUX_NCTF25 VCCAUX_NCTF26 VCCAUX_NCTF27 VCCAUX_NCTF28 VCCAUX_NCTF29 VCCAUX_NCTF30 VCCAUX_NCTF31 VCCAUX_NCTF32 VCCAUX_NCTF33 VCCAUX_NCTF34 VCCAUX_NCTF35 VCCAUX_NCTF36 VCCAUX_NCTF37 VCCAUX_NCTF38 VCCAUX_NCTF39 VCCAUX_NCTF40 VCCAUX_NCTF41 VCCAUX_NCTF42 VCCAUX_NCTF43 VCCAUX_NCTF44 VCCAUX_NCTF45 VCCAUX_NCTF46 VCCAUX_NCTF47 VCCAUX_NCTF48 VCCAUX_NCTF49 VCCAUX_NCTF50 VCCAUX_NCTF51 VCCAUX_NCTF52 VCCAUX_NCTF53 VCCAUX_NCTF54 VCCAUX_NCTF55 VCCAUX_NCTF56 VCCAUX_NCTF57

AG27 AF27 AG26 AF26 AG25 AF25 AG24 AF24 AG23 AF23 AG22 AF22 AG21 AF21 AG20 AF20 AG19 AF19 R19 AG18 AF18 R18 AG17 AF17 AE17 AD17 AB17 AA17 W17 V17 T17 R17 AG16 AF16 AE16 AD16 AC16 AB16 AA16 Y16 W16 V16 U16 T16 R16 AG15 AF15 AE15 AD15 AC15 AB15 AA15 Y15 W15 V15 U15 T15 R15

Calistoga

GMCH Strap pin

Depopulate R2504 for Calistoga-Allen

(7) MCH_CFG_5	R137	*2.2K_4	
(7) MCH_CFG_6	R136	*2.2K_4	
(7) MCH_CFG_7	R130	*2.2K_4	
(7) MCH_CFG_9	R129	*2.2K_4	
(7) MCH_CFG_10	R143	*2.2K_4	
(7) MCH_CFG_11	R141	2.2K_4	
(7) MCH_CFG_12	R144	*2.2K_4	
(7) MCH_CFG_13	R140	*2.2K_4	
(7) MCH_CFG_16	R142	*2.2K_4	+3VRUN
(7) MCH_CFG_18	R117	*1K/F_4	
(7) MCH_CFG_19	R110	*1K/F_4	+3VRUN
(7) MCH_CFG_20	R109	*1K/F_4	+3VRUN

intel WW51 recommand

1.MCH_CFG_5 Low = DMI X2, High=DMIX4

2.MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)

3.MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU

4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility

5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility

6.MCH_CFG_11: Low=Calistoga, High=Reserved

7.MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled,
High=Dynamic ODT Enabled.

8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V

9.MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.

10.MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	Calistoga_D (POWER)	1A
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+1.5V L53 10uH_8 +V1.5_DPLLA
C556 0.1U_4
+ C296 330U
L49 10uH_8 +V1.5_DPLLB
C537 0.1U_4
+ C184 330U
L27 FCM2012C-121_8 +V1.5_HPLL
C318 0.1U_4
C342 10U_8
L26 FCM2012C-121_8 +V1.5_MPLL
C309 0.1U_4
C341 10U_8

+V3.3_TVDAC L52 I@BLM18PG181SN1D_8 +V3.3_ATVBG
80mils
C267 10U_8 C555 0.1U_4 C293 0.022U_4
Oreginal FCM2012C-181 "CX000181008"
+V3.3_ATVBG C553 0.1U_4 C279 0.022U_4
+V3.3_ATVBG C554 0.1U_4 C287 0.022U_4
+1.5V L23 E@BLM18PG181SN1D-6_8 +V3.3_ATVBG

LE4 A:
Note:
940GML/945GM contact +V3.3_ATVBG
945PM contact +1.5V

+V1.5_PCIE L48 PCIE_L
60mils +1.5V
C513 10U_8 C515 10U_8 + C516 220U_6.3V BLM21PG220SN1D
RC0805

LE4 C:
Solve black screen issue
to change L48 material
Del R389

+1.5V_3GPLL R93 0.5/F_6 3GPLL_FB_R L18 1uH_6 3GPLL_FB_L R103 0_8 +1.5V
60mils 60mils
RC0805 0.002ohm/1%

LE4 B: del R111,C246
change +1.5V_AUX to 1.5V

+2_5VRUN R396 I@0_8 R2_5VRUNA
R401 E@0_8

LE4 A:
Note:
940GML/945GM contact Power plan
945PM contact GAN plan

+V2.5_CRTDAC +1.05V R118 I@0_8 V2.5VCRTDAC
R127 E@0_8

LE4 A:
Note:
940GML/945GM contact +2.5_CRTDAC
945PM contact +1.05V

+V3.3_ATVBG +1.5V R131 I@0_8 V3.3_ATVBG
R438 E@0_8

LE4 A:
Note:
940GML/945GM contact +V3.3_ATVBG
945PM contact +1.5V

+3VRUN +1.5V
C248 10U_8 C244 0.1U_4 C322 0.1U_4 C343 10U_8

+3.3S_TVDAC_LDO
30mils
+1.5V
BAT54 D6 I@PDZ5.6B
V1_5SFOLLOW 1 2
+V3.3_TVDAC R440 I@10_4
0.002 1% R154 I@0_8
RC0805

LE4 B:
Note:
940GML/945GM has circuit
945PM NA

+1.5V R397 I@0_8 VCCD_LVDS
R398 E@0_8

LE4 A:
Note:
940GML/945GM contact Power plan
945PM contact GAN plan

+V1.5_TVDAC L20 V15_TVDAC_R R400 0_8 +1.5V
C257 0.022U_4 C250 0.1U_4
FCM2012C-121_8
RC0805
Oreginal FCM2012C-181 "CX000181008"
+V1.5_QTVDAC L22
C259 0.022U_4 C251 0.1U_4
FCM2012C-121_8
Oreginal FCM2012C-181 "CX000181008"

+2_5VRUN R392 I@0_8 R2_5VRUN
C205 0.1U_4 C240 10U_8

LE4 A:
Note:
940GML/945GM contact Power plan
945PM contact GAN plan

+2_5VRUN C234 0.1U_4 C207 4.7U_6
R393 E@0_8 R2_5VRUN
R2_5VRUN +V1.5_PCIE
+2_5VRUN C233 0.1U_4
+V1.5_3GPLL C231 0.1U_4 C235 10U_8
R2.5VCRTDAC C256 0.1U_4 C258 0.022U_4
+V1.5_DPLLB +V1.5_DPLLA +V1.5_HPLL
R2_5VRUNA C211 0.01U_4 C213 0.1U_4
+V1.5_MPLL
RV3.3_ATVBG C270 0.1U_4 C271 0.022U_4
+V3.3_ATVBG +V3.3_ATVBG
+1.5V VCCD_LVDS +V1.5_TVDAC
+3VRUN 40mils +V1.5_QTVDAC
+1.5V

LE4 B:

U35H

	VCCSYNC	H22	
	VCC_TXLVDS0	C30	
	VCC_TXLVDS1	B30	
	VCC_TXLVDS2	A30	
	VCC3G0	AJ41	
	VCC3G1	AB41	
	VCC3G2	Y41	
	VCC3G3	V41	
	VCC3G4	R41	
	VCC3G5	N41	
	VCC3G6	L41	
	VCCA_3GPLL	AC33	
	VCCA_3GBG	G41	
	VSSA_3GBG	H41	
	VCCA_CRTDAC0	F21	
	VCCA_CRTDAC1	E21	
	VSSA_CRTDAC	G21	
	VCCA_DPLLA	B26	
	VCCA_DPLLB	C39	
	VCCA_HPLL	AF1	
	VCCA_LVDS	A38	
	VSSA_LVDS	B39	
	VCCA_MPLL	AF2	
	VCCA_TVBG	H20	
	VSSA_TVBG	G20	
	VCCA_TVDACA0	E19	
	VCCA_TVDACA1	F19	
	VCCA_TVDACB0	C20	
	VCCA_TVDACB1	D20	
	VCCA_TVDACC0	E20	
	VCCA_TVDACC1	F20	
	VCCD_HMPLL0	AH1	
	VCCD_HMPLL1	AH2	
	VCCD_LVDS0	A28	
	VCCD_LVDS1	B28	
	VCCD_LVDS2	C28	
	VCCD_TVDAC	D21	
	VCC_HV0	A23	
	VCC_HV1	B23	
	VCC_HV2	B25	
	VCCD_QTVDAC	H19	
	VCCAUX0	AK31	
	VCCAUX1	AE31	
	VCCAUX2	AE31	
	VCCAUX3	AC31	
	VCCAUX4	AL30	
	VCCAUX5	AK30	
	VCCAUX6	AJ30	
	VCCAUX7	AH30	
	VCCAUX8	AG30	
	VCCAUX9	AF30	
	VCCAUX10	AE30	
	VCCAUX11	AD30	
	VCCAUX12	AC30	
	VCCAUX13	AG29	
	VCCAUX14	AF29	
	VCCAUX15	AE29	
	VCCAUX16	AD29	
	VCCAUX17	AC29	
	VCCAUX18	AG28	
	VCCAUX19	AF28	
	VCCAUX20	AE28	
	VCCAUX21	AH22	
	VCCAUX22	AJ21	
	VCCAUX23	AH21	
	VCCAUX24	AJ20	
	VCCAUX25	AH20	
	VCCAUX26	AH19	
	VCCAUX27	P19	
	VCCAUX28	P16	
	VCCAUX29	AH15	
	VCCAUX30	P15	
	VCCAUX31	AH14	
	VCCAUX32	AG14	
	VCCAUX33	AF14	
	VCCAUX34	AE14	
	VCCAUX35	Y14	
	VCCAUX36	AF13	
	VCCAUX37	AE13	
	VCCAUX38	AE12	
	VCCAUX39	AF12	
	VCCAUX40	AD12	

POWER

Calistoga

+1.05V

VTT_0	AC14	
VTT_1	AB14	
VTT_2	W14	
VTT_3	V14	
VTT_4	T14	
VTT_5	R14	
VTT_6	P14	
VTT_7	N14	
VTT_8	M14	
VTT_9	L14	
VTT_10	AD13	
VTT_11	AC13	
VTT_12	AB13	
VTT_13	AA13	
VTT_14	Y13	
VTT_15	W13	
VTT_16	V13	
VTT_17	U13	
VTT_18	T13	
VTT_19	R13	
VTT_20	N13	
VTT_21	M13	
VTT_22	L13	
VTT_23	AB12	
VTT_24	AA12	
VTT_25	Y12	
VTT_26	W12	
VTT_27	V12	
VTT_28	U12	
VTT_29	T12	
VTT_30	R12	
VTT_31	P12	
VTT_32	N12	
VTT_33	M12	
VTT_34	L12	
VTT_35	R11	
VTT_36	P11	
VTT_37	N11	
VTT_38	M11	
VTT_39	R10	
VTT_40	P10	
VTT_41	N10	
VTT_42	M10	
VTT_43	P9	
VTT_44	N9	
VTT_45	M9	
VTT_46	R8	
VTT_47	P8	
VTT_48	N8	
VTT_49	M8	
VTT_50	P7	
VTT_51	N7	
VTT_52	M7	
VTT_53	R6	
VTT_54	P6	
VTT_55	M6	
VTT_56	A6	
VTT_57	R5	
VTT_58	P5	
VTT_59	N5	
VTT_60	M5	
VTT_61	P4	
VTT_62	N4	
VTT_63	M4	
VTT_64	R3	
VTT_65	P3	
VTT_66	N3	
VTT_67	M3	
VTT_68	R2	
VTT_69	P2	
VTT_70	M2	
VTT_71	D2	
VTT_72	AB1	
VTT_73	R1	
VTT_74	P1	
VTT_75	N1	
VTT_76	M1	

2005/07/14
VTTLF_CAP3
C303 0.47U_6

VTT_56 , VTT_71 and 72 are attached with 0.1u seperated .Checking

2005/07/14
VTTLF_CAP2
VTTLF_CAP1
C561 0.47U_6 C312 0.22U_4

+1.05V +1.5V +V1.5_PCIE +2_5VRUN +3VRUN

+1.05V	(4,5,6,7,9,12,15,38,40)
+1.5V	(5,7,9,13,15,27,38,40)
+V1.5_PCIE	(7)
+2_5VRUN	(19,22,40)
+3VRUN	(3,5,7,9,12,13,14,15,16,17,18,19,20,22,23,26,27,28,30,31,32,33,36,40,41)

+1.05V
330U/2.5V/ESR-9/POS
+ C290 C245 4.7U/6.3v_8 C283 2.2U/6.3V_6 C249 0.1U_4 C261 10U_8
+1.05V
C241 0.22U_4 C239 0.22U_4 C264 0.47U_6 C284 0.47U_6

+2_5VRUN R91 10_4 VCCGFOLLOW
25mils
BAT54 D1 PDZ5.6B
+1.05V
L19 FCM2012C-121_8 +V2.5_CRTDAC
Within 3" of GMCH

+3.3S_TVDAC_LDO
For TV-OUT
+5VRUN
U16
OUT IN GND BYP EN
I@AAT3218
C300 I@10U_8 C299 I@0.01U_4 C306 I@1U_6

LE4 B:
Note:
940GML/945GM has circuit
945PM NA

PROJECT : LE4		
Quanta Computer Inc.		
Size	Document Number: Calistoga_E (POWER2)	Rev: 1A
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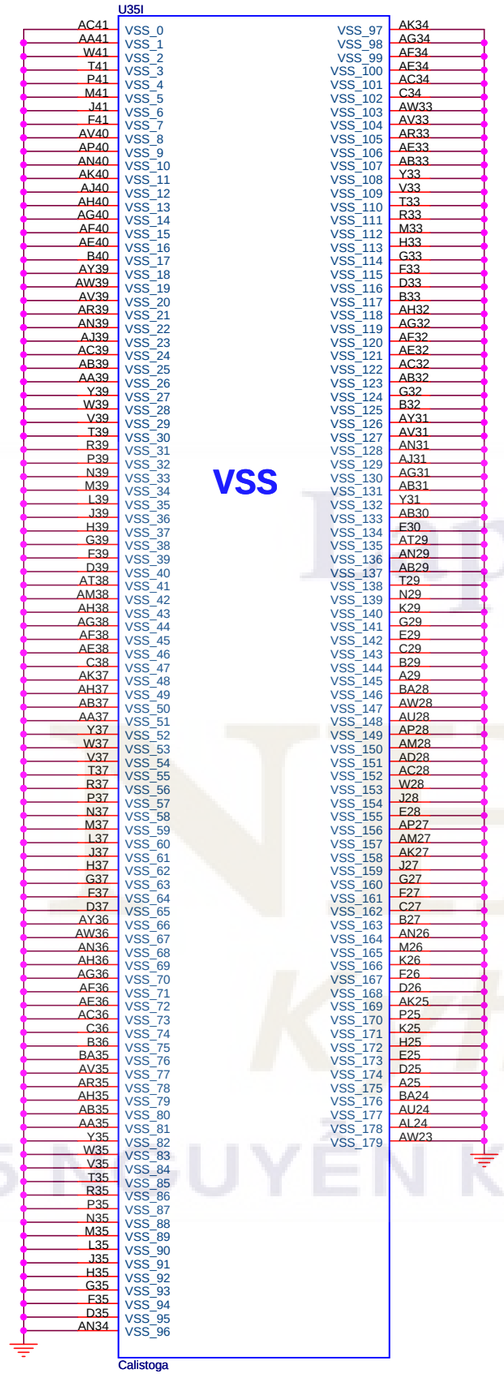

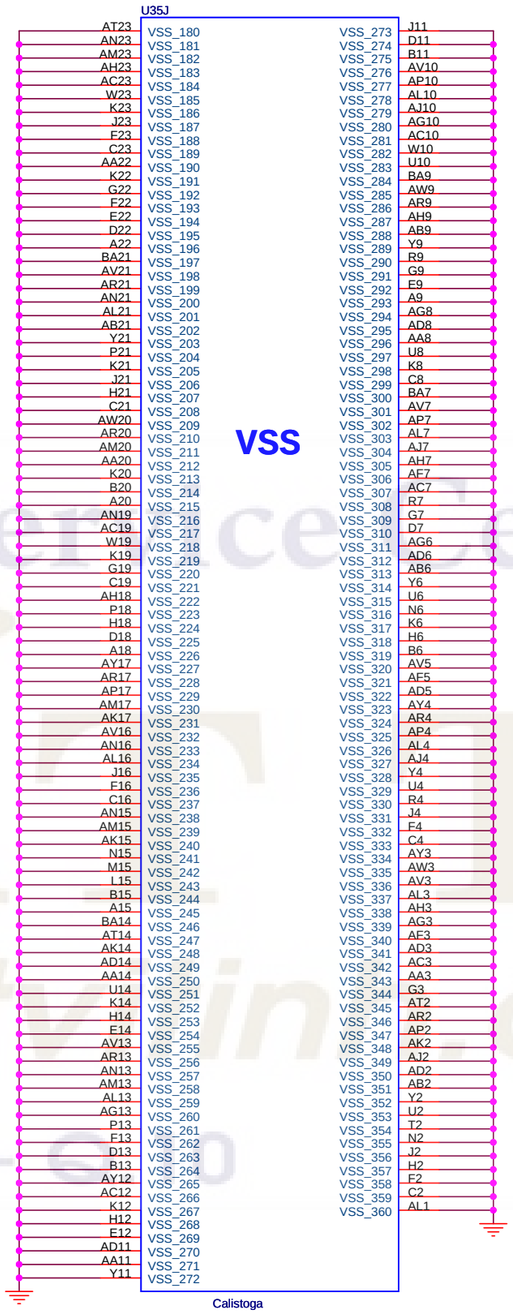

PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	Calistoga_F (VSS NCTF)	1A
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RTC

VCCRTC
C667 1U_4
3VPCU
D15 CH500H-40
D14 CH500H-40
VCCRTC_2
R312 1K/F_4
R546 1M_4
C684 1U/6.3V_4
G1 SHORT_ PAD1
R545 20K/F_4
Place near to Mini-door
LE4 A:
C459 15P_4
CLK_32KX1
Y5 32.768KHZ
BG332768909
C457 18P_4
CLK_32KX2
R315 10M_6
CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF
LE4 B: Change C459 value from 18p to 15p
BT1 BAT_CONN
RTCRST#
SM_INTRUDER#
ICH_INTVRMEN
Internal PU

5VPCU
20MIL
20MIL
R316 1.2K/F_4
VCCRTC_1
R317 1K/F_4
VCCRTC_3
Q23 MMBT3904
R310 4.7K_4
R311 15K/F_4
add RTC Bat rechargeable circuit

+3VRUN
R494 10K_4
Internal PU
(31) SATA_LED#
SATA_LED#
Review current rating

(32) SATA_RXN0_C
(32) SATA_RXP0_C
(32) SATA_TXN0
(32) SATA_TXP0
C449 3900P_P_4
C448 3900P_P_4
CKL:1n ~ 20nF
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
SATA_RXN2_C
SATA_RXP2_C
SATA_TXN2_C
SATA_TXP2_C
T254
T124
T245
T243
T249
T248

(3) CLK_PCIE_SATA#
(3) CLK_PCIE_SATA
CLK_PCIE_SATA#
CLK_PCIE_SATA
25mils/15mils
R289 24.9/F_4
SATA_BIAS
Place within 500 mils of ICH7

(32) PDIOR#
(32) PDIOW#
(32) PDDACK#
(32) IRQ14
(32) PIORDY
(32) PDDREQ
PDIOR#
PDIOW#
PDDACK#
IRQ14
PIORDY
PDDREQ

+3VRUN
R334 4.7K_4
R496 4.7K_4
Difference
IRQ14
PIORDY
LE4 B:
Change R496 and R334 from 8.2K to 4.7K

VCCRTC
ICH7 internal VR enable strap

	INTVRMEN
Enable (default)	1
Disable	0

R555 332K/F_6
ICH_INTVRMEN
R556 *0/F_4

U23A

RTXC1
RTXC2
RTCRST#
INTRUDER#
INTVRMEN
EE_CS
EE_SHCLK
EE_DOUT
EE_DIN
LAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
ACZ_BIT_CLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDOUT
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIASN
SATARBIASP
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
ICH7-M

RTC
LPC
LAN
CPU
AC-97/AZALIA
SATA
IDE

LAD0 (26,27,30)
LAD1 (26,27,30)
LAD2 (26,27,30)
LAD3 (26,27,30)
LDRQ#0 (26,27,30)
T251
LFRAME# (26,27,30)
GATEA20 (30)
H_A20M# (4)
R5506 close to MCH
H_CPUSLP# (4,6)
R222 *0_4
H_DPRSTP# R
H_DPSLP# R
R477 0_4
R473 0_4
ICH_DPRSTP# (4,37)
H_DPSLP# (4)
H_FERR# (4)
Should be 2" close ICH7
R481 0/F_4
Difference
H_PWRGD (4)
T97
H_IGNNE# (4)
H_INIT# (4)
H_INTR (4)
RCIN# (30)
H_NMI (4)
H_SMI# (4)
H_STPCLK# (4)
H_THERMTRIP_R
R471 24.9_4
PM_THRMTRIP# (4,7)
Should be 2" close ICH7
PDD[15:0] (32)
PDA[2:0] (32)
PDCS1# (32)
PDCS3# (32)

+3VRUN
R236 10K_4
R244 10K_4
RCIN#
GATEA20
+1.05V
R226 *56_4
R234 *56_4
+1.05V
R230 56_4
+1.05V
R472 56_4

0 ohm ?
ACZ_SDOUT
R552 39_4
ACZ_SDOUT_AUDIO (28)
C689 *10P_4
Near To ICH7-M
ACZ_SYNC
R553 39_4
ACZ_SYNC_AUDIO (28)
C690 *10P_4
ACZ_BCLK
R551 39_4
BIT_CLK_AUDIO (28)
C688 *10P_4
ACZ_RST#
R547 39_4
ACZ_RST#_AUDIO (28)
ACZ_SDIN0 (28)

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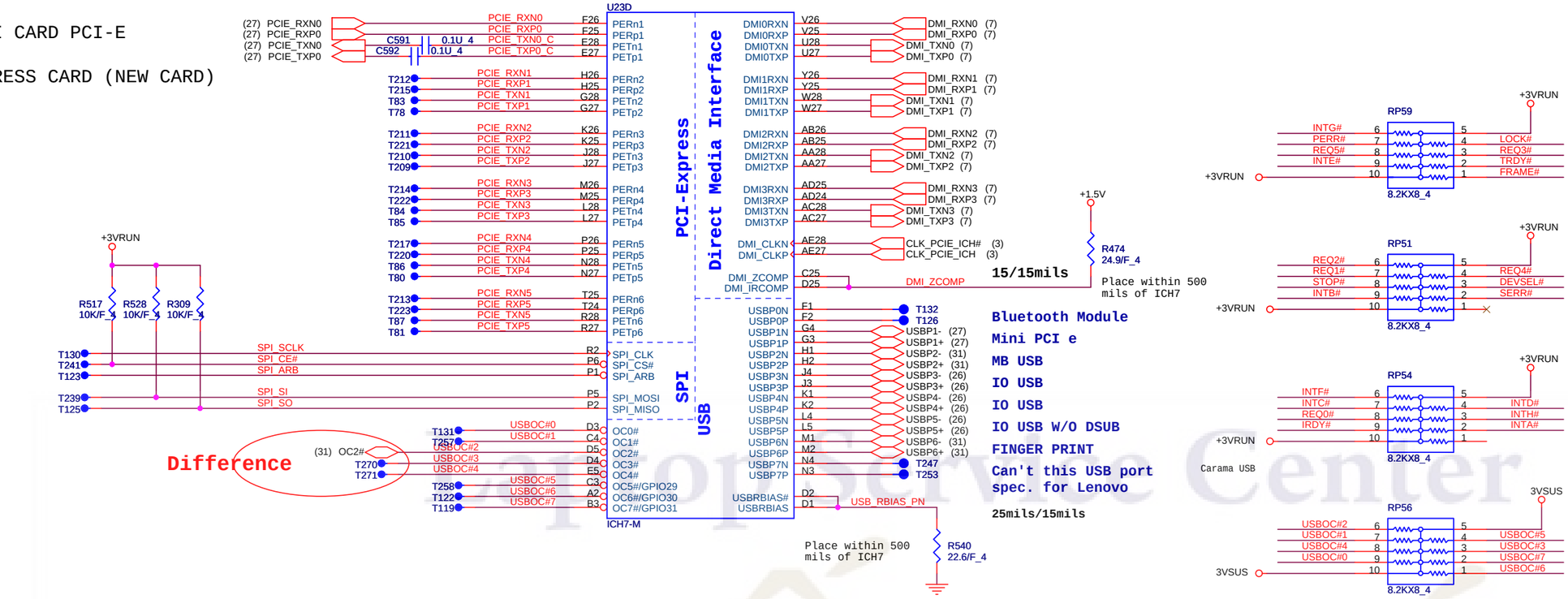
MINI CARD PCI-E

EXPRESS CARD (NEW CARD)



PROJECT : LE4

Quanta Computer Inc.

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	ICH7-M PCI E (2 of 4)	1A

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R376
No stuff-->boot
Stuff-->No boot

LE4 B:
Change Value from 1K to 680

PCLK_SMB R482 2.2K_4
PDAT_SMB R485 2.2K_4
PCIE_WAKE# R498 680_4

RI# R207 10K_4
SMB_LINK_ALERT# R215 10K_4
SMLINK0 R218 10K_4
SMLINK1 R221 10K_4
EXTSMI#_R R495 *10K_4
WAKE_SCI#_R R459 10K_4
SMBALERT# R225 10K_4

DNBSWON# R478 10K_4
SYS_RST# R229 10K_6
PM_BATLOW# R247 8.2K/F_4
SWI# R270 10K_4

CLKRUN# R259 8.2K/F_4
SERIRQ R248 8.2K/F_4
LCDID0 R554 10K_4
LCDID1 R253 10K_4
RUNTIME_SCI#_R R488 10K/F_4
SYS_RST# R238 *10K/F_4
RSMRST# R294 10K/F_4

to Clock Gen & DIMM
SYS_RST is suspend rail

U23C
ICH7-M

SMB: SMBCLK, SMBDATA, LINKALERT#, SMLINK0, SMLINK1
SYS GPIO: RI#, SPKR, SUS_STAT#, SYS_RST#, GPIO0/BM_BUSY#, GPIO11/SMBALERT#, GPIO18/STPPCI#, GPIO20/STPCPU#, GPIO26, GPIO27, GPIO28, GPIO32/CLKRUN#, GPIO33/AZ_DOCK_EN#, GPIO34/AZ_DOCK_RST#, WAKE#, SERIRQ, THRM#, VRMPWRGD, GPIO6, GPIO7, GPIO8
Power MGT: SATA GP10, Clocks, GPIO21/SATA0GP, GPIO19/SATA1GP, GPIO36/SATA2GP, GPIO37/SATA3GP, CLK14, CLK48, SUSCLK, SLP_S3#, SLP_S4#, SLP_S5#, PWROK, GPIO16/DPRSLPVR, TP0/BATLOW#, PWRBTN#, LAN_RST#, RSMRST#, GPIO9, GPIO10, GPIO12, GPIO13, GPIO14, GPIO15, GPIO24, GPIO25, GPIO35, GPIO38, GPIO39
GPIO: GPIO6, GPIO7, GPIO8

(3,33) PCLK_SMB
(3,33) PDAT_SMB
T88 SMLINK0
T92 SMLINK1
T94 RI#
(24,26) RI#
(28) ACZ_SPKR
R267 *1K_4
(24,26,27) SUS_STAT#
(4) SYS_RST#
(7) PM_BMBUSY#
R499 0/F_4
SMBALERT#
R250 *10K_4
R246 *10K_4
No ASF support
(3) PM_STPPCI#
(3) PM_STPCPU#
R483 0_4
R486 0/F_4
PM_STPPCI_ICH#
PM_STPCPU_ICH#
T96
T99 BIOS_REC_R
T216 FWH_MFG_MODE_R
Note: Connect to EC; Reserve PH/3V
(24,26,27,30,33) CLKRUN#
T229 ICH_GPO33
BOARD_ID2 U2
R252 8.2K/F_4
(27) PCIE_WAKE#
(24,26,27,30) SERIRQ
(5) THERM_ALERT#
VR_PWRGD_CK410
T225
(30) SCI#
(30) KBSMI#
R491 0_4
R492 0/F_4
RUNTIME_SCI#_R
EXTSMI#_R

CLK14 14M_ICH
CLK48 CLKUSB_48
SUSCLK ICH_SUSCLK
SLP_S3# R476 100/F_4 SUSB# (30)
SLP_S4# R480 100/F_4 SUSC# (30)
SLP_S5#
PWROK ICH_PWROK
GPIO16/DPRSLPVR PM_DPRSLPVR_R R475 100/F_4
R227 0_4
R233 *100K/F_4
PM_EXTTS#1 (7,17)
PM_DPRSLPVR (37)
CKL :100Kohm PD
TP0/BATLOW# PM_BATLOW# R243 100/F_4 PM_BATLOW# (30)
PWRBTN# DNBSWON# R500 100K/F_4 DNBSWON# (30)
LAN_RST# R460 0/F_4 PLTRST# PLTRST# (13,18,26,27,32)
RSMRST# PM_RSMRST#_R R295 100/F_4 RSMRST# RSMRST# (30)
GPIO9 SWI# SWI# (30)
GPIO10 GPIO10 T98
GPIO12 MXM_THERM# T226
GPIO13 WAKE_SCI#_R T79
GPIO14 R4 LCDID0 LCDID0 (22)
GPIO15 E22 LCDID1 LCDID1 (22)
GPIO24 R3 GPIO24 T261
GPIO25 D20 GPIO25 T230
GPIO35 AD21 AMP_BEEP (28)
GPIO38 AD20 T218
GPIO39 AE20 R_PLTRST_DELAY# R255 *E@0_4 PLTRST_DELAY#
PLTRST_DELAY# (18)
GPIO25 /Suspend rail is a HW strap , don't pull down .

MXM_ON#: 1 -> No MXM Module
0 -> MXM Module
MXM_THERM# R251 10K_4 +3V_S5

GPIO24 USBEN_LS# (26)
GPIO25 USBEN_RJ# (26)

+3VRUN U21 NL17SZ14DFT2G
R239 *10K_4
(3,37) CLK_EN#
VR_PWRGD_CK410
Note: External pull-up 3V

LE4 A:
Place close to ICH7
CLKUSB_48 R314 *10_4 C458 *10P_4
14M_ICH R550 *33_4 C681 *10P_4

LE4 B:
del R487,R256,R469 and R462in BOM
R487 *10K/F_6
R256 *0/F_4
BIOS_REC
BIOS_REC_R R597 0_4 USBEN_MB# (31)
R489 *0_4

LE4 C:
Add to select power on/off for USB function with R598 and R597
3VPCU
R462 *10K_4
R469 *0/F_4
FWH_MFG_MODE
FWH_MFG_MODE_R R598 0_4
R470 *0_4
(26) USBEN_LE3#

LE4 C:
Add to select power on/off for USB function

3VSUS
PWM require 6.9K
Change to 6.8K
C675 0.047U_4
R543 6.8K_4
+3VRUN
(7,37) DELAY_VR_PWRGOOD
(22,30) PWROK
R542 100K_4
U41 TC7SH08FU
ICH_PWROK
R541 10K_4
Level is incorrect !!

BOARD_ID0 GPIO21	BOARD_ID1 GPIO19	BOARD_ID2 GPIO34	BOARD_ID3 GPIO36	BOARD_ID4 GPIO37	
L	L	L	L	L	LE3--L
L	L	L	L	H	LE4--H

+3VRUN
R265 *10K/F_4 BOARD_ID0 R512 10K_4
R493 *10K/F_4 BOARD_ID1 R490 10K/F_4
R466 *10K_4 BOARD_ID2 R461 10K/F_4
R257 *10K_4 BOARD_ID3 R258 10K_4
R268 *10K_4 BOARD_ID4 R269 10K_4

CHECK
PATA,SATA Select
PATA Mode: 1
SATA Mode: 0

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Quanta Computer Inc.
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LE4 C:
Del C386

Add C718 and C719

Oreginal 270U P/N "CH7270LM885"

Check with Intel for power plan.

30mils

30mils

U23E — ICH7-M

U23F — ICH7-M

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Quanta Computer Inc.			
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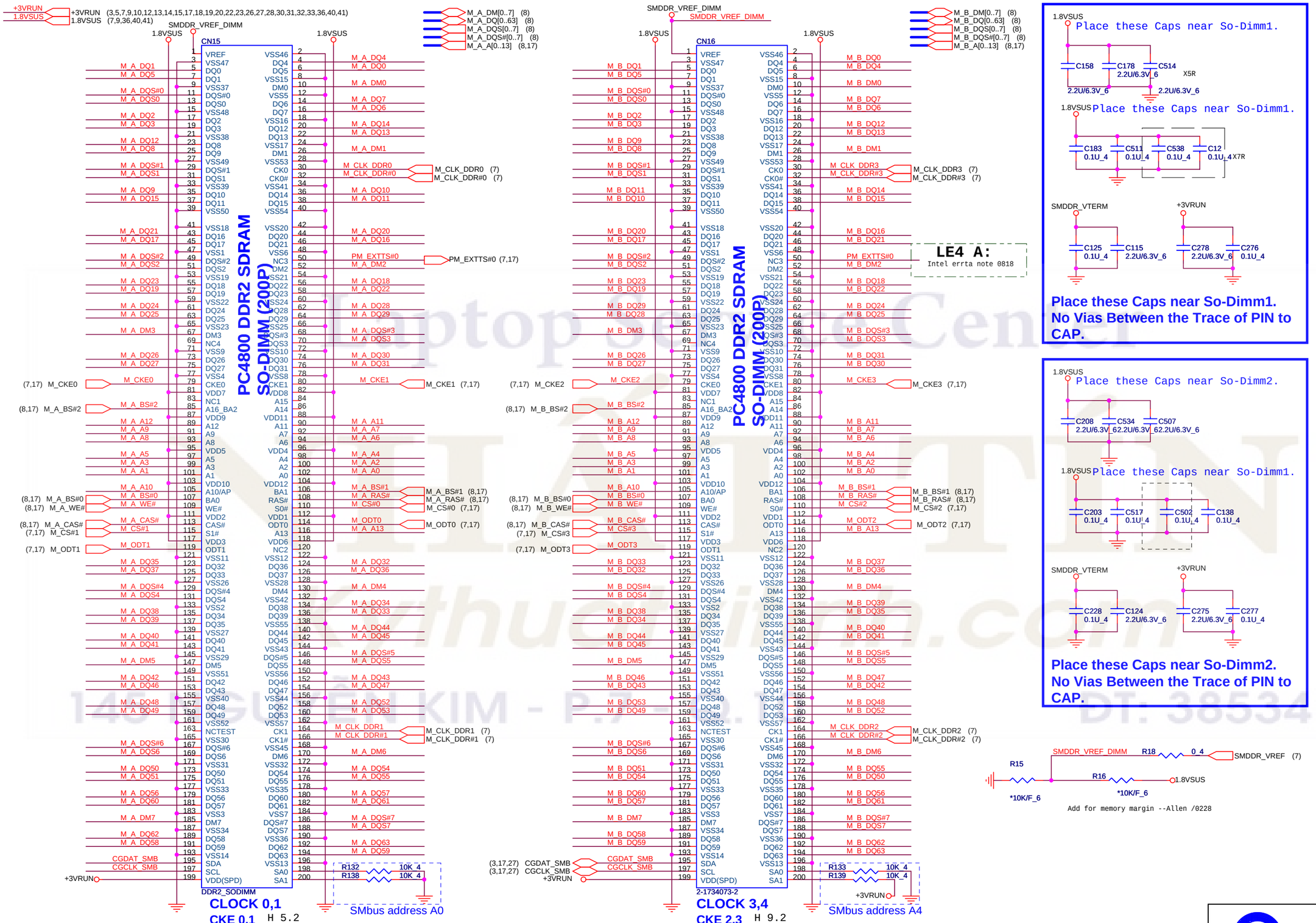

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Quanta Computer Inc.		
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	DDR II SO-DIMM (200P)	1A
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DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

M_A_A[13..0] → M_A_A[13..0] (8,16)
SMDDR_VTERM → SMDDR_VTERM (16,36,40)

SMDDR_VTERM

C127 C218 C128 C135 C220 C180 C209 C204 C182 C139 C157 C219 C212 — 0.1U_4

(7,16) M_ODT0 — RP25: M_ODT0, M_A_A13, M_A_A9, M_A_A8, M_A_A5, M_A_A3 — 56X2 — SMDDR_VTERM

(7,16) M_CKE1 — RP5: M_A_A11, M_CKE1, M_A_A10 — 56X2

(8,16) M_A_WE# — RP17: M_A_WE#, M_A_A6, M_A_A7, M_A_A2, M_A_A4 — 56X2 — SMDDR_VTERM

(8,16) M_A_BS#1 — RP18: M_A_BS#1, M_A_A0, M_A_A12 — 56X2

RP10: M_A_A1, M_A_CAS#, M_A_BS#0 — 56X2

(8,16) M_A_CAS# — RP7: M_A_A14, M_A_A15, M_A_A1 — 56X2

(8,16) M_A_BS#0 — RP21: M_A_CAS#, M_A_BS#0, M_A_RAS# — 56X2 — SMDDR_VTERM

DDRII B CHANNEL

M_B_A[13..0] → M_B_A[13..0] (8,16)
1.8VSUS → 1.8VSUS (7,9,16,36,40,41)
+3VRUN → +3VRUN (3,5,7,9,10,12,13,14,15,16,18,19,20,22,23,26,27,28,30,31,32,33,36,40,41)

SMDDR_VTERM

C181 C156 C137 C217 C206 C179 C134 C133 C129 C225 C223 C224 C221 — 0.1U_4

Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

(8,16) M_B_BS#1 — RP20: M_B_BS#1, M_B_A0, M_B_A3 — 56X2

RP16: M_B_A1, M_B_A12, M_B_A5 — 56X2

RP11: M_B_A2, M_B_A4, M_B_A8 — 56X2 — SMDDR_VTERM

RP14: M_B_A9, M_B_A6, M_B_A7 — 56X2

(7,16) M_CKE2 — RP8: M_CKE2, M_B_BS#2, M_CS#2 — 56X2

(8,16) M_B_BS#2 — RP12: M_B_RAS#, M_B_WE#, M_B_CAS# — 56X2 — SMDDR_VTERM

(7,16) M_CS#2 — RP3: M_B_A10, M_B_BS#0, M_CS#0 — 56X2

(8,16) M_B_RAS# — RP23: M_B_RAS#, M_B_WE#, M_B_CAS# — 56X2

(8,16) M_B_WE# — RP24: M_B_A10, M_B_BS#0, M_CS#3 — 56X2

(8,16) M_B_CAS# — RP19: M_CS#3, M_ODT3, M_ODT1 — 56X2

(8,16) M_B_BS#0 — RP22: M_CS#1, M_B_A11, M_CKE3 — 56X2 — SMDDR_VTERM

(7,16) M_CS#0 — RP28: M_CKE0, M_A_BS#2, M_CKE1 — 56X2

(8,16) M_A_RAS# — RP27: M_A_RAS#, M_ODT2, M_B_A13 — 56X2

(7,16) M_ODT2 — RP26: M_CS#2, M_ODT0, M_CKE2 — 56X2

(7,16) M_CS#3 — RP6: M_A_A14, M_A_A15, M_B_A14 — 56X2

(7,16) M_ODT3 — RP4: M_CKE3, M_A_BS#1, M_CKE0 — 56X2

(7,16) M_ODT1 — SMDDR_VTERM

(7,16) M_CS#1

(7,16) M_CKE3

(8,16) M_A_BS#2

(7,16) M_CKE0

Uninstall

+3VRUN

R62 *200_4 — C185 *0.1U_4

U9 *LM86CIMM

(3,16,27) CGCLK_SMB — CGCLK_SMB — SCLK

(3,16,27) CGDAT_SMB — CGDAT_SMB — SDA

(7,16) PM_EXTTS#0 — PM_EXTTS#0 — ALERT#

(7,14) PM_EXTTS#1 — PM_EXTTS#1 — R58 *0_4 — OVERT#

VCC ← LM86_3V

DXP ← DDR_THERMDA

DXN

GND → DDR_THERMDC

Q2 *PMST3904

Allen

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	DDR II TERMINATION	1A
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(7) PCIE_MTX_GRX_P[0..15]
(7) PCIE_MTX_GRX_N[0..15]

(7) PCIE_MRX_GTX_P[0..15]

PCIE_MRX_GTX_P0	E@0.1U_4 C148	PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1	E@0.1U_4 C172	PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2	E@0.1U_4 C150	PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3	E@0.1U_4 C174	PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4	E@0.1U_4 C152	PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5	E@0.1U_4 C176	PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6	E@0.1U_4 C154	PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7	E@0.1U_4 C162	PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8	E@0.1U_4 C140	PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9	E@0.1U_4 C164	PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10	E@0.1U_4 C142	PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11	E@0.1U_4 C166	PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12	E@0.1U_4 C144	PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13	E@0.1U_4 C168	PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14	E@0.1U_4 C146	PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15	E@0.1U_4 C170	PCIE_MRX_GTX_C_P15

U33A

PART 1 OF 4

PCIE_MTX_GRX_P0	AF1	PEX_RX0P	PEX_TX0P	AD5
PCIE_MTX_GRX_N0	AG2	PEX_RX0N	PEX_TX0N	AD6
PCIE_MTX_GRX_P1	AG3	PEX_RX1P	PEX_TX1P	AE6
PCIE_MTX_GRX_N1	AG4	PEX_RX1N	PEX_TX1N	AE7
PCIE_MTX_GRX_P2	AF4	PEX_RX2P	PEX_TX2P	AD7
PCIE_MTX_GRX_N2	AF5	PEX_RX2N	PEX_TX2N	AC7
PCIE_MTX_GRX_P3	AG6	PEX_RX3P	PEX_TX3P	AE9
PCIE_MTX_GRX_N3	AG7	PEX_RX3N	PEX_TX3N	AE10
PCIE_MTX_GRX_P4	AF7	PEX_RX4P	PEX_TX4P	AD10
PCIE_MTX_GRX_N4	AF8	PEX_RX4N	PEX_TX4N	AC10
PCIE_MTX_GRX_P5	AG9	PEX_RX5P	PEX_TX5P	AE12
PCIE_MTX_GRX_N5	AG10	PEX_RX5N	PEX_TX5N	AE13
PCIE_MTX_GRX_P6	AF10	PEX_RX6P	PEX_TX6P	AD13
PCIE_MTX_GRX_N6	AF11	PEX_RX6N	PEX_TX6N	AC13
PCIE_MTX_GRX_P7	AG12	PEX_RX7P	PEX_TX7P	AC15
PCIE_MTX_GRX_N7	AG13	PEX_RX7N	PEX_TX7N	AD15
PCIE_MTX_GRX_P8	AG15	PEX_RX8P	PEX_TX8P	AE15
PCIE_MTX_GRX_N8	AG16	PEX_RX8N	PEX_TX8N	AE16
PCIE_MTX_GRX_P9	AF16	PEX_RX9P	PEX_TX9P	AC18
PCIE_MTX_GRX_N9	AF17	PEX_RX9N	PEX_TX9N	AD18
PCIE_MTX_GRX_P10	AG18	PEX_RX10P	PEX_TX10P	AE18
PCIE_MTX_GRX_N10	AG19	PEX_RX10N	PEX_TX10N	AE19
PCIE_MTX_GRX_P11	AF19	PEX_RX11P	PEX_TX11P	AC21
PCIE_MTX_GRX_N11	AF20	PEX_RX11N	PEX_TX11N	AD21
PCIE_MTX_GRX_P12	AG21	PEX_RX12P	PEX_TX12P	AE21
PCIE_MTX_GRX_N12	AG22	PEX_RX12N	PEX_TX12N	AE22
PCIE_MTX_GRX_P13	AF22	PEX_RX13P	PEX_TX13P	AD22
PCIE_MTX_GRX_N13	AF23	PEX_RX13N	PEX_TX13N	AD23
PCIE_MTX_GRX_P14	AG24	PEX_RX14P	PEX_TX14P	AF25
PCIE_MTX_GRX_N14	AG25	PEX_RX14N	PEX_TX14N	AE25
PCIE_MTX_GRX_P15	AG26	PEX_RX15P	PEX_TX15P	AF24
PCIE_MTX_GRX_N15	AF27	PEX_RX15N	PEX_TX15N	AD24

PCI-EXPRESS INTERFACE

		Clock	PEX_TSTCLK_OUT	AF13
(3) CLK_PCIE_VGA	AE3	PEX_REFCLK	PEX_TSTCLK_OUT#	AF14
(3) CLK_PCIE_VGA#	AE4	PEX_REFCLK#		
			PEX_RST#	AC6

PCIE_MRX_GTX_C_P0 … PCIE_MRX_GTX_C_P15 (AD5, AD6, AE6, AE7, AD7, AC7, AE9, AE10, AD10, AC10, AE12, AE13, AD13, AC13, AC15, AD15, AE15, AE16, AC18, AD18, AE18, AE19, AC21, AD21, AE21, AE22, AD22, AD23, AF25, AE25, AF24, AD24)

PCIE_MTX_GRX_C_P0 … PCIE_MTX_GRX_C_P15 (AF1, AG2, AG3, AG4, AF4, AF5, AG6, AG7, AF7, AF8, AG9, AG10, AF10, AF11, AG12, AG13, AG15, AG16, AF16, AF17, AG18, AG19, AF19, AF20, AG21, AG22, AF22, AF23, AG24, AG25, AG26, AF27)

R_PLTRST_DELAY# — R387 *E@200_4 — R59 *E@0 — PLTRST_DELAY# (14) — PLTRST_DELAY#

LE4 B:
del R387,R59 in BOM

(7) PCIE_MRX_GTX_N[0..15]

PCIE_MRX_GTX_N0	E@0.1U_4 C149	PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1	E@0.1U_4 C173	PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2	E@0.1U_4 C151	PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3	E@0.1U_4 C175	PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4	E@0.1U_4 C153	PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_N5	E@0.1U_4 C177	PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_N6	E@0.1U_4 C155	PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7	E@0.1U_4 C163	PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_N8	E@0.1U_4 C141	PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9	E@0.1U_4 C165	PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10	E@0.1U_4 C143	PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11	E@0.1U_4 C167	PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12	E@0.1U_4 C145	PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13	E@0.1U_4 C169	PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14	E@0.1U_4 C147	PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_N15	E@0.1U_4 C171	PCIE_MRX_GTX_C_N15

+3VRUN — U31 E@TC7SH08FU — C482 E@0.1U — PLTRST# — PLTRST# (13,14,26,27,32)

LE4 B:
del U31, C482 in BOM

R_PLTRST_DELAY# — R349 *E@0_4

+1.22V_GFX_PCIE — L15 E@BLM11A121S_6 — G72_PLLVDD
C120 E@4.7U_6.3V_6
C61 E@0.1U_4

+VCC_GFX_CORE
C40 E@100P_4, C45 E@0.01U_4, C58 E@0.01U_4, C42 E@100P_4, C96 E@0.01U_4
C56 E@220P_4, C71 E@100P_4, C84 E@220P_4, C95 E@100P_4, C68 E@1U_6.3V_4
C101 E@220P_4, C66 E@0.01U_4, C87 E@220P_4, C86 E@220P_4, C99 E@10U_6.3V_6
C60 E@10U_6.3V_6, C83 E@10U_6.3V_6
PLACE NEAR BALLS

G72_PLLVDD → VDD_01 … VDD_36 (J9, M9, N9, R9, T9, J10, J11, M11, N11, R11, T11, L12, M12, T12, U12, L13, M13, T13, U13, W13, M14, T14, L15, M15, T15, U15, W15, L16, M16, T16, U16, W16, M17, N17, R17, T17)

PEX_IOVDD_01 … PEX_IOVDD_08 (AB10, AB11, AB14, AB15, W17, W18, AB20, AB21)

PEX_IOVDDQ_01 … PEX_IOVDDQ_19 (AA4, AB5, AB6, AB7, AB8, AB9, AC9, AC11, AB12, AC12, AB13, AB16, AC16, AB17, AC17, AB18, AB19, AC19, AC20)

VDD_LP_01 … VDD_LP_04 (W9, W10, W11, W12)

VDD33_01 … VDD33_06 (J12, F13, J13, F14, J15, J16)

NC_01 … NC_04 (D12, E12, E12, C13)

+1.22V_GFX_PCIE — L44 E@BLM11A121S_6 — PEX_PLL_AVDD (Y6) — PEX_PLLAVDD
C504 E@4.7U_6.3V_6, C501 E@1U_6.3V_4, C503 E@1U_6.3V_4, C107 E@0.1U_4, C97 E@0.01U_4
PEX_PLL_DVDD (AA5) — PEX_PLLDVDD
PEX_PLLGND (AA6)

+1.22V_GFX_PCIE
C106 E@0.1U_4, C121 E@0.022U_4, C118 E@0.022U_4, C114 E@0.022U_4
C112 E@10U_6.3V_6, C122 E@1U_6.3V_4, C510 E@4.7U_6.3V_6
PLACE NEAR BALLS
PLACE NEAR GPU

+1.22V_GFX_PCIE
C111 E@10U_6.3V_6, C117 E@0.022U_4, C116 E@0.1U_4, C108 E@0.1U_4, C123 E@1U_6.3V_4, C508 E@4.7U_6.3V_6
PLACE NEAR BALLS

+VCC_GFX_CORE
C74 E@220P_4, C85 E@0.01U_4, C65 E@0.1U_4

+3VRUN
C39 E@0.1U_4, C54 E@4700P_4, C31 E@0.022U_4, C43 E@1U_6.3V_4
PLACE NEAR BALLS

LE4 B:
Update correct power plane

+1.22V_GFX_PCIE — C100 330U/2.5V-12m
+VCC_GFX_CORE — C17 330U/2.5V-12m
Place near VGA chipset

LE4 A:

G72M

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	VGA G72M (PCIe POWER)	1A
Date: Tuesday, March 14, 2006	Sheet 18 of 42	

LE4 B:
Cancel R355,R367 in BOM

LE4 B:
Cancel parts in BOM

LE4 B:
Cancel parts in BOM

LE4 B:
Cancel parts in BOM

	CFG3	CFG2	CFG1	CFG0
128MB(16M*16)	0	0	1	0
	DEV3	DEV2	DEV1	DEV0
G72M	1	0	0	0

LE4 B:
Update correct power plane

LE4 B:
Cancel R21 in BOM

LE4 B:
Update correct power plane

LE4 B:
Del R361, C481 in BOM

LE4 B:
Cancel R57 in BOM

LE4 B:
Cancel R362 in BOM

LE4 C:
Add U46,R599,C711

Thermal Sensor for Graphic

SLAVE ADDRESS: 9A

LE4 B:
Del R13, R14 in BOM

LE4 C:

B:Change U9 from G781-1 to MAX6649 for thermal issue

D:Change U9 footprint from SOIC8 to MSOP8

Place close to VGA Chip

PROJECT : LE4		
Quanta Computer Inc.		
Size	Document Number	Rev
	VGA-G72M (VIDEO)	1A
Date: Tuesday, March 14, 2006	Sheet 19 of 42	

FB_CMD[0..26] (21)
FBD[0..63] (21)
FBDQM[0..7] (21)
FBDQS[0..7] (21)
FBDQS#[0..7] (21)

U33C

Part 3 of 4

MEMORY INTERFACE

FBD0	A26	FB_DQ0	FB_CMD0	G27	FB_CMD0
FBD1	C24	FB_DQ1	FB_CMD1	D25	FB_CMD1
FBD2	B24	FB_DQ2	FB_CMD2	F26	FB_CMD2
FBD3	A24	FB_DQ3	FB_CMD3	F25	FB_CMD3
FBD4	C22	FB_DQ4	FB_CMD4	G25	FB_CMD4
FBD5	A25	FB_DQ5	FB_CMD5	J25	FB_CMD5
FBD6	B25	FB_DQ6	FB_CMD6	J27	FB_CMD6
FBD7	D23	FB_DQ7	FB_CMD7	M26	FB_CMD7
FBD8	G22	FB_DQ8	FB_CMD8	C27	FB_CMD8
FBD9	J23	FB_DQ9	FB_CMD9	C25	FB_CMD9
FBD10	E24	FB_DQ10	FB_CMD10	D24	FB_CMD10
FBD11	F23	FB_DQ11	FB_CMD11	N27	FB_CMD11
FBD12	J24	FB_DQ12	FB_CMD12	G24	FB_CMD12
FBD13	F24	FB_DQ13	FB_CMD13	J26	FB_CMD13
FBD14	G23	FB_DQ14	FB_CMD14	M27	FB_CMD14
FBD15	H24	FB_DQ15	FB_CMD15	C26	FB_CMD15
FBD16	D16	FB_DQ16	FB_CMD16	M25	FB_CMD16
FBD17	E16	FB_DQ17	FB_CMD17	D26	FB_CMD17
FBD18	D17	FB_DQ18	FB_CMD18	D27	FB_CMD18
FBD19	E18	FB_DQ19	FB_CMD19	K26	FB_CMD19
FBD20	E19	FB_DQ20	FB_CMD20	K25	FB_CMD20
FBD21	E18	FB_DQ21	FB_CMD21	K24	FB_CMD21
FBD22	D20	FB_DQ22	FB_CMD22	F27	FB_CMD22
FBD23	D19	FB_DQ23	FB_CMD23	K27	FB_CMD23
FBD24	A18	FB_DQ24	FB_CMD24	G26	FB_CMD24
FBD25	B18	FB_DQ25	FB_CMD25	B27	FB_CMD25
FBD26	A19	FB_DQ26	FB_CMD26	N24	FB_CMD26
FBD27	B19	FB_DQ27			
FBD28	D18	FB_DQ28			
FBD29	C19	FB_DQ29			
FBD30	C16	FB_DQ30	FB_DQM0	D21	FBDQM0
FBD31	C18	FB_DQ31	FB_DQM1	F22	FBDQM1
FBD32	N26	FB_DQ32	FB_DQM2	F20	FBDQM2
FBD33	N25	FB_DQ33	FB_DQM3	A21	FBDQM3
FBD34	R25	FB_DQ34	FB_DQM4	V27	FBDQM4
FBD35	R26	FB_DQ35	FB_DQM5	W22	FBDQM5
FBD36	R27	FB_DQ36	FB_DQM6	V22	FBDQM6
FBD37	T25	FB_DQ37	FB_DQM7	V24	FBDQM7
FBD38	T27	FB_DQ38			
FBD39	T26	FB_DQ39	FB_DQS_RN0	A22	FBDQS#0
FBD40	AB23	FB_DQ40	FB_DQS_RN1	E22	FBDQS#1
FBD41	Y24	FB_DQ41	FB_DQS_RN2	F21	FBDQS#2
FBD42	AB24	FB_DQ42	FB_DQS_RN3	B21	FBDQS#3
FBD43	AB22	FB_DQ43	FB_DQS_RN4	V26	FBDQS#4
FBD44	AC24	FB_DQ44	FB_DQS_RN5	W23	FBDQS#5
FBD45	AC22	FB_DQ45	FB_DQS_RN6	V23	FBDQS#6
FBD46	AA23	FB_DQ46	FB_DQS_RN7	W27	FBDQS#7
FBD47	AA22	FB_DQ47			
FBD48	T24	FB_DQ48	FB_DQS_WP0	B22	FBDQS0
FBD49	T23	FB_DQ49	FB_DQS_WP1	D22	FBDQS1
FBD50	R24	FB_DQ50	FB_DQS_WP2	E21	FBDQS2
FBD51	R23	FB_DQ51	FB_DQS_WP3	C21	FBDQS3
FBD52	R22	FB_DQ52	FB_DQS_WP4	V25	FBDQS4
FBD53	T22	FB_DQ53	FB_DQS_WP5	W24	FBDQS5
FBD54	N23	FB_DQ54	FB_DQS_WP6	U24	FBDQS6
FBD55	P24	FB_DQ55	FB_DQS_WP7	W26	FBDQS7
FBD56	AA24	FB_DQ56			
FBD57	AA27	FB_DQ57			
FBD58	AA26	FB_DQ58			
FBD59	AB25	FB_DQ59			
FBD60	AB26	FB_DQ60	FBVTT_01	E15	
FBD61	AB27	FB_DQ61	FBVTT_02	F15	
FBD62	AA25	FB_DQ62	FBVTT_03	F16	
FBD63	W25	FB_DQ63	FBVTT_04	J17	
			FBVTT_05	J18	
			FBVTT_06	L19	
			FBVTT_07	N19	
			FBVTT_08	R19	
			FBVTT_09	U19	
			FBVTT_10	W19	
			FBVDDQ_01	F17	
			FBVDDQ_02	F19	
			FBVDDQ_03	J19	
			FBVDDQ_04	M19	
			FBVDDQ_05	T19	
			FBVDDQ_06	J22	
			FBVDDQ_07	L22	
			FBVDDQ_08	P22	
			FBVDDQ_09	U22	
			FBVDDQ_10	Y22	
(21) FB_CLK0	L24	FB_CLK0			
(21) FB_CLK0#	K23	FB_CLK0#			
(21) FB_CLK1	M22	FB_CLK1			
(21) FB_CLK1#	N22	FB_CLK1#			
	M23	FB_REFCLK			
	M24	FB_REFCLK#			
T4	K22	FB_DEBUG			
FBVREF	A16	FB_VREF			
	D14	FB_PLLVDD	FBCAL_PD_VDDQ	D15	FBCAL_PD_VDDQ
	D13	FB_PLLAVDD	FBCAL_PU_GND	E13	FBCAL_PU_GND
	C15	FB_PLLAGND	FBCAL_TERM_GND	H22	FBCAL_TERM_GND

read strobe

write strobe

T6

T5

G72M

U33D

Part 4 of 4

GND

B2	GND_01	GND_48	P14
F2	GND_02	GND_49	R14
H2	GND_03	GND_50	U14
L2	GND_04	GND_51	W14
P2	GND_05	GND_52	AC14
U2	GND_06	GND_53	AD14
Y2	GND_07	GND_54	N15
AC2	GND_08	GND_55	P15
AF2	GND_09	GND_56	R15
AF3	GND_10	GND_57	AF15
B5	GND_11	GND_58	N16
E5	GND_12	GND_59	P16
L5	GND_13	GND_60	R16
P5	GND_14	GND_61	AD16
U5	GND_15	GND_62	B17
Y5	GND_16	GND_63	E17
AC5	GND_17	GND_64	L17
H6	GND_18	GND_65	P17
AF6	GND_19	GND_66	U17
B8	GND_20	GND_67	AD17
E8	GND_21	GND_68	AF18
AD8	GND_22	GND_69	K19
K9	GND_23	GND_70	P19
P9	GND_24	GND_71	V19
V9	GND_25	GND_72	AD19
AD9	GND_26	GND_73	B20
AF9	GND_27	GND_74	E20
B11	GND_28	GND_75	AD20
E11	GND_29	GND_76	AF21
F11	GND_30	GND_77	B23
L11	GND_31	GND_78	E23
P11	GND_32	GND_79	H23
U11	GND_33	GND_80	L23
AD11	GND_34	GND_81	P23
N12	GND_35	GND_82	U23
P12	GND_36	GND_83	Y23
R12	GND_37	GND_84	AC23
AD12	GND_38	GND_85	AF24
AF12	GND_39	GND_86	B26
N13	GND_40	GND_87	E26
P13	GND_41	GND_88	H26
R13	GND_42	GND_89	L26
B14	GND_43	GND_90	P26
E14	GND_44	GND_91	U26
J14	GND_45	GND_92	Y26
L14	GND_46	GND_93	AC26
N14	GND_47	GND_94	AF26

G72M

+1.8VRUN
R365 E@1K/F_4
FBVREF
R364 E@1K/F_4
C489 E@0.1U_4

FBVREF = FBVDDQ * Rb/(Rt + Rb).
VREF = 0.5 * FBVDDQ.
DDR: 0.9V = 1.8V * 1K/(1K + 1K).

LE4 B: del L5 in BOM

+3VRUN
L5 *E@BLM11A121S_6
FBA_PLLVDD
+1.22V_GFX_PCIE
FB_PLLAVDD
L7 E@BLM11A121S_6
C21 E@4.7U_6.3V_6
C23 E@1U_6.3V_4
C26 E@0.01U_4

+1.8VRUN
R34 E@40.2/F_4
R40 E@0_4
R32 E@30/F_4

LE4 B: del R40 in BOM

PLACE BELOW GPU

+1.8VRUN
C104 E@4700P_4
C103 E@0.022U_4
C15 E@0.1U_4
C14 E@4700P_4
C160 E@0.1U_4
C93 E@4.7U_6.3V_6
C161 E@1U_6.3V_4
C47 E@4700P_4
C48 E@0.022U_4
C63 E@0.1U_4
C62 E@4700P_4
C76 E@0.022U_4
C77 E@0.1U_4
C88 E@4.7U_6.3V_6
C44 E@4700P_4
C35 E@0.022U_4
C36 E@0.1U_4
C50 E@0.022U_4
C37 E@0.1U_4
C82 E@1U_6.3V_4

+1.8VRUN
C16 330U/2.5V-12m

LE4 A:
Place near VGA chipset

PROJECT : LE4
Quanta Computer Inc.

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	VGA-G72M (MENORY, GND)	1A
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FB_CMD[0..26] (20)
FBD[0..63] (20)
FBDQM[0..7] (20)
FBDQS[0..7] (20)
FBDQS#[0..7] (20)

R48 E@10K_4 FB_CMD12
R384 E@10K_4 FB_CMD11
R358 E@120_4 FB_CLK0 FB_CLK0#
R52 E@120_4 FB_CLK1 FB_CLK1#

U32 VRAM
U4 VRAM
U7 VRAM
U34 VRAM

R47 E@1K/F_4
R383 E@1K/F_4
C81 E@0.1U_P_4
R50 E@1K/F_4
R385 E@1K/F_4
C91 E@0.1U_P_4

C485 C494 E@0.01U_4 C493 E@0.01U_4 E@4.7U_6.3V_6
C483 E@0.1U_4 C492 C484 E@0.01U_4 E@0.1U_10V_4
C8 C79 E@0.1U_4 C9 E@0.01U_4 E@4.7U_6.3V_6
C10 E@0.1U_4 C80 C78 E@0.01U_4
C496 C41 E@0.1U_4 C486 E@0.01U_4 E@4.7U_6.3V_6
C90 E@0.1U_4 C92 C89 E@0.01U_4
C495 C498 E@0.1U_4 C11 E@0.01U_4 E@4.7U_6.3V_6
C499 E@0.1U_4 C49 C497 E@0.01U_4

+1.8VRUN VREF1 VREF2 FB_CLK0 FB_CLK0# FB_CLK1 FB_CLK1#

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	VGA-G72M (VRAM)	1A
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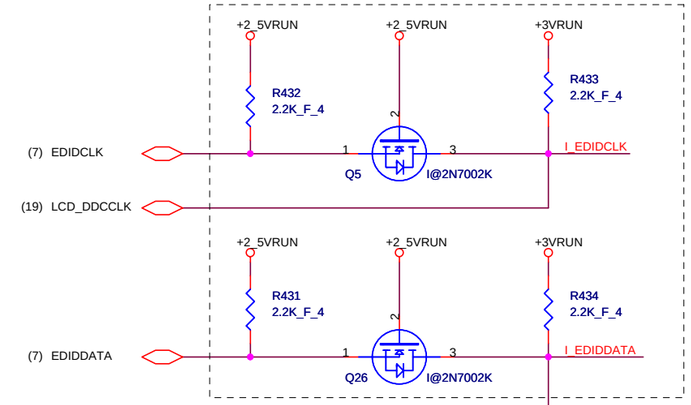
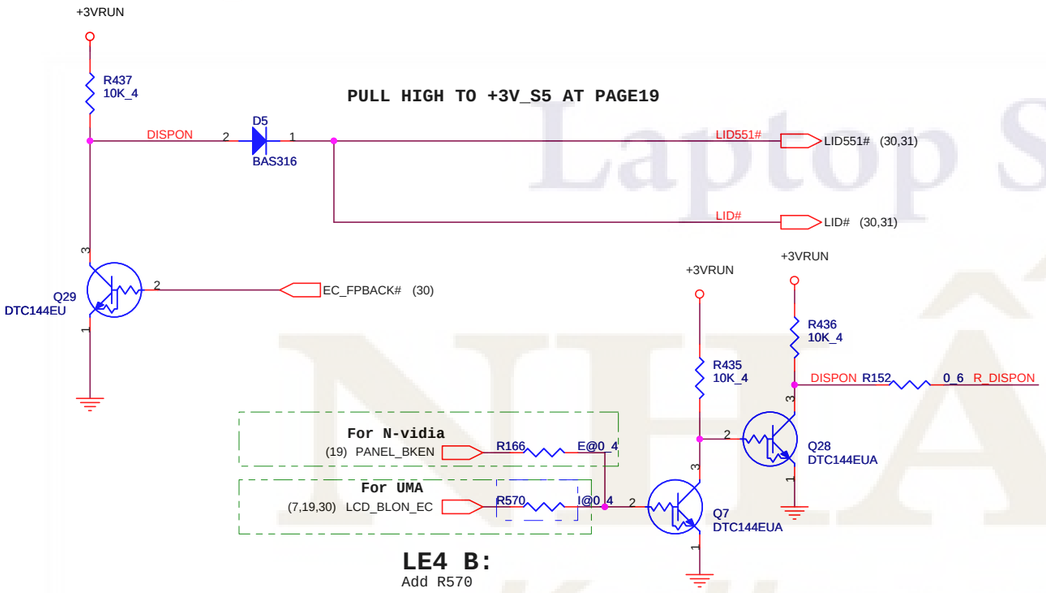
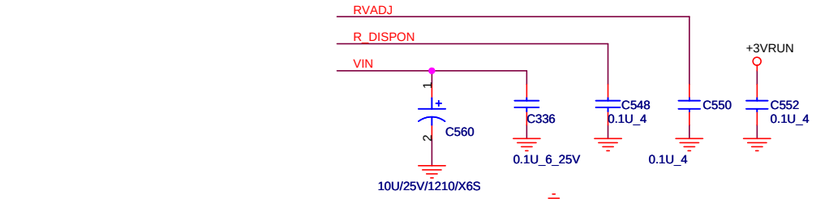
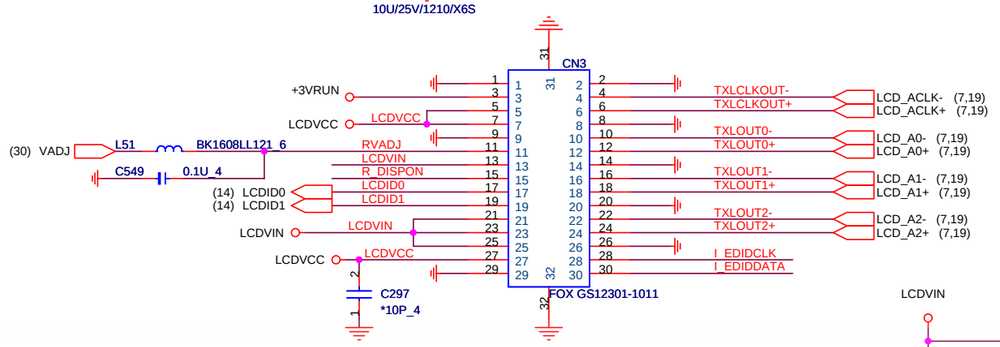


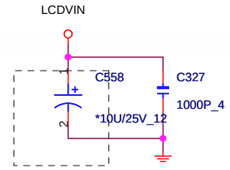
ADD LEVEL SHIFT FOR EDID



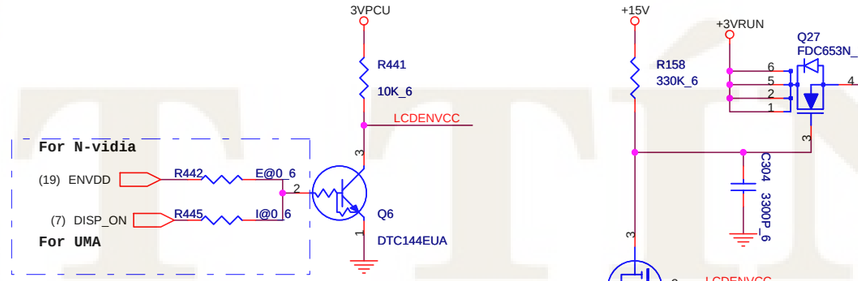
LE4 B:
Add R570



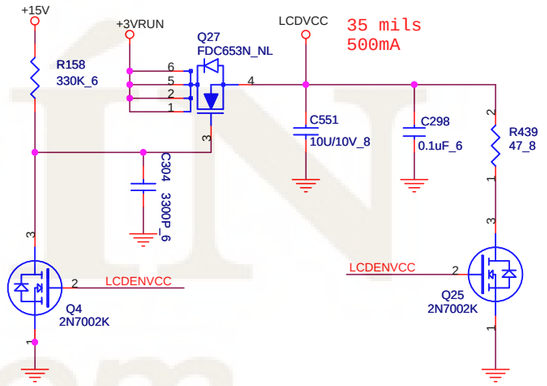




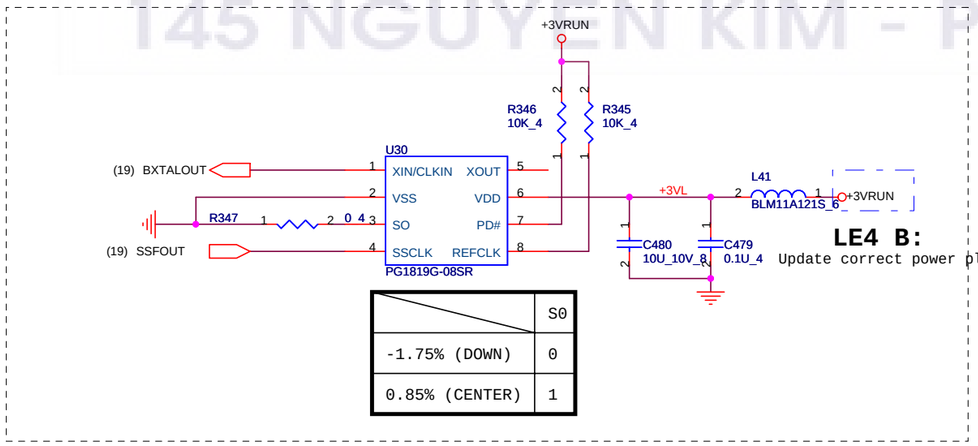
LCD CONNECTOR



LE4 B:
Add opantion

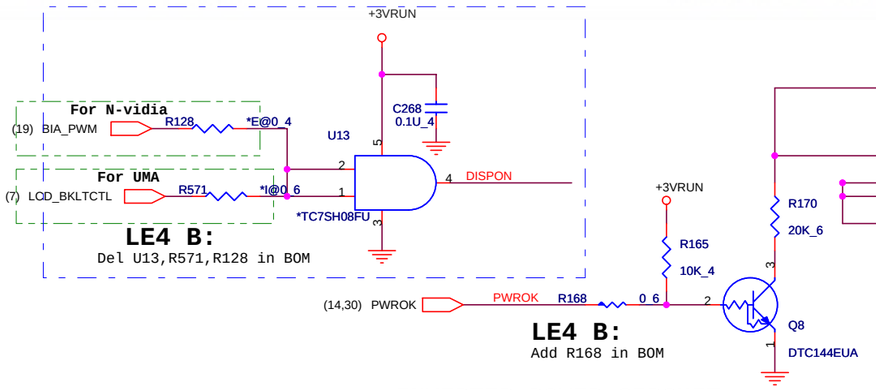


LCD VCC



LE4 B:
Update correct power plane

	S0
-1.75% (DOWN)	0
0.85% (CENTER)	1



LE4 B:
Del U13,R571,R128 in BOM

LE4 B:
Add R168 in BOM

INVERTER POWER CIRCUIT

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	LCD CON. & LCD POWER	1A
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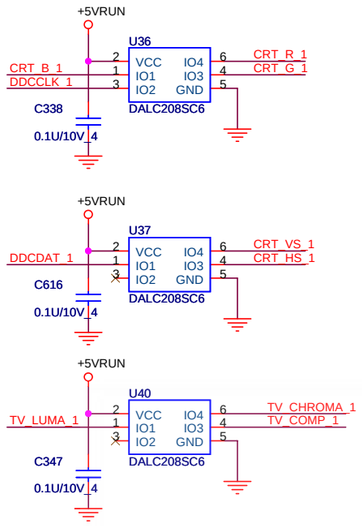
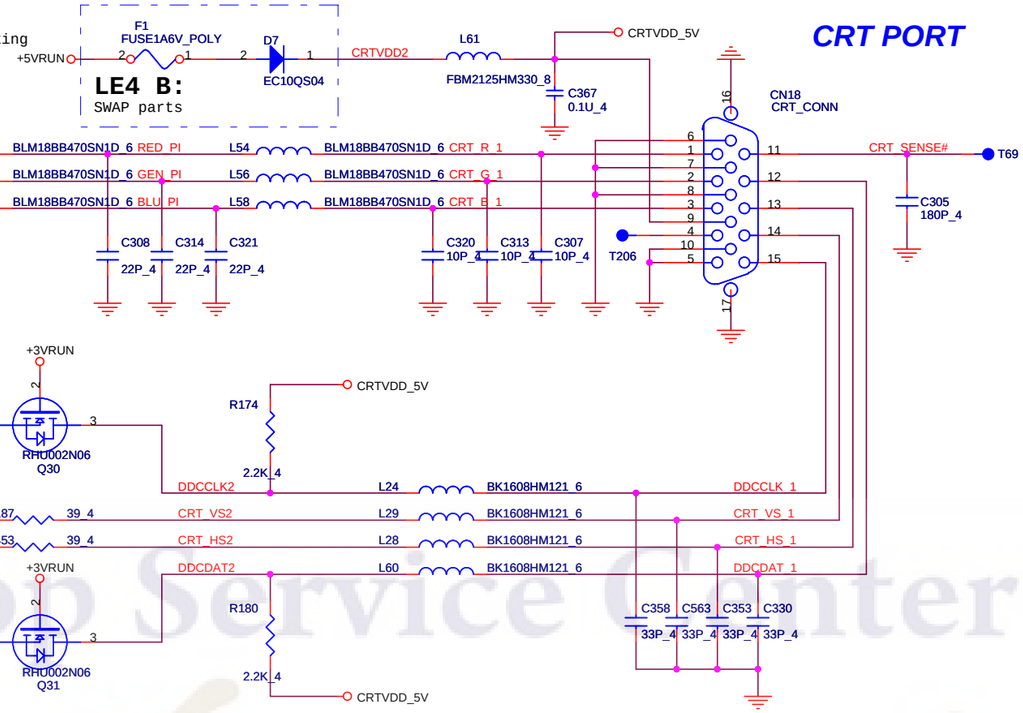
ESD PORTECTION



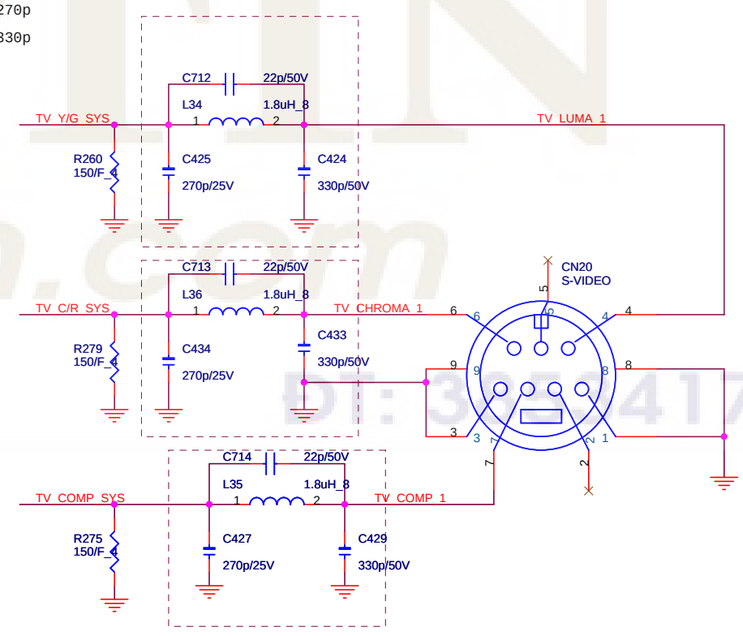
CRT PORT

LE4 C:
Change D7 packing



TV-OUT

LE4 C:
Change C425,C434 and C427 from 6p to 270p
Change C424,C433 and C429 from 6p to 330p
ChangeL35 size from 0603 to 0805
Add C712 ,C713 and C714



(7) CRT_R_COM
(7) CRT_G_COM
(7) CRT_B_COM
R414 I@0_4 VGA_RED_SYS
R410 I@0_4 VGA_GEN_SYS
R405 I@0_4 VGA_BLU_SYS

(7) VSYNC_COM
(7) HSYNC_COM
RN4 I@4P2R-S-0 VSYNC
HSYNC

(7) DDCCLK
(7) DDCDAT
RN2 I@4P2R-S-0 CRTDCLK
CRTDDAT

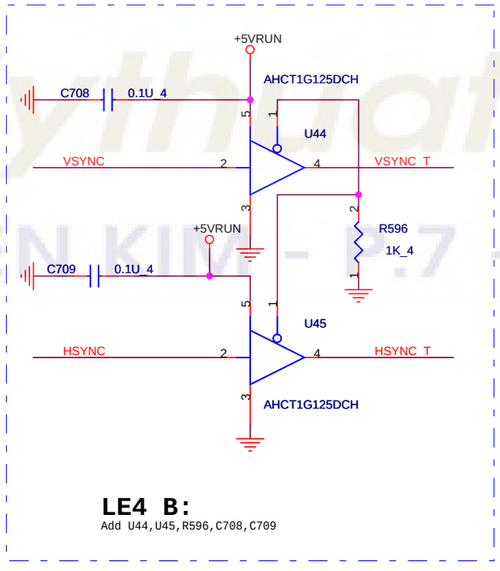
(19) VGA_RED
(19) VGA_GRN
(19) VGA_BLU
R413 E@0_4 VGA_RED_SYS
R408 E@0_4 VGA_GEN_SYS
R402 E@0_4 VGA_BLU_SYS

(19) VGAVSYNC
(19) VGAHSYNC
RN3 E@4P2R-S-0 VSYNC
HSYNC

(19) VGADDCCLK
(19) VGADDCDAT
RN1 E@4P2R-S-0 CRTDCLK
CRTDDAT

(7) TV_Y/G
R422 I@0_4 TV_Y/G_SYS
(7) TV_C/R
R418 I@0_4 TV_C/R_SYS
(7) TV_COMP
R427 I@0_4 TV_COMP_SYS

(19) TV_Y
R424 E@0_4 TV_Y/G_SYS
(19) TV_C
R420 E@0_4 TV_C/R_SYS
(19) TV_CVBS
R429 E@0_4 TV_COMP_SYS



LE4 B:
Add U44,U45,R596,C708,C709

Intel CRB

150 ohm@ 100MHZ
(100mA)

6pf 16V 6pf 16V

CX8PG181001 (180 ohm ,1.5A)

CH00606TB04 CH00606TB04

PROJECT : LE4
Quanta Computer Inc.

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	CRT & TV-OUT CONN	1A
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LE4 B:
SAWP GNT2# AND REQ2#

(13) GNT2# — GNT2# — L2
(13) REQ2# — REQ2# — L3
AD25 R280 150_4 — N5
(13,33) FRAME# — FRAME# — R6
(13,33) IRDY# — IRDY# — V5
(13,33) DEVSEL# — DEVSEL# — U6
(13,33) TRDY# — TRDY# — W5
(13,33) SERR# — SERR# — W6
(13,33) STOP# — STOP# — V6
(13,33) PERR# — PERR# — R7
(13,33) PAR — PAR — U7
(13,33) C/BE3# — P2
(13,33) C/BE2# — U5
(13,33) C/BE1# — V7
(13,33) C/BE0# — C/BE0# — W10
(3) PCLK_PCM — PCLK_PCM — L1
(13,25,33) PCIRST# — PCIRST# — K3
GRST# — K5
(13,33) AD[0..31]

AD0 R11, AD1 P11, AD2 U11, AD3 V11, AD4 W11, AD5 R10, AD6 U10, AD7 V10, AD8 R9, AD9 U9, AD10 V9, AD11 W9, AD12 V8, AD13 U8, AD14 R8, AD15 W7, AD16 W4, AD17 T2, AD18 T1, AD19 R3, AD20 P5, AD21 R2, AD22 R1, AD23 P3, AD24 N3, AD25 N2, AD26 N1, AD27 M5, AD28 M6, AD29 M3, AD30 M2, AD31 M1

U22A

GNT# L2, REQ# L3, IDSEL, FRAME# R6, IRDY# V5, DEVSEL# U6, TRDY# W5, SERR# W6, STOP# V6, PERR# R7, PAR U7, CBE3 P2, CBE2 U5, CBE1 V7, CBE0 W10, PCLK L1, PRST# K3, GRST# K5, AD00 R11, AD01 P11, AD02 U11, AD03 V11, AD04 W11, AD05 R10, AD06 U10, AD07 V10, AD08 R9, AD09 U9, AD10 V9, AD11 W9, AD12 V8, AD13 U8, AD14 R8, AD15 W7, AD16 W4, AD17 T2, AD18 T1, AD19 R3, AD20 P5, AD21 R2, AD22 R1, AD23 P3, AD24 N3, AD25 N2, AD26 N1, AD27 M5, AD28 M6, AD29 M3, AD30 M2, AD31 M1

PCI Interface | 1394 Interface | Miscellaneous

PCI7412

PN

1394_XIN — C391 12P-50V_4 — Y3 FW@24.576MHZ B6624576473 — C389 12P-50V_4 — 1394_XOUT
XI R19, XO R18
R0 T18, R1 T19, CPS R12, TEST0 P12, VSSPLL R17
R0 R205 FW@6.34K/F_4
CPS R237 FW@0_4
R241 FW@0_4

LE4 C:
Change R237 and R241 from 390K and 330 to 0 ohm

TPA0P V14, TPA0N W14, TPBIAS0 R13, TPB0P V13, TPB0N W13
TPA1P V16, TPA1N W16, TPBIAS1 W17, TPB1P V15, TPB1N W15
1394_TPA1+ T91, 1394_TPA1- T90, TPBIAS1 T89, 1394_TPB1+ T93, 1394_TPB1- T95

VDDPLL15 P15, PHY_TEST_MA P17
R219 FW@4.7K_4 — 1394_AVDD — C394 1U-16V_6
PC0_RSVD U12, PC1_RSVD V12, PC2_RSVD W12
AGND_00 U13, AGND_01 U14, AGND_02 R14
3VSUS — R283 10K_4 — D2 *1SS355_NC — SUS_STAT# (14,26,27)
SUSPEND# J5, RI_OUT# L5, SPKROUT H3
R281 0_4 — PCMSPK — PCI_PME# (13,33)
R282 *0_4 — PCMSPK (28)
RI# (14,26)
VR_EN# K2, USB_EN E10
SCL G2, SDA G3 — SCL_CARD — SDA_CARD

MFUNC0 G1 — INTC# — INTC# (13)
MFUNC1 H5 — INTD# — INTD# (13)
MFUNC2 H2 — INTE# — INTE# (13)
MFUNC3 H1 — SERIRQ (14,26,27,30)
MFUNC4 J1 — R284 10K_4 — 3VSUS
MFUNC5 J2 — T111
MFUNC6 J3 — CLKRUN# (14,26,27,30,33)

LATCH/VD3/VPPD0 C9 — R249 0_4 — TPS_LATCH (25)
CLOCK/VD1/VCCD0# A9 — R245 0_4 — TPS_CLOCK (25)
DATA/VD2/VPPD1 B9 — R240 0_4 — TPS_DATA (25)
RSVD_03/VD0/VCCD1#/PS_MODE C4 — R278 10K_4 — 3VSUS

LE4 A-1108;

LE4 C:
Add C?, solve 1394 hang up and busy on system.

LE4 B:
TPBIAS0 — C715 270P-25V_4 — R38 FW@56.2/F_4 — R39 FW@56.2/F_4 — C34 1U-16V_6
TPA0P — TPA0N — R24 FW@0_4 — R23 FW@0_4 — L1394_TPA0+ — L1394_TPA0-
TPB0P — TPB0N — R26 0_4 — R25 0_4 — L1394_TPB0+ — L1394_TPB0-
R37 FW@56.2/F_4 — R36 FW@56.2/F_4
R42 FW@5.1K/F_6 — C28 270P-25V_4

LE4 B:
No Struff
L9 *PLW3216S900SQ2T1 <PN>
TPA0P — L1394_TPA0+
TPA0N — L1394_TPA0-
L10 *PLW3216S900SQ2T1 <PN>
TPB0P — L1394_TPB0+
TPB0N — L1394_TPB0-
J1 — FOX_UV31413-K1
L1394_TPB0- 1, L1394_TPA0- 3, L1394_TPA0+ 4, L1394_TPB0+ 2, 5, 6

1394_TPA1+, 1394_TPA1-, TPBIAS1, 1394_TPB1+, 1394_TPB1-
PCMSPK — R604 47K_4
R600 0_4, R601 0_4, R602 0_4, R603 0_4
C716 1U-16V_6

LE4 C:
Solve to hang up and busy on system

3VSUS — R286 100K_4 — C436 0.22U/10V_4
GRST# — D3 *1SS355_NC — GRST#_7402 (30)
D18 *1SS355_NC — R285 *0_4 — PCIRST#

LE4 B:
Add L71
3VSUS — L71 FW@BK1608HS800_6 — L32 FW@BK1608HS800_6
1394_AVDD — C398 0.1U-10V_4 — C392 1U-16V_6
PCLK_PCM — R290 *33_4 — C440 *10P_4

3VSUS — R261 2.2K_4, R264 2.2K_4, R262 *220_4, R263 *220_4
U24 24LC02BT: VCC 8, NC 7, SCL 6, SDA 5, A0 1, A1 2, A3 3, GND 4
SCL_CARD, SDA_CARD
3VSUS — C422 0.1U-10V_4

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DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

3 IN1 CARD READER (push-push)

U22C

FlashMedia Interface

SC_OC# F2
SC_PWR_CTRL G5
SC_VCC5 G6
SD_CMD/SM_ALE/SC_GPIO2 C5
SD_CLK/SM_RE#/SC_GPIO1 A4
SM_CLE/SC_GPIO0 B4
SM_R/B#/SC_RFU D1
SM_PHYS_WP#/SC_FCB E3
SC_CLK E2
SC_RST F5
SC_DATA E1
CLK_48 F1 — TI_CLK48M — TI_CLK48M (3)
SC_CD# E3
SD_CD# E9 — SD_CDZ
MS_CD# A8 — MS_CDZ
SM_CD# B8
XD_CD#/SM_PHYS_WP# A3
MC_PWR_CTRL_0 C8 — MC_PWR_CTRL_0#
MC_PWR_CTRL_1/SM_R/B# E8 — SM_R/B# — R266 CR@10K_4
MS_BS/SD_CMD/SM_WE# E8 — MS_BS_SD_CMD_SM_WEZ — R271 CR@10K_4
MS_CLK/SD_CLK/SM_EL_WP# A7 — MS_CLK_SD_CLK_SM_ELWPZ_R — R254 47_6 — MS_CLK_SD_CLK_SM_ELWPZ
MS_SDIO(DATA0)/SD_DATA0/SM_D0 B7 — MS_DATA0_SD_DAT0_SM_D0
MS_DATA1/SD_DATA1_SM_D1 C7 — MS_DATA1_SD_DAT1_SM_D1
MS_DATA2/SD_DATA2_SM_D2 A6 — MS_DATA2_SD_DAT2_SM_D2
MS_DATA3/SD_DATA3_SM_D3 B6 — MS_DATA3_SD_DAT3_SM_D3
SD_WP/SM_CE# E7 — SD_WP_SM_CEZ — R277 CR@10K_4
SD_DAT0/SM_D4/SC_GPIO6 C6
SD_DAT1/SM_D5/SC_GPIO5 A5
SD_DAT2/SM_D6/SC_GPIO4 B5
SD_DAT3/SM_D7/SC_GPIO3 E6

PCI7412

VCC_FM

CN8

MS_DATA3_SD_DAT3_SM_D3 — 18 SD-1(DAT3)
MS_BS_SD_CMD_SM_WEZ — 15 SD-2(CMD)
12 SD-3(VSS)
10 SD-4(VCC)
MS_CLK_SD_CLK_SM_ELWPZ — 7 SD-5(CLK)
4 SD-6(VSS)
MS_DATA0_SD_DAT0_SM_D0 — 3 SD-7(DAT0)
MS_DATA1_SD_DAT1_SM_D1 — 2 SD-8(DAT1)
MS_DATA2_SD_DAT2_SM_D2 — 20 SD-9(DAT2)
SD_CDZ — 21 SD-CD1
23 SD-CD2(G)
SD_WP_SM_CEZ — 1 SD-WP1
22 SD-WP-COM
24 NAIL1
25 NAIL2
26 NAIL3

(VSS)MS-1 5
(BS)MS-2 6
(DAT1)MS-3 8
(DAT0)MS-4 9
(DAT2)MS-5 11
(INS)MS-6 13
(DAT3)MS-7 14
(SCLK)MS-8 16
(VCC)MS-9 17
(VSS)MS-10 19

MS_BS_SD_CMD_SM_WEZ
MS_DATA1_SD_DAT1_SM_D1
MS_DATA0_SD_DAT0_SM_D0
MS_DATA2_SD_DAT2_SM_D2
MS_CDZ
MS_DATA3_SD_DAT3_SM_D3
MS_CLK_SD_CLK_SM_ELWPZ

3@3IN1_DFHD23MS069

VCC_FM

C451 0.1U-10V_4 — C410 0.1U-10V_4 — C409 CR@.1U-10V_4 — C443 CR@.1U-10V_4

LE4 D:
change footprint form
3IN1-R009-020-XX-21P to
3IN1-R009-020-XX-21P-LE4

3VSUS

Q35 TPS2061DGNR
R242 CR@10K_4
MC_PWR_CTRL_0#
IN1 IN2 EN# GND GND-C OC# OUT3 OUT2 OUT1
VCC_FM
C598 10U-10V_8
C411 0.1U-10V_4

Supporting MMC/SD/MS Cards
Foxconn P/N:DFHS19FR012

U22B

CardBus Interface

CAD31 C10 A_CAD31
CAD30 A10 A_CAD30
CAD29 F11 A_CAD29
CAD28 E11 A_CAD28
CAD27 C11 A_CAD27
CAD26 B13 A_CAD26
CAD25 C13 A_CAD25
CAD24 A14 A_CAD24
CAD23 B14 A_CAD23
CAD22 B15 A_CAD22
CAD21 E14 A_CAD21
CAD20 A16 A_CAD20
CAD19 D19 A_CAD19
CAD18 E17 A_CAD18
CAD17 F15 A_CAD17
CAD16 H19 A_CAD16
CAD15 J17 A_CAD15
CAD14 J15 A_CAD14
CAD13 J18 A_CAD13
CAD12 K15 A_CAD12
CAD11 K17 A_CAD11
CAD10 K18 A_CAD10
CAD09 L15 A_CAD9
CAD08 L18 A_CAD8
CAD07 L19 A_CAD7
CAD06 M17 A_CAD6
CAD05 M18 A_CAD5
CAD04 N19 A_CAD4
CAD03 M15 A_CAD3
CAD02 N17 A_CAD2
CAD01 N18 A_CAD1
CAD00 P19 A_CAD0

CCBE3 E13 A_CC/BE3#
CCBE2 E18 A_CC/BE2#
CCBE1 H18 A_CC/BE1#
CCBE0 L17 A_CC/BE0#

RSVD_04/D2 B10 A_CRSVD/D2
CCD1#/CD1# N15 A_CCD1#
CCD2#/CD2# B11 A_CCD2#

CVS1/VS1# A13 A_CVS1#
CRST# C15 A_CRST#
CBLOCK# H15 A_CBLOCK#
CREQ#/INPACK# C14 A_CREQ#
CSERR#/WAIT# C12 A_CSERR#
CDEVSEL# F19 A_CDEVSEL#
CFRAME# E19 A_CFRAME#
CGRANT# G17 A_CGNT#
CINT# F12 A_CINT#
CVS2/VS2# B16 A_CVS2#
CPERR# G19 A_CPERR#
CSTOP# G18 A_CSTOP#
CIRDY F17 A_CIRDY#
CTRDY# G15 A_CTRDY#

RSVD_02/A18 H17 A_CRSVD/A18
RSVD_01/D14 M19 A_RSVD/D14

CCLKRUN# A11 A_CCLKRUN#
CPAR H14 A_CPAR
VCCCA_01 A15
VCCCA_00 J19 — A_VCC
CSTSCHG A12 A_CSTSCHG
CAUDIO B12 A_CAUDIO
CCLK F18 A_CCLK — R443 47_6 — A_CCLK1

PCI7412

CN4

A_CAD0 1
A_CAD1 2
A_CAD3 3
A_CAD5 4
A_CAD7 5
A_CC/BE0# 6
A_CAD9 7
A_CAD11 8
A_CAD12 9
A_CAD14 10
A_CC/BE1# 11
A_CPAR 12
A_CPERR# 13
A_CGNT# 14
A_CINT# 15
16

GND1 SKTAAD0/D3 SKTAAD1/D4 SKTAD3/D5 SKTAD5/D6 SKTAAD7/D7 -SKTACBE0/CE1# SKTAAD9/A10 SKTABAD11/OE# SKTAAD12/A11 SKTAAD14/A9 -SKTACBE1/A8 SKTAPAR/A13 -SKTAPERR/A14 -SKTAGNT/WE# -SKTAINT/RDY

UPPER PIN

SKTAPCLK/A16 -SKTAIRDY/A15 -SKTACBE2/A12 SKTAAD18/A7 SKTAAD20/A6 SKTAAD21/A5 SKTAAD22/A4 SKTAAD23/A3 SKTAAD24/A2 SKTAAD25/A1 SKTAAD26/A0 SKTAAD27/D0 SKTAAD29/D1 SKTARSVD/D2 -SKTACLKRUN/WP GND2

A_CCLK1 19
A_CIRDY# 20
A_CC/BE2# 21
A_CAD18 22
A_CAD20 23
A_CAD21 24
A_CAD22 25
A_CAD23 26
A_CAD24 27
A_CAD25 28
A_CAD26 29
A_CAD27 30
A_CAD29 31
A_CRSVD/D2 32
A_CCLKRUN# 33
34
35
A_CCD1# 36
A_CAD2 37
A_CAD4 38
A_CAD6 39
A_RSVD/D14 40
A_CAD8 41
A_CAD10 42
A_CVS1# 43
A_CAD13 44
A_CAD15 45
A_CAD16 46
A_CRSVD/A18 47
A_CBLOCK# 48
A_CSTOP# 49
A_CDEVSEL# 50

GND3 -SKTACD1/CD1# SKTAAD2/D11 SKTAD4/D12 SKTAAD6/D13 SKTARSVD/D14 SKTAAD8/D15 SKTAAD10/CE2# -SKTAVS1/VS1# SKTAAD13/IORD# SKTAAD15/IOWR# SKTAAD16/A17 -SKTRSVD/A18 -SKTALOCK/A19 -SKTASTOP/A20 -SKTADEVSEL/A21

LOWER PIN

A_CTRDY# 53
A_CFRAME# 54
A_CAD17 55
A_CAD19 56
A_CVS2# 57
A_CRST# 58
A_CSERR# 59
A_CREQ# 60
A_CC/BE3# 61
A_CAUDIO 62
A_CSTSCHG 63
A_CAD28 64
A_CAD30 65
A_CAD31 66
A_CCD2# 67
68

-SKTATRDY/A22 -SKTAFRAME/A23 SKTAAD17/A24 SKTAAD19/A25 -SKTAVS2VS2# -SKTARST/RESET 0SKTASERR/WAIT# -SKTAREQ/INPACK# -SKTACBE3/REG# SKTAAUDIO/BVD2 -SKTASTSCHG/BVD1 SKTAAD28/D8 SKTAAD30/D9 SKTAAD31/D10 -SKTACD2/CD2# GND4

SKTA/VCC1 17 — A_VCC
SKTA/VCC2 51
SKTA/VPP1 18 — A_VPP
SKTA/VPP2 52
GND5 69
GND6 70
GND7 71
GND8 72

CARDBUS SLOT
FOX_1CA4C5G2-TC_CARD BUS

CARD BUS

3VSUS

C415 0.1U-10V_4 — C412 10U-10V_8
C418 0.1U-10V_4 — C396 0.1U-10V_4 — C435 10U-10V_8 — C416 0.01U-16V_4 — C397 0.01U-16V_4
C421 0.1U-10V_4 — C423 1U-16V_6 — C437 1U-16V_6
1394_AVDD
C403 0.1U-10V_4 — C399 1U-16V_6
VCC_FM
C441 2.2U-6.3V_6
R302 CR@150K_6
C395 0.1U-10V_4
1394_AVDD
CLOSE CONN

U22D

Power/GND

1.5V_00 K1
1.5V_01 K19
VDDPLL33 U19
GND_00 H6
GND_01 K6
GND_02 N6
GND_03 P7
GND_04 P9
GND_05 M14
GND_06 K14
GND_07 G14
GND_08 F13
GND_09 F10
GND_10 F7

VCC33_00 J6
VCC33_01 L6
VCC33_02 P6
VCC33_03 P8
VCC33_04 P10
VCC33_05 L14
VCC33_06 J14
VCC33_07 F14
VCC33_08 F12
VCC33_09 F9
VCC33_10 F6
AVDD33_00 P13
AVDD33_01 P14
AVDD33_02 U15
VCCP_00 P1
VCCP_01 W8

3VSUS
1394_AVDD
3VSUS

PCI7412

5VSUS

U18

(24) TPS_DATA — TPS_DATA
(24) TPS_CLOCK — TPS_CLOCK
(24) TPS_LATCH — TPS_LATCH
T74
A_VPP
A_VCC
(13,24,33) PCIRST#

1 5V_0
2 5V_1
3 DATA
4 CLOCK
5 LATCH
6 NC_0
7 12V_0
8 AVPP/AVCORE
9 AVCC0
10 AVCC1
11 GND
12 RESET#
25 NC

24 5V_2
23 NC_3
22 NC_2
21 SHDN#
20 12V_1
19 BVPP/BVCORE
18 BVCC1
17 BVCC0
16 NC_1
15 OC#
14 3.3VIN0
13 3.3VIN1

3VSUS

TPS2220APWP

TPS_CLOCK
R457 *47K_4

A_VPP
C571 0.1U-10V_4 — C570 0.01U-16V_4
5VSUS
C581 0.1U-10V_4 — C575 10U-10V_8
3VSUS
C583 0.1U-10V_4 — C584 0.1U-10V_4 — C580 10U-10V_8 — C588 0.01U-16V_4 — C582 0.01U-16V_4

A_VCC
C568 0.01U-16V_4 — C567 0.01U-16V_4 — C572 0.1U-10V_4 — C574 0.1U-10V_4 — C576 10U-10V_8
A_VCC
C569 0.01U-16V_4 — C577 10U-10V_8
3VSUS
C587 0.1U-10V_4 — C586 1U-16V_6 — C585 1U-16V_6

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Quanta Computer Inc.

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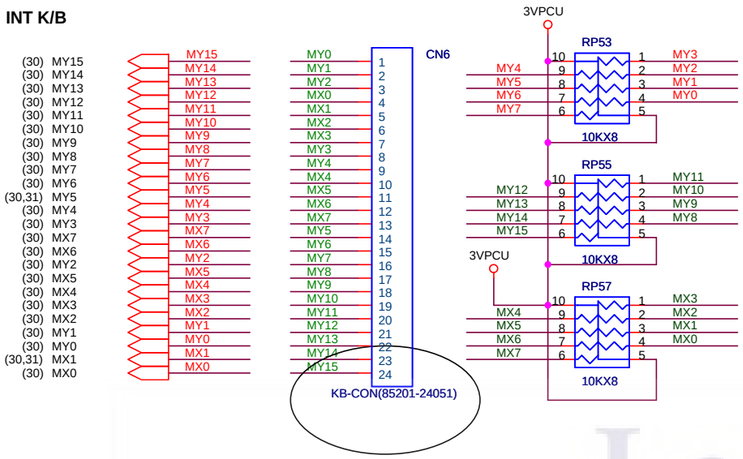
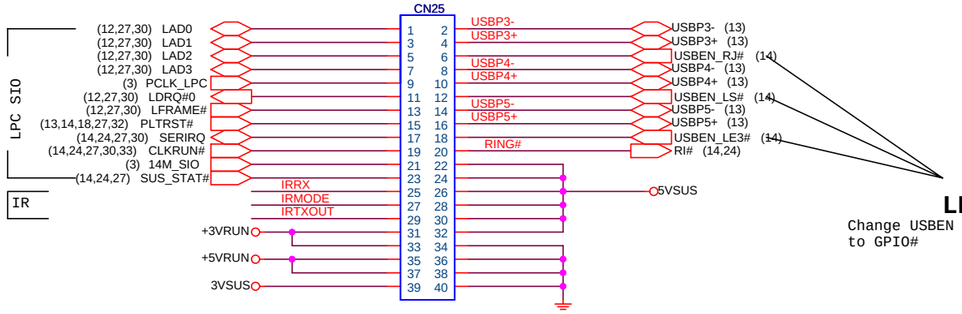
INT K/B



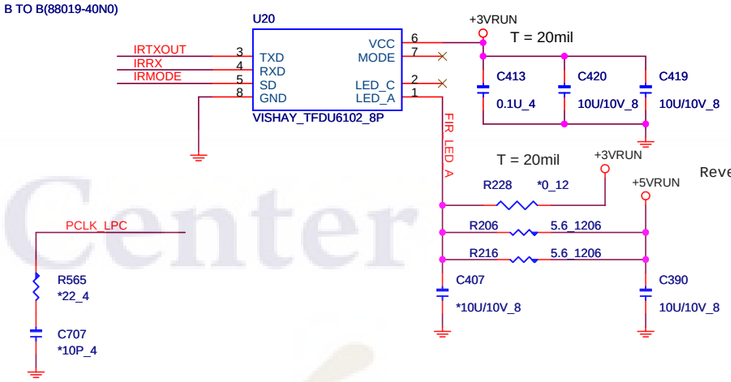
1/27 update keymatrix as same as le1

M/B TO MODEM/B

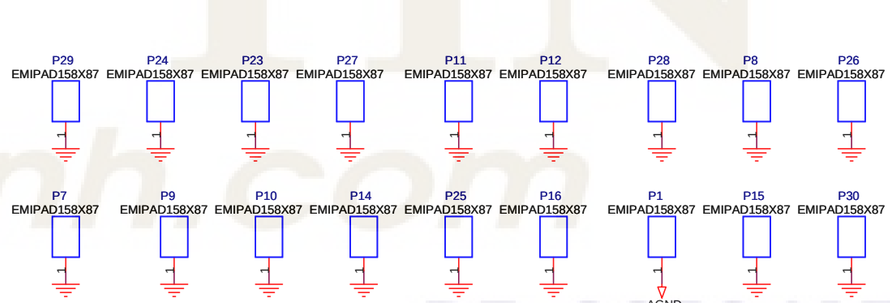


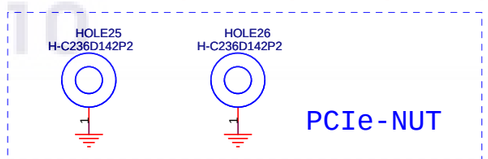
LE4 C:
Change USBEN meaning from OC# to GPIO#

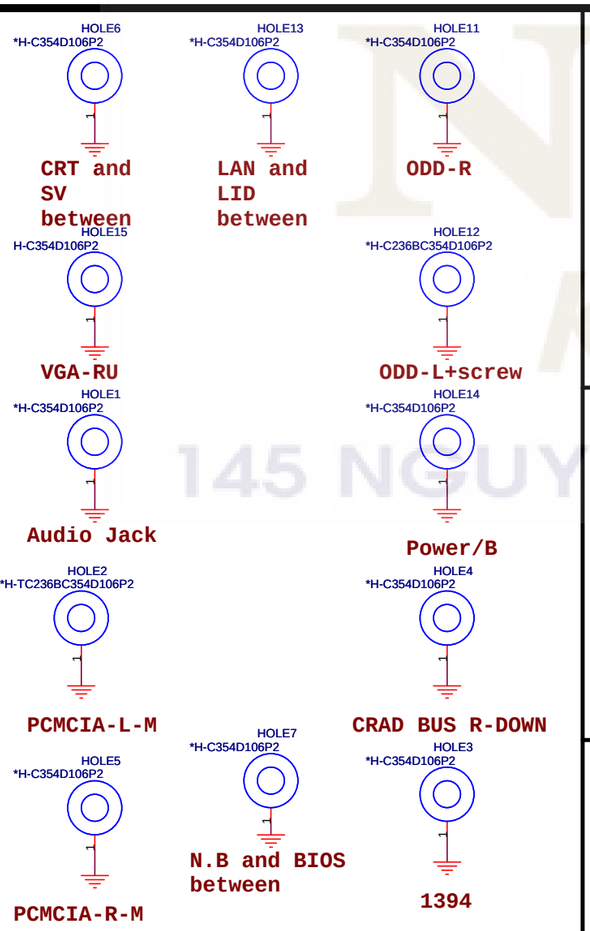
MODEM B TO B(88019-40N0)

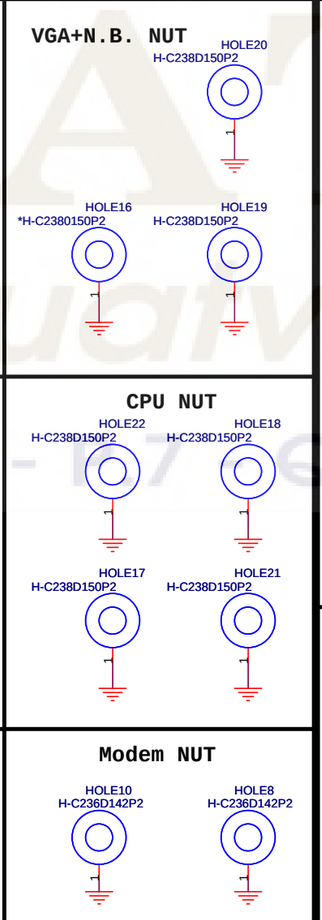


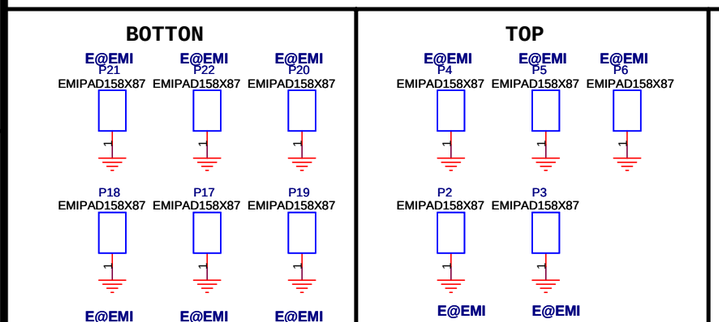
Reverse +3V to FIR LED_A

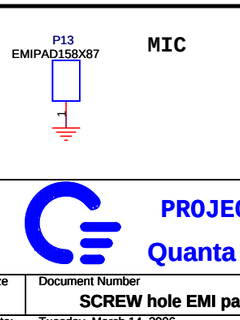












LE4 C:
Arrange modem cable

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	SCREW hole EMI pad	1A
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Need one more wireless LED /mini card on MB ?
currently , No LED here

R306 1 2 0_6
*DLW21HN900SQ2L
(13) USBP1-
(13) USBP1+
CARD_USBP6-
CARD_USBP6+
R303 1 2 0_6
CMLI

LE4 B:
Add debug function

PCI-Express TX and RX direct to connector

0816a

For Debug Only

PCI-E Mini Card

CN22

67910-0002

LE4 A-1108:
+3VSUS change

0816a

LE4 C:
1. Del R298,Q24,R313,R305
2. Add Q36,Q37,R605 for enable wireless led circiut

Q24 *PDTC144EU
Q21 DTC144EUA
Q36 SI2301BDS
Q37 2N7002K

C447 0.1U_4
C444 1U/_P_6
C428 0.1U_4
C348 10U/10V_8
C430 0.01U_4
C456 0.1U_4
C450 10U/10V_8

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Quanta Computer Inc.

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	MIMI PCI e	1A
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LE4 A-1108:

3VSUS

L50 BK2125HS330-T

For associated Line Side Device portion of this design see Conexant RD02-D450 reference schematic

C247 10U/10V_8 C243 0.1U_4 C238 0.1U_4

3V_DVDD

VDDIO is used in determining which HD Audio bus voltage is present on the system. When VDDIO is +1.5V, the device will use 1.5v signaling on the HDA interface pins; when VDDIO is +3.3v, the device will use 3.3v signaling on the HDA interface pins.

L21 *BK2125HS330-T +3VRUN

AVDD

U10 GMT_G910T21U Vout Vin GND +5VRUN

C543 0.1U_4 C230 0.1U_4 C260 0.1U_4 C202 10U/10V_8 C69 1U_4 C75 0.1U_4 C59 10U/10V_8

AGND

U11 CX20549-12

VDDIO DVDD DVDDM AVDD_20 AVDD_31 AVDDHP

(12) ACZ_RST#_AUDIO ACZ_RST#_AUDIO 10 RESET#

(12) BIT_CLK_AUDIO BIT_CLK_AUDIO R104 33_4 BITCLK 5 BIT_CLK

(12) ACZ_SYNC_AUDIO ACZ_SYNC_AUDIO 9 SYNC

(12) ACZ_SDIN0 R99 0_4 SDI 7 SDI

(12) ACZ_SDOUT_AUDIO ACZ_SDOUT_AUDIO 4 SDO

MIC_BIAS_L MIC_BIAS_R MIC_L MIC_R 29 30 21 22 MICBIAS_INT INT_MIC

LINEOUT_L LINEOUT_R 35 36 LINEOUT_L (29) LINEOUT_R (29) Speaker

PORT-A_BIAS_L PORT-A_BIAS_R PORT-A_L PORT-A_R 33 34 38 39 LINEIN_L_1 C263 1U_6 HPOUT_L HPOUT_L (29) LINEIN_R_1 C262 1U_6 HPOUT_R HPOUT_R (29)

(29) DIBP_HS DIBP_HS R122 0_4 DIBP 44 DIBP

(29) DIBN_HS DIBN_HS R123 0_4 DIBN 43 DIBN

Near To Codec

PORT-B_BIAS_L PORT-B_BIAS_R PORT-B_L PORT-B_R 14 15 23 24 EXT_MICBIAS_L EXT_MICBIAS_R EXT_MIC_L EXT_MIC_R MIC IN

BEEP 11 PCBEEP

CD_L CD_GND CD_R 17 18 19 CDAUDL C229 1U/16V_6 CDGND C215 1U/16V_6 CDAUDR C216 1U_6 AGND AVDD

SENSE 13 SENSE R75 5.11K/F_6 SENSE_PORT_A T20 R71 5.11K/F_6 R68 10K/F_4 SENSE_PORT_B R69 39.2K_4 R70 20K_4 SENSE_MIC T19 SENSE_LINEOUT (29)

48 SPDIF

(29) EAPD EAPD 47 EAPD

1 NC_1 2 NC_2 16 NC_16

VREF_HI VREF_LO VC_REFA 26 27 28 VREF_HI VREF_LO VC_REFA C540 1U_4 AGND C541 1U_4

3V_DVDD R403 237K/F_8 RCOSC 41 RCOSC

RC0805

VSSIO_42 VSSIO_46 DVSS 42 46 6

AVSS_12 AVSS_25 AVSS_32 AVSSHP 12 25 32 40

AGND

BIT_CLK_AUDIO ACZ_SYNC_AUDIO ACZ_SDIN0

R399 *22_4

C544 *10P_4 C236 *10P_4 C542 *10P_4

DIGITAL ANALOG

+5VRUN U15 74AHCT1G86GW C201 0.1U/10V_4 0.1U/10V_4 +5VRUN C291 E200505-0166 04/9 5/6 update

(24) PCMSPK (14) ACZ_SPKR (29,30) MUTE# (14) AMP_BEEP R153 *0_4 U14 74AHCT1G08GW PCBEEP R80 10K_4 R84 10K_4 C232 0.47U/10V_6 BEEP

BEEP

MIC

R572 *0_4

LE4 B: add R572

LE4 C: Cancel R572
ADD R80,R84,U15,U14,C301,C291

EXT_MICBIAS_R EXT_MICBIAS_L R77 *10K_4 R76 *10K_4 AVDD AVDD

R64 2.2K_4 R65 2.2K_4

EXT_MIC_R C227 10U_8 EXT_MIC_L C226 10U_8 R_SYS_MIC_1 L1 BK1608LL121_6 SYS_MIC_1 R_SYS_MIC_2 L3 BK1608LL121_6 SYS_MIC_2 SENSE_PORT_B R6 0_6

R63 *1K_4 R66 *1K_4

AGND AGND

C2 100P_4 C5 100P_4

AGND AGND

MIC JACK

CN13

JACK_MIC(010178FR006G101JL)

AGND AGND

Fox : JA6333L-1S0-TR => AC97
JA6333L-3S0-TR => Azalia

LE4 B:

SWAP CN13,CN14
position and Change
Footprint

C: Change to 0_4

R343 0_4

MICGND

CN12 INT_MIC1 R344 0_4 R_INT_MIC L40 BK1608LL121_6 L_INT_MIC

INT_MIC

MICGND

R342 *1K_4 C478 100P_4

MICGND

MICBIAS_INT R394 *10K_4 AVDD

R395 2.2K_4

C539 10U_8 INT_MIC

R390 *1K_4

AGND

LE4 C:
Modidy bias voltage type from C539 before

PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	Azalia Codec / Audio Jack	1A
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0816a

EAPD
low:mute

LE4 C:
slove power on systrm
when the sound had
bob

LE4 C:
Support Vista function

LE4 B: add D17 and R573

AUDIO POWER

LE4 A:
Place near Audio port with CN26

AUDIO POWER

LE4 C:
Del R350

LE4 A:
Place near Audio port with CN14

LE4 C:
Support Vista function

08/04:Change CN5 Left/right pin define and P/N

LE4 A:
Place near audio codec

LE4 B:
Change GND plane from
AUDGND to AGND

LE4 B:
SWAP CN13,CN14
position and Change
Footprint

When Docking insert , disable BTL

GAIN	SPKR MODE	HP MODE
0	10.5	3
1	9	0

Modem connector

2/16 swap audio conn
pin define

Size	Document Number: Audio Amp.		Rev: 1A
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PROJECT : LE4
Quanta Computer Inc.

LDRQ#(pin 8) internal is no use

(12,26,27) LDRQ#0 — LDRQ#0 — R502 *0_6 — DRQ0#

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

0816a: R532 *0_4; R564 RC0805 0_8; L39 FBM2125HM330_8; C661 0.1U/10V_4; C641 0.1U/10V_4; C475 0.1U/10V_4; C446 *0.1U/10V_4; R297 0_4; 551_AVCC

+3VALW_541: C473 10U/10V_8; C455 0.1U/10V_4; C438 0.1U/10V_4; C462 0.1U/10V_4; C637 0.1U/10V_4

U25 AJ875410F34

LE4 B:

Pull high, Add R593, R592

BT1#	R593	4.7K_4
BT4#	R592	4.7K_4
ENV1	R332	10K_4
BADDR0	R331	*10K_4
BADDR1	R330	*10K_4
SHBM	R329	10K_4

BADDR1-0	I/O Address	
	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

LE4 B:

Pull high, add R594, R595

TINT-	R340	4.7K_4
PR_INSERT#	R559	4.7K_4
NBSWON#	R508	4.7K_4
KBSMI#	R503	4.7K_4
PWROK	R514	4.7K_4
BT2#	R594	4.7K_4
BT3#	R595	4.7K_4

C622 0.1U/10V_4; RN5 10KX4 (ABDATA, ABCLK, MBDATA, MBCLK)

LCD_BLON_EC — R274 100K_4

LE4 B: Change BT4# from pin 43 to pin176

LE4 B: pin 24 add 591_PME#

LE4 B: Chnage pin 176 form 551_LPCPD# to BT4#

Power LED controll

LE4 B: pin 175 EC_FPBACK# change to pin 41

LE4 A:

for EC Debug

R549 10K_4; R536 10K_4; BATLED0# R548 *0_4; BATLED1# R535 *0_4

PS/2 to Port Replicator

RN6 10KX4 (MSCLK, MSDATA, KPCLK, KPDATA); R338 10K_4 TPCLK; R333 10K_4 TPDATA

FLASH 8Mbit (1M Byte),NO PLCC TYPE

AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

U42 SST39VF080; R558 100K_4; C693 0.1U/10V_4; C644 0.1U/10V_4; C645 0.047U/10V_4

IOSEL# is NC now

LE4 B:

AKE358AKZ61 IC EEPROM(40P)MX29LV008BTTC-70G(1M*8)LF

AKE358AKZ87 IC EEPROM(40P)MX29LV008CTTC-70G(1M*8)LF

1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
2.SIO has internal 20 mS delay of VCC1_PWROK

Battery LED BLUE and AMBER

U27 *NM24C08

LE4 A:

Change Power plan

R287 *4.7K_4; Q20 PDTC143TT; R273 4.7K_4

LE4 B:

Add R273 in BOM

PROJECT : LE4		
Quanta Computer Inc.		
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	PC87541 & FLASH	1A
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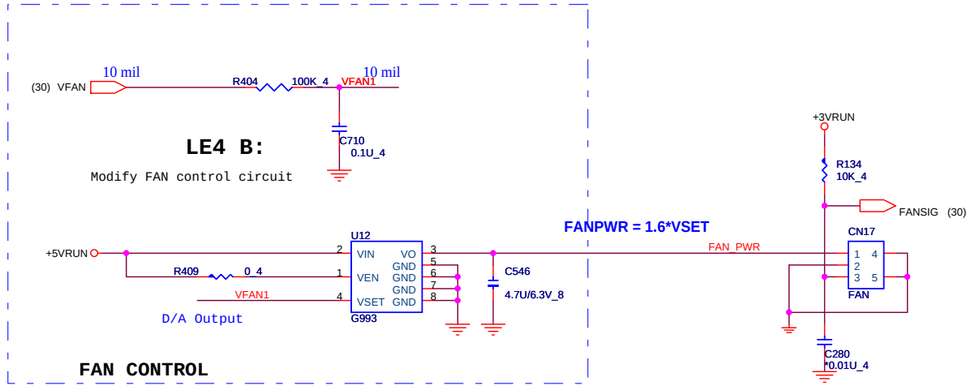

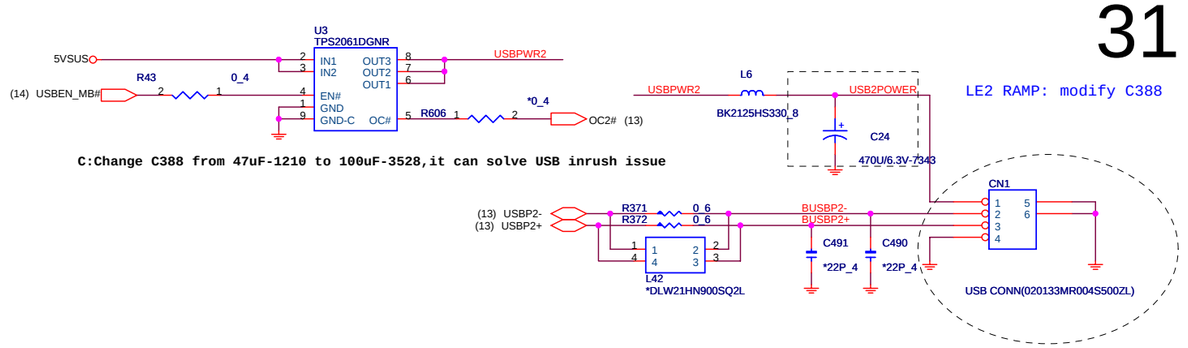

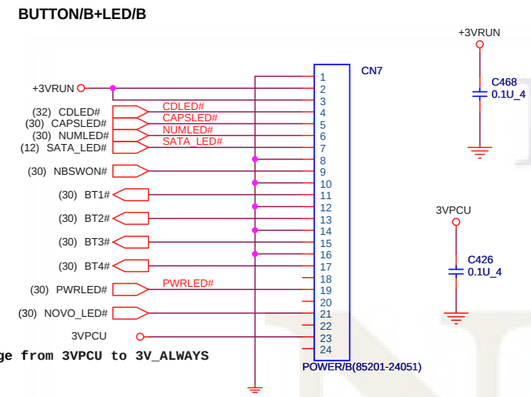

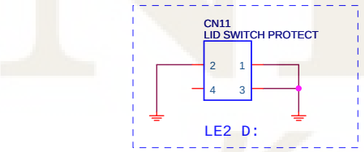

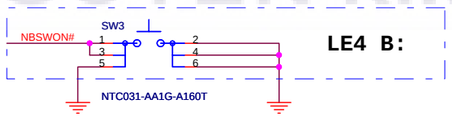

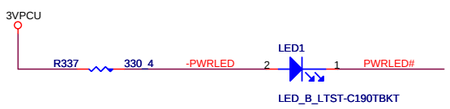

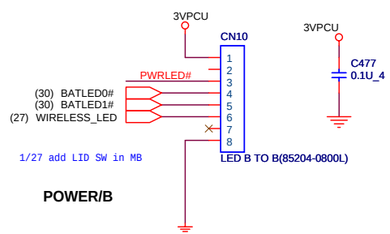

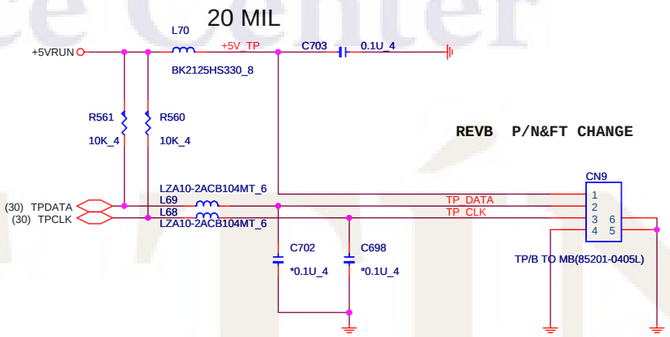

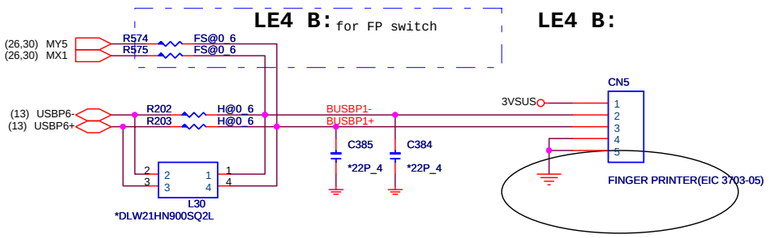

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	USB BT FP TP PB BD FAN	1A
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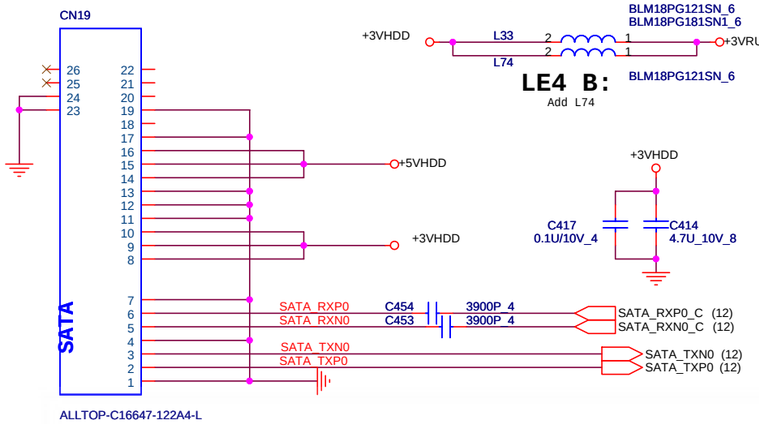
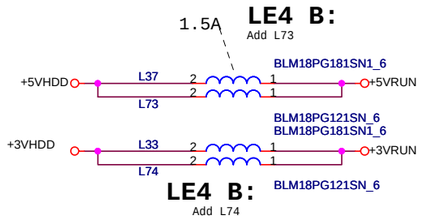
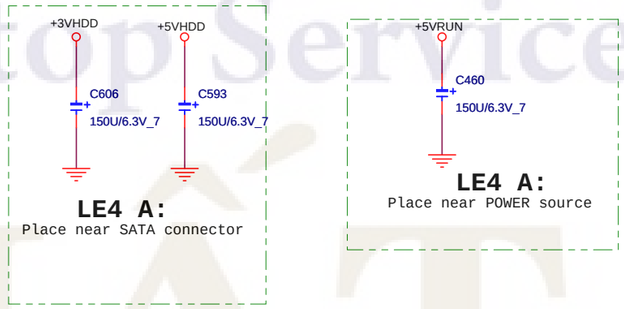
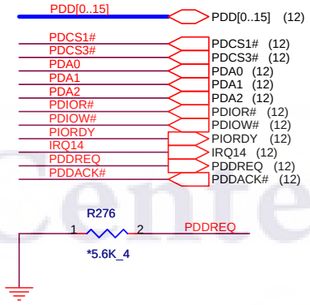
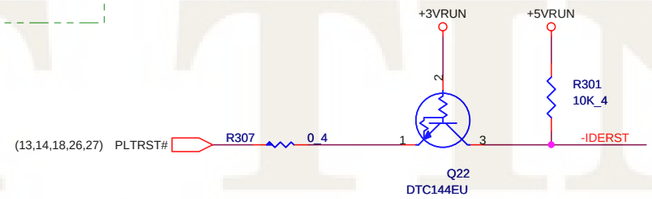
SATA HDD



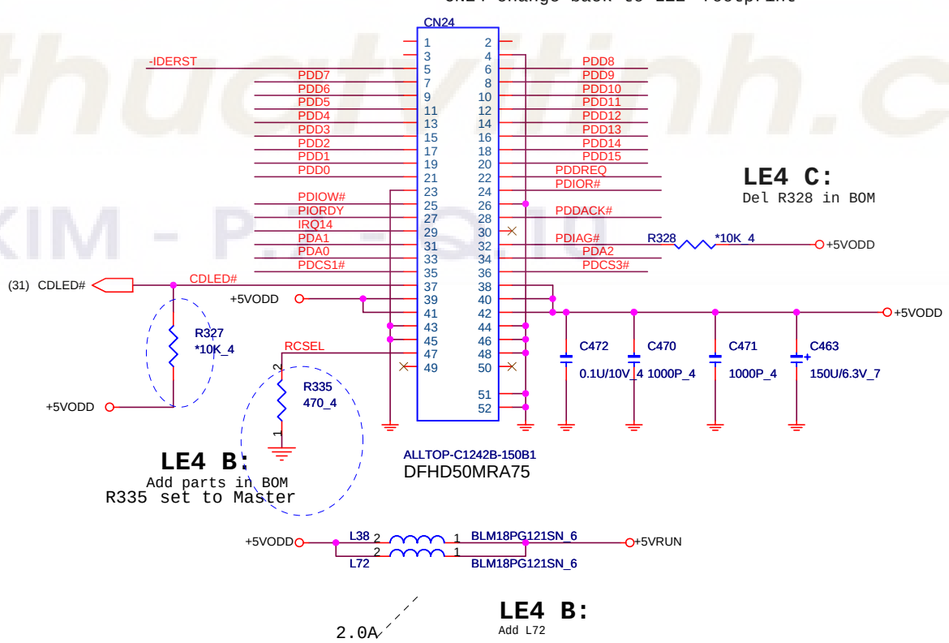








ODD



PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	SATA HDD & PATA ODD	1A
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FOR 10/100
FOR GIGA

+3V_S5 R562 4@0_8
+3VRUN R563 5@0_8

VDDIO_LAN

C706 10U/10V_8 | C686 0.1U_4 | C672 0.1U_4 | C668 0.1U_4 | C696 0.01U/16V_4 | C660 0.01U/16V_4 | C680 0.01U/16V_4 | C654 0.01U/16V_4

+1.8V_1.2V_LAN

U26

Voltage Rail	4401	5702	5705M
VDDIO_PCI	3V_S5	+3V	+3V
+3V_2.5V_LAN	3.3V	2.5V	2.5V
+1.8V_1.2V_LAN	1.8V	1.2V	1.2V

(13,24) AD[31..0] → AD[31..0]

AD0 N7 … AD31 B8

CBE_0# M4 | CBE_1# L3 | CBE_2# F3 | CBE_3# C4

(13,24) C/BE0#
(13,24) C/BE1#
(13,24) C/BE2#
(13,24) C/BE3#

+3V_S5 R321 4.7K_4 → VAUXPRSNT J12

(13) REQ1# → REQ# C3
(13) GNT1# → GNT# J3
(13,24) FRAME# → FRAME# F2
(13,24) IRDY# → IRDY# F1
(13,24) DEVSEL# → DEVSEL# H3
(13,24) STOP# → STOP# H1
(13,24) TRDY# → TRDY# G3
(13,24) PAR → PAR J1
(13,24) PERR# → PERR# J2
(13,24) SERR# → SERR# A2
(13) INTB# → INTA# H2
(13,24,25) PCIRST# → PCI_RST# C2
(3) PCLK_LAN → PCI_CLK A3

LE4 C:
Select enable or disable LAN function

AD23 R523 0_4 → IDSEL A4
(30) LAN_PME# R522 0_4 (13,24) PCI_PME# → LAN_PME# A6

4401,5788 support CLKRUN

(14,24,26,27,30) CLKRUN# R525 0_4 → CSTSCHG C8 / CLKRUN# H4
(3,14) PCLK_SMB R520 *0_4 → SMB_CLK A10
(3,14) PDAT_SMB R521 *0_4 → SMB_DATA C9
R322 5@4.7K_4 → LOW_PWR M11

4401 and 5788M don't support SMBus

M66EN F4

+3V_2.5V_LAN
C685 0.1U_4 | C670 0.1U_4 | C694 0.01U/16V_4
C466 27P_4 | C465 27P_4 | Y6 25MHZ BG625000737 | R319 200_6
CLK_LAN_X1 → XTALVDD J14 / XTALI N11
CLK_LAN_X2 ← XTALO N10

+1.8V_1.2V_LAN L67 BK1608HS330_6 **10mils** LAN_PLLVDD2
C682 0.1U_4 | C683 4.7U/6.3V_8
T264 → NC/PLLVDD3 P7 / PLLVDD2 H14

L8 M9 N8 NC NC NC

@BCM4401/5788

15mm x 15mm
BGA196

BIASVDD A14 ← BIASVDD ← L64 PBY201209T-300Y-S_8 ← +3V_2.5V_LAN
C651 1000P_4
VDDIO A11 F11 K12 L12 ← +3V_S5

VESD1 P1 VESD2 G2 VESD3 A1 ← +3V_S5

NC/VDDP K14 L13 ← +3V_2.5V_LAN
VDDP P11
NC/AVDD A13 ← LAN_AVDD ← L65 BK1608HS330_6 ← +3V_2.5V_LAN
NC/AVDD F14
C652 0.1U_4

EPHY_AVDD/AVDDL F12 EPHY_AVDD/AVDDL F13 ← LAN_AVDDL

NC/TRD[3]- E14 / NC/TRD[3]+ E13 → TX3N / TX3P → TX3N (34) TX3P (34)
NC/TRD[2]- D14 / NC/TRD[2]+ D13 → TX2N / TX2P → TX2N (34) TX2P (34)
RDN/TRD[1]- C14 / RDP/TRD[1]+ C13 → TX1N / TX1P → TX1N (34) TX1P (34)
TDN/TRD[0]- B14 / TDP/TRD[0]+ B13 → TX0N / TX0P → TX0N (34) TX0P (34)

C671 5@0.1U_4 | C665 5@0.1U_4 | C662 0.1U_4 | C659 0.1U_4
R537 5@49.9/F_4 | R534 5@49.9/F_4 | R533 5@49.9/F_4 | R531 5@49.9/F_4 | R530 49.9/F_4 | R529 49.9/F_4 | R527 49.9/F_4 | R526 49.9/F_4

LINK_LED10#/LINKLEDB G13 10MBPS#
LINK_LED100#/SPD100LEDB H13 -100MBPS R538 0_4 → 100MBPS# (34)
COL_LED#/SPD1000LEDB G12 1GBPS#
ACT_LED#/TRAFFICLEDB G14 ACT# → ACT# (34)

ALWAYS USE -100MBPS
1.27Kohm+-1% for 4401
1.24Kohm+-1% for 5788M

RDAC D10 ← LAN_RDAC → R519 5@1.24K/F_4/4@1.27K/F_4

GPIO0 H12
GPIO1 K13 ← EEWP# ← R320 1K_4 ← +3V_S5
GPIO2 J13

SPROM_CLK/EECLK M10 ← EECLK ← R323 5@1K_4
SPROM_CS/EEDATA P10 ← EEDATA ← R324 5@1K_4

SPROMDOUT/NC N9 ← BCM_DI
SPROMDIN/NC P9 → BCM_DO

+3V_S5 → C697 5@0.1U_4
U29: EEWP# EECLK EEDATA; VCC WP# SCL SDA A0 A1 A3 GND; 5@24C128

LAN_AVDDL ← L66 ← +1.8V_1.2V_LAN
C673 0.1U_4 | BK1608HS330_6

U28: EEDATA EECLK BCM_DI BCM_DO; CS SK DI DO VCC NC ORG GND; 4@93LC46
+3V_S5 → C679 4@0.1U_4

TRST# D11 ← BCM_TRST# ← R518 1K_4 ← +3V_S5
TDI D12
TCK C12
TMS A12
TDO B12

Q18 5@BCP69T1 (1G) | C633 10U/10V_8 | C625 0.01U/16V_4

40mils

REGIN33/REGSUP25 B11
NC/REGCTL25 C11
OUT33/REGSEN25 C10

40mils **2.5V@88mA 0.564W**
Q19 5@BCP69T1 (1G)
C634 10U/10V_8 | C626 0.01U/16V_4 | C620 0.01U/16V_4 | C618 0.01U/16V_4 → +3V_2.5V_LAN

NC/REGSUP12 B9
NC/REGCTL12 B10
REGOUT18/REGSEN12 A9

40mils **1.2V@618mA 0.803W**
C635 10U/10V_8 | C621 0.01U_4 | C619 0.01U_4 | C627 0.01U_4 → +1.8V_1.2V_LAN

NC L7 / NC K11 / NC K4 / NC J11 / NC J4 / NC H10 / NC M8 / NC L14 / VSS/NC L11 / VSS/NC H11
NC/CS# E11
EECLK_PXE/SCLK E10
EEDATA_PXE/SI G11
NC/SO

1.5" AWAY_FROM_CHIP
Use Philips BCP69-16, hfe=75~275

VSS B7 D4 D5 D6 D7 D8 D9 NC/VSS E2 E5 E6 E7 E8 E9 F5 F6 F7 F8 F9 F10 G4 G5 G6 G7 G8 G9 G10 H9 K2 L6 L9 M6 M12 M13 N1 N12 N13 ND/VSS

BCM4401 is for 10/100(1.8)
BCM5702 is for giga
BCM5705M is for giga cost-down(12)

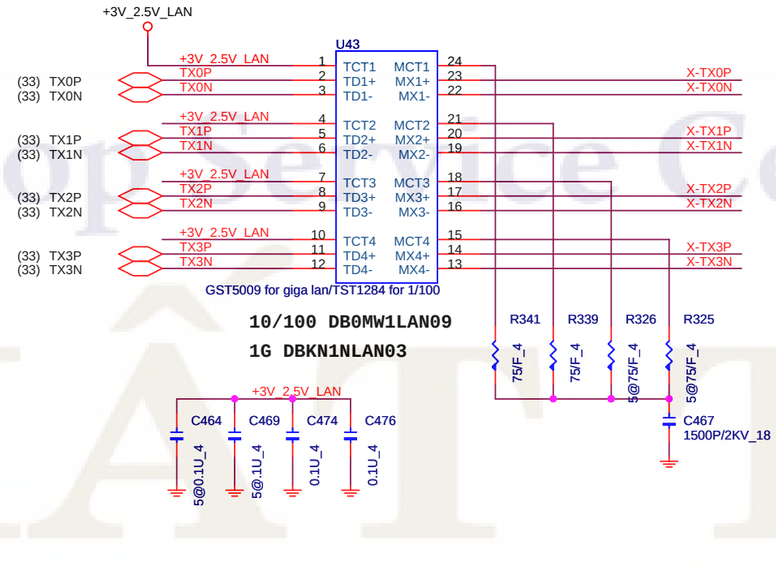
PCLK_LAN → R524 *22_4 | C655 *10P_4

+3V_2.5V_LAN: C704 10U/10V_8 | C691 0.1U_4 | C666 0.1U_4 | C701 0.1U_4
+1.8V_1.2V_LAN: C705 10U/10V_8 | C695 0.1U_4 | C700 0.1U_4 | C699 0.1U_4 | C677 0.01U/16V_4 | C676 0.01U/16V_4 | C678 0.01U/16V_4 | C653 0.01U/16V_4

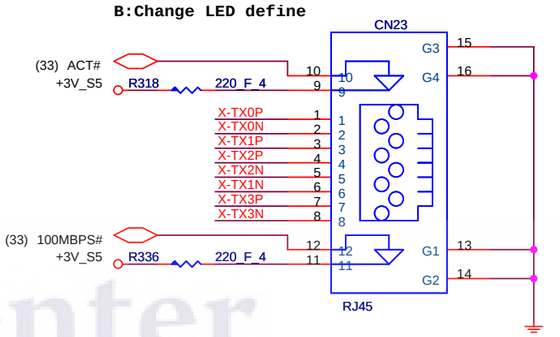
Digitally signed by fdsf
DN: cn=fdsf, o=fdsf, ou=ffsdf, email=fdfsd@fsdff, c=US
Date: 2010.02.13 13:19:59 +07'00'

Title:	BCM4401/5705M LAN	Rev A
Date:	Tuesday, March 14, 2006	Sheet 33 of 42

B:Change 10/100 LAN transform U23 to ST1284A(DB0MW1LAN09)



B:Change LED define



PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	DVO CH7011A & RJ45-11 CON	A
Date: Tuesday, March 14, 2006	Sheet 34 of 42	

LE4 B: add PL27 change PL18 same as PL27

PL27 HI0805R800R-10

PL18 HI0805R800R-10

LE4 C: VA-1

PJ1 2DC-S726B201

PJ1.1

PC168 0.1U_50V_6

PC169 1000P_X7_6

LE4 B: del PL4

PC171 0.1U_50V_6

LE4 B: change size 0805 to 0603

LE4 C: VA-1

PD17 SSM24PT

PD18 SSM24PT

VA

PC173 10U_25V_1206

PR183 0.01

R3

VA2

PL5 FBJ3216HS800-T

VIN

300mil

PR192 10K_F_6

PQ55 DTA124EU

PC88 10U_25V_1206

PC89 0.1U_50V_6

8724_3D3_LDO

PC170 1U_X7_8

LE4 C:

PC167 0.1U_50V_6

PQ56 SI4425BDY-T1-E3

PD16 RB500

PR86 100K_F_6

8724_3D3_LDO

PR87 100K_F_6

CELL-SET

0 = 4 CELL

1 = 3 CELL

LE4 C: VA-1

LE4 B: del PR80

LE4 A:

PR81 75K_6

PR88 825_F_6

PR182

PR90 1.33K_F_6

8724LDO

PR90 33_6

CELL_SET

CELL_SET (30)

PQ35 2N7002K

PC90 0.1U_50V_6

PR94 200K_F_6

PR186 100K_F_6

PQ38 SI4425BDY-T1-E3

PR82 10K_F_6

PC78 0.01U_50V_6

PR84 0_6

PC172 1U_X7_8

PC85 1U_10V_X5_6

PC86 1U_10V_X5_6

PD8 SW1010C

8724DLOV

8724BST

PR91 0_6

PC87 0.1U_50V_6

PQ40 DTA124EU

ACOK

8724LDO

CC-SET_R

8724_3D3_LDO

(30) CC-SET

(30) ACIN

PR96 10K_F_6

PR95 15K_6

PC82 1000P_X7_6

PC80 1000P_X7_6

PC79 0.1U_50V_6

ACOK#

8724DH

8724LX

8724DL

PQ37 SI4914DY-T1-E3

PL6 10uH 30% 4.4A(SIL104R-100PF)L-F

8724LXR

PR97 0.01

V_CHG

V_CHG

PC92 0.1U_50V_6

PC94 10U_25V_1206

PC93 10U_25V_1206

LE4 B: change c from 0.015ohm to 0.01ohm

DCIN CSSP CSSN CELLS LDO DLOV BST DHI LX DLO PGND CSIP CSIN BATT REF CLS GND GND

VCTL ICTL REFIN ACOK ICHG IINP SHDN CCV CCI CCS

PU5 MAX8724

R1

R2

PR85 20K_6

PR89 13.3K_F_6

PC84 1U_10V_X5_6

PC77 0.1U_50V_6

PC81 0.01U_50V_6

PC83 0.01U_50V_6

PR83 1K_6

PR202 *0_6

PR180 100K_F_6

PR181 20K_6

PR179 *0_6

PC91

PQ39 2N7002K

PD9 SW1010C

PR93 1M_F_6

1U_X7_8

ACOK#

3VPCU

LE4 C:

CSIP

CSIN

5VPCU

(12,15,36,38,39,40) 5VPCU

3VPCU

(12,14,15,22,26,30,31,39,40) 3VPCU

VAD-5

PR191 100K_F_6

ACOK

PD19 RB500

PQ61 2N7002K

VIN

(22,36,37,38,39,41) VIN

3VPCU

PD20 SW1010

PR187 475K_F_6

PR190 100K_F_6

ACOK-2

D/C#

D/C# (30)

PQ58 2N7002K

P331

P332

PU9 LMV331

PR188 332K_F_6

PR189 100K_F_6

PQ62 2N7002K

BL/C# (30)

4A

PR195 100K_4

MBATV

MBATV (30)

PL8 HI0805R800R-10

PR193 14K_F_4

PC176 0.01U_25V_4

V_CHG

PF1 TR2/6125FA10A

PL7 HI0805R800R-10

PJ2 SUYIN_200275MR005G118ZL

Iinput =(V CLS / V REF)*(0.075/ RS1)

ICHG =(V ICTL / V REFIN)*(0.075/ RS2)

3VPCU

PR196 330_4

PR197 330_4

PR194

10K_F_4

(5,30) MBCLK

(5,30) MBDATA

(30) TEMP_MBAT

PD22 ZD5.6V

PD21 ZD5.6V

10V

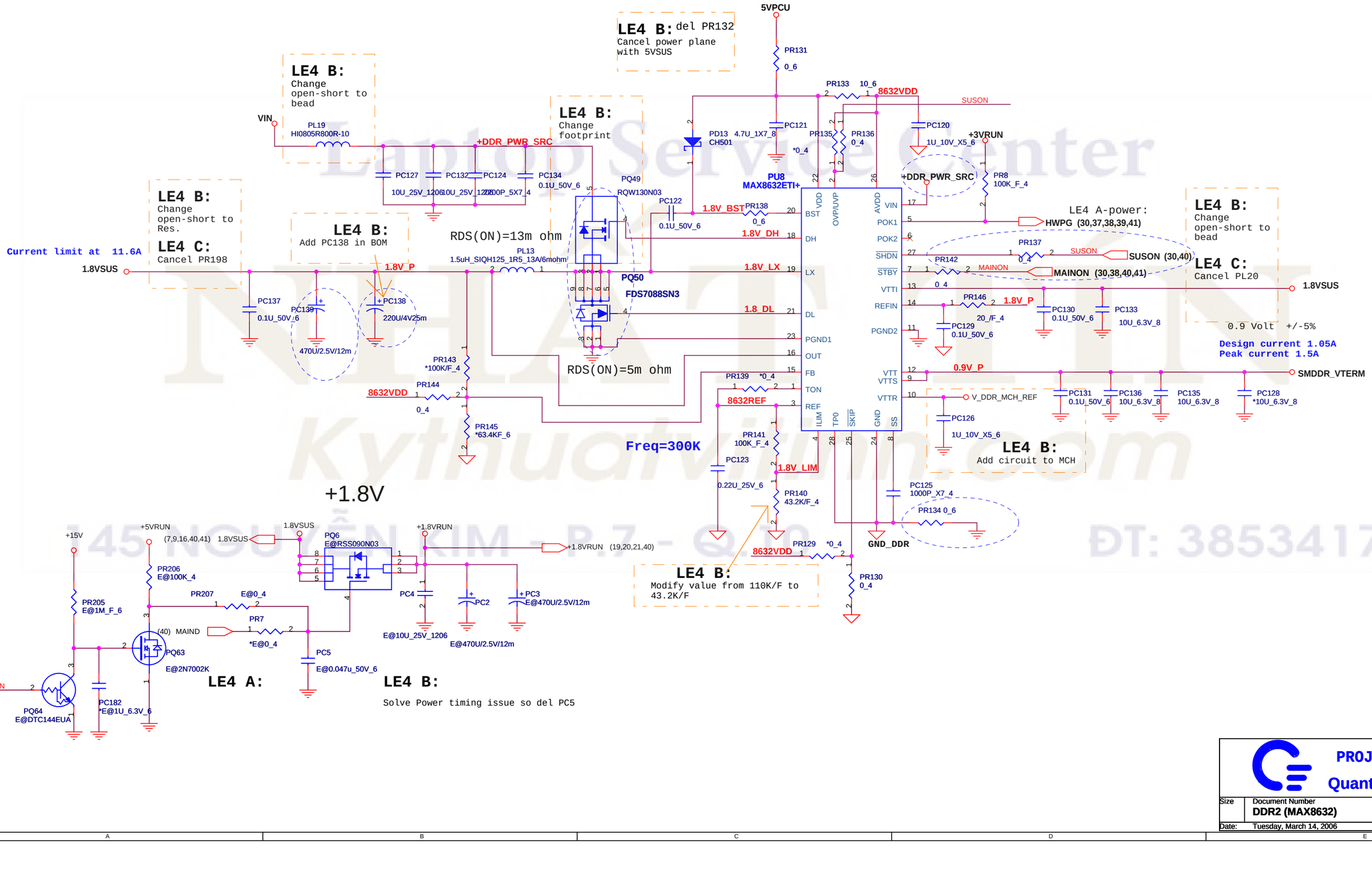
PC177 0.1U_10V_4

LE4 C:

PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	Charger --MAX8724	1A
Date: Tuesday, March 14, 2006	Sheet 35 of 42	



PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 (MAX8632)	1A
Date: Tuesday, March 14, 2006	Sheet 36 of 42	

LE4 B:
Change netname from
VR_PWRGD_CK410# to CLK_EN#

CLK_EN#
PQ34 2N7002K
PR79 1K_F_4
VRON
PR78 *0_4
PC76 0.1U_4
CLKEN

5VSUS
PR33 0_6
LE4 B: change PC68
10u 25V_1206 to 4.7u_0805
8771VDD
PR66 10_4
PC68 4.7U_1X7_8
PD6 SDM10K45-7-F
8771VCC
PC63 2.2U_10V_X5_6
8771BST1
PC67 0.22U_25V_6
+CPU_PWR_SRC
PR70 0_6
PR43 200K_F_4
8771BST1_R
8771LX1
8771DH1
8771DL1

LE4 B:
Change footprint

LE4 B:
del PC165,PC166,PC55

LE4 B:
Change open-short to bead
PL21 HI0805R800R-10
PL22 HI0805R800R-10
VIN
+CPU_PWR_SRC
PC157 100U/25V+
PC53 2200P_5X7_4
PC60 10U_25V_1206 X6S_1206
PC72 10U_25V_1206 X6S_1206

5VSUS
PR36 0_6
PR38 10K_F_4
PR39 1.91K_F_4
PR171 10K_F_4
PR62 *0_6
T272
(7,14) DELAY_VR_PWRGOOD
(3,14) CLK_EN#
CLKEN

PQ33 RQW130N03
PQ32 FDS7088SN3
PQ28 FDS7088SN3
PC58 *1nF_50V_4
*1.5n_50V_6
PC41
PR30 *0_6
PL17 0.45_25A_20%_ETQP4LR45XFC
VCC_CORE
PC12 0.01U_25V_4
PC20 330UF_2V_7mohm
PC143 330UF_2V_7mohm
PC142 330UF_2V_7mohm

PR176 2.1K_F_4
PR177 4.02K_F_4
PR174 NTC 10K_6-B4.25K
8771CSP1
PC163 0.22U_10V_6
PR56 0_4
8771CSN12

distribute evenly between N side and S side, preferably on secondary side.

(5) H_VID0
(5) H_VID1
(5) H_VID2
(5) H_VID3
(5) H_VID4
(5) H_VID5
(5) H_VID6
PR64 PR63 PR58 PR54 PR49 PR47 PR45 0_4
D0 D1 D2 D3 D4 D5 D6

(4) PSI#
PR40 0_4
PSI

(30) VRON
PR173 100K_F_4
(30,36,38,39,41) HWPG
PR172 0_4
(4,12) ICH_DPRSTP#
PR37 0_4
PR44 0_4
(14) PM_DPRSLPVR
SHDN
DPRSTP
DPRSLPVR

LE4 A:

PC161 100P_50V_4
PC49 470P_X7_4
PR42 71.5K_F_4
PC59 0.22U_10V_6
8771REF
CCV
TIME
REF

PR168 10K_F_4
8771VCC
PR169 *NTC 10K_6-B4.25K_6
5VSUS
PR41 56_4
PR167 10K_F_4
PC159 0.1U_10V_4
PR175 0_6
GND EP
THRM
VRHOT
POUT

(4) PH_PROCHOT#

LE4 B:
Change nename

PU3
MAX8771
VCC VDD TON BST1 LX1 DH1 DL1 PGND1 FB CCI GNDS CSP1 CSN12 CSP2 DH2 DL2 LX2 BST2 PGND2
PHASEGD PWRGD CLKEN D0 D1 D2 D3 D4 D5 D6 PSI SHDN DPRSTP DPRSLPVR CCV TIME REF GND EP THRM VRHOT POUT

PR165 *3.48K/F_4
PC158 *4700P_4
PR164 3.48K_F_4
PR166 100_4
PC50 4700P_X7_4
PR46
PC56 470P_X7_4
20K_4
PR170 100_4
PC160 1000P_X7_6
PR48 *100_4
VCCSENSE (5)
8/11 change
VCC_CORE
VSSSENSE (5)
8/11 change
PR53 *100_4

LE4 B:
Enable Value

PR65 0_6
PC65 0.22U_25V_6
PC31 *1nF_50V_4
8771BST2
PD4 SDM10K45-7-F
8771VDD

PQ20 FDS7088SN3
PQ21 FDS7088SN3
*1.5n_50V_6

LE4 B:
Change Footprint
PQ29 RQW130N03

PR28 *0_6
PC40
PL15 0.45_25A_20%_ETQP4LR45XFC

LE4 B: Add PC20 in BOM
LE4 B: Del PC26 parts in BOM
PC141 330UF_2V_7mohm
PC19 330UF_2V_7mohm
PC26 330UF_2V_7mohm
330UF_2V_7mohm_7343
PC140 0.01U_25V_4

PR32 2.1K_F_4
PR34 4.02K_F_4
PR29 NTC 10K_6-B4.25K
8771CSP2
PC47 0.22U_10V_6
PR52
8771CSN12

distribute evenly between N side and S side, preferably on secondary side.

LE4 B:
del PC48

PC57 0.1U_50V_6
PC74 0.1U_50V_6
PC162 100U/25V+
PC75 2200P_5X7_4
PC73 10U_25V_1206 X6S_1206
PC62 10U_25V_1206 X6S_1206

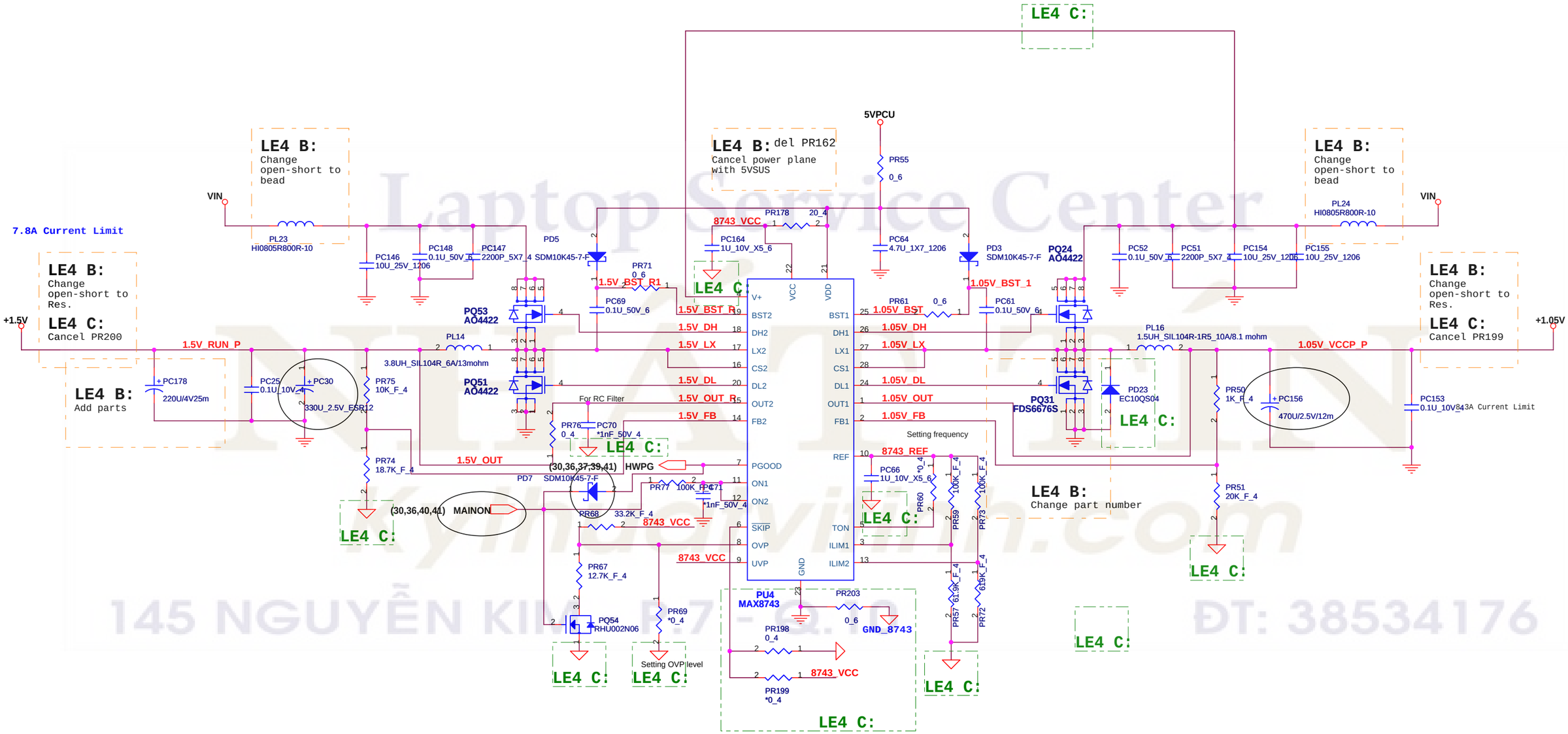
Use differential routing away from switch nodes
8771LX1 and 8771LX2

Add layout note on pins 22 and 28 of MAX8771 controller. These nets have large voltage swings. Need to route them away from the sensitive areas that are trying to detect small changes in voltage, such as the voltage sense VccSense VssSense lines.

Sense lines are 18 mil wide, Z0=27.4 Ohm.
Use differential routing with 7 mil spacing.
Route external layer with solid GND reference (no split planes).
Use 25 mil separation from any other signal.

Use differential routing away from switch nodes
8771LX1 and 8771LX2

PROJECT : LE4		
Quanta Computer Inc.		
Size	Document Number: CPU power MAX8771	Rev: 1A
Date: Tuesday, March 14, 2006	Sheet 37 of 42	



PROJECT : LE4		
Quanta Computer Inc.		
Size	Document Number: VCCP (MAX8743)	Rev: 1A
Date: Tuesday, March 14, 2006	Sheet 38 of 42	

LE4 B:
Change
open-short to
bead

LE4 A-power:

VIN
PL25
HI0805R800R-10
+DC1_PWR_SRC2
PC43
*10U_25V_1206
PC33
0.1U_50V_6
PC34
10U_25V_1206
PC36
0.1U_50V_6
PC32
2200P_5X7_4

8734VCC
PR31
47_6
PC46
1U_10V_X5_6
PD2
CH501
PD1
CH501
5V_AL
PC45
4.7U_1X7_8

Place PC78, PC79 as close as possible to
PQ25 drain and PQ24 source

LE4 A-power:
+DC1_PWR_SRC1
PL26
VIN
PC7 HI0805R800R-10
10U_25V_1206
0.1U_50V_6
PC9
PC8
2200P_5X7_4

BST_3_1
BST_5_1
PQ19
RSS090N03
PQ10
RSS090N03

Place PC81, PC82 as close as possible to
PQ27 drain and PQ26 source

LE4 B:
Change Vaule from 2.5UH
to 3.3UH
IND SMD 3.3UH 30% 6.6A
PL2

LE4 B:
Change Vaule from 2.5UH
to 3.3UH
PL3
IND SMD 3.3UH 30% 6.6A(PLC-1045-3R3)L-F

Current Limit at 6.7A
3VPCU
+3.3V_SUSP
PC14
220U/4V/25m
PC13
0.1U_50V_6
PR153
*0_4
PR152
0_4
PQ15
RSS090N03
PC37
0.1U_50V_6
PR27
0_6
PR22
0_6
PC38
0.1U_50V_6
PQ11
RSS090N03
RDS(ON)=20m ohm

Current Limit at 5.7A
5VPCU
+5V_SUSP
PC16
0.1U_50V_6
PC10
220U/6.3V/ESR25
PR160
*0_4
PR156
0_4

V+ 20
VCC 17
N.C. 1
BST3 28
DH3 26
LX3 27
DL3 24
OUT3 22
FB3 7
ON3 3
ON5 4
LDO3 25
LDO5 18
BST5 14
DH5 16
LX5 15
DL5 19
OUT5 21
FB5 9
PRO 10
ILIM5 11
ILIM3 5
REF 8
TON 13
GND 23
PGOOD 2
SKIP 12
SHDN 6

BST3
DH3
LX3
DL3
FB3
ON5
BST5
DH5
LX5
DL5
FB5
PRO#
ILIM5
ILIM3
8734REF
TON

PU2
MAX8734AEEI+

3V_AL
PC44
4.7U_1X7_8
PC144
1U_10V_X5_6
PR163 0_6
GND_DC/DC
PR18
*100K_F_4
HWPG (30,36,37,38,41)

5V_AL
PR23
2K_F_4
PR21
240K_4
PC35
*1000P_50V_4
PR148
0_4

LE4 A-power:
PR157 200K_4
+DC1_PWR_SRC2
1999_SHDN# (5)
PC145
0.1U_50V_6
PR161
100K_F_4

8734VCC
8734VCC
8734REF
REF=2V
PR159
*0_4
PR158
*0_4
PR147
63.4K_F_4
PR151
63.4K_F_4
ILIM5
ILIM3
PRO#
TON
PR155
0_4
PR154
0_4
PR150
91K_F_4
PR149
63.4K_F_4

LE4 B: add PC150.PC149
Add parts in BOM
Change PC149,PC152 size and Value
from 0603 to 0805 and from 0.1 and
4.7u

DL3
PR162 0_4
PC150
0.01U_50V_6
PC151
0.01U_50V_6
PD14
BAT54S
PD15
BAT54S
+15V
5VPCU
PC180
0.1U_50V_6
PC149
4.7U_1X7_8
PC181
0.1U_50V_6
PC152
4.7U_1X7_8
10V

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	D/D (MAX8734)	1A
Date: Tuesday, March 14, 2006	Sheet 39 of 42	

DISCHARGE

+15V +5VRUN +3VRUN +2_5VRUN +1.8VRUN +VCC_GFX_CORE +1.22V_GFX_PCIE

PR26 1M_F_6 PR16 22_8 PR100 22_8 PR14 22_8 PR6 22_8 PR98 22_8 PR1 22_8

(30,36,38,41) MAINON — MAINON — PQ23 PDTC144EU

PQ17 2N7002K PQ44 2N7002K PQ15 2N7002K PQ5 2N7002K PQ42 2N7002K PQ1 2N7002K

LE4 B:
Change Power plane

LE4 A:

+15V — PR4 1M_F_6 — PQ2 2N7002K — PC1 *2200P_5X7_6

(36) MAIND — MAIND

5VPCU — PQ18 AO4422 — PC23 0.1U_10V_4 10V — PC24 0.1U_10V_4 10V

+5VRUN (4,10,15,23,26,28,29,30,31,32,36)
3A
+5VRUN

3VPCU — PC15 0.1U_10V_4 10V — AO4422 PQ13 — PC17 0.1U_10V_4 10V

+3VRUN (3,5,7,9,10,12,13,14,15,16,17,18,19,20,22,23,26,27,28,30,31,32,33,36,41)
4.5A
+3VRUN

PR3 *1M_6

+15V +1.5V VCC_CORE SMDDR_VTERM +1.05V

PR20 1M_F_6 PR92 22_8 PR13 22_8 PR9 22_8 PR11 22_8

MAINON — PQ52 PDTC144EU

PQ36 2N7002K PQ12 2N7002K PQ7 2N7002K PQ9 2N7002K

LE4 A:
S5_ON a:

LE4 B:
Cancel Circuit

200mils
S0-S5

LE4 A:
modify PQ40

3VPCU — PQ60 SI3456DV — +3V_S5 — 0.5A — +3V_S5 (4,14,15,30,33,34)

PC175 10U_6.3V_8

LE4 B: add PL28

PL28 HI0805R800R-00 — +3VRUN
PL1 HI0805R800R-00 — +5VRUN

PR12 0_4 — VCNTL 2.5VA — PR19 6.34K_F_4 — PR17 20K_F_4

PC29 10U_6.3V_8 — PC11 1U_X5_6

PU1 APL5331
VIN VOUT VCNTL NC VREF NC GND1 AGND GND NC

+2.5VA — PC27 1000P_X7_6 — PC18 10U_6.3V_8 — PC28 10U_6.3V_8

2.5V/ 1A
+2_5VRUN

LE4 A:
S5_ON b:

+15V — PR5 100K_4 — PR99 10K_F_4 — PQ3 FDS6676S

(30) S5_ON — S5_ON — PQ41 RHU002N06

+3V_S5 — PR184 22_8 — PQ59 2N7002K — PC174 0.1U_25V_6

LE4 B:
Change Power plane

3VPCU — PQ14 SI3456DV — PC21 0.1U_10V_4 10V

3VPCU (12,14,15,22,26,30,31,35,39)

3VSUS — 1A — 3VSUS (13,14,24,25,26,27,28,31) — PC22 0.1U_10V_4 10V

5VPCU — PQ26 AO4422 — PC42 0.1U_10V_4 10V

5VPCU (12,15,35,36,38,39)

5VSUS (25,26,31,37,41)
2A
5VSUS

PC54 0.1U_10V_4 10V

LE4 B:
Modify discharge circuit
with +3V_S5

+15V 5VSUS 3VSUS 1.8VSUS +15V

PR25 1M_F_6 PR35 22_8 PR15 22_8 PR10 22_8 PR24 1M_F_6

SUSON_G SUSD

(30,36) SUSON — PQ22 PDTC144EU

PQ30 2N7002K PQ25 2N7002K PQ8 2N7002K PQ27 2N7002K

PC39 *2200P_50V_6

LE4 C:
Change power plane from
10V to +15V

Quanta Computer Inc.	PROJECT : LE4		
Size	Document Number: Discharge Circuit		Rev: 1A
Date: Tuesday, March 14, 2006	Sheet 40 of 42		

LE4 B:
Cancel dot

LE4 B:
Change footprint

LE4 C:
Change enable type from mainon to +3VRUN

Because it had been fist up with +3VRUN to +VCC_GFX_CORE and 1.8VRUN

LE4 A:
V_PWRCNTL:
High(3.3V) = 1.0V
Low(0V) = 1.1V

LE4 C:
Cancel PR201

LE4 C:
Portest diode with ?? reserve.

LE4 C:
Slove +VCC_GFX_CORE of rippe

LE4 B:
Del PR125 in BOM

LE4 B:
Change to LF part number

LE4 A:
Add GND pin

LE4 B:
Modify value from 127K/F to 43.2K/F

LE4 C:
Add +3VRUN and MAINON selector function and fixed circiut for C-test

1.2V/1.0V 12A

250 mils

+VCC_GFX_CORE

VIN

1993_VIN

5VSUS

VGA_CORE

VGA_BST

1993_DH

1993_LX

1993_DL

VGA_CSP

VGA_P_VCC

VGA_REFIN

VGA_P_REF

1993PG

HWPG (30,36,37,38,39)

GFX_CORE_CNTRL(19)

MAINON

+3VRUN

PU6 E@MAX1993ETG

PU7 E@SC4215

EN_4215

1.8VSUS

4215FB

R1

R2

Vo=0.8(R1+R2)/R2

(30,36,38,40) MAINON

1.22V/ 2A

+1.22V_GFX_PCIE

PROJECT : LE4

Quanta Computer Inc.

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MODEL	REV	CHANGE LIST		CW3 M/B	
				FROM	TO
CW3 M/B	1A	**0316~0317**	**1. ADD EMI Solution (Per EMI Team suggestion)**	A1A	

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Quanta Computer Inc.

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	Change History	1A
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