MODEL	REV	CHANGE LIST
MA2A M/B	3A	E200505-0479
	3B	E200505-3796
	3C	E200507-2695

Model / Page	NT2 M/B BOARD FM	NT2 M/B BOARD TO
1	3A	
2	3A	
3	3A	
4	3A	
5	3A	
6	3A	
7	3A	
8	3A	
9	3A	
10	3A	
11	3A	
12	3B	
13	3A	
14	3A	
15	3A	
16	3A	
17	3A	3C
18	3A	3C
19	3A	
20	3A	
21	3A	
22	3A	
23	3A	
24	3A	
25	3A	3C
26	3B	
27	3A	
28	3A	
29	3B	
30	3B	
31	3A	
32	3A	
33	3A	
34	3A	
35	3A	
36	3A	
37	3A	
38	3A	3C
39	3A	

Quanta Computer Inc.	PROJECT:MA2A	PCBA NO.31MA2MB0044	REV:3C	DOC. NO: 204
	APPROVED BY :Ashen	CHECK BY:Bryan Huang	DRAWING BY:Bryan Huang	DATE :08/19/2005 SHEET 1

MA2A SYSTEM BLOCK DIAGRAM

MAX1845 (1.5V & 1.8V) P34

SC1470 (VCCP1.05V) P35

SC1470 (VGA_CORE) P36

MAX1999 (3VPCU & 5VPCU) P37

MAX1907 (CPU_CORE) P38

DISCHARGE P39

X'TAL 14.318M

CK-GEN CK410M +3V ICS954206 P2

Intel Dothan Processor VCC_CORE GMCH_VTT VCCA 478 uFCPGA P3,4

CPU Thermal Sensor +5V P3

FSB 533/400MHz

VIDEO RAM +2.5V P14,15

DDR II SODIMM0

1.8VSUS SMDDR_VTERM

DDR II SODIMM1 P10

Dual Channel DDR

Alviso-PM/GM GMCH 82875GM/GME GMCH_VTT 1.8VSUS +1.5V +2.5V +3V 1257 PCBGA P5,6,7,8,9

PCI-EXPRESS

ATI M22/M24/M26 708 PCBGA VGA_CORE VGA1.2V +1.8V VDD_MEM +2.5V +3V P11,12,13

VIN +5V +3V LCD/INV CONN P16

+5V +2.5V CRT P17

S-VIDEO P17

FOR Alviso-G (LCD/CRT/S-VIDEO)

SATA 0

X'TAL 32.768K

DMI interface

HDD (PATA OR SATA) +5V P22

Master PATA

Slave SATA

ODD BAYVCC P22

USB 2.0

USB Port 0 ~ 3 5VSUS P21

ICH6-M +3V 3VSUS +2.5V +1.5V 1.5VSUS VCCRTC GMCH_VTT 609 BGA P18,19,20

PCI Bus interface

LPC

AC'97

USB 2.0

TO Port Replicator

Line-in

CODEC CONEXANT 20468-31 +5V +3V P23

MODEM DAA CONEXANT +5V +3V 3VSUS 20493-21 P23

WIRE

RJ11 P30

AMP MAX9755 P24

MIC IN JACK P24

HeadPhone P24

INT. SPEAKER P24

Finger Printer 5VSUS P26

X'TAL 32.768K

EC/KBC PC97551 3VPCU +3V VCCRTC P25

BIOS 3VPCU P25

TOUCHPAD 5V P26

Keyboard P26

TYPE III MINI-PCI Socket +3V 3VSUS 5VSUS INTB/C REQ1 GNT1 AD20 P28

X'TAL 24.576M

TI PCI7411 288 PBGA (PCMCIA+1394 +Cardreader) +3V 3VSUS 5VSUS +1.5V INTA/B/C REQ0 GNT0 AD25 P31, 32

IEEE 1394 PORT B

TO Port Replicator

4 in 1 Cardreader Socket P32

CARDBUS Slot P31

IEEE 1394 PORT A

1394 Conn. P33

X'TAL 25M

Marvell 88E8036/88E8053 LAN LANVCC LANVCC18 LANVCC10 INTD REQ2 GNT2 AD16 P29, 30

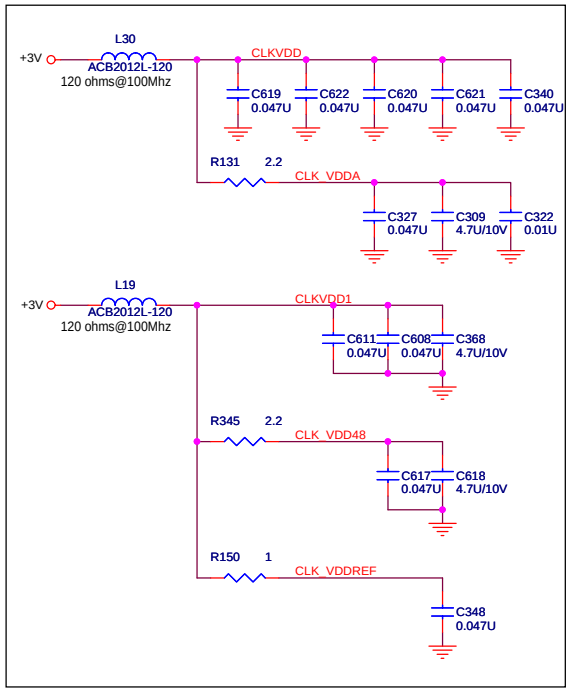
RJ45 P30

PROJECT : MA2A

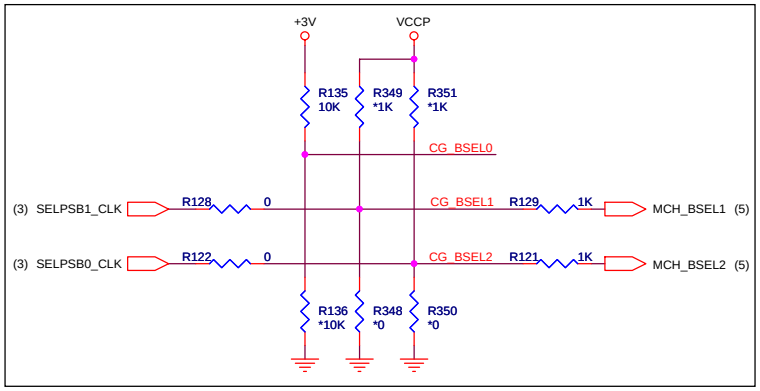
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	3A

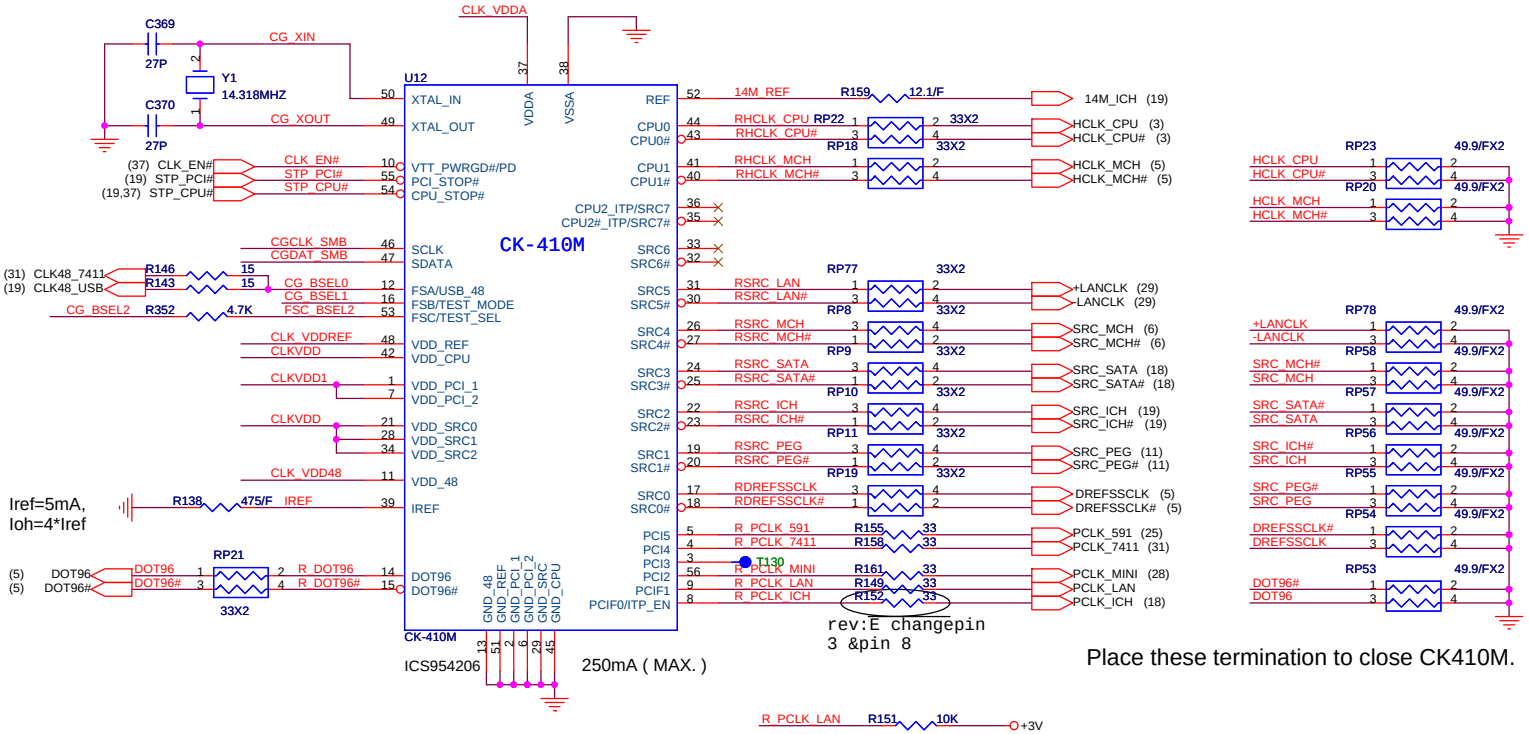
Date: Thursday, March 17, 2005 Sheet 1 of 39



FSC	FSB	FSA	CPU	SRC	PCI	
1	0	1	100	100	33	
0	0	1	133	100	33	Default
0	1	1	166	100	33	
0	1	0	200	100	33	
0	0	0	266	100	33	
1	0	0	333	100	33	
1	1	0	400	100	33	
1	1	1	RESERVED			



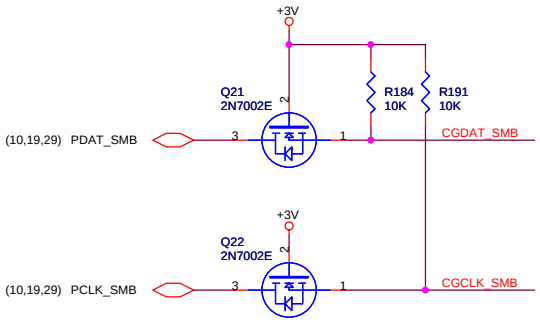
Place these termination to close CK410M.



(3,8,10,11,12,13,16,17,18,19,20,22,25,26,28,34,35,36,37,39) +3V
(3,4,5,6,8,9,18,20,34,39) VCCP

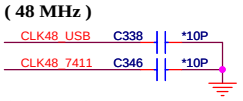
Place these termination to close CK410M.

R_PCLK_LAN R151 10K +3V

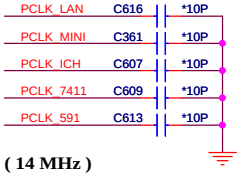


These are for backdrive issue

(48 MHz)



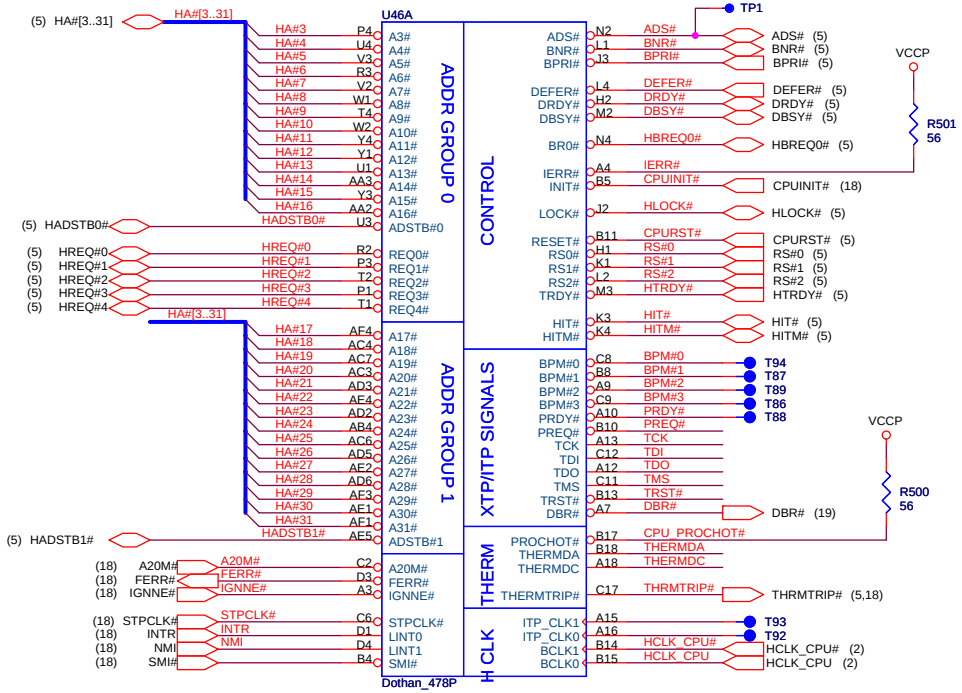
(33 MHz)

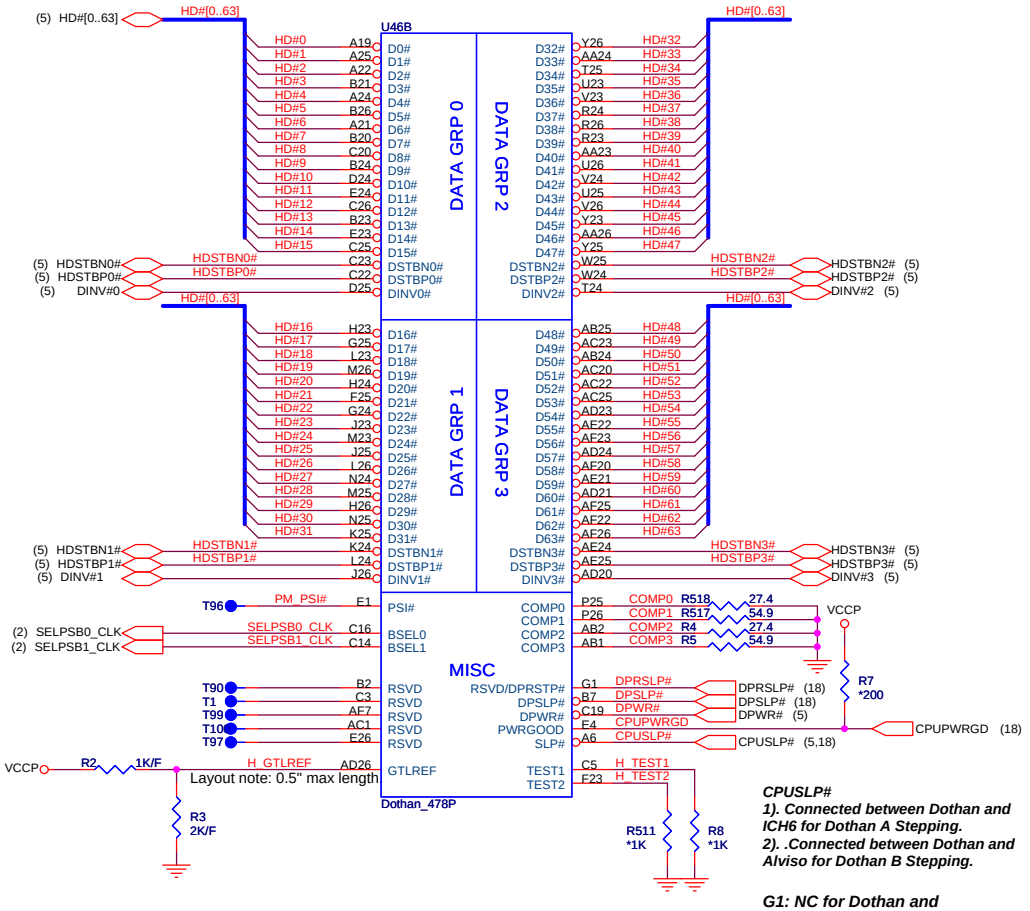


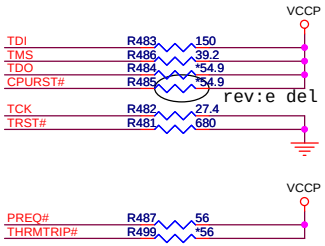
(14 MHz)

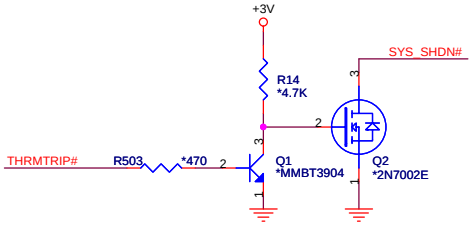
PROJECT : MA2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	3A
Date: Thursday, March 17, 2005	Sheet 2 of 39	

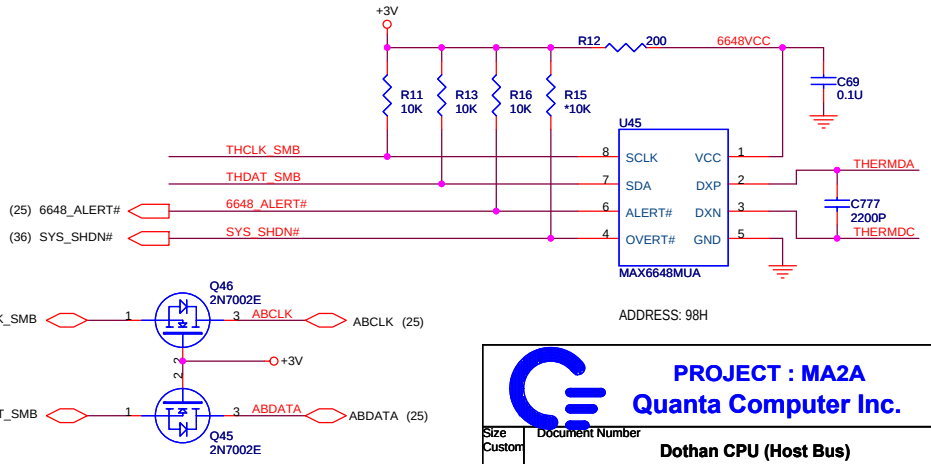






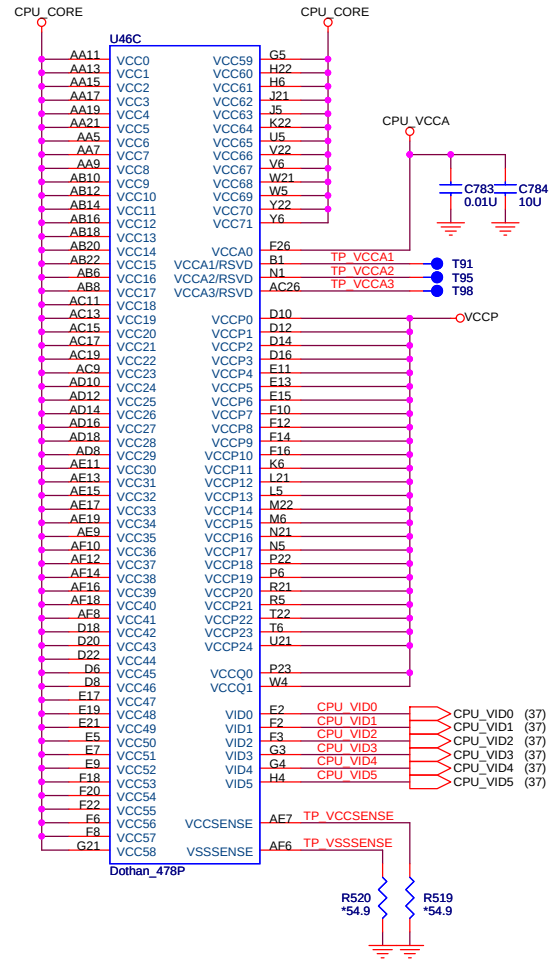


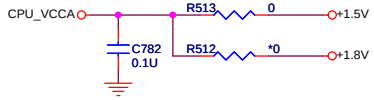
(2,8,10,11,12,13,16,17,18,19,20,22,25,26,28,34,35,36,37,39) +3V
(2,4,5,6,8,9,18,20,34,39) VCCP

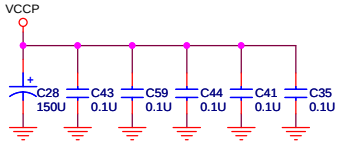


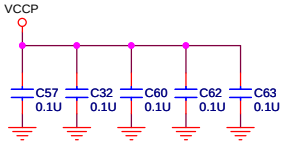
PROJECT : MA2A
Quanta Computer Inc.

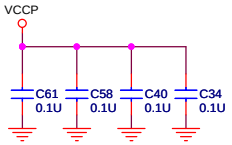
Size	Document Number	Rev
Custom	Dothan CPU (Host Bus)	3A
Date: Thursday, March 17, 2005	Sheet 3 of 39	



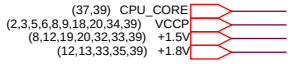


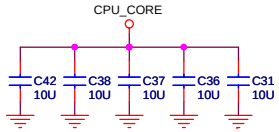


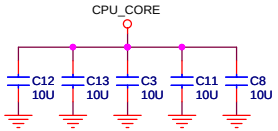


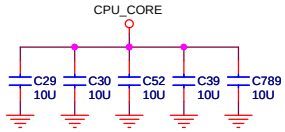


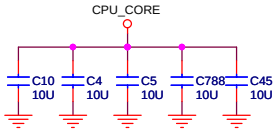
270U/2.0V(CC7343) 12 mΩ * 4
04/13 Intel recommend

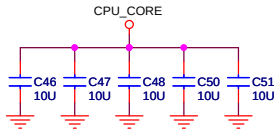


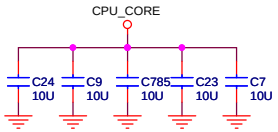


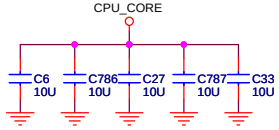






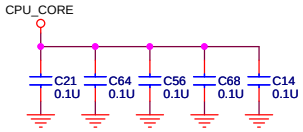


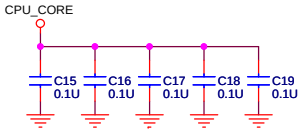


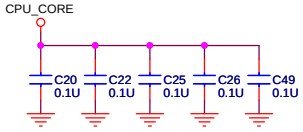


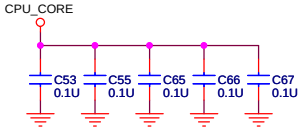
10U/6.3V/X5R(CC0805)
5 mOhm*35

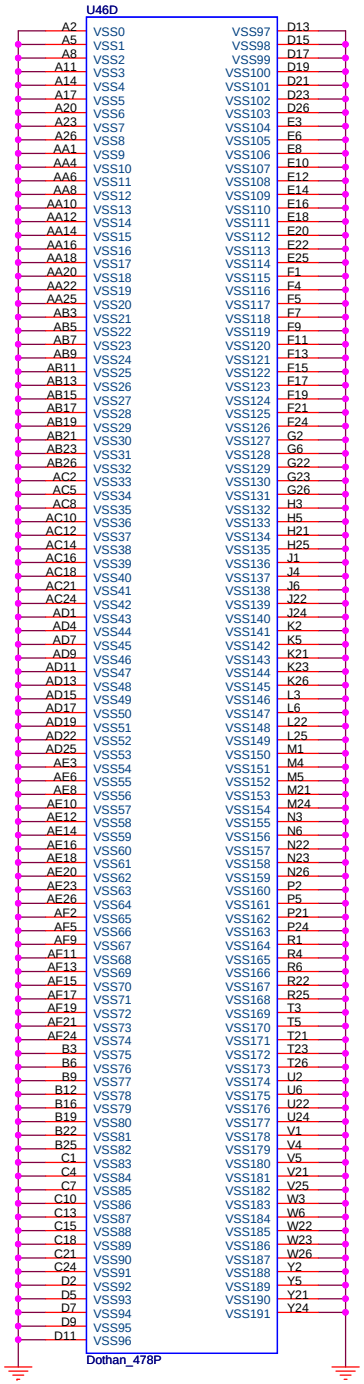
---> 10U/4V/X5R(CC0603)
Murata





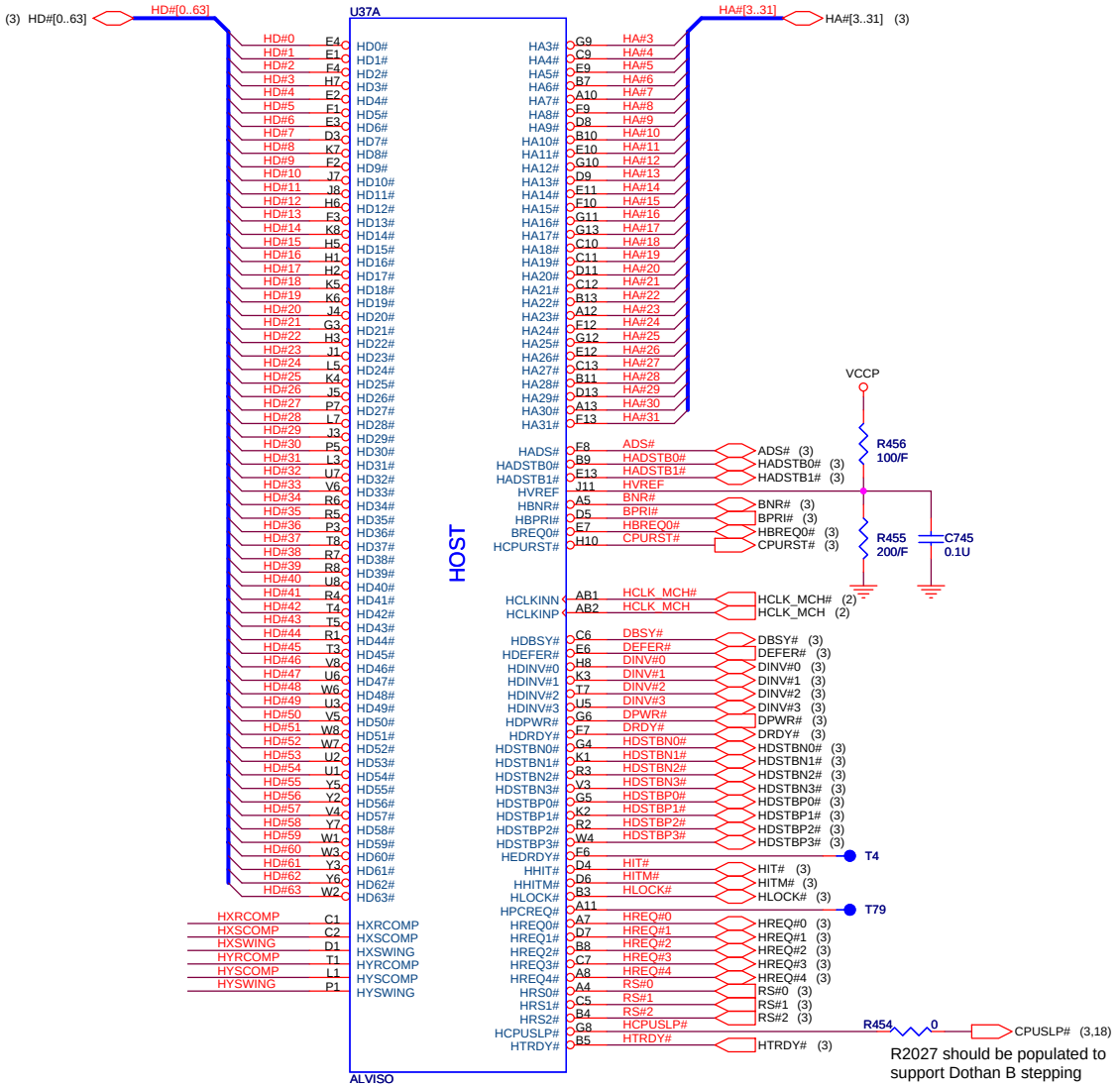


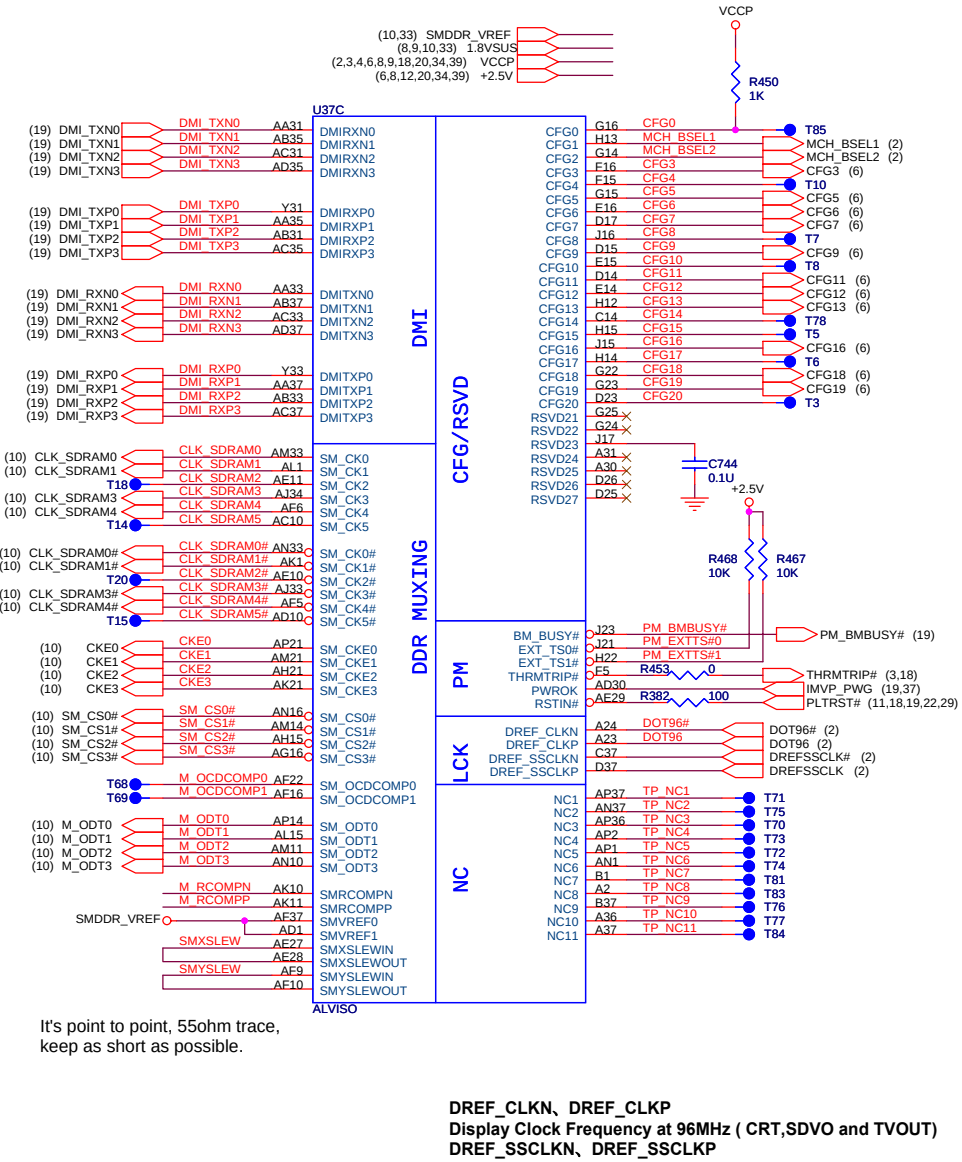


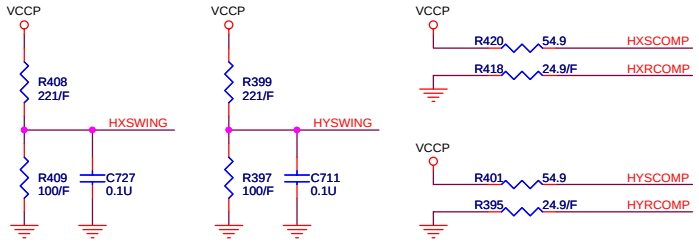


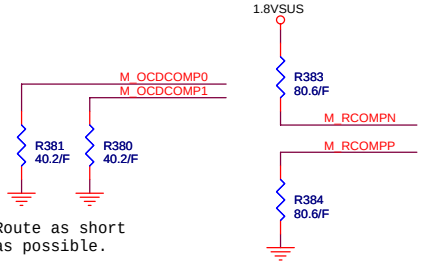
PROJECT : MA2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dothan CPU (Power)	3A
Date: Thursday, March 17, 2005	Sheet 4 of 39	



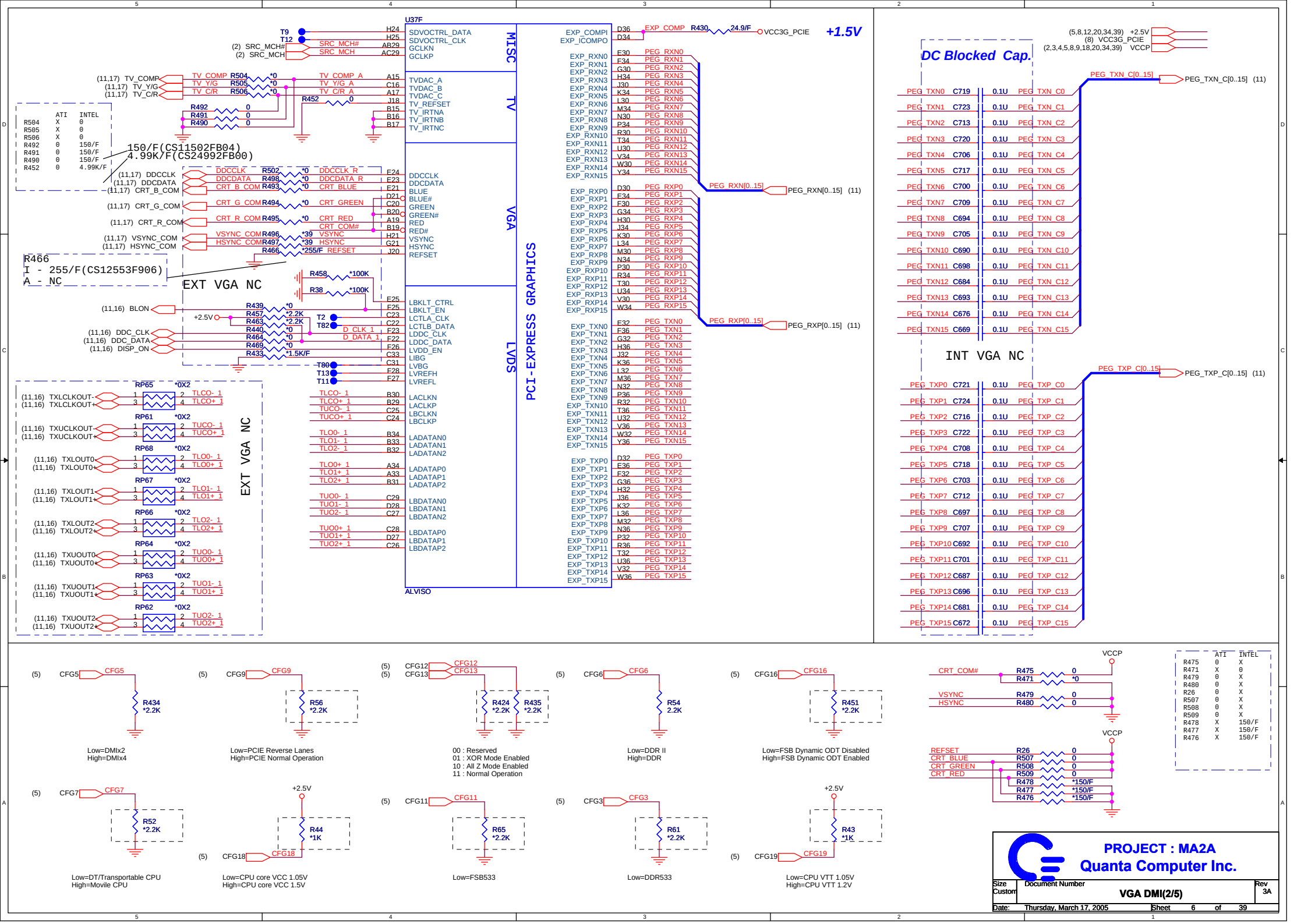


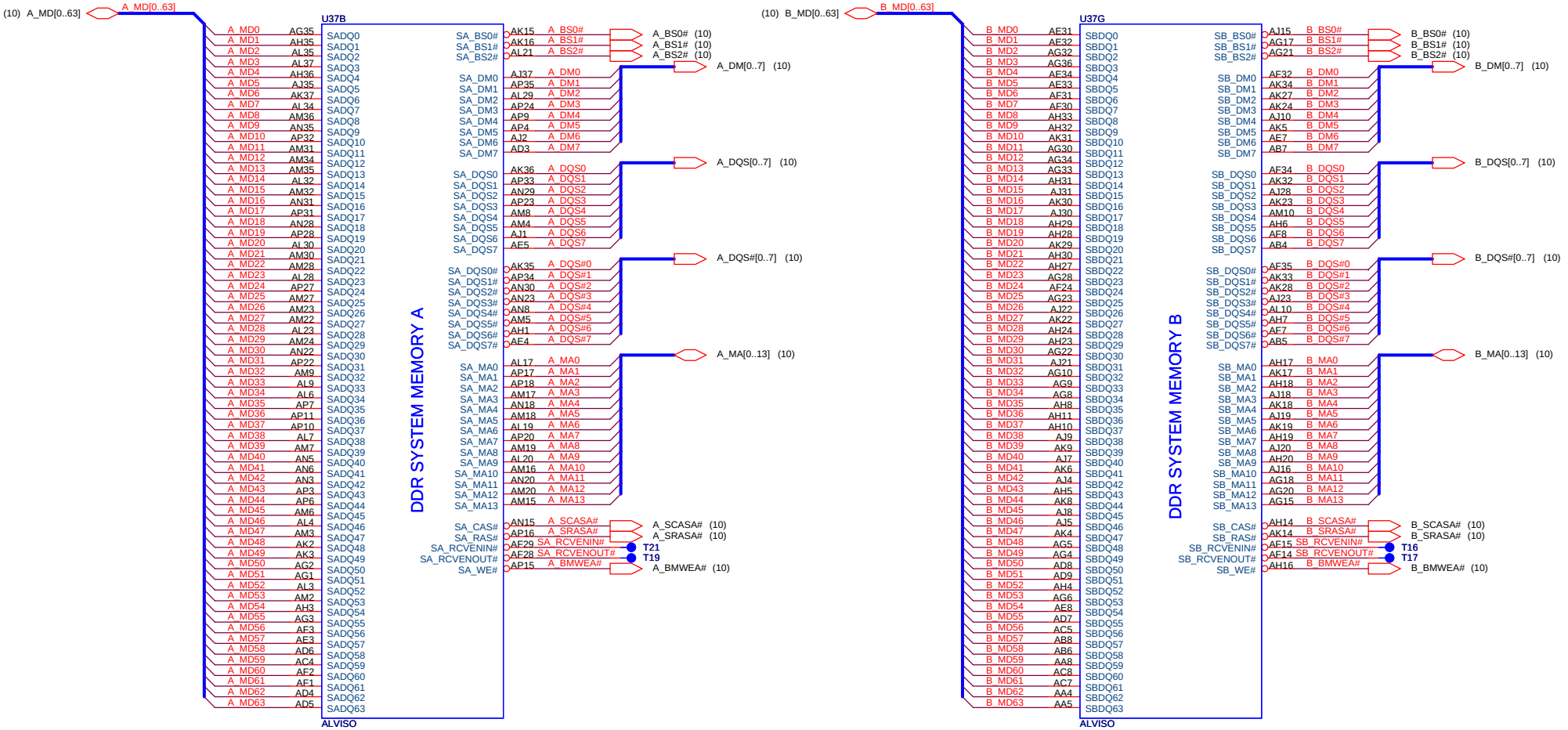




PROJECT : MA2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Alviso Host(1/5)	3A
Date: Thursday, March 17, 2005	Sheet 5 of 39	

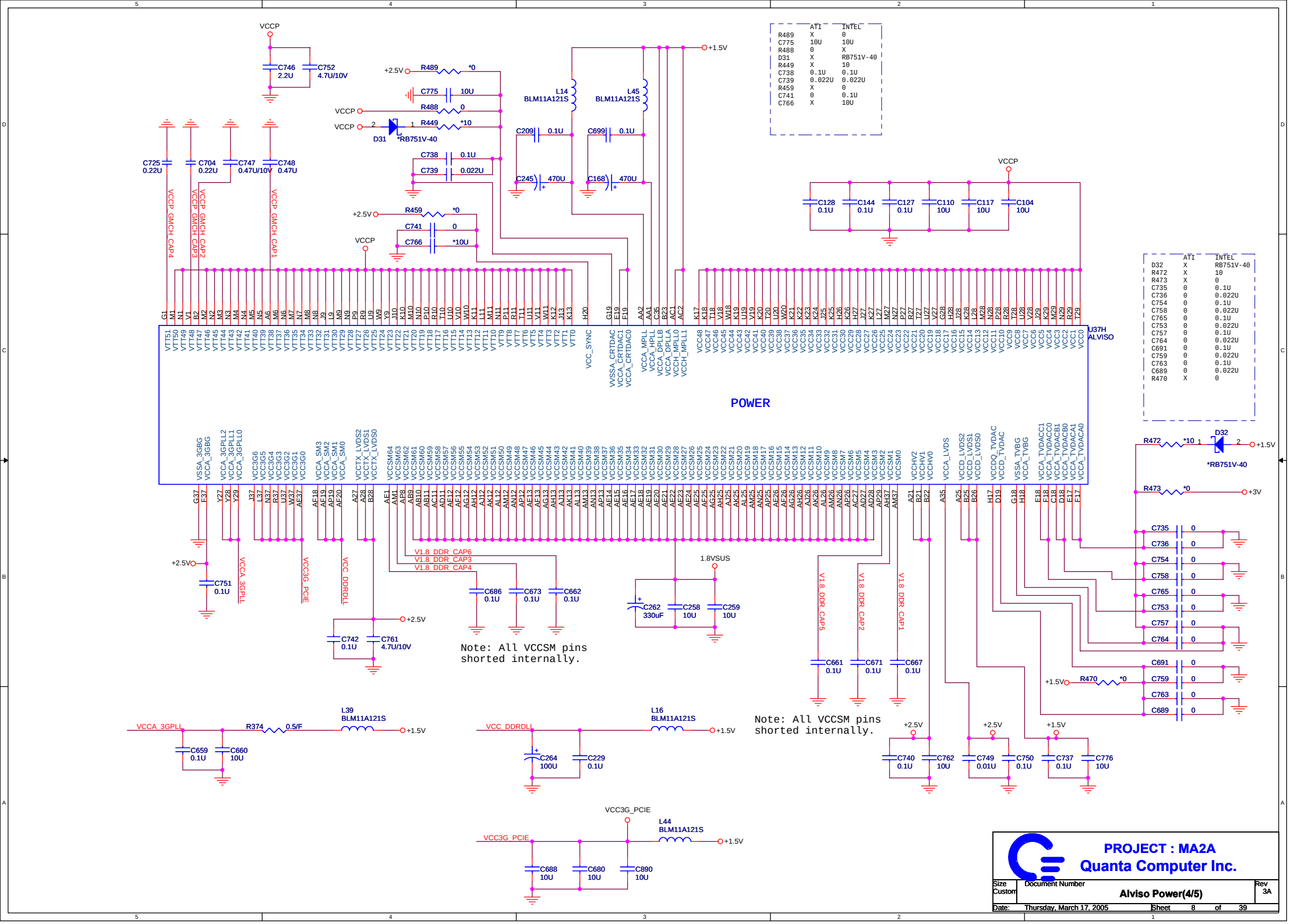

U37F
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
ALVISO
SDVOCTRL_DATA
SDVOCTRL_CLK
GCLKN
GCLKP
TVDAC_A
TVDAC_B
TVDAC_C
TV_REFSET
TV_IRTNA
TV_IRTNB
TV_IRTNC
DDCCLK
DDCDATA
BLUE
BLUE#
GREEN
GREEN#
RED
RED#
VSYNC
HSYNC
REFSET
LBKLT_CTRL
LBKLT_EN
LCTLA_CLK
LCTLB_DATA
LDDC_CLK
LDDC_DATA
LVDD_EN
LIBG
LVBG
LVREFH
LVREFL
LACLKN
LACLKP
LBCLKN
LBCLKP
LADATAN0
LADATAN1
LADATAN2
LADATAP0
LADATAP1
LADATAP2
LBDATAN0
LBDATAN1
LBDATAN2
LBDATAP0
LBDATAP1
LBDATAP2
EXP_COMPI
EXP_ICOMPO
EXP_RXN0
EXP_RXN1
EXP_RXN2
EXP_RXN3
EXP_RXN4
EXP_RXN5
EXP_RXN6
EXP_RXN7
EXP_RXN8
EXP_RXN9
EXP_RXN10
EXP_RXN11
EXP_RXN12
EXP_RXN13
EXP_RXN14
EXP_RXN15
EXP_RXP0
EXP_RXP1
EXP_RXP2
EXP_RXP3
EXP_RXP4
EXP_RXP5
EXP_RXP6
EXP_RXP7
EXP_RXP8
EXP_RXP9
EXP_RXP10
EXP_RXP11
EXP_RXP12
EXP_RXP13
EXP_RXP14
EXP_RXP15
EXP_TXN0
EXP_TXN1
EXP_TXN2
EXP_TXN3
EXP_TXN4
EXP_TXN5
EXP_TXN6
EXP_TXN7
EXP_TXN8
EXP_TXN9
EXP_TXN10
EXP_TXN11
EXP_TXN12
EXP_TXN13
EXP_TXN14
EXP_TXN15
EXP_TXP0
EXP_TXP1
EXP_TXP2
EXP_TXP3
EXP_TXP4
EXP_TXP5
EXP_TXP6
EXP_TXP7
EXP_TXP8
EXP_TXP9
EXP_TXP10
EXP_TXP11
EXP_TXP12
EXP_TXP13
EXP_TXP14
EXP_TXP15
D36
D34
EXP_COMP
R430
24.9/F
VCC3G_PCIE
+1.5V
PEG_RXN[0..15]
PEG_RXP[0..15]
PEG_RXN[0..15] (11)
PEG_RXP[0..15] (11)
PEG_TXN0
PEG_TXN1
PEG_TXN2
PEG_TXN3
PEG_TXN4
PEG_TXN5
PEG_TXN6
PEG_TXN7
PEG_TXN8
PEG_TXN9
PEG_TXN10
PEG_TXN11
PEG_TXN12
PEG_TXN13
PEG_TXN14
PEG_TXN15
PEG_TXP0
PEG_TXP1
PEG_TXP2
PEG_TXP3
PEG_TXP4
PEG_TXP5
PEG_TXP6
PEG_TXP7
PEG_TXP8
PEG_TXP9
PEG_TXP10
PEG_TXP11
PEG_TXP12
PEG_TXP13
PEG_TXP14
PEG_TXP15
(11,17) TV_COMP
(11,17) TV_Y/G
(11,17) TV_C/R
TV_COMP R504 *0 TV_COMP_A A15
TV_Y/G R505 *0 TV_Y/G_A C16
TV_C/R R506 *0 TV_C/R_A A17
R452 0 J18
R492 0 B15
R491 0 B16
R490 0 B17
ATI INTEL
R504 X 0
R505 X 0
R506 X 0
R492 0 150/F
R491 0 150/F
R490 0 150/F
R452 0 4.99K/F
150/F(CS11502FB04)
4.99K/F(CS24992FB00)
(11,17) DDCCLK
(11,17) DDCDATA
(11,17) CRT_B_COM
DDCCLK R502 *0 DDCCLK_R E24
DDCDATA R498 *0 DDCDATA_R E23
CRT_B_COM R493 *0 CRT_BLUE E21
D21
(11,17) CRT_G_COM
CRT_G_COM R494 *0 CRT_GREEN C20
B20
(11,17) CRT_R_COM
CRT_R_COM R495 *0 CRT_RED A19
CRT_COM# B19
(11,17) VSYNC_COM
(11,17) HSYNC_COM
VSYNC_COM R496 *39 VSYNC H21
HSYNC_COM R497 *39 HSYNC G21
R466 *255/F REFSET J20
R466
I - 255/F(CS12553F906)
A - NC
EXT VGA NC
R458 *100K
R38 *100K
(11,16) BLON
+2.5V
R439 *0 E25
R457 *2.2K LBKLT_EN C23
R463 *2.2K LCTLA_CLK C22
R440 *0 LCTLB_DATA F23
R464 *0 LDDC_CLK F22
R469 *0 LDDC_DATA F26
R433 *1.5K/F LVDD_EN C33
LIBG C31
T2 T82 D_CLK_1 D_DATA_1
T80 LVBG F28
T13 LVREFH F27
T11 LVREFL
(11,16) DDC_CLK
(11,16) DDC_DATA
(11,16) DISP_ON
RP65 *0X2
(11,16) TXLCLKOUT-
(11,16) TXLCLKOUT+
TLCO- 1 TLCO+ 1 B30 B29
RP61 *0X2
(11,16) TXUCLKOUT-
(11,16) TXUCLKOUT+
TUCO- 1 TUCO+ 1 C25 C24
RP68 *0X2
(11,16) TXLOUT0-
(11,16) TXLOUT0+
TLO0- 1 TLO0+ 1 B34 A34
RP67 *0X2
(11,16) TXLOUT1-
(11,16) TXLOUT1+
TLO1- 1 TLO1+ 1 B33 A33
RP66 *0X2
(11,16) TXLOUT2-
(11,16) TXLOUT2+
TLO2- 1 TLO2+ 1 B32 B31
RP64 *0X2
(11,16) TXUOUT0-
(11,16) TXUOUT0+
TUO0- 1 TUO0+ 1 C29 C28
RP63 *0X2
(11,16) TXUOUT1-
(11,16) TXUOUT1+
TUO1- 1 TUO1+ 1 D28 D27
RP62 *0X2
(11,16) TXUOUT2-
(11,16) TXUOUT2+
TUO2- 1 TUO2+ 1 C27 C26
EXT VGA NC
(5,8,12,20,34,39) +2.5V
(8) VCC3G_PCIE
(2,3,4,5,8,9,18,20,34,39) VCCP
DC Blocked Cap.
PEG_TXN_C[0..15]
PEG_TXN_C[0..15] (11)
PEG_TXN0 C719 0.1U PEG_TXN_C0
PEG_TXN1 C723 0.1U PEG_TXN_C1
PEG_TXN2 C713 0.1U PEG_TXN_C2
PEG_TXN3 C720 0.1U PEG_TXN_C3
PEG_TXN4 C706 0.1U PEG_TXN_C4
PEG_TXN5 C717 0.1U PEG_TXN_C5
PEG_TXN6 C700 0.1U PEG_TXN_C6
PEG_TXN7 C709 0.1U PEG_TXN_C7
PEG_TXN8 C694 0.1U PEG_TXN_C8
PEG_TXN9 C705 0.1U PEG_TXN_C9
PEG_TXN10 C690 0.1U PEG_TXN_C10
PEG_TXN11 C698 0.1U PEG_TXN_C11
PEG_TXN12 C684 0.1U PEG_TXN_C12
PEG_TXN13 C693 0.1U PEG_TXN_C13
PEG_TXN14 C676 0.1U PEG_TXN_C14
PEG_TXN15 C669 0.1U PEG_TXN_C15
INT VGA NC
PEG_TXP_C[0..15]
PEG_TXP_C[0..15] (11)
PEG_TXP0 C721 0.1U PEG_TXP_C0
PEG_TXP1 C724 0.1U PEG_TXP_C1
PEG_TXP2 C716 0.1U PEG_TXP_C2
PEG_TXP3 C722 0.1U PEG_TXP_C3
PEG_TXP4 C708 0.1U PEG_TXP_C4
PEG_TXP5 C718 0.1U PEG_TXP_C5
PEG_TXP6 C703 0.1U PEG_TXP_C6
PEG_TXP7 C712 0.1U PEG_TXP_C7
PEG_TXP8 C697 0.1U PEG_TXP_C8
PEG_TXP9 C707 0.1U PEG_TXP_C9
PEG_TXP10 C692 0.1U PEG_TXP_C10
PEG_TXP11 C701 0.1U PEG_TXP_C11
PEG_TXP12 C687 0.1U PEG_TXP_C12
PEG_TXP13 C696 0.1U PEG_TXP_C13
PEG_TXP14 C681 0.1U PEG_TXP_C14
PEG_TXP15 C672 0.1U PEG_TXP_C15
(5) CFG5
R434 *2.2K
Low=DMIx2
High=DMIx4
(5) CFG9
R56 *2.2K
Low=PCIE Reverse Lanes
High=PCIE Normal Operation
(5) CFG12
(5) CFG13
R424 *2.2K
R435 *2.2K
00 : Reserved
01 : XOR Mode Enabled
10 : All Z Mode Enabled
11 : Normal Operation
(5) CFG6
R54 2.2K
Low=DDR II
High=DDR
(5) CFG16
R451 *2.2K
Low=FSB Dynamic ODT Disabled
High=FSB Dynamic ODT Enabled
(5) CFG7
R52 *2.2K
Low=DT/Transportable CPU
High=Movile CPU
+2.5V
(5) CFG18
R44 *1K
Low=CPU core VCC 1.05V
High=CPU core VCC 1.5V
(5) CFG11
R65 *2.2K
Low=FSB533
(5) CFG3
R61 *2.2K
Low=DDR533
+2.5V
(5) CFG19
R43 *1K
Low=CPU VTT 1.05V
High=CPU VTT 1.2V
VCCP
CRT_COM# R475 0 R471 *0
VSYNC R479 0
HSYNC R480 0
VCCP
REFSET R26 0
CRT_BLUE R507 0
CRT_GREEN R508 0
CRT_RED R509 0
R478 *150/F
R477 *150/F
R476 *150/F
ATI INTEL
R475 0 X
R471 X 0
R479 0 X
R480 0 X
R26 0 X
R507 0 X
R508 0 X
R509 0 X
R478 X 150/F
R477 X 150/F
R476 X 150/F
PROJECT : MA2A
Quanta Computer Inc.
Size Custom
Document Number
VGA DMI(2/5)
Rev 3A
Date: Thursday, March 17, 2005
Sheet 6 of 39



PROJECT : MA2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ALVISO DDR(3/5)	3A

Date: Thursday, March 17, 2005 Sheet 7 of 39

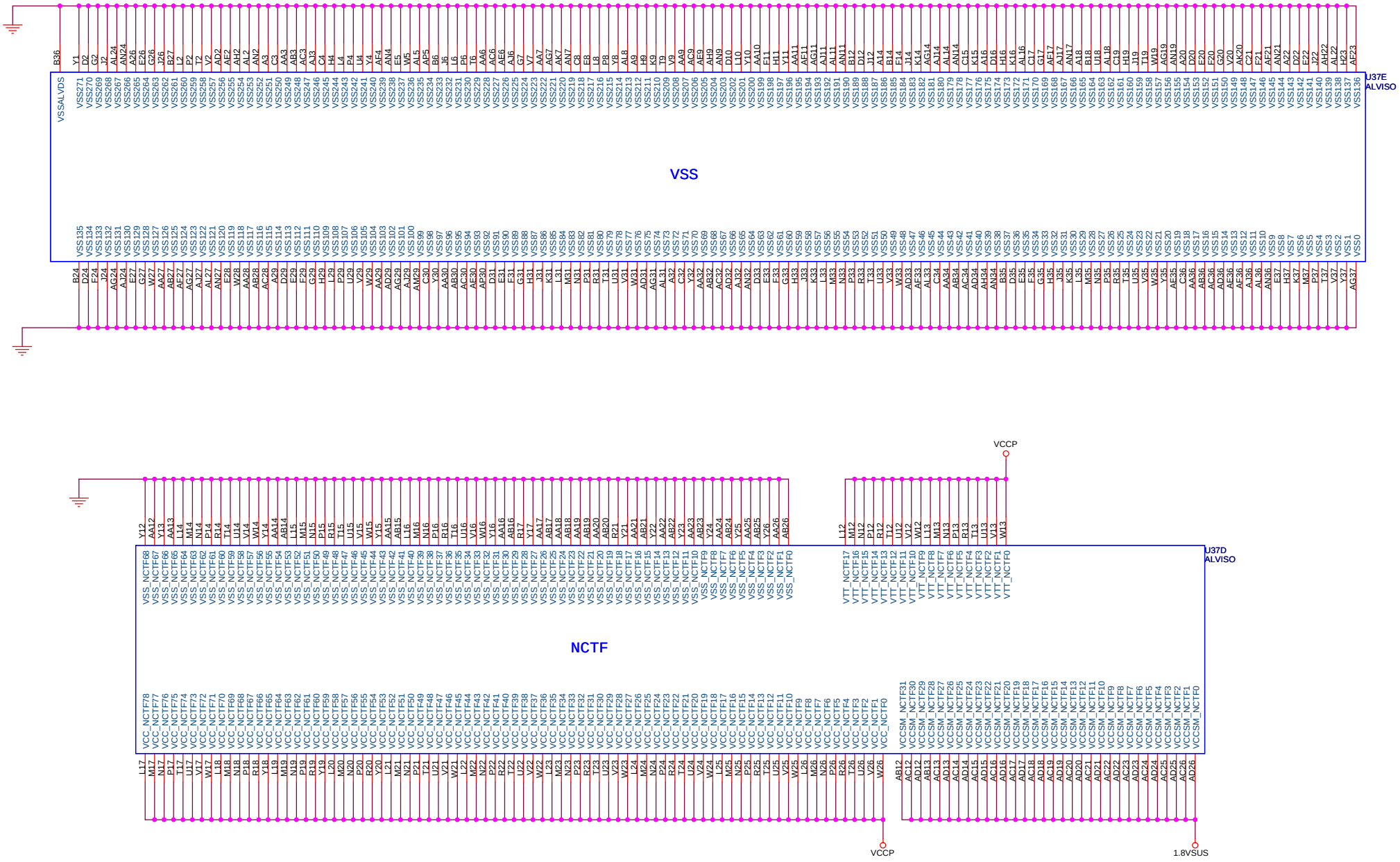


	ATI	INTEL
R489	X	0
C775	10U	10U
R488	0	X
D31	X	RB751V-40
R449	X	10
C738	0.1U	0.1U
C739	0.022U	0.022U
R459	X	0
C741	0	0.1U
C766	X	10U

	ATI	INTEL
D32	X	RB751V-40
R472	X	10
R473	X	0
C735	0	0.1U
C736	0	0.022U
C754	0	0.1U
C758	0	0.022U
C765	0	0.1U
C753	0	0.022U
C757	0	0.1U
C764	0	0.022U
C691	0	0.1U
C759	0	0.022U
C763	0	0.1U
C689	0	0.022U
R470	X	0

PROJECT : MA2A
Quanta Computer Inc.

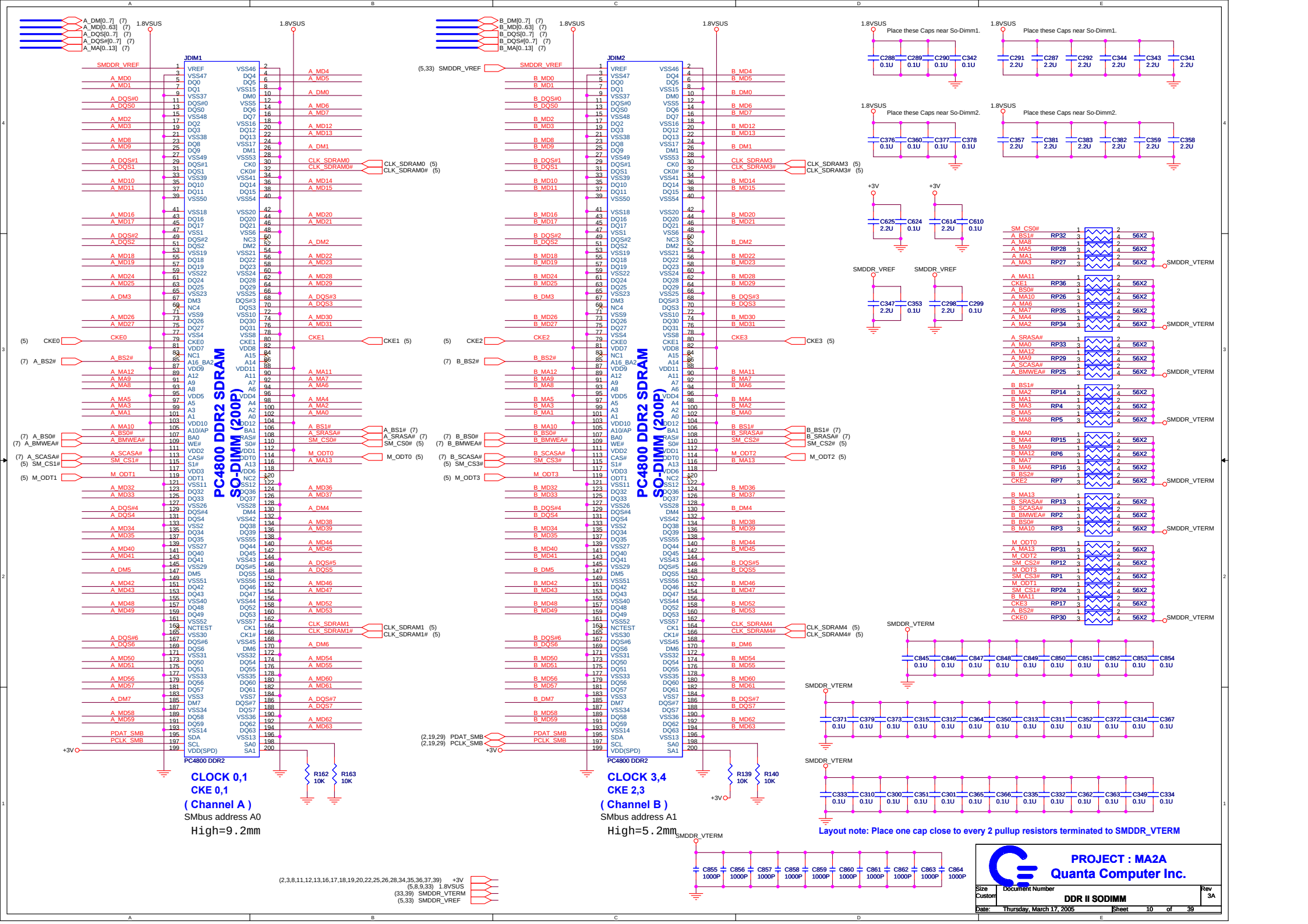
Size	Document Number	Rev
Custom	Alviso Power(4/5)	3A
Date: Thursday, March 17, 2005	Sheet 8 of 39	

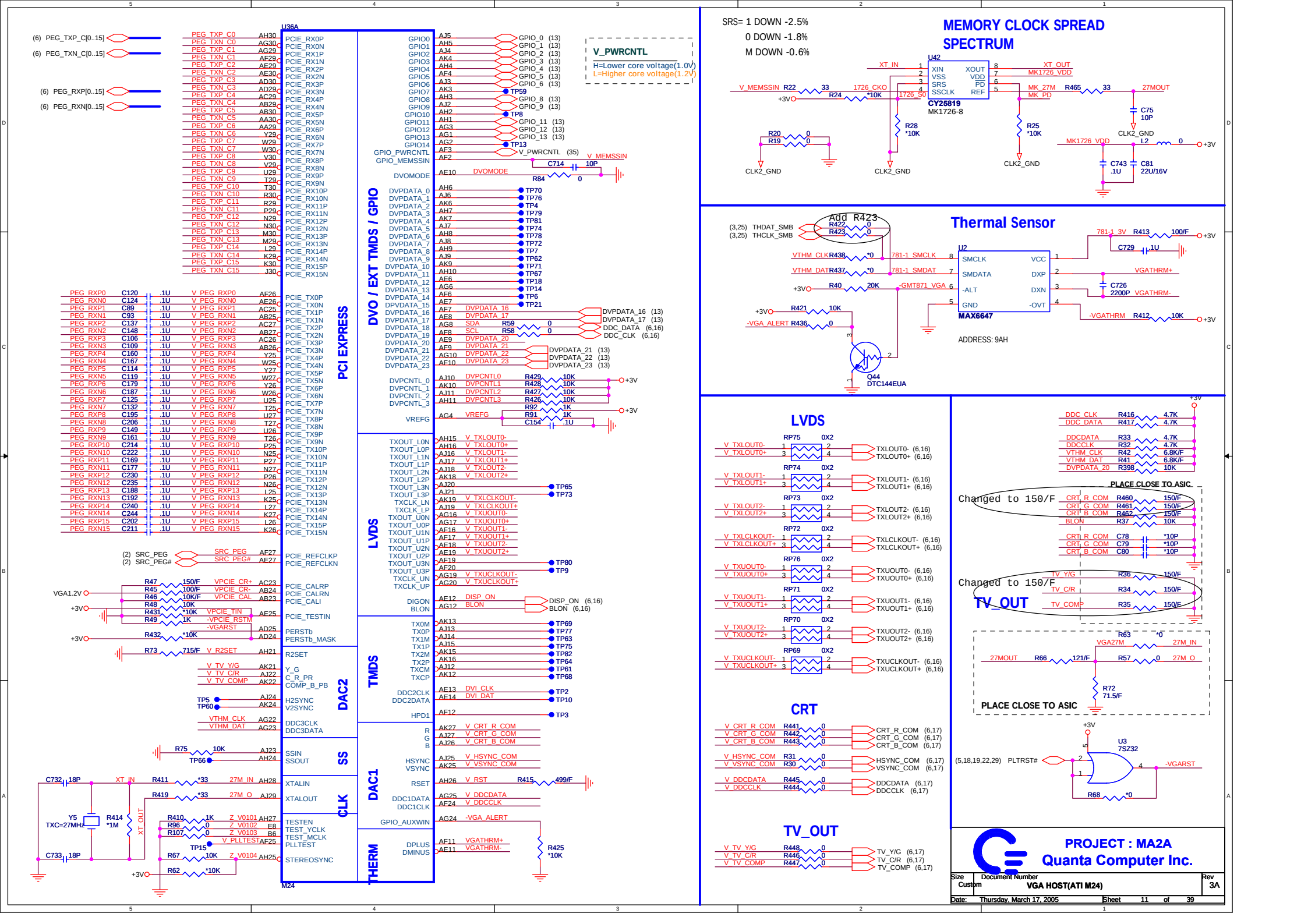


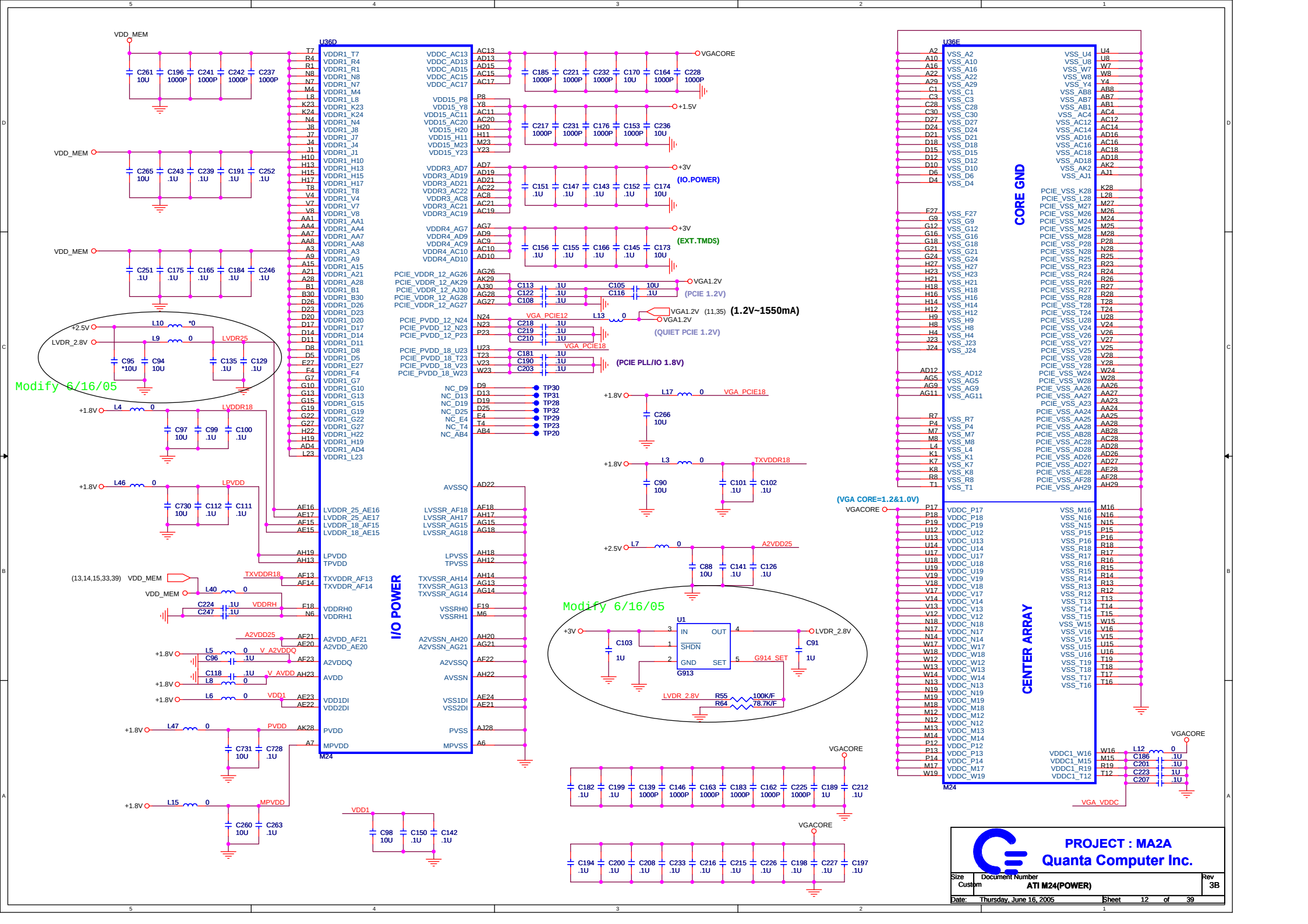
PROJECT : MA2A

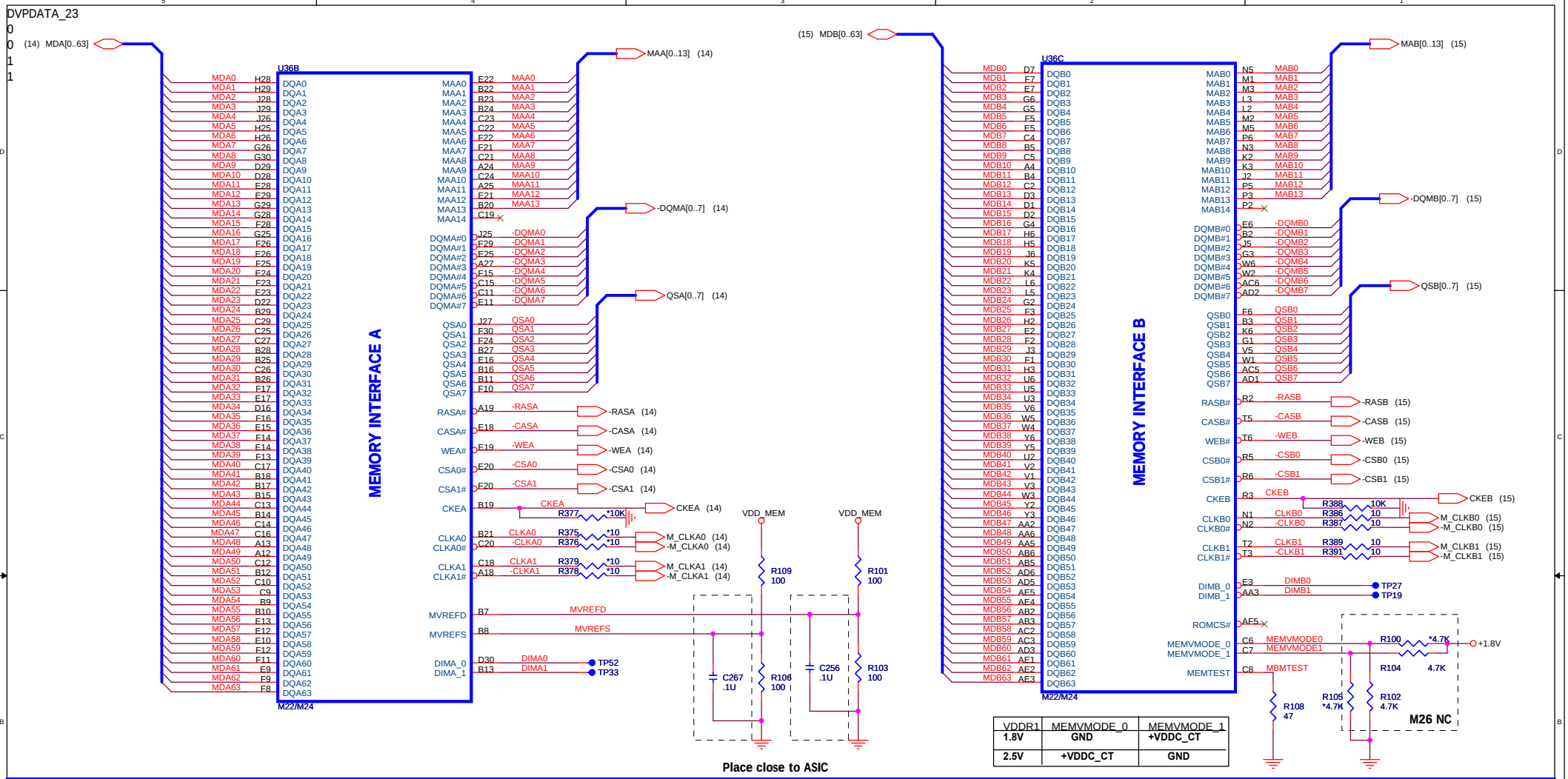
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VSS/NCTF(5/5)	3A
Date: Thursday, March 17, 2005	Sheet 9 of 39	


JDIM1
PC4800 DDR2 SDRAM SO-DIMM (200P)
PC4800 DDR2
CLOCK 0,1
CKE 0,1
(Channel A)
SMbus address A0
High=9.2mm
JDIM2
PC4800 DDR2 SDRAM SO-DIMM (200P)
PC4800 DDR2
CLOCK 3,4
CKE 2,3
(Channel B)
SMbus address A1
High=5.2mm
Place these Caps near So-Dimm1.
Place these Caps near So-Dimm2.
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM
PROJECT : MA2A
Quanta Computer Inc.
DDR II SODIMM
Thursday, March 17, 2005


U36A
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_RX8P
PCIE_RX8N
PCIE_RX9P
PCIE_RX9N
PCIE_RX10P
PCIE_RX10N
PCIE_RX11P
PCIE_RX11N
PCIE_RX12P
PCIE_RX12N
PCIE_RX13P
PCIE_RX13N
PCIE_RX14P
PCIE_RX14N
PCIE_RX15P
PCIE_RX15N
PCI EXPRESS
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
PCIE_TX5N
PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
PCIE_TX8P
PCIE_TX8N
PCIE_TX9P
PCIE_TX9N
PCIE_TX10P
PCIE_TX10N
PCIE_TX11P
PCIE_TX11N
PCIE_TX12P
PCIE_TX12N
PCIE_TX13P
PCIE_TX13N
PCIE_TX14P
PCIE_TX14N
PCIE_TX15P
PCIE_TX15N
PCIE_REFCLKP
PCIE_REFCLKN
PCIE_CALRP
PCIE_CALRN
PCIE_CALI
PCIE_TESTIN
PERSTb
PERSTb_MASK
R2SET
Y_G
C_R_PR
COMP_B_PB
H2SYNC
V2SYNC
DDC3CLK
DDC3DATA
SSIN
SSOUT
XTALIN
XTALOUT
TESTEN
TEST_YCLK
TEST_MCLK
PLLTEST
STEREOSYNC
DAC2
SS
CLK
M24
DVO / EXT TMDS / GPIO
LVDS
TMDS
DAC1
THERM
V_PWRCNTL
H=Lower core voltage(1.0V)
L=Higher core voltage(1.2V)
SRS= 1 DOWN -2.5%
0 DOWN -1.8%
M DOWN -0.6%
MEMORY CLOCK SPREAD SPECTRUM
U42
CY25819
MK1726-8
Thermal Sensor
Add R423
U2
MAX6647
ADDRESS: 9AH
Q44
DTC144EUA
LVDS
CRT
TV_OUT
PLACE CLOSE TO ASIC
Changed to 150/F
PROJECT : MA2A
Quanta Computer Inc.
VGA HOST(ATI M24)
Thursday, March 17, 2005
Sheet 11 of 39


U36D
I/O POWER
M24
U36E
CORE GND
CENTER ARRAY
M24
VDD_MEM
VGACORE
+1.5V
+3V
(IO.POWER)
(EXT.TMDS)
VGA1.2V
(PCIE 1.2V)
(1.2V~1550mA)
(QUIET PCIE 1.2V)
(PCIE PLL/IO 1.8V)
Modify 6/16/05
Modify 6/16/05
(VGA CORE=1.2&1.0V)
PROJECT : MA2A
Quanta Computer Inc.
ATI M24(POWER)
Thursday, June 16, 2005



VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND

STRAPS PIN

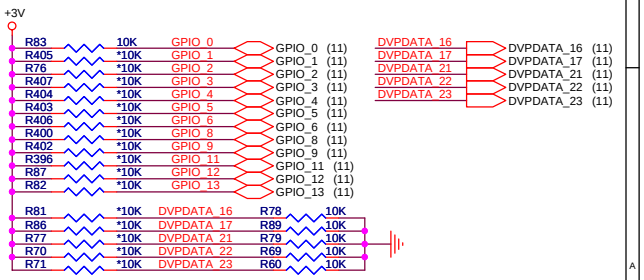
GPIO_0	PCI-Express Current Calibration Bandgap Backup
	0: use reference voltage from Bandgap
	1: use reference voltage from resistor divider
GPIO_1	PCI-Express PLL Calibration force enable
	0: Disable PLL force calibration
	1: Enable PLL force calibration
GPIO_(3,2)	**00: PCI Express 1.0 mode**
	01: RESERVED
	10: PCI Express 1.0 mode
	11: RESERVED
GPIO_4	Turn off PCI-Express impedance / strength calibration
	0: enable
	1: disable
GPIO_5	Bypass PCI-Express PLL
GPIO_6	PCI-Express transmitter current compensation
	0: Normal
	1: Inject extra current for output buffer switching

STRAPS PIN

GPIO_8	Strap to set the debug muxes to bting out DEBUG signals even if registers are inaccessible
GPIO(9,13:11) INT P/D	ROMIDCFG
	0x0x: No ROM, CHG_ID=0
	0x1x: No Rom, CHG_ID=1
	1000: Parallel ROM, Chip ID'S from ROM
	1000: Parallel ROM, Chip ID'S from ROM

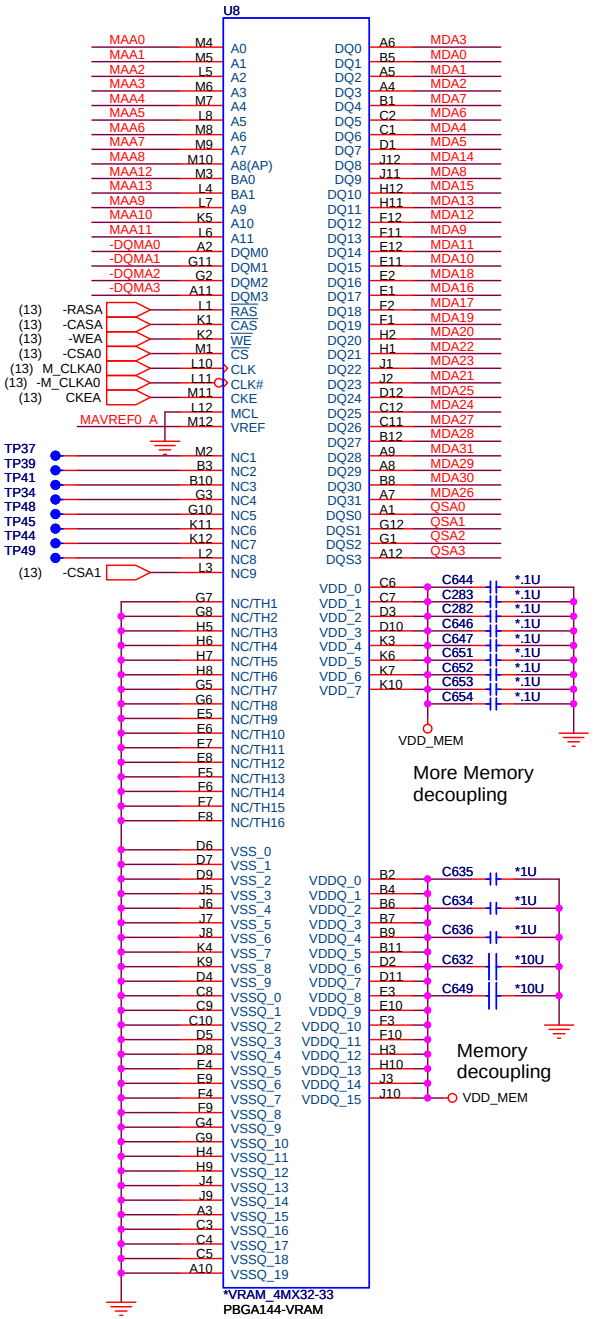
DVPDATA_23~22 MEM TYPE

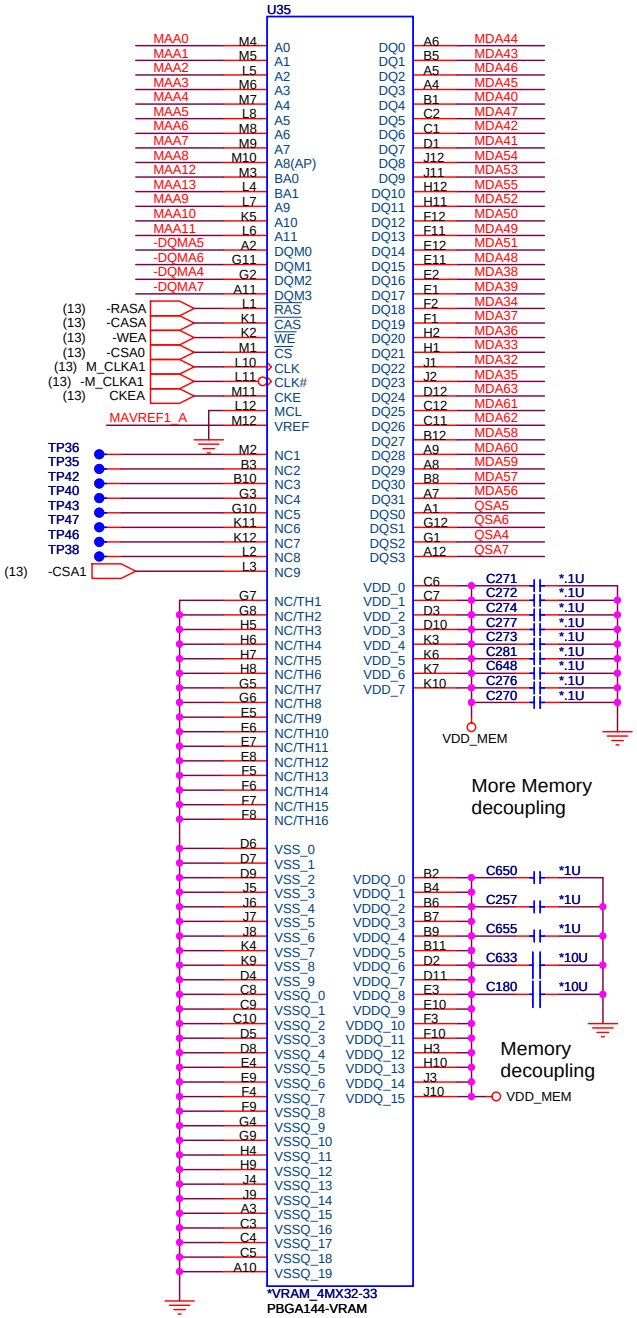
DVPDATA_23	DVPDATA_22	
0	0	Samsung 8M x 32 (1.8V) - M24C
0	1	Samsung 4M x 32 (1.8V) - M24C
1	0	Hynix 8M x 32 (1.8V) - M24C
1	1	Hynix 4M x 32 (1.8V) - M24C



PROJECT : MA2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI M24 MEM/STRAPS PIN	3A
Date: Thursday, March 17, 2005	Sheet 13 of 39	



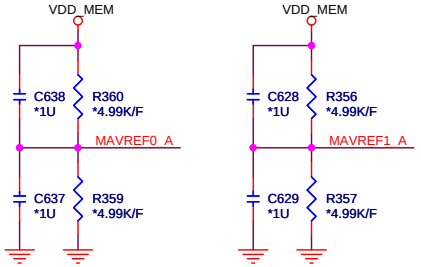


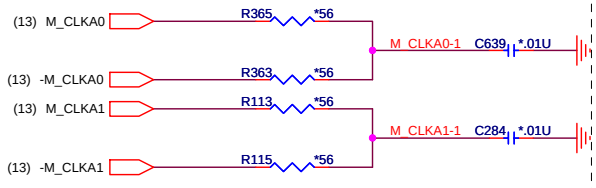
VGA DDR MEMORY A

@64/128MBytes DDR 128Mbit 1MX32X4 uBGA

MAA[0..13] (13)
MDA[0..63] (13)
-DQMA[0..7] (13)
QSA[0..7] (13)

Place close to memory

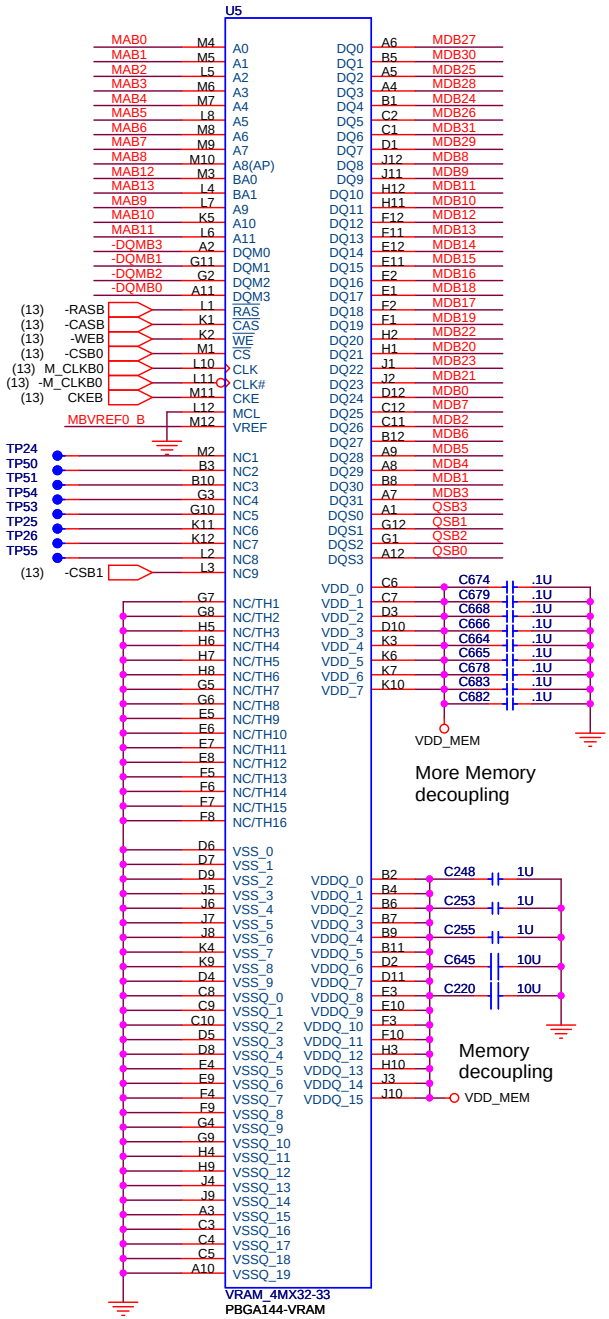


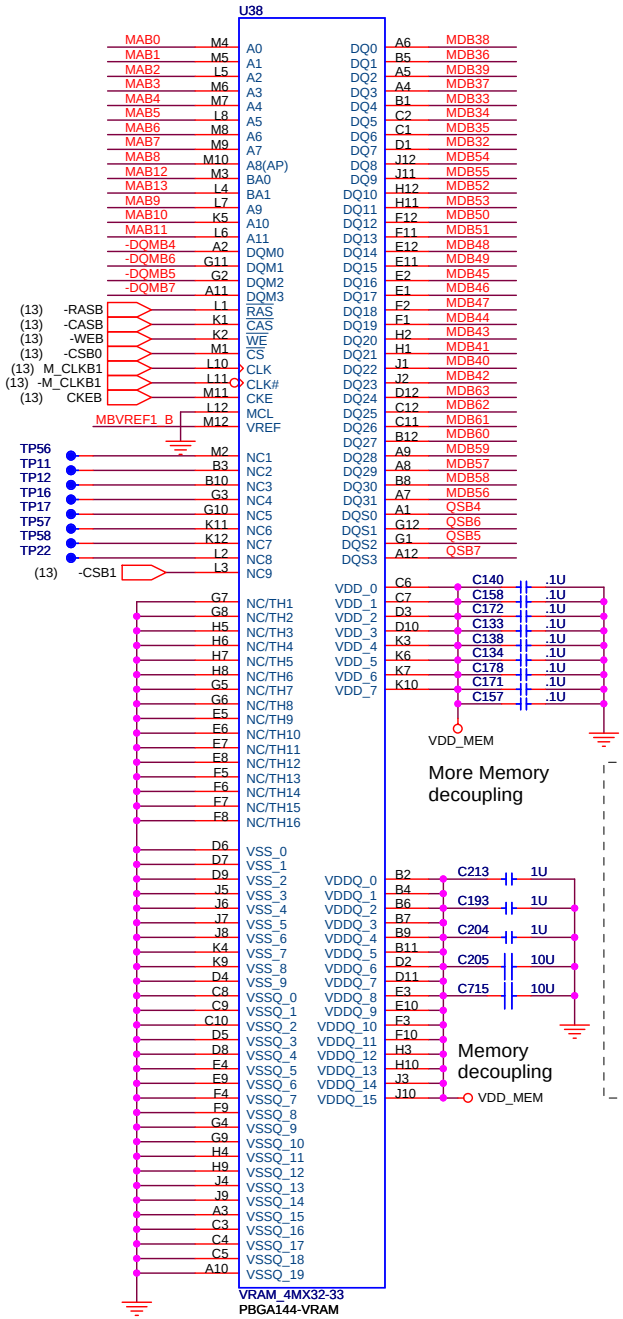


At least a 2.5:1 spacing between the pair

These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory

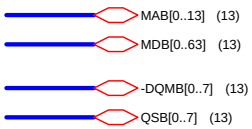
PROJECT : MA2A Quanta Computer Inc.		
Size: B	Document Number: VGA DDR VRAM-A CANNEL	Rev: 3A
Date: Thursday, March 17, 2005	Sheet 14 of 39	



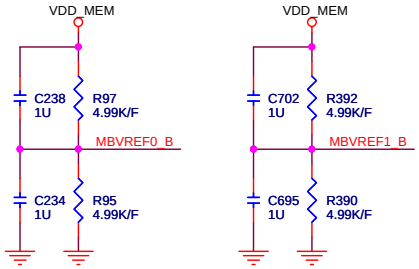


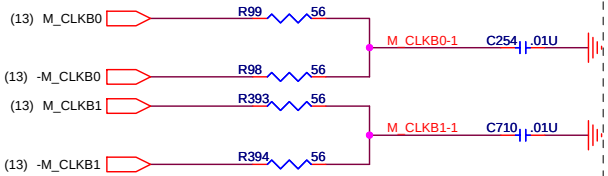
VGA DDR MEMORY B

@64/128MBytes DDR 128Mbit 1MX32X4 uBGA



Place close to memory





At least a 2.5:1 spacing between the pair

These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory

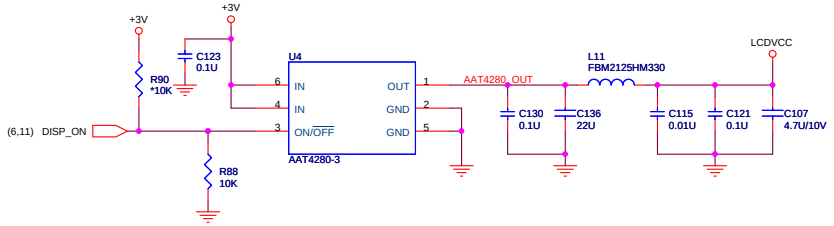
PROJECT : MA2A

Quanta Computer Inc.

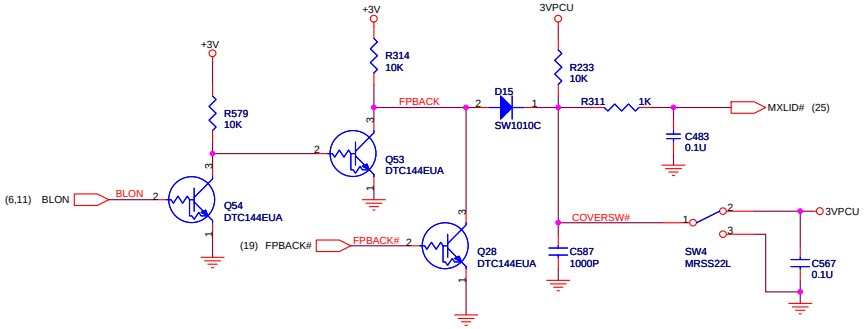
Size	Document Number	Rev
B	VGA DDR VRAM-B CANNEL	3A

Date: Thursday, March 17, 2005 Sheet 15 of 39

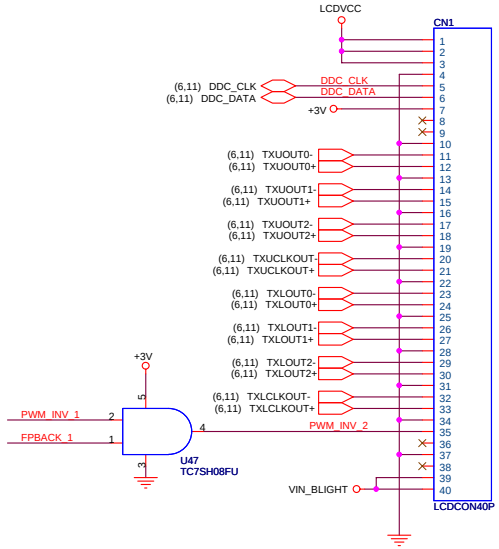
PANEL VCC CONTROL

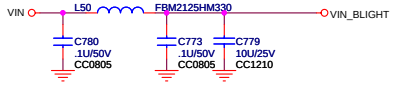


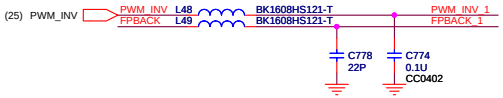
BACKLIGHT CONTROL



LCD CONNECTOR

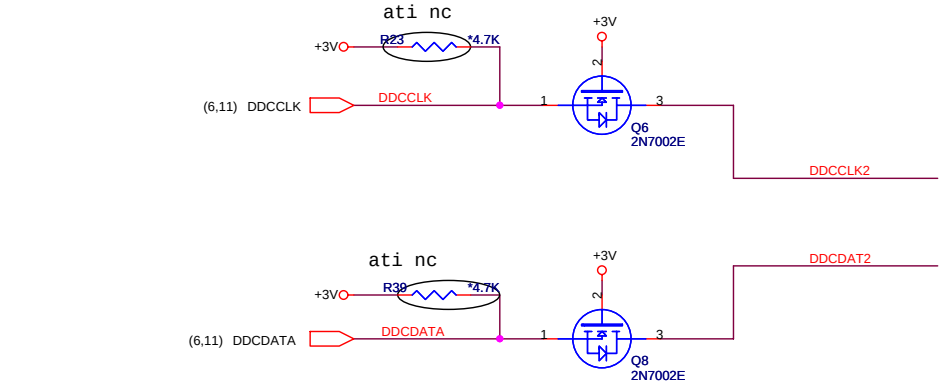


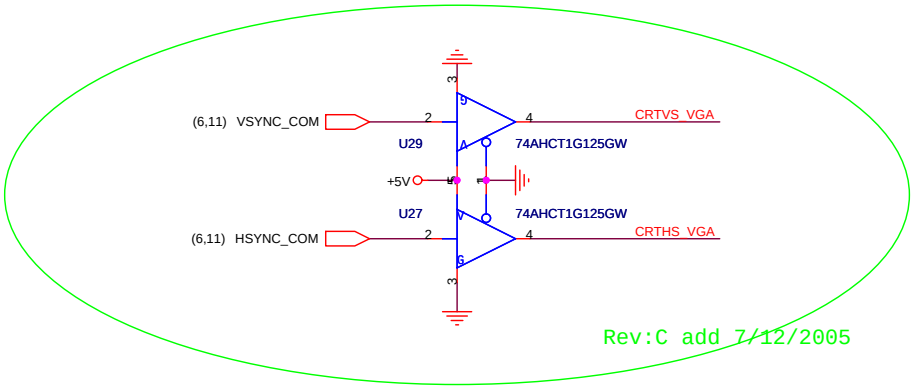




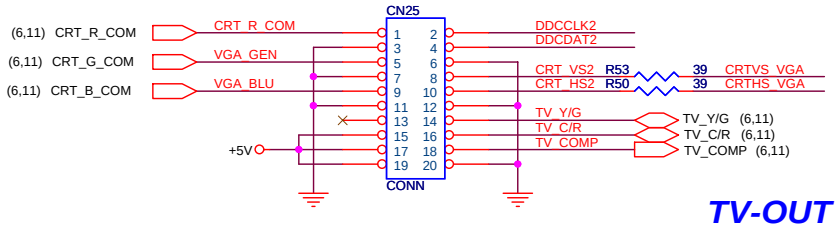
PROJECT : MA2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD LVDS CON	3A
Date: Thursday, March 17, 2005	Sheet 16 of 39	





CRT PORT

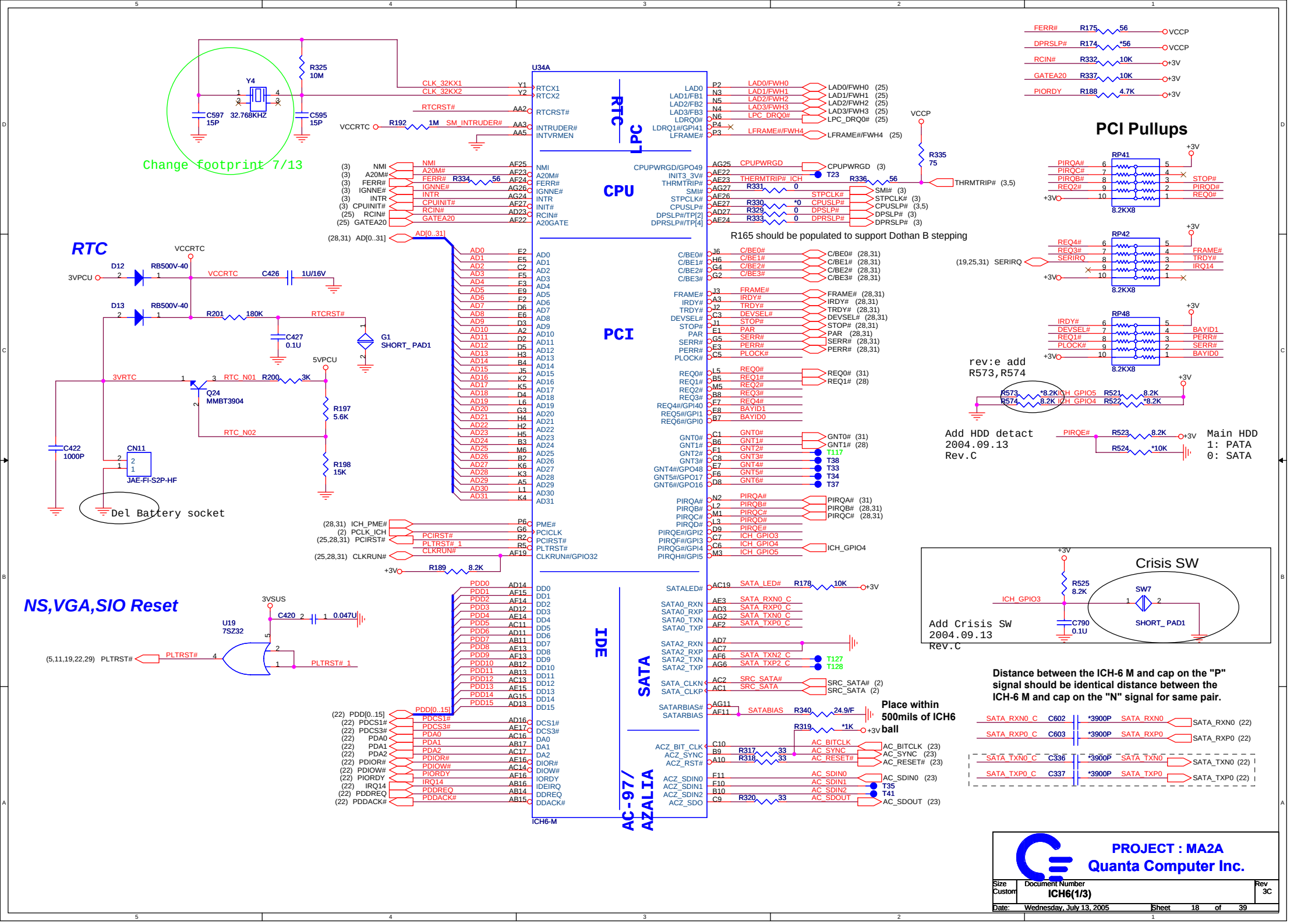


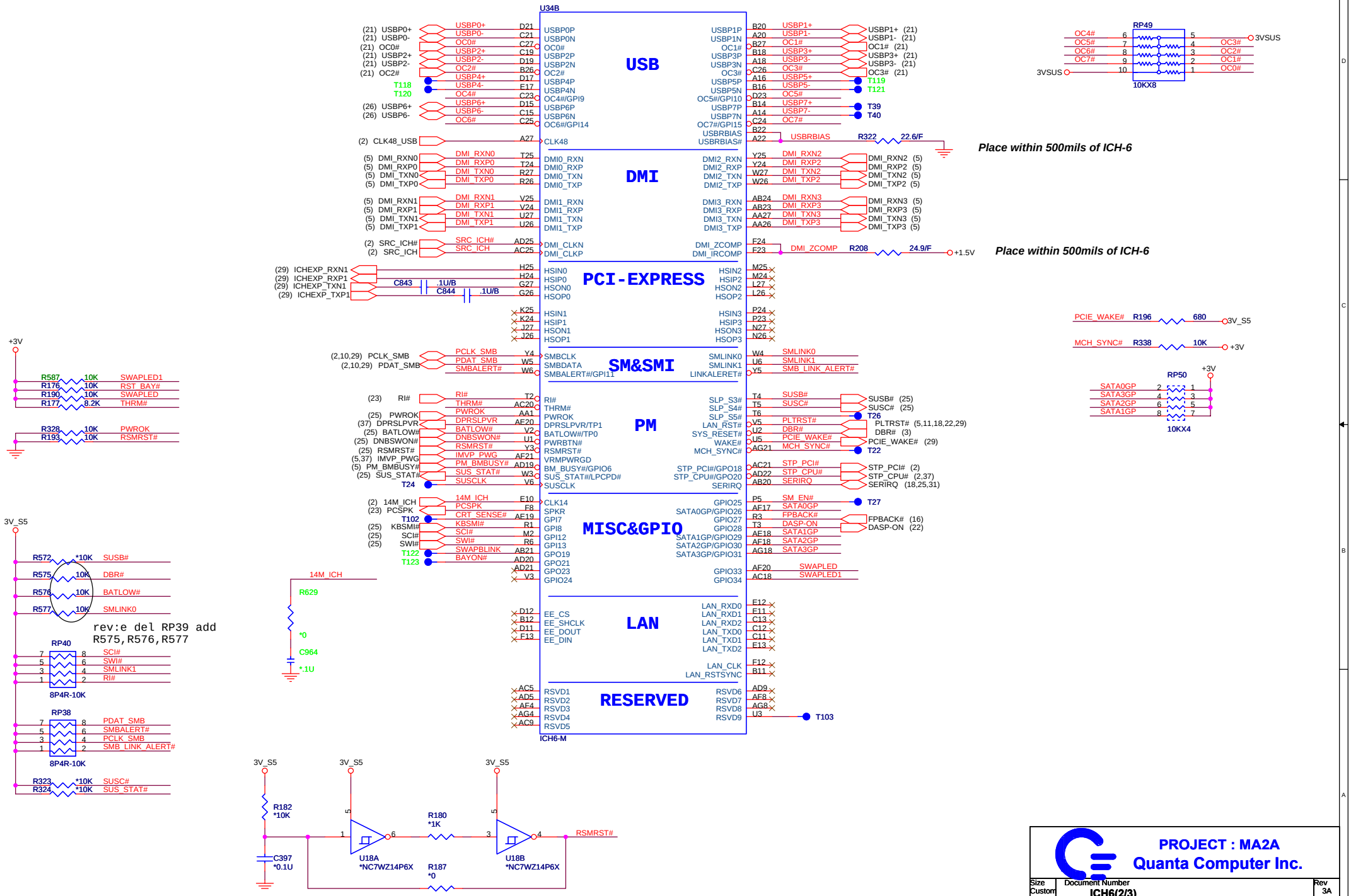
TV-OUT

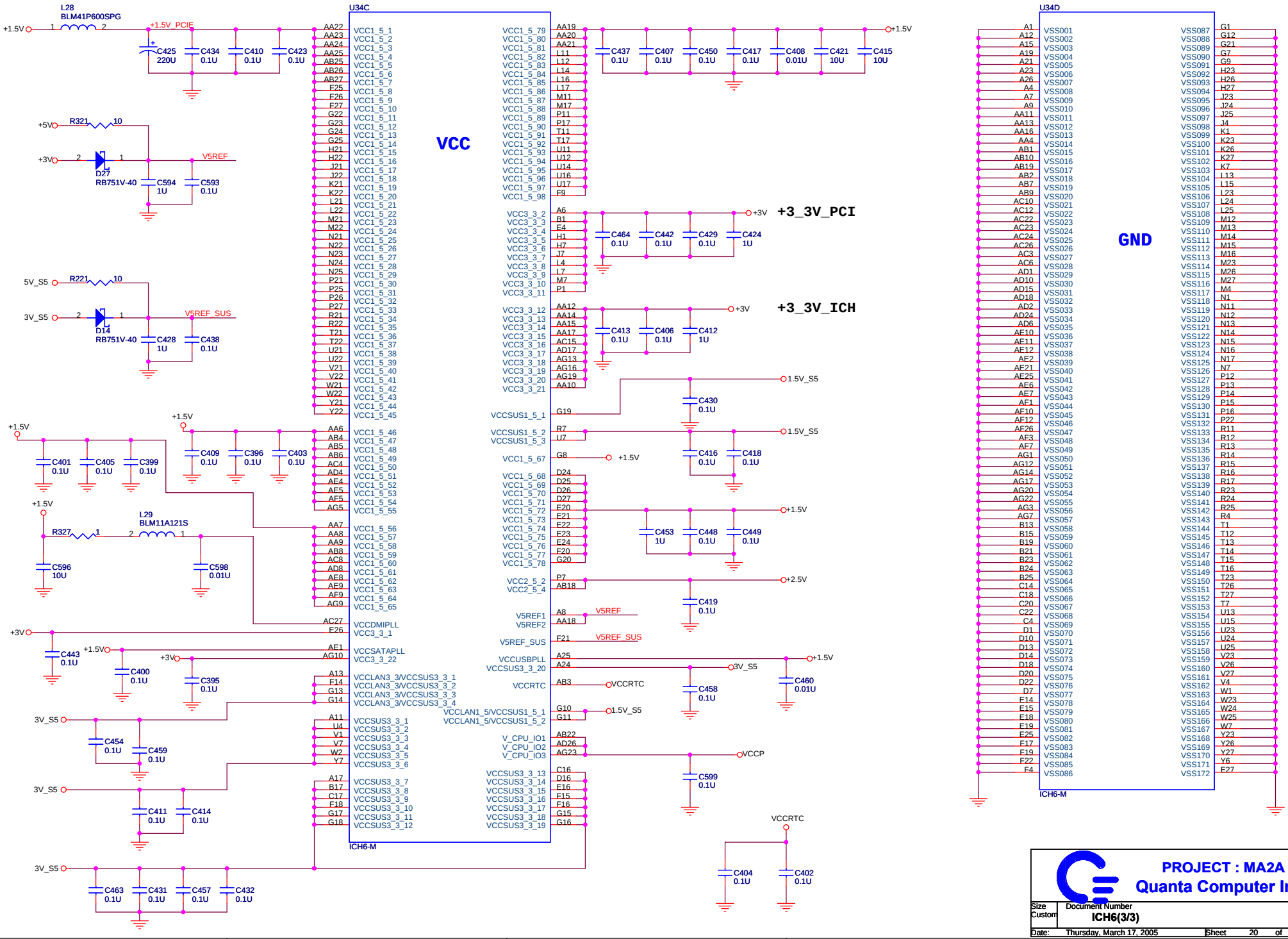
PROJECT : MA2A
Quanta Computer Inc.

Size	Document Number	Rev
B	SVIDEO/CRT/PANLE/HDTV	3C

Date: Wednesday, July 13, 2005 Sheet 17 of 39


Change footprint 7/13
Y4
32.768KHZ
C597 15P
C595 15P
R325 10M
CLK_32KX1
CLK_32KX2
RTCRST#
VCCRTC
R192 1M SM_INTRUDER#
U34A
RTC
LPC
CPU
PCI
IDE
SATA
AC-97/ AZALIA
ICH6-M
RTC
D12 RB500V-40
D13 RB500V-40
3VPCU
VCCRTC
C426 1U/16V
R201 180K
C427 0.1U
G1 SHORT_ PAD1
5VPCU
3VRTC
RTC_N01
R200 3K
Q24 MMBT3904
R197 5.6K
RTC_N02
R198 15K
C422 1000P
CN11
JAE-FI-S2P-HF
Del Battery socket
NS,VGA,SIO Reset
3VSUS
U19 7SZ32
C420 0.047U
PLTRST#
PLTRST# 1
R189 8.2K
R165 should be populated to support Dothan B stepping
R335 75
THRMTRIP# (3,5)
PCI Pullups
RP41
RP42
RP48
8.2KX8
rev:e add R573,R574
R573 *8.2K ICH_GPIO5
R574 8.2K ICH_GPIO4
R521 8.2K
R522 *8.2K
Add HDD detact 2004.09.13 Rev.C
PIRQE# R523 8.2K
R524 *10K
Main HDD 1: PATA 0: SATA
Crisis SW
R525 8.2K
SW7
C790 0.1U
SHORT_ PAD1
Add Crisis SW 2004.09.13 Rev.C
Distance between the ICH-6 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.
SATA_RXN0_C C602 *3900P SATA_RXN0
SATA_RXP0_C C603 *3900P SATA_RXP0
SATA_TXN0_C C336 *3900P SATA_TXN0
SATA_TXP0_C C337 *3900P SATA_TXP0
Place within 500mils of ICH6 ball
R340 24.9/F
R319 *1K
PROJECT : MA2A
Quanta Computer Inc.
Size Custom
Document Number ICH6(1/3)
Rev 3C
Date: Wednesday, July 13, 2005
Sheet 18 of 39


U34B
USB
DMI
PCI-EXPRESS
SM&SMI
PM
MISC&GPIO
LAN
RESERVED
ICH6-M
Place within 500mils of ICH-6
Place within 500mils of ICH-6
RP49
10KX8
RP50
10KX4
RP40
RP38
8P4R-10K
rev:e del RP39 add
R575,R576,R577
U18A
*NC7WZ14P6X
U18B
*NC7WZ14P6X
PROJECT : MA2A
Quanta Computer Inc.
ICH6(2/3)
Thursday, March 17, 2005
Sheet 19 of 39


L28
BLM41P600SPG
+1.5V
+1.5V_PCIE
C425 220U
C434 0.1U
C410 0.1U
C423 0.1U
U34C
VCC
R321 10
+5V
+3V
D27
RB751V-40
V5REF
C594 1U
C593 0.1U
R221 10
5V_S5
3V_S5
D14
RB751V-40
V5REF_SUS
C428 1U
C438 0.1U
C401 0.1U
C405 0.1U
C399 0.1U
C409 0.1U
C396 0.1U
C403 0.1U
L29
BLM11A121S
R327
C596 10U
C598 0.01U
C443 0.1U
C400 0.1U
C395 0.1U
C454 0.1U
C459 0.1U
C411 0.1U
C414 0.1U
C463 0.1U
C431 0.1U
C457 0.1U
C432 0.1U
C437 0.1U
C407 0.1U
C450 0.1U
C417 0.1U
C408 0.01U
C421 10U
C415 10U
C464 0.1U
C442 0.1U
C429 0.1U
C424 1U
+3_3V_PCI
C413 0.1U
C406 0.1U
C412 1U
+3_3V_ICH
C430 0.1U
1.5V_S5
C416 0.1U
C418 0.1U
C453 1U
C448 0.1U
C449 0.1U
C419 0.1U
+2.5V
C458 0.1U
3V_S5
C460 0.01U
C599 0.1U
VCCP
VCCRTC
C404 0.1U
C402 0.1U
ICH6-M
U34D
GND
VSS001
VSS002
VSS003
VSS004
VSS005
VSS006
VSS007
VSS008
VSS009
VSS010
VSS011
VSS012
VSS013
VSS014
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VSS166
VSS167
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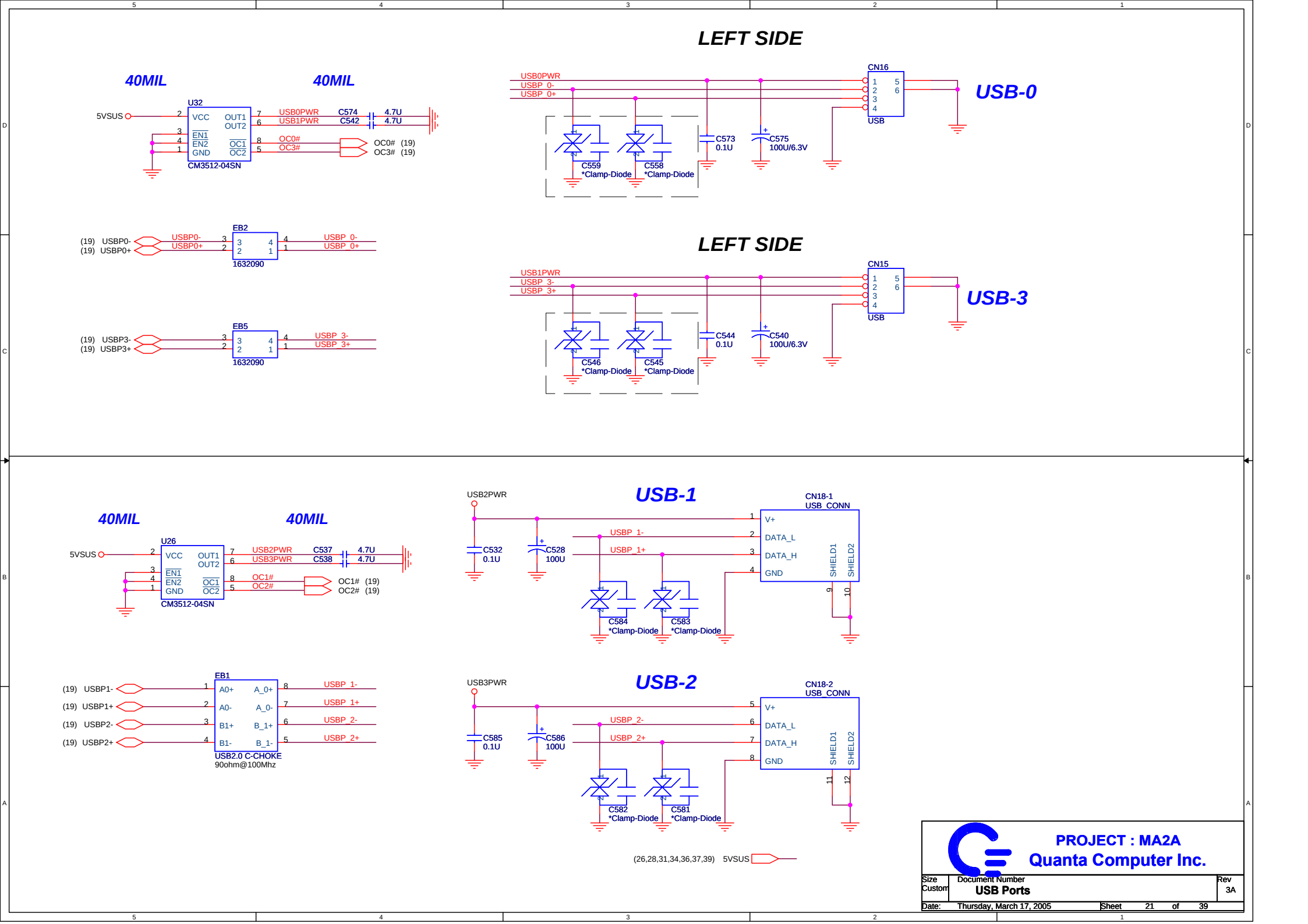
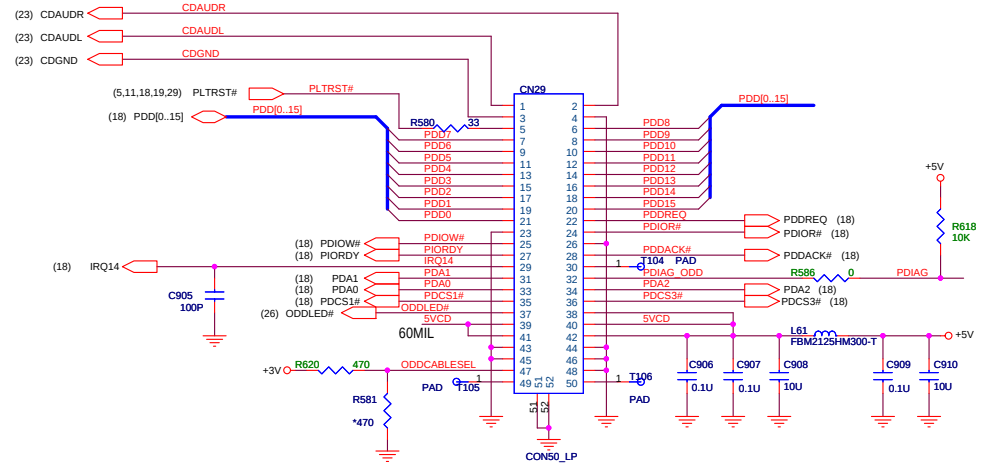
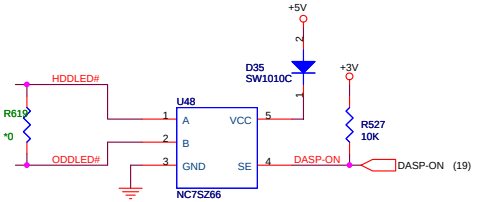
VSS169
VSS170
VSS171
VSS172
ICH6-M
PROJECT : MA2A
Quanta Computer Inc.
Size Custom
Document Number ICH6(3/3)
Rev 3A
Date: Thursday, March 17, 2005
Sheet 20 of 39


LEFT SIDE
40MIL
40MIL
U32
5VSUS
VCC
OUT1
OUT2
EN1
EN2
GND
OC1
OC2
CM3512-04SN
USB0PWR
USB1PWR
C574
C542
4.7U
4.7U
OC0#
OC3#
OC0# (19)
OC3# (19)
USBP0-
USBP0+
EB2
1632090
USBP_0-
USBP_0+
(19) USBP0-
(19) USBP0+
USBP3-
USBP3+
EB5
USBP_3-
USBP_3+
(19) USBP3-
(19) USBP3+
USB0PWR
USBP_0-
USBP_0+
CN16
USB
USB-0
C559
*Clamp-Diode
C558
*Clamp-Diode
C573
0.1U
C575
100U/6.3V
LEFT SIDE
USB1PWR
USBP_3-
USBP_3+
CN15
USB
USB-3
C546
*Clamp-Diode
C545
*Clamp-Diode
C544
0.1U
C540
100U/6.3V
40MIL
40MIL
U26
5VSUS
CM3512-04SN
USB2PWR
USB3PWR
C537
C538
4.7U
4.7U
OC1#
OC2#
OC1# (19)
OC2# (19)
EB1
USB2.0 C-CHOKE
90ohm@100Mhz
(19) USBP1-
(19) USBP1+
(19) USBP2-
(19) USBP2+
A0+
A0-
B1+
B1-
A_0+
A_0-
B_1+
B_1-
USBP_1-
USBP_1+
USBP_2-
USBP_2+
USB-1
USB2PWR
C532
0.1U
C528
100U
USBP_1-
USBP_1+
CN18-1
USB_CONN
V+
DATA_L
DATA_H
GND
SHIELD1
SHIELD2
C584
*Clamp-Diode
C583
*Clamp-Diode
USB-2
USB3PWR
C585
0.1U
C586
100U
USBP_2-
USBP_2+
CN18-2
USB_CONN
C582
*Clamp-Diode
C581
*Clamp-Diode
(26,28,31,34,36,37,39) 5VSUS
PROJECT : MA2A
Quanta Computer Inc.
Size
Custom
Document Number
USB Ports
Rev
3A
Date: Thursday, March 17, 2005
Sheet 21 of 39

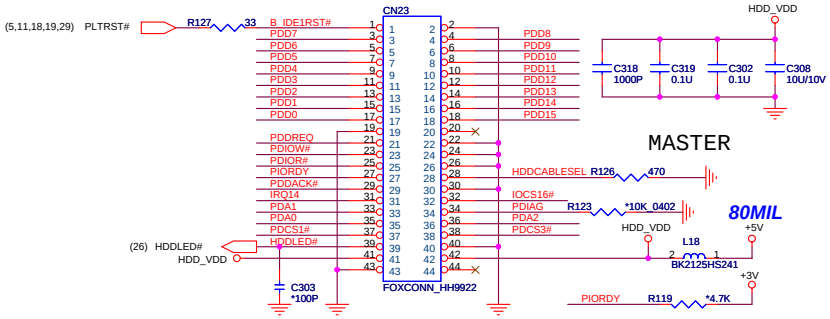
For fix ODD change 0427

CD-ROM connector

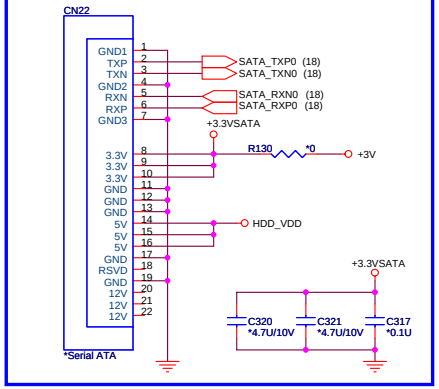




HDD CONNECTOR



SATA CONNECTOR



PROJECT : MA2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	IDE (HDD&CD_ROM	3A
Date: Thursday, March 17, 2005	Sheet 22 of 39	

For Layout:
Place decoupling caps near the power pins of SmartAMC device.

3VSUS B: Change net from 3V to 3VSUS

MC5 10U/6.3V, MC15 0.1U_0402, MC16 0.1U_0402, MC14 0.1U_0402, MC10 0.1U_0402, MC6 0.1U_0402

MR12 249K (1%)

For Layout: Close to SmartAMC device.

B: Change MR2,MR3 footprint to R0603 for EMI

L20 *BK2125HM121

MC3 0.1U_0402, MC12 1U/10V, MC13 10U/6.3V

+3.3VA, AGND

MU1 — 20468-31 <Conexant Name>

VDD5, VDD18, VDD10, VDD_CLK, AVDD33, AVDD44

RCOSC1 — RC_OSC

DIB_DATAN — MR16 0

DIB_DATAP — MR15 0

PWRCLKP — MR14 0

PWRCLKN — MR13 0

SDATA_OUT, SYNC, AC_RESET#

AC_ONLY

SDATA_IN0 — MR8 33 — (18) AC_SDIN0

BIT_CLK — BIT_CLK0 — MR6 33 — (18) AC_BITCLK

ID0# — MR11 *0

ID1# — MR10 *0

EAPD

PC_BEEP — BEEP

DSPKOUT

MIC_IN — MIC — MC4 10U/10V/V — MIC1 — MIC1 (24)

CD_IN_R — RCDR

CD_IN_GND — CDGND1

CD_IN_L — RCDL

LINE_IN_L — LINE_INL — MC19 0.1U

LINE_IN_R — LINE_INR — MC20 0.1U

LINE_OUT_L — AC97OUT_L — AC97OUT_L (24)

LINE_OUT_R — AC97OUT_R — AC97OUT_R (24)

HP_OUT_L, HP_OUT_R

REF_FLT, VC_SCA, VREF_SCA

MBIAS/AVDD — MIC_BIAS — MR5 3K

S_PDIF

GPIO_4 — HPSENCE_PR

GPIO_5 — HPSENSE (24)

XTLO, XTLI — MR3 33, MR4 *1M — MY1 24.576MHZ — MC1 22P, MC2 22P

GNDC2, GND8, GNDC9, GNDC19, AVSS_CLK, AGND35, AGND41

15:5:15 routing , 50 mil to other signal

MC18 150P_0402, MC17 150P_0402

(18) AC_SDOUT, (18) AC_SYNC, (18) AC_RESET#

Modified. B-Stage

Check this pin fumction .

CN9 — AMC Connector — DIB_DATAP, PWRCLKN, DIB_DATAN, PWRCLKP

CODEC POWER

+5V, U15 GMT_G960T63U (IN, ADJ, OUT), 800mA (30MIL), +3.3VA

C391 0.47U_0402, C388 0.1U_0402, R168 *124, R169 0

SOFTWARE EQ CONTROL TABLE

GPIO4	GOIO5	S/W EQ
LOW	LOW	ON
LOW	HIGH	OFF
HIGH	LOW	OFF
HIGH	HIGH	OFF

MC7 0.1U_0402, MC8 0.1U_0402, MC9 0.1U_0402, MC11 1U/10V

R623 *1K, R624 1K

RI FUNCTION

3VSUS, 3VSUS

R218 2.2K, R215 10K

Q26 DTC144EUA, Q27 DTC144EUA

RI# (19)

(31) PCICRI# — PCICRI#

PC BEEP CONTROL

For Layout:
Place crystal and associated circuitry very near SmartAMC Device.

Ground Tie — MR1 0, MR17 0, MR2 0

NORMAL : LOW

(31) PCMSPK#, (19) PCSPK — U14 7SH86

C384 0.1U_0402

BEEP1 — R165 2.2K — BEEP2 — C380 0.47U/10V — BEEP

R171 1K, C387 1000P_0402

RCDR — C345 10U/10V — R148 4.7K — CDAUDR (22)

RCDL — C325 10U/10V — R137 4.7K — CDAUDL (22)

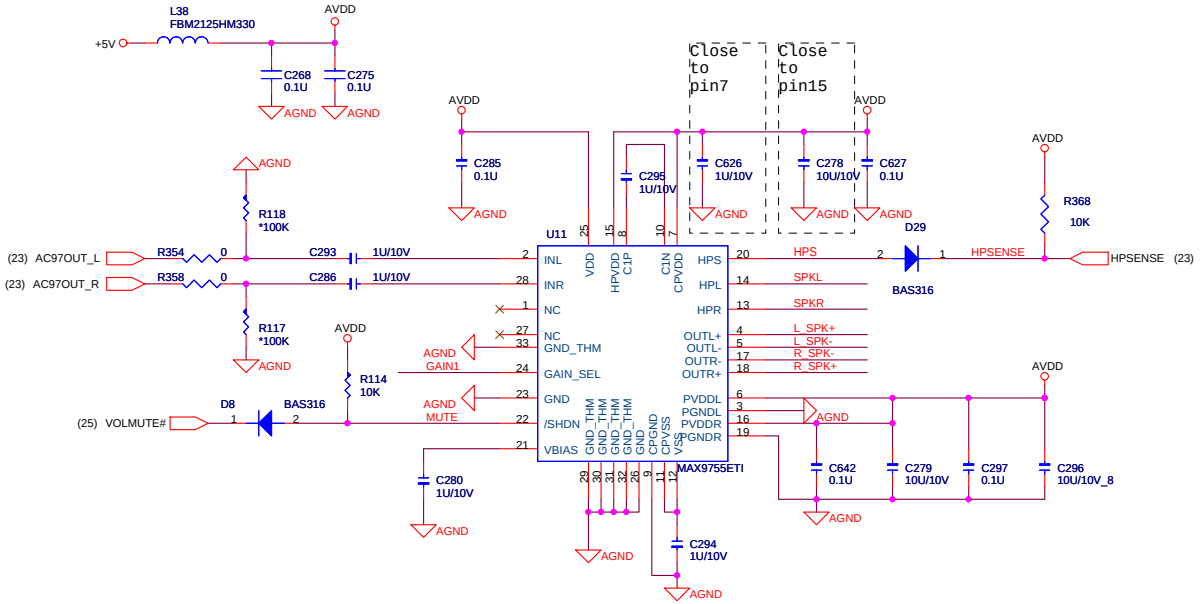
CDGND1 — C339 10U/10V — R144 4.7K — CDGND (22)

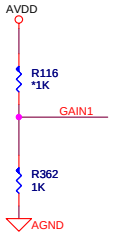
R141 4.7K, R134 4.7K, R147 4.7K

PROJECT : MA2A
Quanta Computer Inc.

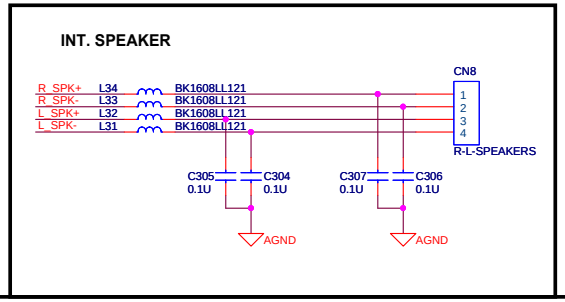
Size	Document Number	Rev
Custom	SMARTAMC-CONEXANT_20468-31	3A
Date: Thursday, March 17, 2005	Sheet 23 of 39	

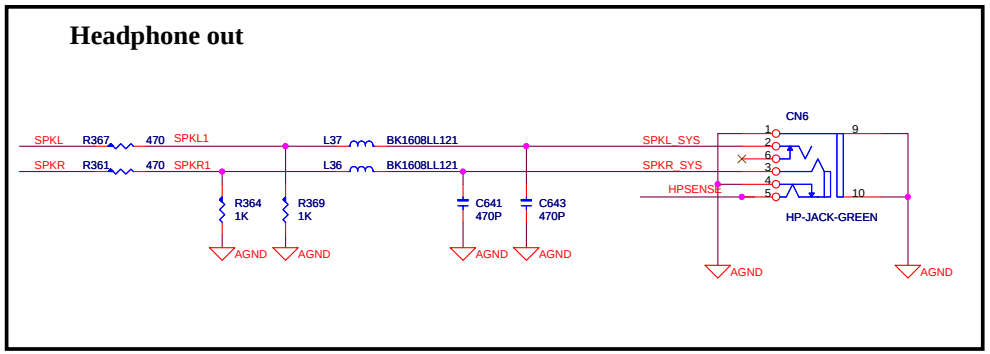
AUDIO AMPLIFIER-MAX9755

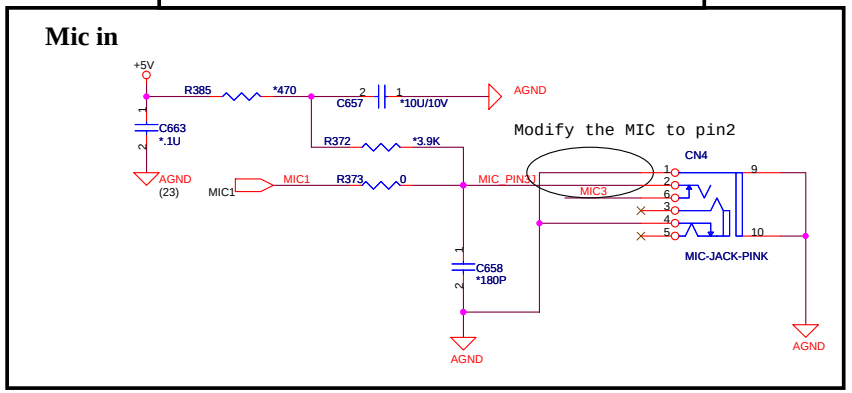




GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0







PROJECT : MA2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AUDIO AMP & JACK	3A
Date: Thursday, March 17, 2005	Sheet 24 of 39	

KBC-NS97551L

U28

PC97551VPC

Host interface

AD Input

DA output

PWM or PORT-A

PORT-B

Key matrix scan

PORT-C

PORT-D-1

PORT-E

JTAG debug port

PS2 interface

PORT-H

PORT-I

PORT-J-1

PORTJ-2

PORT-D-2

PORT-K

PORT-M

PORT-L

LDRQ#(pin 8) internal is no use

Modify the RF_OFF#

POWER SWITCH

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

SHBM=1: Enable shared memory with host BIOS

I/O Address

BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

8Mbit (1M Byte), TSSOP40

ST Micro M29W008AB/AMD-29LV081B/SST39VF080

*PLCC32

*NM24C02-WMN6T

Change footprint 7/13

Rev:C Add 7/13/2005
Close to EC "U28"

rev:e del d18

Pin 103 internal is "A19",Can't use to GPIO

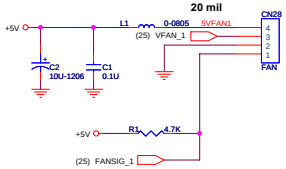
PROJECT : MA2A
Quanta Computer Inc.

KBC-PC87551VPC

Rev 3C

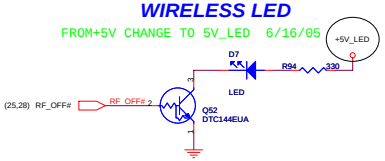
Wednesday, July 13, 2005 Sheet 25 of 39

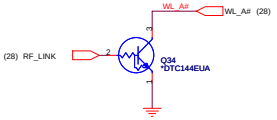
FAN OUT PWM CONNECTOR



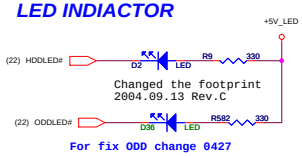
WIRELESS LED

FROM+5V CHANGE TO 5V_LED 6/16/05

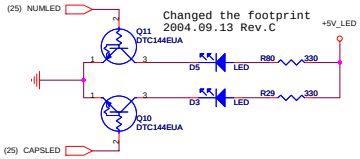




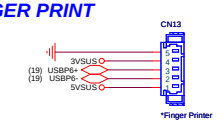
LED INDIACTOR



For fix ODD change 0427

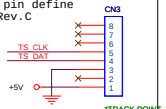


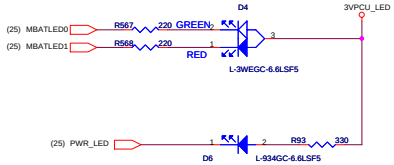
FINGER PRINT



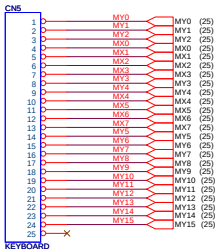
TRACK POINT

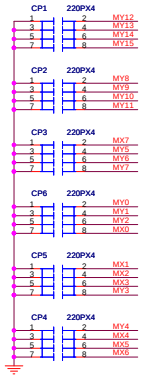
Changed the pin define
2004.09.13 Rev.C

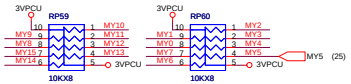




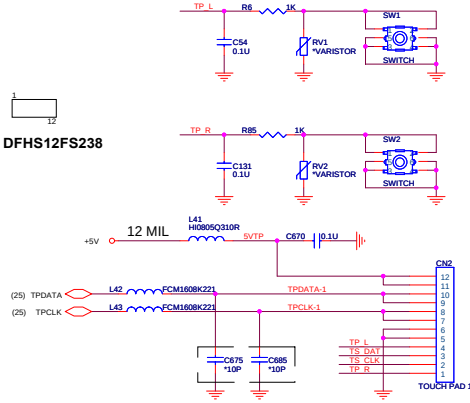
KEYBOARD



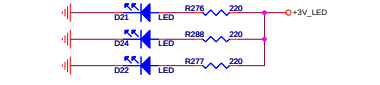


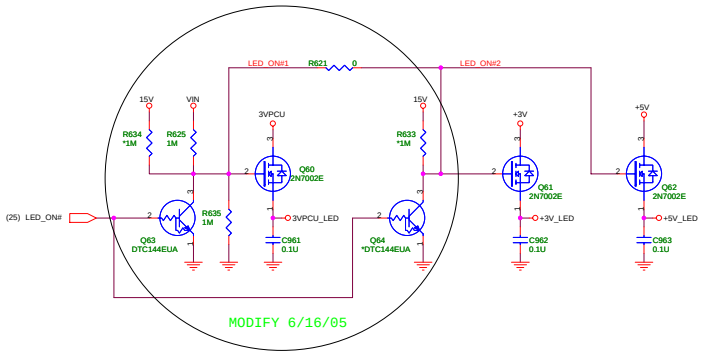


TOUCHPAD



E: Change the PN and footprint from DFHS12FS203 to DFHS12FS238.

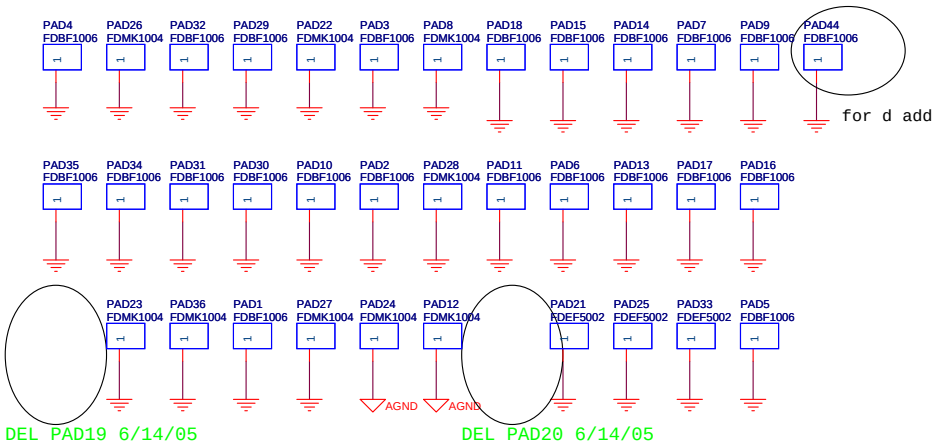


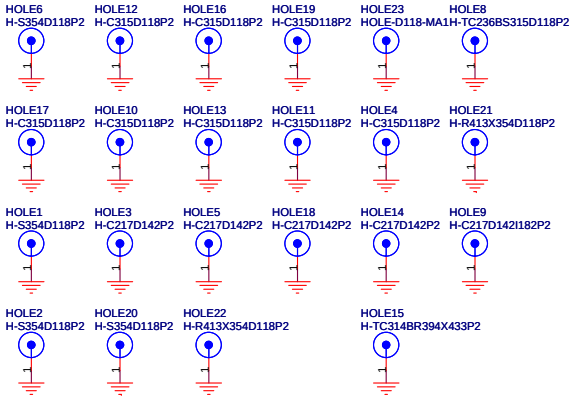


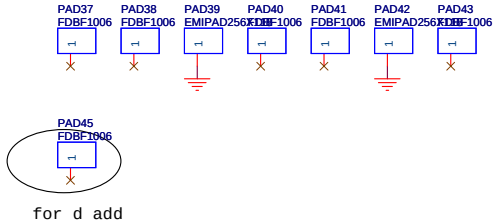
MODIFY 6/16/05

PROJECT : MA2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	K/B & FAN & LED & SW	3B
Date: Thursday, June 16, 2005	Sheet 26 of 39	







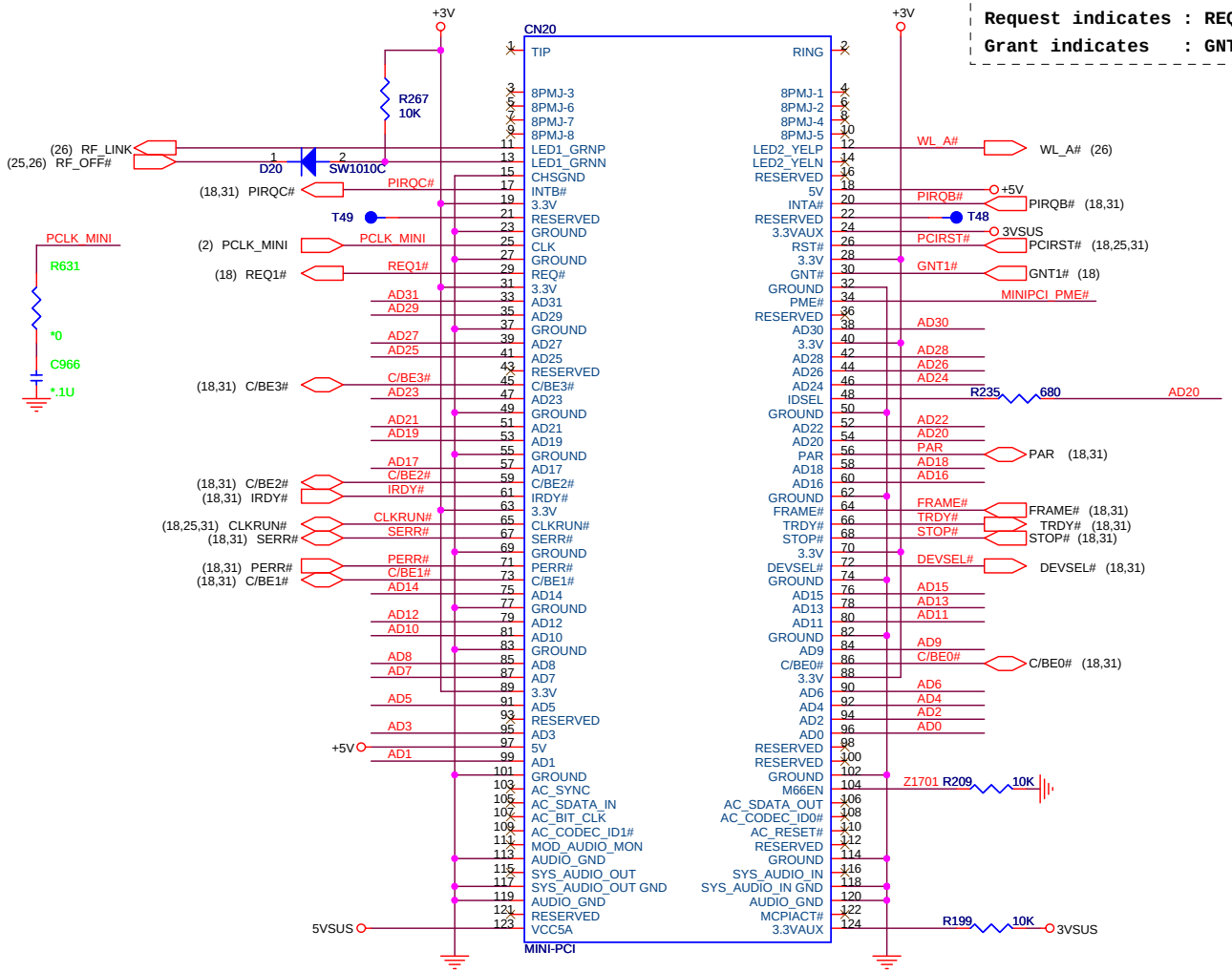
PROJECT : MA2A
Quanta Computer Inc.

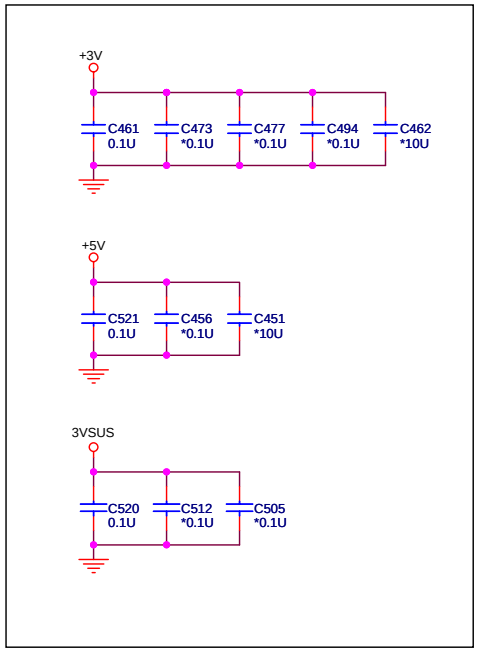
Size	Document Number	Rev
Custom	EMI PAD	3A
Date: Thursday, March 17, 2005	Sheet 27 of 39	

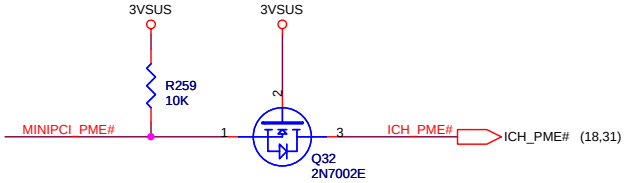
TYPE III MINI PCI SOCKET

AD[0..31] — AD[0..31] (18,31)

ID Select	:	AD20
Interrupt Pin	:	PIRQB# , PIRQC#
Request indicates	:	REQ1#
Grant indicates	:	GNT1#







PROJECT : MA2A
Quanta Computer Inc.

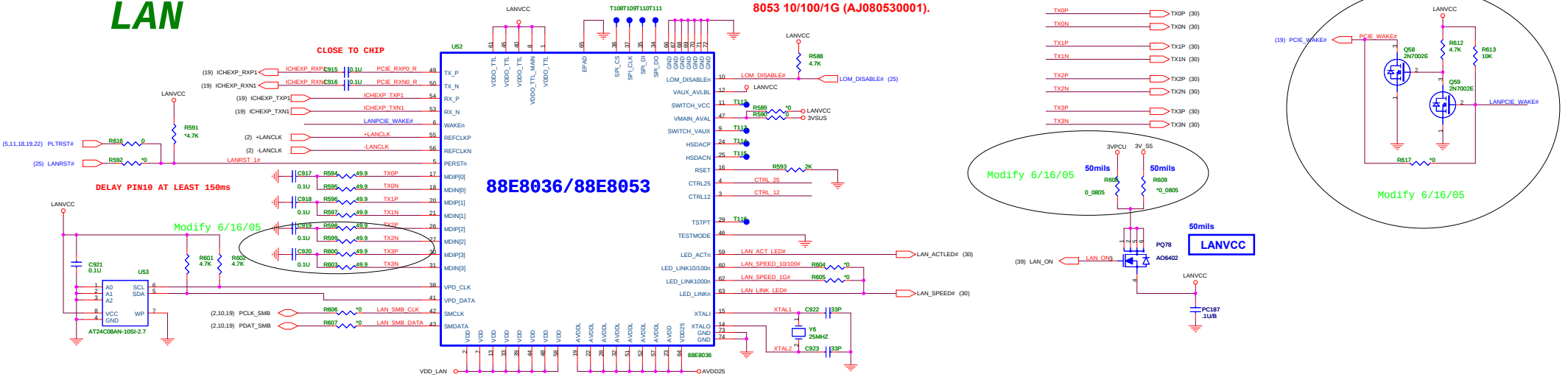
Size	Document Number	Rev
B	MINI PCI Socket & MDC	3A

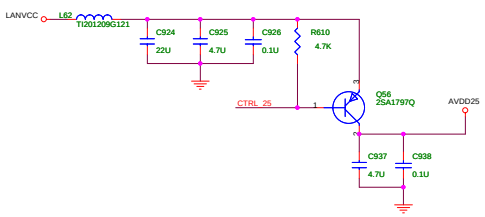
Date: Thursday, March 17, 2005 Sheet 28 of 39

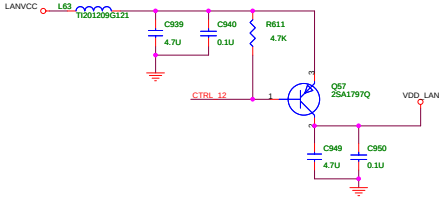
LAN

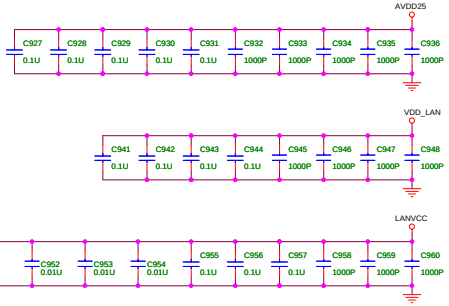
8036 10/100(AJ080360F02)

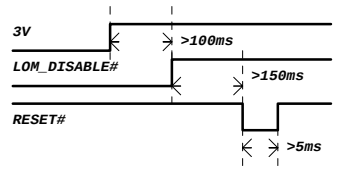
8053 10/100/1G (AJ080530001).







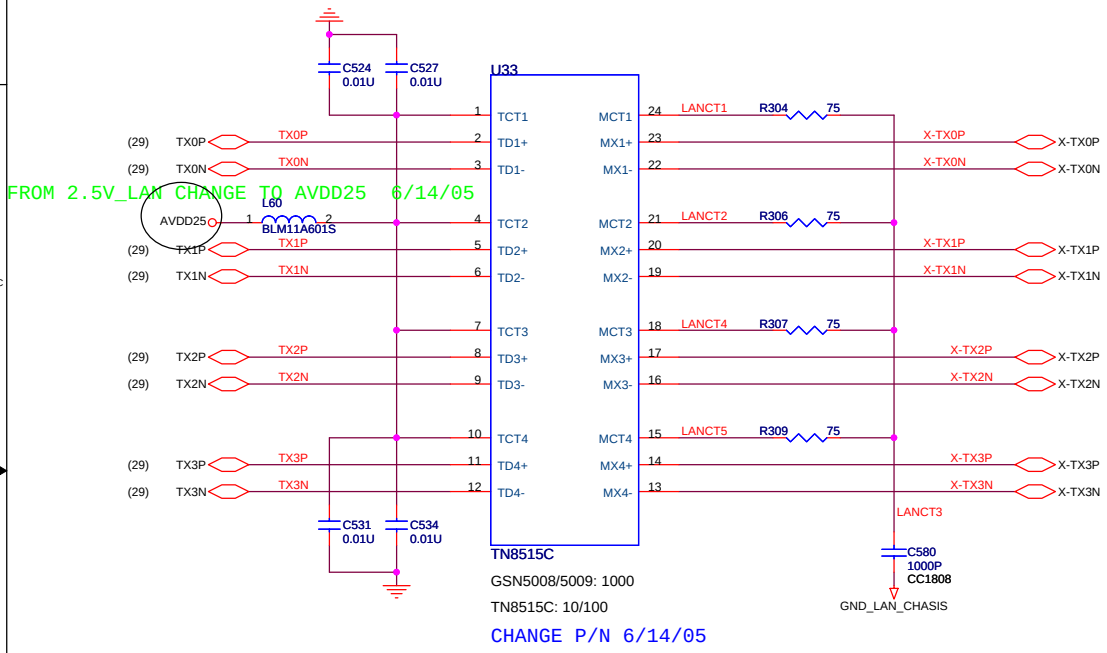


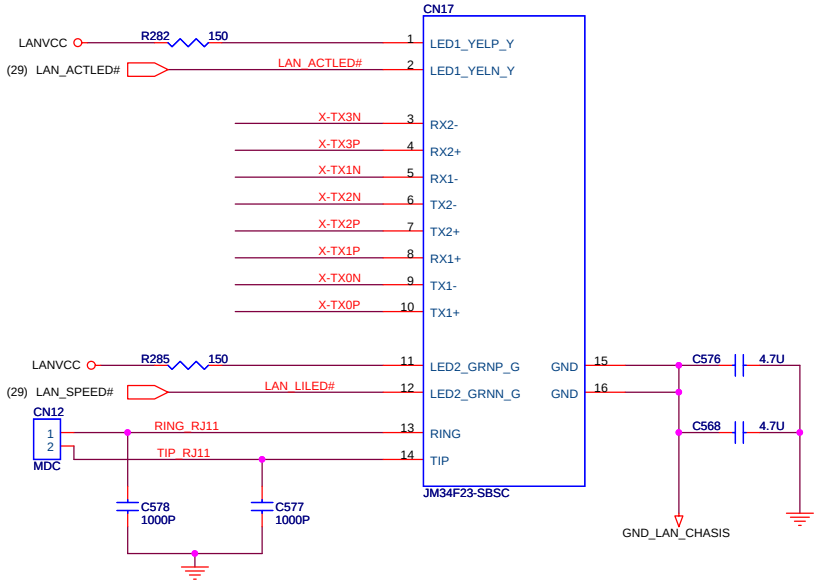


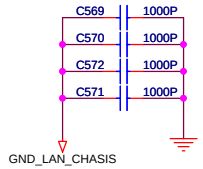
PIN number	88E8053	88E8036
34	SPI_DO (Unused)	NC
35	SPI_DI (Unused)	NC
36	SPI_CS (Unused)	NC
37	SPI_CLK (Unused)	NC
26	MDIP2	NC
27	MDIN2	NC
30	MDIP3	NC
31	MDIN3	NC
42	NC	NC
43	NC	NC
60	LINK 10M/100M	LINK 10M
62	LINK 1000M	LINK 100M
16	RESISTOR 5K	RESISTOR 2K
64	2.5V	NC

PROJECT : MA2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCIE LAN 88E8036/88E8053	3B
Date: Thursday, June 16, 2005	Sheet 29 of 39	







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<OrgAddr2>	Quanta Computer Inc.	
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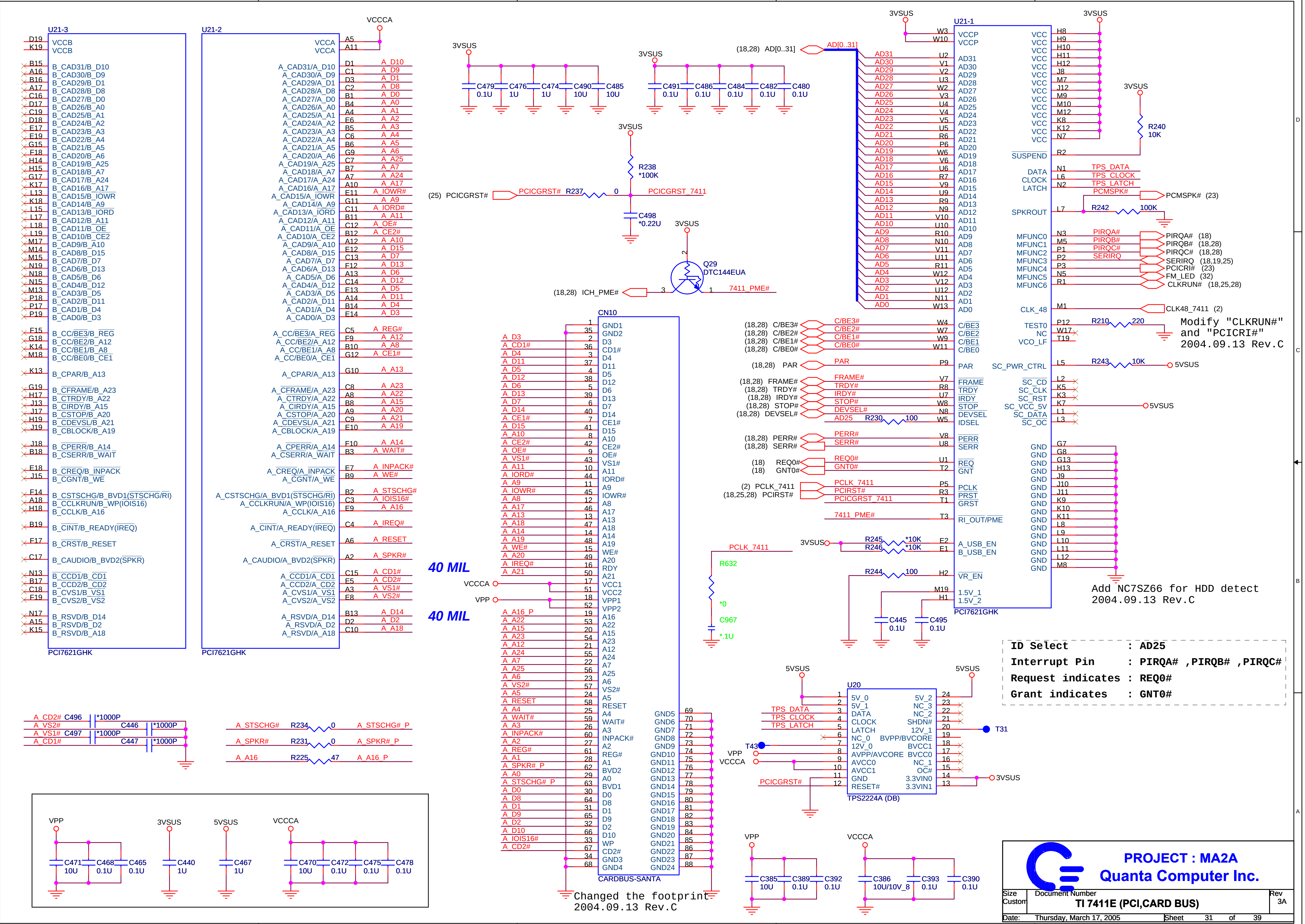
<OrgAddr4>		
Size: Custom	Document Number: LAN, RJ11, RJ45	Rev: 3B
Date: Thursday, June 16, 2005	Sheet 30 of 39	

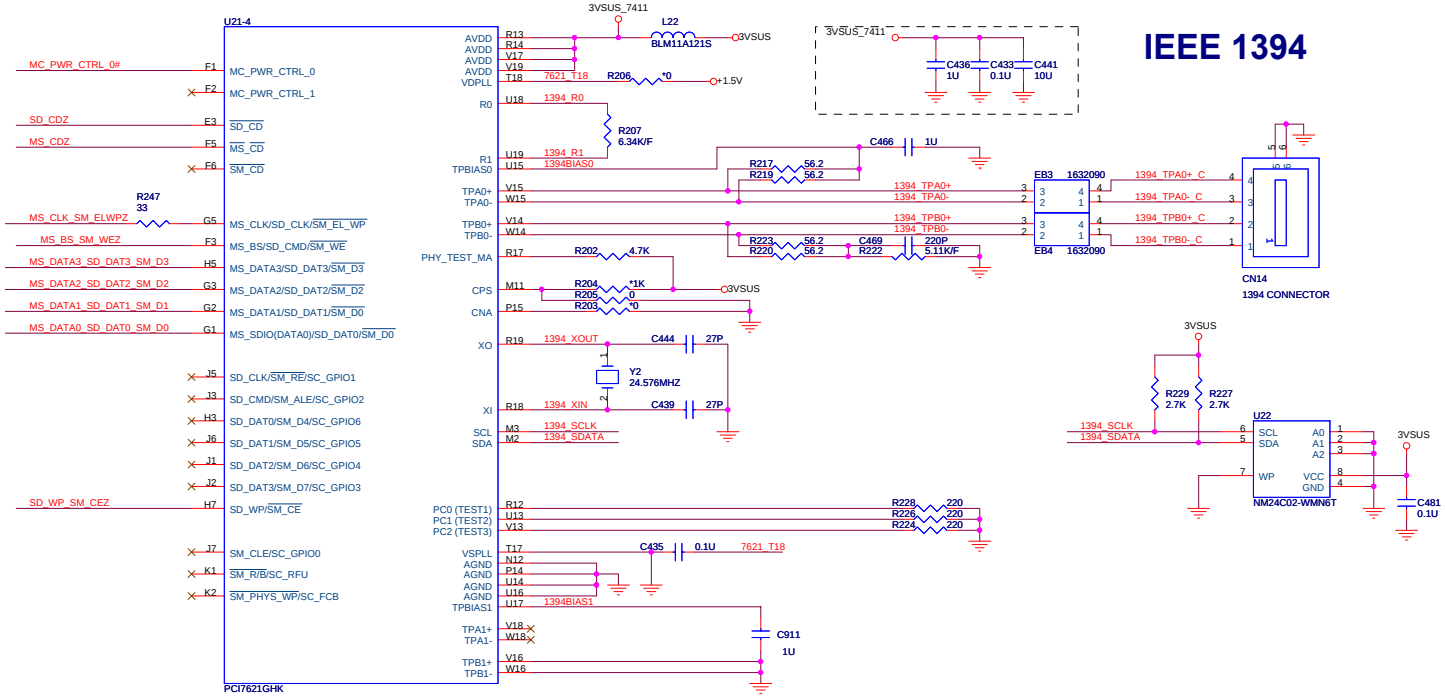

U21-3
U21-2
U21-1
PCI7621GHK
CN10
CARDBUS-SANTA
U20
TPS2224A (DB)
Q29
DTC144EUA
VCCCA
3VSUS
5VSUS
VPP
40 MIL
(25) PCICGRST#
(18,28) ICH_PME#
(18,28) AD[0..31]
PCMSPK# (23)
PIRQA# (18)
PIRQB# (18,28)
PIRQC# (18,28)
SERIRQ (18,19,25)
PCICRI# (23)
FM_LED (32)
CLKRUN# (18,25,28)
CLK48_7411 (2)
Modify "CLKRUN#" and "PCICRI#" 2004.09.13 Rev.C
Add NC7SZ66 for HDD detect 2004.09.13 Rev.C
Changed the footprint 2004.09.13 Rev.C
ID Select : AD25
Interrupt Pin : PIRQA# ,PIRQB# ,PIRQC#
Request indicates : REQ0#
Grant indicates : GNT0#
T31
T43

PROJECT : MA2A

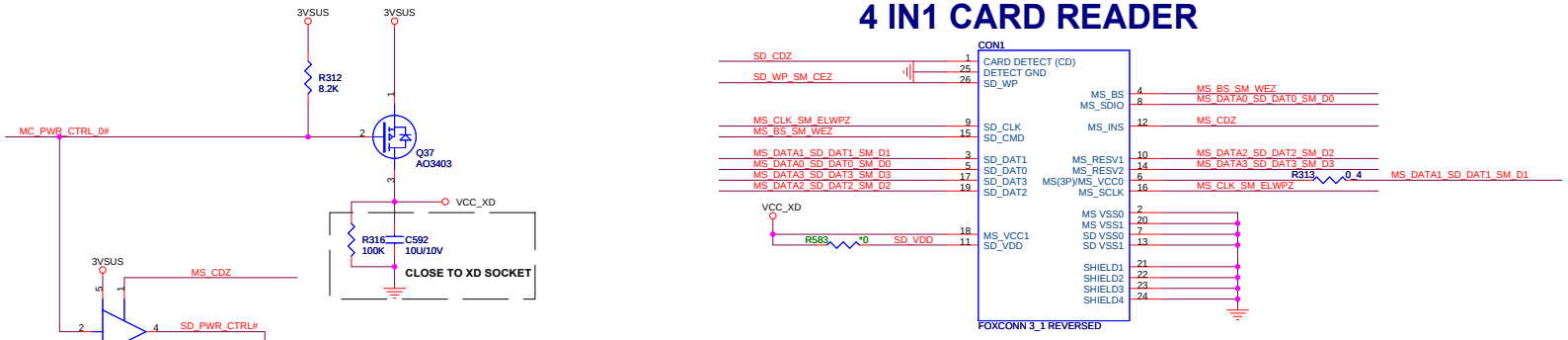
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TI 7411E (PCI,CARD BUS)	3A
Date: Thursday, March 17, 2005	Sheet 31 of 39	

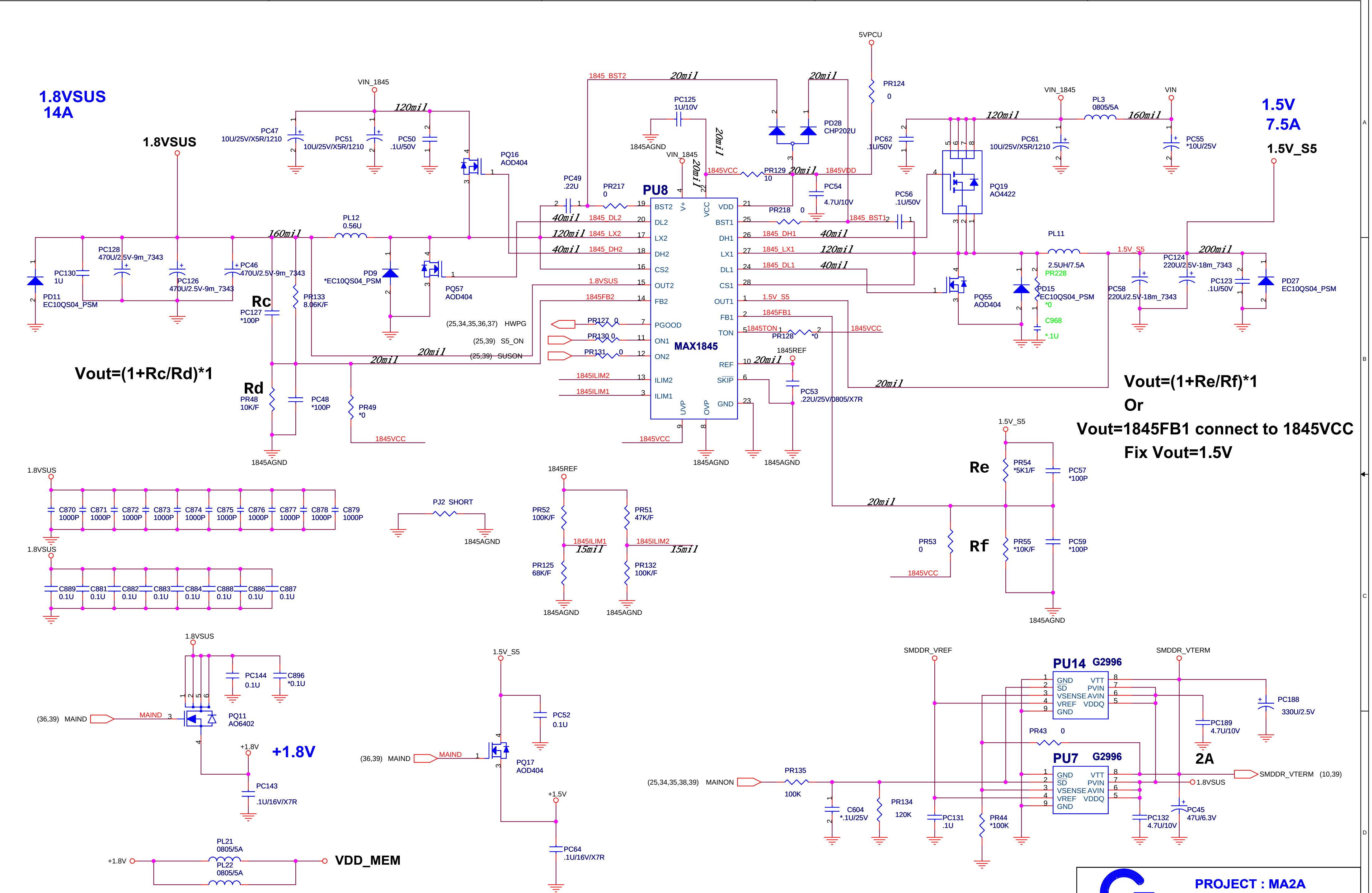
IEEE 1394



4 IN1 CARD READER



PROJECT : MA2A Quanta Computer Inc.			
Size: Custom	Document Number: TI 7411E (1394 & CARD_READER)		Rev: 3A
Date: Thursday, March 17, 2005	Sheet 32 of 39		

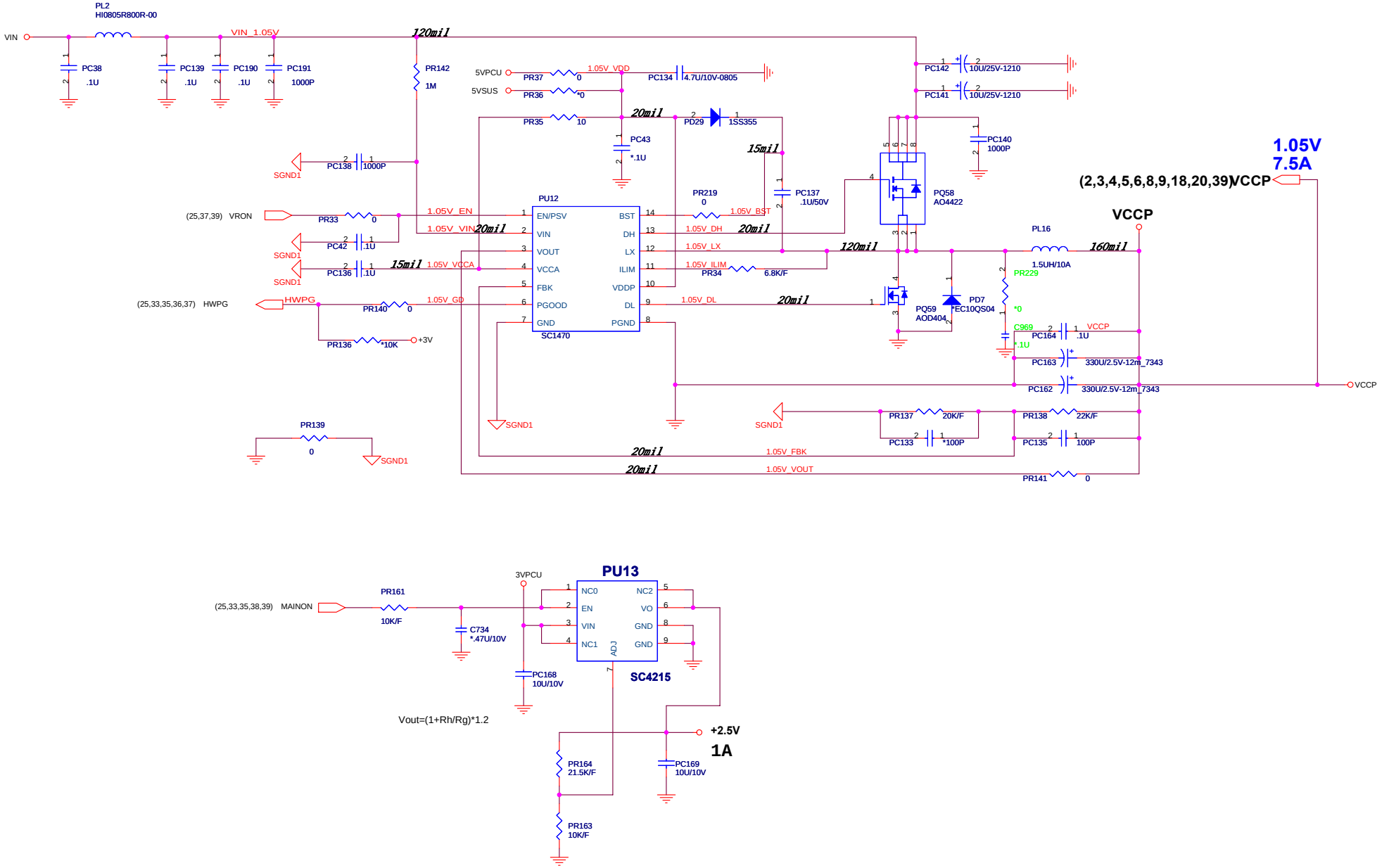


PROJECT : MA2A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.05V/1.5V	3A

Date: Thursday, March 17, 2005 | Sheet 33 of 39

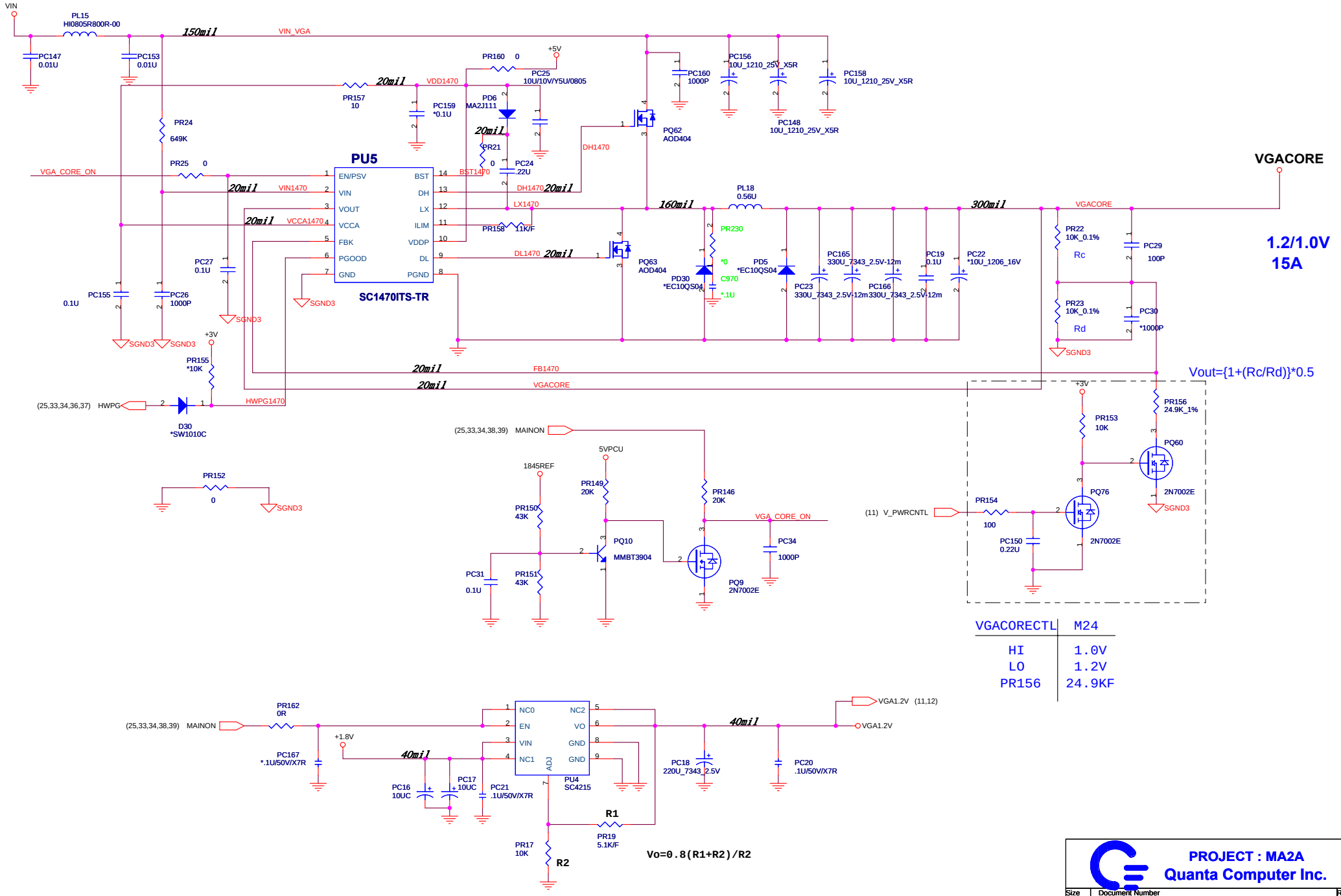


PROJECT : MA2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.8V/0.9V	3A

Date: Thursday, March 17, 2005 Sheet 34 of 39

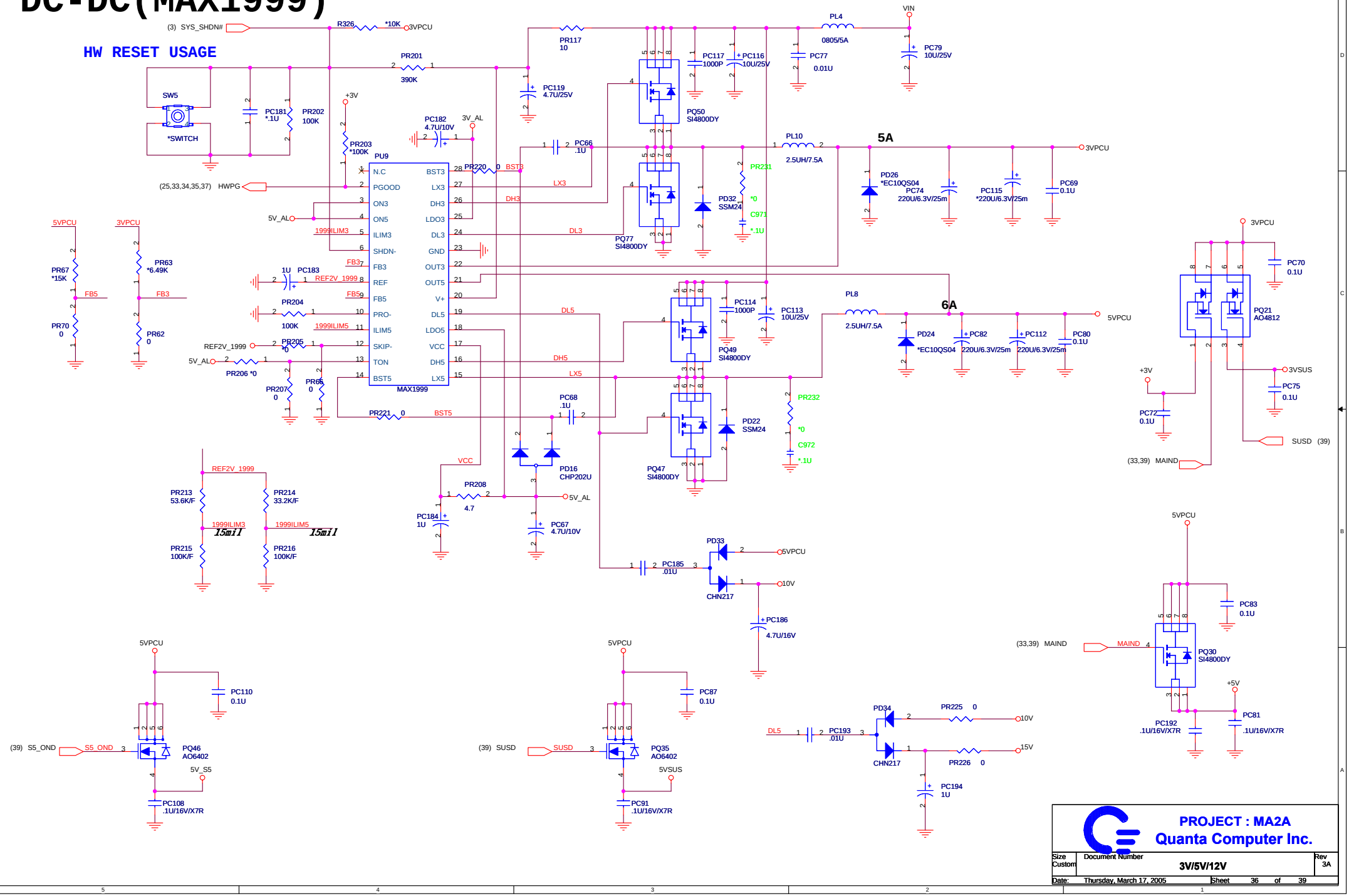
VGA POWER



PROJECT : MA2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA_CORE	3A
Date: Thursday, March 17, 2005	Sheet 35 of 39	

DC-DC(MAX1999)



(21,26,28,31,34,36,39) 5VSUS
(16,18,25,26,29,34,36,38,39) 3VPCU
(2,3,8,10,11,12,13,16,17,18,19,20,22,25,26,28,34,35,36,39) +3V

CPU VCC_CORE (MAX1907)

4ms delay to ICH4-M.

(5,19) IMVP_PWG

(25,33,34,35,36) HWPG

(2) CLK_EN#

(4) CPU_VID5
(4) CPU_VID4
(4) CPU_VID3
(4) CPU_VID2
(4) CPU_VID1
(4) CPU_VID0

0.748V for suspend mode (Deeper sleep)

(19) DPRSLPVR

(2,19) STP_CPU#

(25,34,39) VRON

MAX1907AETL

PJ1 SHORT

CPU_CORE
0.844V ~ 1.356V
27A

CPU_CORE (4,39)

VIN (16,33,34,35,36,38,39)

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	1	0	1.612V
1	0	0	1	1	1	1.084V	0	0	0	1	1	1	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	0	1	1.052V	0	0	1	0	0	1	1.564V
1	0	1	0	1	0	1.036V	0	0	1	0	1	0	1.548V
1	0	1	0	1	1	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	0	0	1.004V	0	0	1	1	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	0	1	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	0	1	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	0	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	1	0	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V

SUSPEND MODE (SUS=HIGH)

S2	S1	S0	Output
OPEN	VCC	GND	0.748V

VCC_BOOT

B2	B1	B0	Output
GND	GND	GND	1.708V
REF	REF	REF	1.372V
OPEN	OPEN	OPEN	1.036V
VCC	VCC	VCC	0.700V
REF	VCC	VCC	1.212V

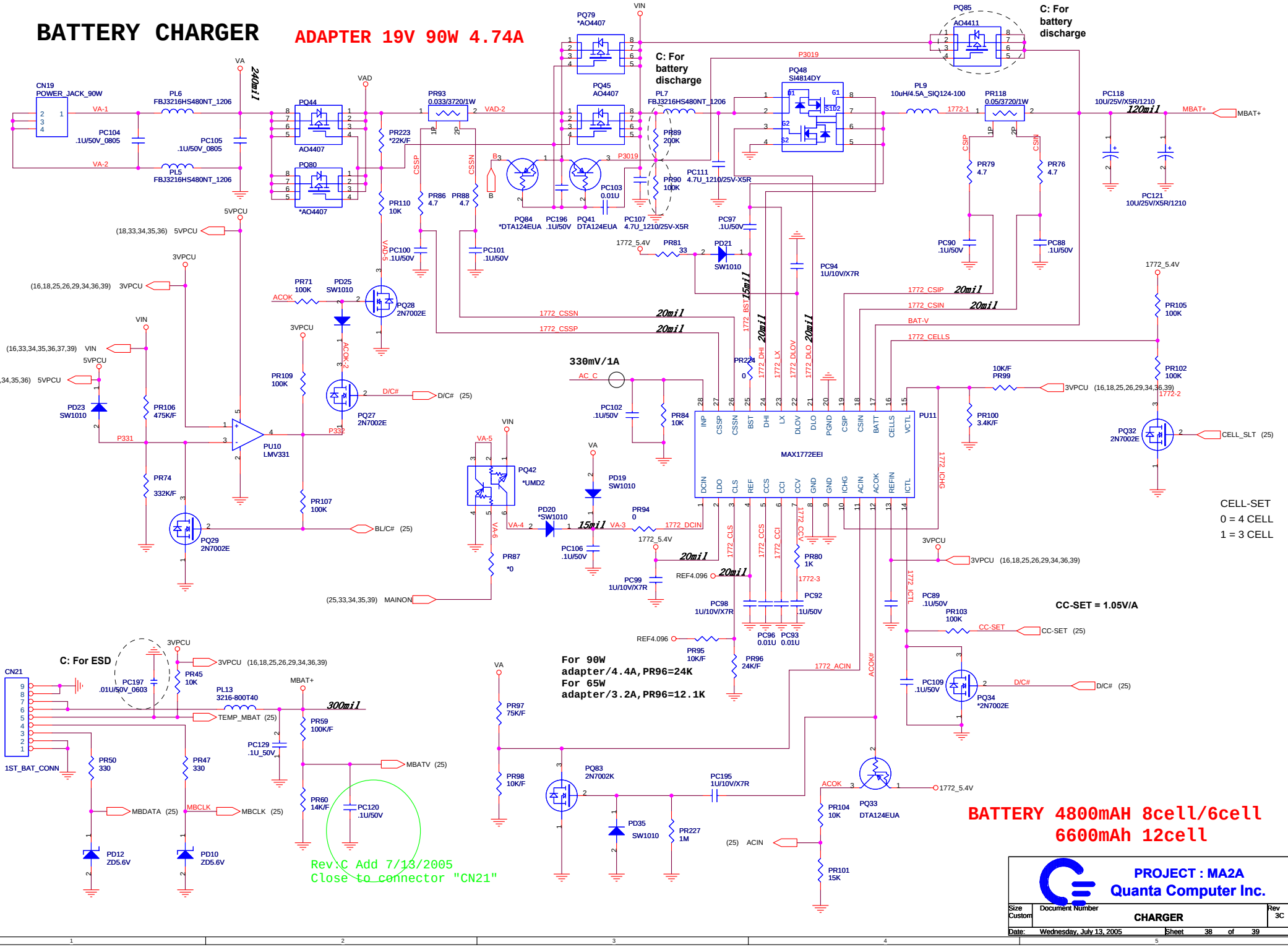
For Yonah

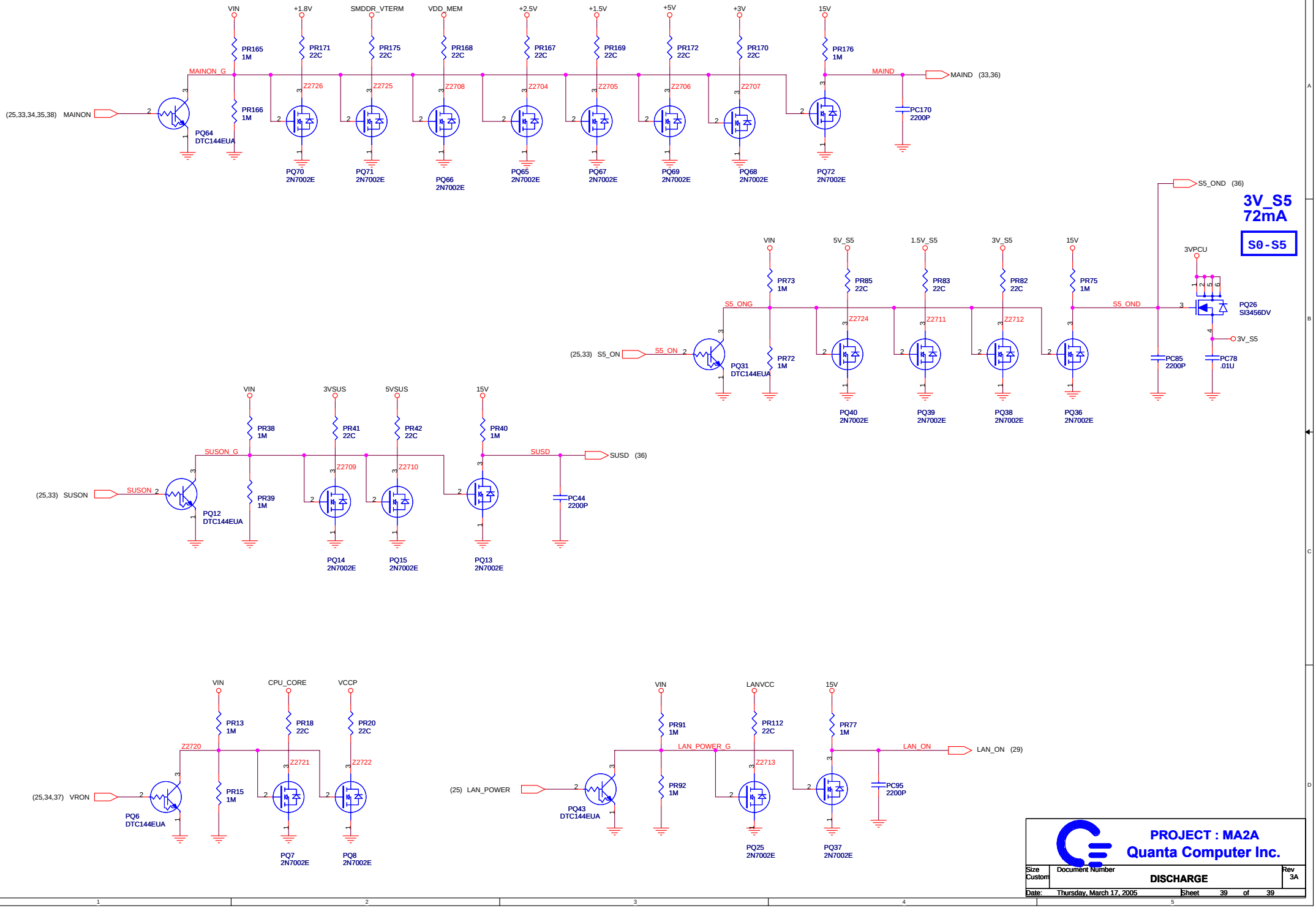
PROJECT : MA2A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	3A
Date: Thursday, March 17, 2005	Sheet 37 of 39	

BATTERY CHARGER

ADAPTER 19V 90W 4.74A




VIN
+1.8V
SMDDR_VTERM
VDD_MEM
+2.5V
+1.5V
+5V
+3V
15V
PR165 1M
PR171 22C
PR175 22C
PR168 22C
PR167 22C
PR169 22C
PR172 22C
PR170 22C
PR176 1M
MAINON_G
MAIND
MAIND (33,36)
(25,33,34,35,38) MAINON
PR166 1M
PC170 2200P
PQ64 DTC144EUA
Z2726
Z2725
Z2708
Z2704
Z2705
Z2706
Z2707
PQ70 2N7002E
PQ71 2N7002E
PQ66 2N7002E
PQ65 2N7002E
PQ67 2N7002E
PQ69 2N7002E
PQ68 2N7002E
PQ72 2N7002E
S5_OND (36)
3V_S5
72mA
S0-S5
VIN
5V_S5
1.5V_S5
3V_S5
15V
3VPCU
PR73 1M
PR85 22C
PR83 22C
PR82 22C
PR75 1M
S5_ONG
S5_OND
PQ26 SI3456DV
3V_S5
(25,33) S5_ON
S5_ON
PR72 1M
PC85 2200P
PC78 .01U
PQ31 DTC144EUA
Z2724
Z2711
Z2712
PQ40 2N7002E
PQ39 2N7002E
PQ38 2N7002E
PQ36 2N7002E
VIN
3VSUS
5VSUS
15V
PR38 1M
PR41 22C
PR42 22C
PR40 1M
SUSON_G
SUSD
SUSD (36)
(25,33) SUSON
SUSON
PR39 1M
PC44 2200P
PQ12 DTC144EUA
Z2709
Z2710
PQ14 2N7002E
PQ15 2N7002E
PQ13 2N7002E
VIN
CPU_CORE
VCCP
PR13 1M
PR18 22C
PR20 22C
Z2720
Z2721
Z2722
(25,34,37) VRON
PR15 1M
PQ6 DTC144EUA
PQ7 2N7002E
PQ8 2N7002E
VIN
LANVCC
15V
PR91 1M
PR112 22C
PR77 1M
LAN_POWER_G
LAN_ON
LAN_ON (29)
(25) LAN_POWER
PR92 1M
PC95 2200P
PQ43 DTC144EUA
Z2713
PQ25 2N7002E
PQ37 2N7002E
PROJECT : MA2A
Quanta Computer Inc.
Size Custom
Document Number
DISCHARGE
Rev 3A
Date: Thursday, March 17, 2005
Sheet 39 of 39