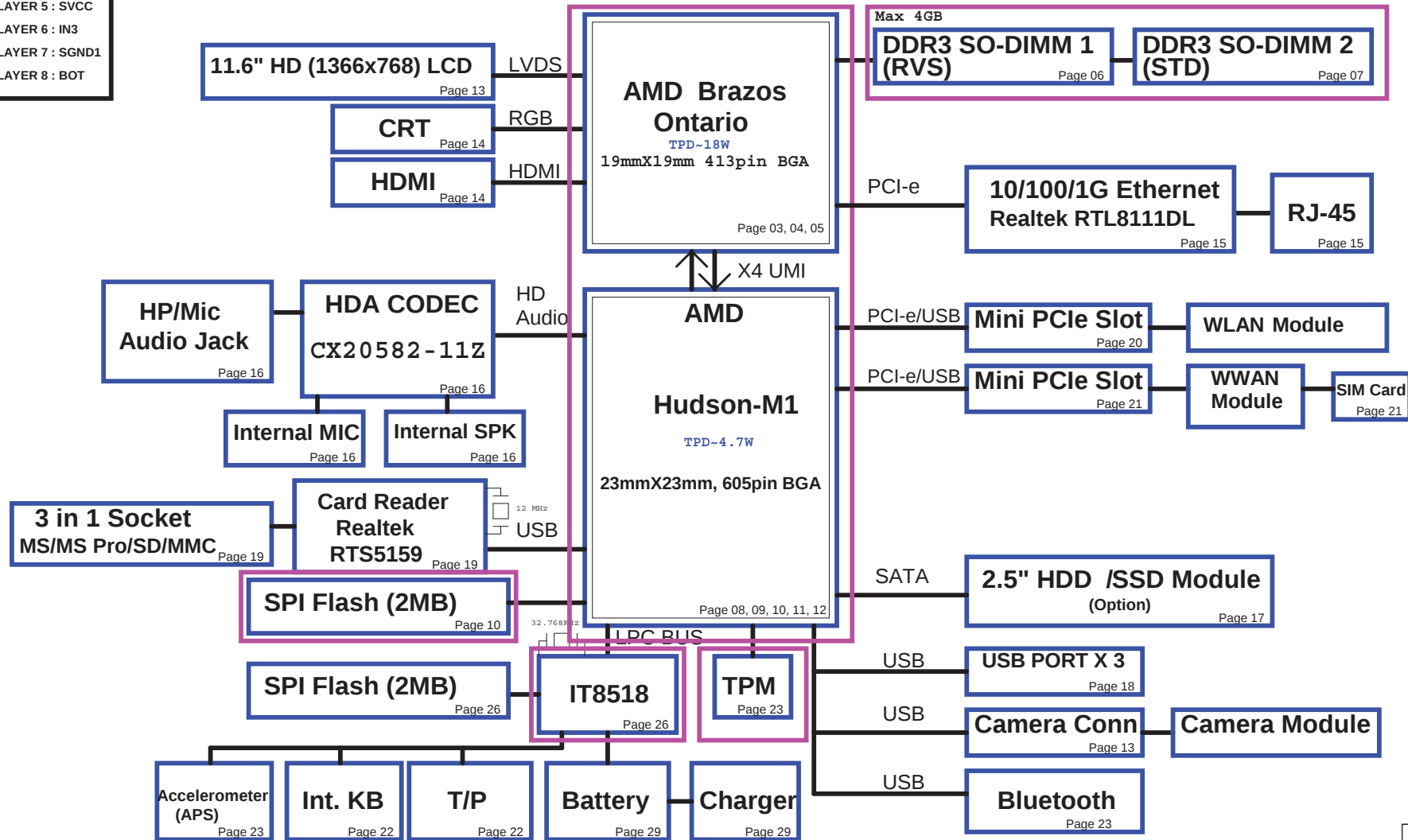


MK-2.0 & Dublin-1.5B Block Diagram -- AMD Ontario

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT



POWER

DC/DC 3V_PCU, 5V_PCU, +15V	Page 30
REGULATOR (DDR3) 1.5V_SUS, 0.75V_DDR_VTT	Page 31
REGULATOR +1V	Page 32
REGULATOR 1.1V_S5, +1.1V	Page 33
REGULATOR +1.8V	Page 34
CPU Core	Page 35
RUN POWER SW 3V_SUS, 5V_SUS, 3V_S5, 5V_S5 +3V, +5V	Page 36
Discharge	Page 36

Power Sequence

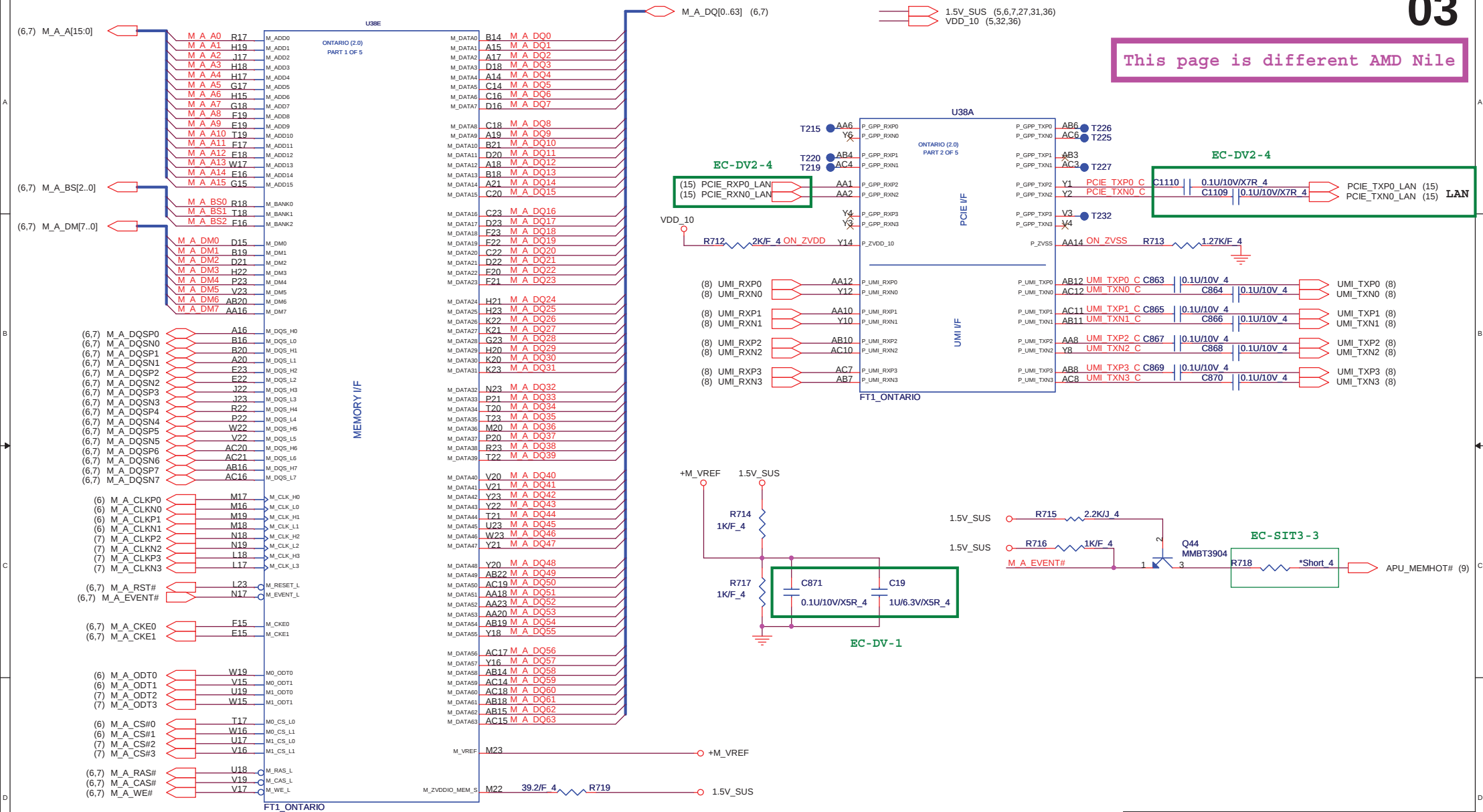
The diagram illustrates the power sequence for the system. The signals shown are:

- AC IN
- 3V/5VPCU
- NBSWON#
- DNBSWON#
- S5_ON/S5
- RSMRST#
- PCIE_WAKE#
- SUSC
- USB
- SUSON
- MAINON
- VR_ON
- CPU_CORE
- VRM_PWRGD
- HWPG
- ECPWROK
- SB_PWRGD_IN
- CPU RESET
- CPU POWER OK

SB820 SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD22 AE22	DDR / RFID
SB_SMBCLK1 SB_SMBDATA1 (+3V_S5)	F5 F4	not used
SB_SCLK2 SB_SDATA2 (+3V_S5)	D25 F23	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal

This page is different AMD Nile



Quanta Computer Inc.

PROJECT : MK2.0

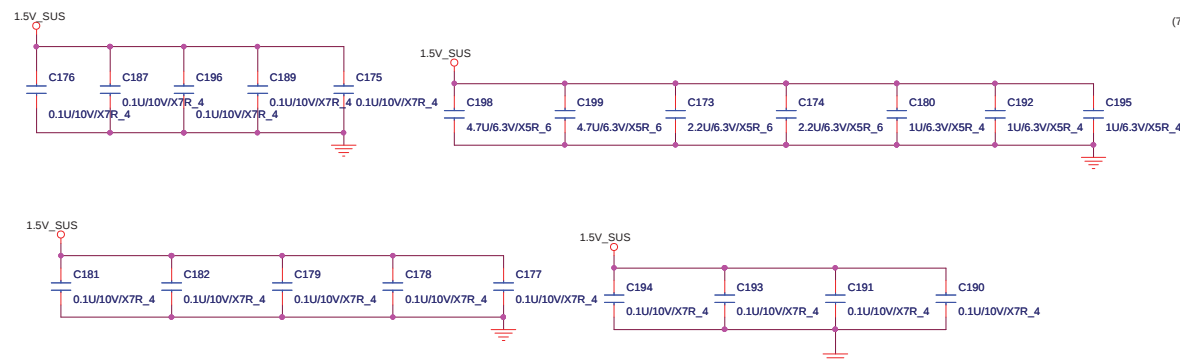
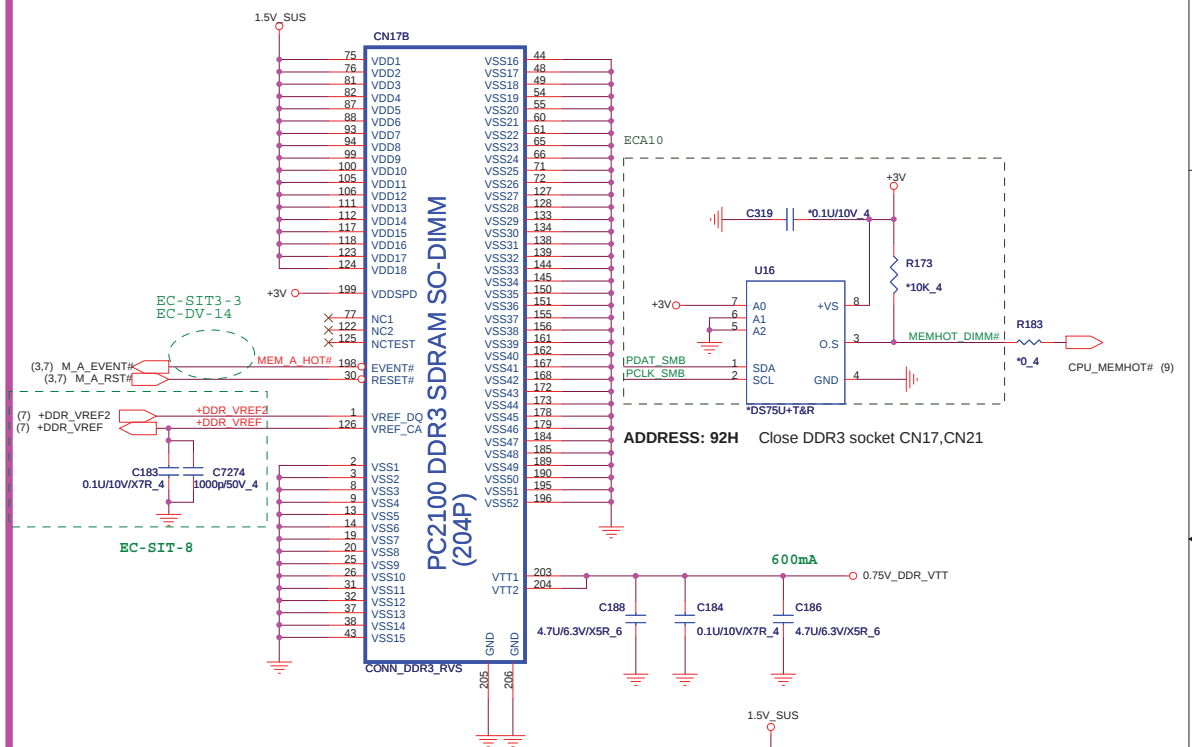
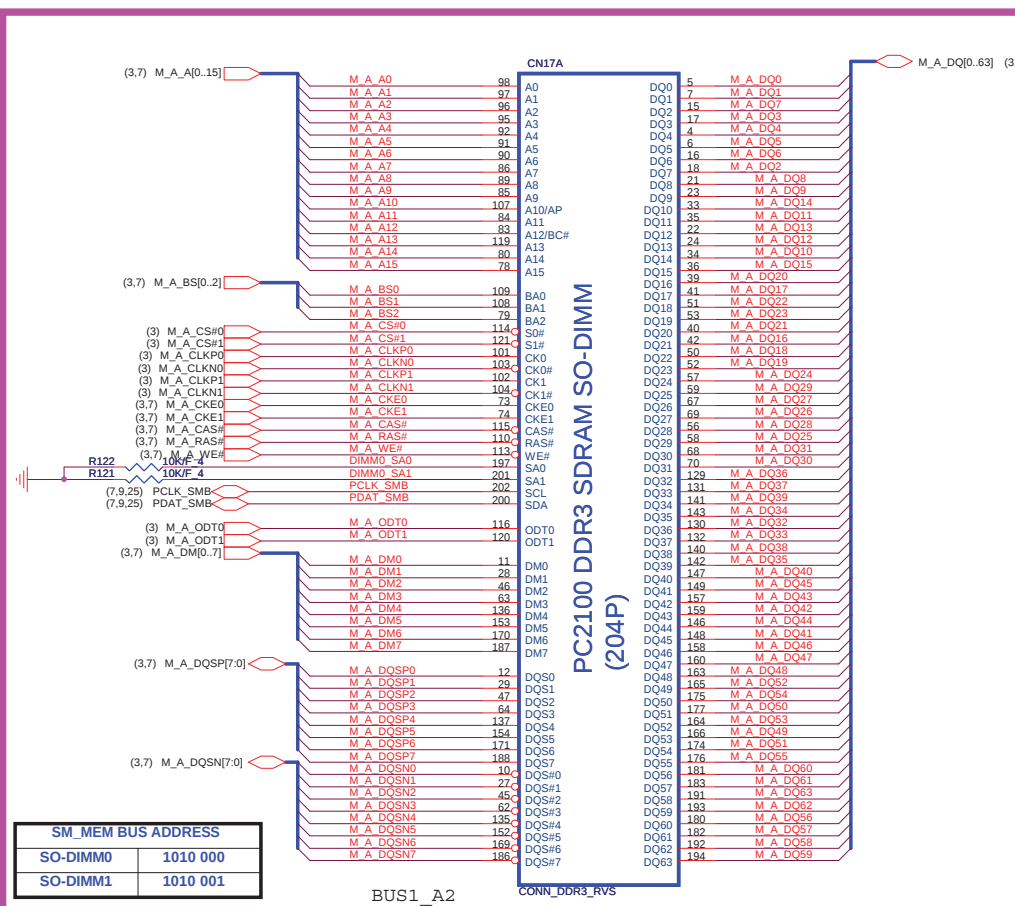
Size	Document Number	Rev
	ONTARIO MEM & PCIe I/F(1/3)	1A

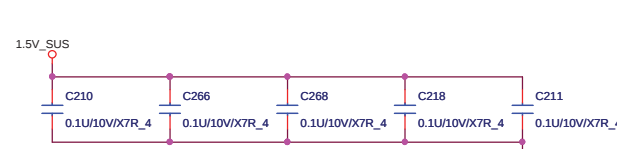
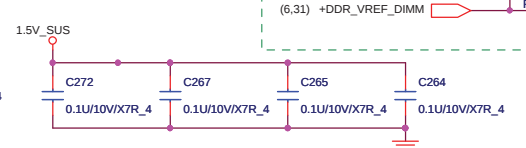
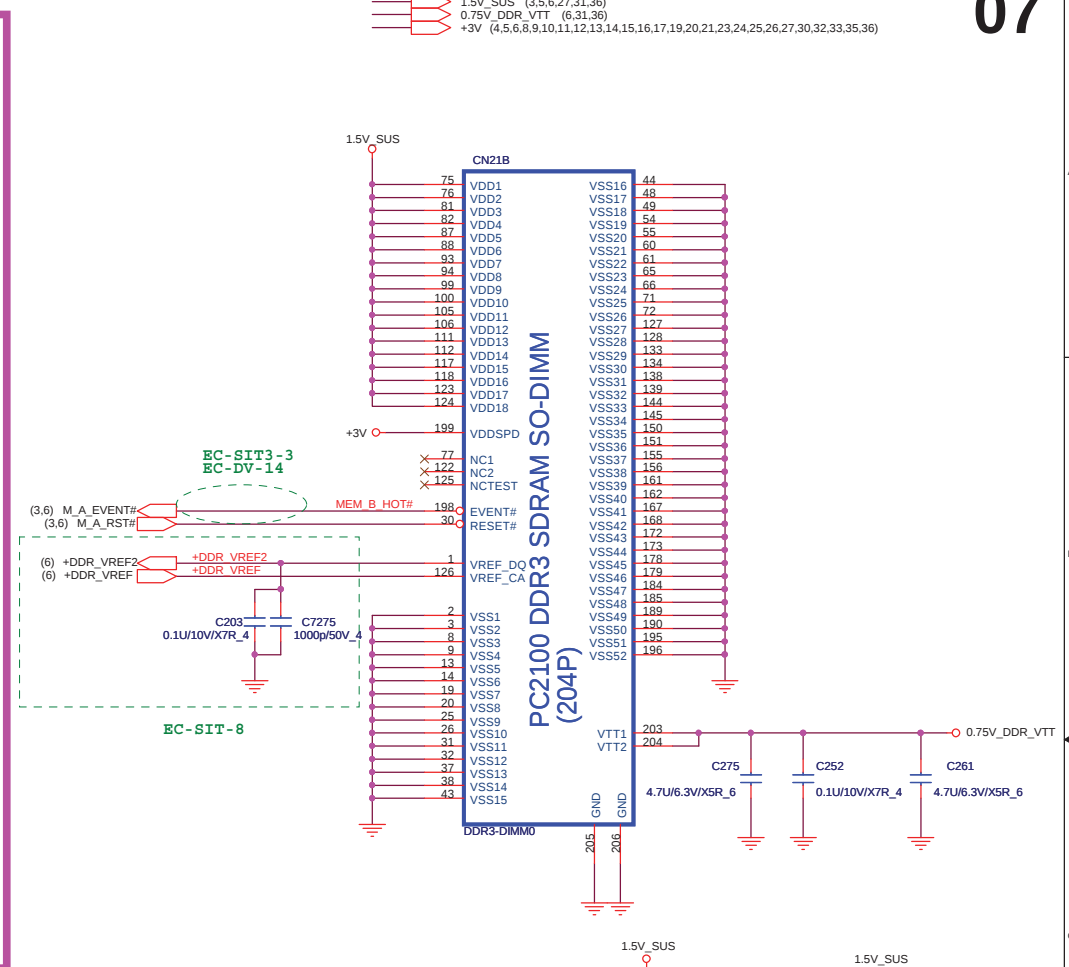
Date: Friday, October 29, 2010 Sheet 3 of 47

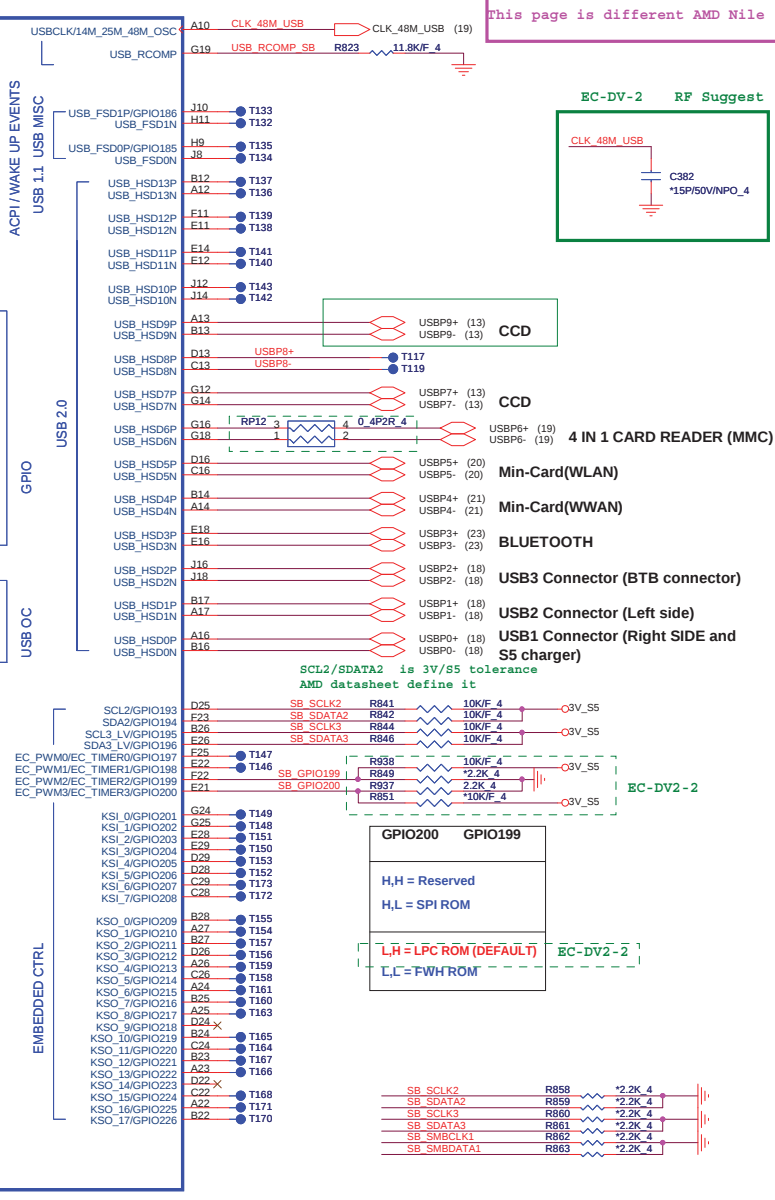
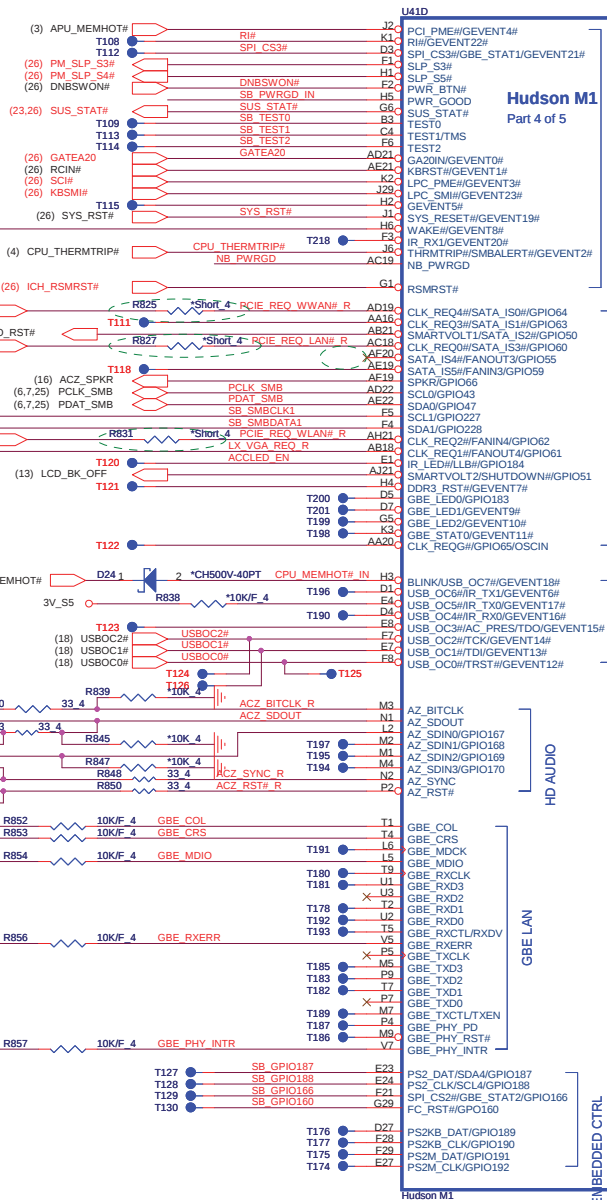
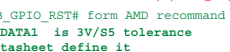
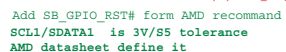


1.5V_SUS (3.5,7,27,31,36)
+DDR_VREF_DIMM (7,31)
0.75V_DDR_VTT (7,31,36)

+3V (4,5,7,8,9,10,11,12,13,14,15,16,17,19,20,21,23,24,25,26,27,30,32,33,35,36)







PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

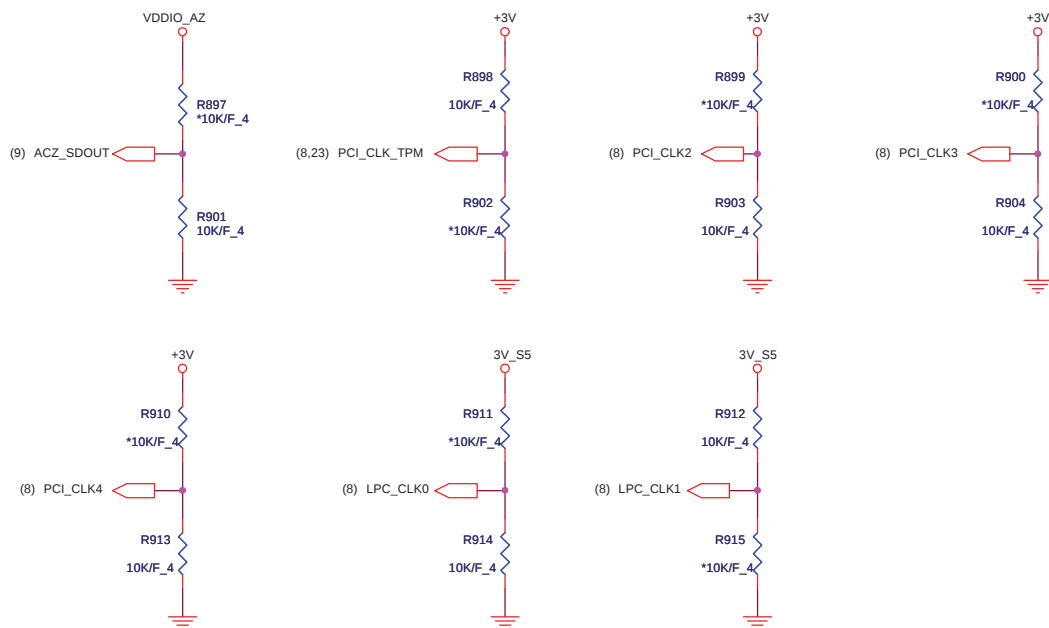




OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

internal have pull
Hi 10K , confirm AMD
ward this pull Hi
not need



PCI_CLK4 CPU/NB HT Clock Selection
0 V - Reserved.
3.3 V - Required setting for integrated clock mode.
This strap is not used if the strap CLKGEN is
configured for external clock generator mode.

REQUIRED STRAPS

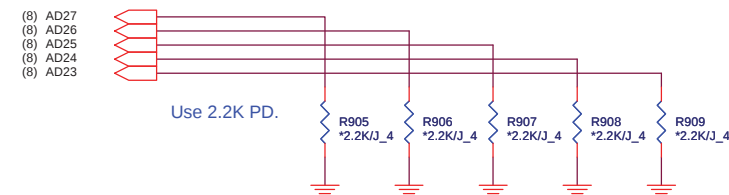
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (Default)	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED	CLKGEN DISABLED	L,H = LPC ROM L,L = FWH ROM	

VDDIO_AZ (11)
+3V (4,5,6,7,8,9,10,11,13,14,15,16,17,19,20,21,23,24,25,26,27,30,32,33,35,36)
3V_S5 (8,9,10,11,18,20,23,25,26,36)

12

DEBUG STRAPS

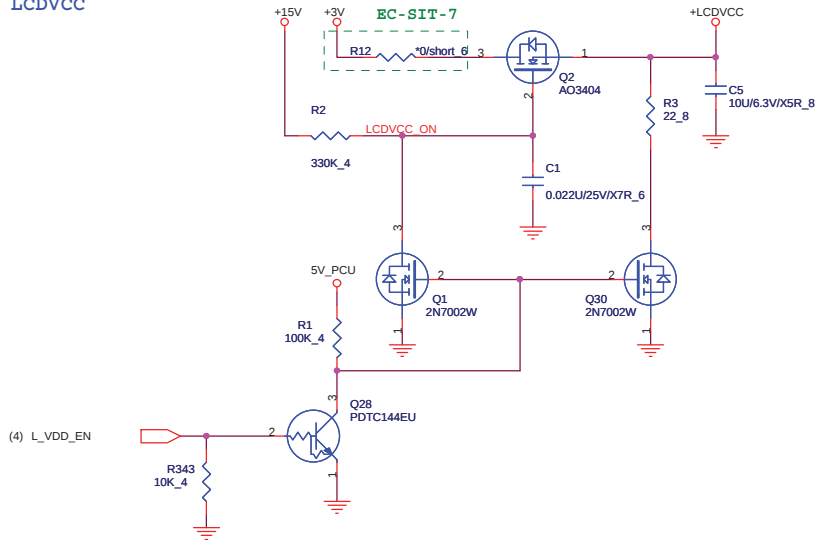
HUDSON-M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



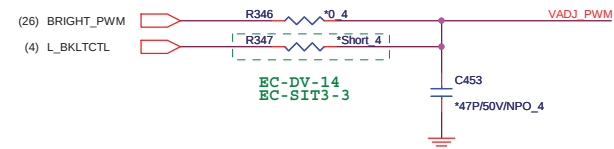
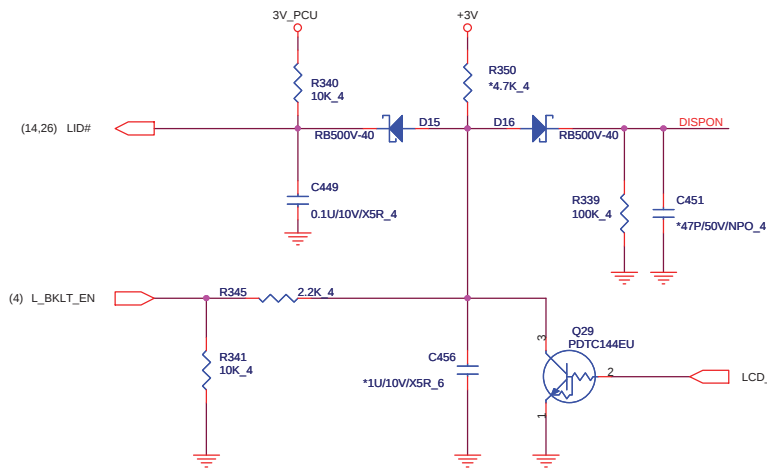
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

+3V (4,5,6,7,8,9,10,11,12,14,15,16,17,19,20,21,23,24,25,26,27,30,32,33,35,36)
 3V_PCU (8,10,14,15,18,25,26,29,30,36)
 +15V (23,30,33,36)
 +5V (14,16,17,22,24,26,27,36)
 VIN (29,30,31,32,33,35,36)
 5V_SUS (25,32,34,35,36)
 5V_PCU (27,29,30,31,33,36)

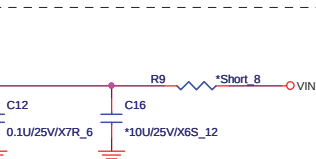
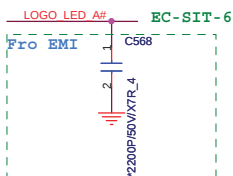
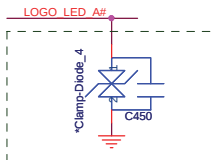
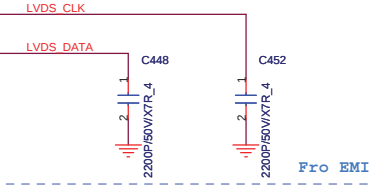
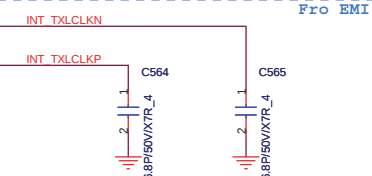
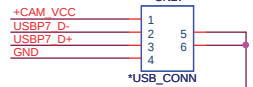
LCDVCC



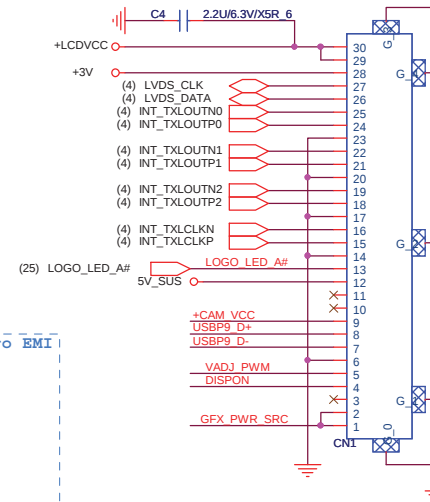
Back light



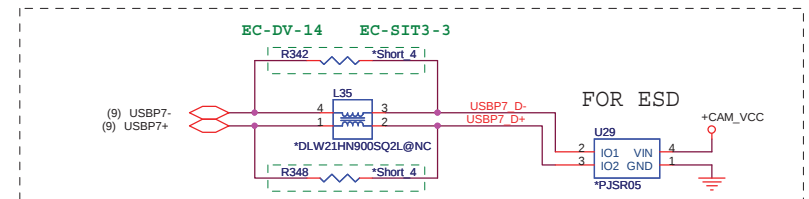
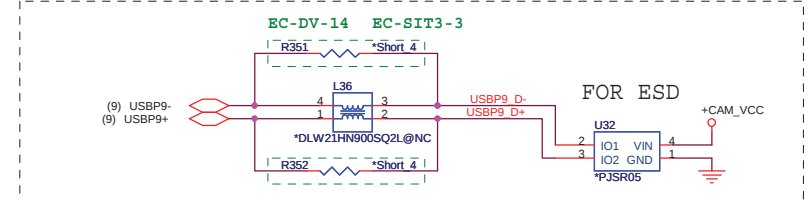
EC-DV2-1



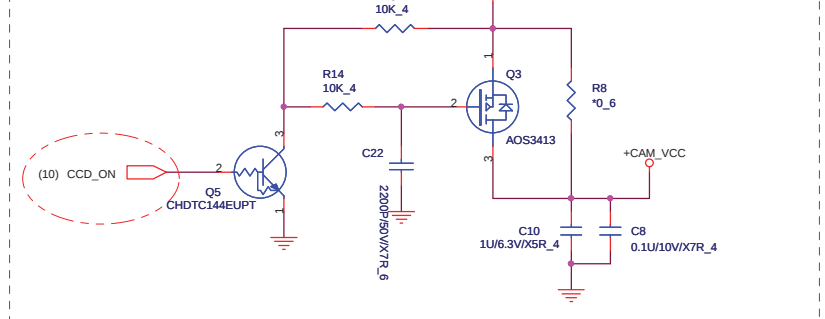
LVD-A30SFY+



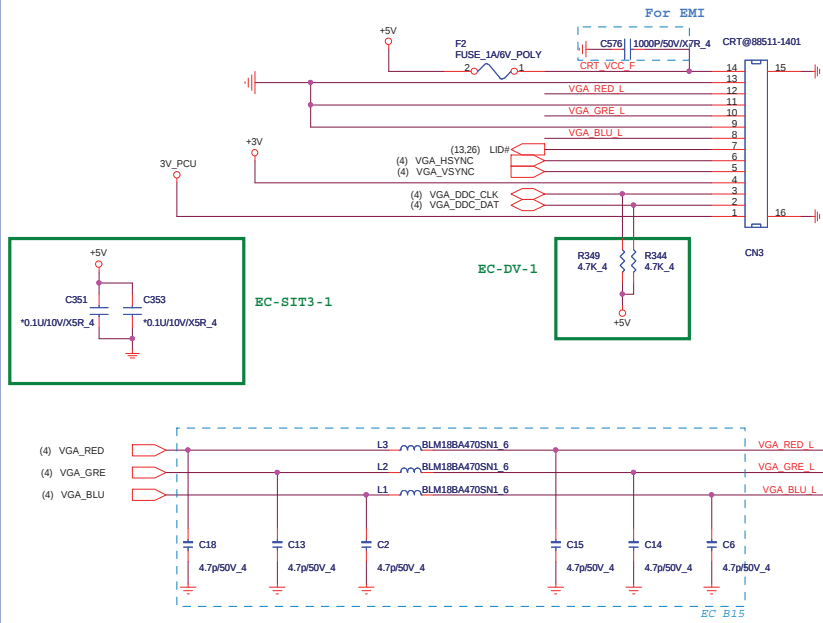
LVDS (11.6")
 (1024x600,
 1366x768)



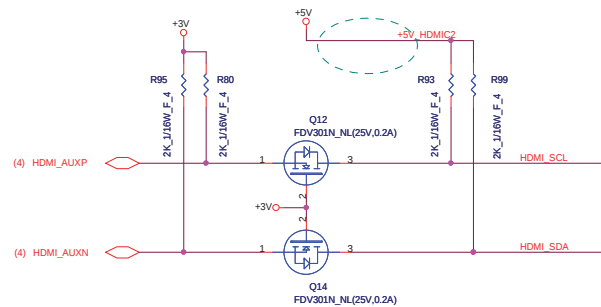
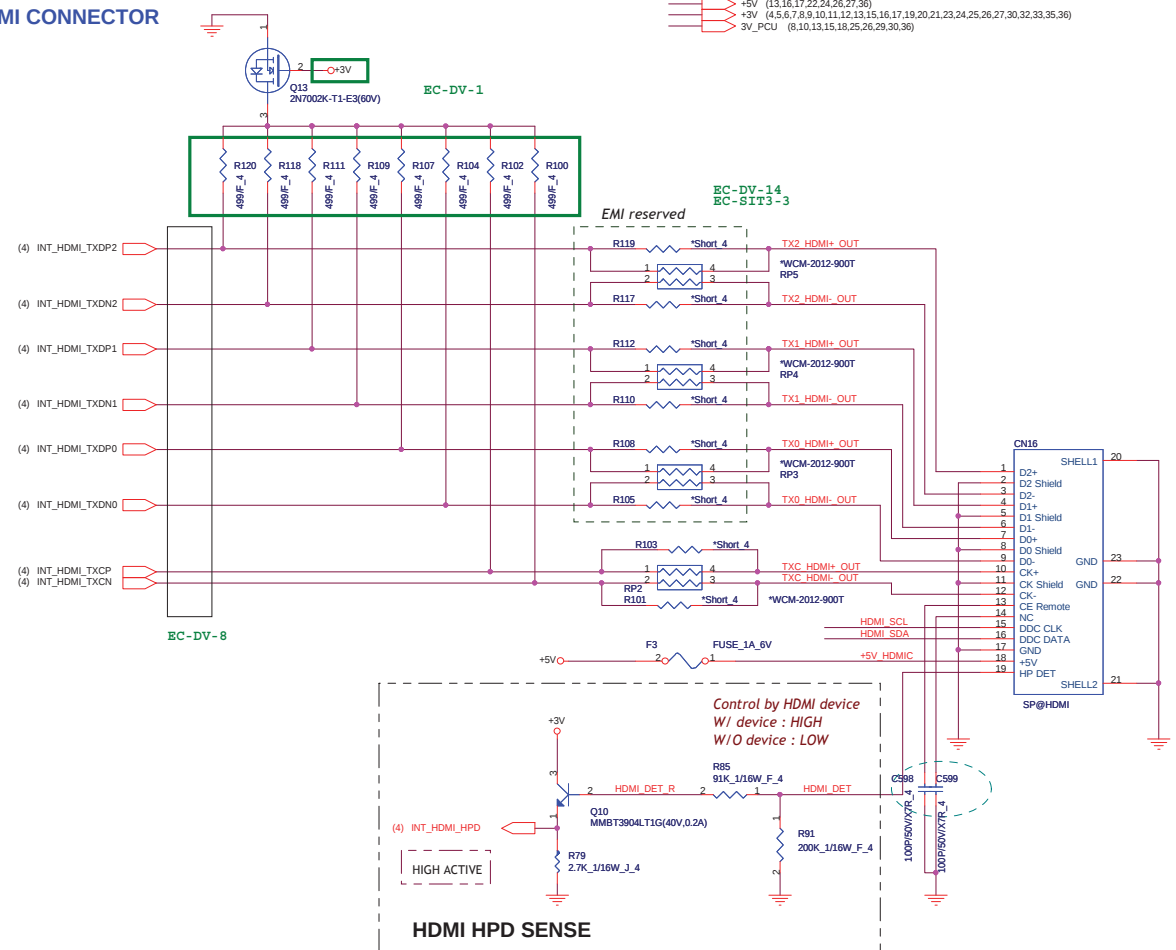
CAMERA VCC Control



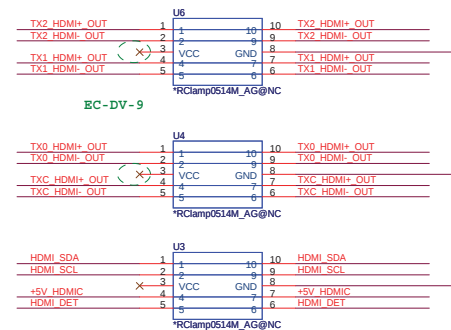
CRT FFC CONNECTOR



HDMI CONNECTOR

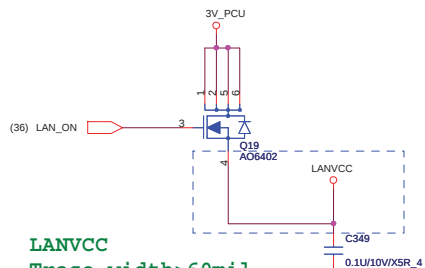


For ESD ---> Layout note: Place close to HDMI Conn

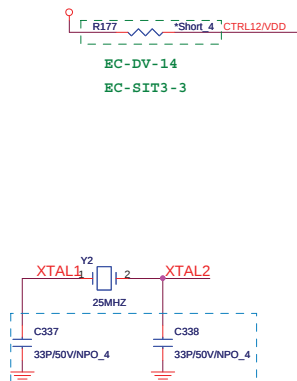


<http://hobi-elektronika.net>

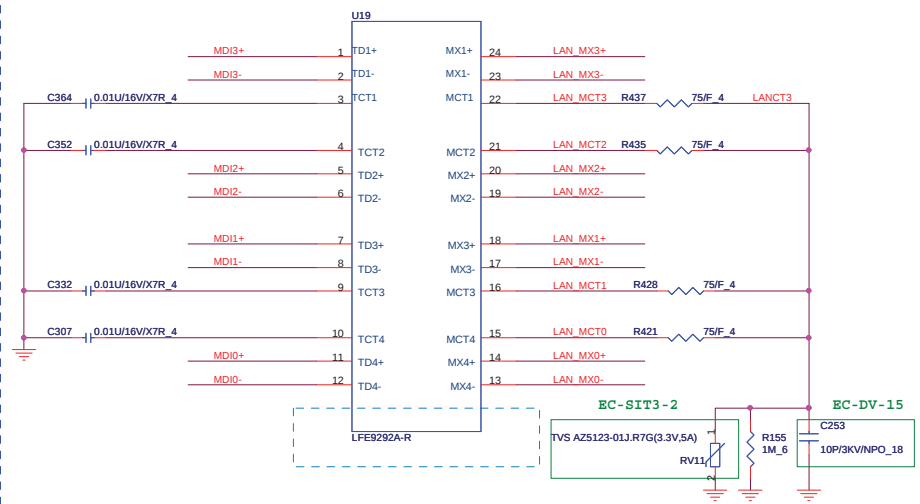
LANVCC



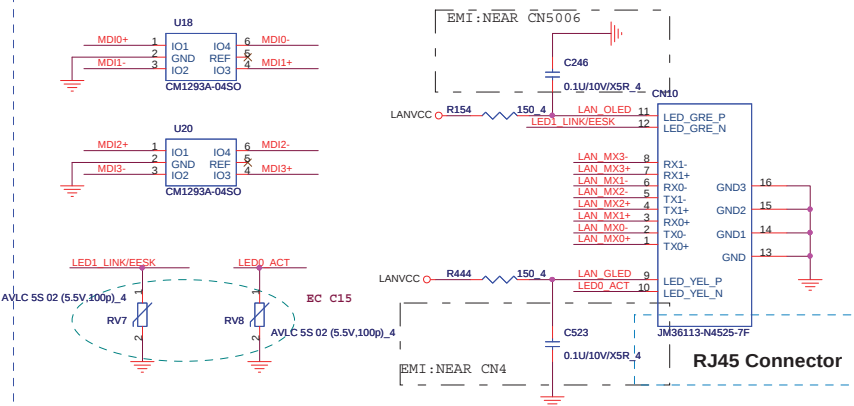
LANVCC



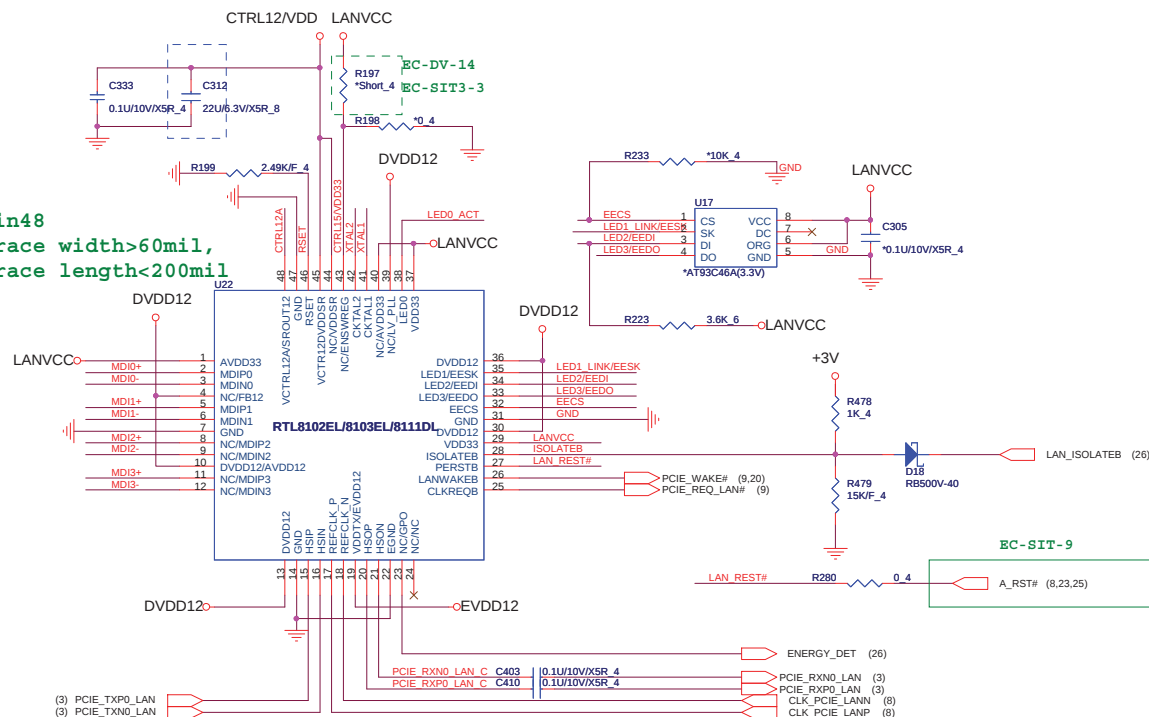
Transformer



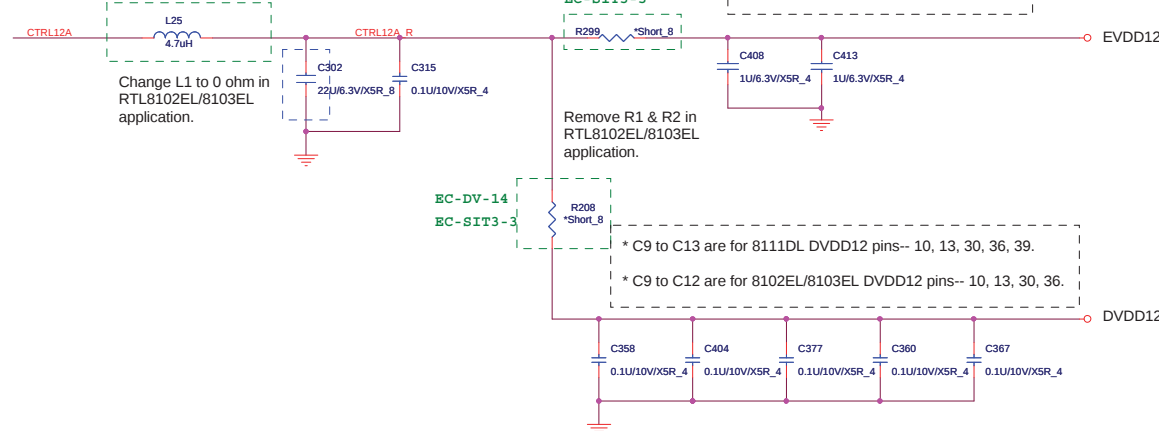
RJ45 Connector



Pin48
Trace width>60mil,
Trace length<200mil



Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.



<http://hobi-elektronika.net>

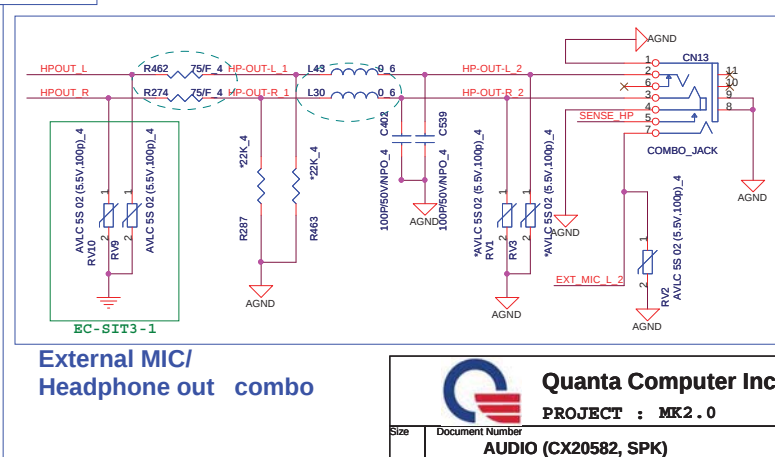
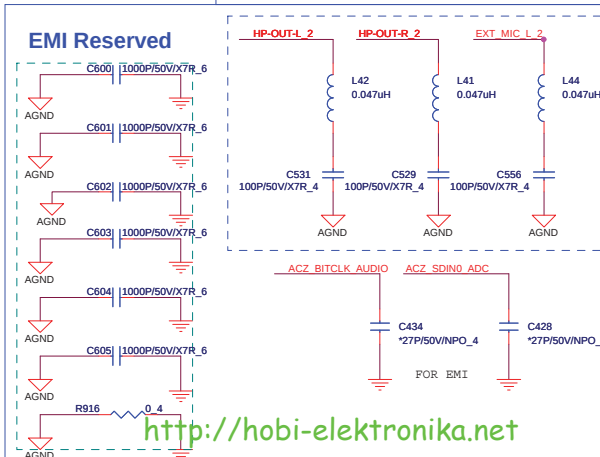
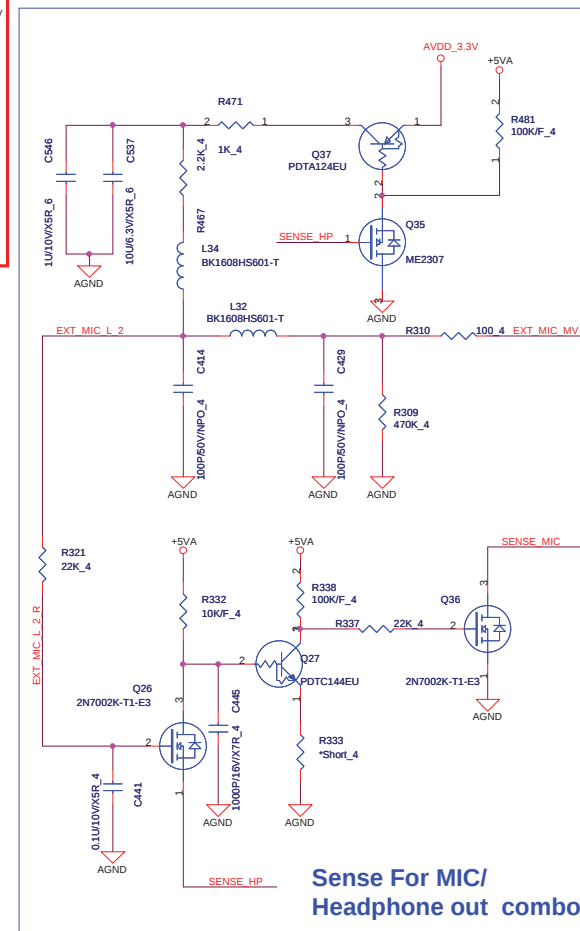
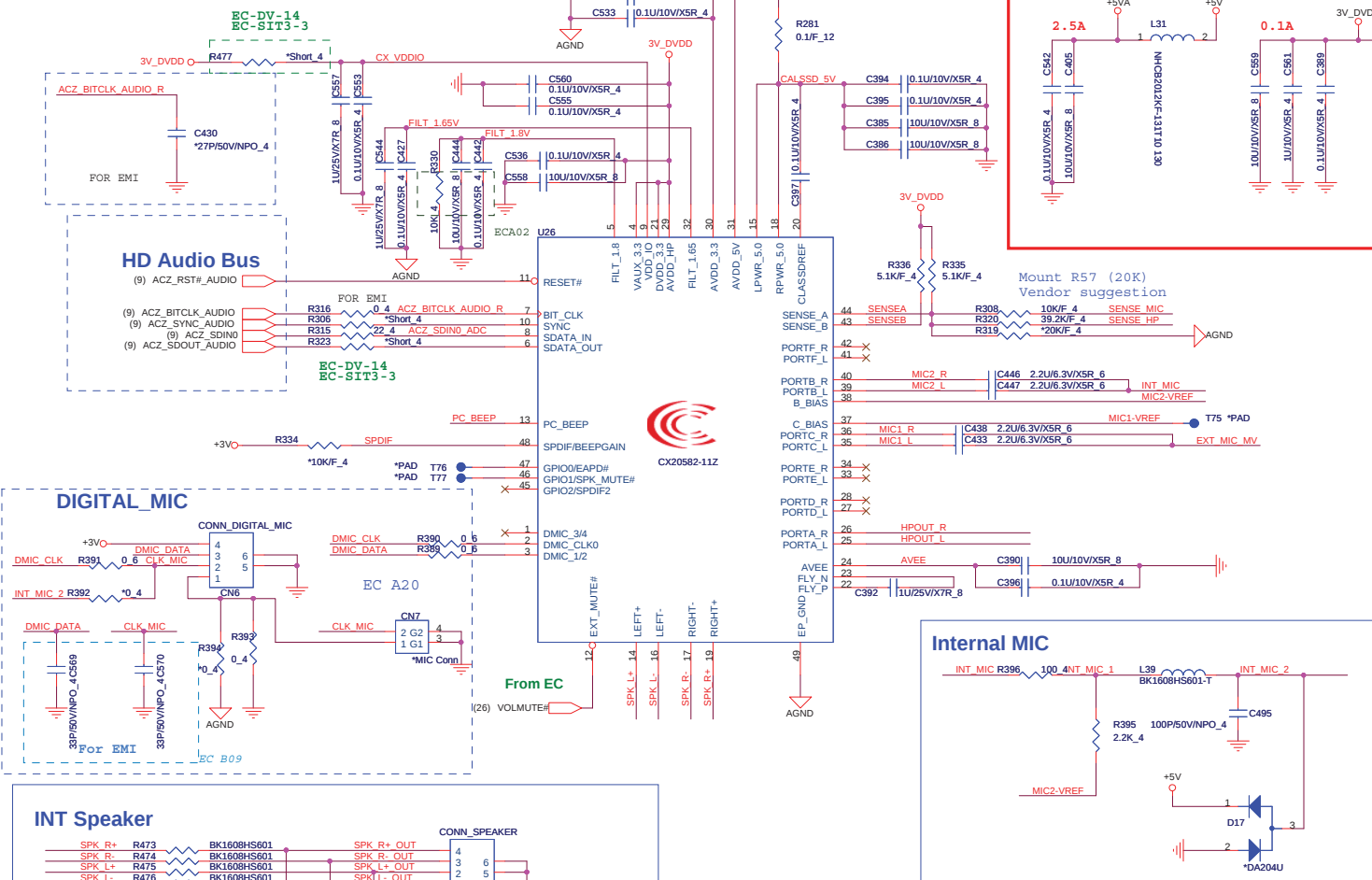
Note:

To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 pins must be powered by a rail that is not removed unless AC power is removed.

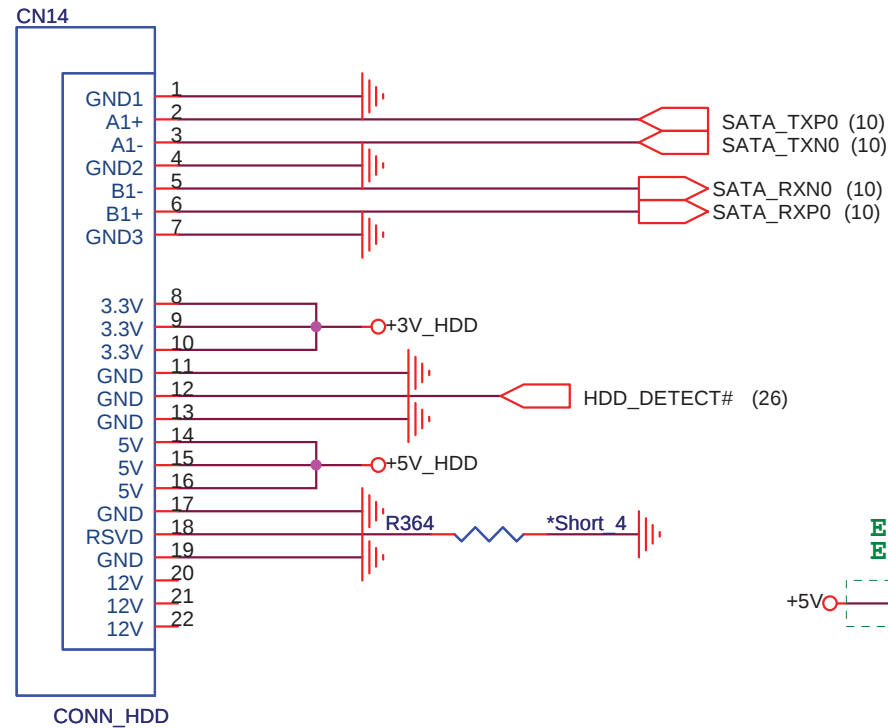
AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.

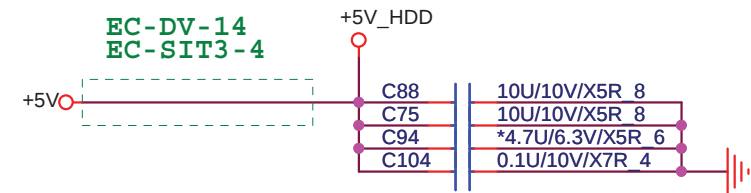
+3V (4,5,6,7,8,9,10,11,12,13,14,15,17,19,20,21,23,24,25,26,27,30,32,33,35,36)
+5V (13,14,17,22,24,26,27,36)



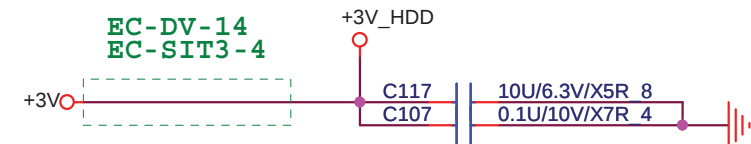
1
+3V (4,5,6,7,8,9,10,11,12,13,14,15,16,19,20,21,23,24,25,26,27,30,32,33,35,36)
+5V (13,14,16,22,24,26,27,36)



DC Current rating: 2 A (MAX)



DC Current rating: 3 A (MAX)



Quanta Computer Inc.

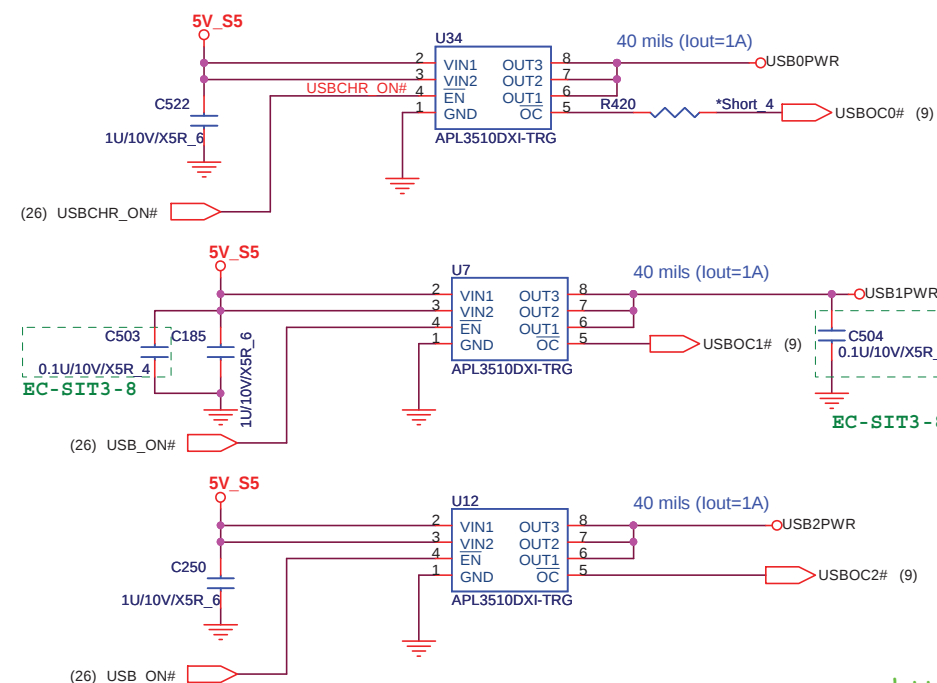
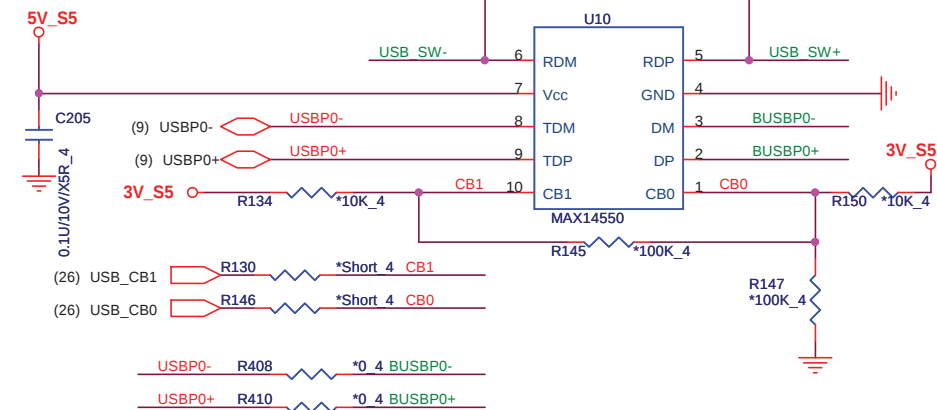
PROJECT : MK2.0

Size	Document Number	Rev
	SATA	1A
Date:	Friday, October 29, 2010	Sheet 17 of 47

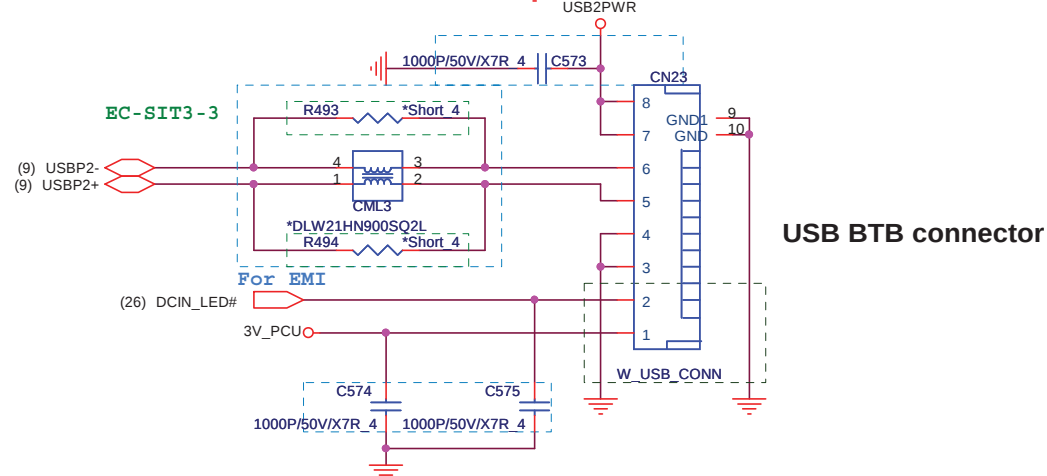
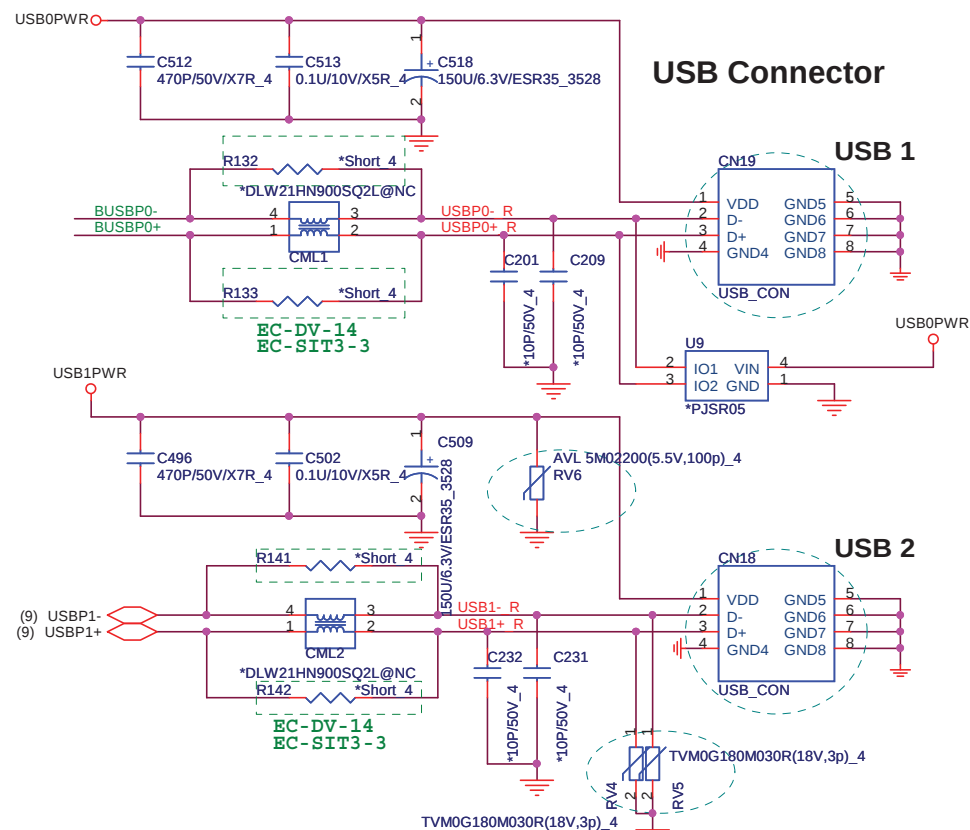
USB SLEEP CHARGE (NEW)

CB0/CB1	Function	Int./Ext. R
0 0	S5 auto detect	Use Int.R
0 1	Blackberry(choice)	NC
1 0	iPod/iPhone(choice)	Use Ext. R
1 1	S0 auto detect	NC

Sleep charger notice



If mount R97, R95, R94.
R102 should mount 49K



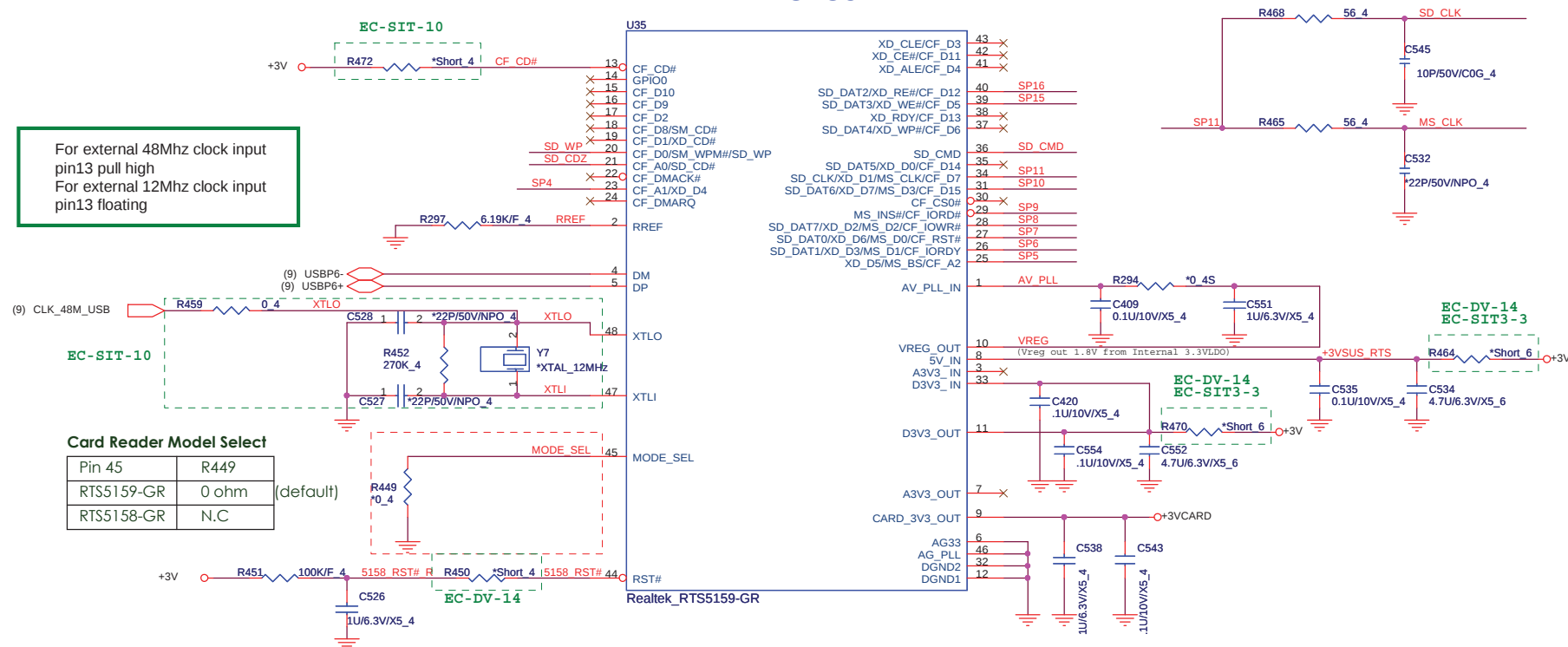
5V_S5 (36)
3V_S5 (8,9,10,11,12,20,23,25,26,36)
5V_SUS (13,25,32,34,35,36)
3V_PCU (8,10,13,14,15,25,26,29,30,36)



Quanta Computer Inc.
PROJECT : MK2.0

Size	Document Number USB x 3	Rev 1A
Date:	Friday, October 29, 2010	Sheet 18 of 47

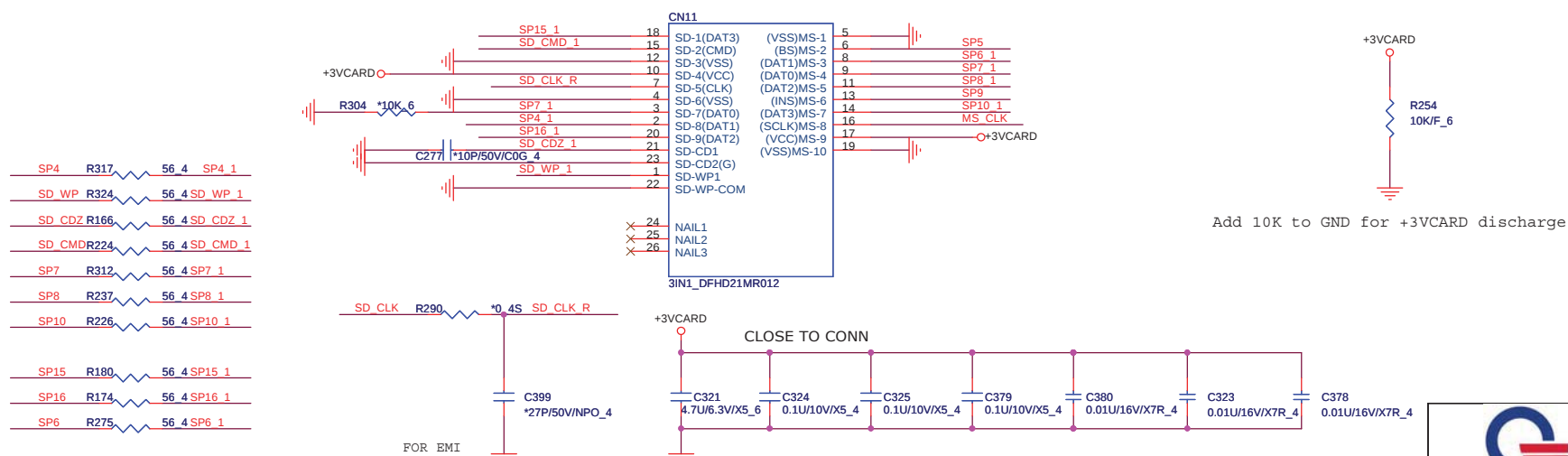
RTL5159



Note:

	SD/MMC	MS
SP0		
SP1		
SP2	SD WP	
SP3	SD CD#	
SP4	SD DAT1	
SP5		MS BS
SP6		MS D1
SP7	SD DAT0	MS D0
SP8	SD DAT7	MS D2
SP9		MS INS#
SP10	SD DAT6	MS D3
SP11	SD CLK	MS SCLK
SP12	SD DAT5	
SP13	SD DAT4	
SP14		
SP15	SD DAT3	
SP16	SD DAT2	
SP17		
SP18		
SP19		

3 IN 1 CARD READER

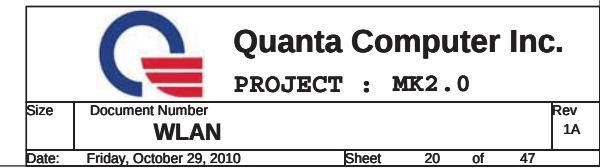


Add 10K to GND for +3VCARD discharge

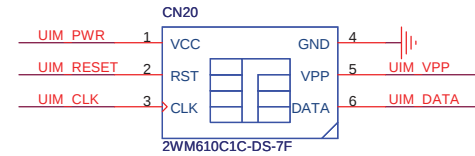
<http://hobi-elektronika.net>

+3V (4,5,6,7,8,9,10,11,12,13,14,15,16,17,20,21,23,24,25,26,27,30,32,33,35,36)

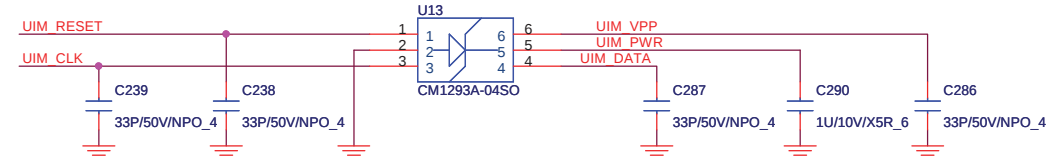




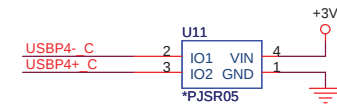
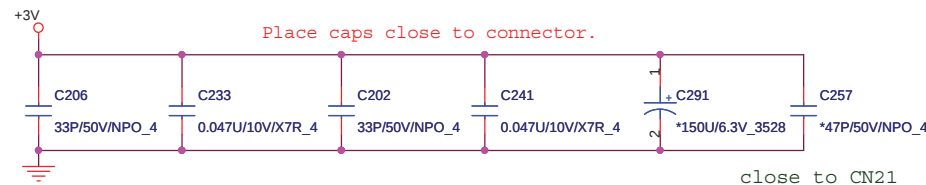
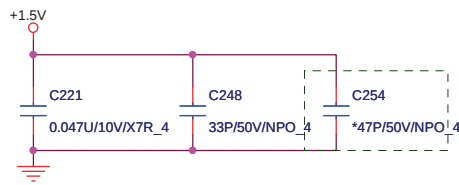
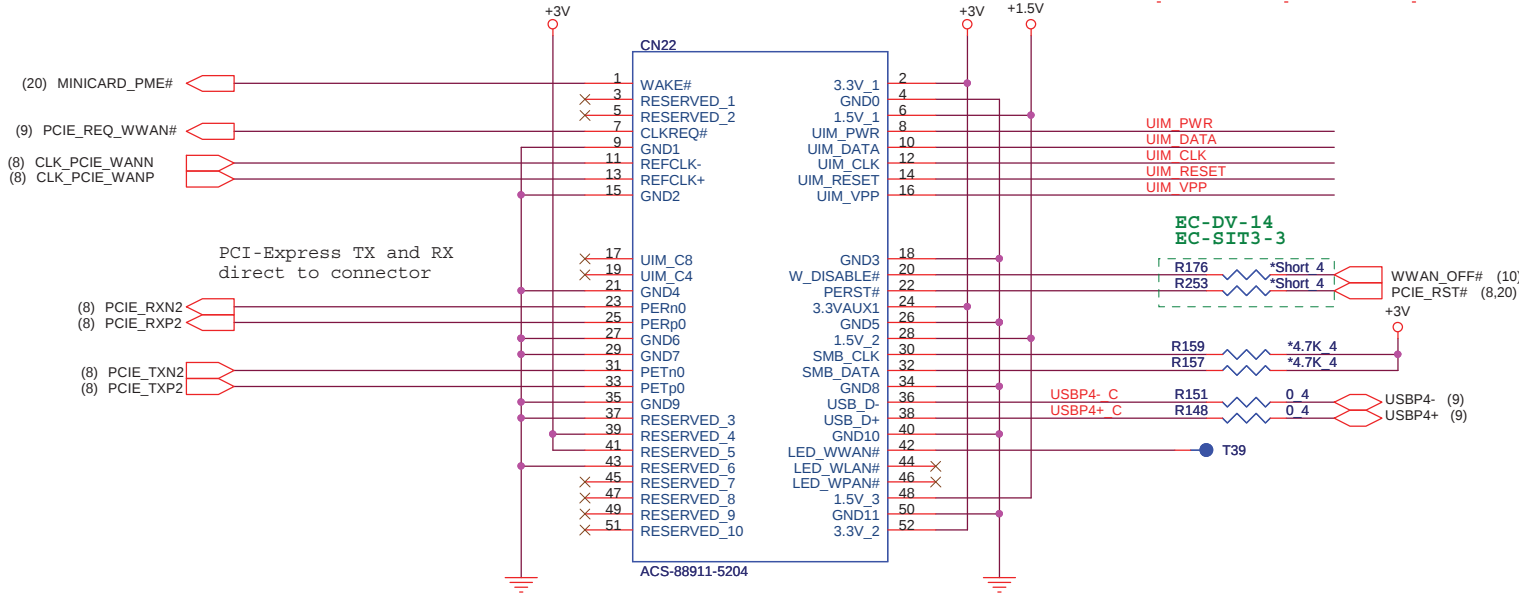
SIM Card CONN



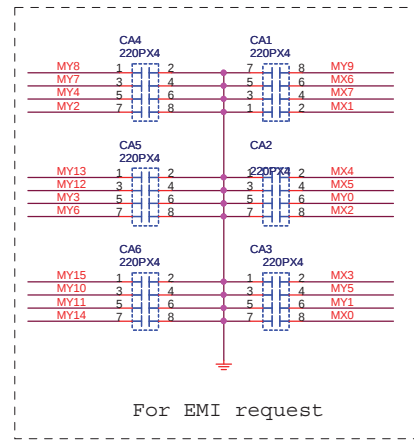
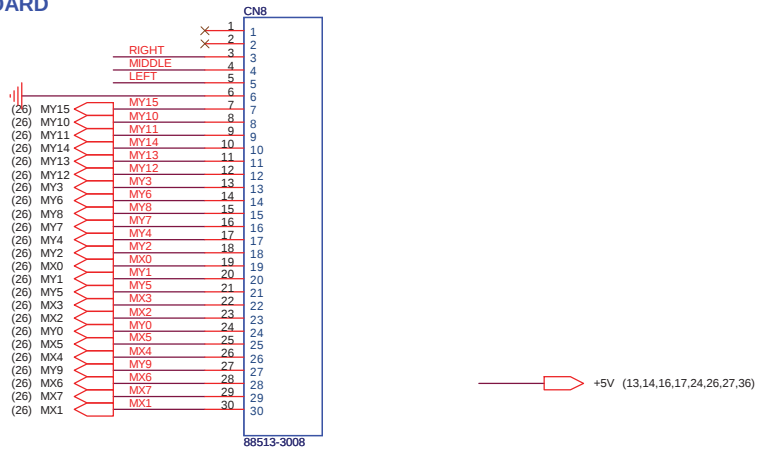
Layout Note:
UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible



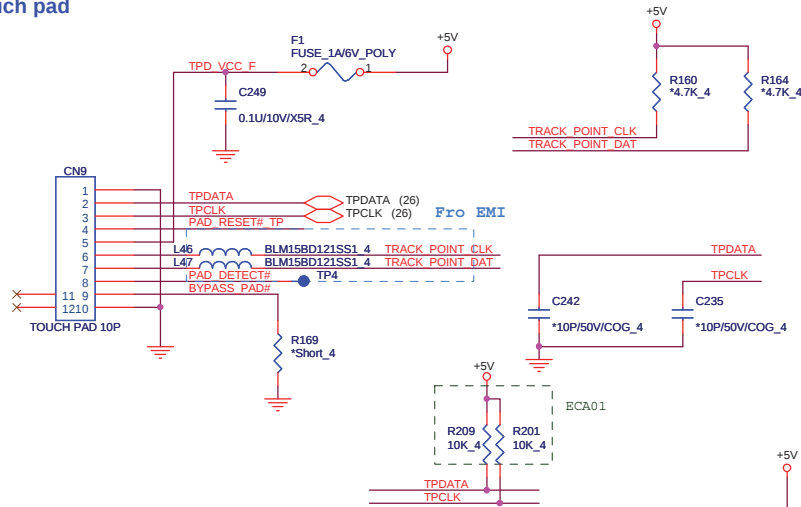
MiniCard WWAN connector



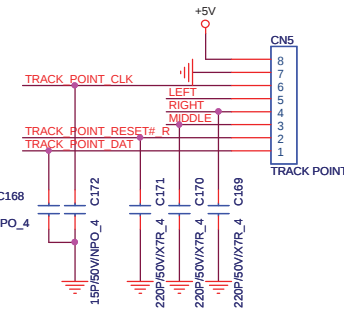
KEYBOARD



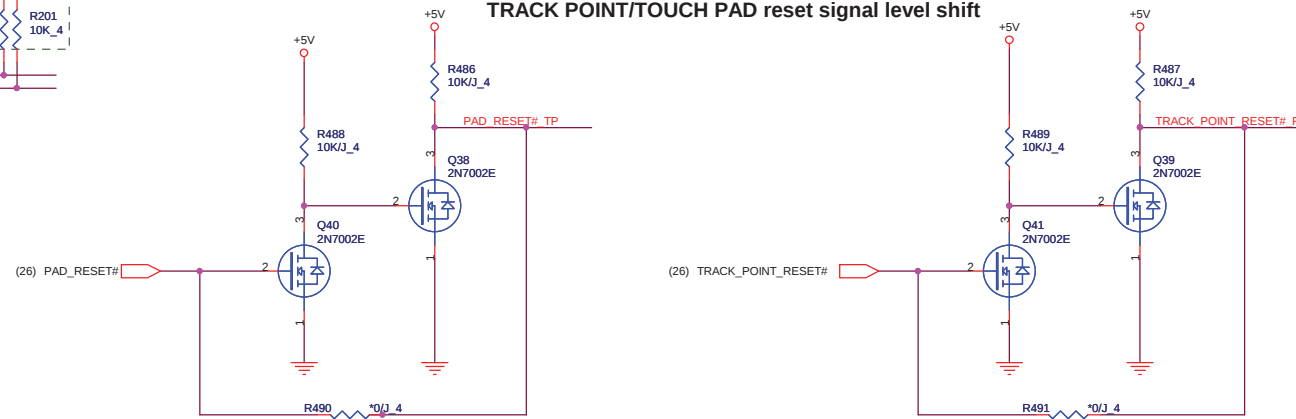
Touch pad



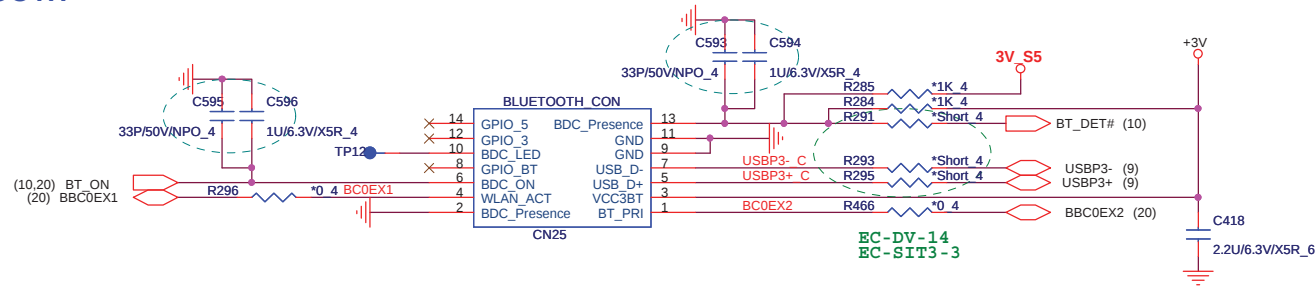
TRACK POINT



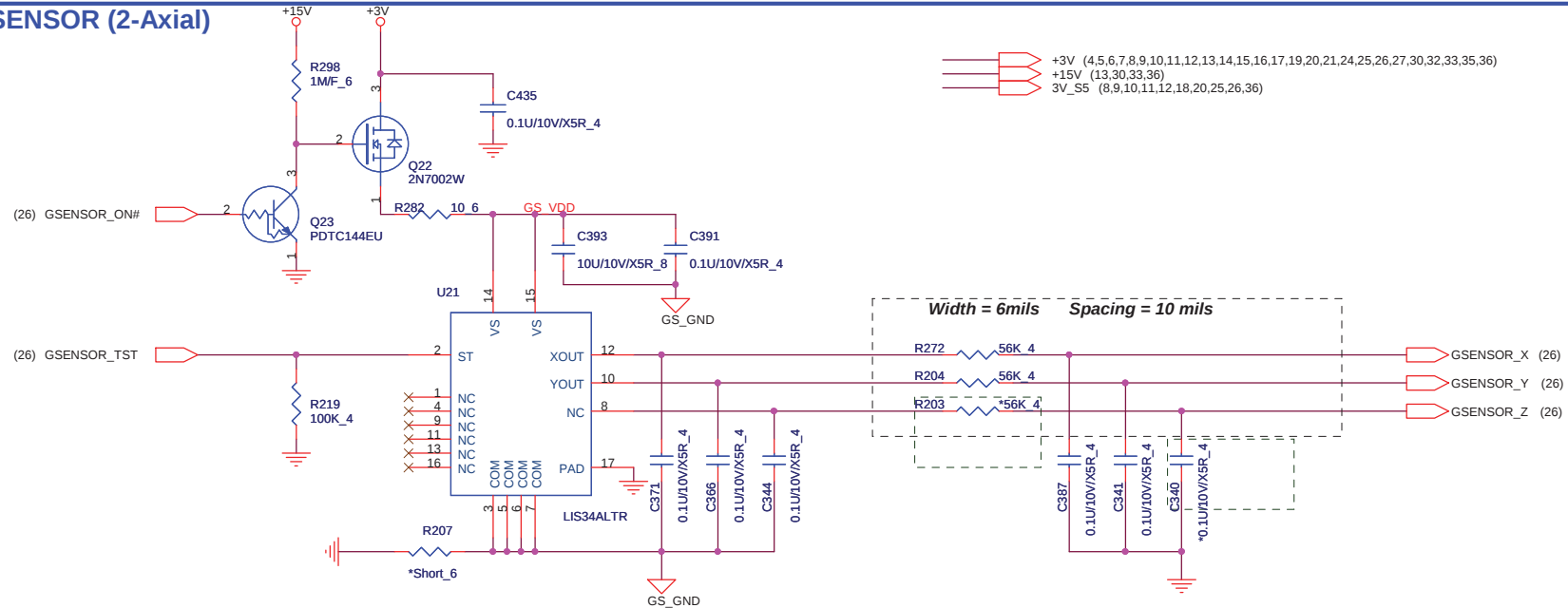
TRACK POINT/TOUCH PAD reset signal level shift



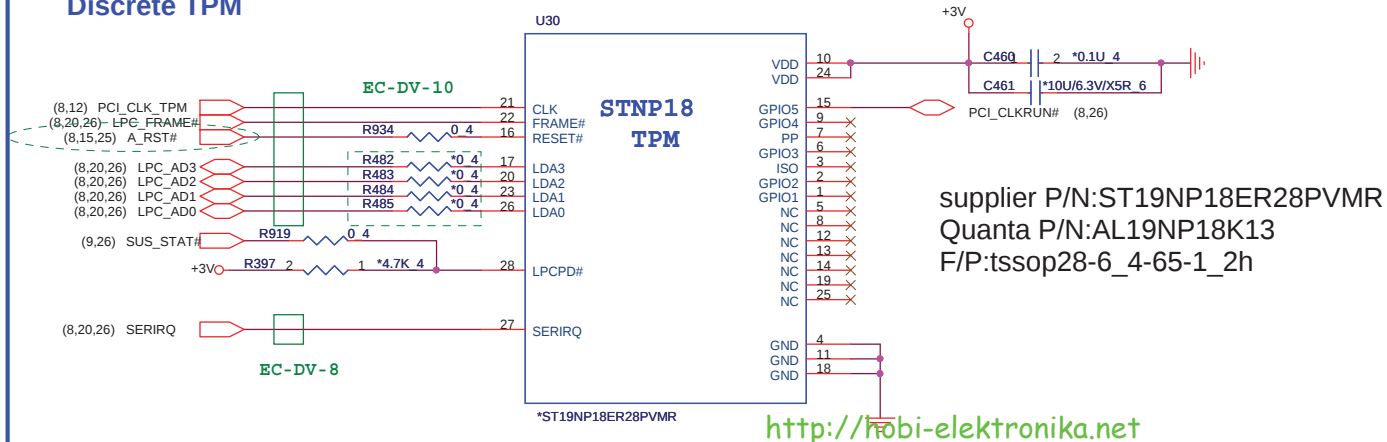
BLUETOOTH



G-SENSOR (2-Axial)



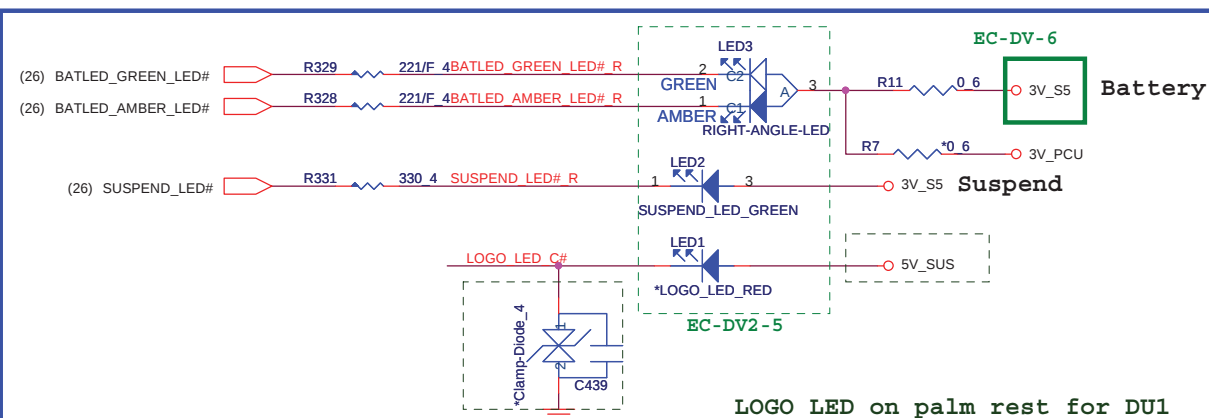
Discrete TPM



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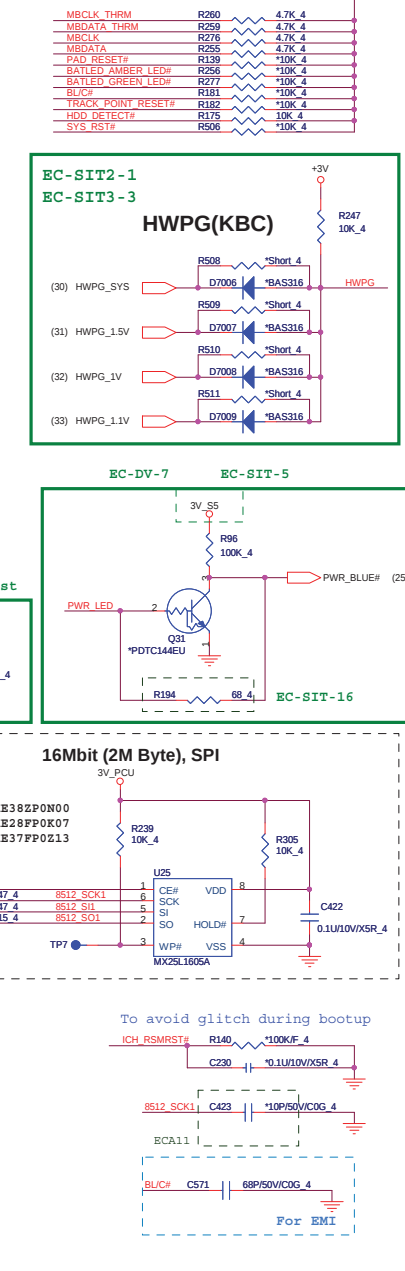


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POWER BUTTON

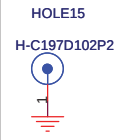
The schematic diagram illustrates the POWER BUTTON circuit. It features a POWER switch connected to a connector CN2. The switch is linked to a network of resistors (R4, R6, R10) and capacitors (C562, C563). A 3V_S5 voltage source is connected to the circuit. The circuit also includes a 3V_PCU input, a 15P/50V/NPO_4 capacitor, and a 15P/50V/NPO_4 capacitor. The circuit is designed for EMI filtering, with components labeled 'Fro EMI'.



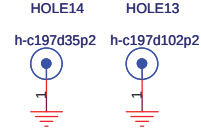
Hole for CPU support



MiniCard WLAN

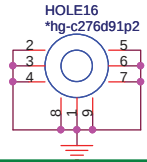


MiniCard WLAN



EC-DV-13

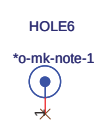
BLUETOOTH



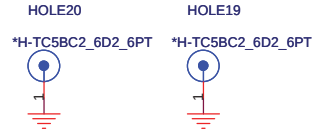
CRT



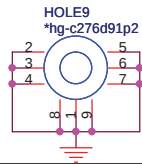
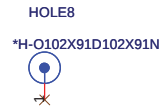
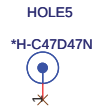
Keyboard



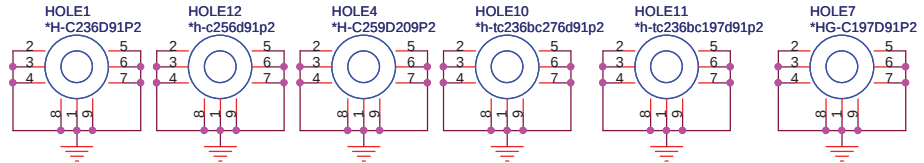
SB



Boundary Hole

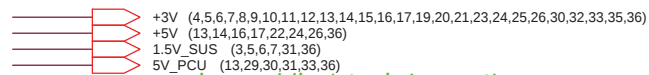
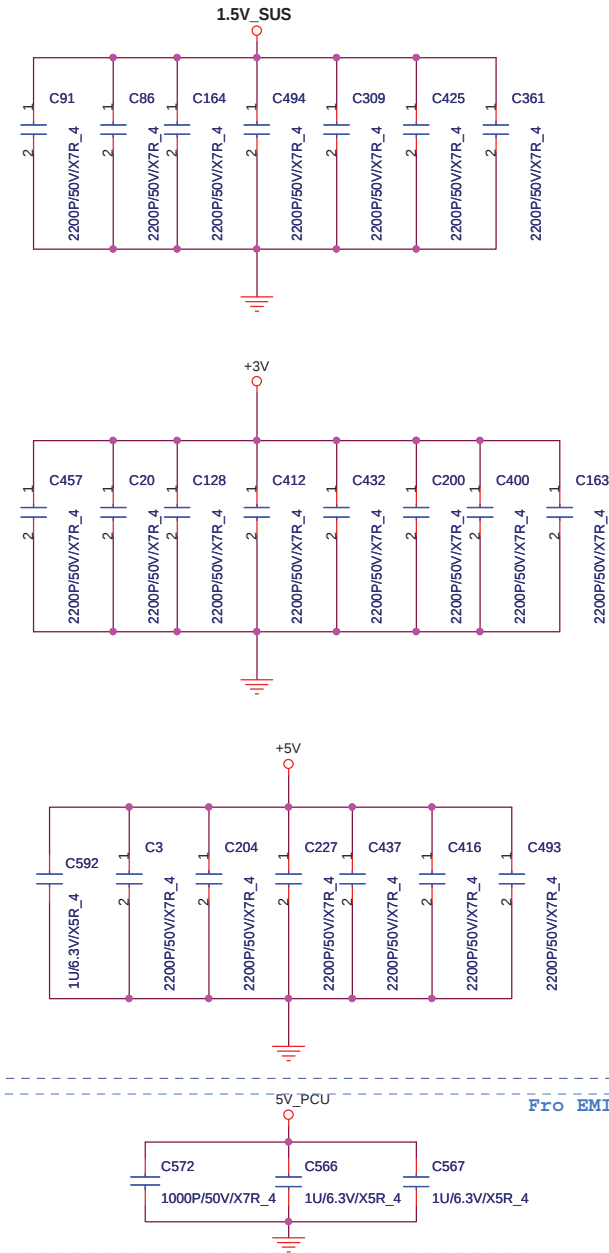


Boundary Hole



EC-DV-13

EMI


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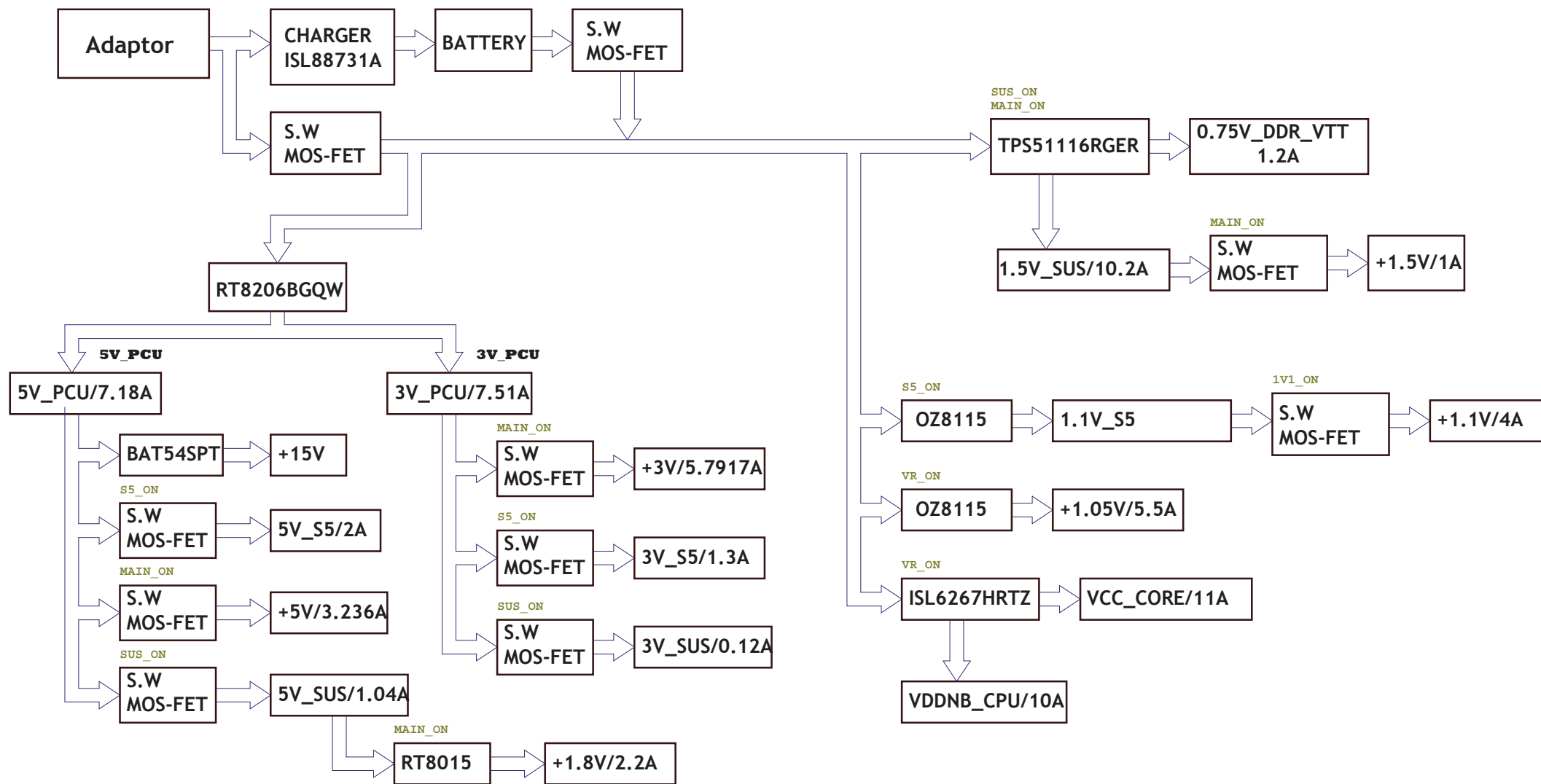

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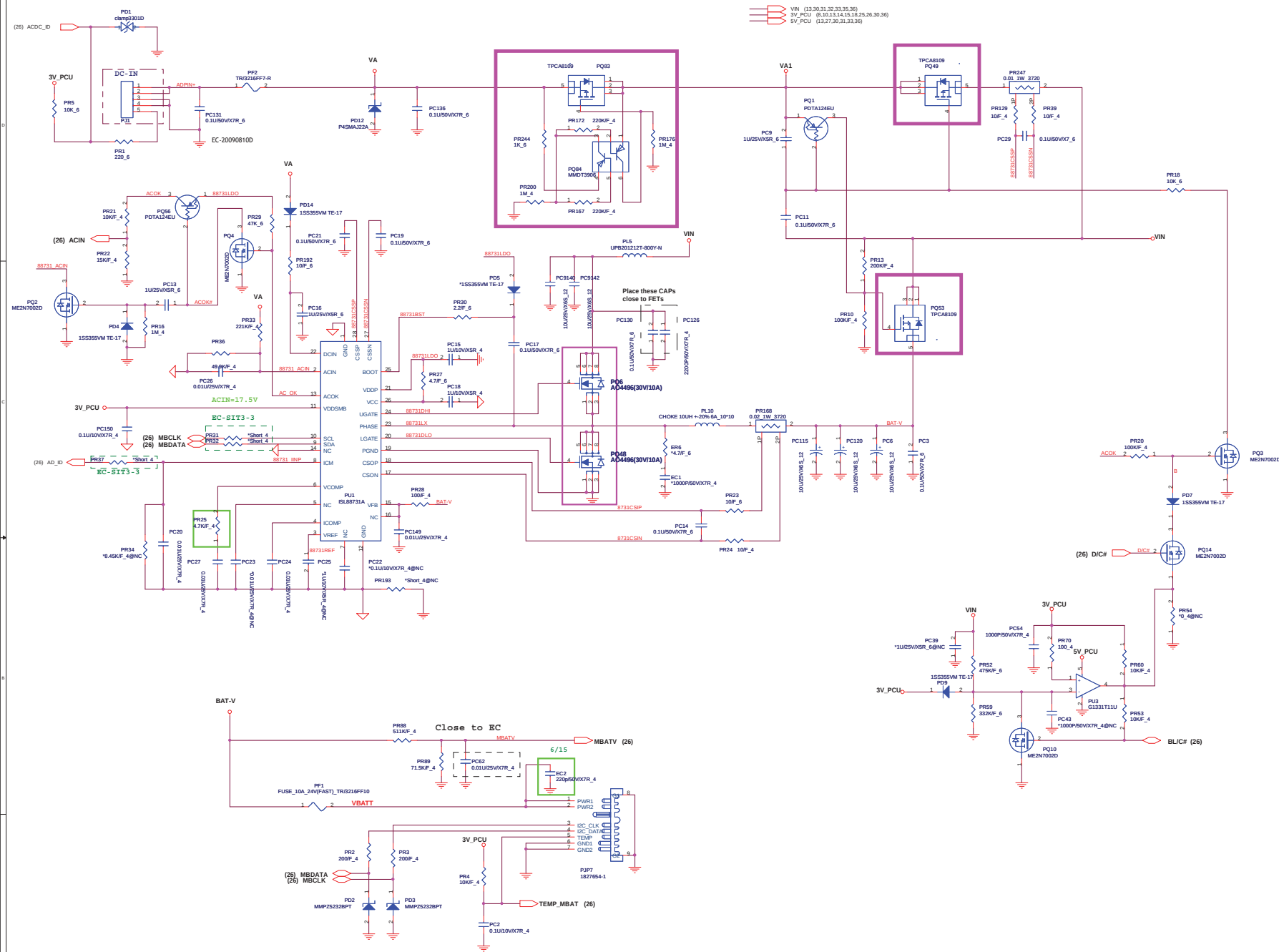
PROJECT : MK2.0

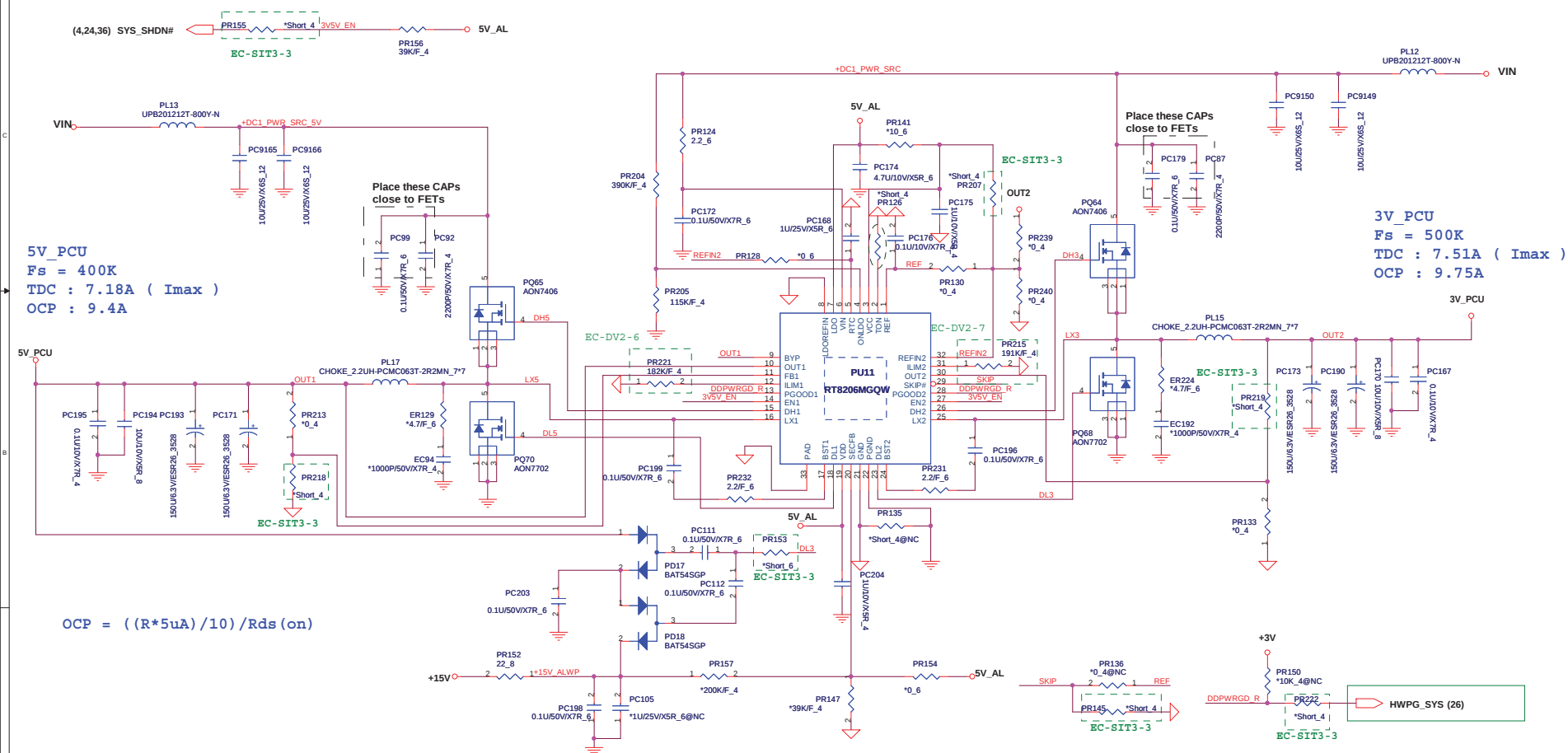
Size	Document Number	Rev
	Screw Hole/EMI	1A
Date:	Friday, October 29, 2010	Sheet 27 of 47

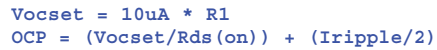
Brazos SYSTEM POWER BLOCK DIAGRAM

28

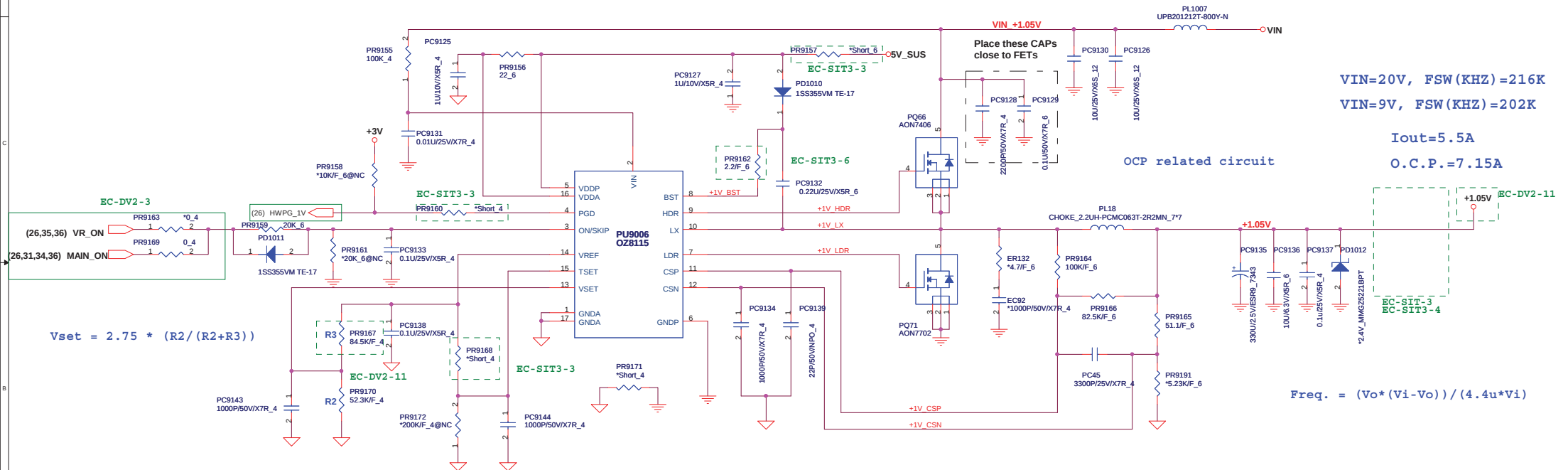








(13,29,30,31,33,35,36) VIN
(3,5,36) +1.05V
(13,25,34,35,36) 5V_SUS
(4,5,6,7,8,9,10,11,12,13,14,15,16,17,19,20,21,23,24,25,26,27,30,33,35,36) +3V



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Size Document Number
+1.05V (OZ8115)
Date: Friday, October 29, 2010 Sheet 32 of 47 Rev 1A

This page is different AMD Nile

VIN=20V, FSW(KHZ)=236K

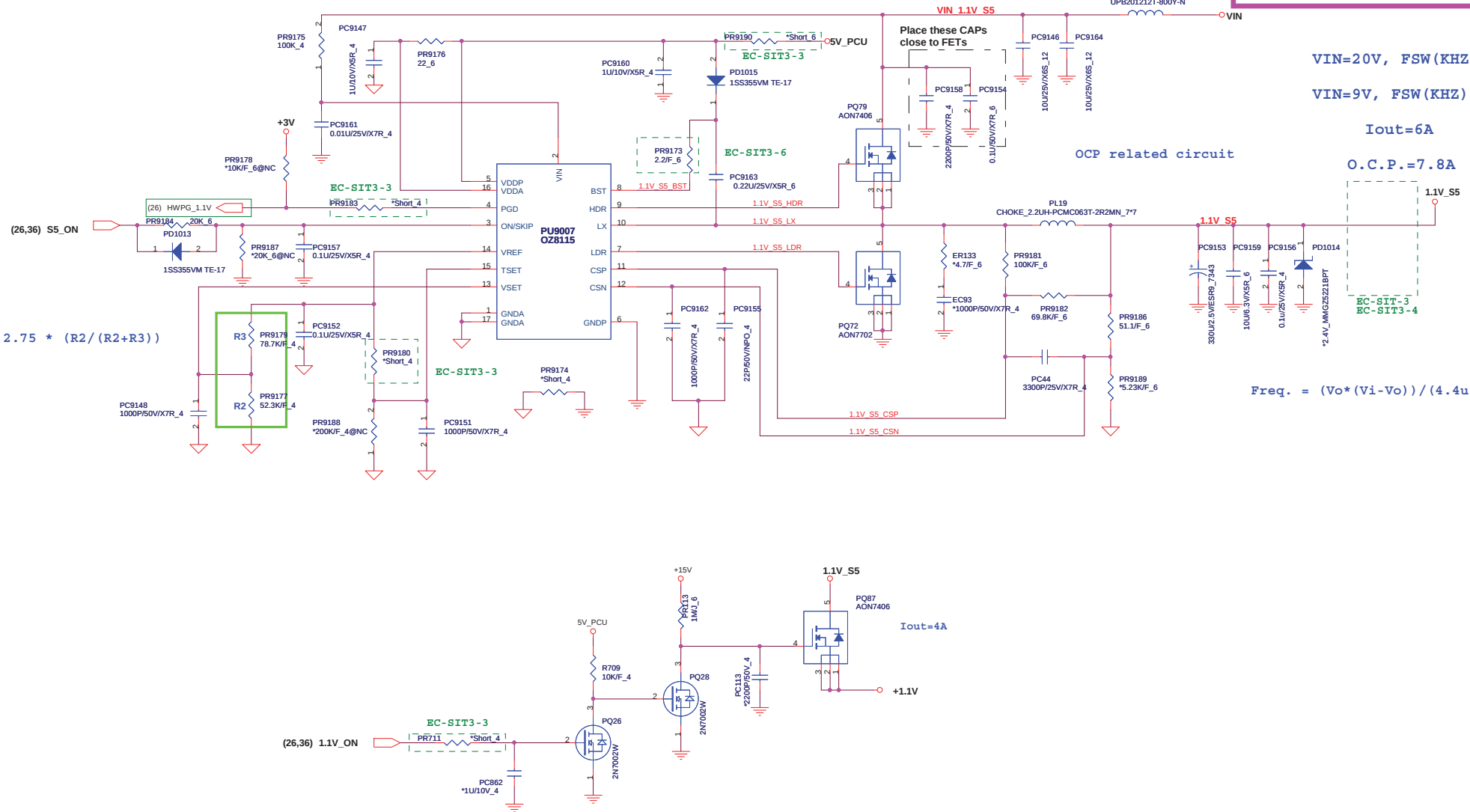
VIN=9V, FSW(KHZ)=219K

Iout=6A

O.C.P.=7.8A

Freq. = (Vo*(Vi-Vo))/(4.4u*Vi)

$$V_{set} = 2.75 * (R2 / (R2 + R3))$$



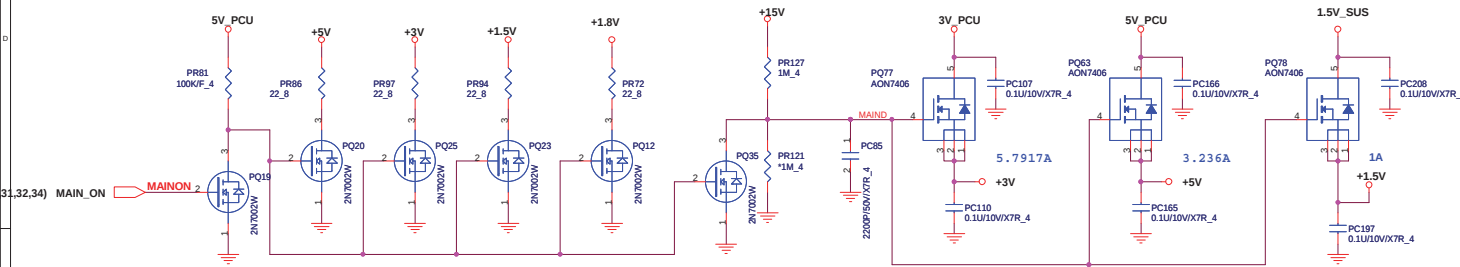
Quanta Computer Inc.
PROJECT : MK2.0

Size	Document Number	Rev
	+1.1V (OZ8115)	1A
Date:	Friday, October 29, 2010	Sheet 33 of 47

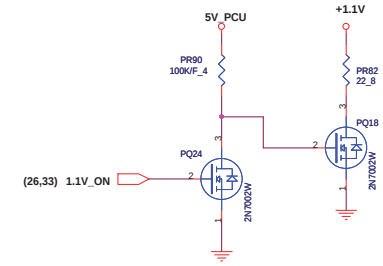


TDC: 2.2A (max)
OCP : 4A

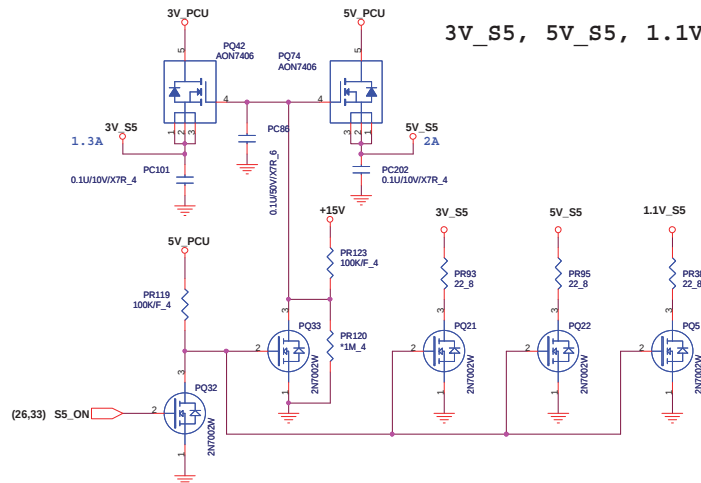
+3V, +5V, +1.8V, +1.5V



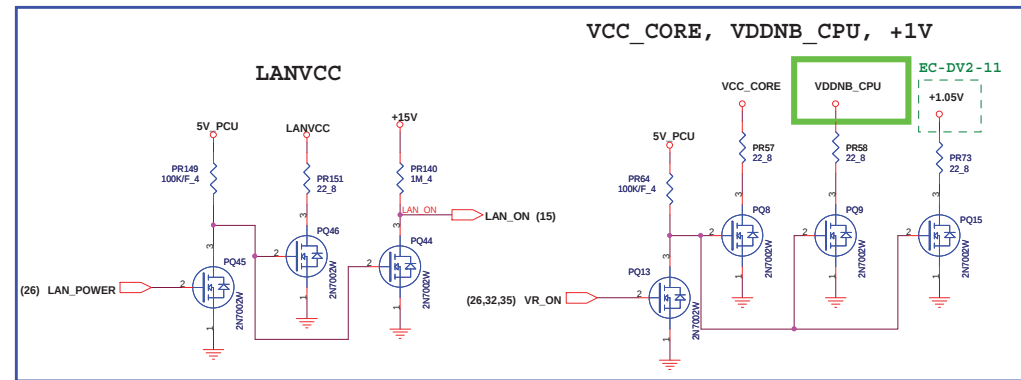
+1.1V



3V_S5, 5V_S5, 1.1V_S5

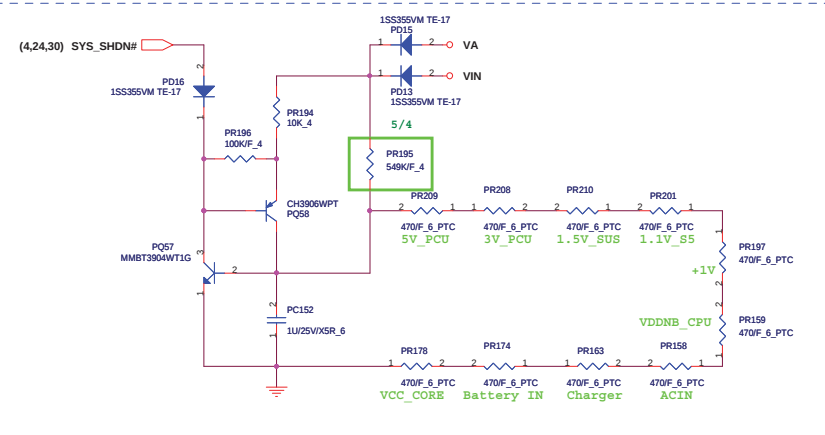
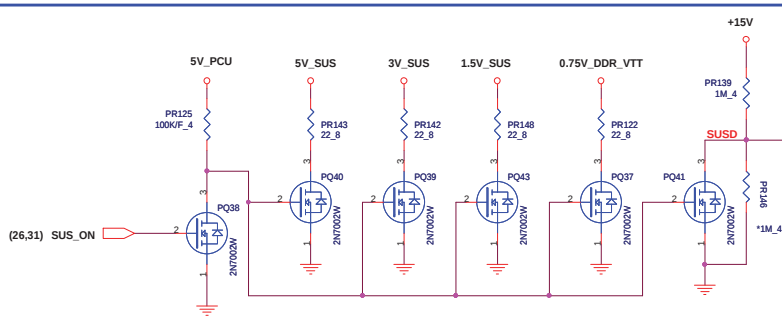


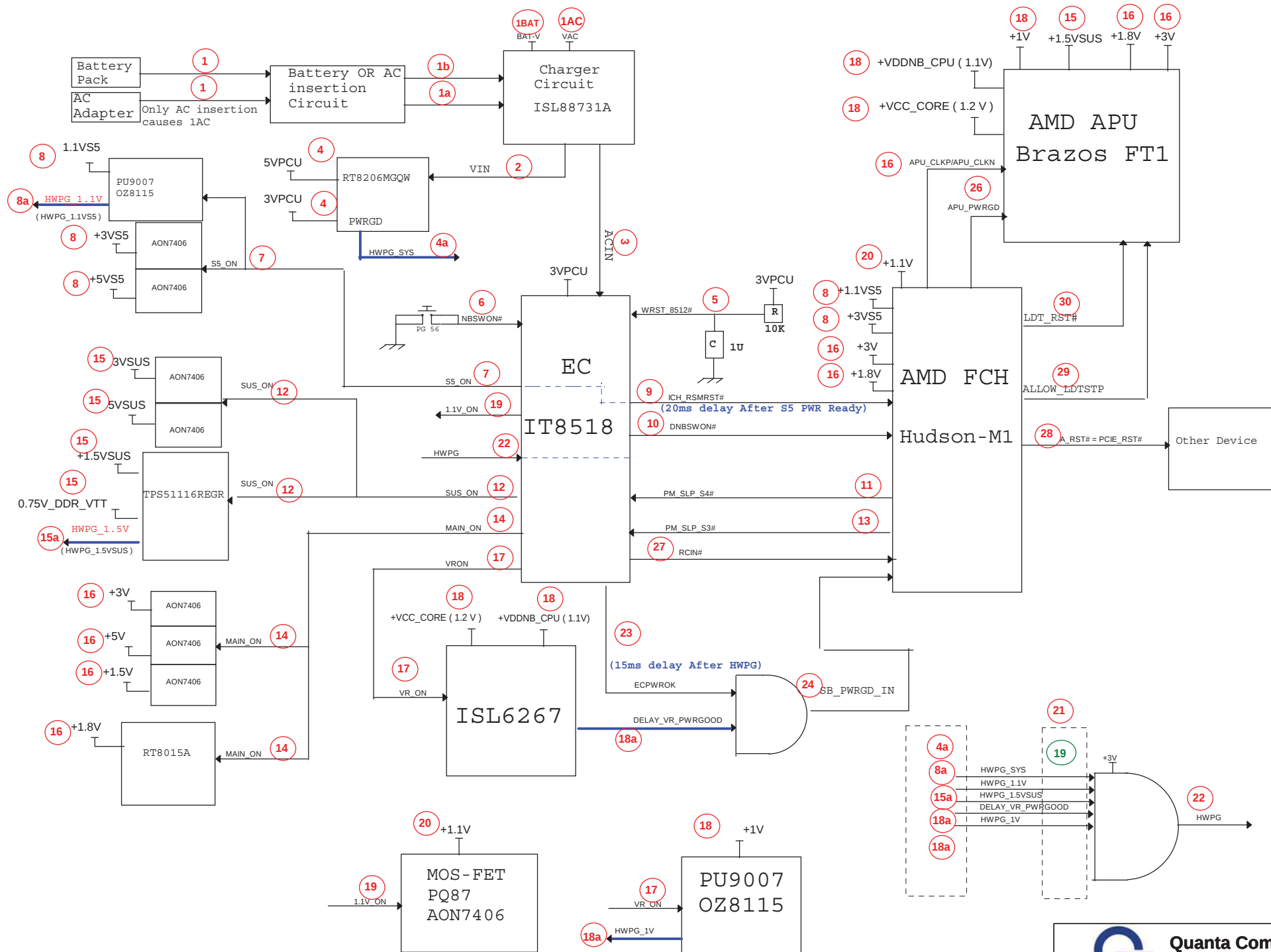
LANVCC



VCC_CORE, VDDNB_CPU, +1V

3V_SUS, 5V_SUS, 1.5V_SUS, 0.75V_DDR_VTT





[illegible]

Revision History

Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
A1A		DV	Initial release		

Schematic Value Explanation Description :

RESISTOR

Value	F	4	6	8	12	1210	*	Description
*1K/F_4	1%	0402 (1005)					DE POP	1K ohm 1% SMD 0402 package and DE POP
1K_6	5%		0603 (1608)				POP	1K ohm 5% SMD 0603 package and POP
1K_8	5%			0805 (2125)			POP	1K ohm 5% SMD 0805 package and POP
1K_12	5%				1206 (3216)		POP	1K ohm 5% SMD 1206 package and POP
1K_1210	5%					1210 (3225)	POP	1K ohm 5% SMD 1210 package and POP

CAPACITOR

Value	Voltage	Material	6				*	Description
*0.1U/10V/X5R_4	10V	X5R	0402 (1005)				DE POP	0.1UF 10V X5R SMD 0402 package DE POP
1U/25V/X7R_6	25V	X7R	0603 (1608)				POP	0.1UF 25V X7R SMD 0603 package POP

EC #	Page	Date	Part Affected	Description
EC-DV-01 (AMD Suggest)	11	10/08/01	C1094	Change value from 0.1U to 1U
	11	10/08/01	L60	Add a Inductor and connect to VDDPL_1.1V
	11	10/08/01	C1073	Change value from 4.7U to 2.2U
	11	10/08/01		PCH NET"XDDXL_33_S" change power rail from 3V_S5 to +3V
	4	10/08/01	R728	Because Prochot# has been pull up +3V, delete one pull up resistor. Delete R728.
	8	10/08/01	C1042, C1045, C1043, C1044	Change value from 18P to 22P.
	10	10/08/01	U44	Change SPI ROM input and output with PCH.
	4	10/08/01	R92	"LTDPO_APD"add pull down resistor
	4	10/08/01	R739,R740	Delete R739, R740
	14	10/08/01	R344,R349	"VGA_DAC_SDA and VGA_DAC_SCL" add pull up 4.7k resistor from +3V to +5V power rail.
	14	10/08/01	R100,R102,R104,R107,R109,R111,R118,R120	Change resistor value to 499 ohm
	14	10/08/01	Q13	Change Q13 power rail from +3X to +5V
	03	10/08/01	C871, C19	Add C871 and C19
	06	10/08/01	R123,R163	Change value from 10k to 1K
	11	10/08/01		Change "VDDIO_AZ" from +1.5V_SUS to +3V
	9	10/08/01	R324	Change value from 4.7K to 10K
	9	10/08/01	R324	USBOC1# and USBOC2# change pull up voltage from 3V_SUS to 3V_S5
EC-DV-02	8 9 10 26	10/08/02	C376,C381 C382, C370 C375	Add RF tesm suggest
EC-DV-03	9	10/08/02	RP12	Change footprint type for layout
EC-DV-04	26	10/08/02	U15	Change EC from IT8502E to IT8518
EC-DV-05	26	10/08/02	R192, R195	To prevent EC leakage issue
EC-DV-06	25	10/08/02		Change battery LED power rail from 3V_PCU to 3V_S5
EC-DV-07	26	10/08/02	R96,Q31	Fro EC suggest, change power LED control singnal from low active to high active.
EC-DV-08	14 23	10/08/02		Celete duplicate net.
EC-DV-09	14	10/08/02		Delete GND net of pin3 from U4 and U6

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FL7B / MK2 Schematic EC Tracking Record DV (for DV) JULY. 26, 2010

EC #	Page	Date	Part Affected	Description
EC-DV-10	23	10/08/02	R482,R483,R484,R485	Add resistor to improve LPC signal quality.
EC-DV-11	4	10/08/02	CN26,R922,R88,R89,R90,R926,R927,R928,R929,R924,R923	Change debug port to HDT+
EC-DV-12	4	10/08/02	Q33,R381	Add lever shift circuit to avoid leakage current
EC-DV-13	27	10/08/02	Hole1,Hole12,Hole4,Hole10,Hole11,Hole24	Change screw footprint for layout
EC-DV-14	14 6 7 13 15 16 17 18 19 20 21 23 25	10/08/02	R119,R117,R112,R110,R108,R105,R103,R101 R124 R158 R342,R348,R347 R177,R197,R208,R299 R477,R306,R323 R38,R72 R132,R133,R141,R142 R470,R464,R450 R200 R176 R291,R293,R295 R4,R6,R10	Change short pad to normal footprint type
EC-DV-15	15	10/08/02	C253	ESD suggest

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EC #	Page	Date	Part Affected	Description
EC-DV2-1	13	10/08/24	CN27,R342,R348	Because LVDS CONN still combine, delete USB component.
EC-DV2-2	9	10/08/24	R937,R938,R849,R851	EPROM setteing from SPI to LPC ROM.
EC-DV2-3	32	10/08/24	PR9153,PR9169	AMD Suggest it to meet power sequence.
EC-DV2-4	3,8	10/08/24	C109,C110	AMD Suggest that use APU PCIe interface to link LAN to enhance its performance.
EC-DV2-5	25	10/08/24	LED1,LED2,LED3	For ID design. Delete LED1 ,add LED2 and LED3
EC-DV2-6	30	10/08/24	PR221	For 5V_PCU OCP
EC-DV2-7	30	10/08/24	PR215	For 3V_PCU OCP
EC-DV2-8	35	10/08/24	PR277	For VDDNB_CPU OCP
EC-DV2-9	35	10/08/24	PR267	For VCC_CORE OCP
EC-DV2-10	35	10/08/24	PL9	For CPU Ripple voltage
EC-DV2-11	32	10/08/24	PR9167	For AMD request change +1V to +1.05V
EC-DV2-12	31	10/08/24	PC169	For 1.5V_SUS output ripple voltage
EC-DV2-13	35	10/08/24	PC231,PC212,PR246,PC222,PC242, PC228,PC254,PR270,PR267	Chip vendor suggest.
EC-DV2-14	26	10/08/24	D7006,D7007,D7008,D7009,R508,R509,R510,R511	Mount Diode for easy debug


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 Size Document Number Rev
 EC list for DV2 1A
 Date: Friday, October 25, 2010 Sheet 42 of 47

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FL7B / MK2 Schematic EC Tracking Record DV (for SIT) 09. 17, 2010

EC #	Page	Date	Part Affected	Description
EC-SIT-1	35	10/09/17	PU9	Chip vendor(Intersil) suggest that some power chip pin change from +5V to 5V_SUS to prevent 5V leakage current.
EC-SIT-2	31~34	10/09/17	PJP2,PJP6,PJP12,PJP13,PJP14,PJP15, PJP16,PJP17,PJP18	Power jump PCB footprint change from open type to short type
EC-SIT-3	26	10/09/17	R512	For S3/S4/S5 leaksge issue from 20mA to 5mA. This pin is re-define from output to input. But EC don't use this pin. Resever it.
EC-SIT-4	25	10/09/17	CN2 pin4	Power LED plan change from 3VPCU to 3V_S5 to prevent LED flight one tie issue during plug adapter. Fix ECR72256 from Vendor(ITE) suggestion
EC-SIT-5	26	10/09/17	Q31, R194	Power LED enable lever from high active to low active. Delete Q31, add R194. Fix ECR72256 from EC team member request
EC-SIT-6	25 13	10/09/17	Q24,Q21,Q25,R311,R301,R288,R314 C568	Because MK2B don't support Logo LED function, delete them. Delete Q24,Q21,Q25,R311,R301,R288,R314,C568
EC-SIT-7	13	10/09/17	R12	Reserve R12(short pad) to prevent LCD short current verication.
EC-SIT-8	6 7	10/09/17	C7274, C7275	Change DDR DIMM Module VREF_CA and VREF_DQ reference power.
EC-SIT-9	15	10/09/17		Because LAN interface cahnge FCH to APU, change its reset signal from PCIE_RST# to A_RST#.
EC-SIT-10	19	10/09/17	Y7, C257, C258,R472,R459	Cardreader clock input from 12MHZ crystal to FCH internal clock.
EC-SIT-11	5	10/09/17	C927, R9796,C934	Delete C927,C934 for layout. Add R796 for AMD suggest.
EC-SIT-12	8	10/09/17	C1111	Reserve a capacitor for RF team request.
EC-SIT-13	11	10/09/17	L48,L50,L52	AMD suggest. Change its current sustain from 1.5A to 5A.
EC-SIT-14	10	10/09/17	R881,R884,R885,R877,R878,C1058	Because BIOS and EC use the same ROM, delete them from BOM.
EC-SIT-15	8	10/09/27	C1043,C1044	Crystal vendor suggest(TXC and Hosonic)that chage fromm 22P to 10P to get good sin=gnal
EC-SIT-16	26	10/10/05	R194	Change value from 0 ohm to 68 ohm to meet ITE8518 current limit issue.

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FL7B / MK2 Schematic EC Tracking Record SIT3 (for SIT3) 10. 29, 2010

EC #	Page	Date	Part Affected	Description
EC-SIT3-1	15,16,18	10/10/28	RV1, RV3, RV9,RV10,RV11,C503,C504	Add ESDprotect component for ESD request.
EC-SIT3-2	4	10/10/28	R739,R740,R741,R742,T116,T179	Delete unnecessary component R739,R740,R741,R742. Add T116 ,T179.
EC-SIT3-3	3	10/10/28	R718	change to short pad
	4		R743,R745,R750,R788,R789,R791,R790,R793,R792,R795,R794,R730,R725,R731	
	5		R785,R786	
	6		R124	
	7		R158	
	8		R809,R810,R811,R812	
	9		R825,R827,R831	
	11		R890,R891,R893,R894	
	13		R342,R348,R347,R351,R352	
	14		R119,R117,R112,R110,R108,R105,R103,R101	
	15		R177,R197,R208,R299	
	16		R477,R306,R323	
	18		R132,R133,R141,R142	
	19		R470,R464,R450,R472	
	20		R273,R252	
	21		R176,R253	
	23		R291,R293,R295	
	26		R508,R509,R510,R511	
	29		PR31,PR32,PR37	
	30		PR155,PR218,PR153,PR126,PR207,PR219,PR145,PR222	
	31		PR132,PR206,PR228,PR230,PR238,PR214,PR235,PR9157,PR9160,PR9168,PR9190,PR9183,PR9180,PR711,PR103,PR256,PR243	
	35		PR160,PR287,PR245,PR283,PR241	
EC-SIT3-4	5	10/10/28	R787,R796,R784	delete power jump
	17		R38,R72	
	20		R200	
	31		PJP12,PJP13,PJP6	
	32		PJP14,PJP15	
	33		PJP16,PJP17	
	34		PJP2,PJP18	
EC-SIT3-5	35	10/10/28	PR251,PR249	Change for PSI function
EC-SIT3-6	32,33	10/10/28	PR9162,PR9173	Change for switch phase voltage

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EC #	Page	Date	Part Affected	Description

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EC #	Page	Date	Part Affected	Description

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