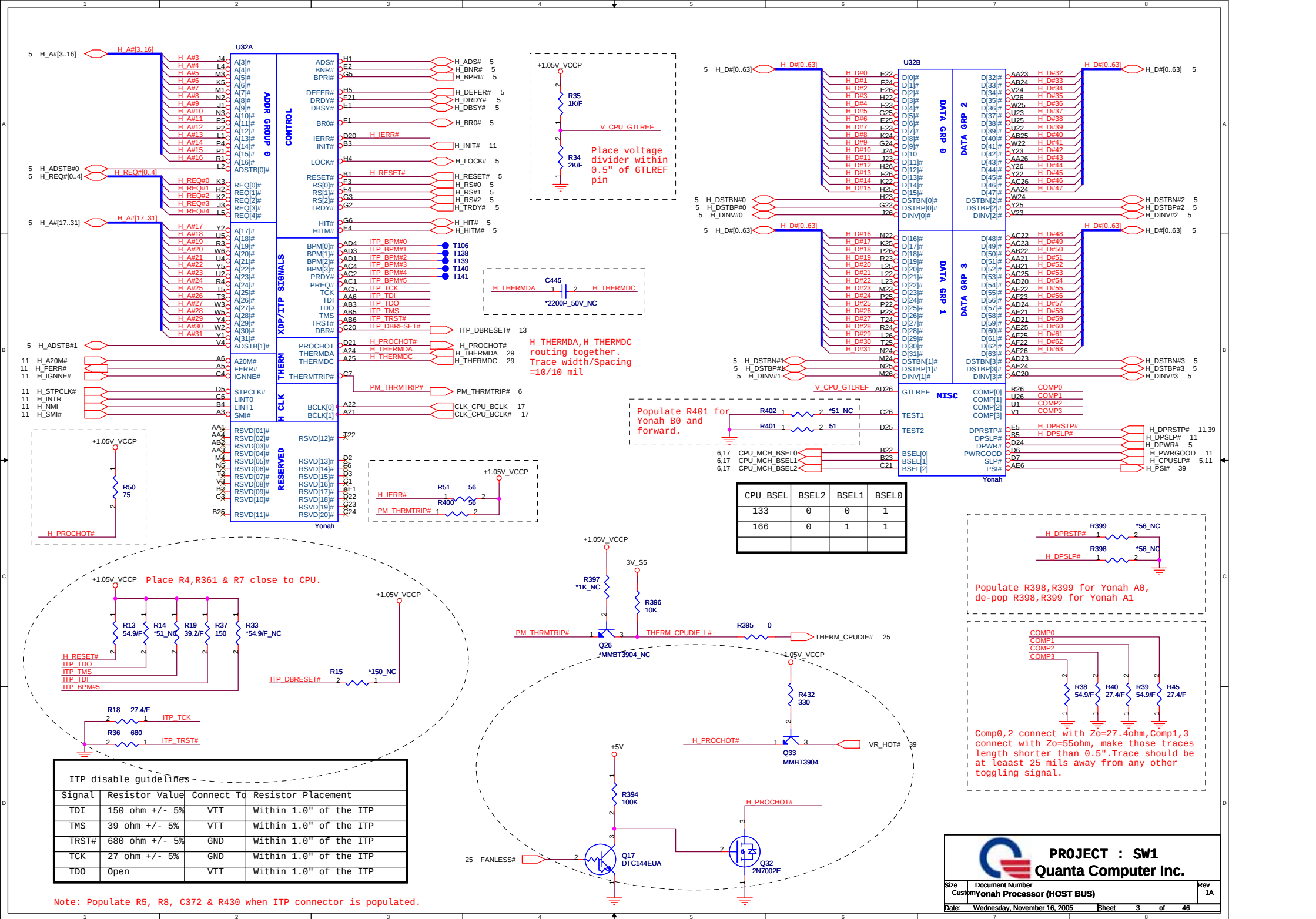


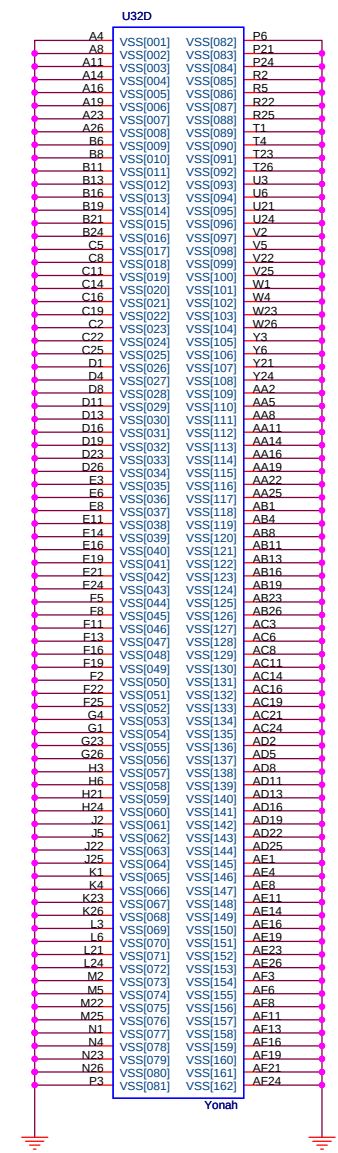
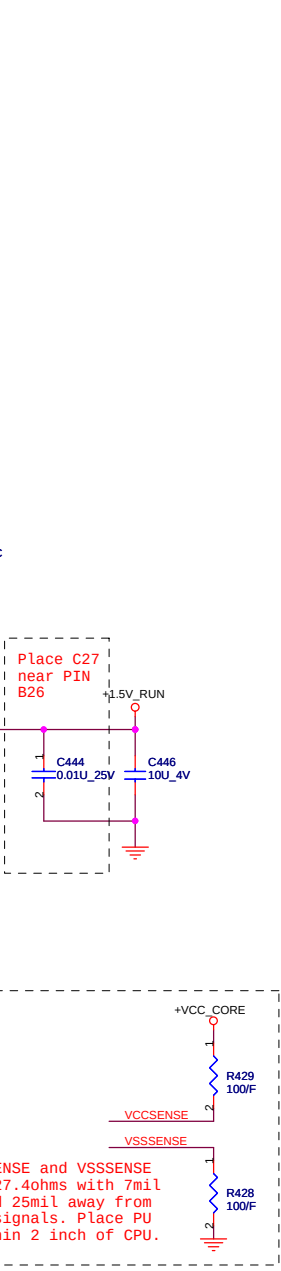
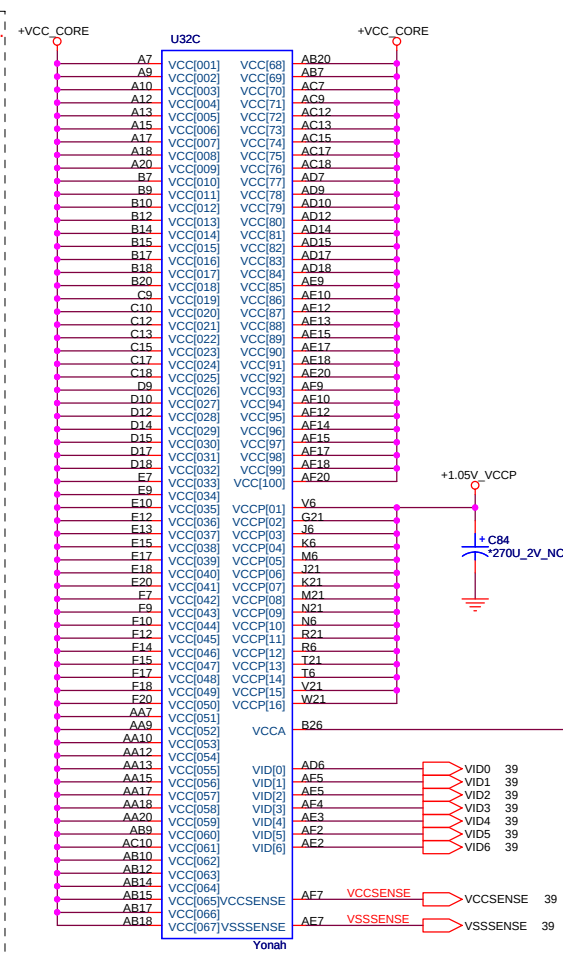
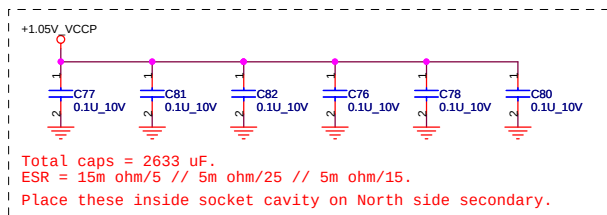
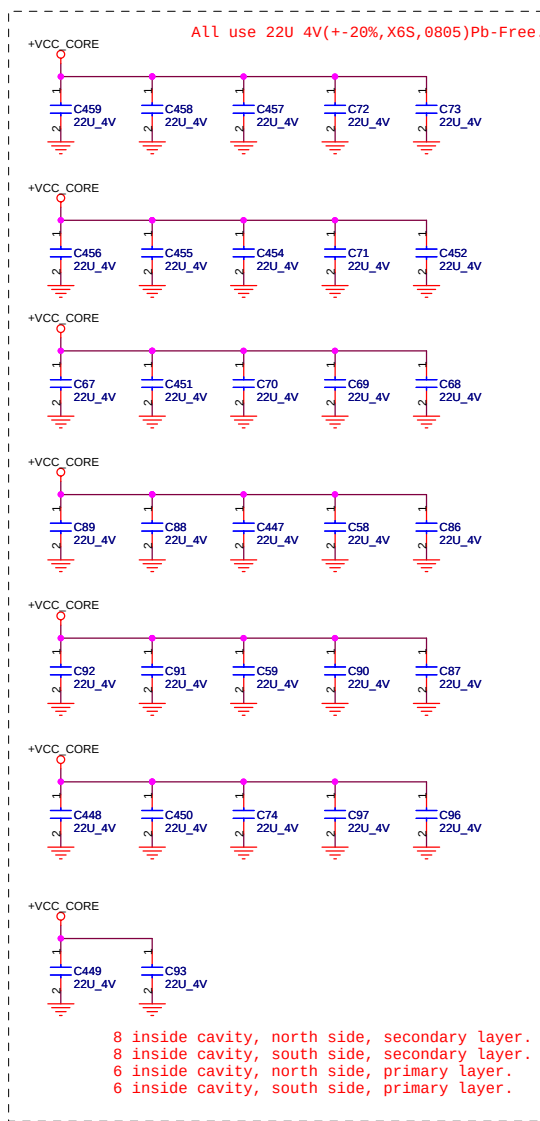
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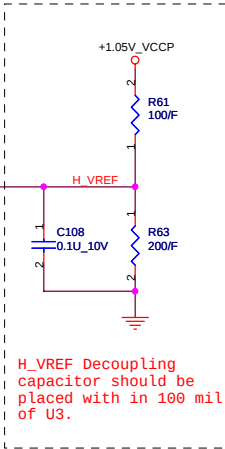
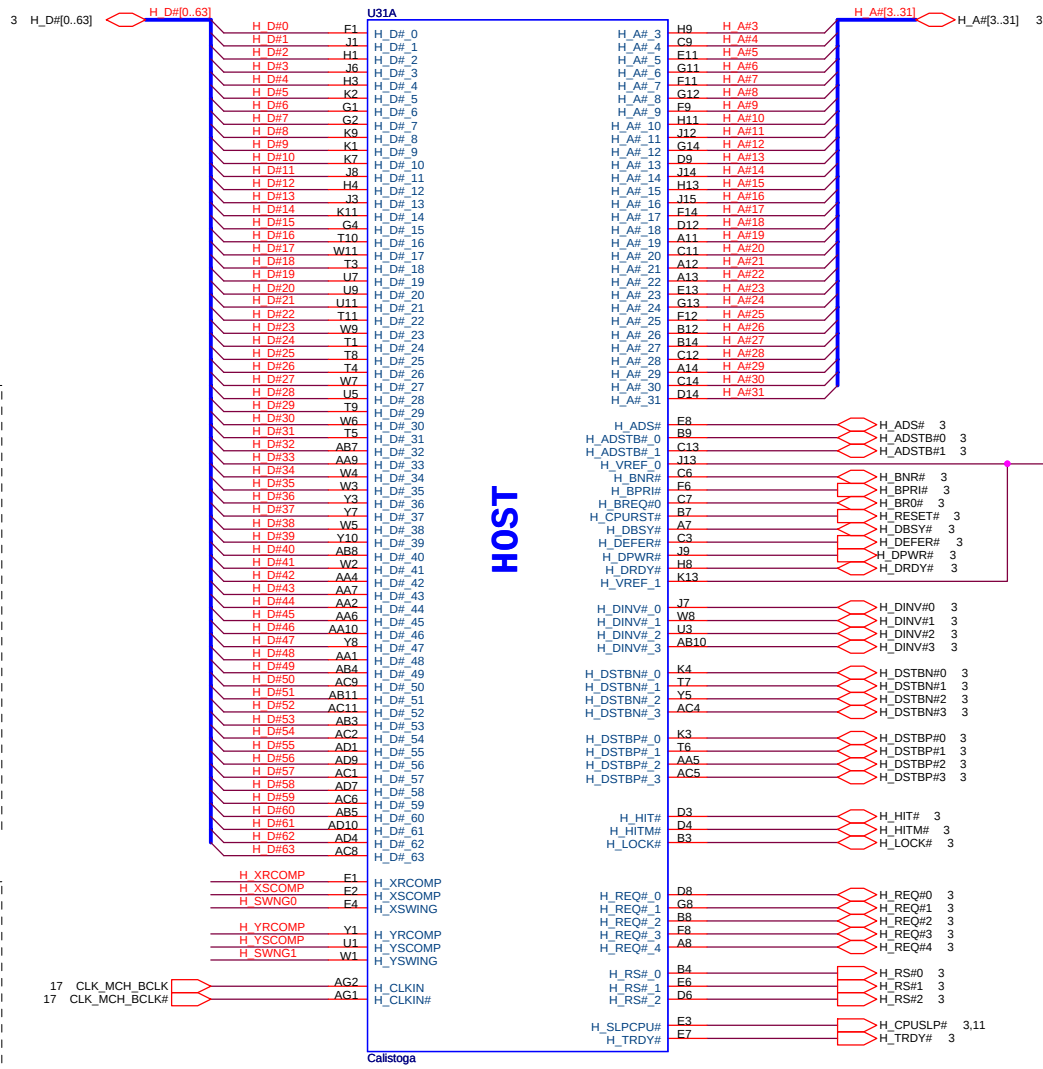
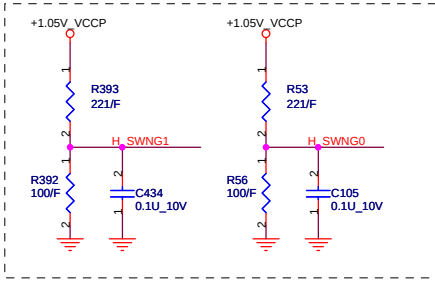
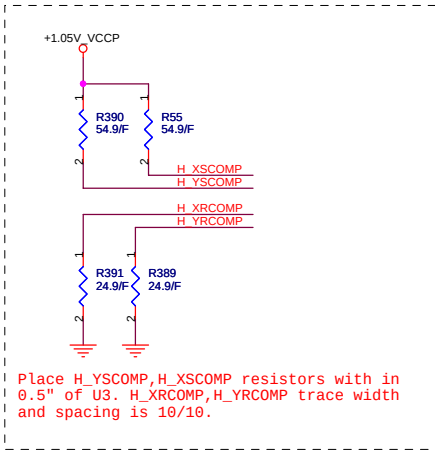
Pg#	Description	DNI LIST
1	Schematic Block Diagram	
2	Front Page	
3-4	Yonah	
5-10	Calistoga	
11-14	ICH7	
15-16	DDR2 SO-DIMM(200P)	
17	Clock Generator	
18-21	VGA	
22	LCD Conn. & SSP	
23	CRT Conn	
24	SATA & IDE Conn	
25	PCCARD/Conn & 1394	
26	Express Card & Smart Card	
27	Mini Card	
28	MDC Conn.	
29	SIO (MEC5004)	
30	SIO (MEC5018)	
31	SERIAL PORT & USB	
32	Flash ROM	
33	TP,BT & FIR	
34	Switch,Keyboard & LED	
35	FAN & Thermal	
36-37	Audio CODEC(STAC9200)/Phone Jack	
38-39	LOM (BCM5752)/Switch	
40-41	Docking Conn/Q-Switch	
42	System Reset Circuit	
43-44	Battery Selector & Charger	
45	DDR2_1.8VSUS, 0.9V	
46	1.5VSUS,1.05V(VTT)	
47	CPU Power	
48	D/D Power	
49	RUN Power Switch	
50	VGA DC/DC	
51	DCIN/Batt Conn.	
52	PAD& SCREW	
53	SMBUS BLOCK	

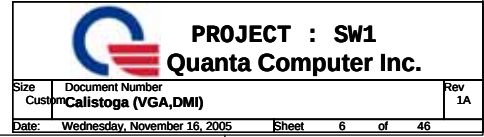
Power & Ground

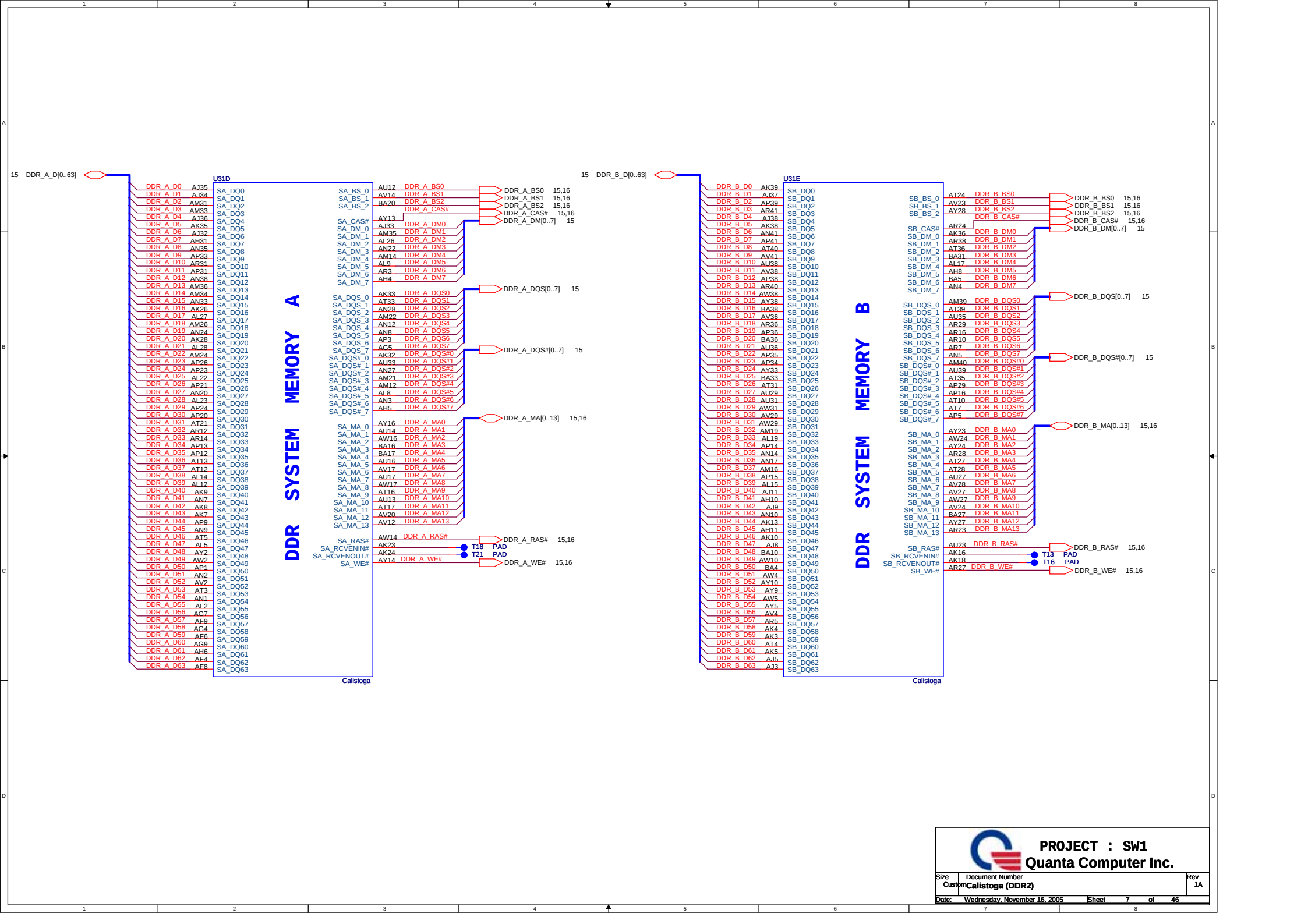
Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (20V)	
PBATT+		MAIN BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~20V)	
RTC_PWR3_3V		RTC & PCL POWER (3.3V)	
+12V		+12V	DRUNPWROK
VHCORE		CPU CORE POWER (1.25/1.15V)	RUNPWROK
V1_2RUN		AGTL+ POWER (1.2V)	RUNPWROK
+3VRUN		SLP_S3# CTRLD POWER	RUN_ON
+3VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VALW		8051 POWER (5V)	
+5VRUN		SLP_S3# CTRLD POWER	RUN_ON
+5VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VHDD		HDD POWER (5V)	HDDC_EN#
+5VMOD		MODULE POWER (5V)	MODC_EN#
STRB#5V		EXTERNAL FDD POWER (5V)	FDD/LPT#
+5VFAN1, +5VFAN2		FAN POWER (5V)	FAN_OFF/ON#
VDDA		AUDIO ANALOG POWER (5V)	RUN_ON
1_8VSUS		RESUME WELL IN ICH	
1_8VRUN		SLP_S3# CTRLD POWER	
+3VALW		8051 POWER (3V)	
V1_5RUN		AGP I/O POWER	
 GND	ALL PAGES	DIGITAL GROUND	
 GNDP		CPU POWER GND	
 CGNDP		CHARGER GND	
 DGNDP		DC/DC POWER GND	
 LANGND		COMBO CONN GND	

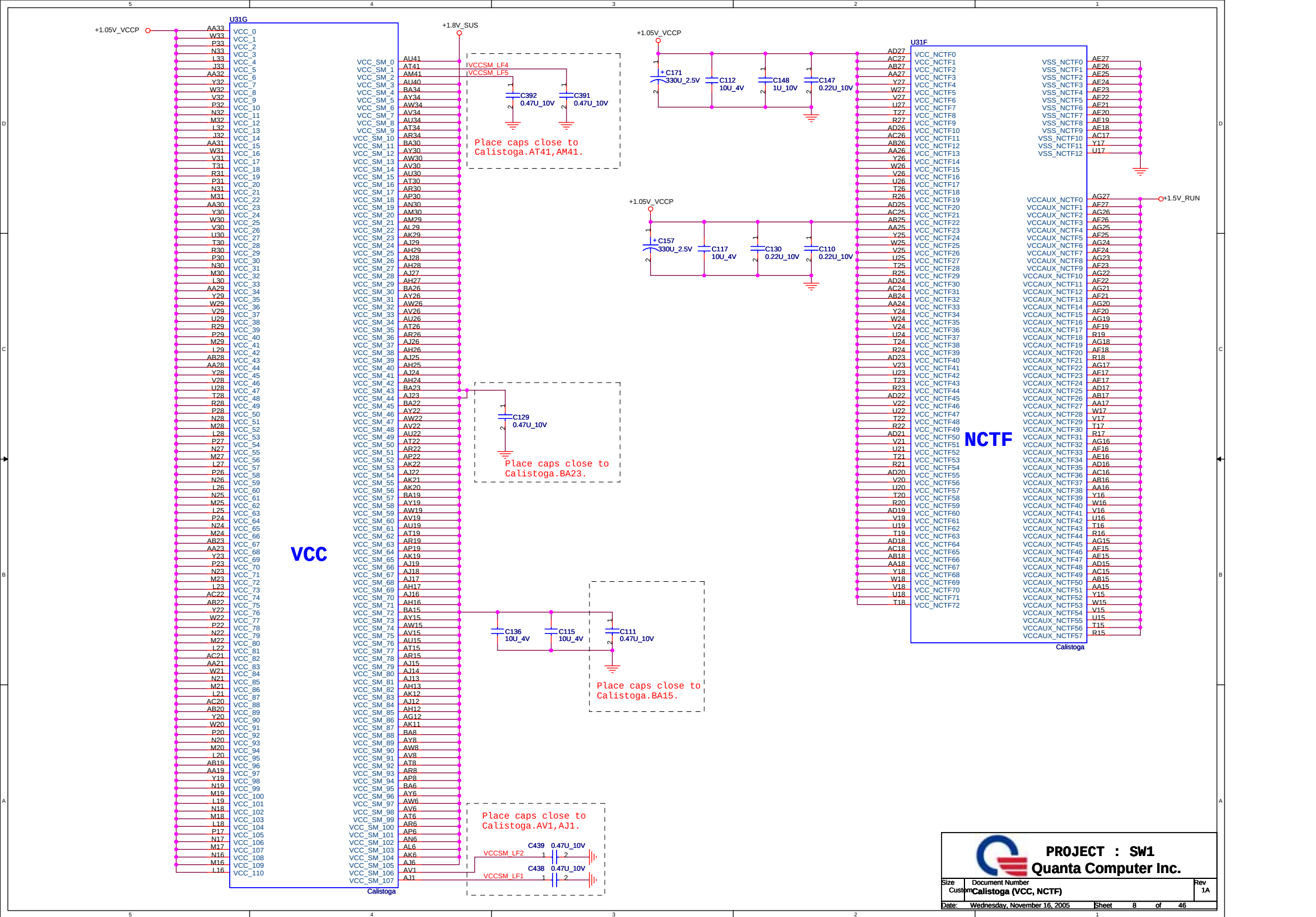


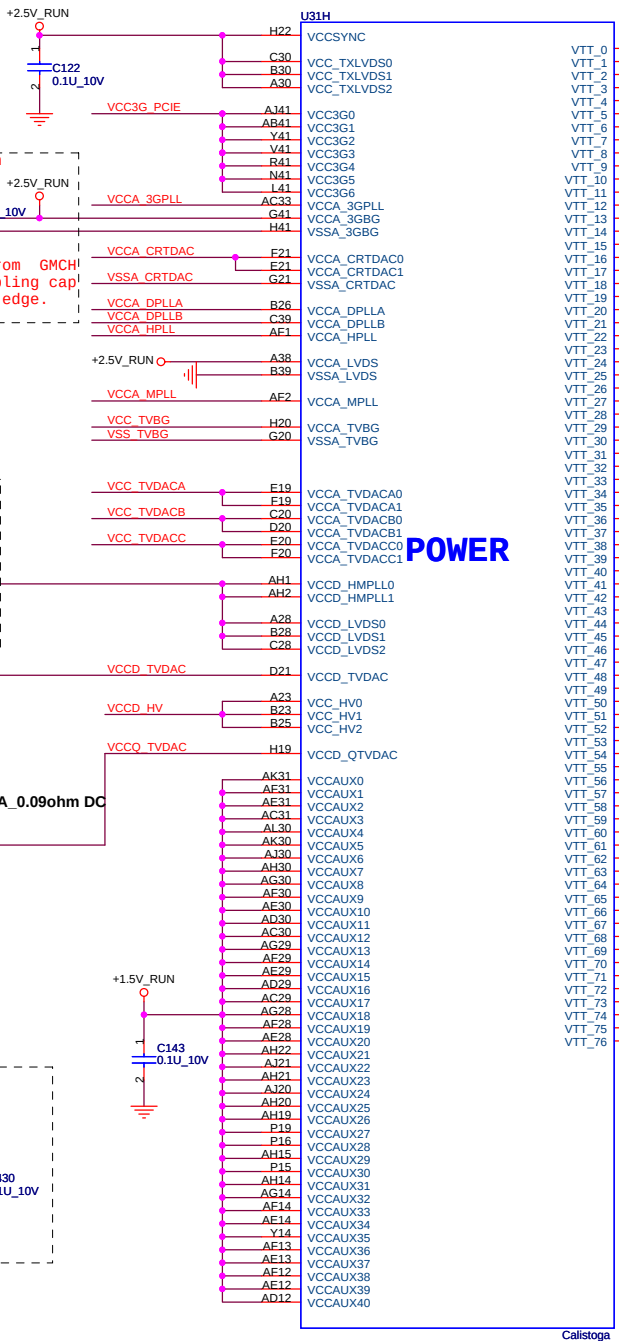
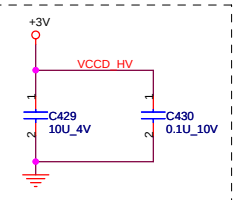
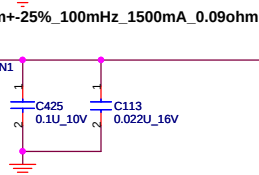
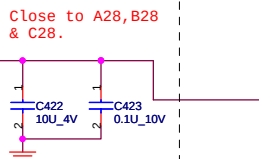
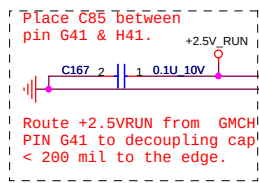
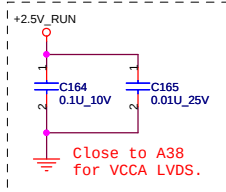
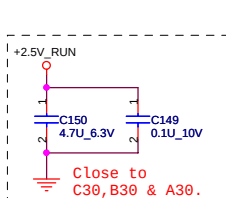
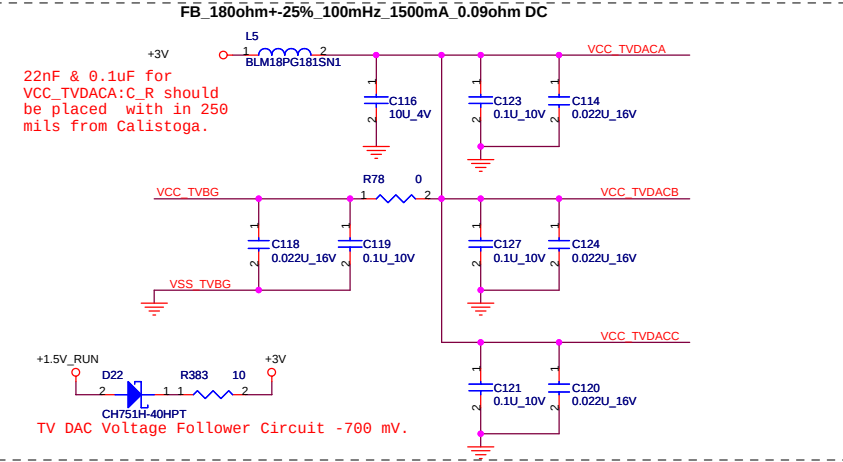
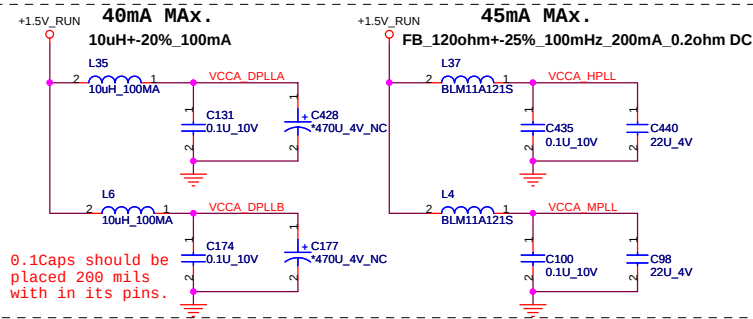
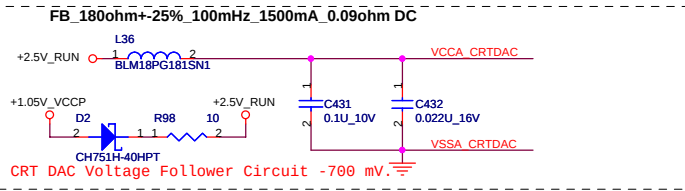
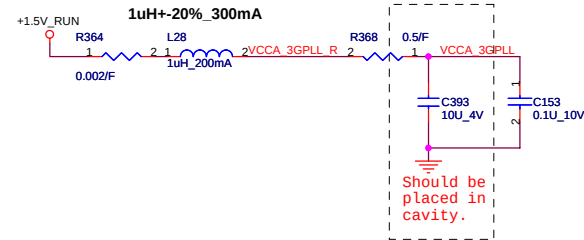
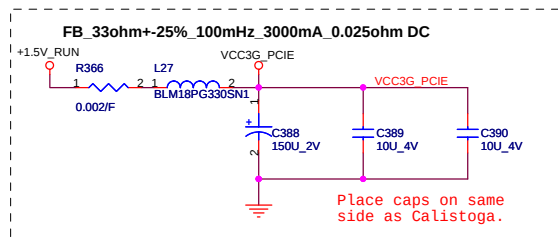




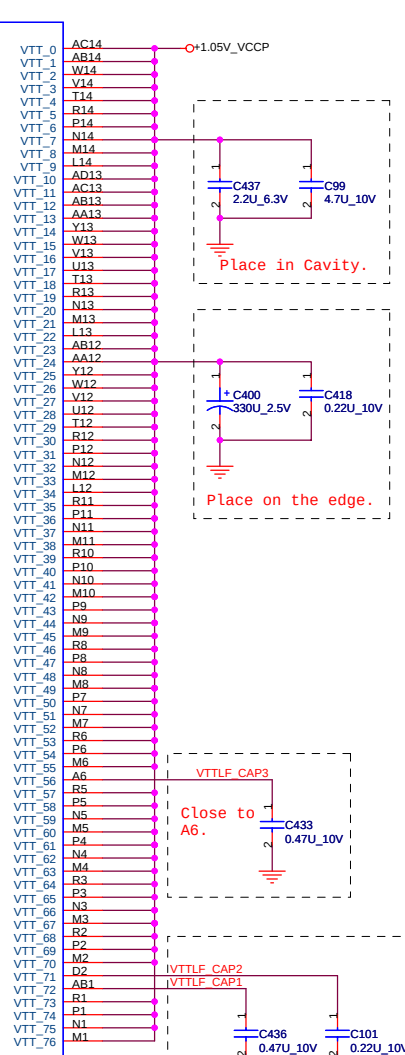


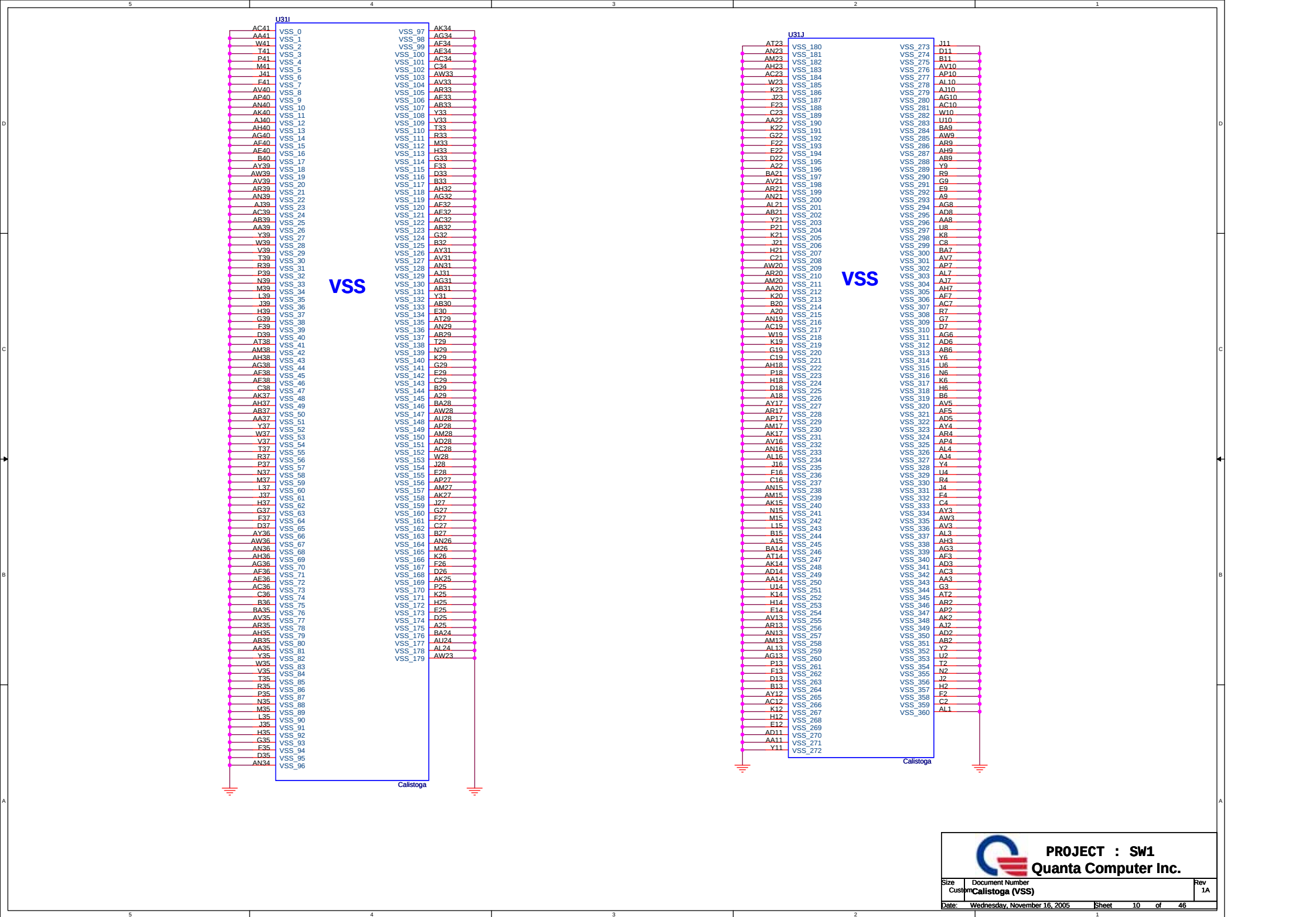




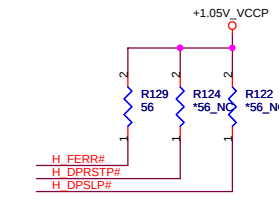
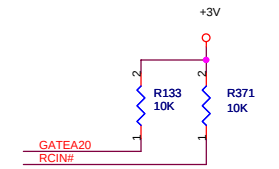
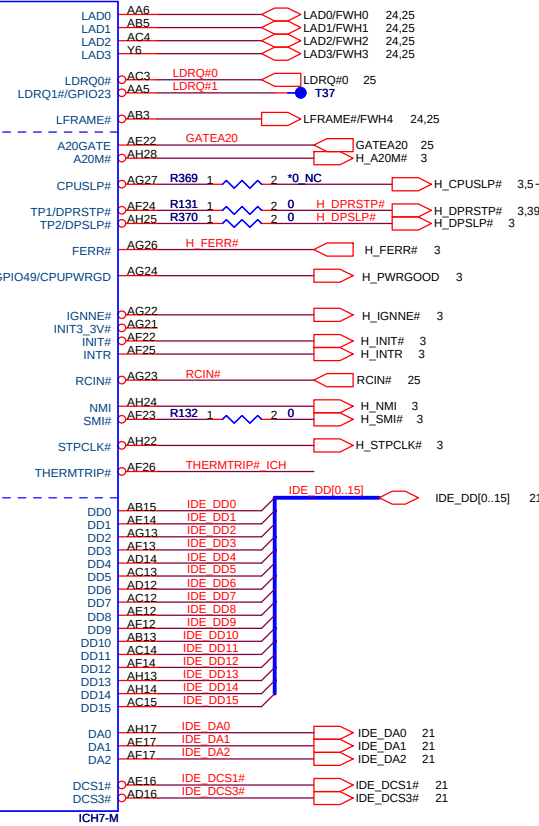
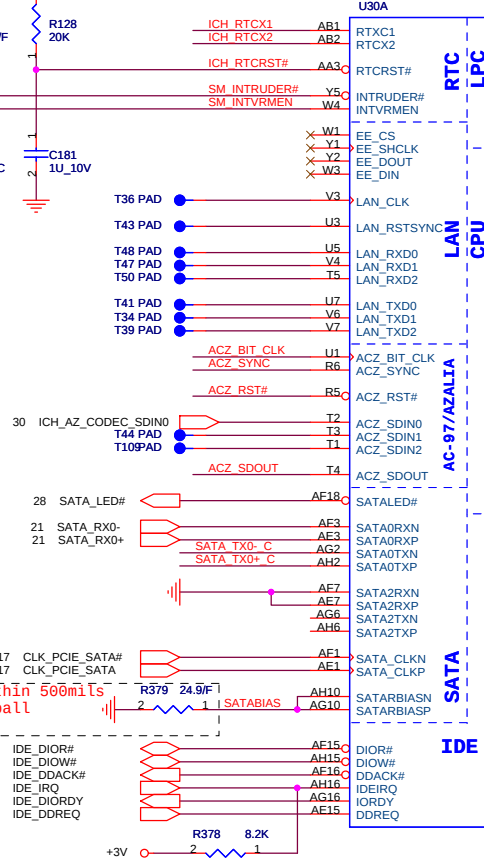
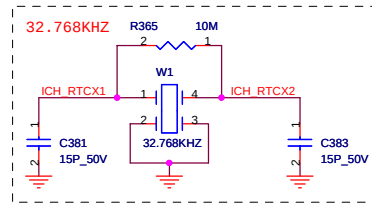
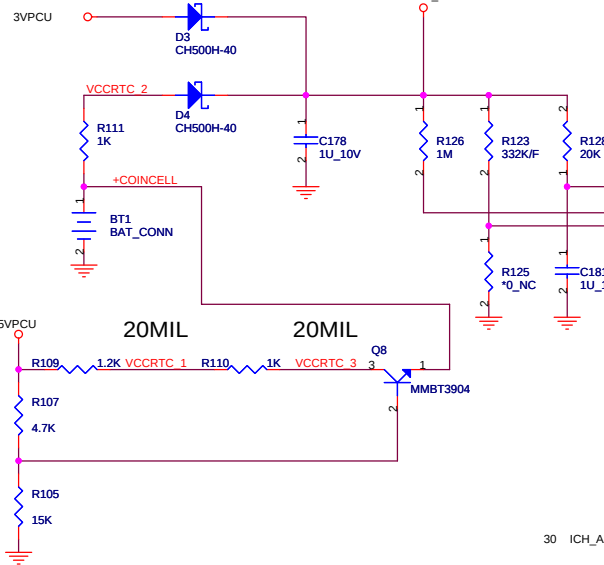


POWER

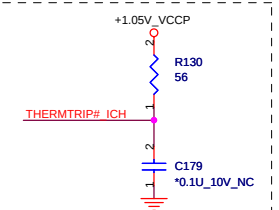




RTC

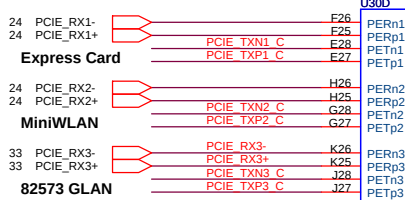
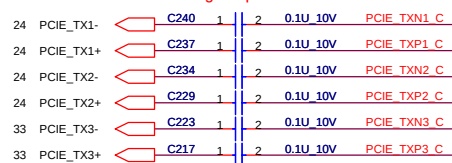


Depop R369 if the MCH is driving CPUSLP# to the CPU. Place the resistors from ICH & MCH close together minimize stubs for either pop option.

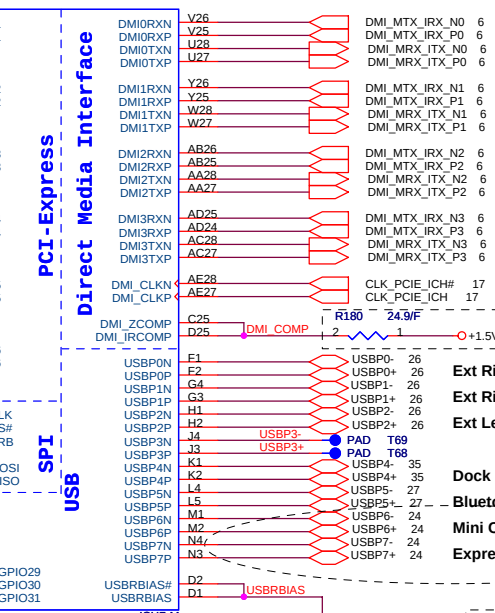
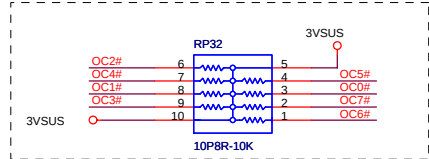
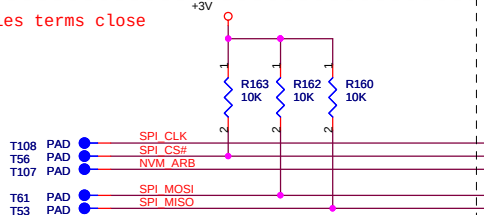


R130 & C179 should be placed as close as possible to ICH ball.

Place TX DC blocking caps close ICH7.



Place series terms close to source.

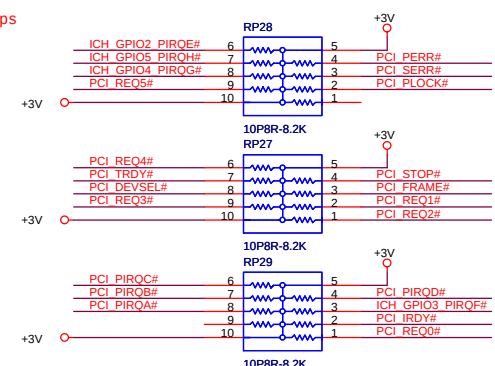


Short D2 and D1 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

Place within 500mils of ICH7

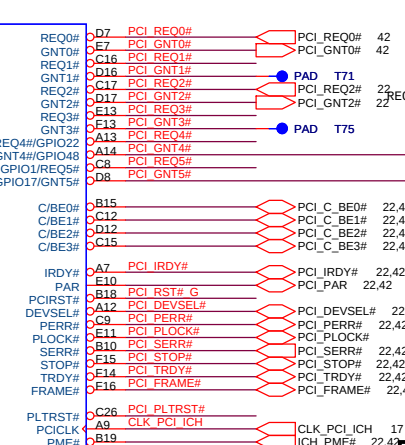
Ext Right Side Top
Ext Right Side
Ext Left Side
Dock
Bluetooth
Mini Card
Express Card

PCI Pullups



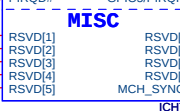
		GNT5#	GNT4#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

PCI

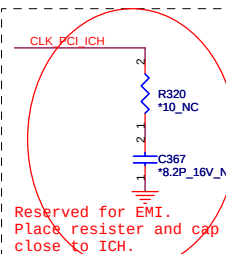


Interrupt I/F

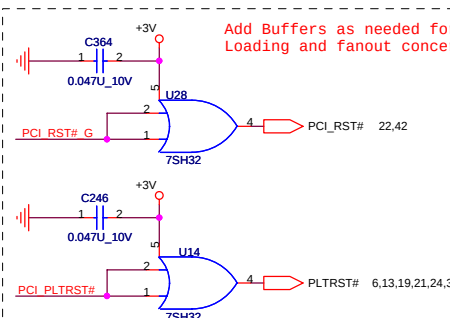
MISC



		REQ0	GNT0	PIRQA
DOCK				
Cardbus or Cardbus/1394		REQ1	GNT1	PIRQD
1394/MediaCard		REQ2	GNT2	PIRQC
LOM(4401)		REQ3	GNT3	PIRQB

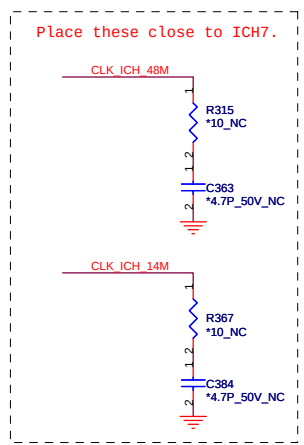
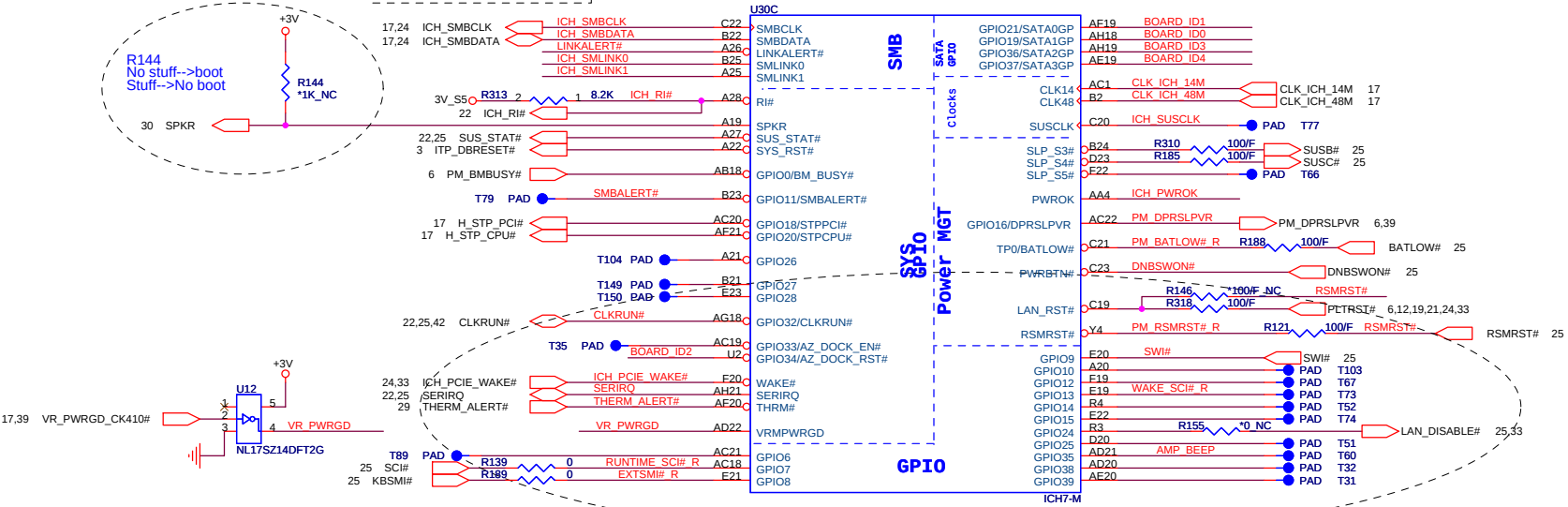
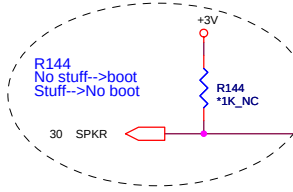
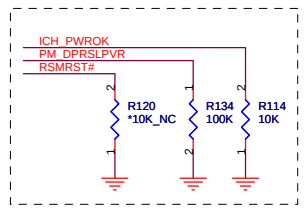
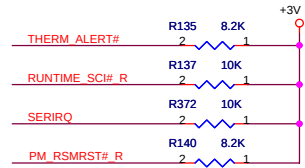
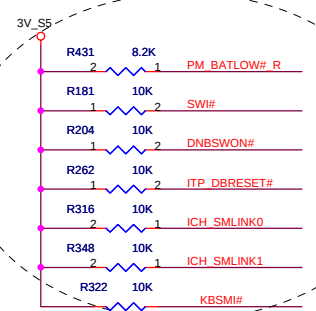
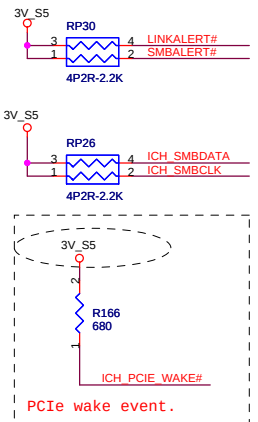
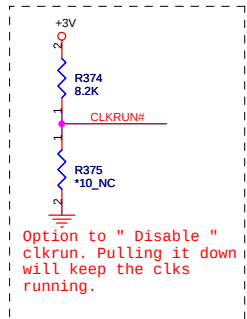


Reserved for EMI. Place resistor and cap close to ICH.



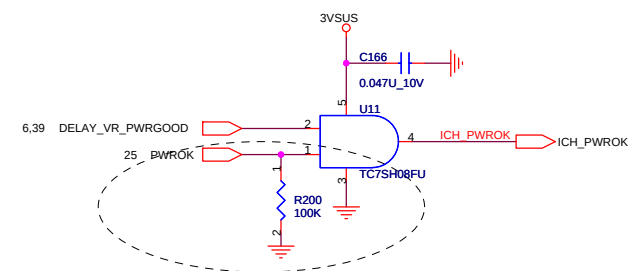
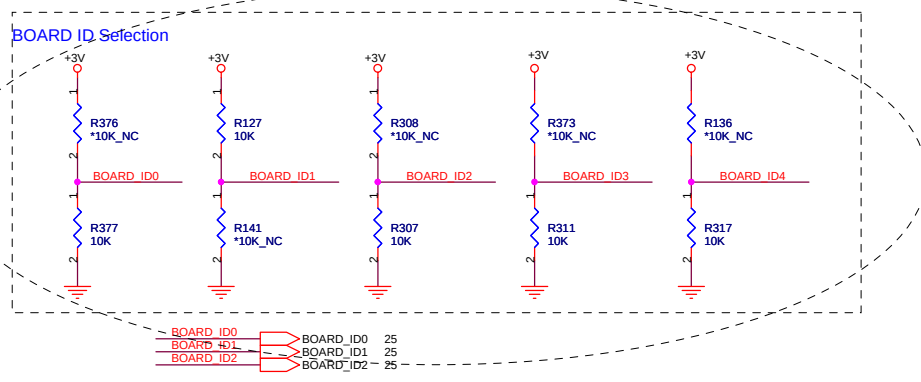
PROJECT : SW1
Quanta Computer Inc.

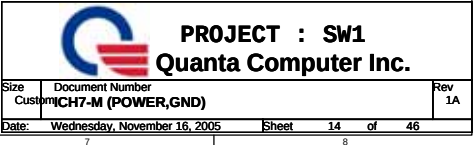
Size	Document Number	Rev
Customer	CH7-M (USB,DMI,PCIE,PCI)	1A
Date:	Wednesday, November 16, 2005	Sheet 12 of 46

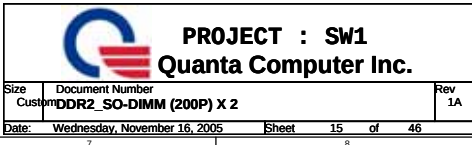


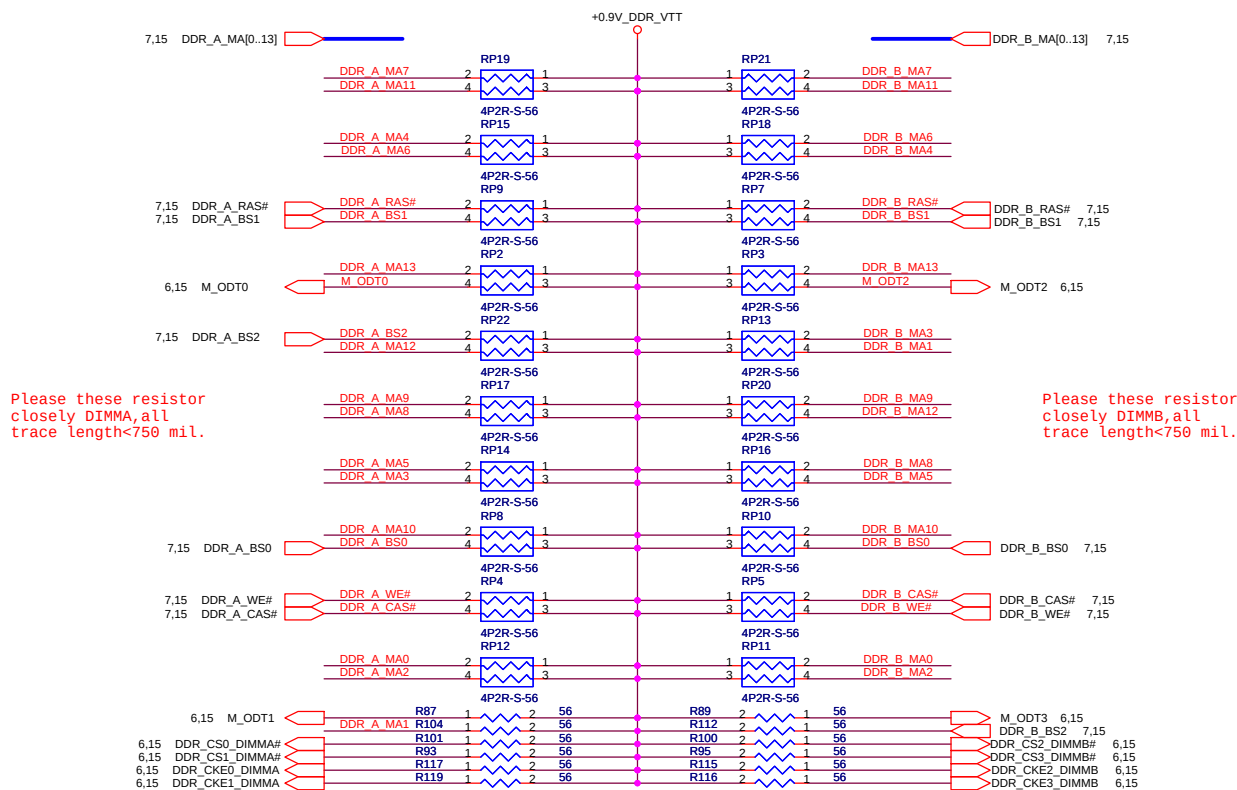
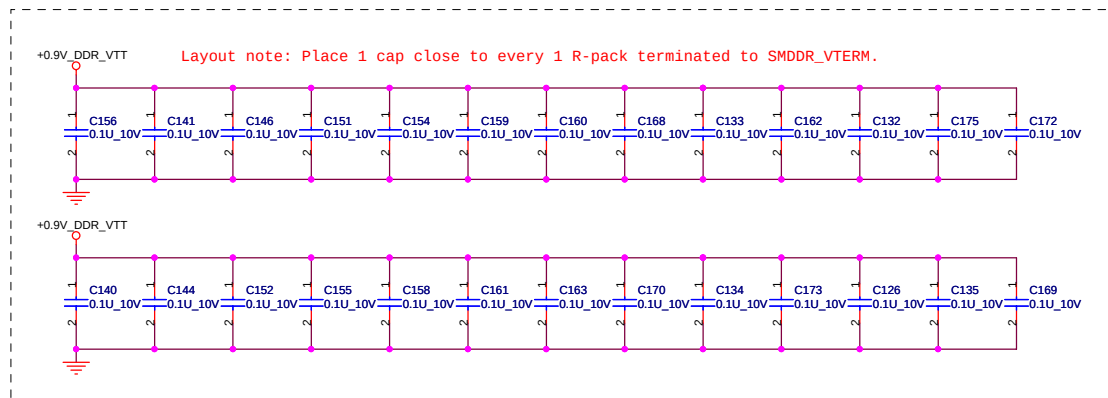
MBID Table	MBID0	MBID1
TW3	Low	Low
DW1	High	Low
SW1	Low	High
...	High	High

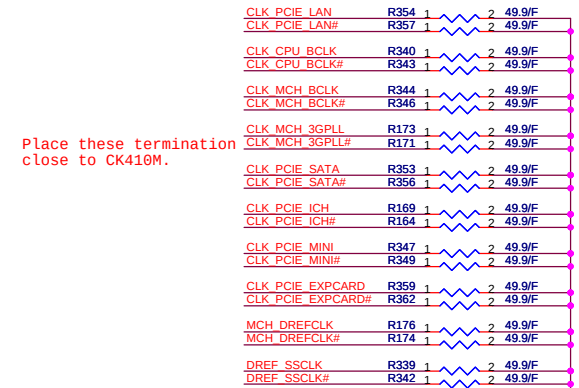
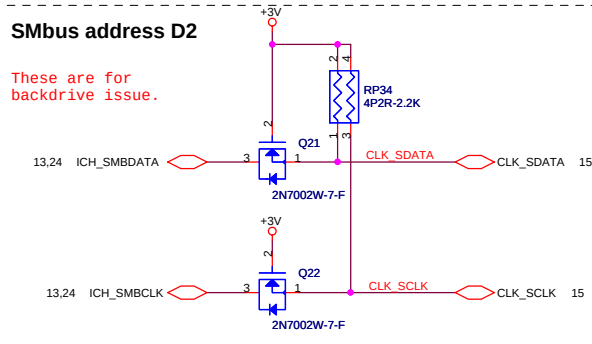
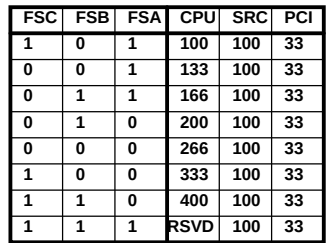
MBID2	
SATA	Low
PATA	High



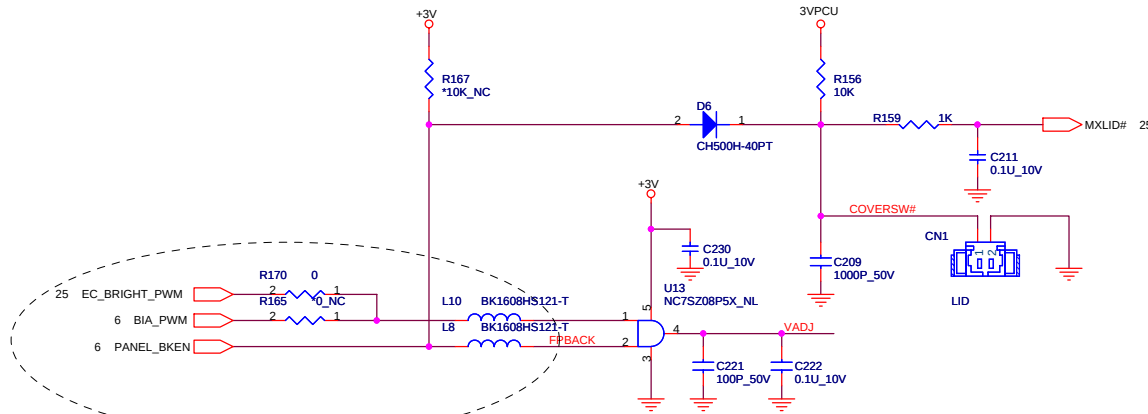
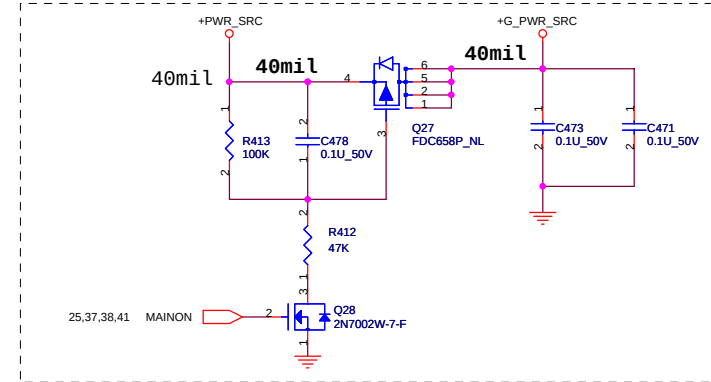
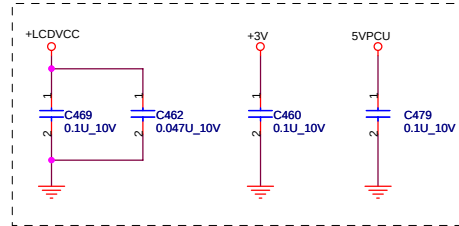
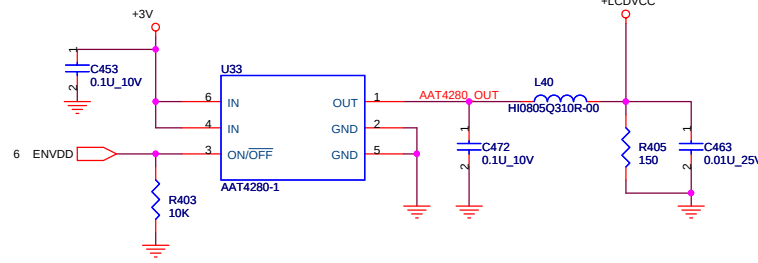
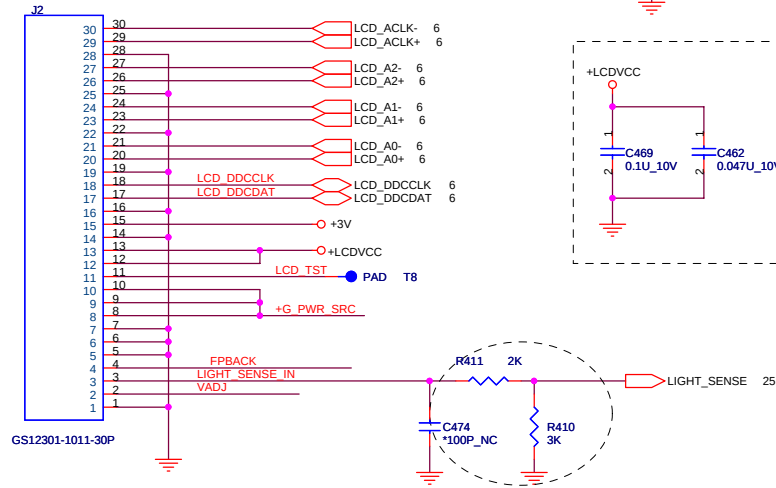




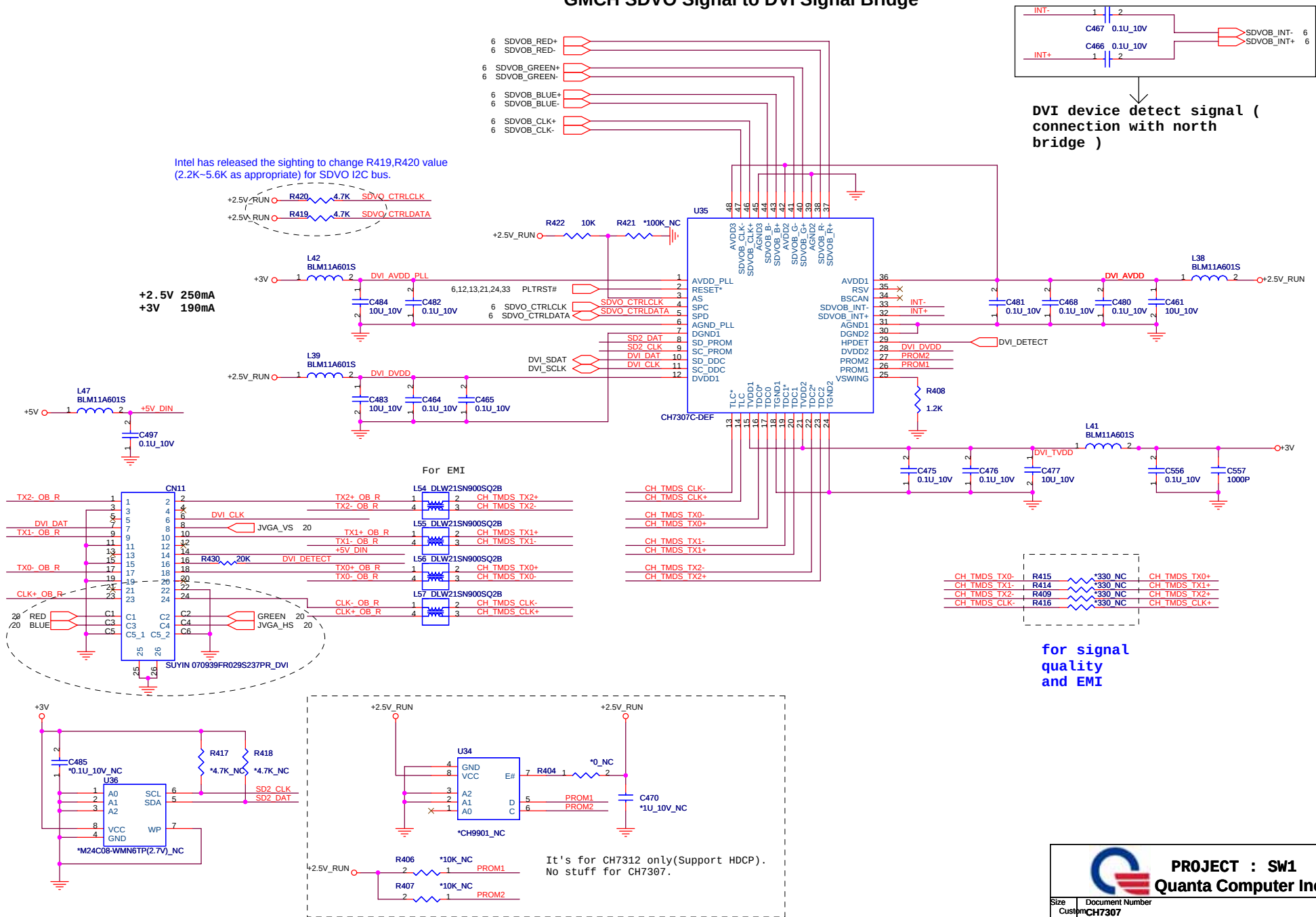




LCD CONNECTOR

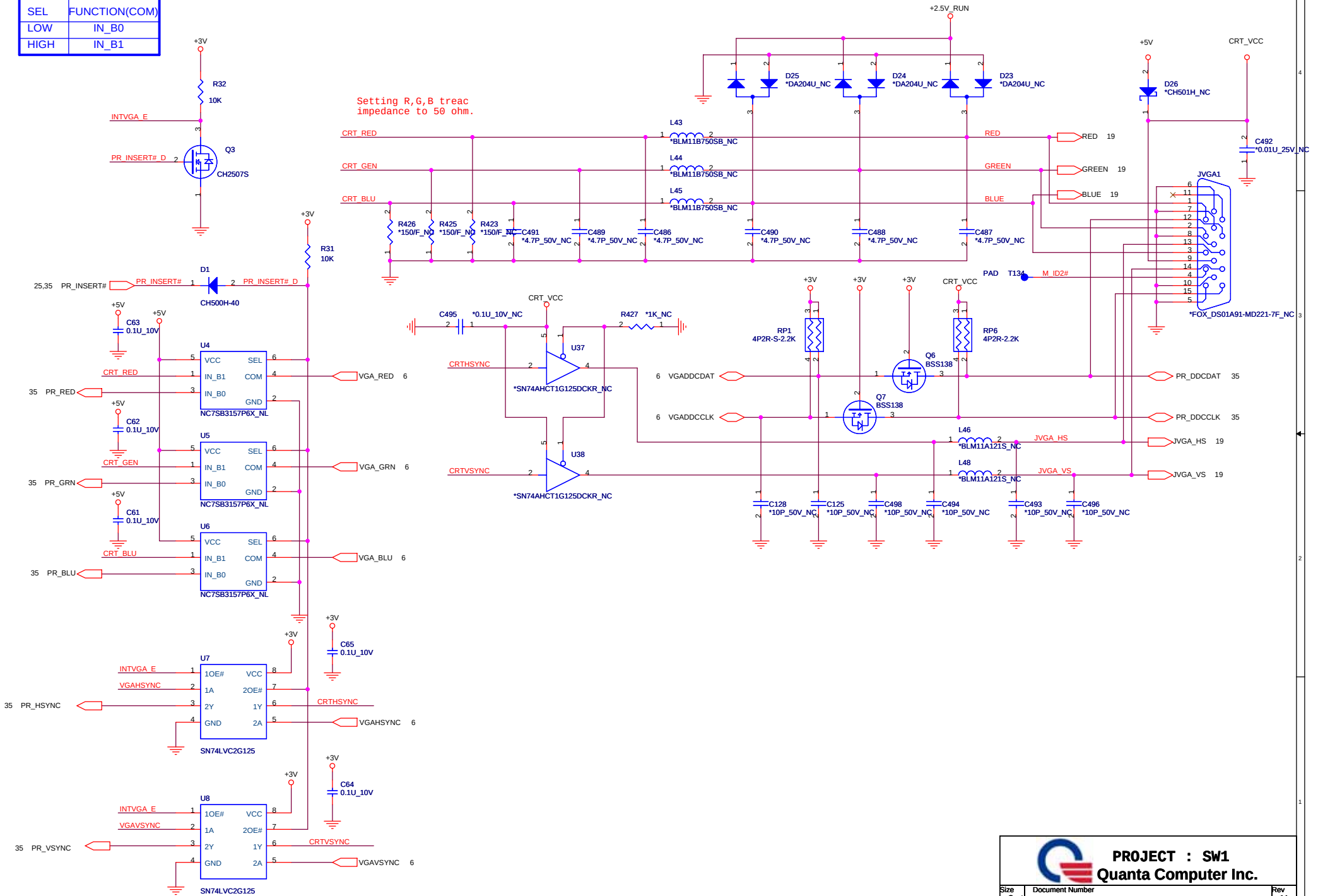


GMCH SDVO Signal to DVI Signal Bridge

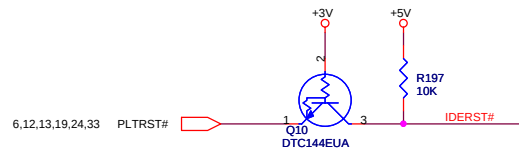
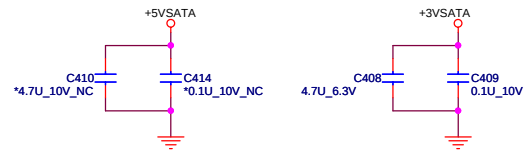
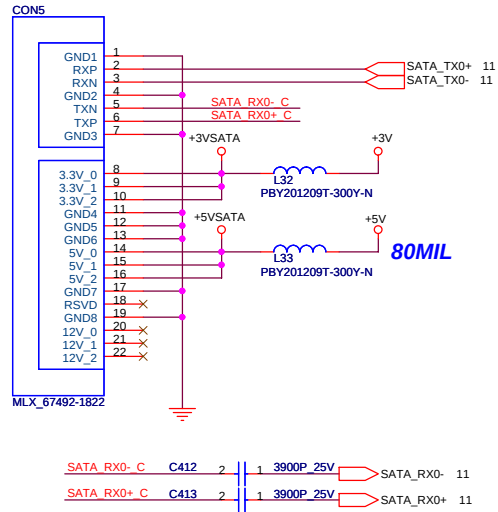


CRT SWITCH

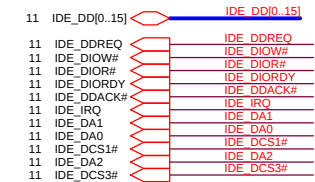
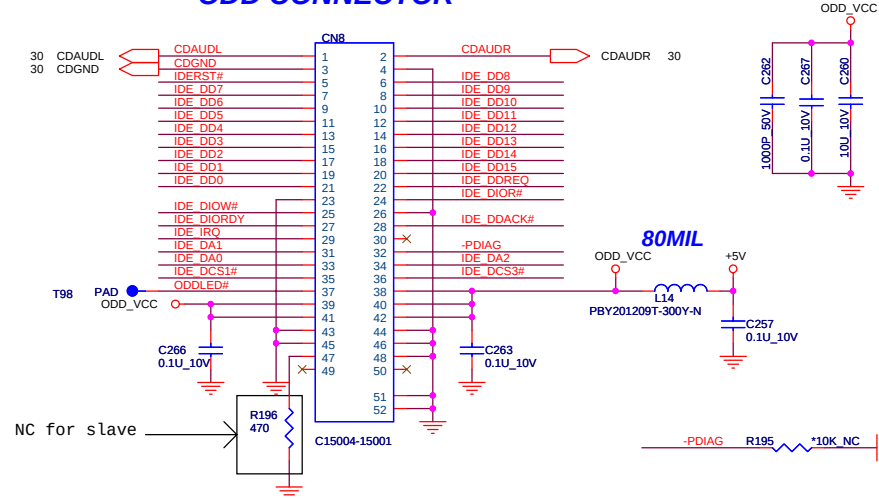
SEL	FUNCTION(COM)
LOW	IN_B0
HIGH	IN_B1



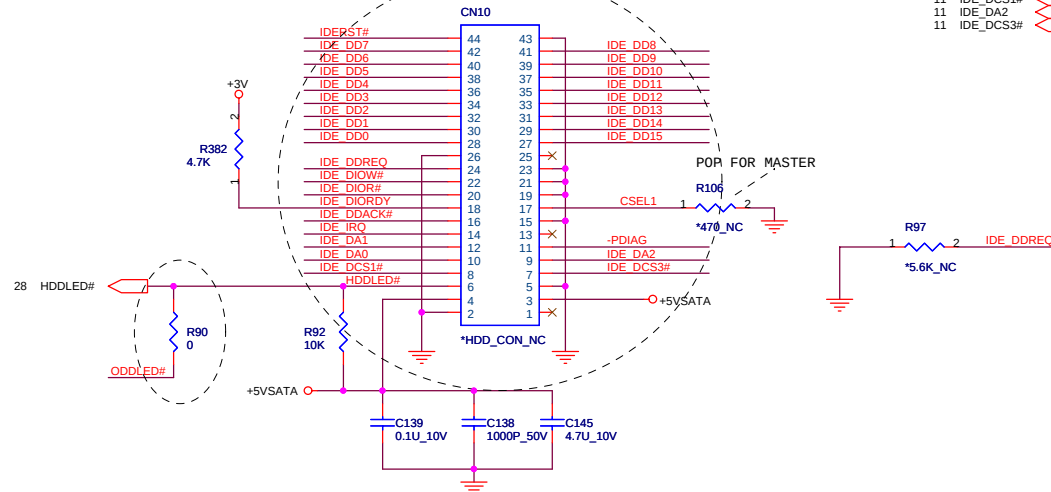
SATA Connector.

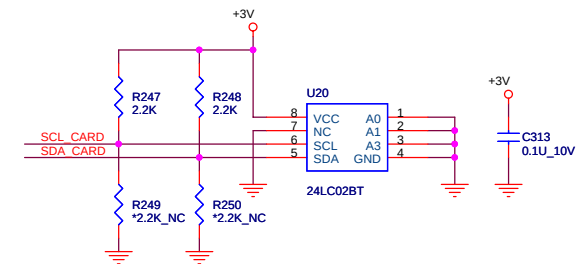
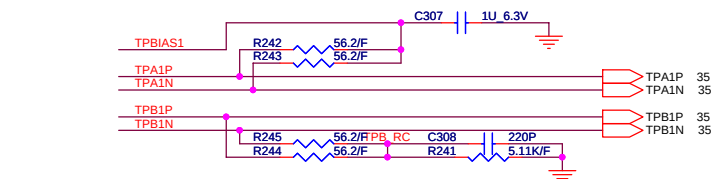
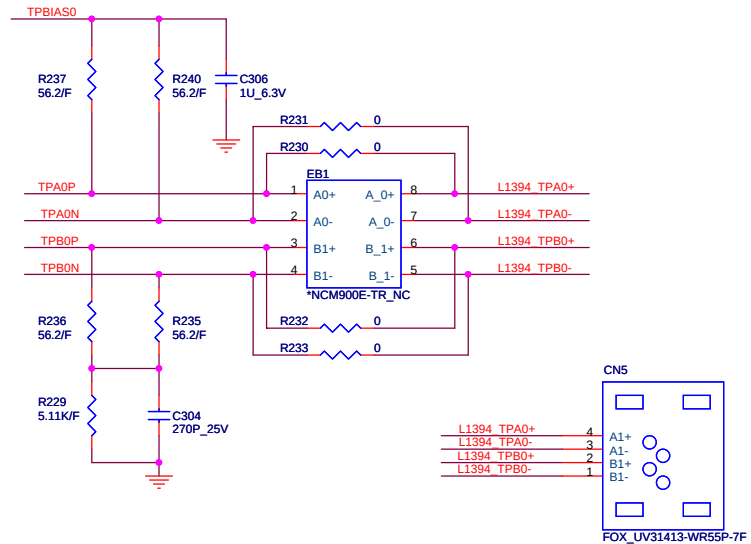


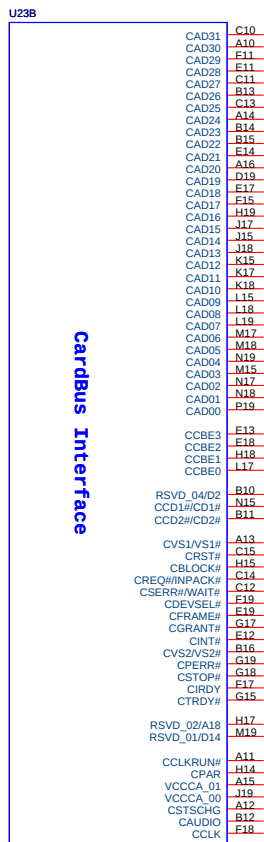
ODD CONNECTOR



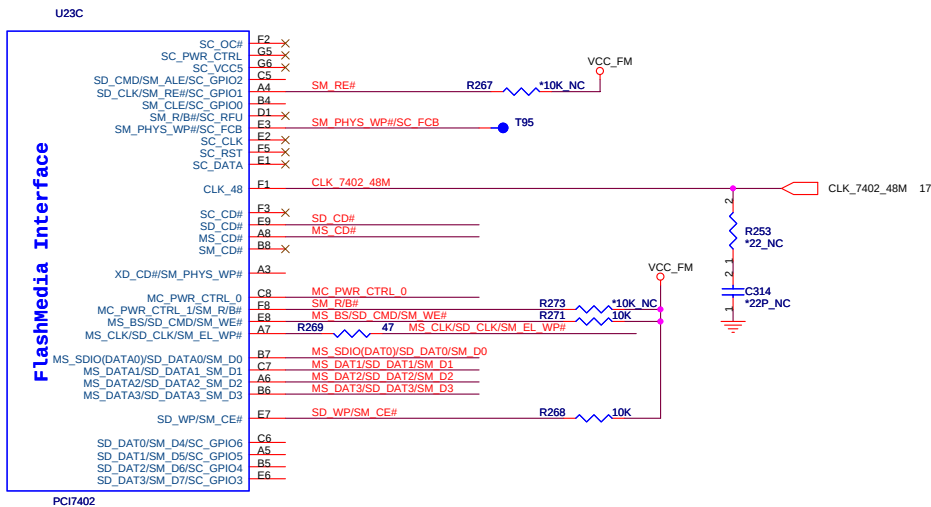
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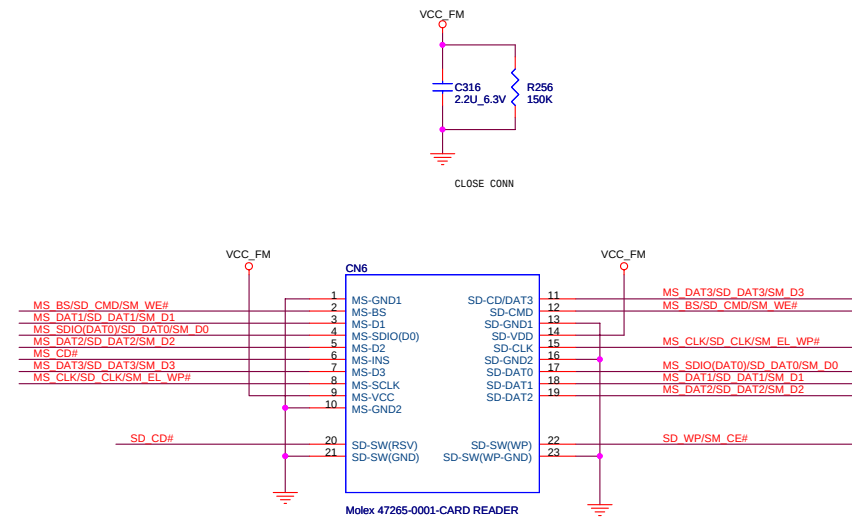
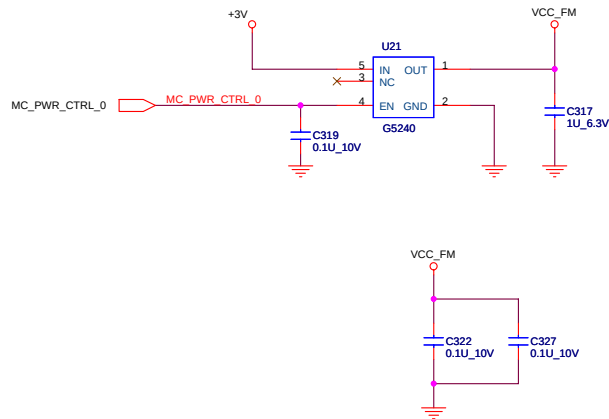


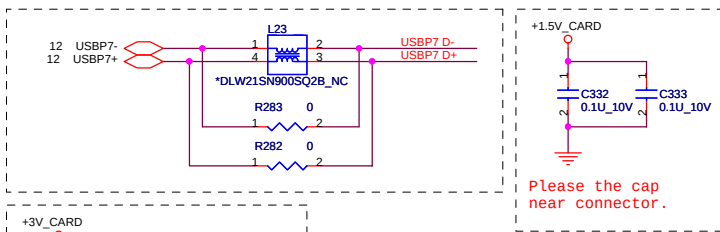


PCI7402

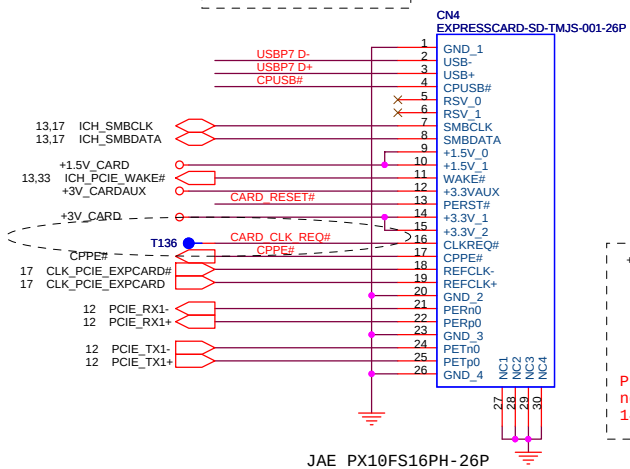
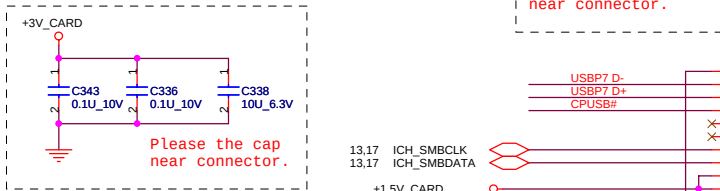


For SD/MS power

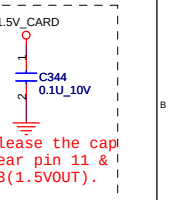
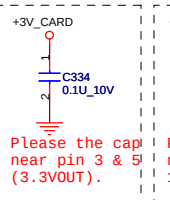
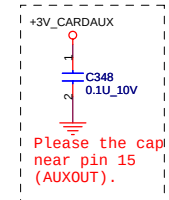
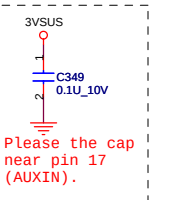
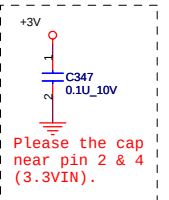
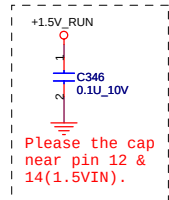
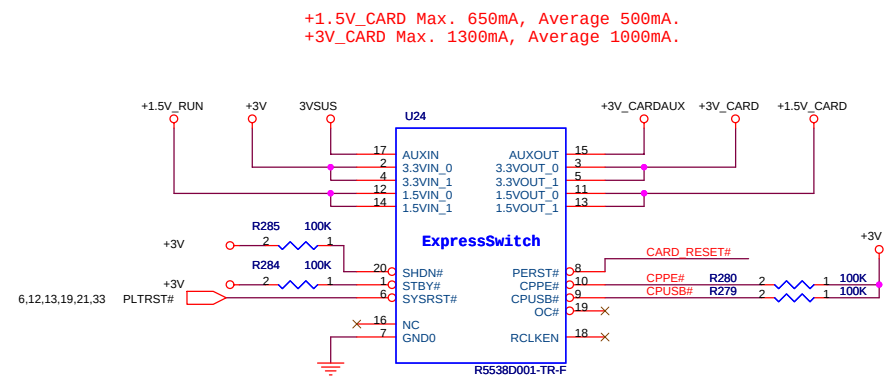




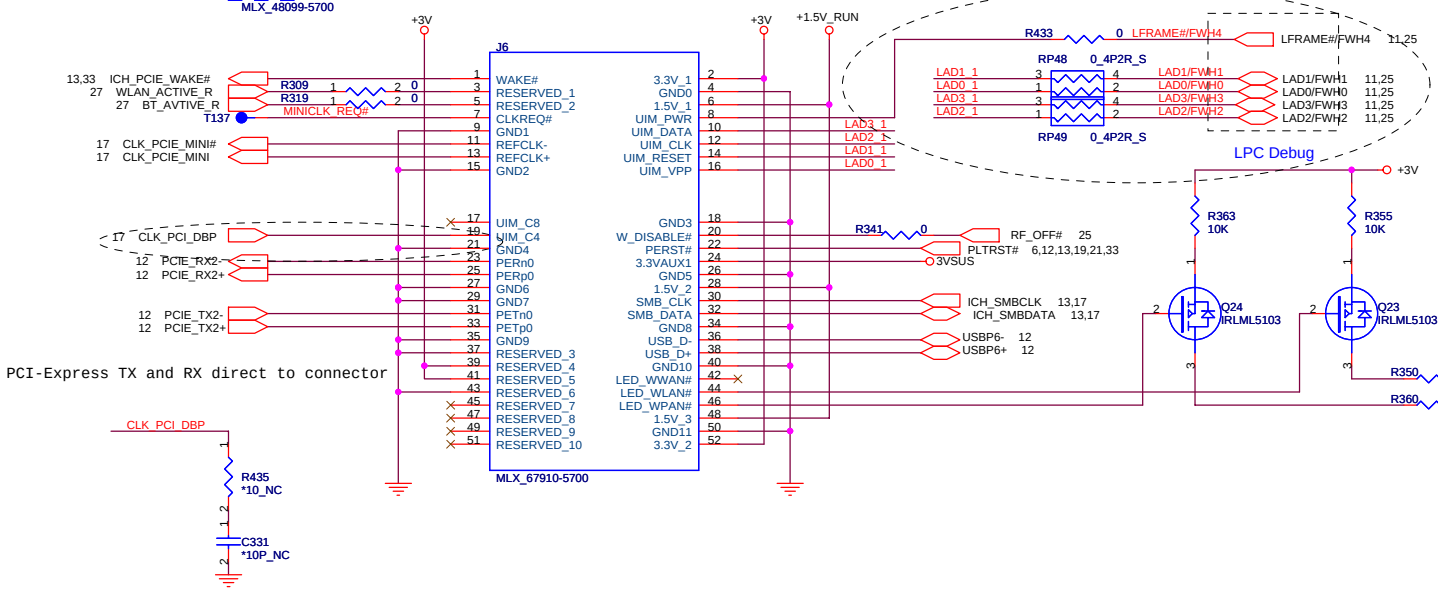
Express Card



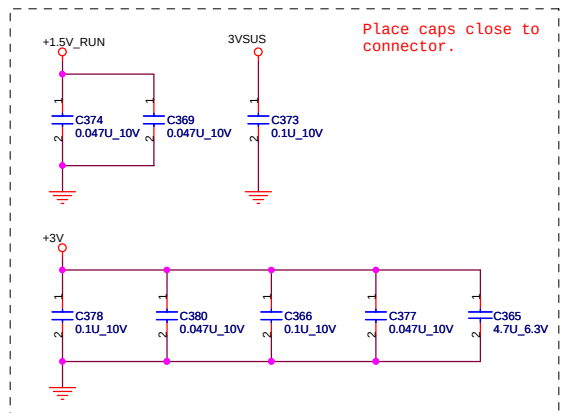
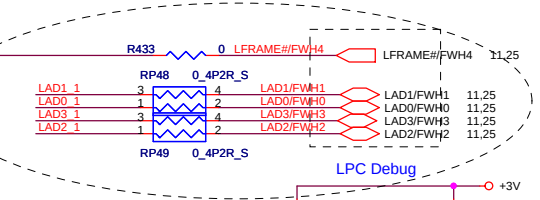
PCI-Express TX and RX direct to connector.



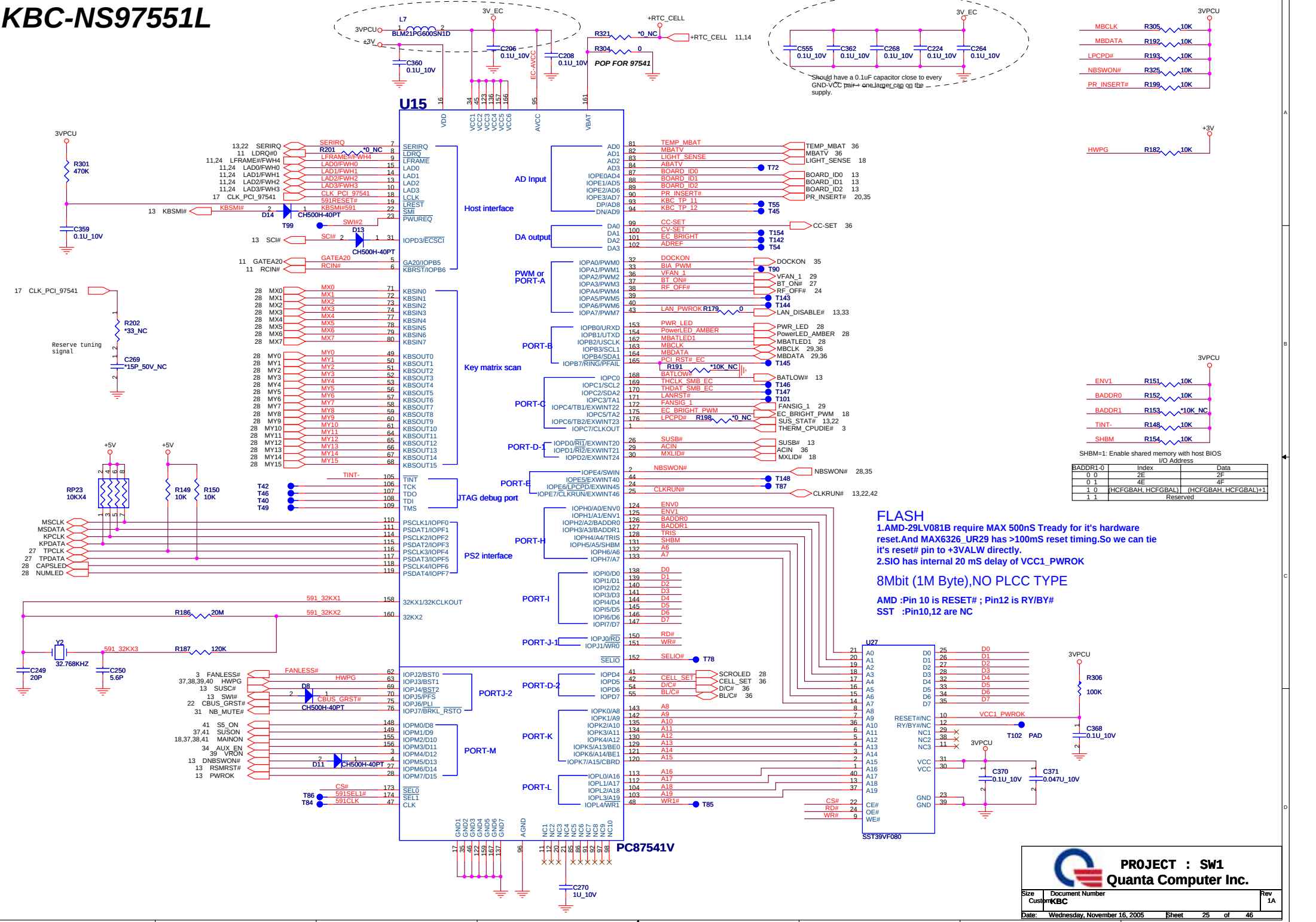
MiniCard WLAN connector



PCI-Express TX and RX direct to connector



KBC-NS97551L

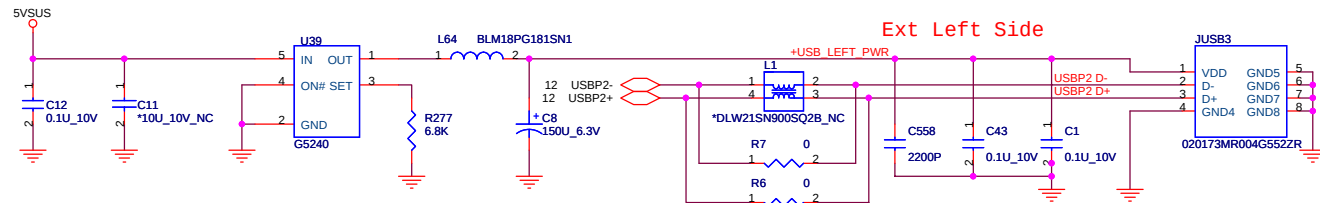
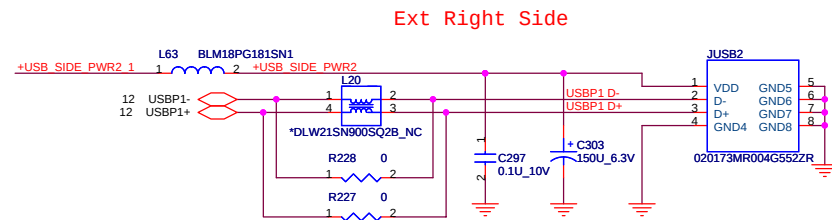
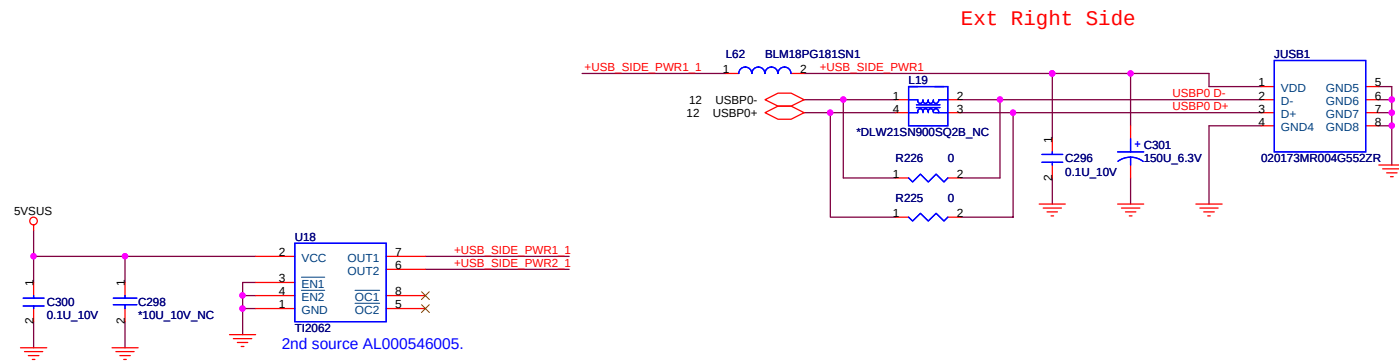


SHBM=1: Enable shared memory with host BIOS

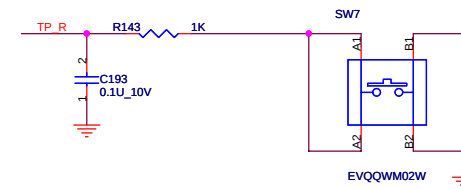
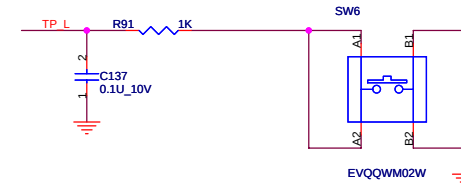
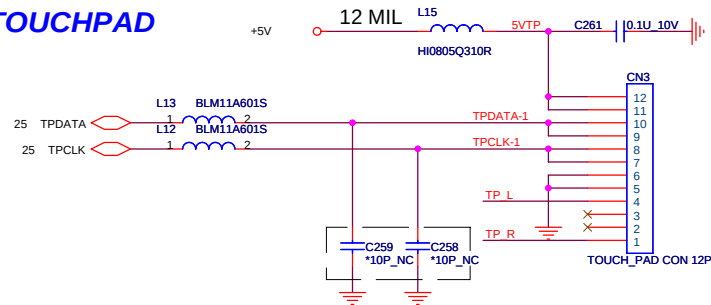
BADDR1-0	Index	I/O Address	Data
0 0	2E		2F
0 1	4E		4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1	
1 1		Reserved	

FLASH
1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326 UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
2.SIO has internal 20 mS delay of VCC1_PWROK

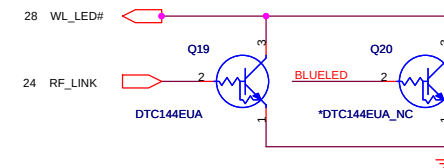
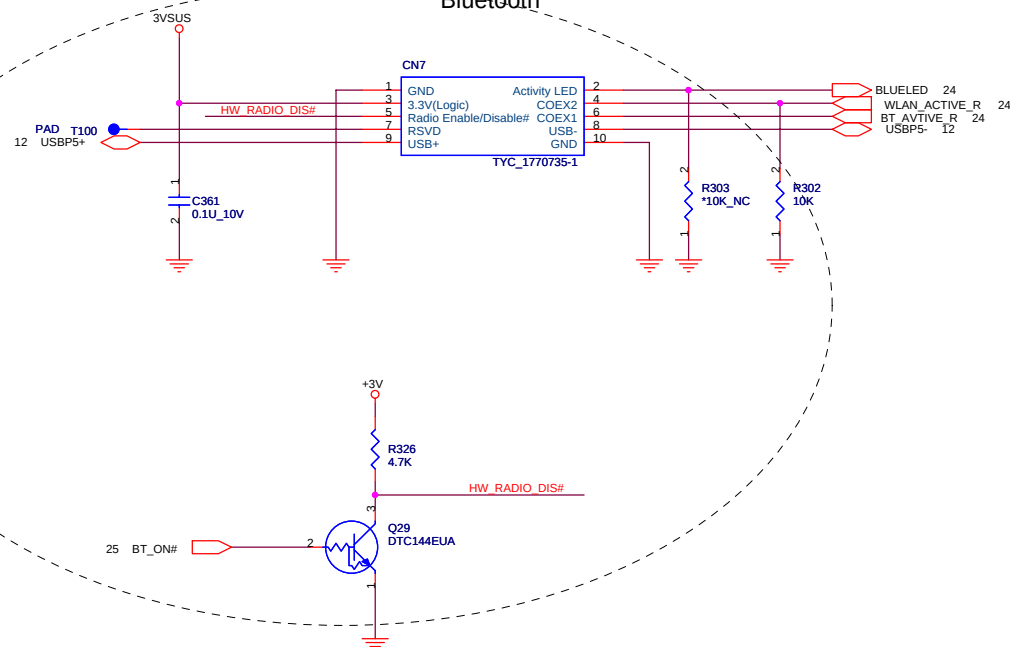
8Mbit (1M Byte),NO PLCC TYPE
AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC



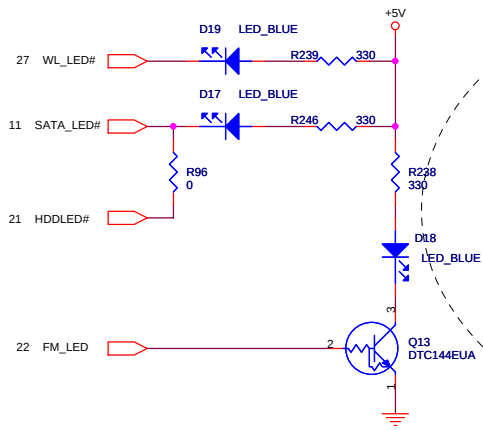
TOUCHPAD



Bluetooth



LED



AC Present (Orange)

System power (Blue)

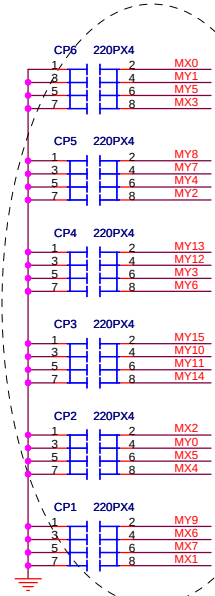
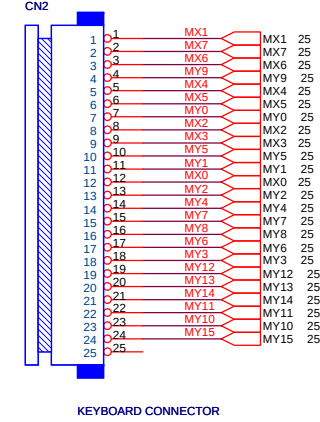
25 PWR_LED

25 MBATLED1

Status:
1. Charge - ON
2. Discharge - OFF

B stage:
Change color from blue to orange

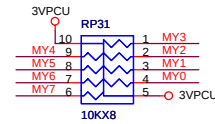
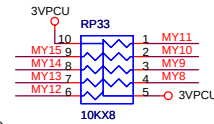
KEYBOARD



WLAN

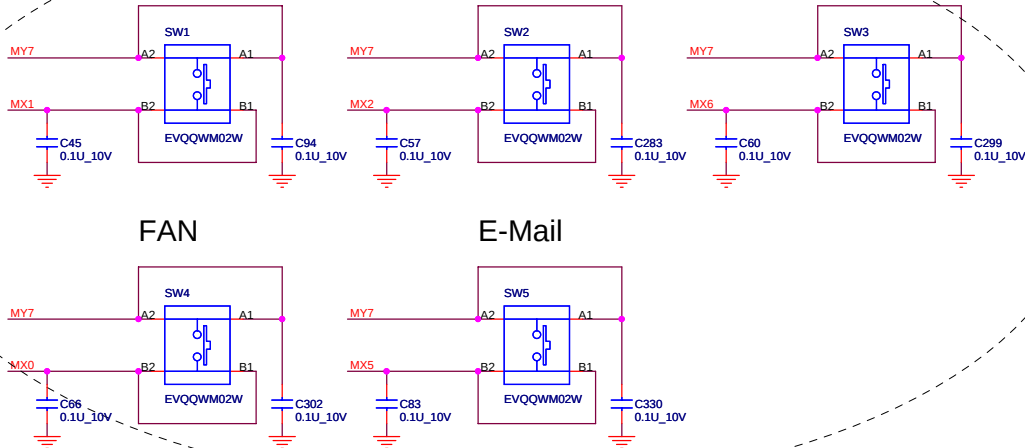
IE

MUTE

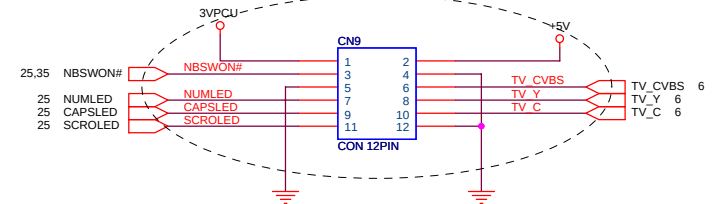


FAN

E-Mail

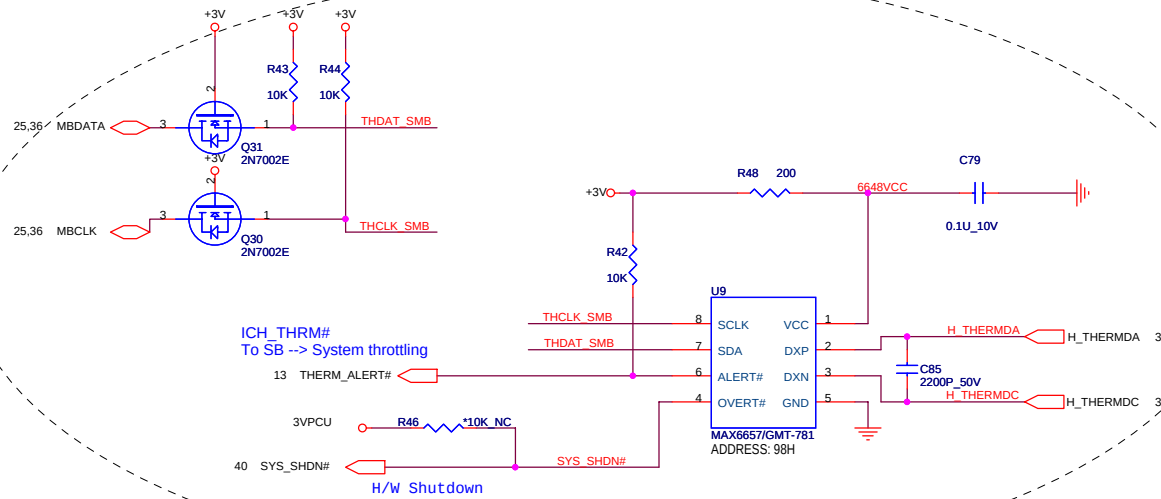
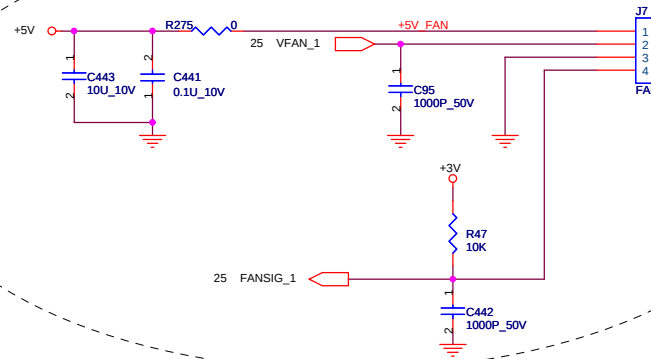


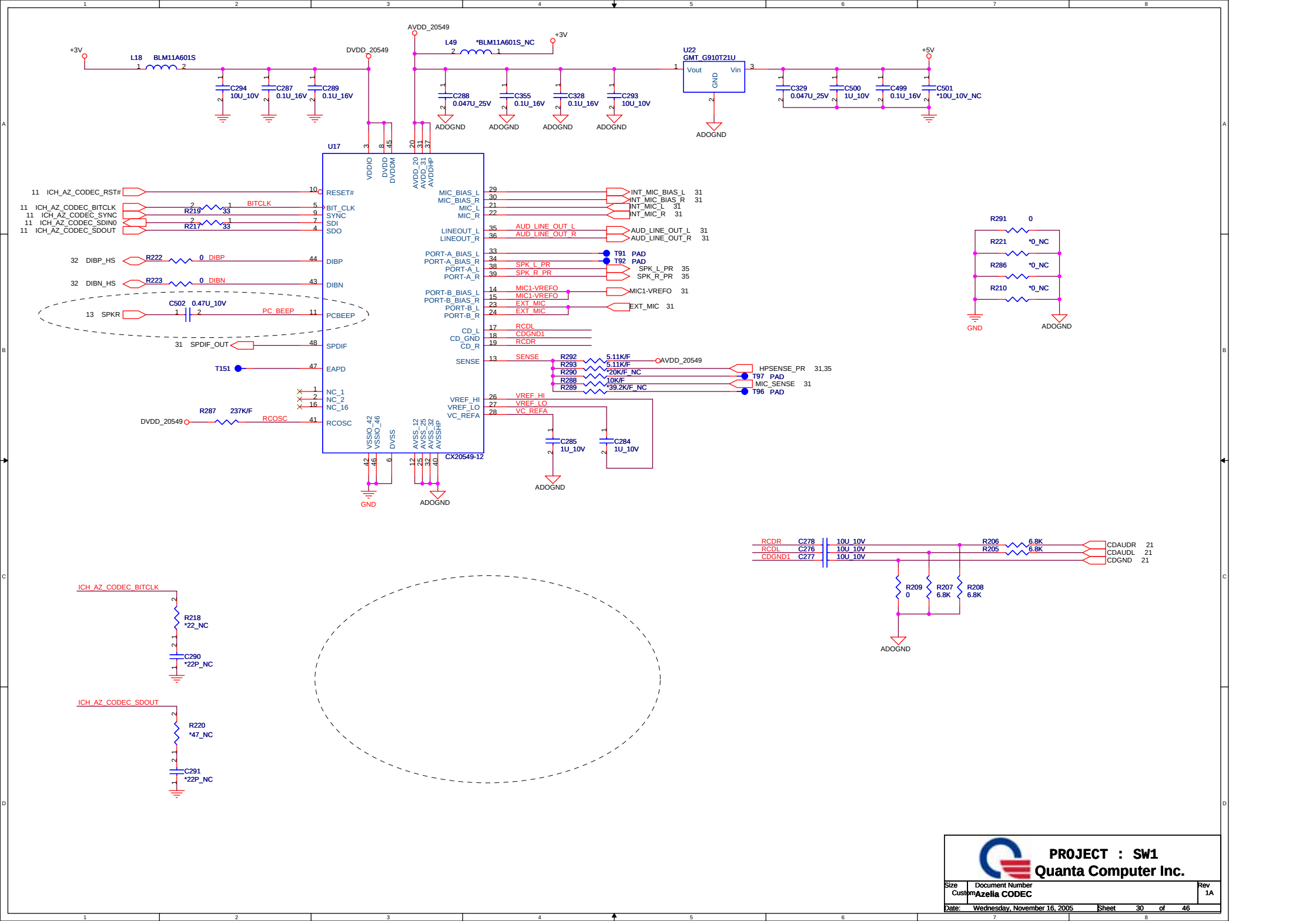
I/O Board CONN



PROJECT : SW1
Quanta Computer Inc.

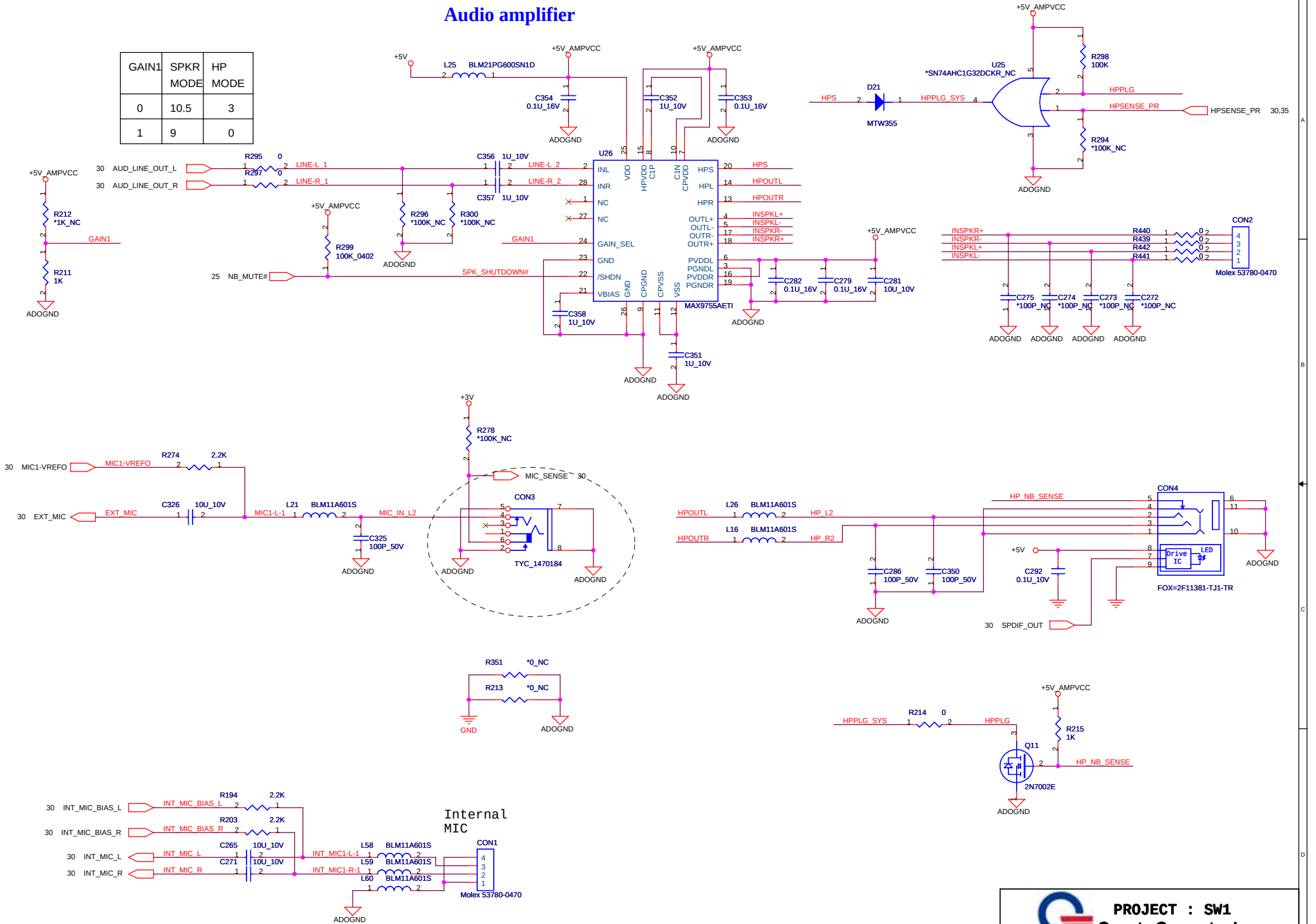
1st FAN OUT CONNECTOR

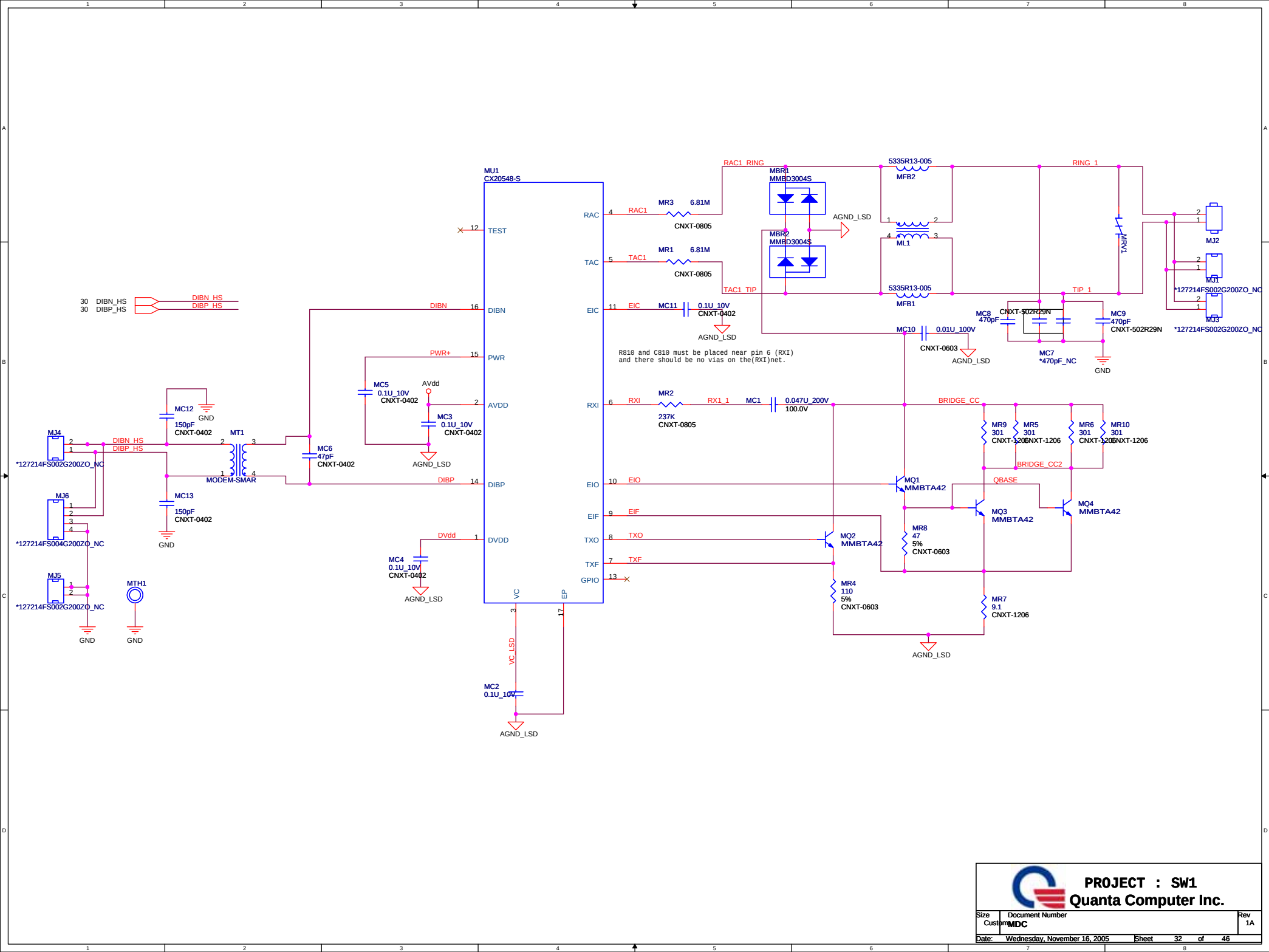


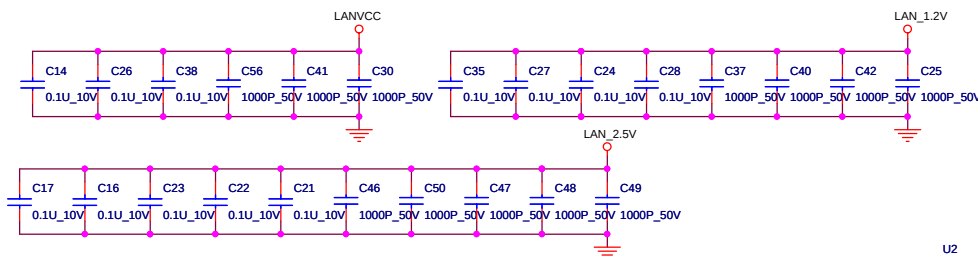


Audio amplifier

GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0





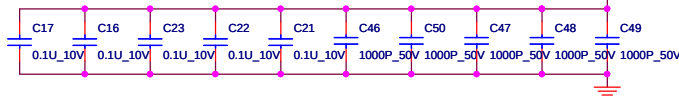


C: 88E8053 LF PN: AJ080530010 (20050411)
1Mbits

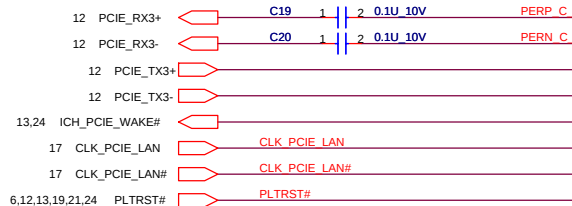
C: Add 9 X GND Pad for LAN controller.
(20050411)

C: Add these GND pin for via hole to GND Plane.

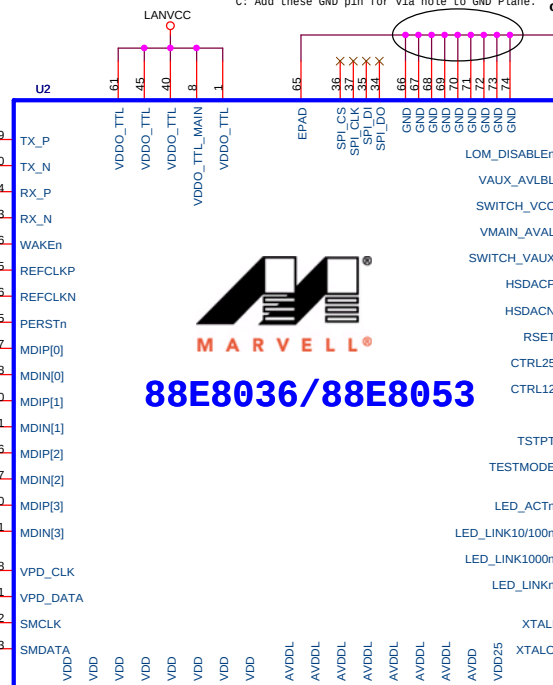
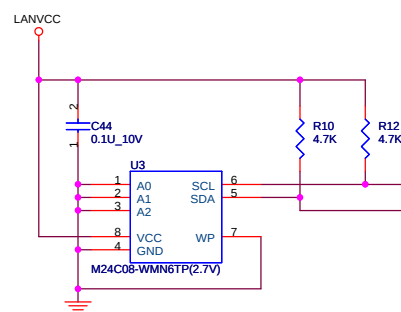
C: Add RC (R37 change to 200K, Add C101) delay to control LOM_DISABLE#. (20050411)



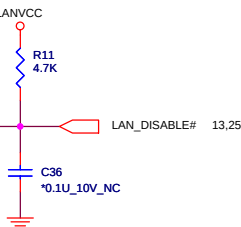
C: Reserve R36. Change LANRST# to PCIRST# source from MB option modify. (2005/04/11)



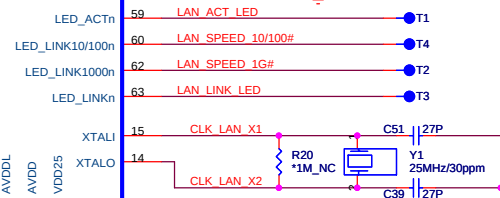
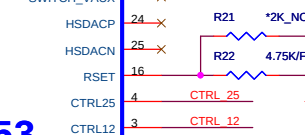
DELAY PIN10 AT LEAST 150ms



MARVELL®
88E8036/88E8053

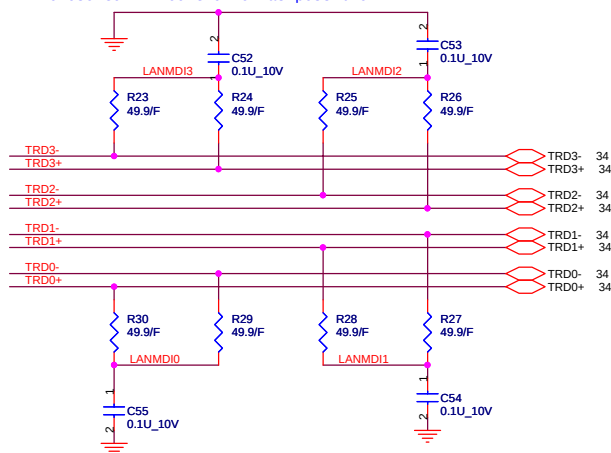


Populate R21 for 10/100
Populate R22 for 10/100/1000

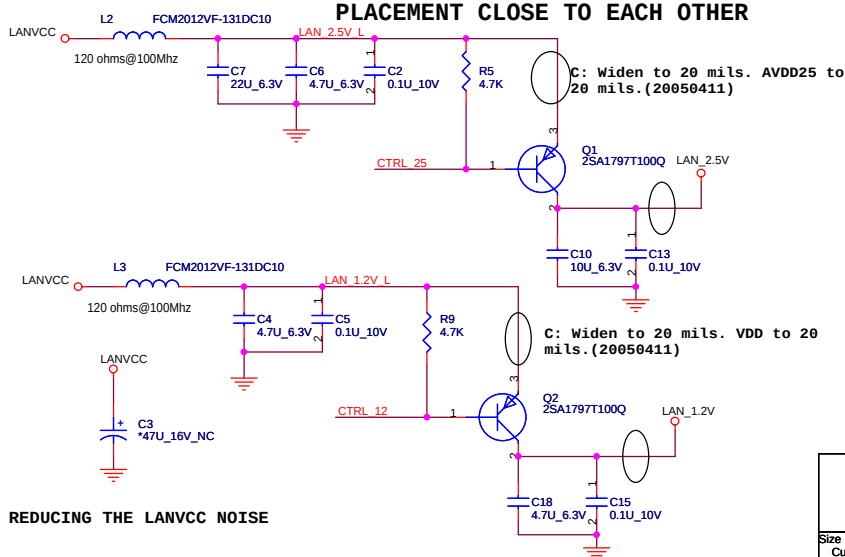


LAN_1.2V LAN_2.5V

A1A: Place termination resistors and caps as close to LAN controller as possible

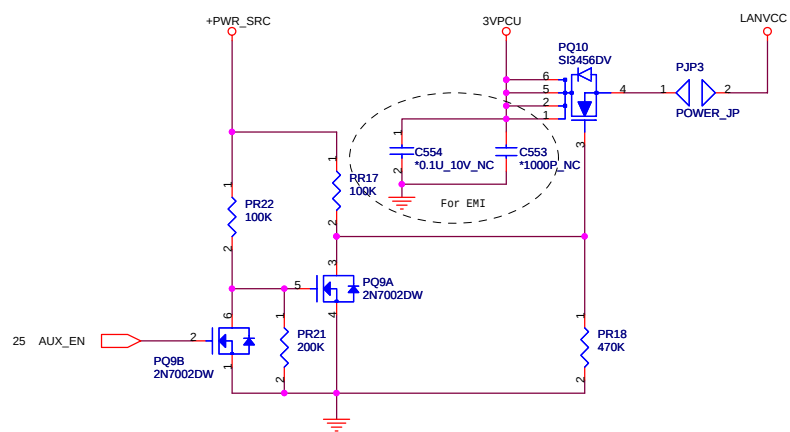
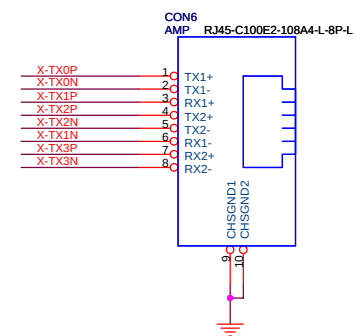
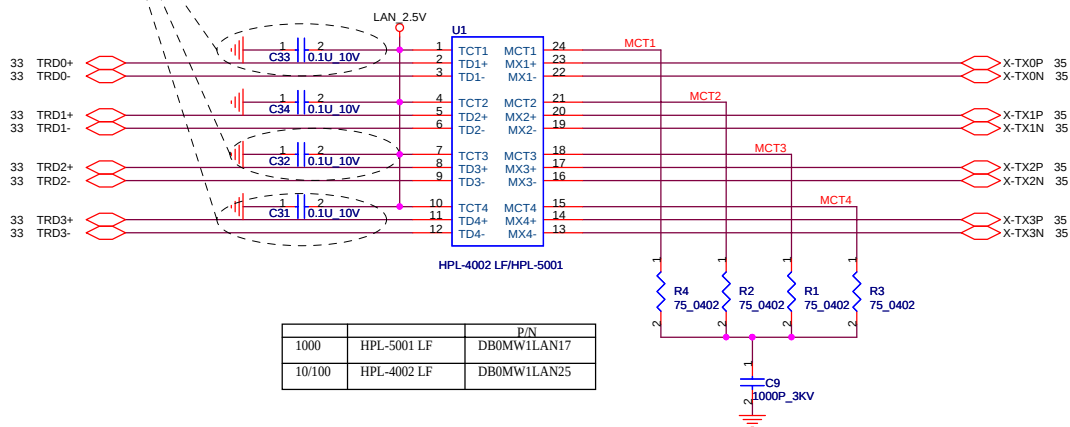


PLACEMENT CLOSE TO EACH OTHER

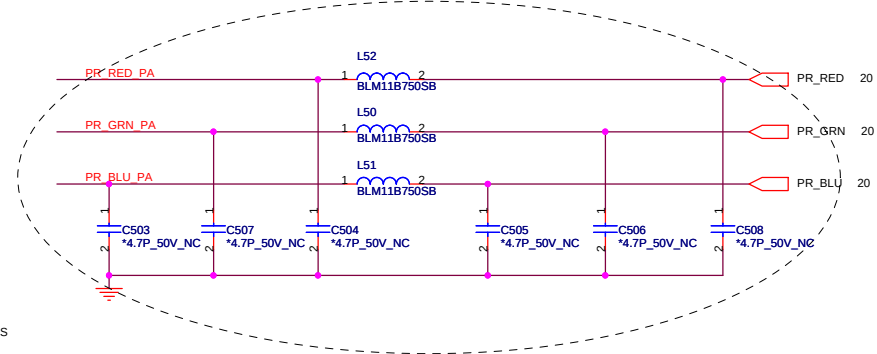
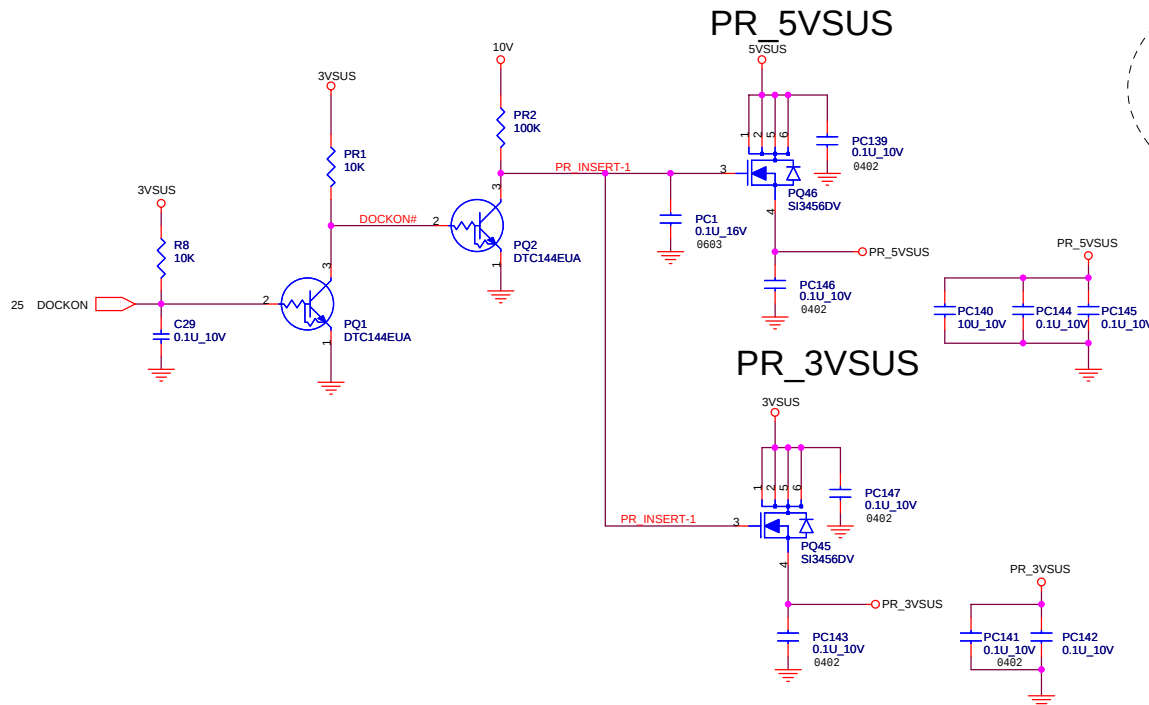
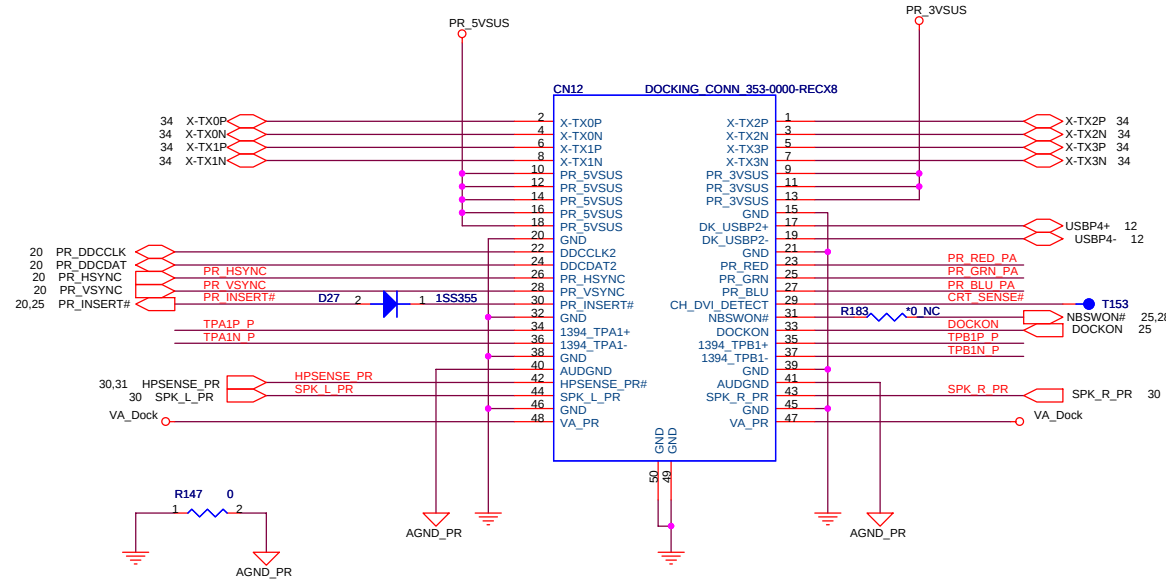


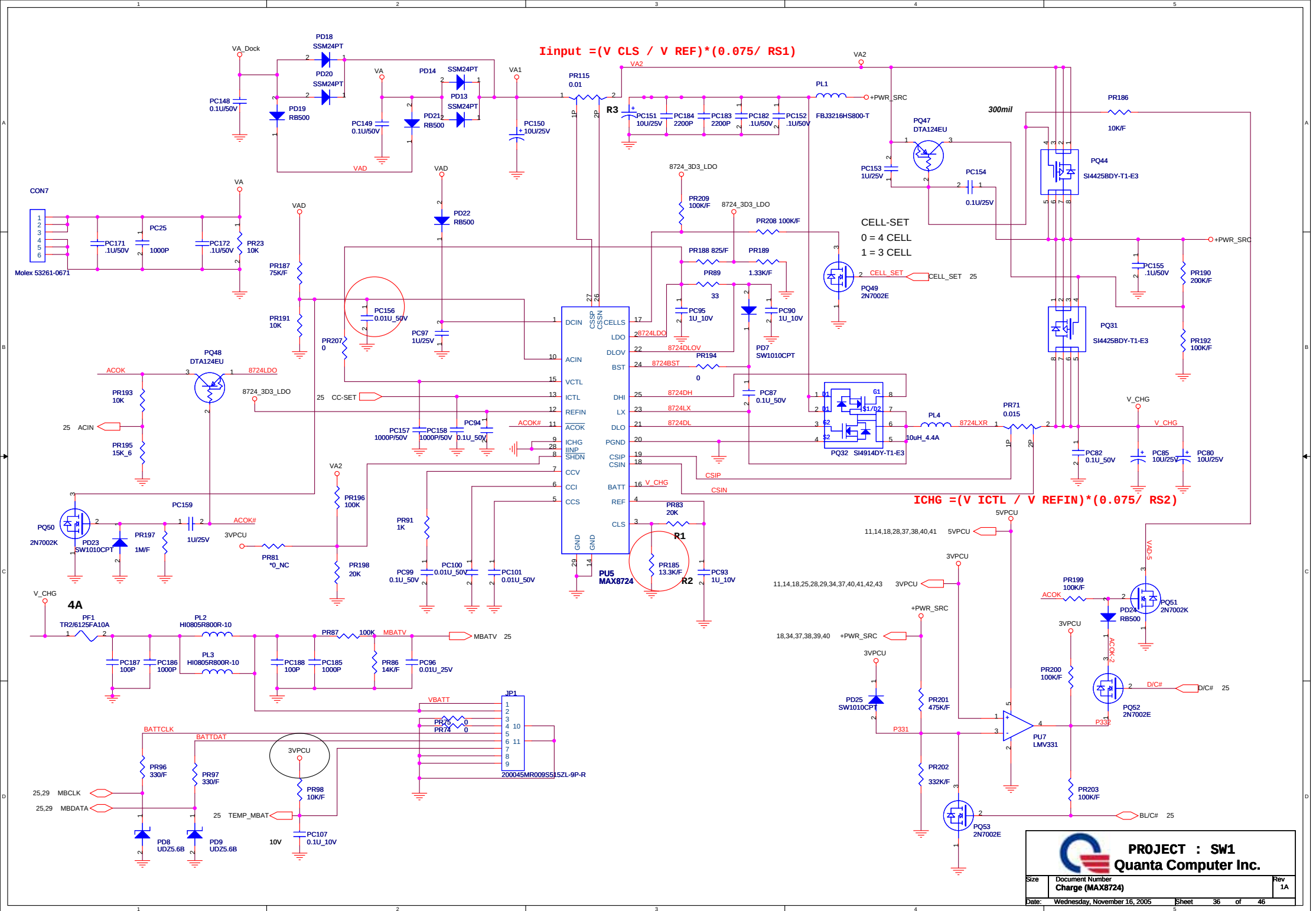
0804 REDUCING THE LANVCC NOISE

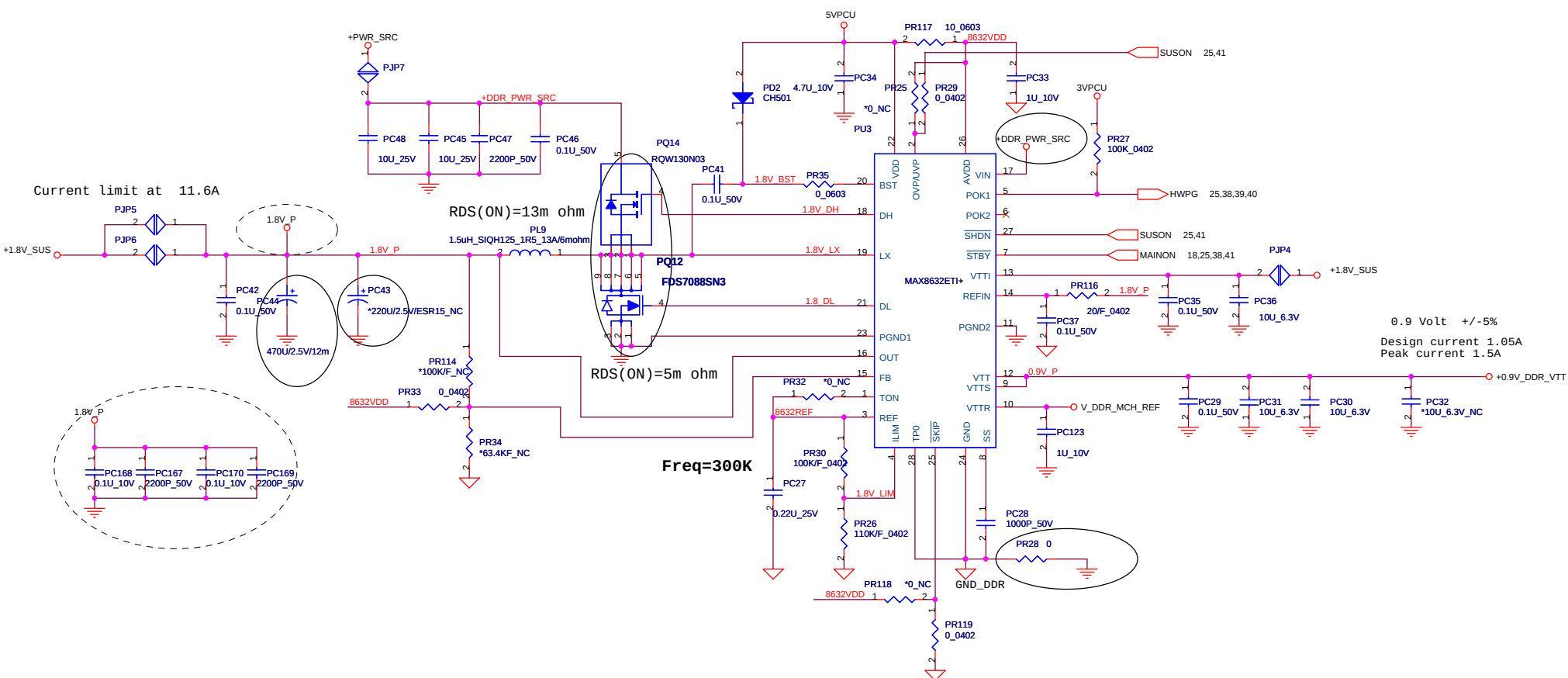
Populate for 82573



CABLE DOCKING CONNECTOR







10/19 add for MAX8771 version 2 bug.

10/19 add for MAX8771 version 2 bug.

Place close to IC pin 27

Add layout note on pins 22 and 28 of MAX8771 controller. These nets have large voltage swings. Need to route them away from the sensitive areas that are trying to detect small changes in voltage, such as the voltage sense VccSense VssSense lines.

10/19 change to 237K for heavy load jitter issue

10/19 change to 1000P for heavy load jitter issue

distribute evenly between N side and S side, preferably on secondary side.

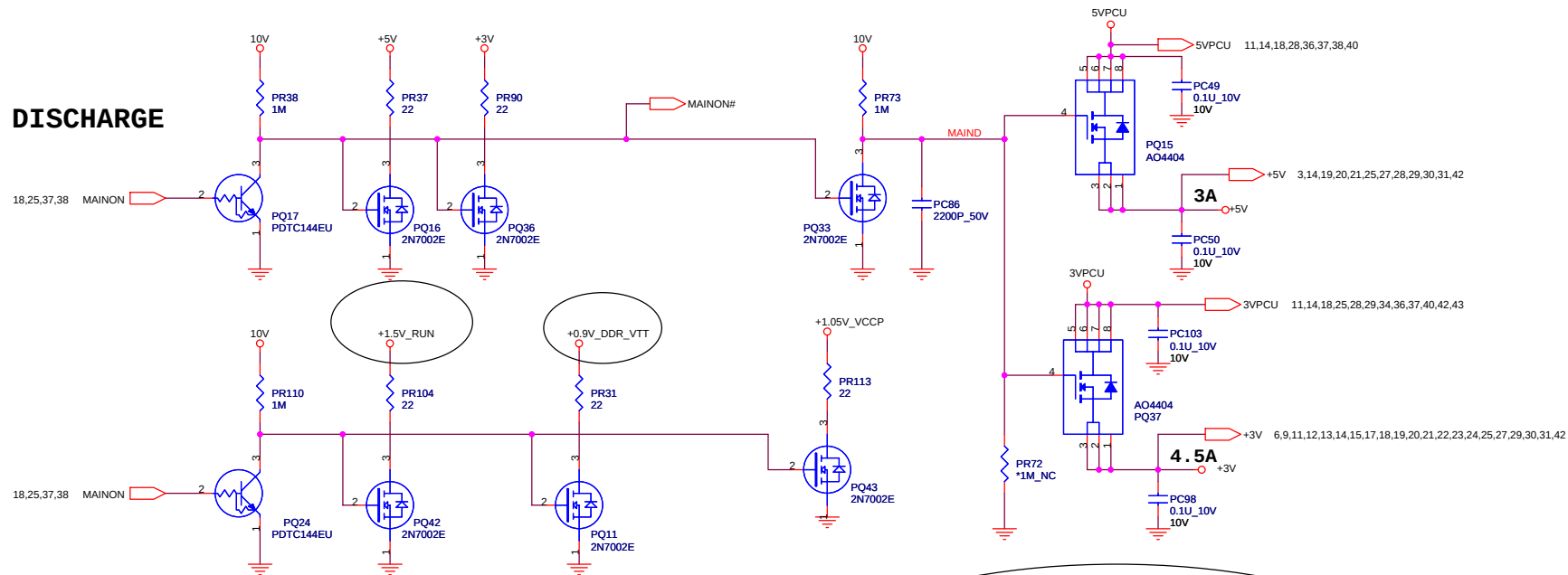
Use differential routing away from switch nodes 8771LX1 and 8771LX2

distribute evenly between N side and S side, preferably on secondary side.

Sense lines are 18 mil wide, Z0=27.4 Ohm. Use differential routing with 7 mil spacing. Route external layer with solid GND reference (no split planes). Use 25 mil separation from any other signal.

Use differential routing away from switch nodes 8771LX1 and 8771LX2

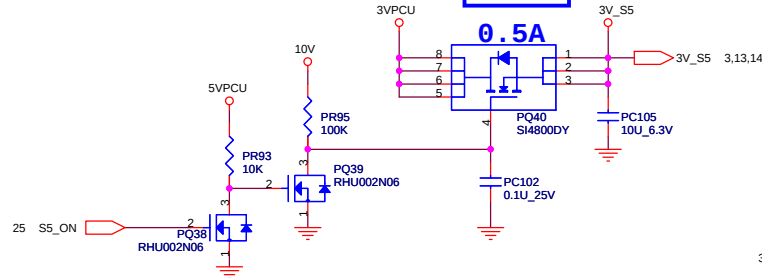
DISCHARGE



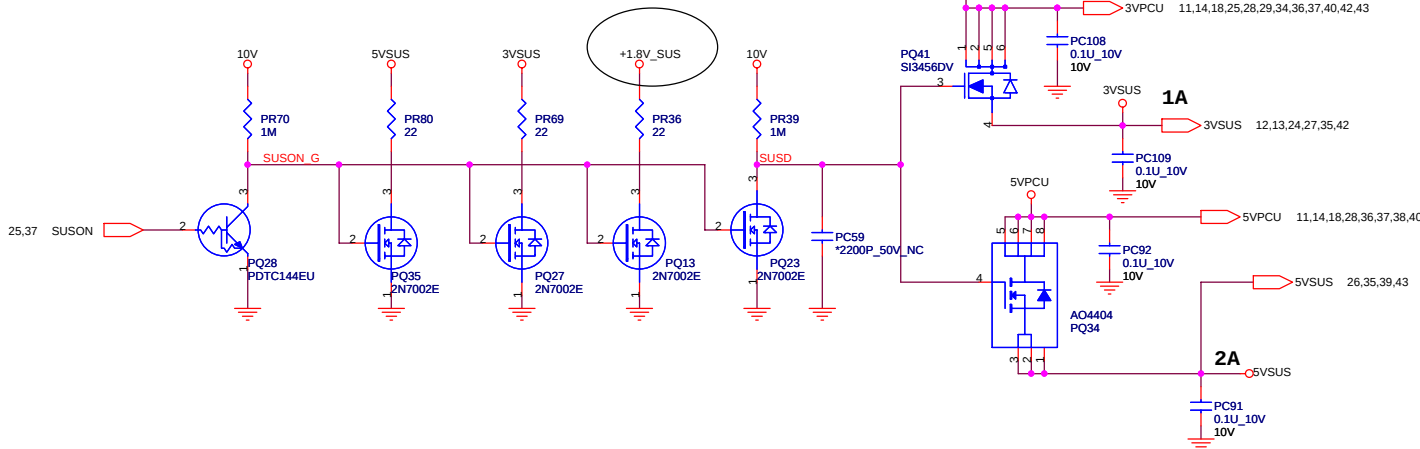
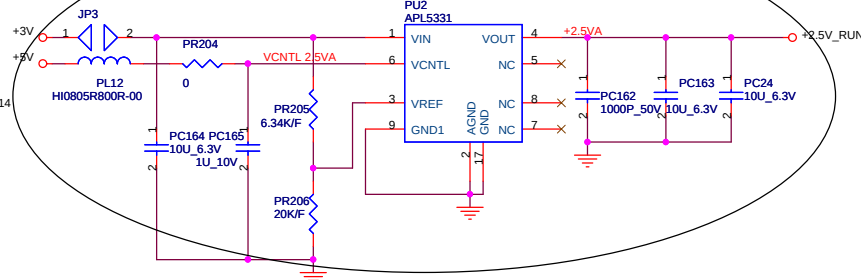
200mils

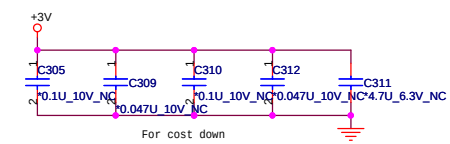
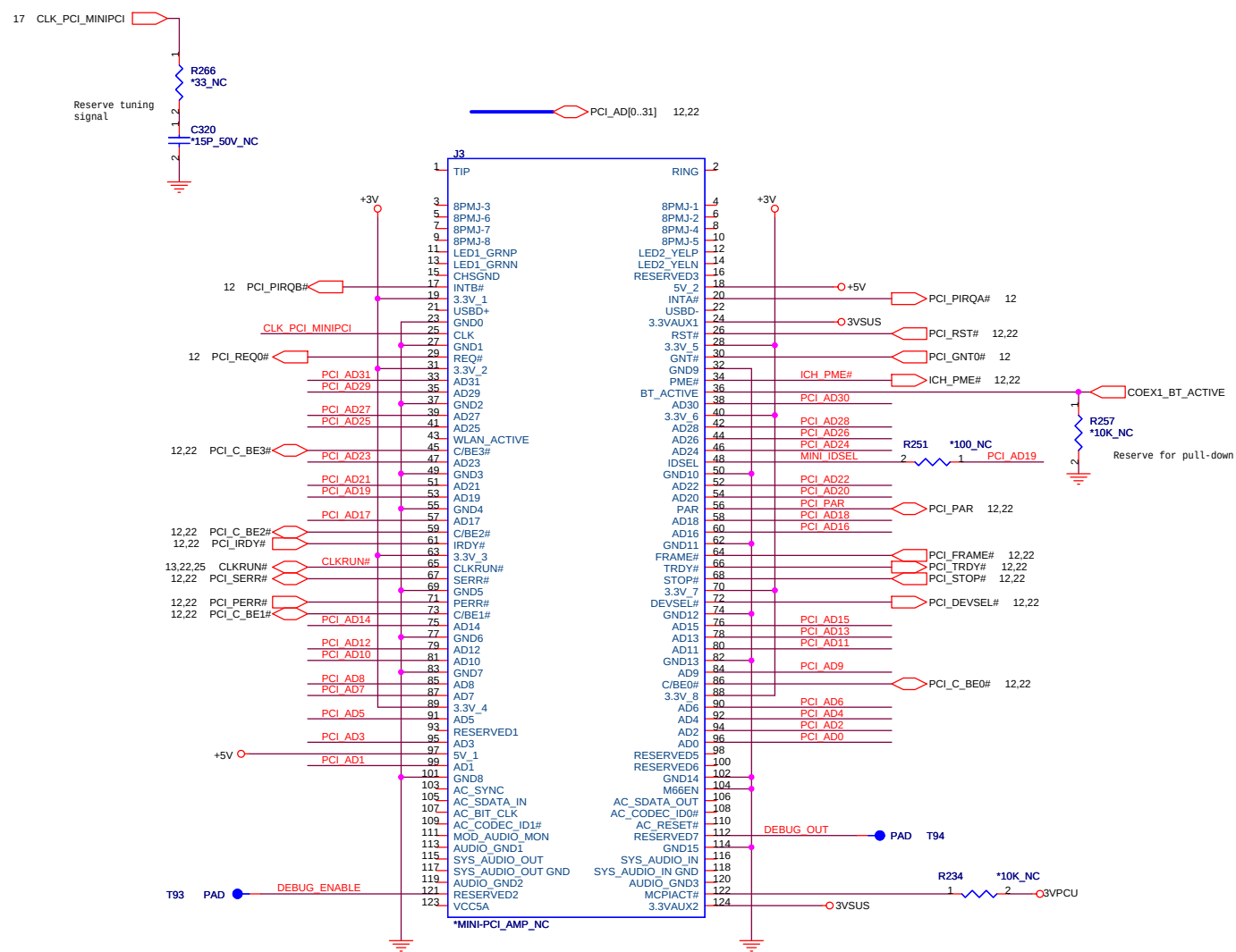
S0-S5

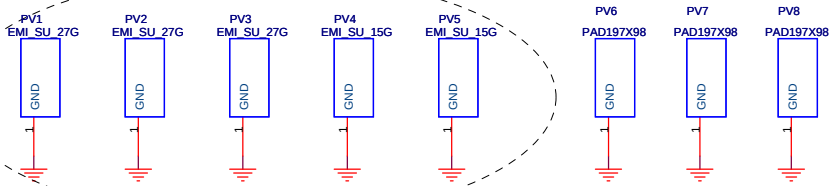
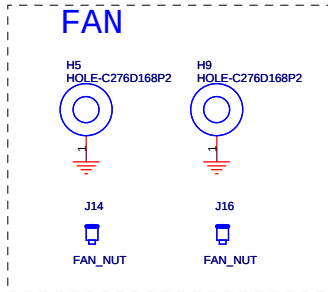
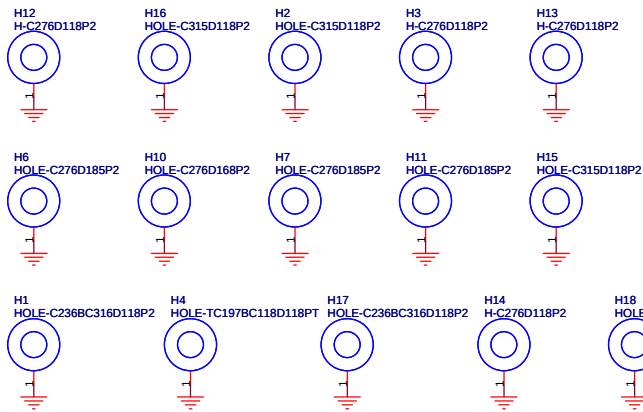
0.5A



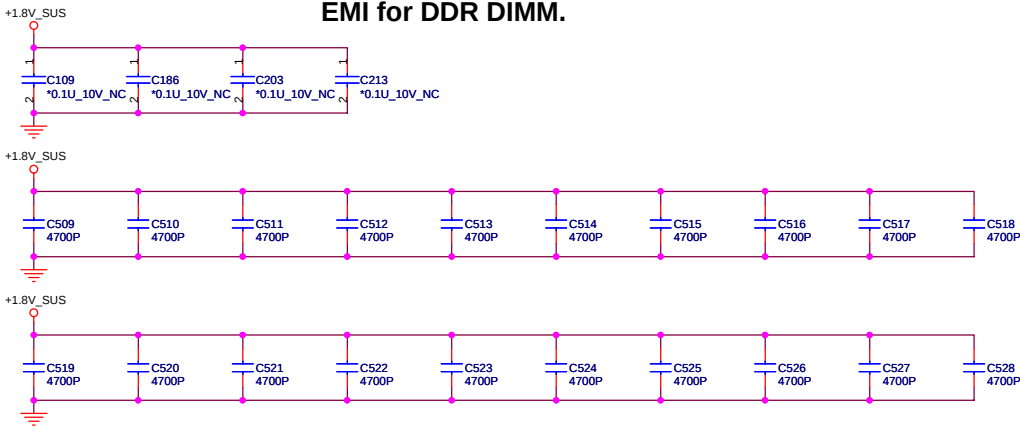
2.5V/ 1A



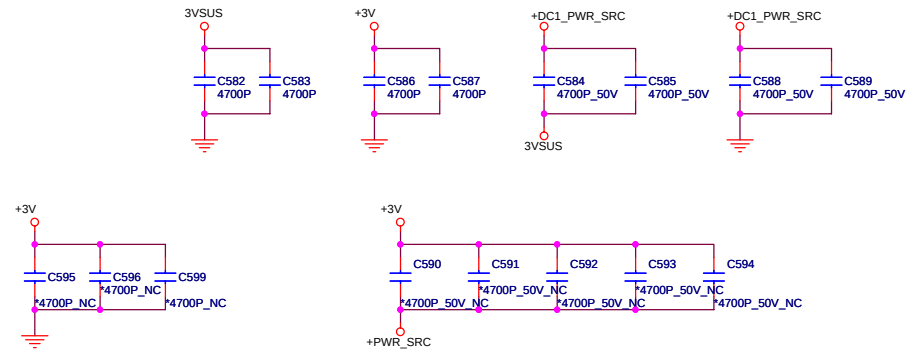
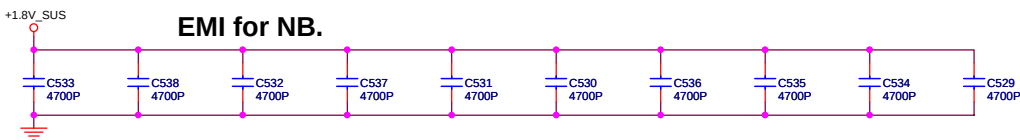




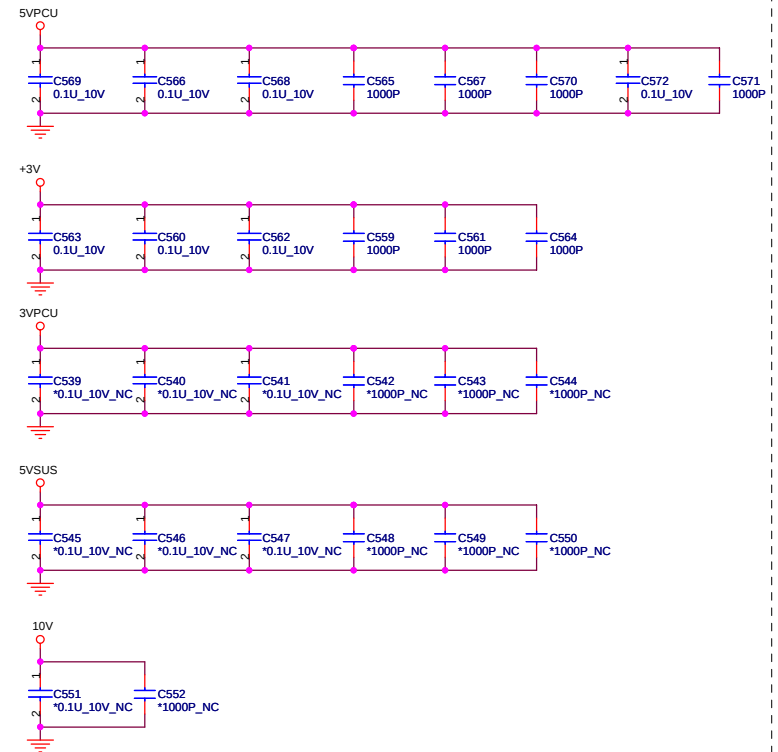
EMI for DDR DIMM.



EMI for NB.



For EMI



PROJECT : SW1
Quanta Computer Inc.

