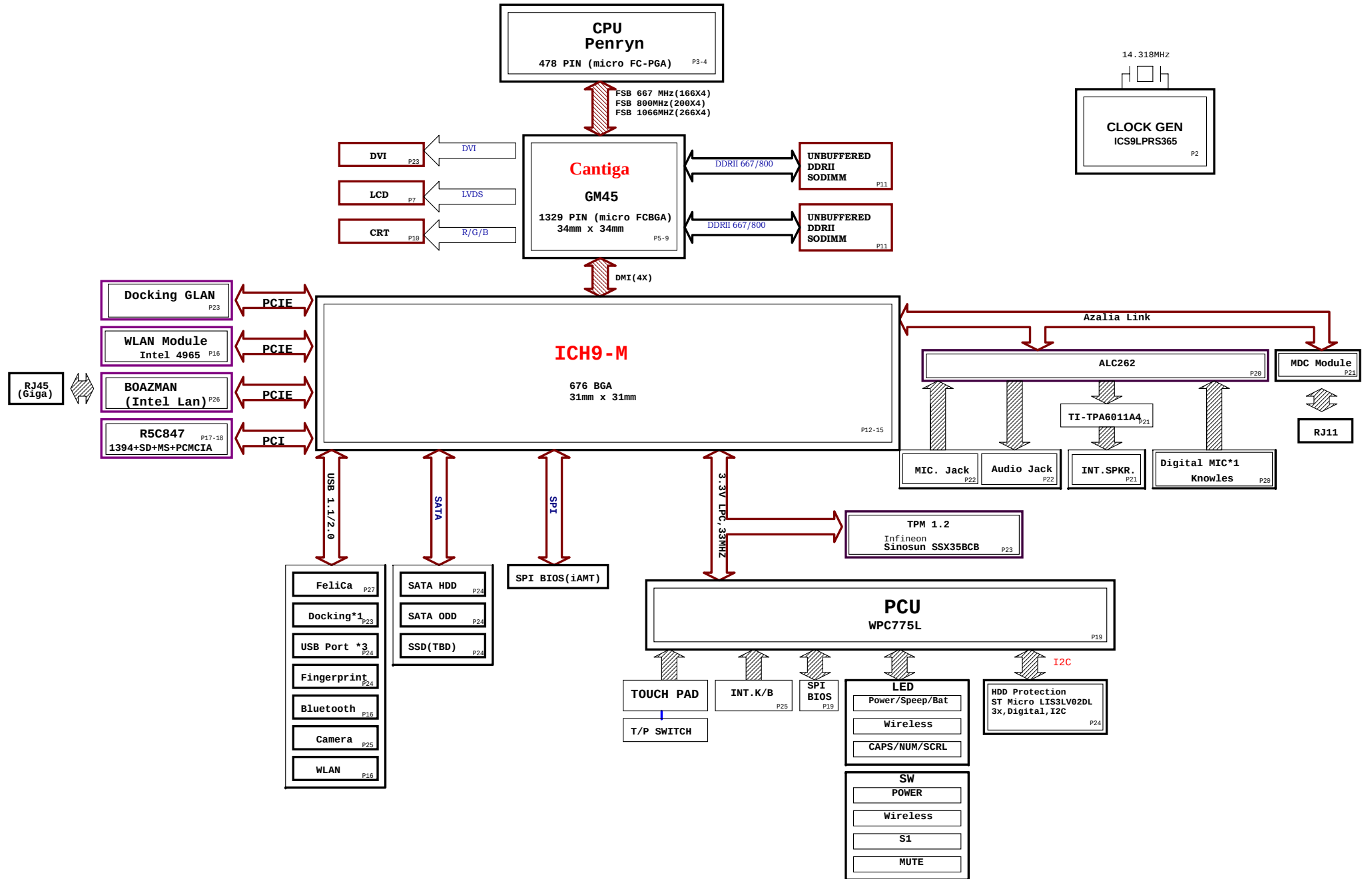
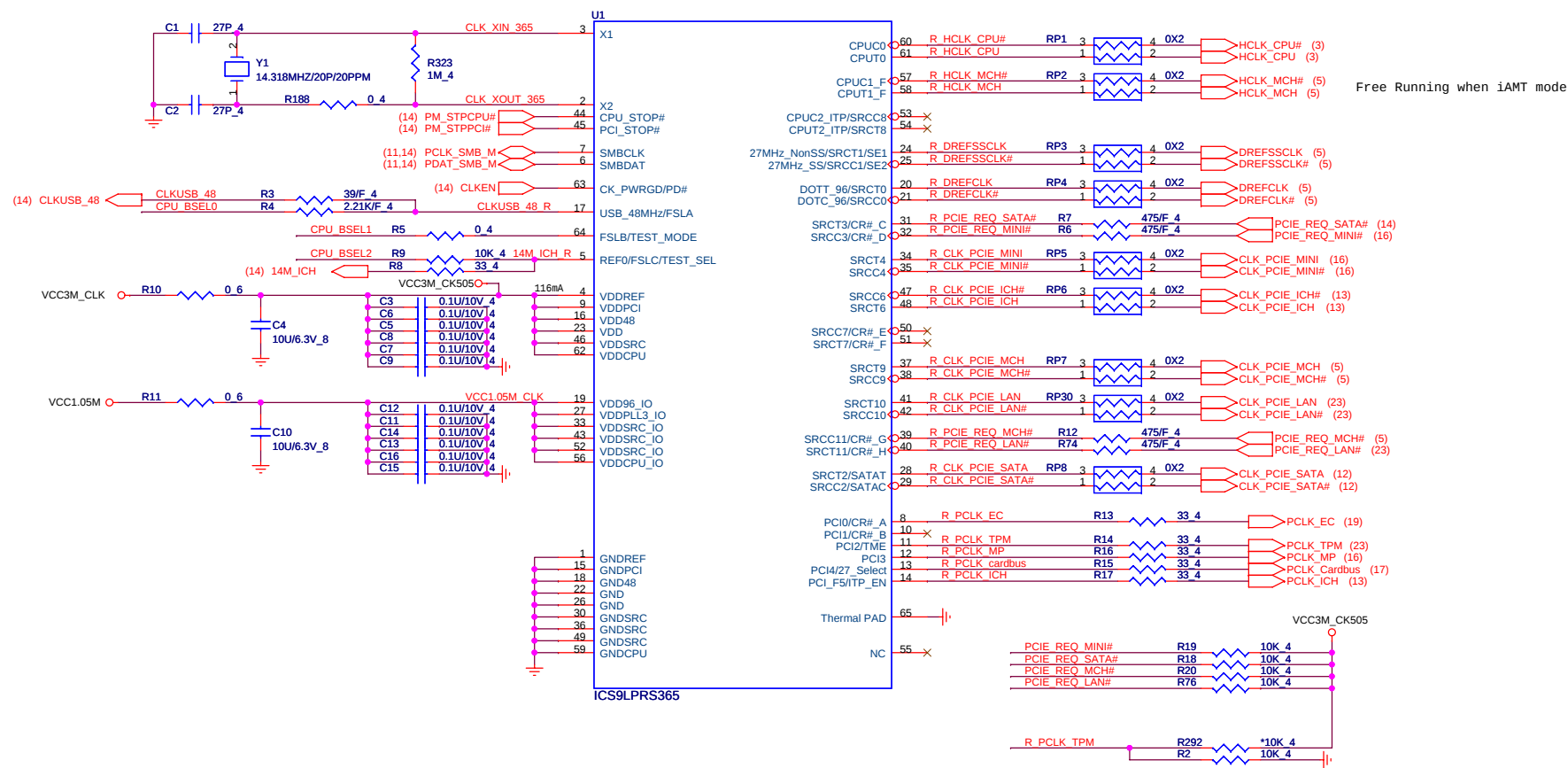


TW1 Block Diagram

1





FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB DOT	Spread %
* 0	0	0	266.66	100	33.33	14.318	48 96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48 96	0.5 Down
0	1	0	200.00	100	33.33	14.318	48 96	0.5 Down
0	1	1	166.66	100	33.33	14.318	48 96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48 96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48 96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48 96	0.5 Down
1	1	1	RESERVED					

27 Select PIN13	PIN 20/21	PIN 24/25
* 0	DOT_96 / DOT_96#	LCDCLK / LCDCLK#
1	SRC_0 / SRC_0#	27M / 27M_SS

ITP_EN(PIN14)	PIN53/54
* 0	SRC8/SRC8#
1	ITP/ITP#

Byte0 Bit4: iAMT Enable/Disable Control

QUANTA
COMPUTER

Title

CLOCK GENERATOR

Size

Document Number

TW1 Main Board

Date

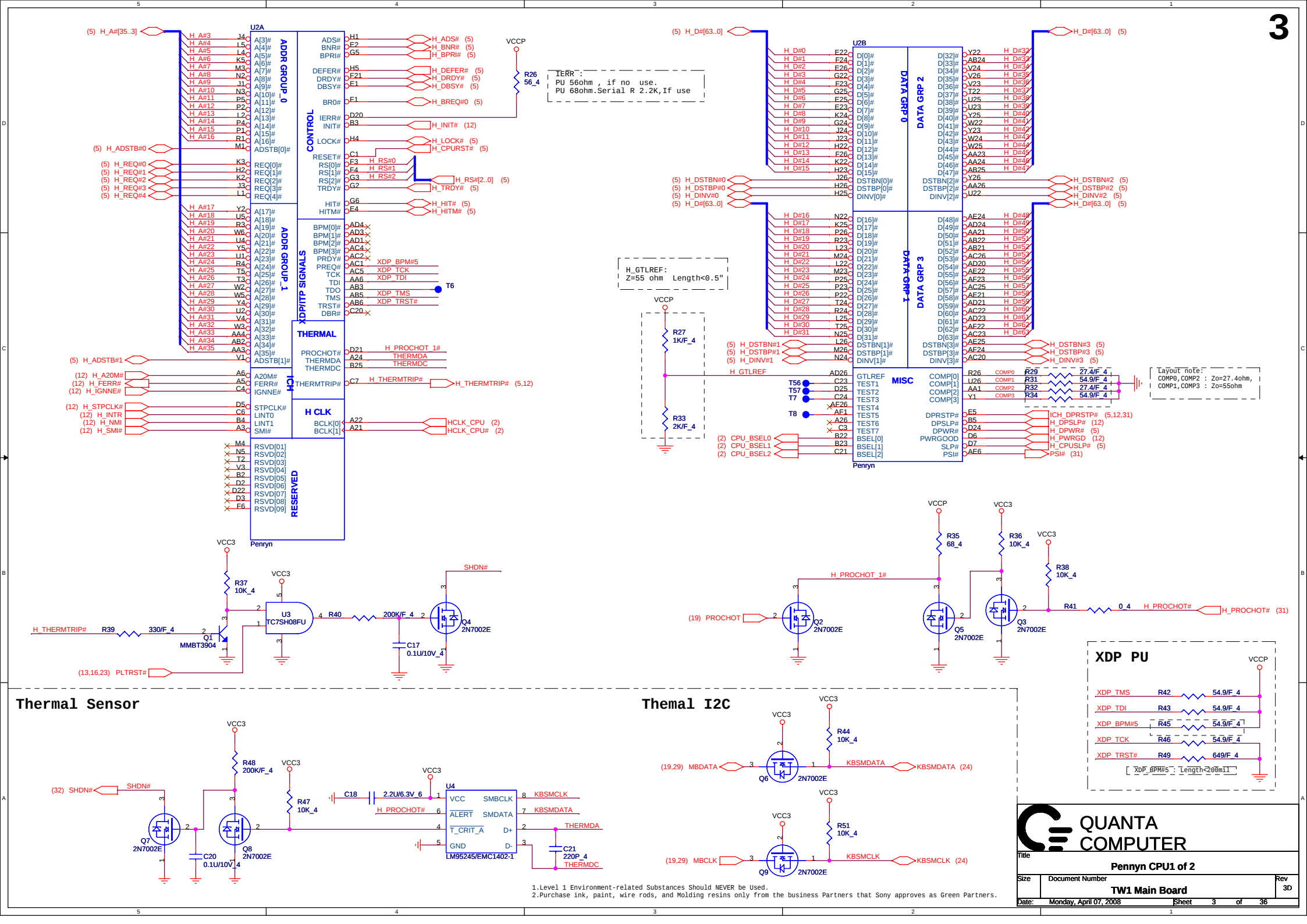
Monday, April 28, 2008

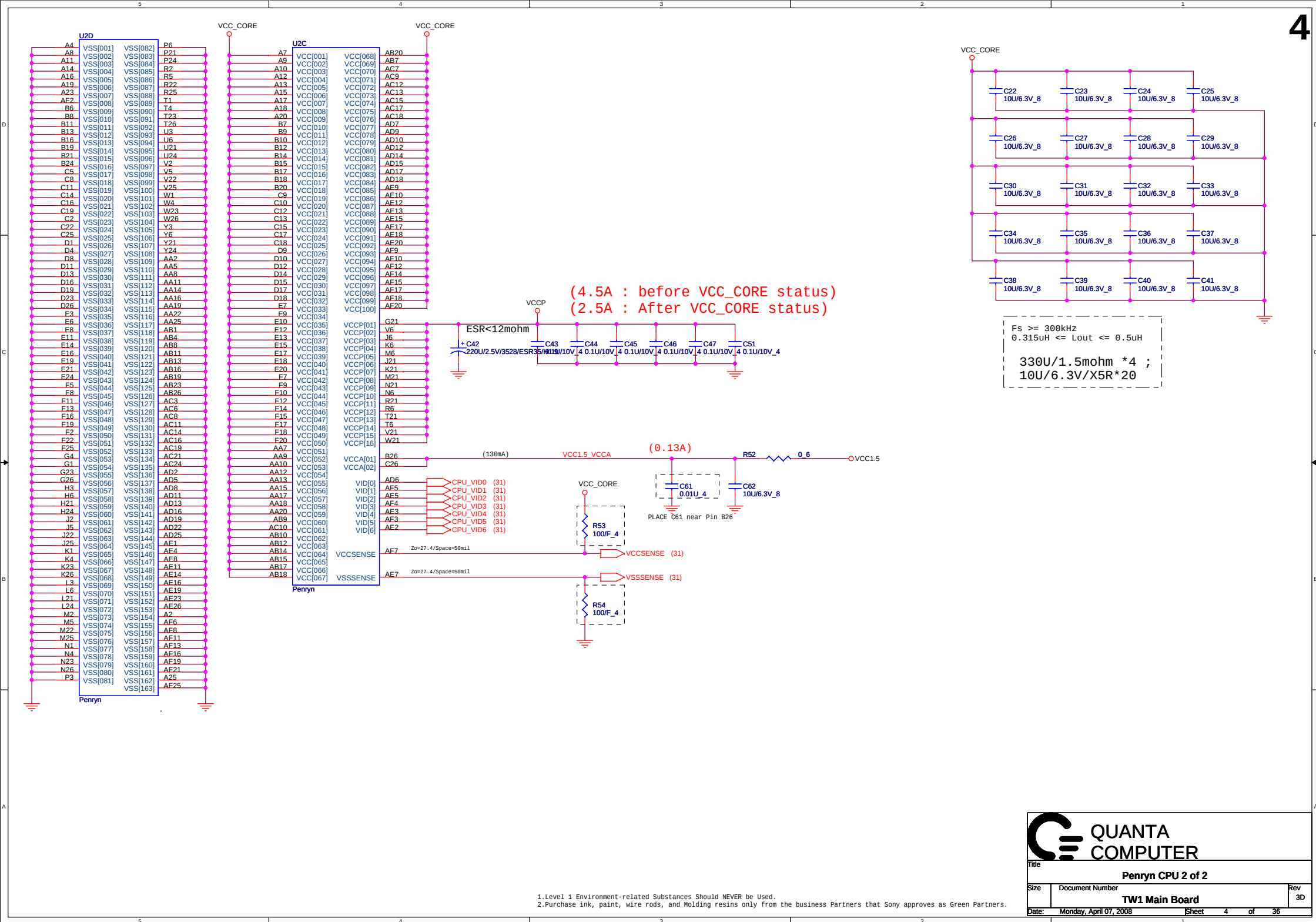
Sheet 2 of 36

Rev

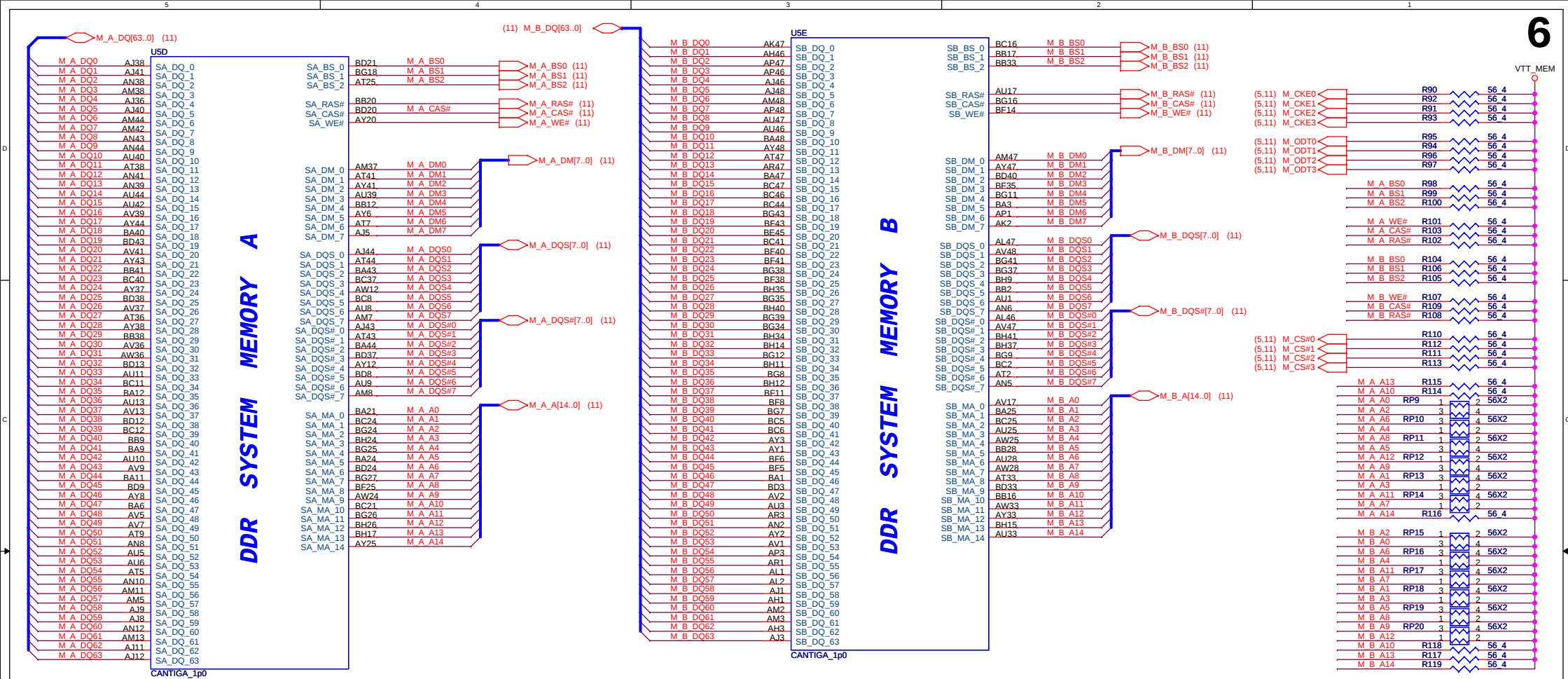
3E

1.Level 1 Environment-related Substances should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.





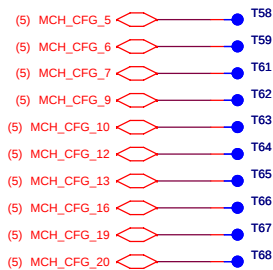




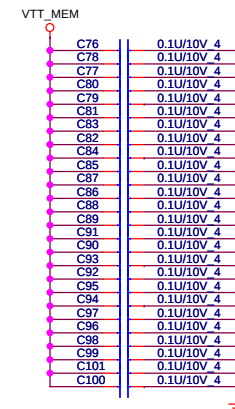
GMCH Strap pin description

	Low	High
C6F5	DMIX2	* DMIX4
C6F6	ITPM HOST interface enable	* ITPM HOST interface disable
C6F7	AMT Firewall will use TLS cipher suite with no confidentiality	* AMT Firewall will use TLS cipher suite with confidentiality
C6F9	PCIe Graphics lan : Reverse Lane	* PCIe Graphics lan : Normal operation
C6F10	PCIe Loopback enable	* PCIe Loopback disable
C6F16	FSB Dynamic ODT Disabled	* FSB Dynamic ODT Enabled
C6F19	* DMI LANE Normal	DMI LANE Reversed
C6F20	* only SDVO/DP/HDMI or PCIe is operational	SDVO/DP/HDMI and PCIe are operation simultaneously via the PEG port
C6F[12:13]	XOR /ALLZ / Clock Un-gating 00 = Reserve 01 = XOR mode enabled 10 = All-Z mode enabled * 11 = Normal Operation(Default)	

Int.Pull-down : CF6 18,19,20
Int.Pull-high : CF6 CF6 3-17

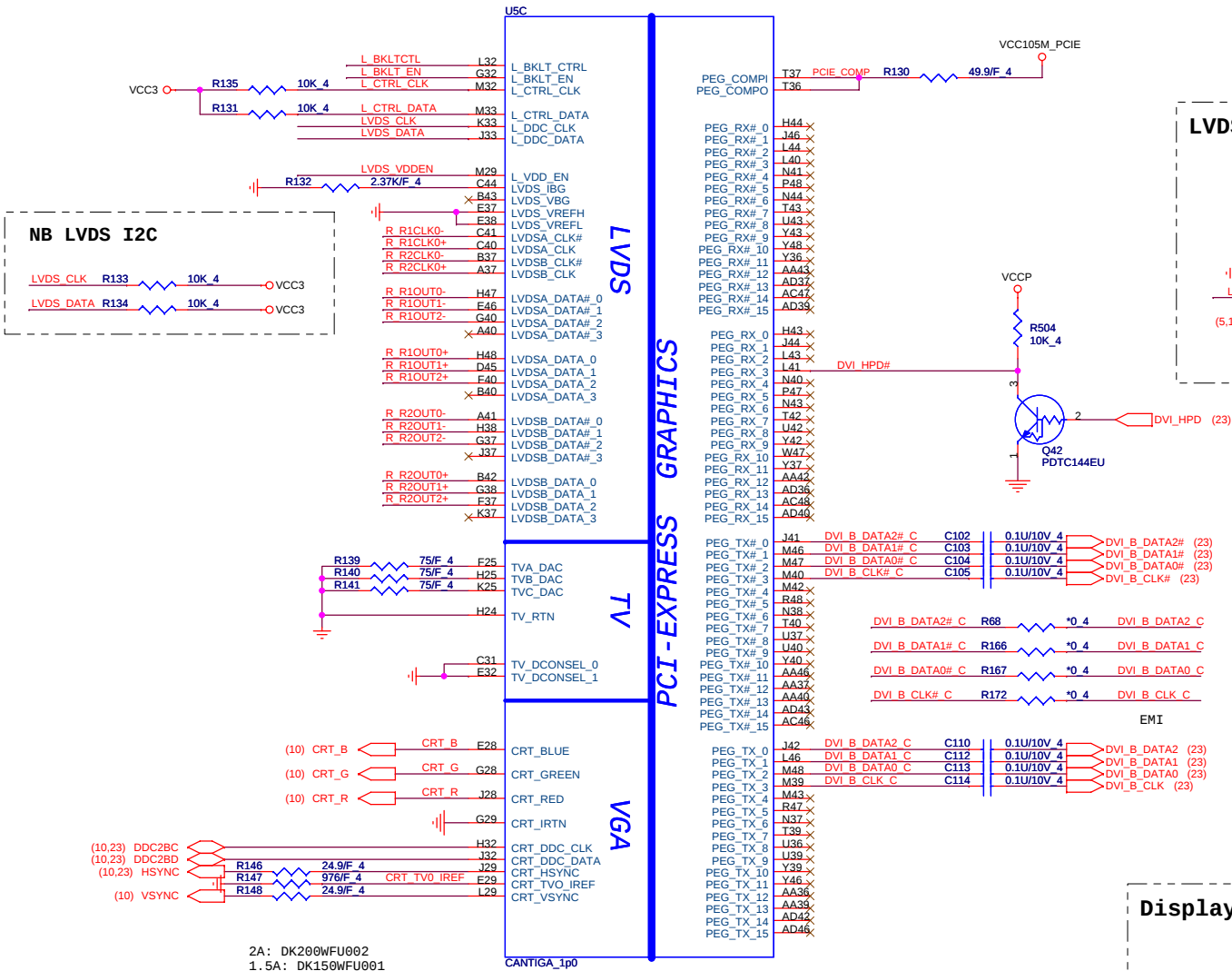


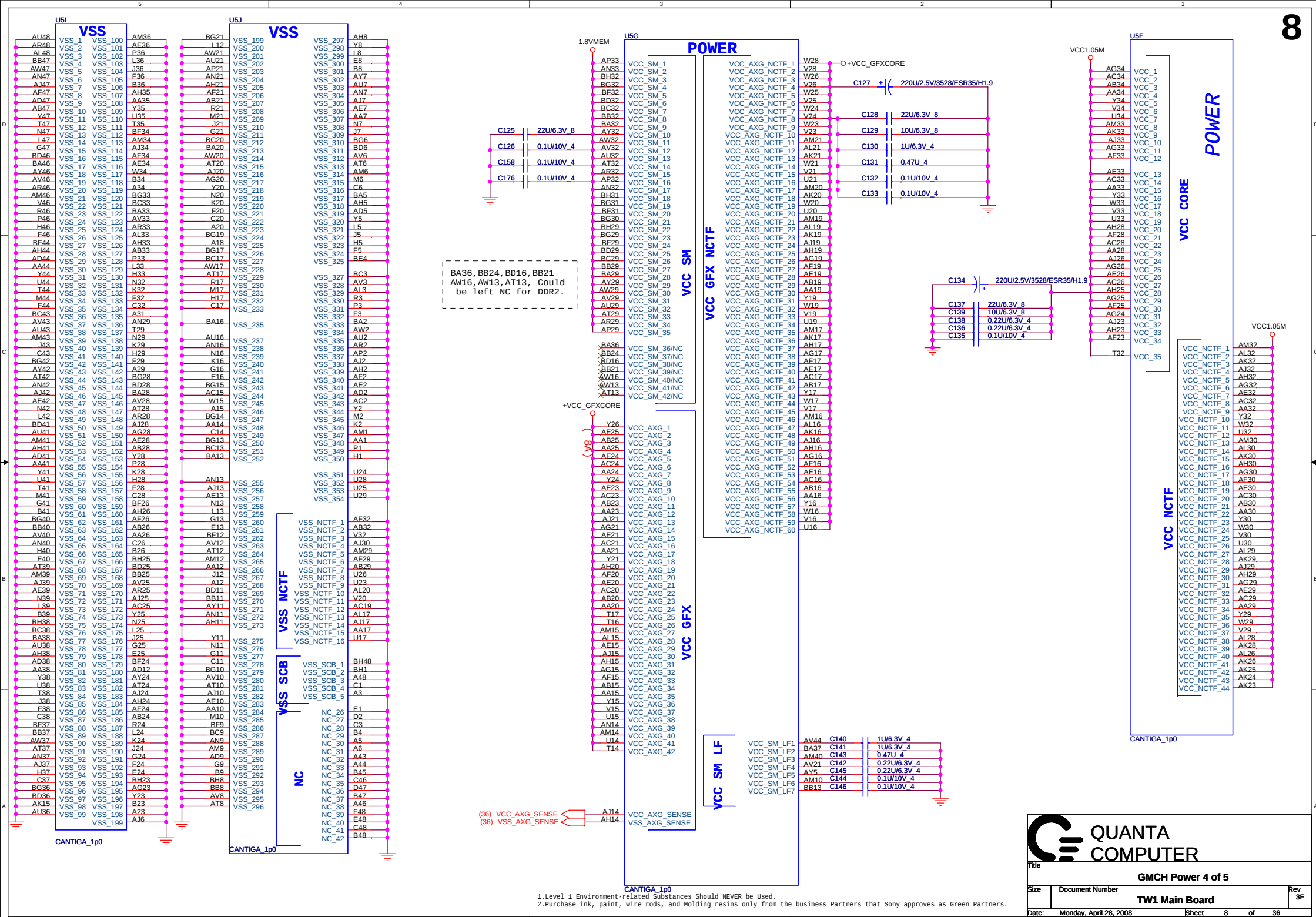
1.Level 1 Environment-related Substances should NEVER be Used.
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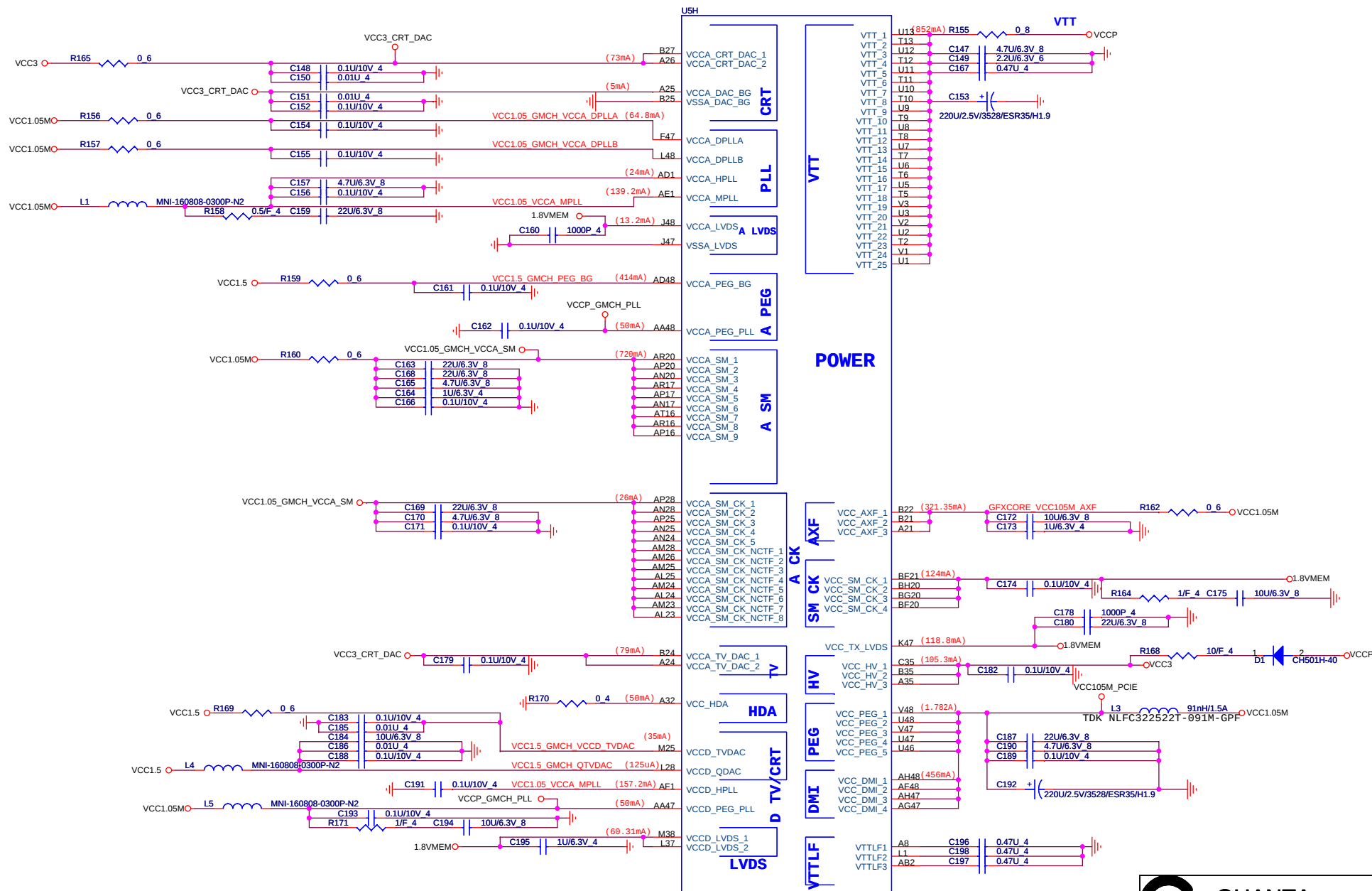


QUANTA
COMPUTER

Title			GMCH DDR II 2 of 5		
Size	Document Number				Rev
	TW1 Main Board				3E
Date	Monday, April 28, 2008				
	Sheet	6	of	36	

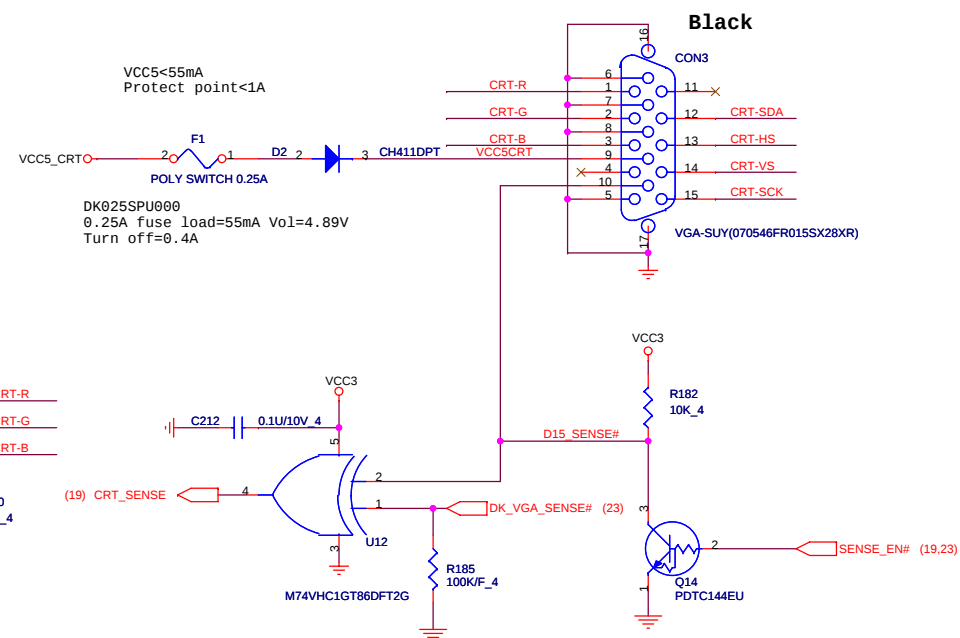
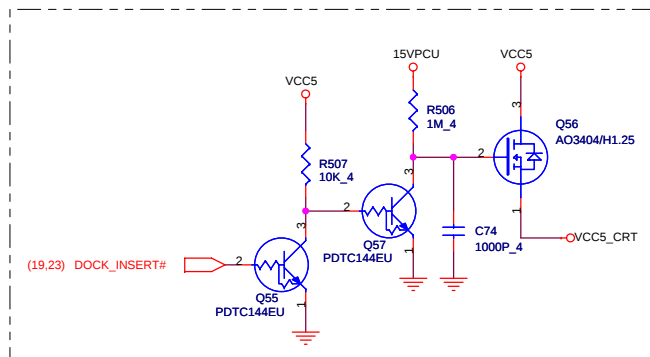
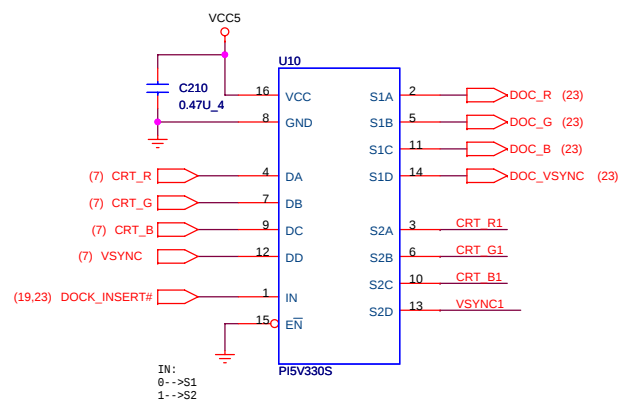
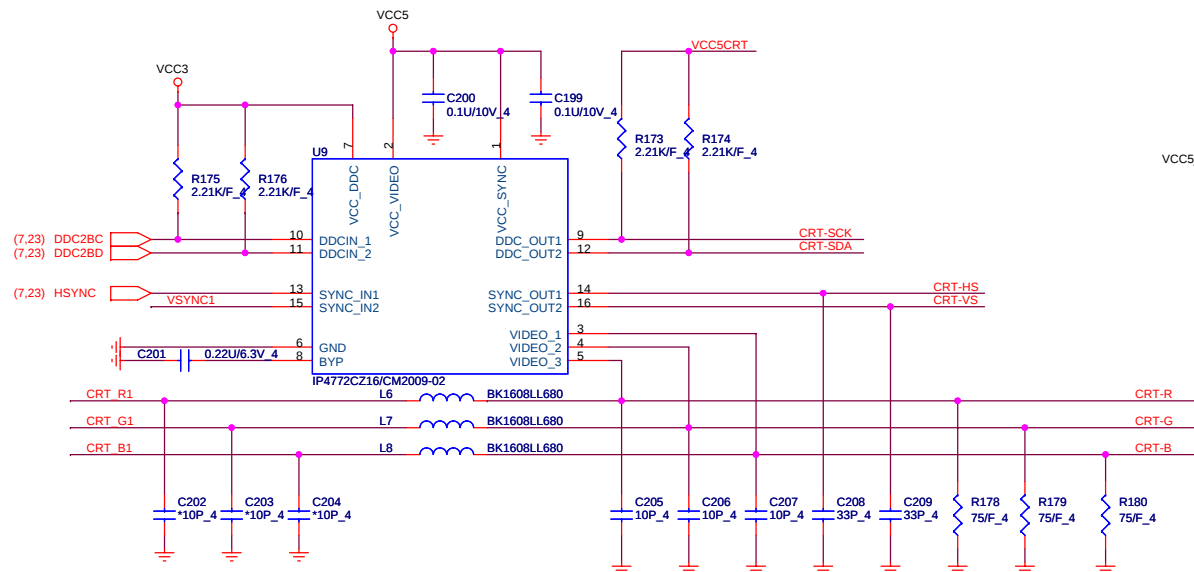






GMCH Power 5 of 5

Size	Document Number	Rev
	TW1 Main Board	3E
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	SENSE_EN#	DK_VGA_SENSE#	D15_SENSE#	Docking_Insert#	CRT_SENSE
Without Docking					
MB CRT no Plug	L	L	H	H	L
MB CRT Plug in	L	L	H => L	H	L => H
MB CRT plug out	L	L	L => H	H	H => L
With Docking					
All no Plug	L	L	H	L	L
MB CRT Plug in	L	L	H => L	L	L => H
MB CRT plug out	L	L	L => H	L	H => L
DOCK DVI Plug in	L	H => L	H	L	H => L
DOCK DVI Plug out	L	L => H	H	L	L => H
DOCK CRT Plug	L	H => L	H	L	H => L
DOCK CRT/DVI Plug	L	L => H	H	L	L => H

[EC Behavior]
 CRT_SENSE: H=>L or L=>H detect which one is inserting
 Docking_Insert#: H=>L detect which one is inserting
 [CRT SW]
 When Docking_Insert# is low switching RGB to Docking CRT
 [SENSE_EN#]
 Input for CRT pin10, EC assert to high when CRT insert[NEO Request]

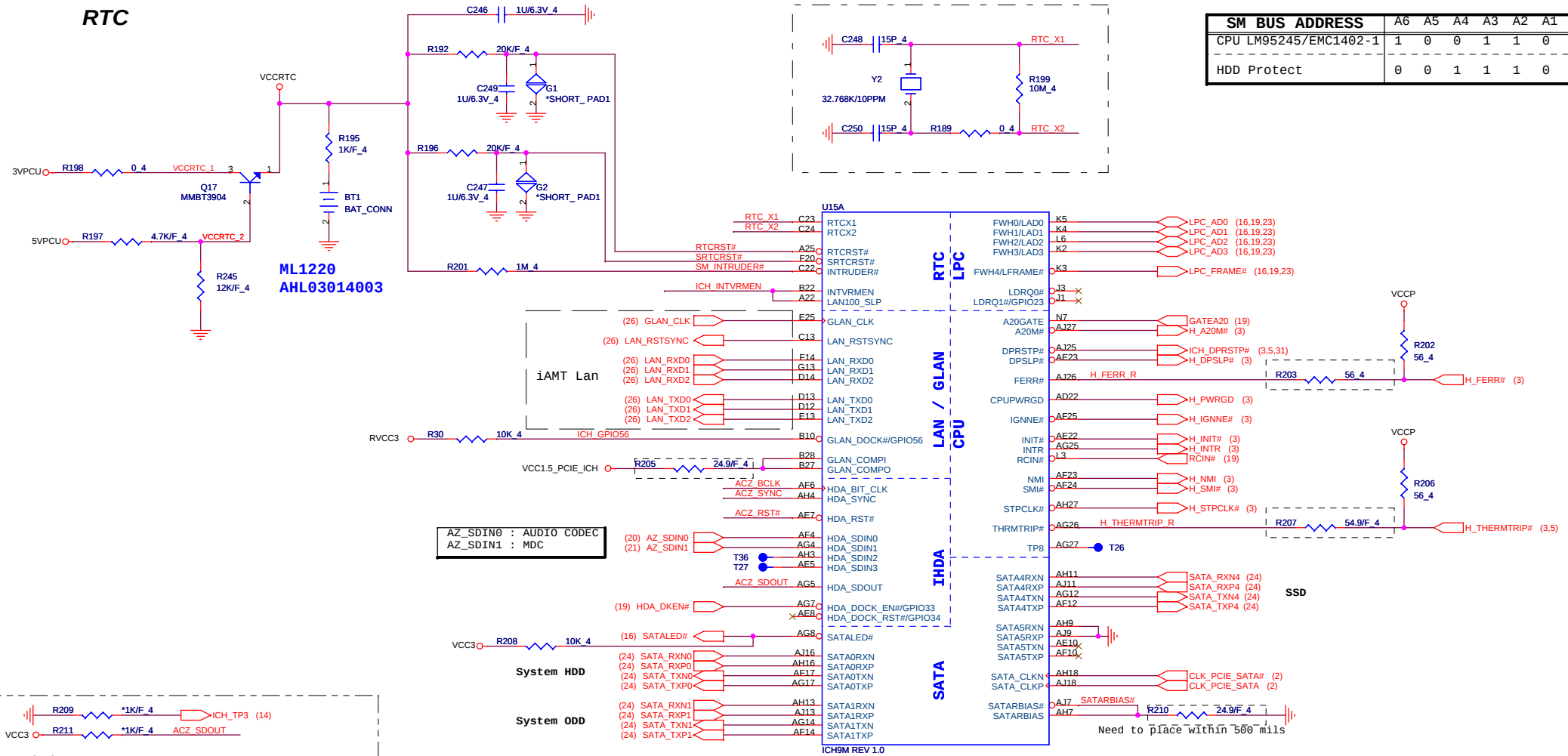


Title			CRT
Size	Document Number	Rev	
		3E	
TW1 Main Board			
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G2 Short-PAD:
Short : Clear ME RTC registers
Open : Keep ME RTC registers

RTC



QUANTA COMPUTER

Title: ICH9-M HOST1 of 4

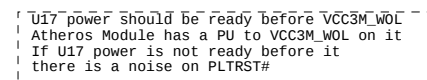
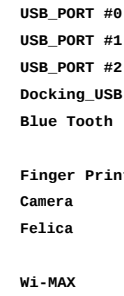
Size: Document Number: TW1 Main Board

Date: Monday, April 28, 2008

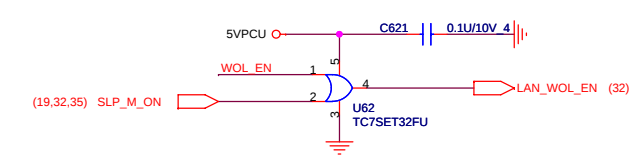
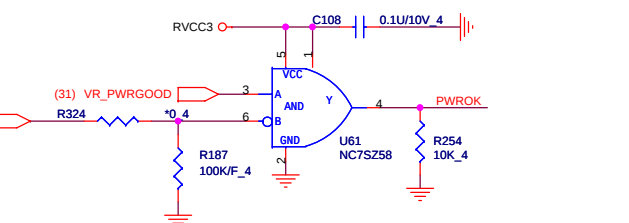
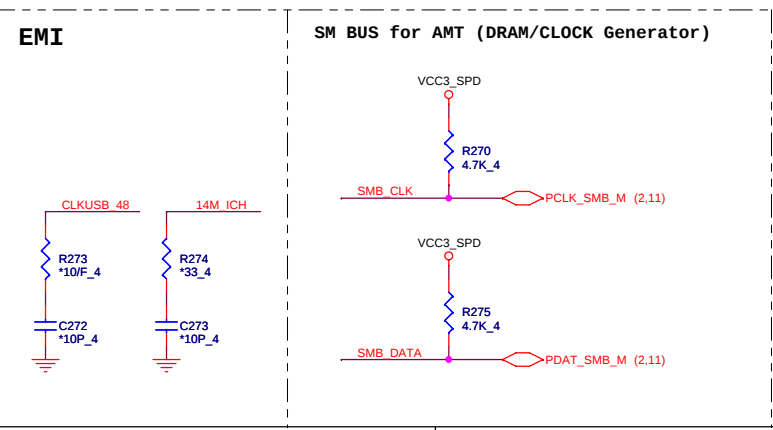
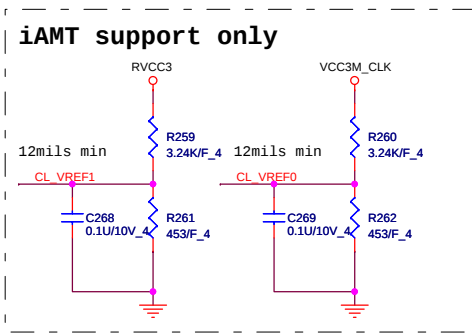
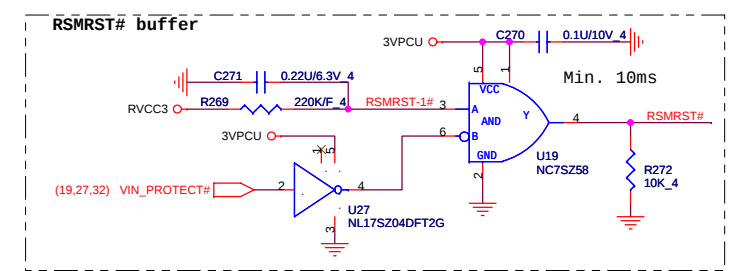
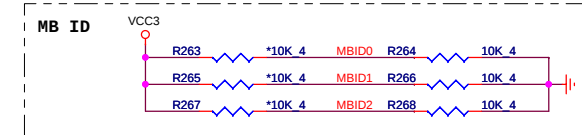
Sheet 12 of 36

Rev 3E

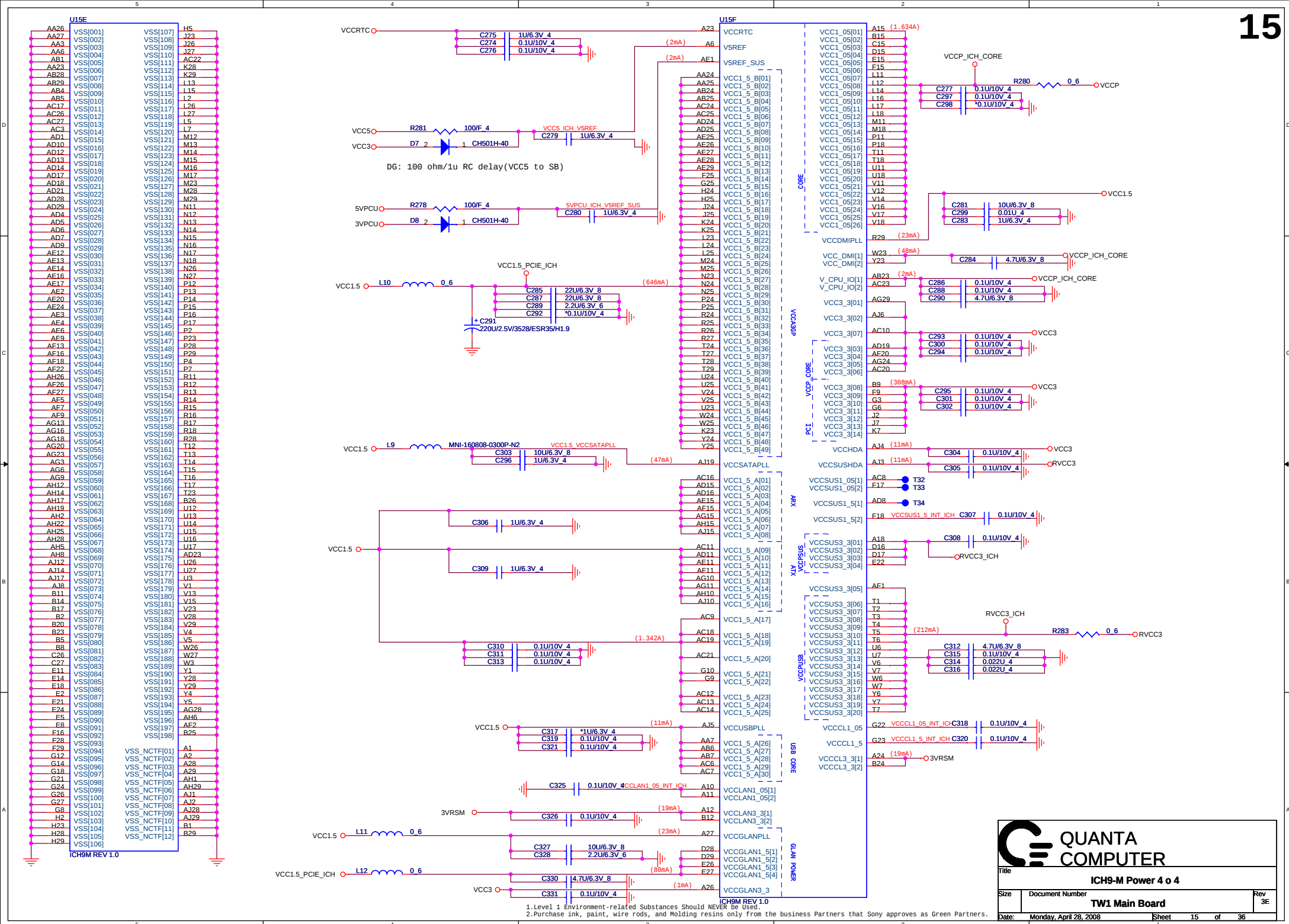
1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase Ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



 QUANTA COMPUTER			
Title			
ICH9-M PCIE 2 of 4			
Size	Document Number		Rev
	TW1 Main Board		3E
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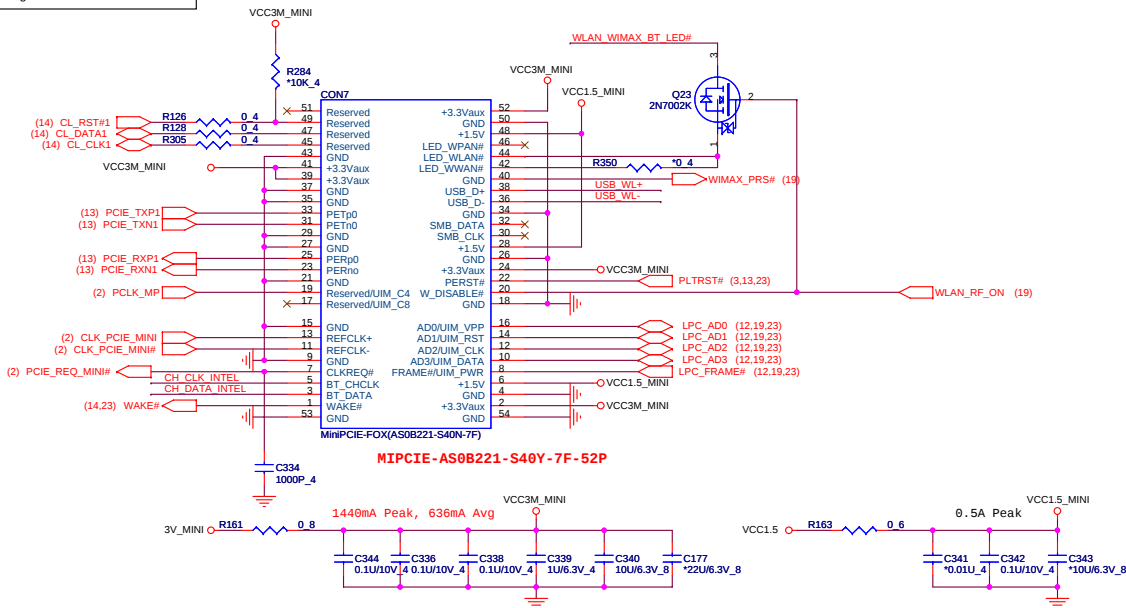


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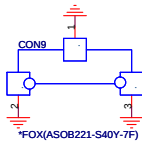
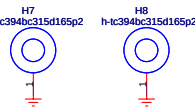


Mini PCI-E Card FOR WL

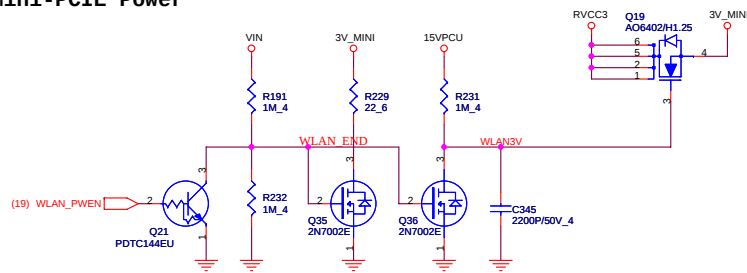
```
WLAN_RF_ON:
Low : disable the radio.
High : Enable the radio.
```



Screw For Half-MiniCard



Mini-PCIE Power



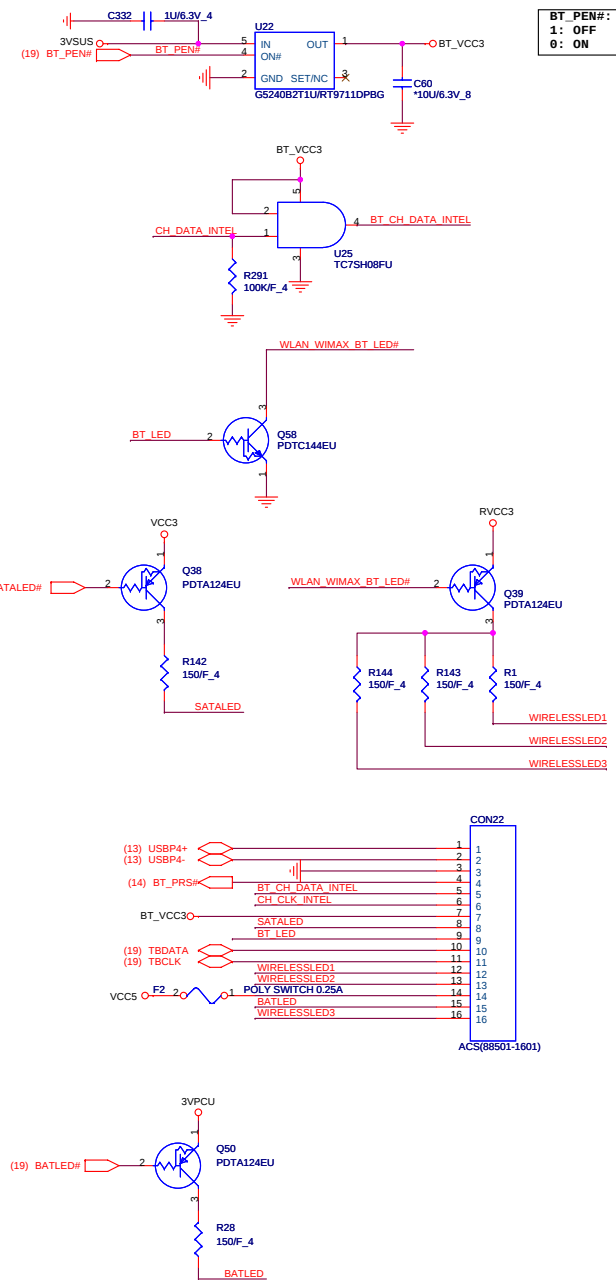
WLAN Power Control Table

WLAN_PWEN: 1:High
0:Low

DC mode				AC mode			
	Atheros WLAN moudle(HB63)	Intel Shirley_Peak	Intel Echo_Peak		Atheros WLAN moudle(HB63)	Intel Shirley_Peak	Intel Echo_Peak
S0	1	1	1	S0/M0	1	1	1
S3	0	1	1	S3	M1 0	1	1
S4	0	0	0		Moff 0	1	1
S5	0	0	0	S4/S5	M1 0	1	1
					Moff 0	0	0

TP & BT

16

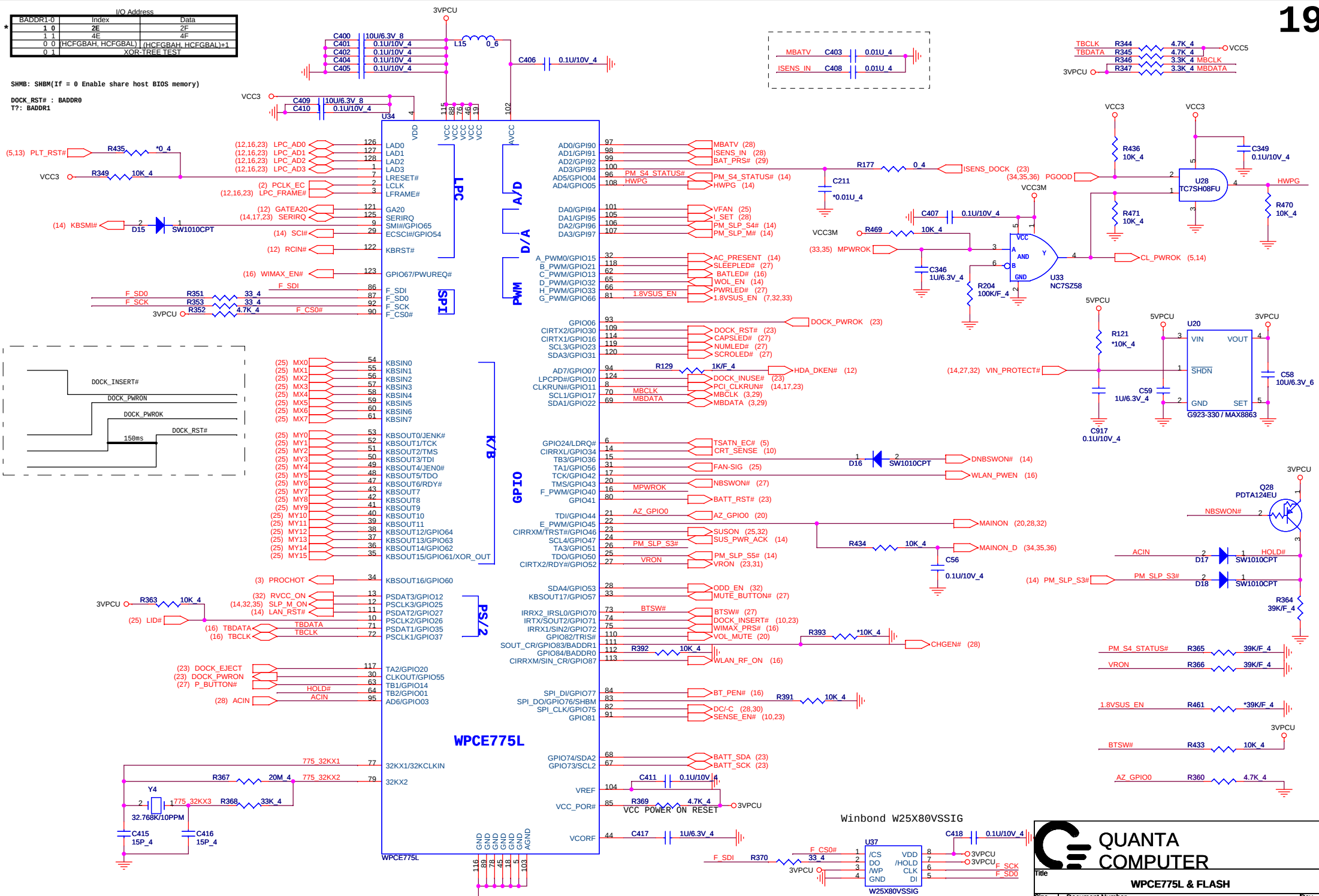


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I/O Address		
BADDR1-0	Index	Data
1 0	2E	2F
1 1	4E	4F
0 0	(HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1	
0 1	XOR-TREE TEST	

SHMB: SHBM(If = 0 Enable share host BIOS memory)

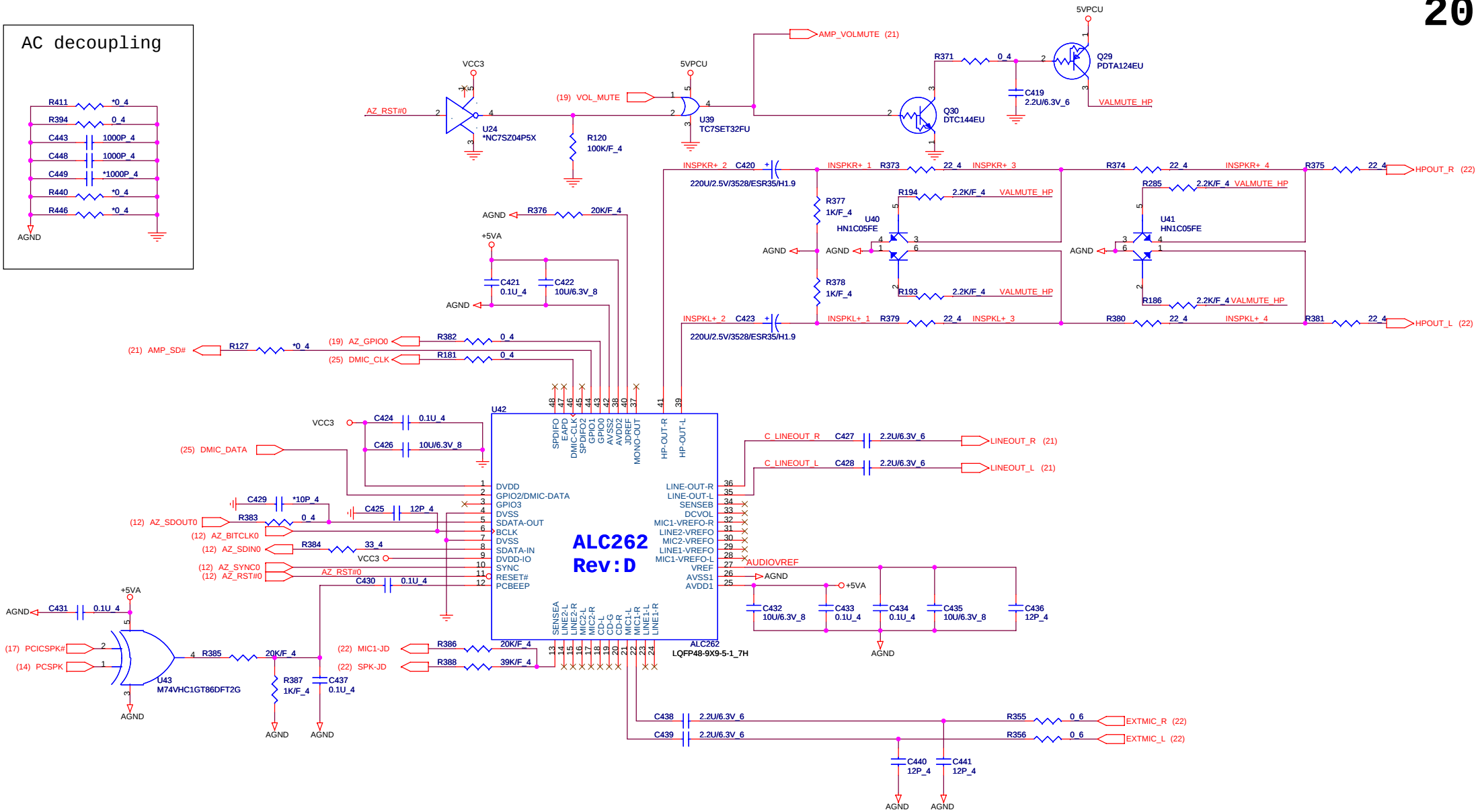
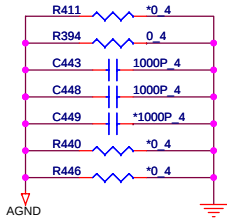
DOCK_RST# : BADDR6
T?: BADDR1



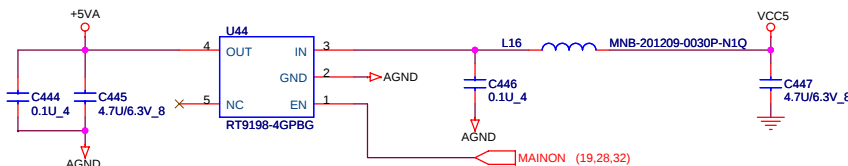
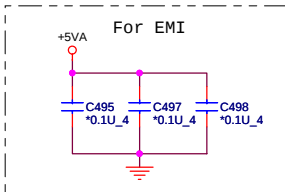
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2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

	QUANTA COMPUTER
Title WPCE775L & FLASH	
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Date: Monday, April 28, 2008	Sheet 19 of 36
Rev 3E	

AC decoupling



ALC262
Rev : D

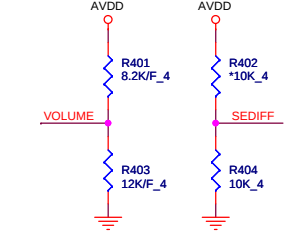
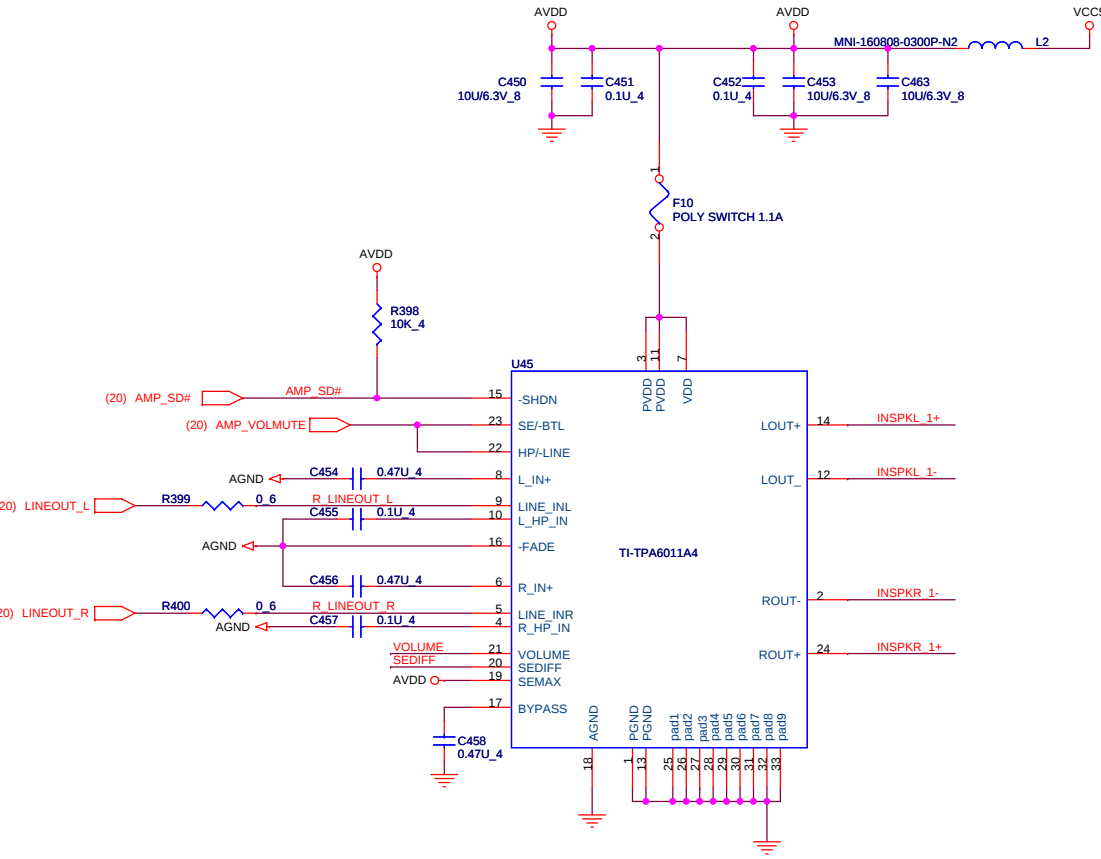


1.Level 1 Environment-related Substances Should NEVER be Used.
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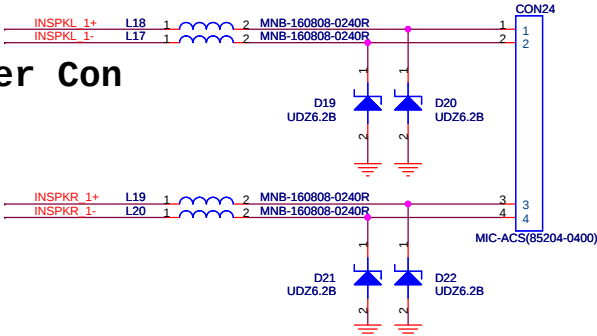
QUANTA
COMPUTER

Title Audio ALC262		
Size	Document Number TW1 Main Board	Rev 3E
Date:	Monday, April 28, 2008	
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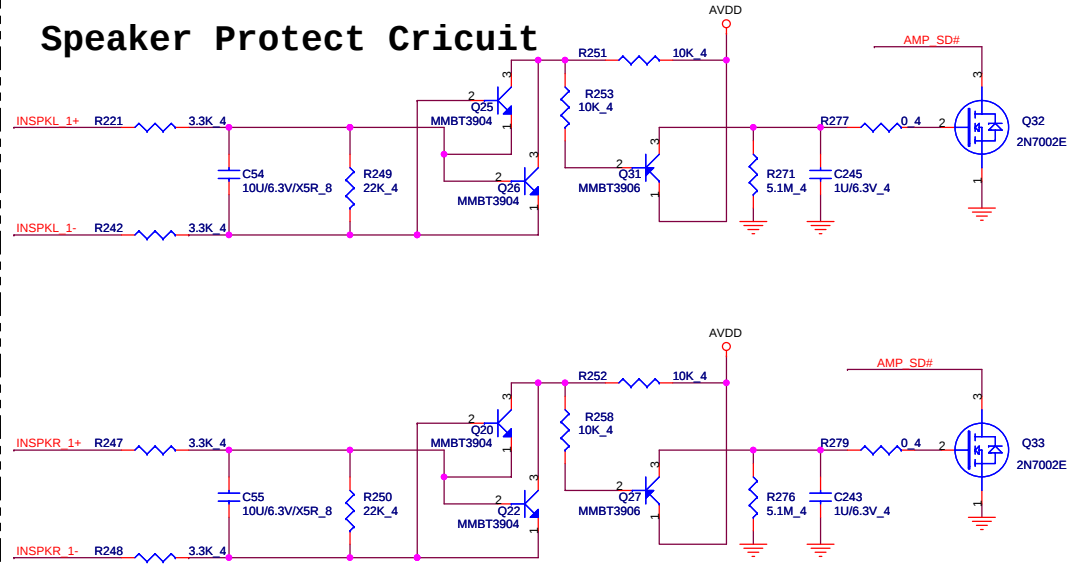
Audio amplifier



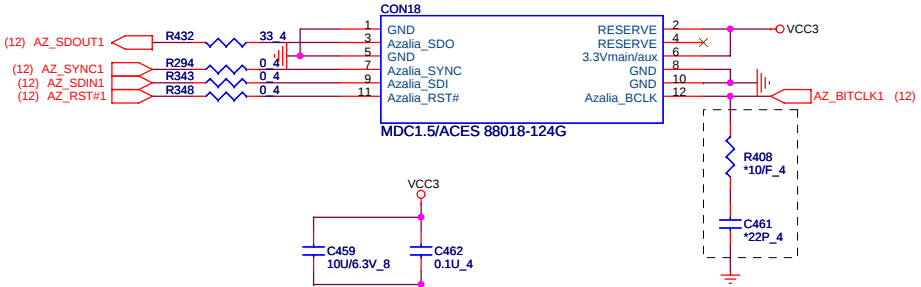
Speaker Con



Speaker Protect Cricuit



MDC V1.5





QUANTA
COMPUTER

Title		
Audio AMP & Int. Speaker		
Size	Document Number	Rev
	TW1 Main Board	3E
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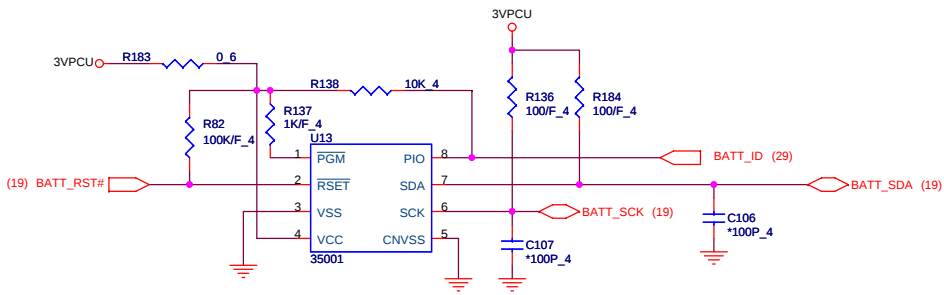
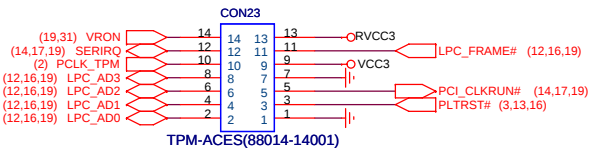
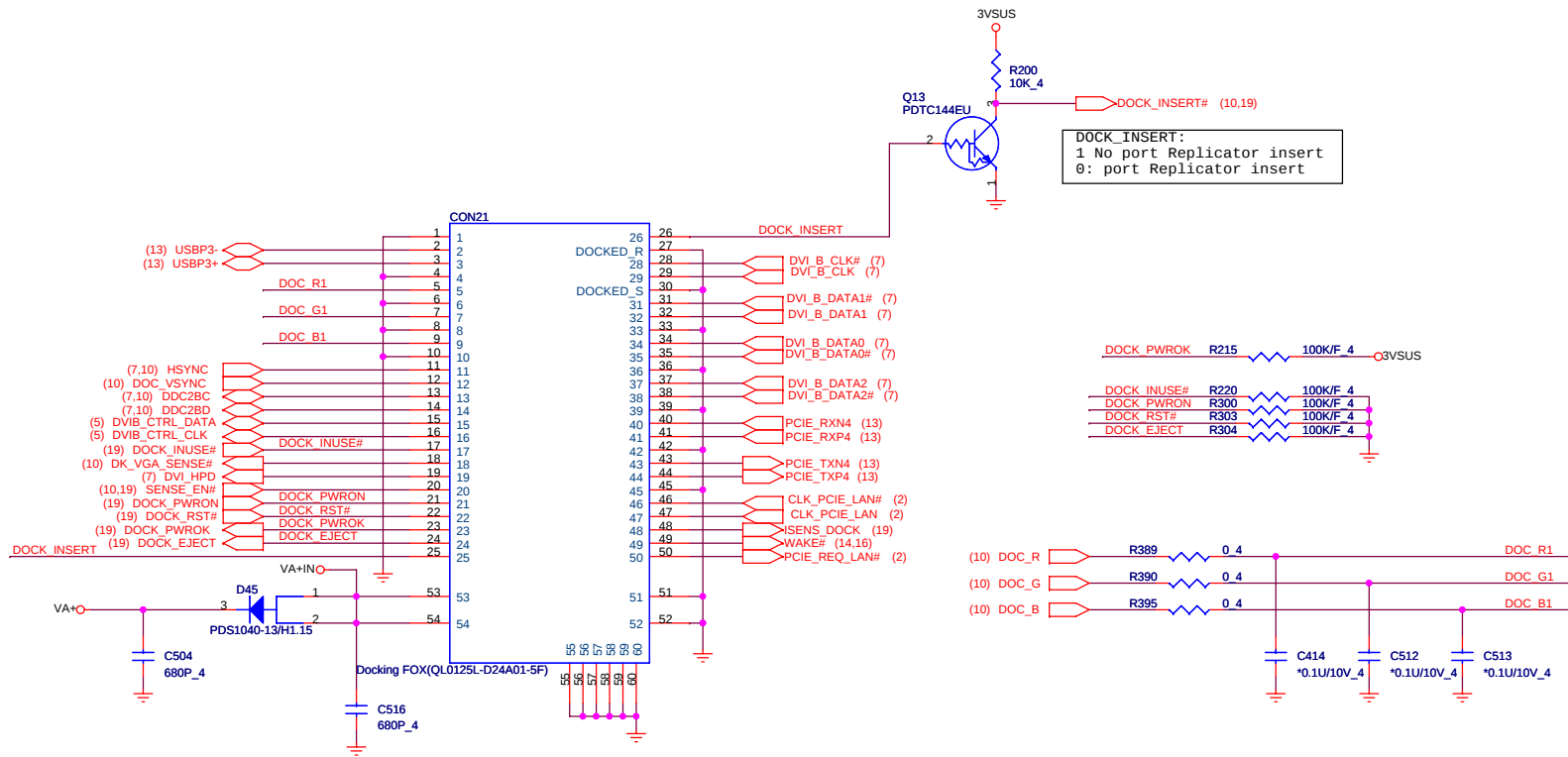
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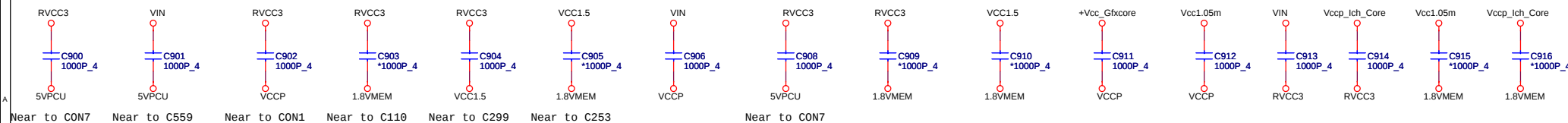
Size	Document Number
	TW1 Main Board

Date: Monday, April 28, 2008 Sheet 22 of 36

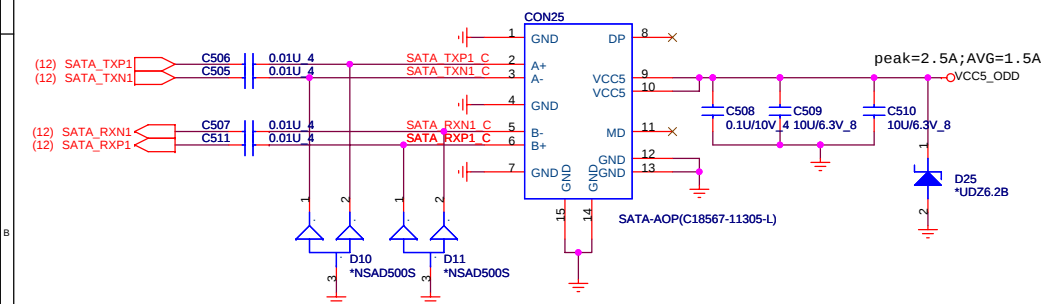
- 1.Level 1 Environment-related Substances should NEVER be Used.
- 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



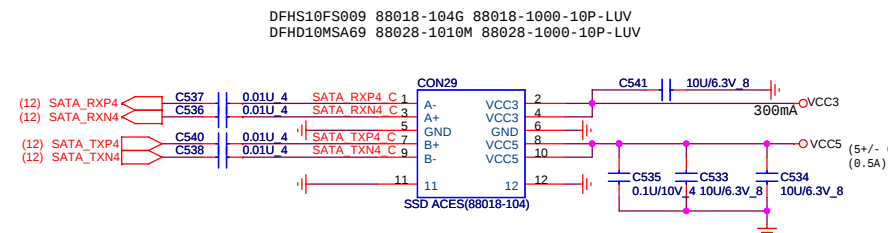
Decoupling Cap



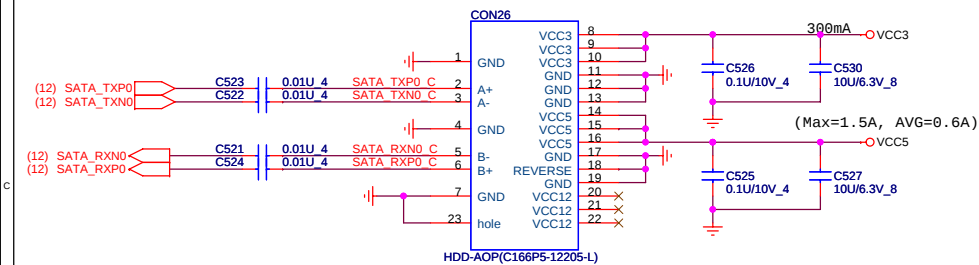
ODD CONNECTOR



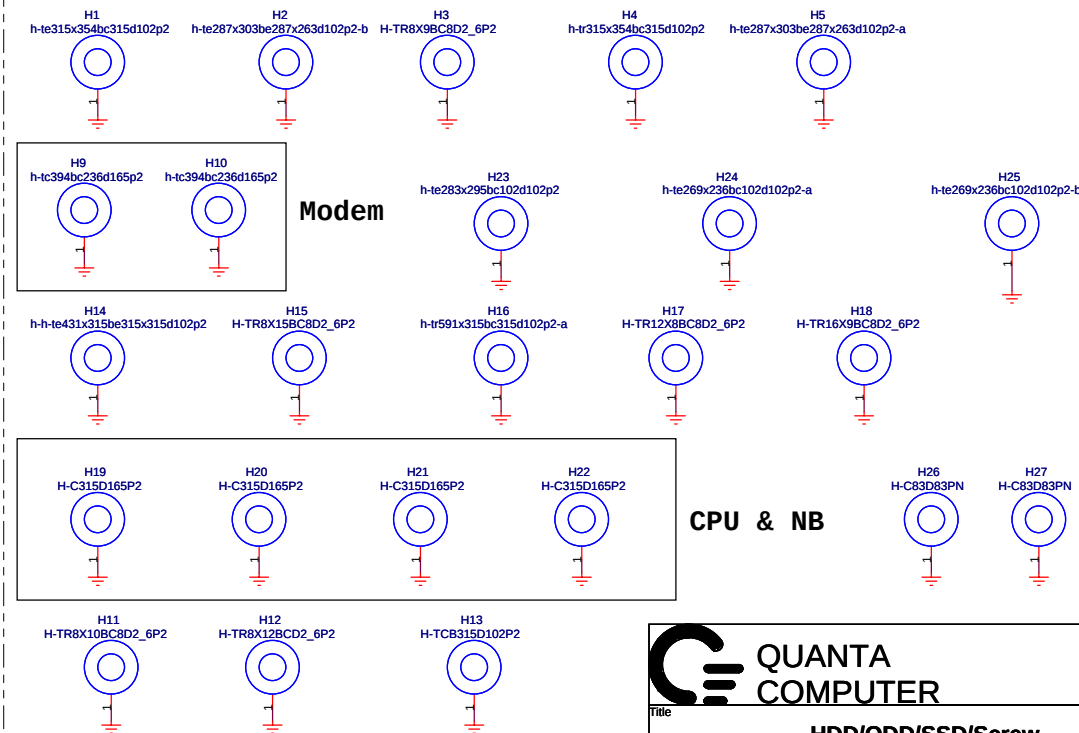
SSD



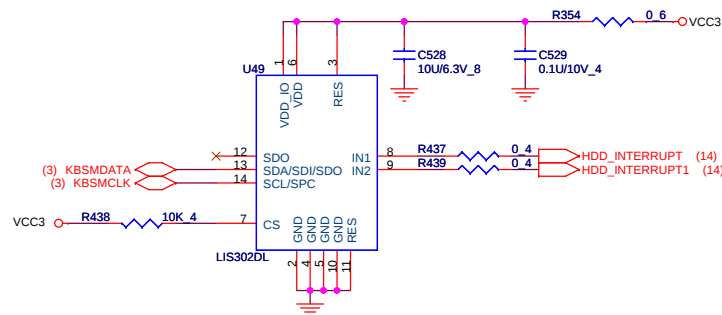
HDD CONNECTOR



Screw



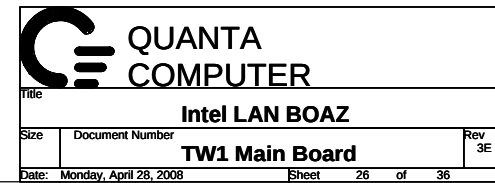
HDD PROTECT



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QUANTA COMPUTER

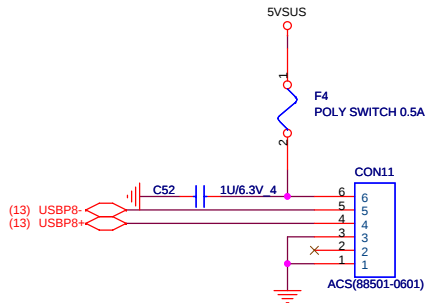
Title		
HDD/ODD/SSD/Screw		
Size	Document Number	Rev
	TW1 Main Board	3E
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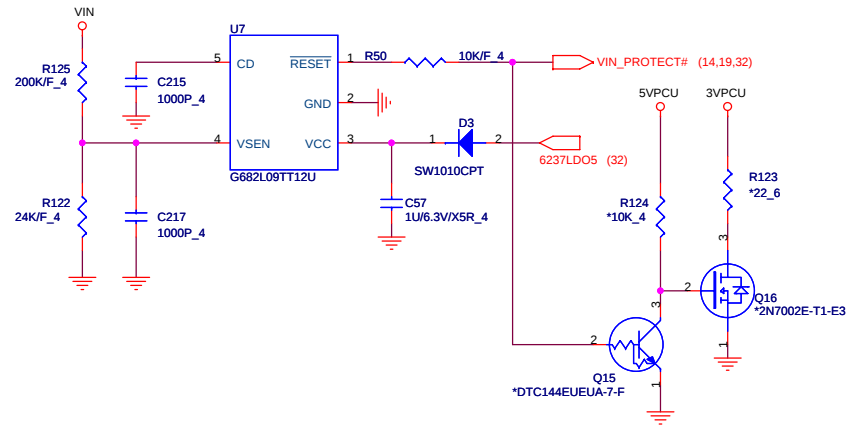
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Felica

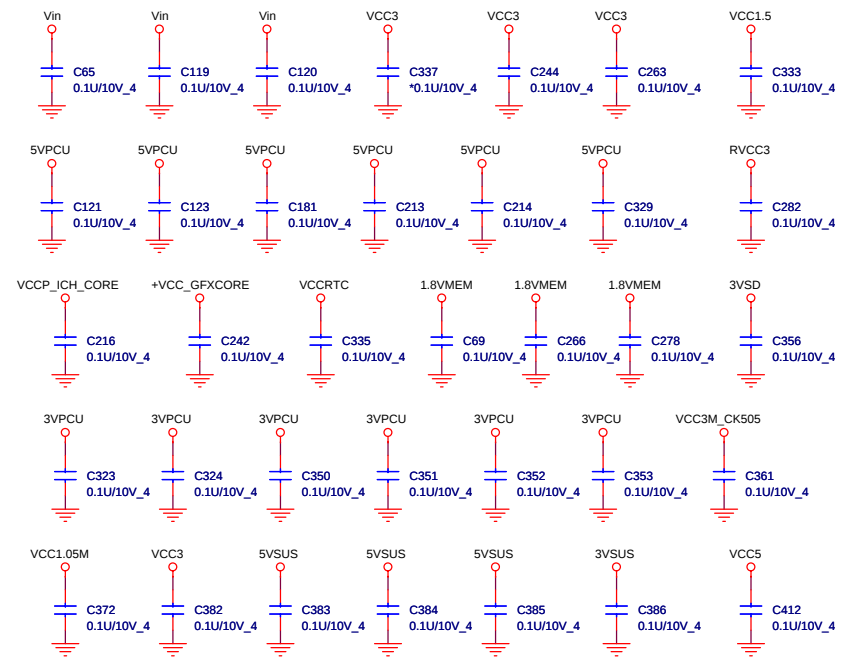
DK050TPU011
0.5A fuse load=0.3A Vol=4.92V
Turn off=1.1A



Reset Cricuit



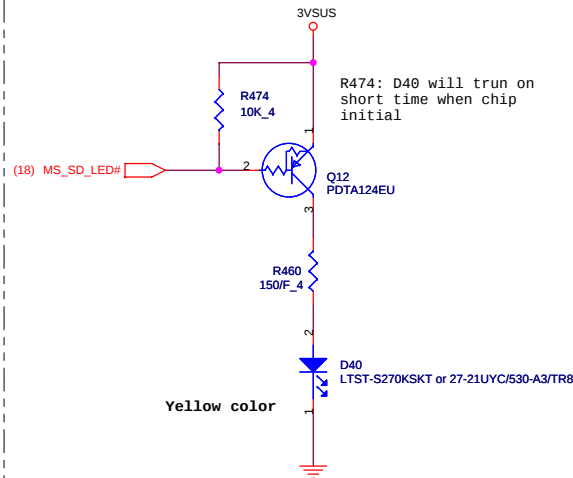
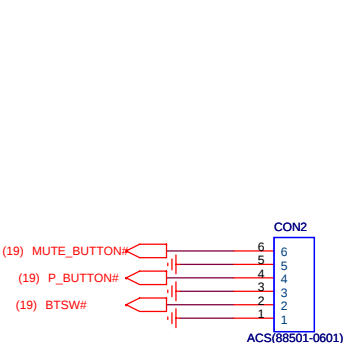
EMI Caps



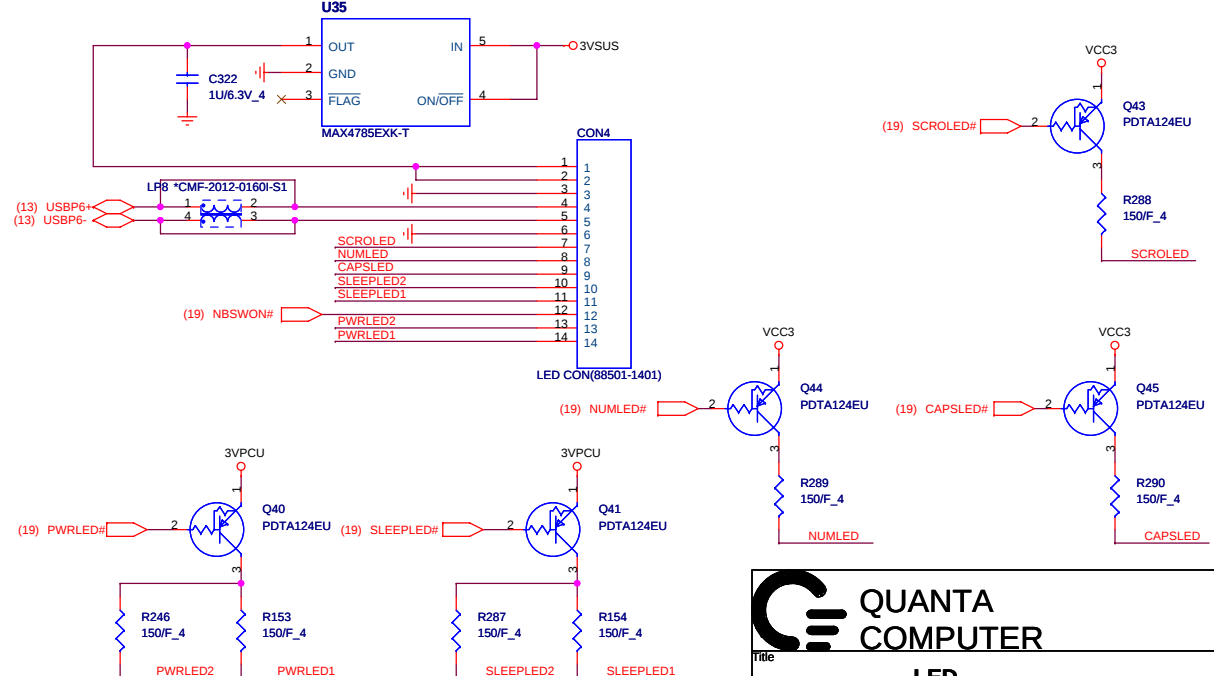
27

Buttom BOARD

LED



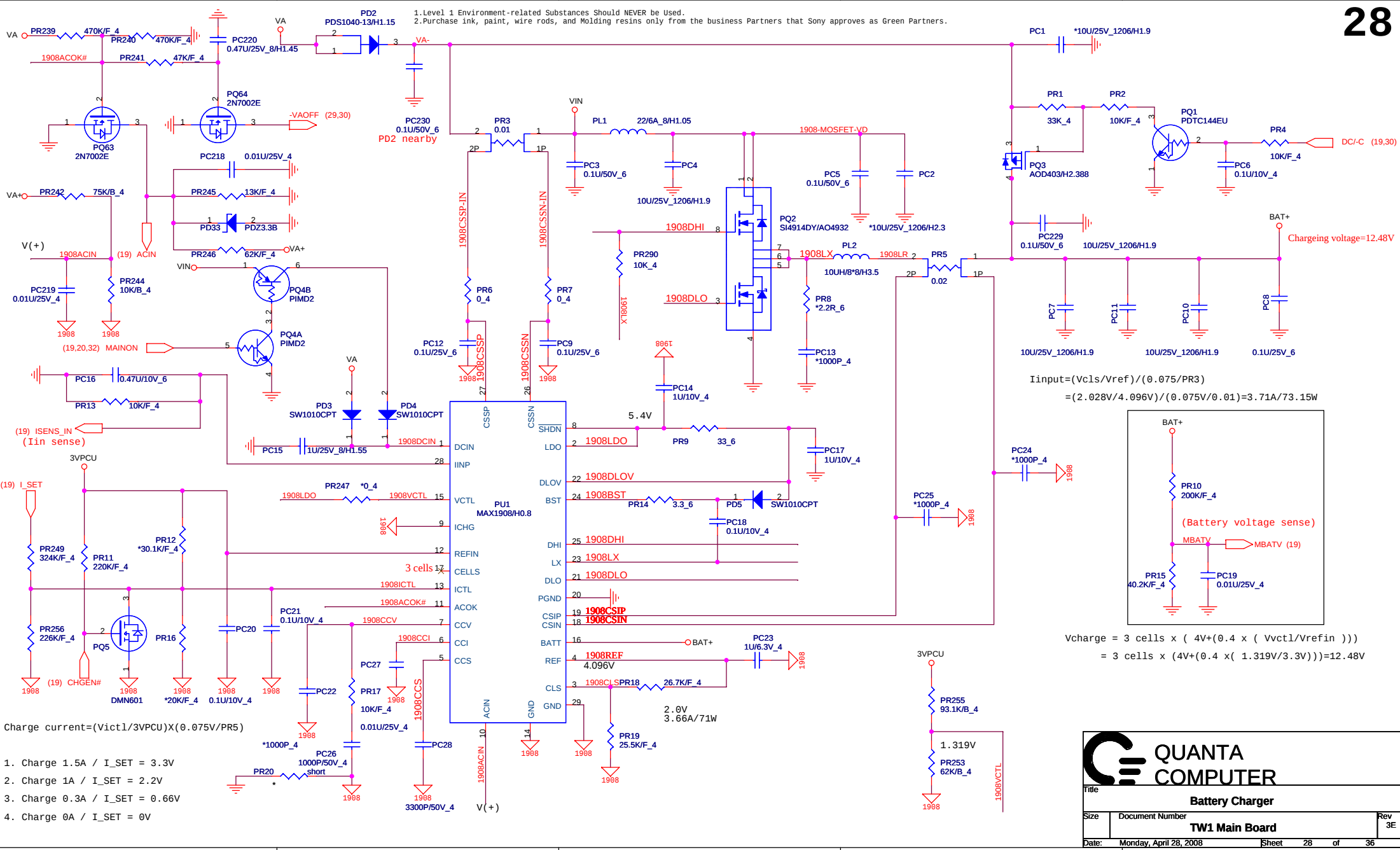
LED BOARD



1.This part should not contain any substances which are specified in SS-00259-1.
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

QUANTA
COMPUTER

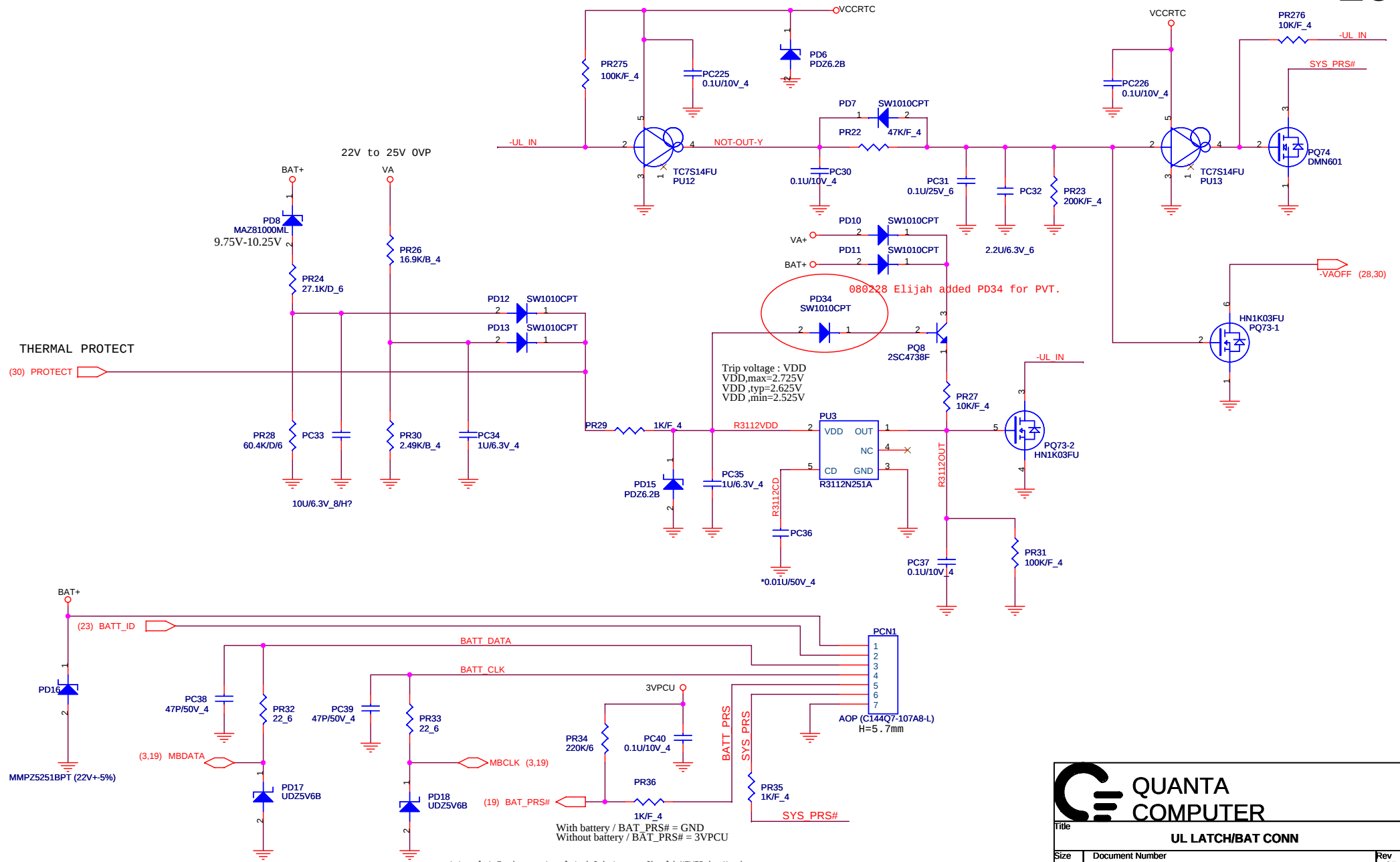
Title LED		
Size	Document Number	Rev 3E
TW1 Main Board		
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QUANTA

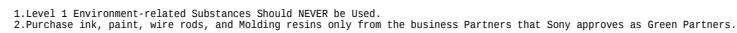
COMPUTER

Title			Battery Charger		
Size	Document Number				Rev
	TW1 Main Board				3E
Date:	Monday, April 28, 2008	Sheet	28	of	36



1. Level 1 Environment-related Substances Should NEVER be Used.
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 QUANTA COMPUTER		
Title UL LATCH/BAT CONN		
Size	Document Number	Rev 3E
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VCC_CORE

15uF/25V/6.8*6.8
85-185 degree/1.85A
-55-85 degree/2.2A

470uF/25V/10.5*10.5
185 degree/0.85A
18uF/25V_1206
Irms is about 3A.

Max Irms is about 7.35A to 9.73A.

PC49 is for EMI preparing.

VIN_6266A

080311 Elijah deleted PD25 & PG26 for PVT.

47A
VCC_CORE

Throttling temp.
185 degree C

(3) H_PROCHOT#

Panasonic
ERT-J0EV474J

Close to Phase 1 Inductor

Panasonic
ERT-J1VR103J

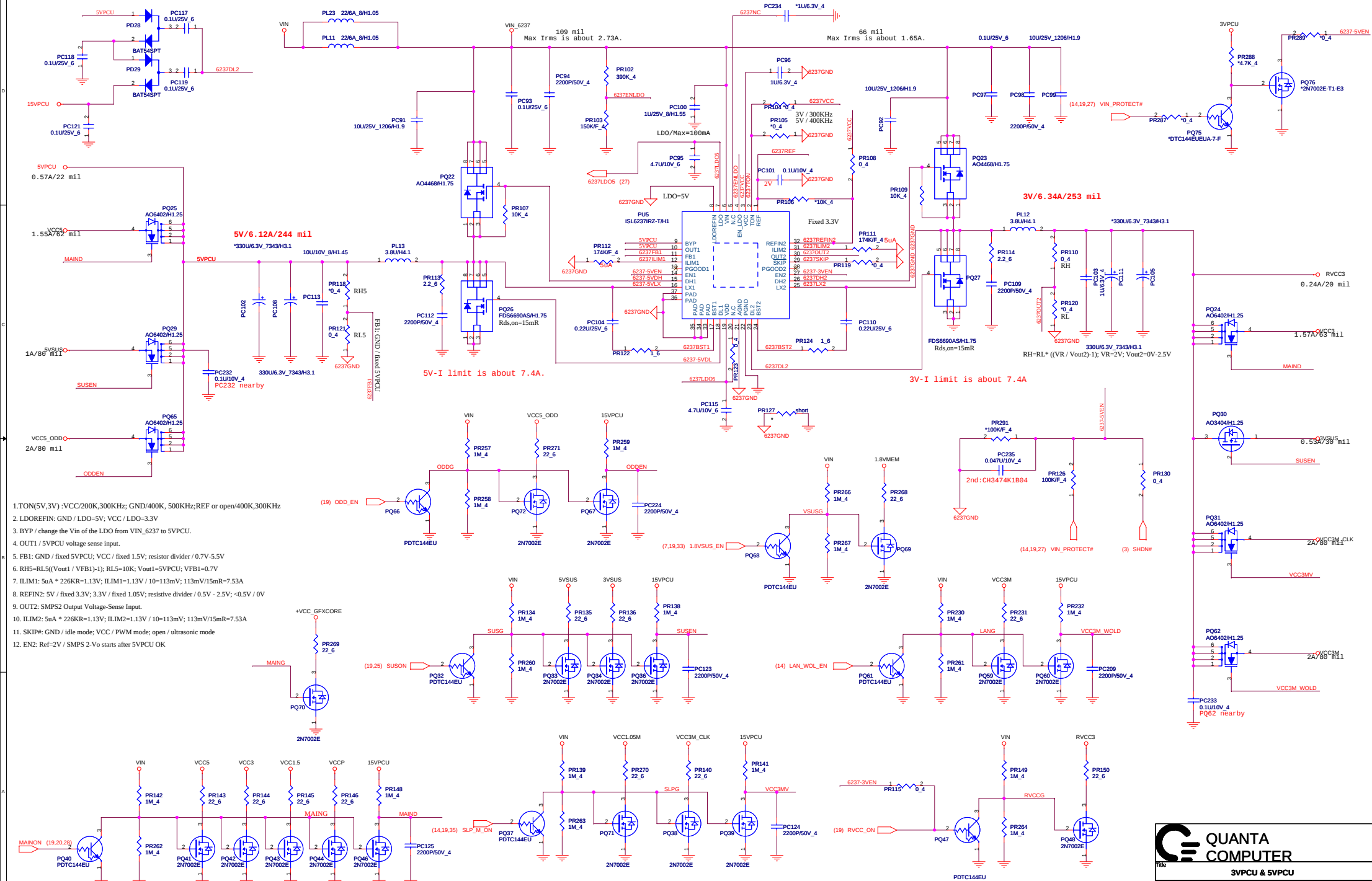
Close to Phase 1 Inductor

VID sets Vo = 1.25V
VID 6,5,4,3,2,1,0 = 0 0 1 0 1 0 0

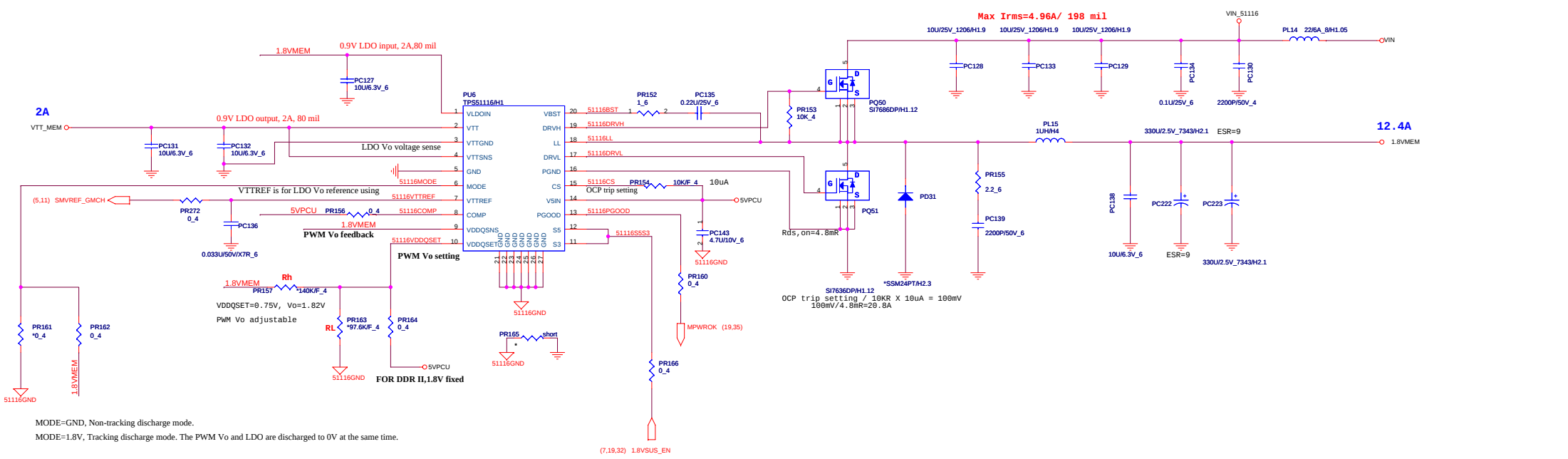
DPRSLPVR	DPRSTP#	PSI#	MODE
0	0	1	2 P CCM
0	0	0	1 P CCM

 QUANTA COMPUTER			
CPU CORE			
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1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



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- 1. Current sense method: Rds,on
- 2. D-CAP mode is quick PWM (set by connecting COMP to 5V).

VTT = VTTREF = VDDQSNS/2 = 0.9V

STATE	S3	S5	1.8VSUS	VTTREF	VTT
S8	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off

MODE	DISCHARGE MODE
+5V	No discharge
+1.8V	Tracking discharge
GND	Non-tracking discharge

VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	2.5 fixed	VDDQSNS/2	DDR
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

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QUANTA
COMPUTER

File

Size

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Rev

3E

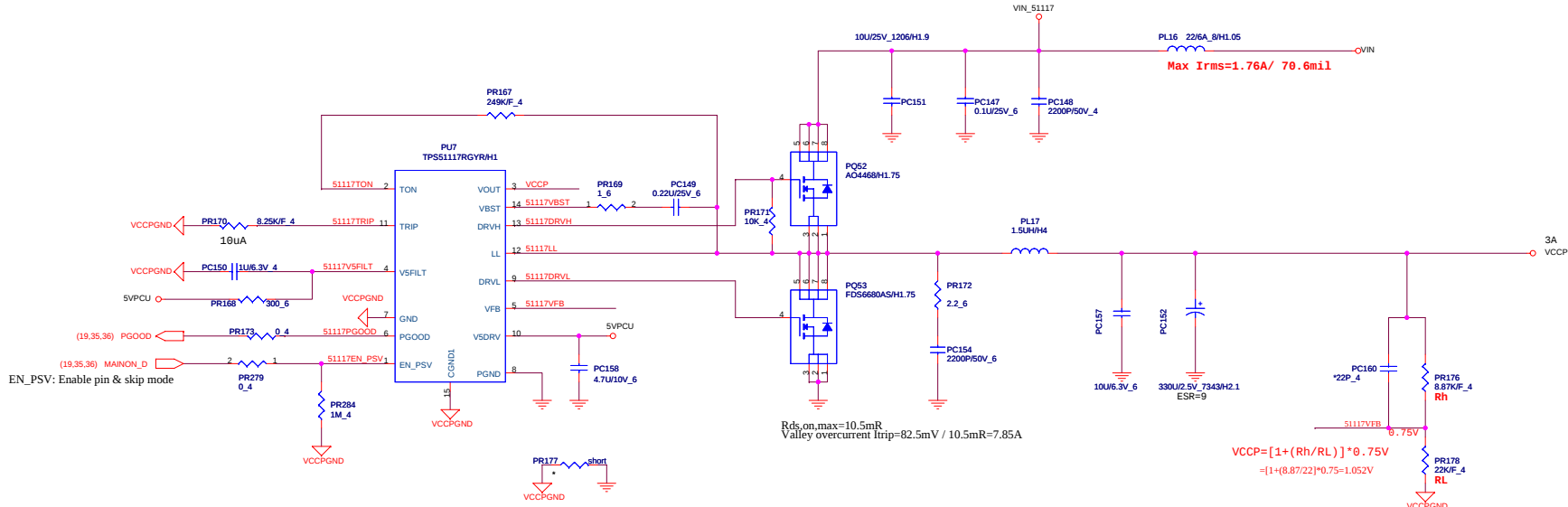
1.8VSUS/VTT_MEM

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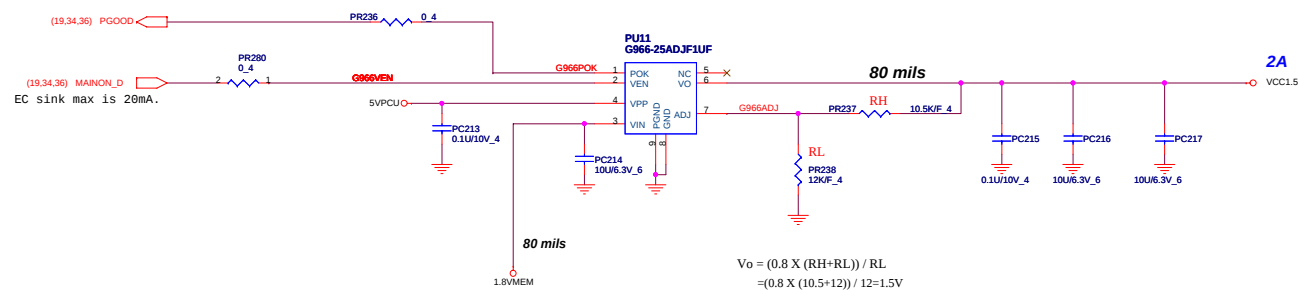
VCCP



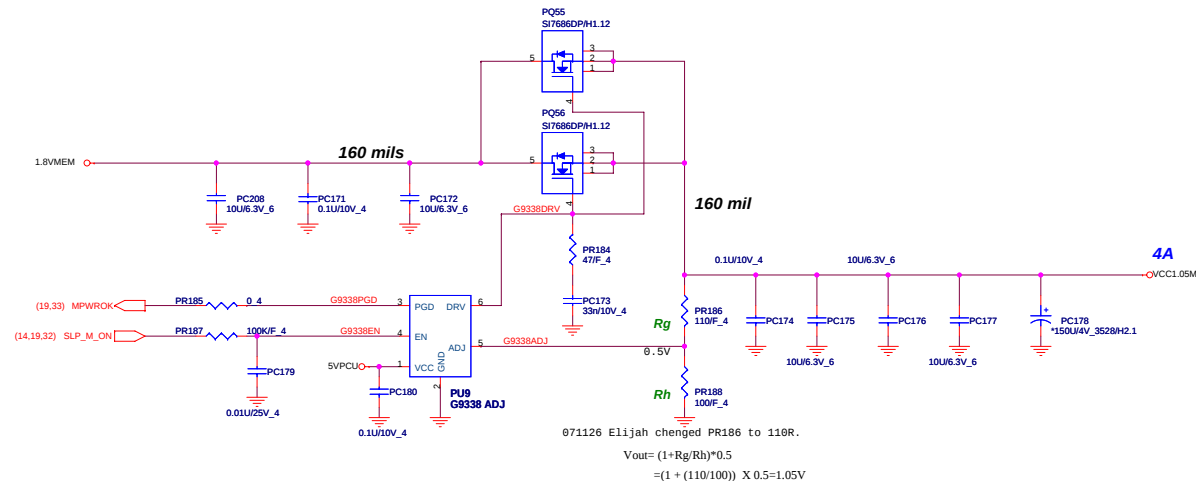
- 1. RTON=200KR, Fs is about 330KHz by the spec table
- 2. TON: $0.21\mu s / V_{in}=19.4V$; $0.374\mu s / V_{in}=9V$ by the spec equation
- 3. TRIP (the trip level of the valley overcurrent): $V_{trip}(mV)=R_{trip}(KR) * 10\mu A=10KR*10\mu A=100mV$
- 4. VSFLT: the VCC of the TPS51117
- 5. VOUT: Output voltage monitor & output discharge.
- 6. VFB: Vo feedback input.
- 7. VSDRV: the driving power of the low side MOSFET

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VCC1.5



VCC1.05M



RENDER MODE	FDE	AF_EN	DEM STATUS	Voltage Window	Audio Filter
SUSPEND	0	1	Enabled	130% NOM	Enabled

Fswitch > 25KHz at the light load.
Because the audio filter is enable.

