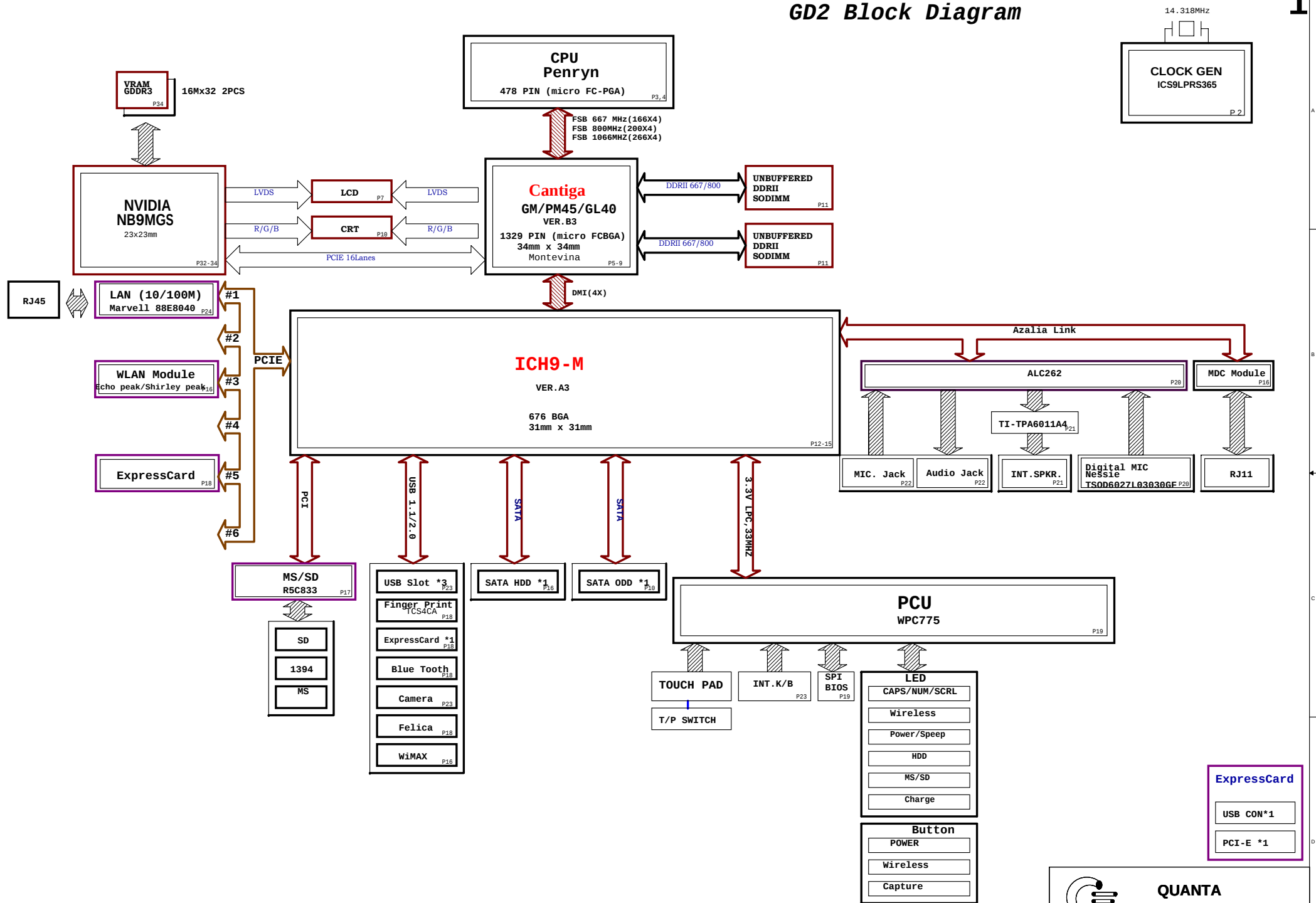
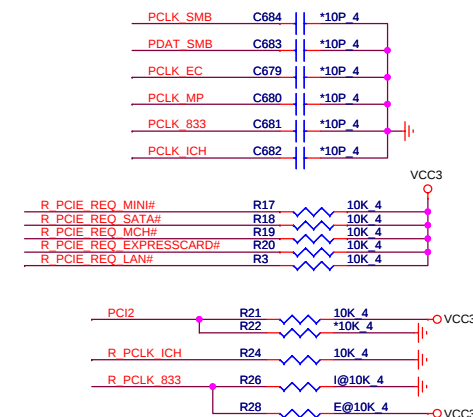
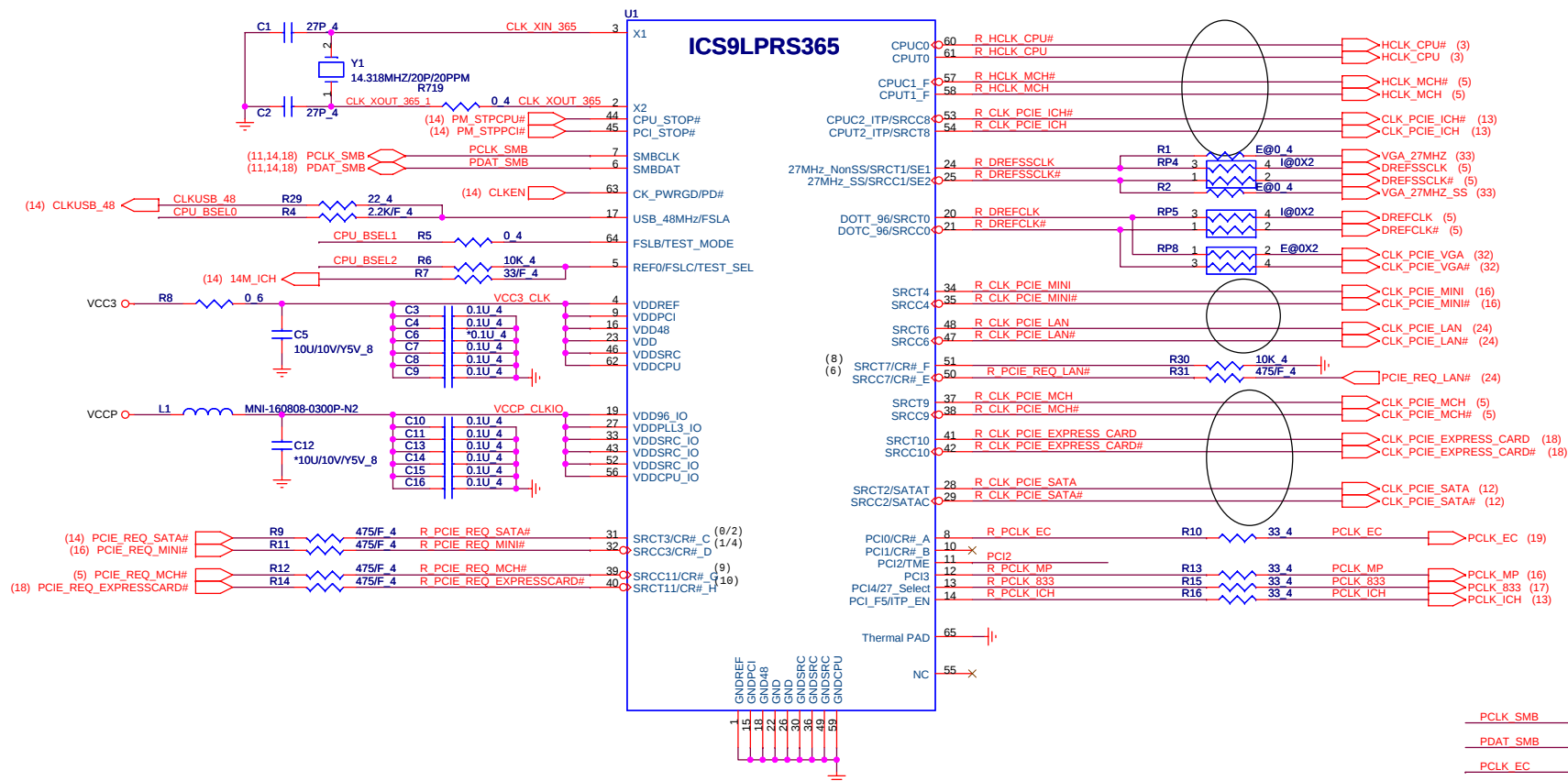


GD2 Block Diagram

1





FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %
* 0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
0	1	0	200.00	100	33.33	14.318	48	96	0.5 Down
0	1	1	166.66	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	RESERVED						

TME(PIN11)		
0 : Overclocking of CPU & SRC allowed.		
* 1 : Overclocking of CPU & SRC NOT allowed.		

27 Select PIN13	PIN 20/21	PIN 24/25
0	DOT_96 / DOT_96#	LCDCCLK / LCDCCLK#
1	SRC_0 / SRC_0#	27M / 27M_SS

(Int. Graphic)
(NB9M-GS)

ITP_EN(PIN14)	PIN53/54
* 0	SRC8/SRC8#
1	ITP/ITP#

QUANTA COMPUTER

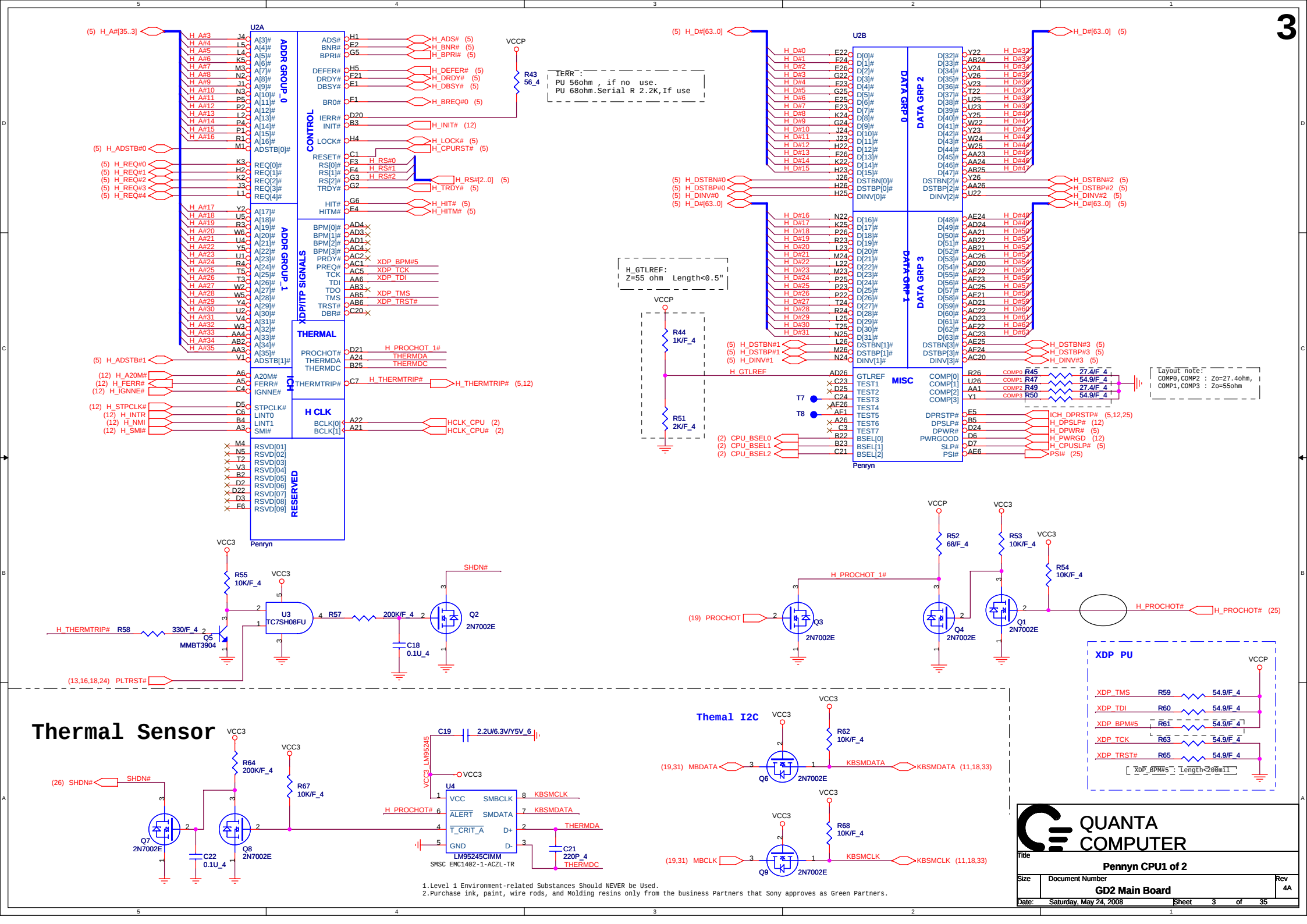
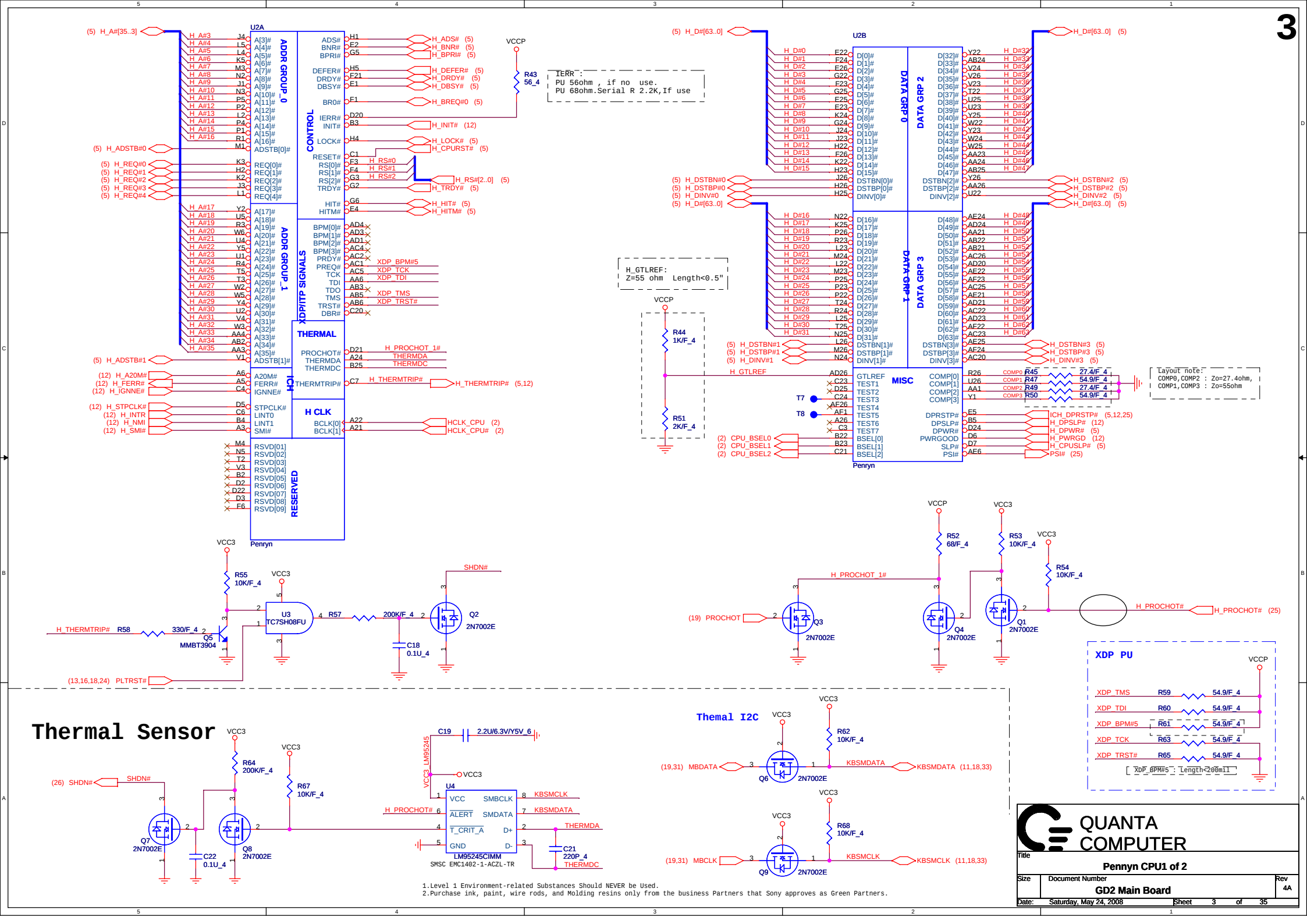
Model: **CLOCK GENERATOR**

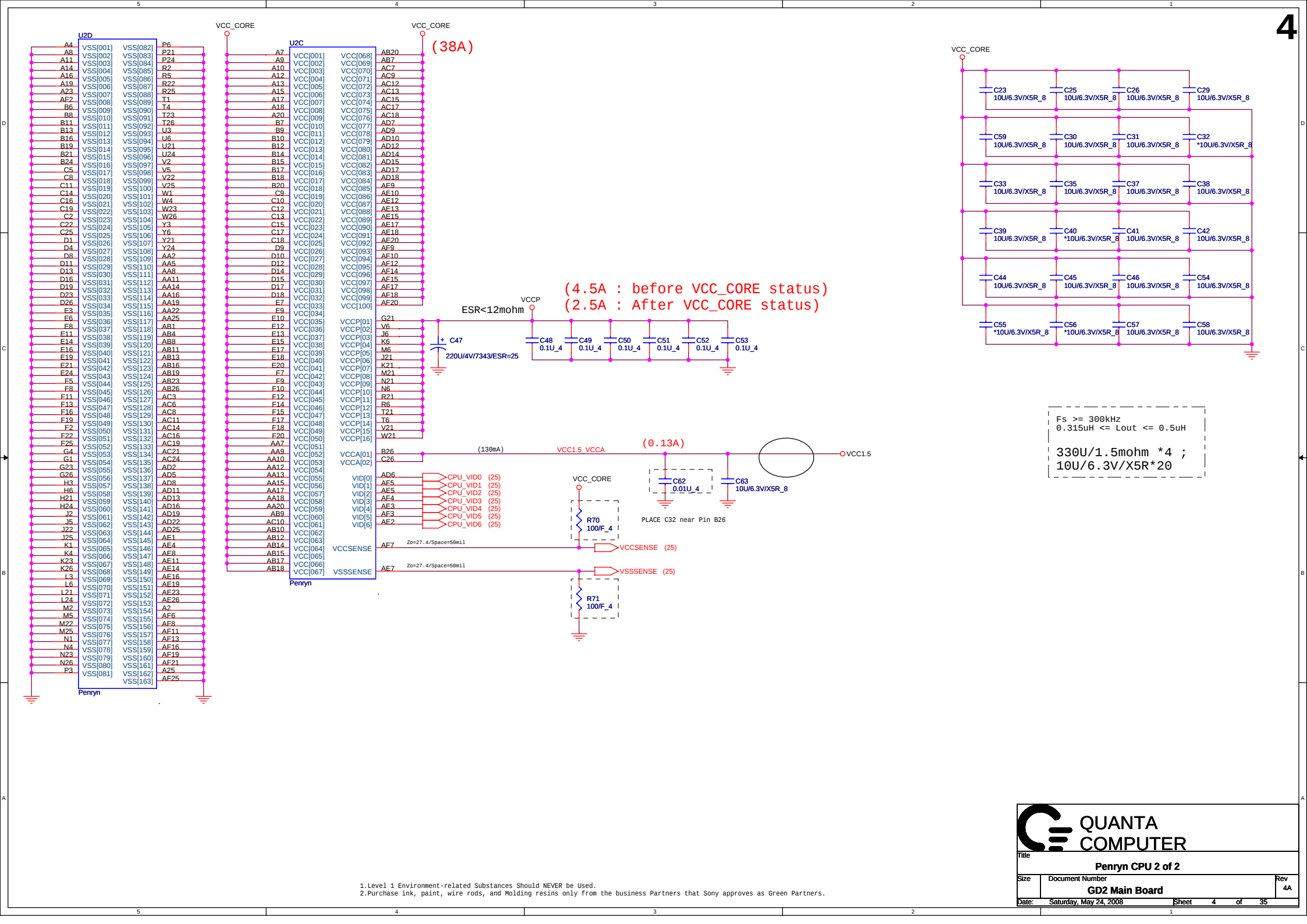
Document Number: **GD2 Main Board**

Date: **Saturday, May 24, 2008**

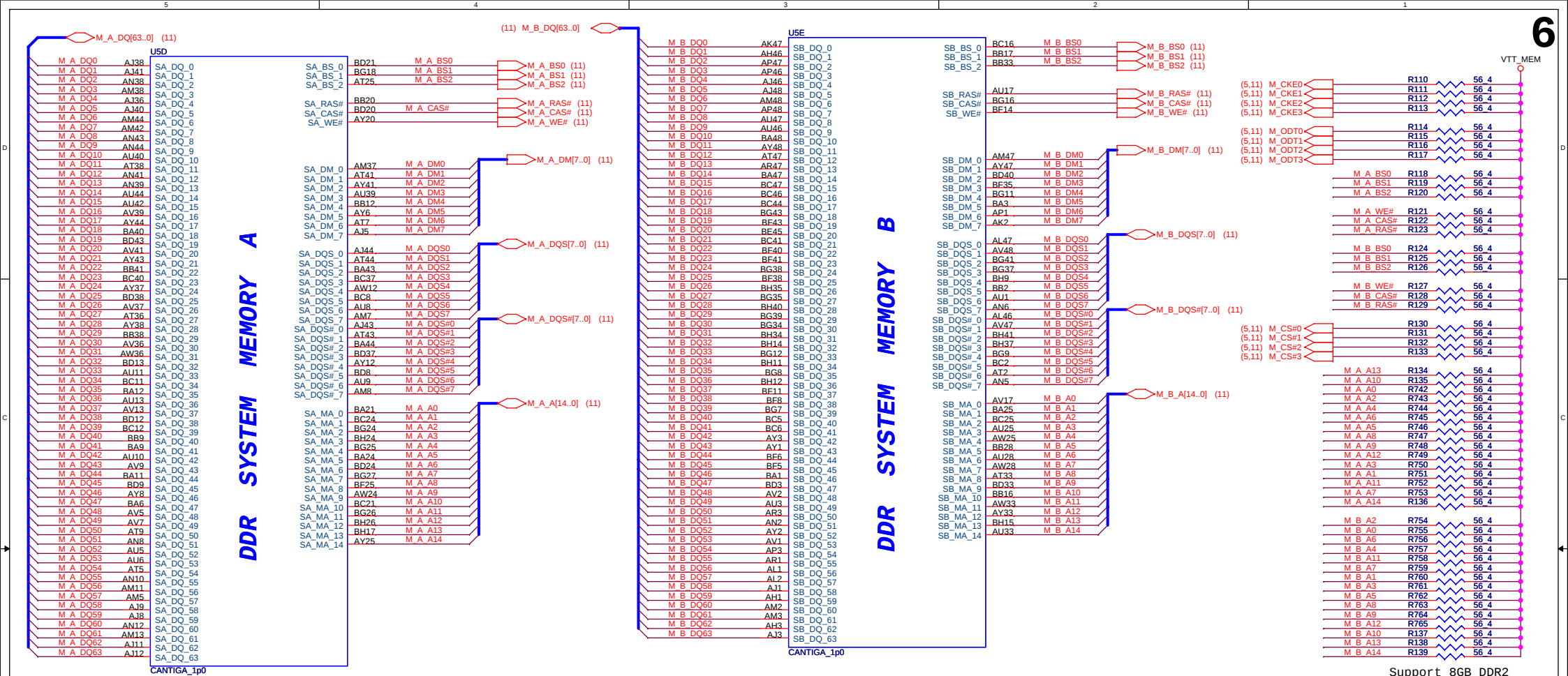
Sheet: **2** of **35**

Rev: **4A**









Support 8GB DDR2

GMCH Strap pin description

Low		High
CGF5	DMIX2	* DMIX4
CGF6	ITPM HOST interface enable	* ITPM HOST interface disable
CGF7	AMT Firewall will use TLS cipher suite with no confidentiality	* AMT Firewall will use TLS cipher suite with confidentiality
CGF9	PCIE Graphics lan : Reverse Lane	* PCIE Graphics lan : Normal operation
CGF10	PCIE Loopback enable	* PCIE Loopback disable
CGF16	FSB Dynamic ODT Disabled	* FSB Dynamic ODT Enabled
CGF19 *	DMI LANE Normal	DMI LANE Reversed
CGF20 *	only SDVO/DP/HDMI or PCIE is operational	SDVO/DP/HDMI and PCIE are operational simultaneously via the PEG port
CGF[12:13]:XOR /ALLZ / Clock Un-gating 00 = Reserve 01 = XOR mode enabled 10 = All-Z mode enabled * 11 = Normal Operation(Default)		
Int.Pull-down : CGF 18,19,20 Int.Pull-high : CGF CGF 3~17		

(5) MCH_CFG_6  T49

(5) MCH_CFG_5  T50

(5) MCH_CFG_7  T51

(5) MCH_CFG_9  T52

(5) MCH_CFG_10  T53

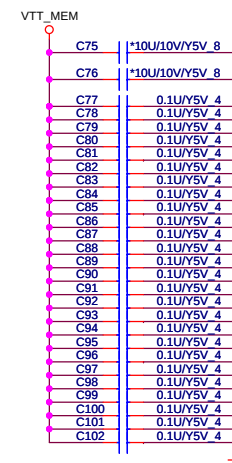
(5) MCH_CFG_12  T54

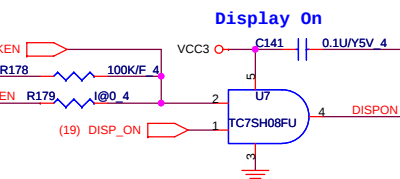
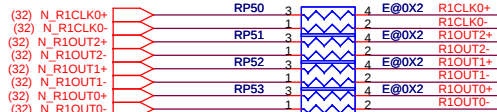
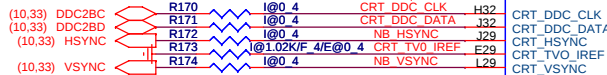
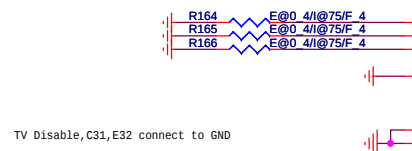
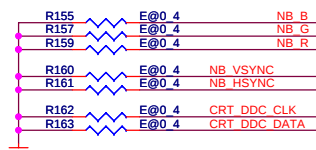
(5) MCH_CFG_13  T55

(5) MCH_CFG_16  T56

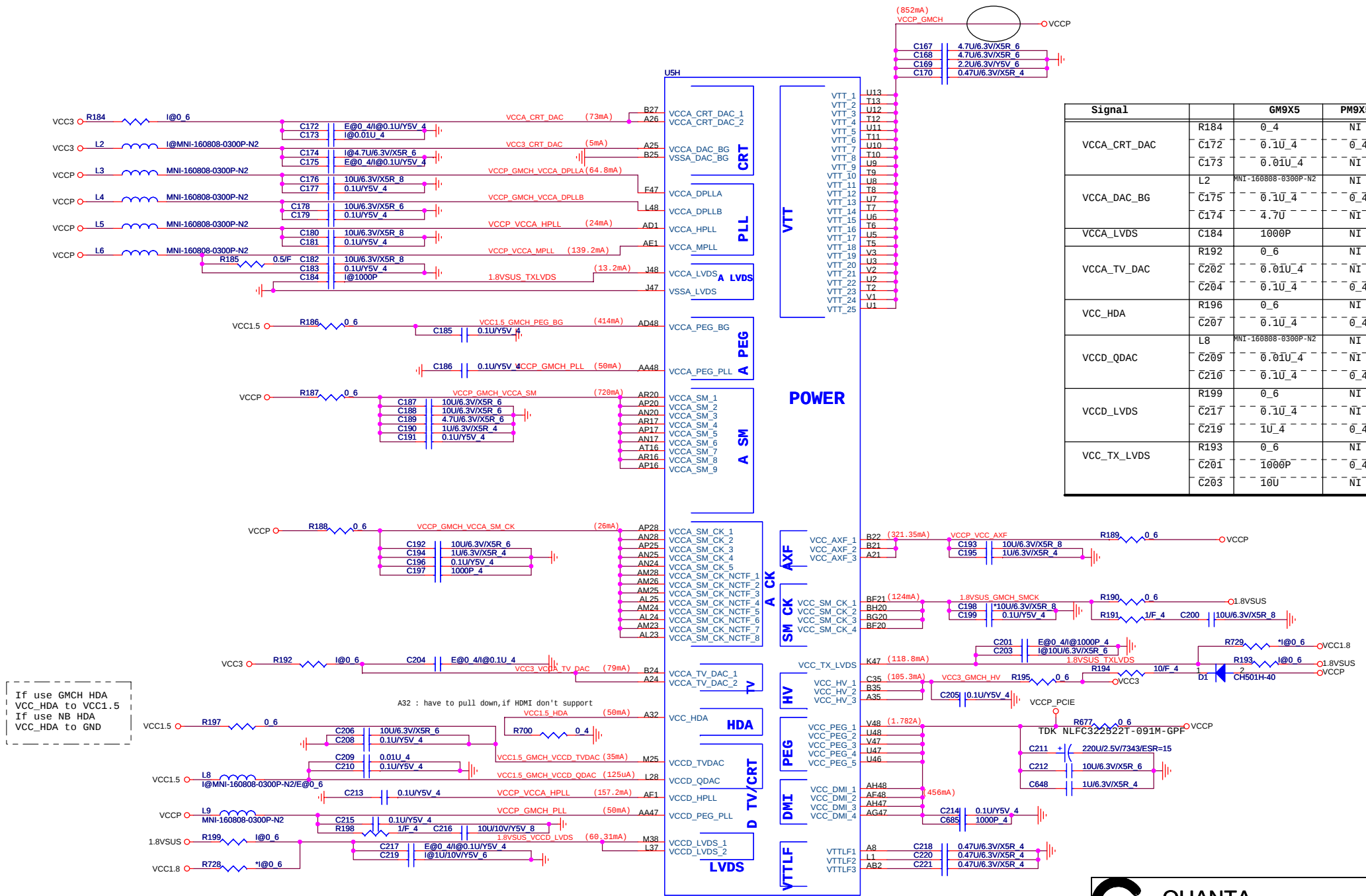
(5) MCH_CFG_19  T57

(5) MCH_CFG_20  T58

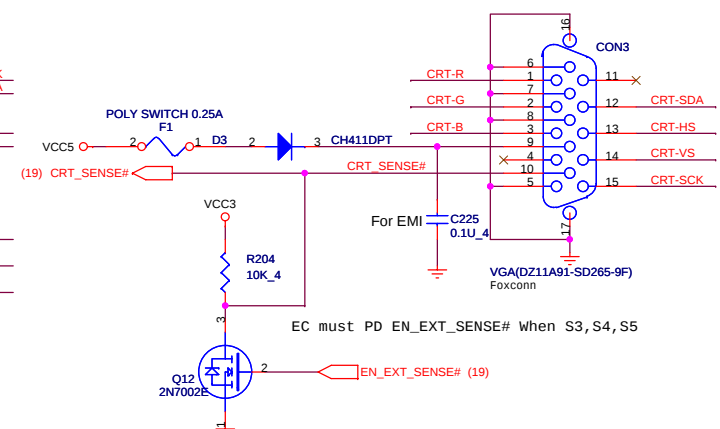
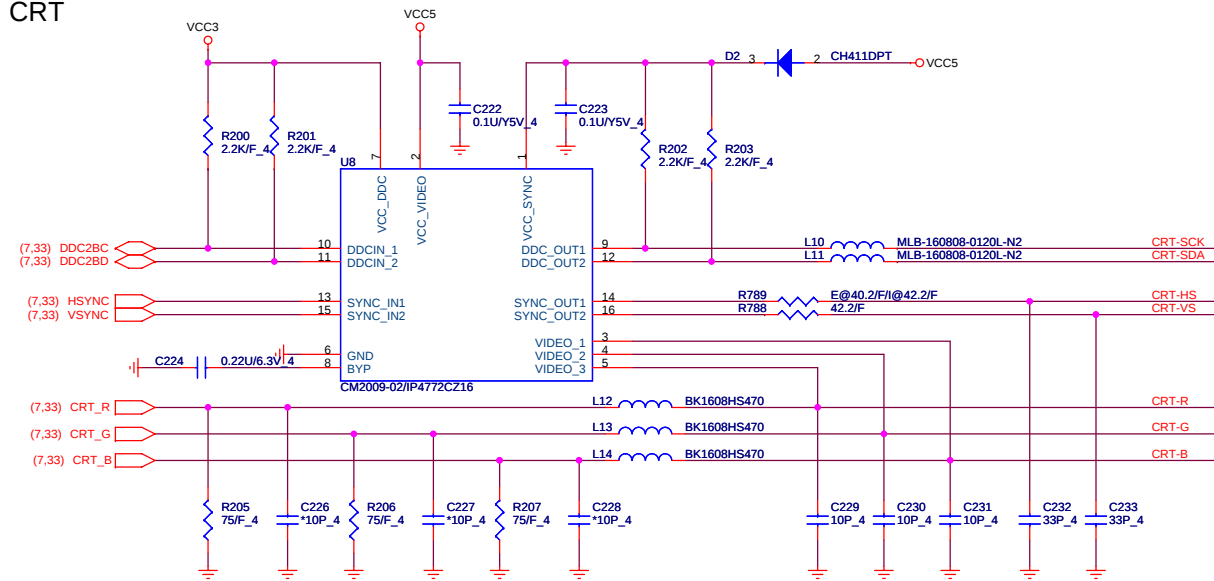




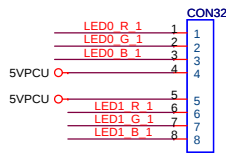
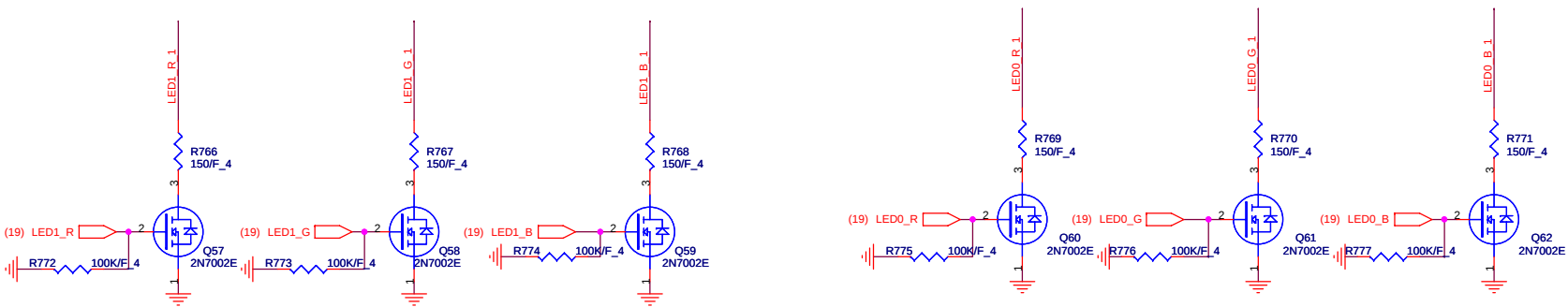
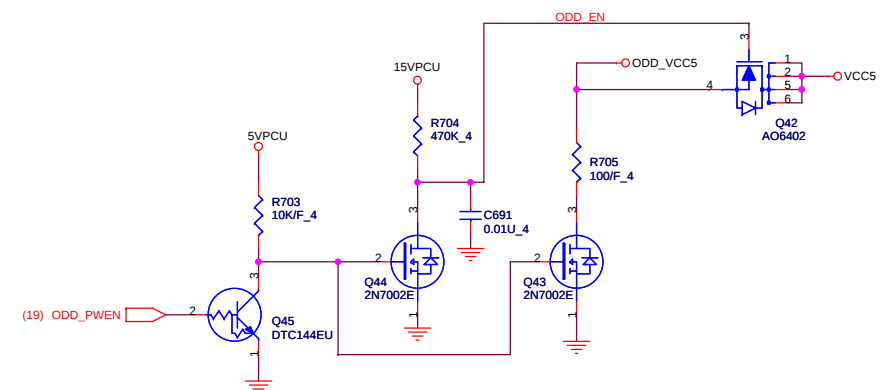
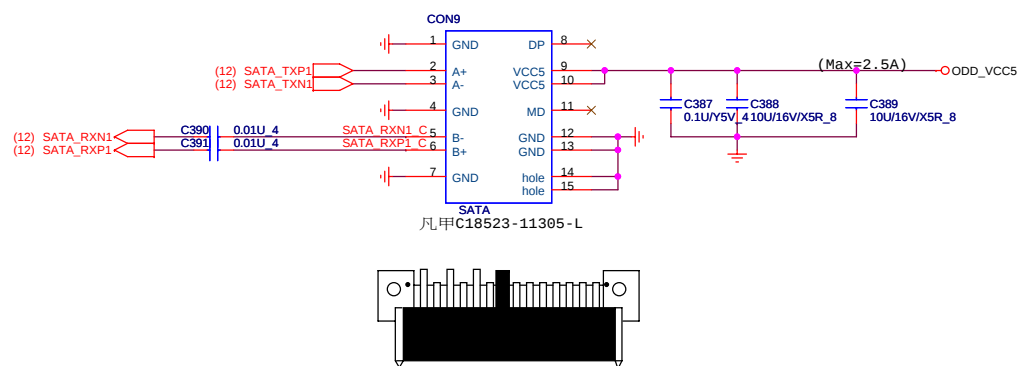
 QUANTA COMPUTER			
Title			
GMCH DMI VEDIO 3 of 5			
Size	Document Number	Re	
GD2 Main Board			
Date:	Saturday, May 24, 2008	Sheet	7 of 35



CRT



ODD CONNECTOR



7LEDA-(87212-0800L)

QUANTA COMPUTER

Title: CRT

Size: Custom

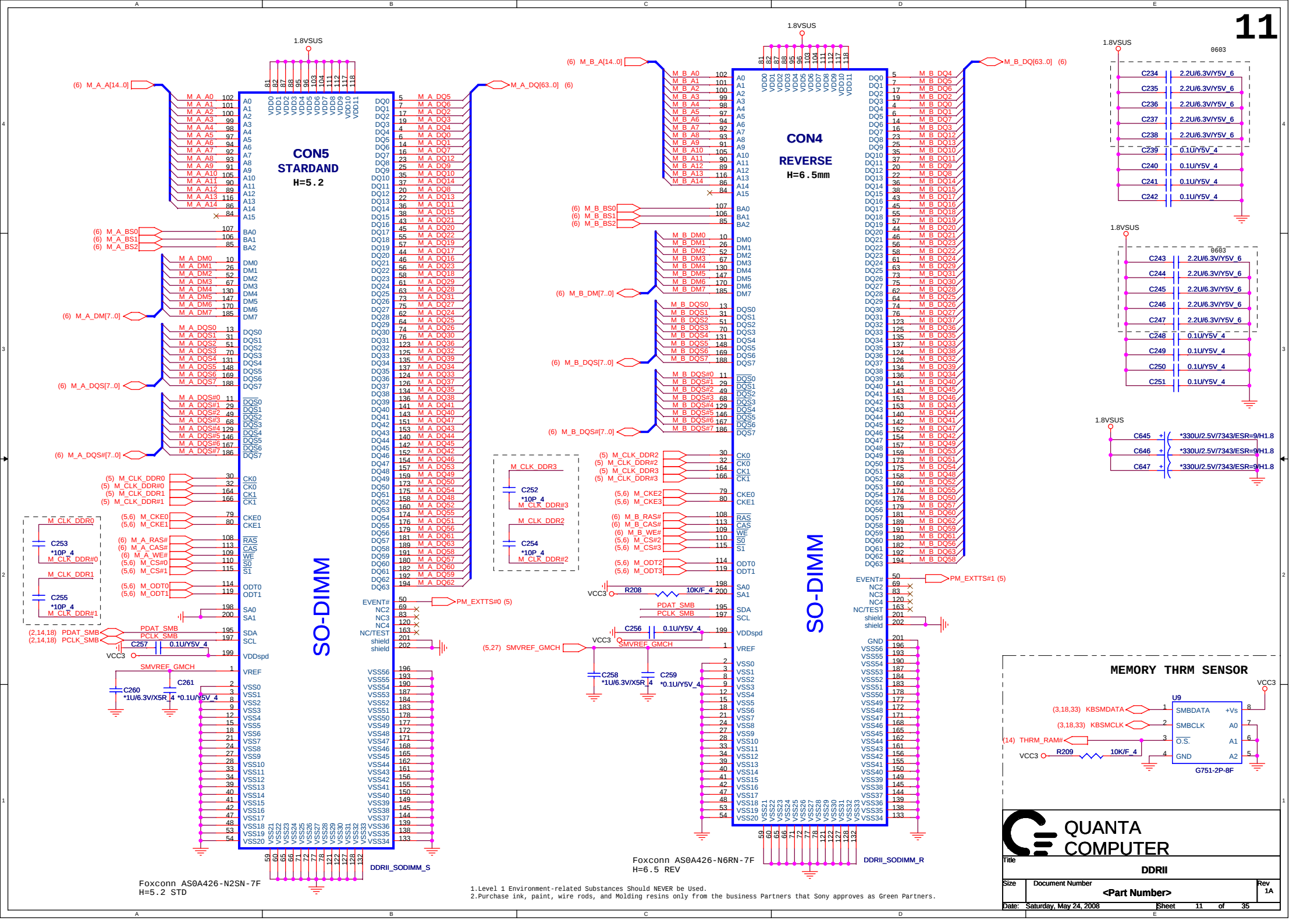
Document Number: GD2 Main Board

Date: Saturday, May 24, 2008

Sheet: 10 of 35

Rev: 4A

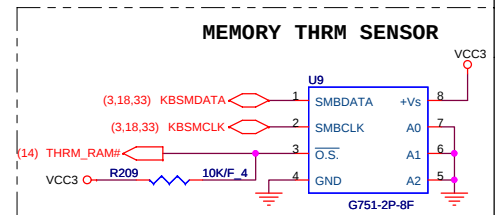
1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



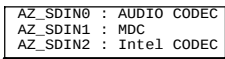
Foxconn AS0A426-N2SN-7F
H=5.2 STD

Foxconn AS0A426-N6RN-7F
H=6.5 REV

- Level 1 Environment-related Substances Should NEVER be Used.
- Purchase Ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



QUANTA COMPUTER		
Title: DDRII		
Size:	Document Number:	Rev 1A
Date: Saturday, May 24, 2008		
Sheet 11 of 35		



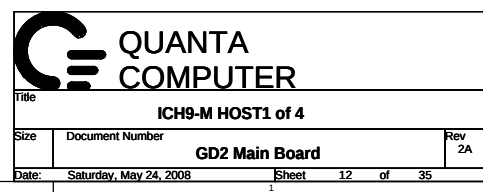
System HDD

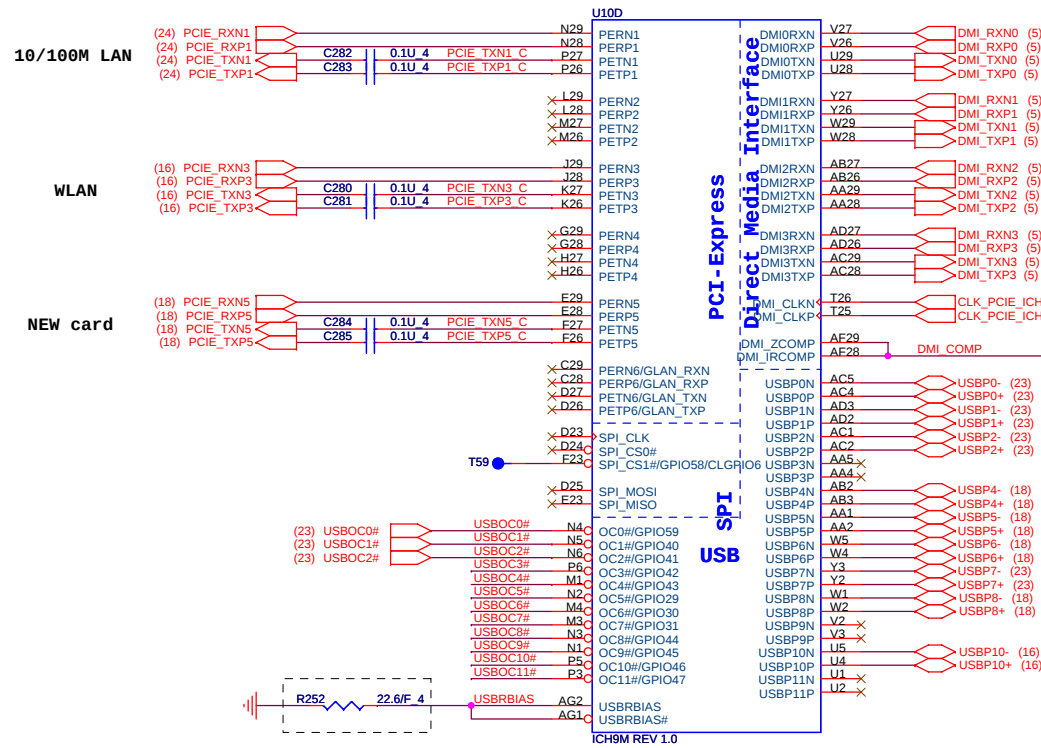
System ODD

ICH_TP3	ACZ_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	* Normal operation
1	1	Set PCIe port config bit 1

	INTVRMEN
Enable (default)	1
Disable	0

VCCRTC
 R240
 332K/F_4
 ICH_INTVRMEN





USB_PORT #0

USB_PORT #1

USB_PORT #2

Blue Tooth

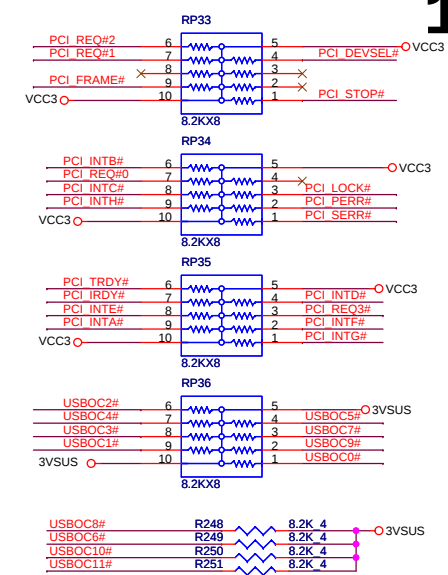
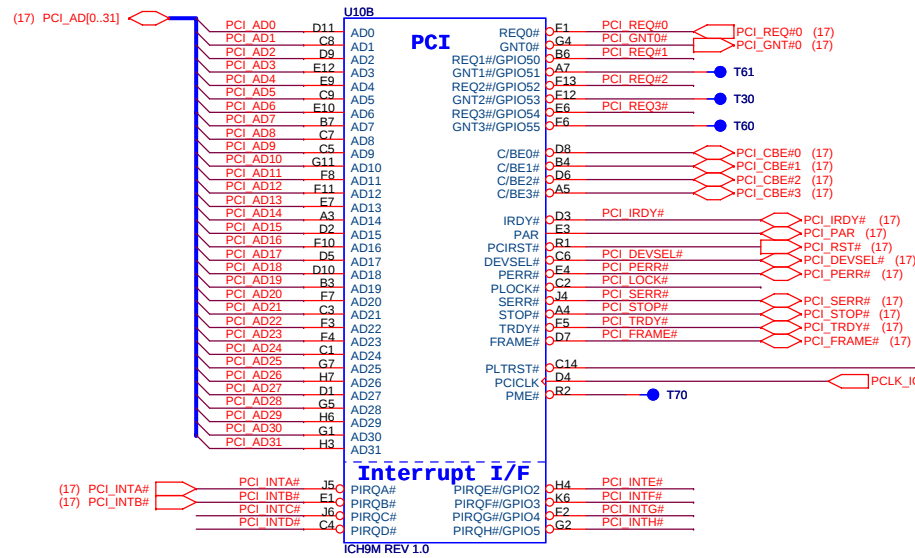
EXPRESS CARD

Finger Print

Camera

Felica

WiMAX



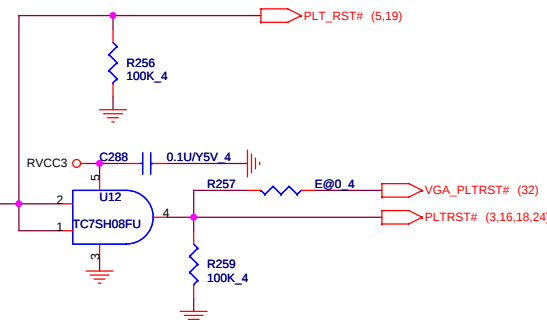
GPIO49 : NC
GPIO20 : Can't pull high.

A16 SWAP Override strap

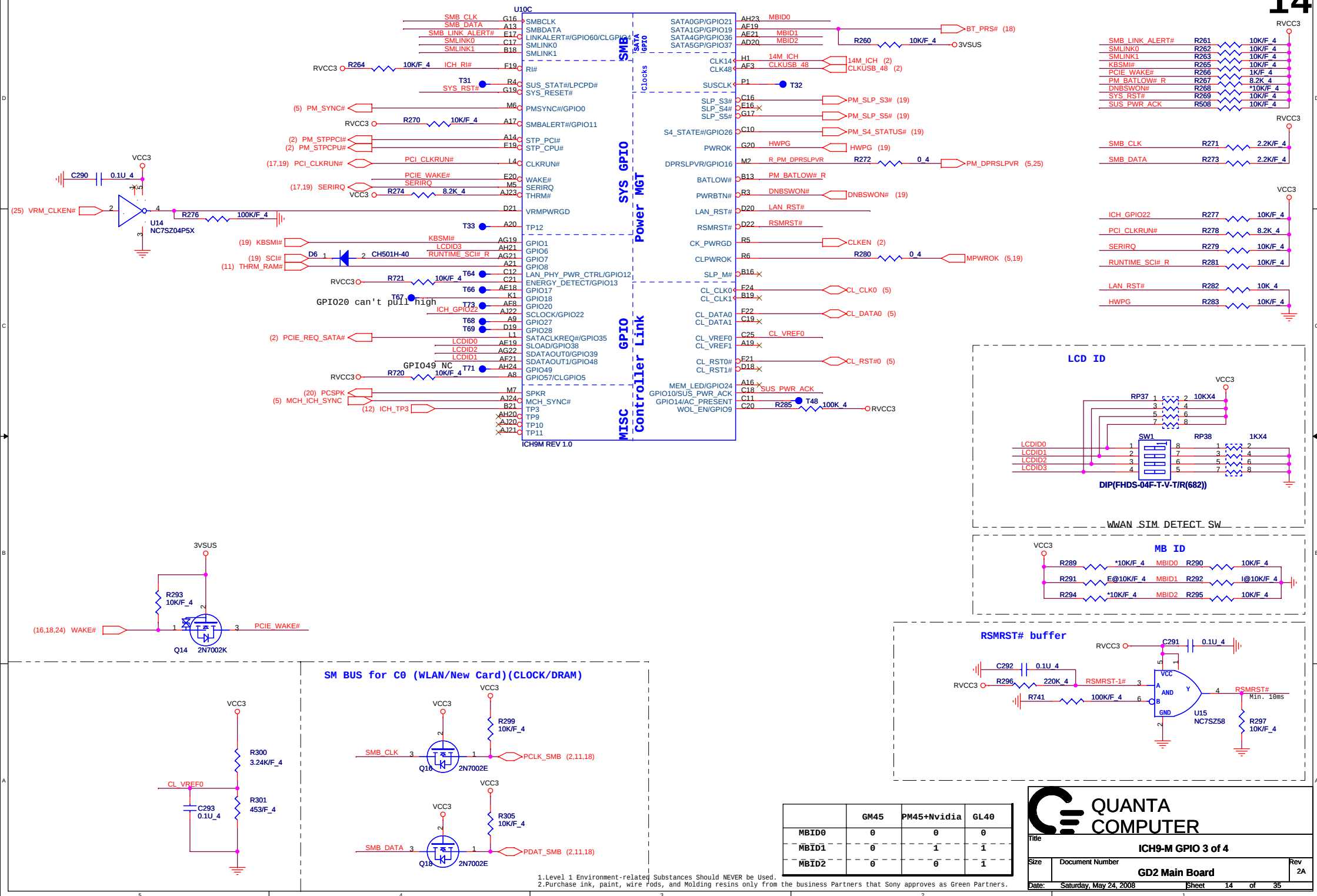
PCI_GNT#3 Low = A16 swap override enabled
High = Default

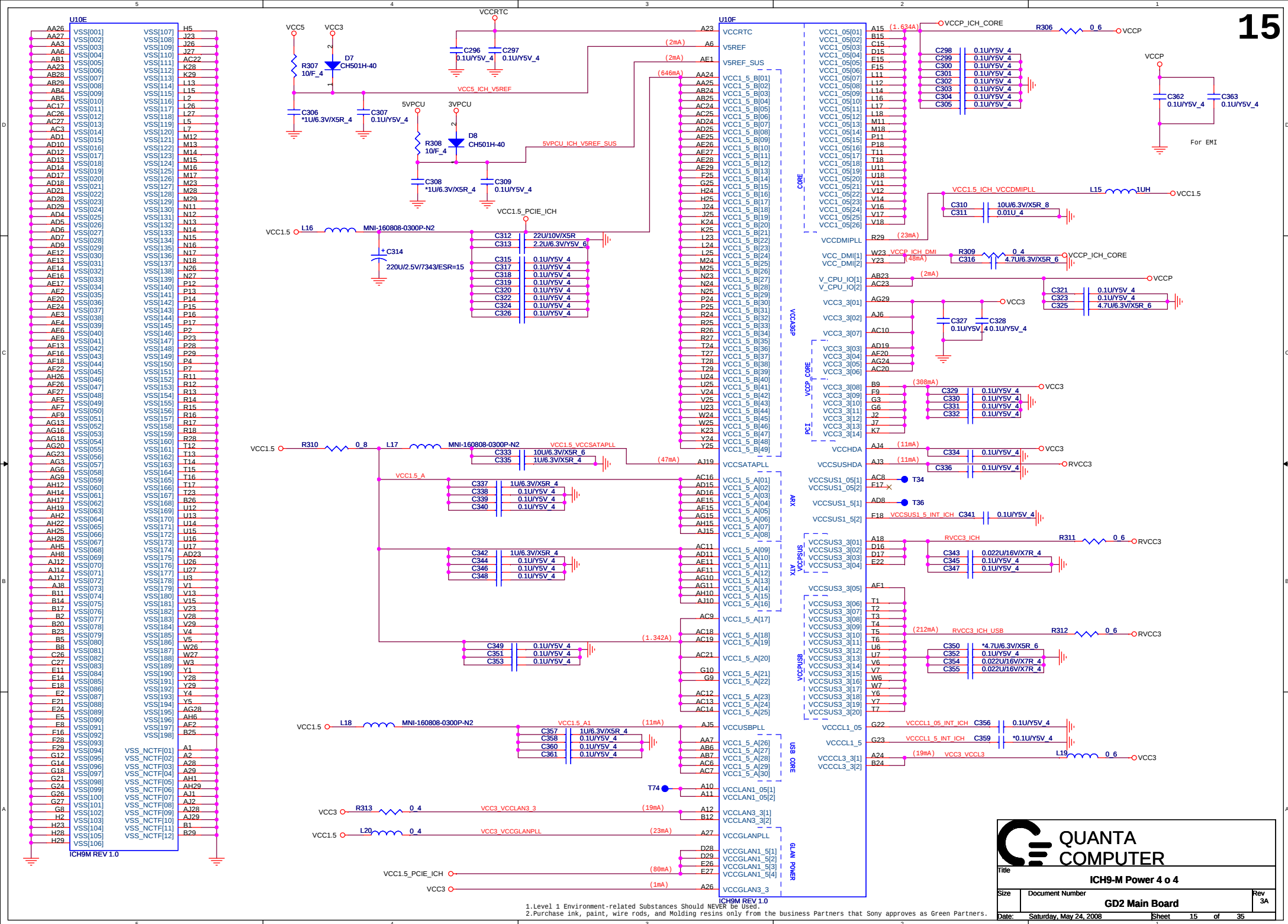
IC9M Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (Default)



Title			IC9M-PCIE 2 of 4		
Size	Document Number				
GD2 Main Board					
Date	Saturday, May 24, 2008				
Sheet 13					of 35
Rev 2A					



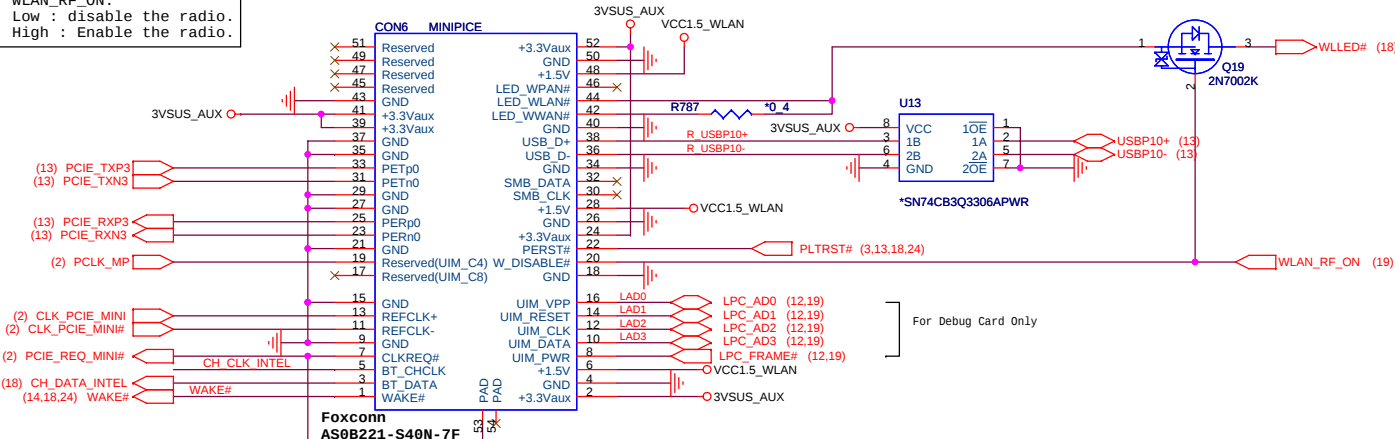


2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Mini PCI-E Card FOR WL

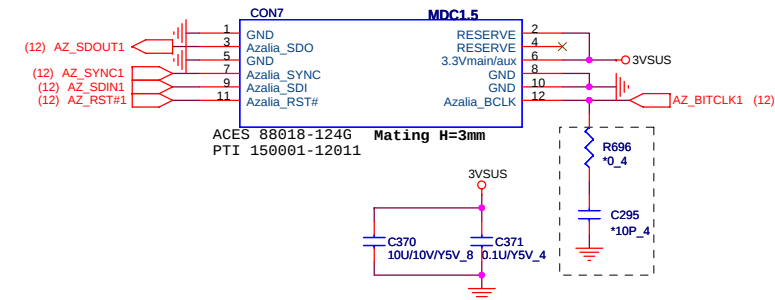
16

WLAN_RF_ON:
Low : disable the radio.
High : Enable the radio.

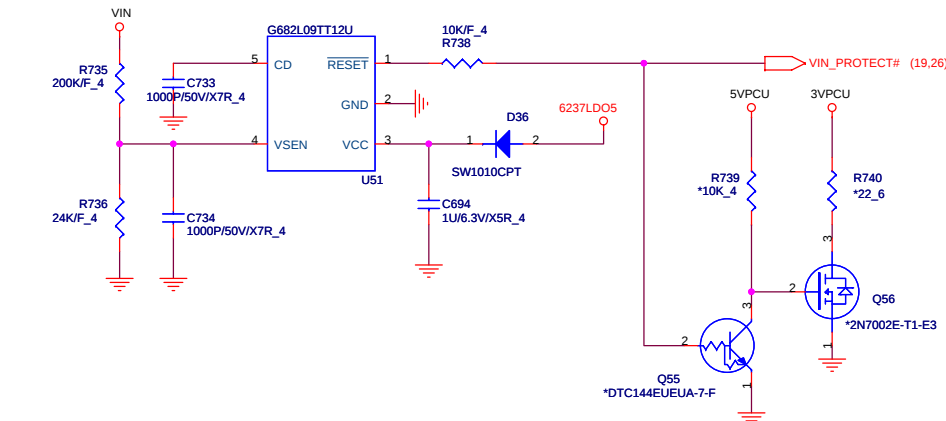


SM BUS ADDRESS	A6	A5	A4	A3	A2	A1	A0
CPU LM95245C1MM	1	0	0	1	1	0	0
EMC1402-1							
NB9MGS LM89-1/G781-1	1	0	0	1	1	0	1
DRAM G751-2P	1	0	0	1	0	0	0
Thermal G751-2P	1	0	0	1	0	0	1

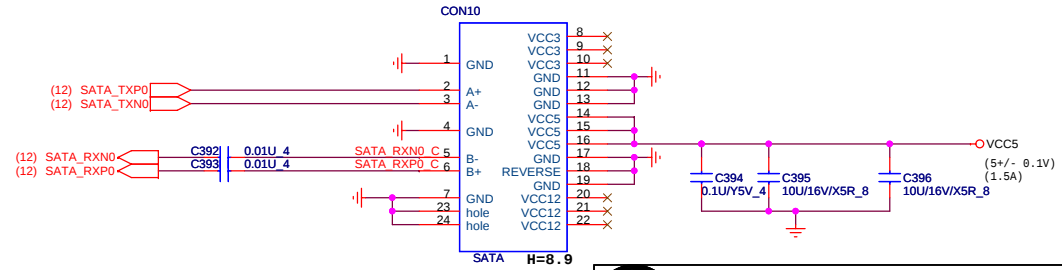
MDC V1.5



Reset Circuit



HDD CONNECTOR



QUANTA COMPUTER

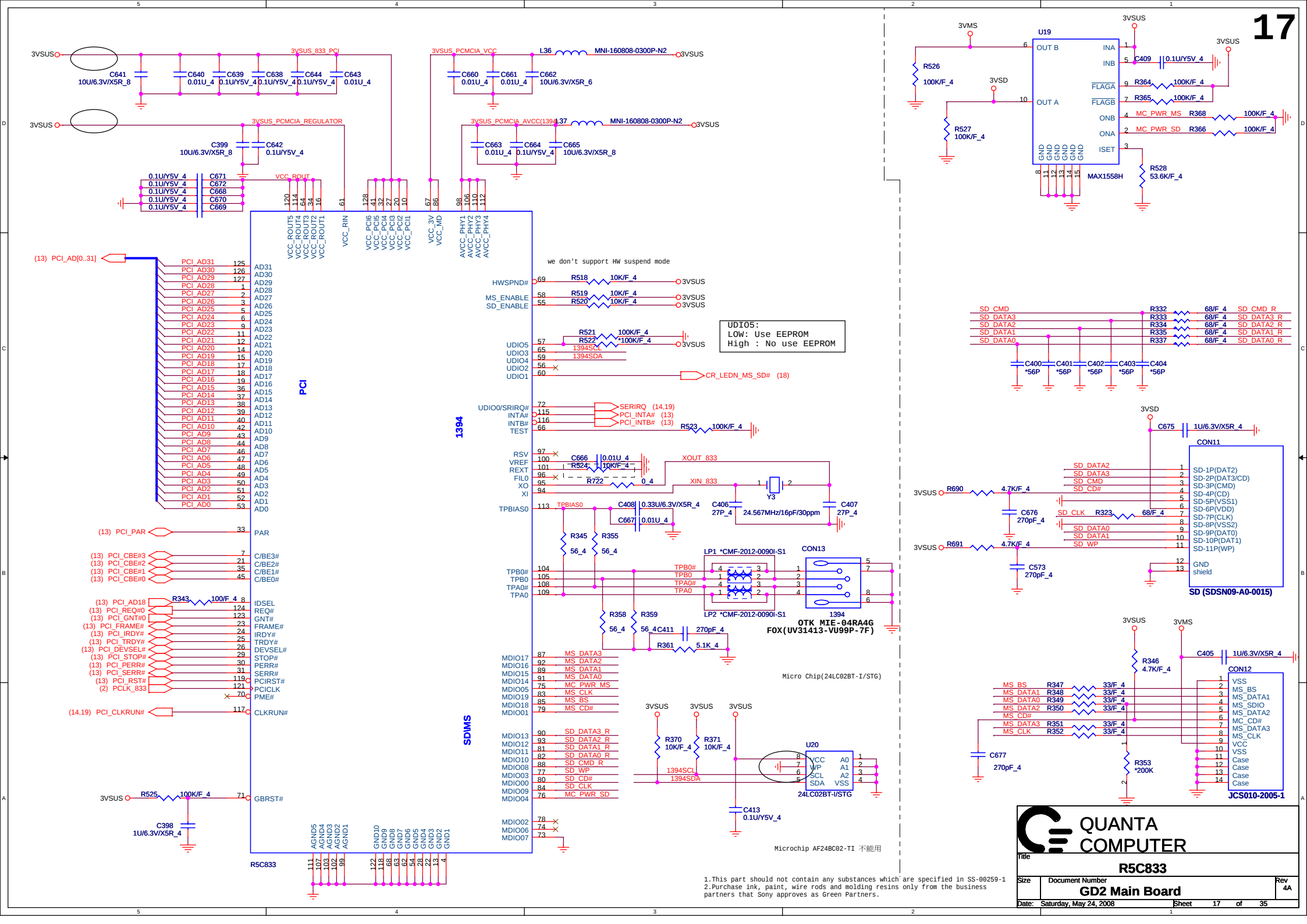
MINIPCE / MDC

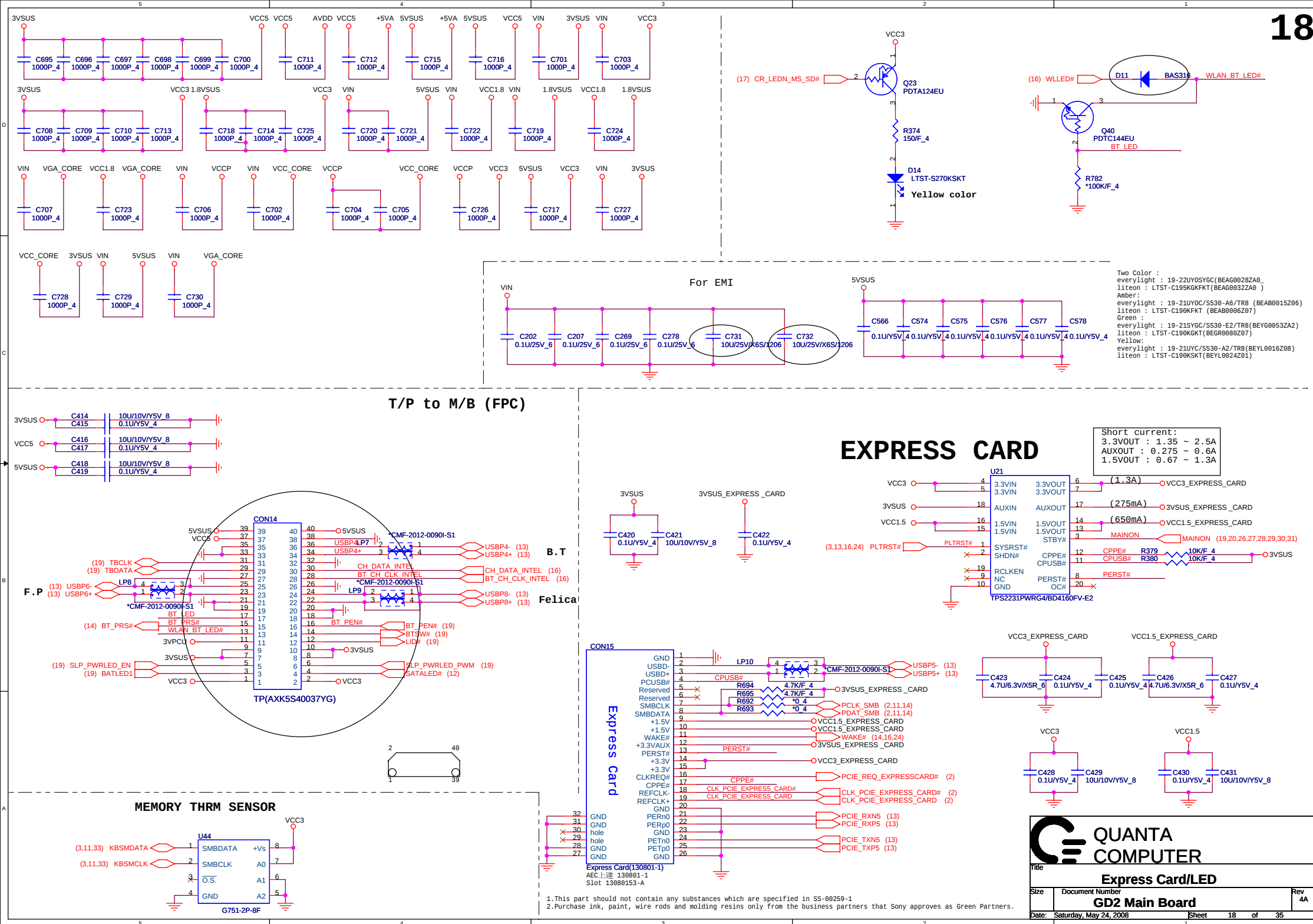
Document Number: GD2 Main Board

Date: Saturday, May 24, 2008

Sheet 16 of 35

1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

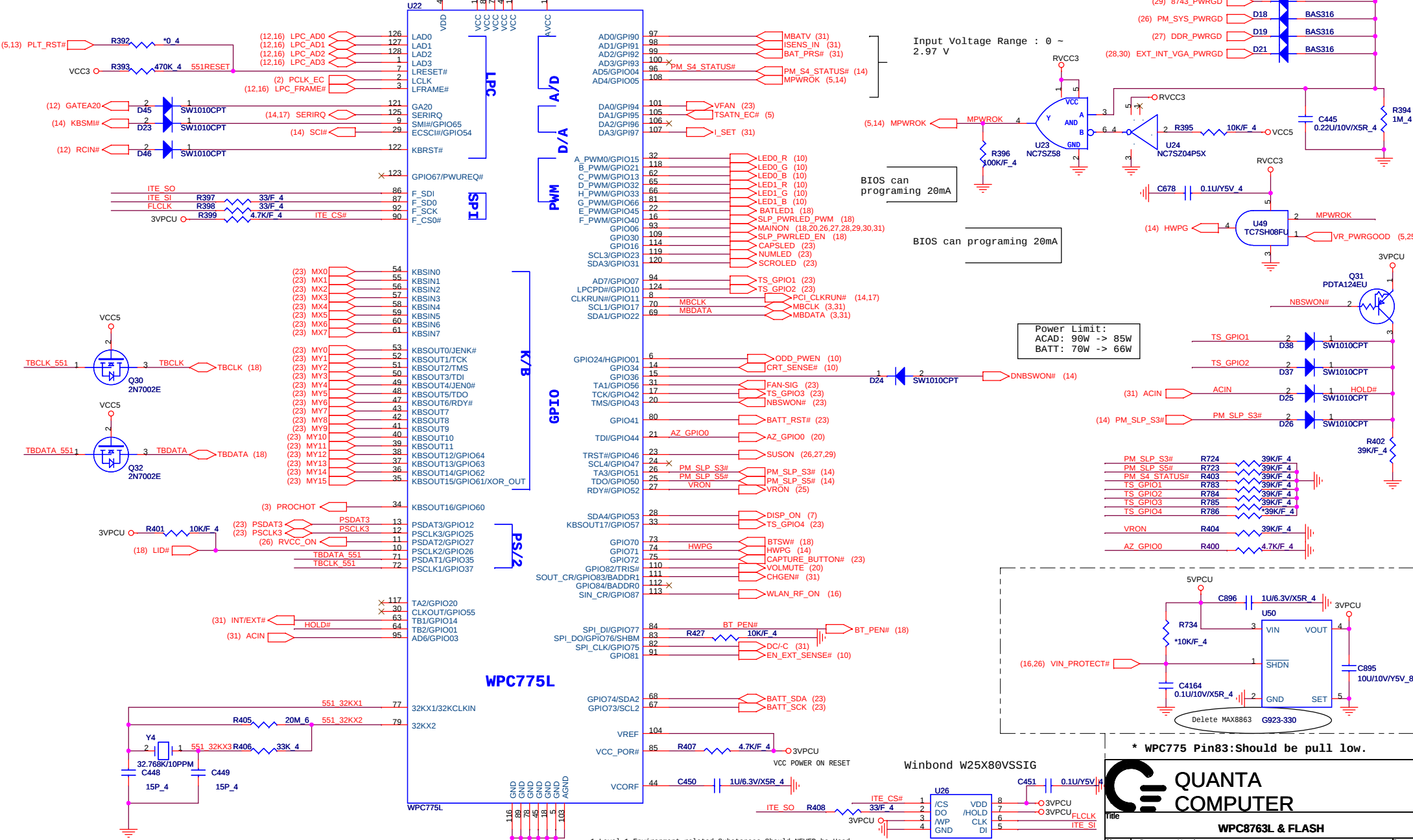




I/O Address			
BADDR1-0		Index	Data
1	0	2E	2F
1	1	4E	4F
0	0	(HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1	
0	1	XOR-TREE TEST	

SHMB: SHBM(If = 0 Enable share host BIOS memory)

CHGEN# : BADDR0
T?: BADDR1



* WPC775 Pin83: Should be pull low.

QUANTA COMPUTER

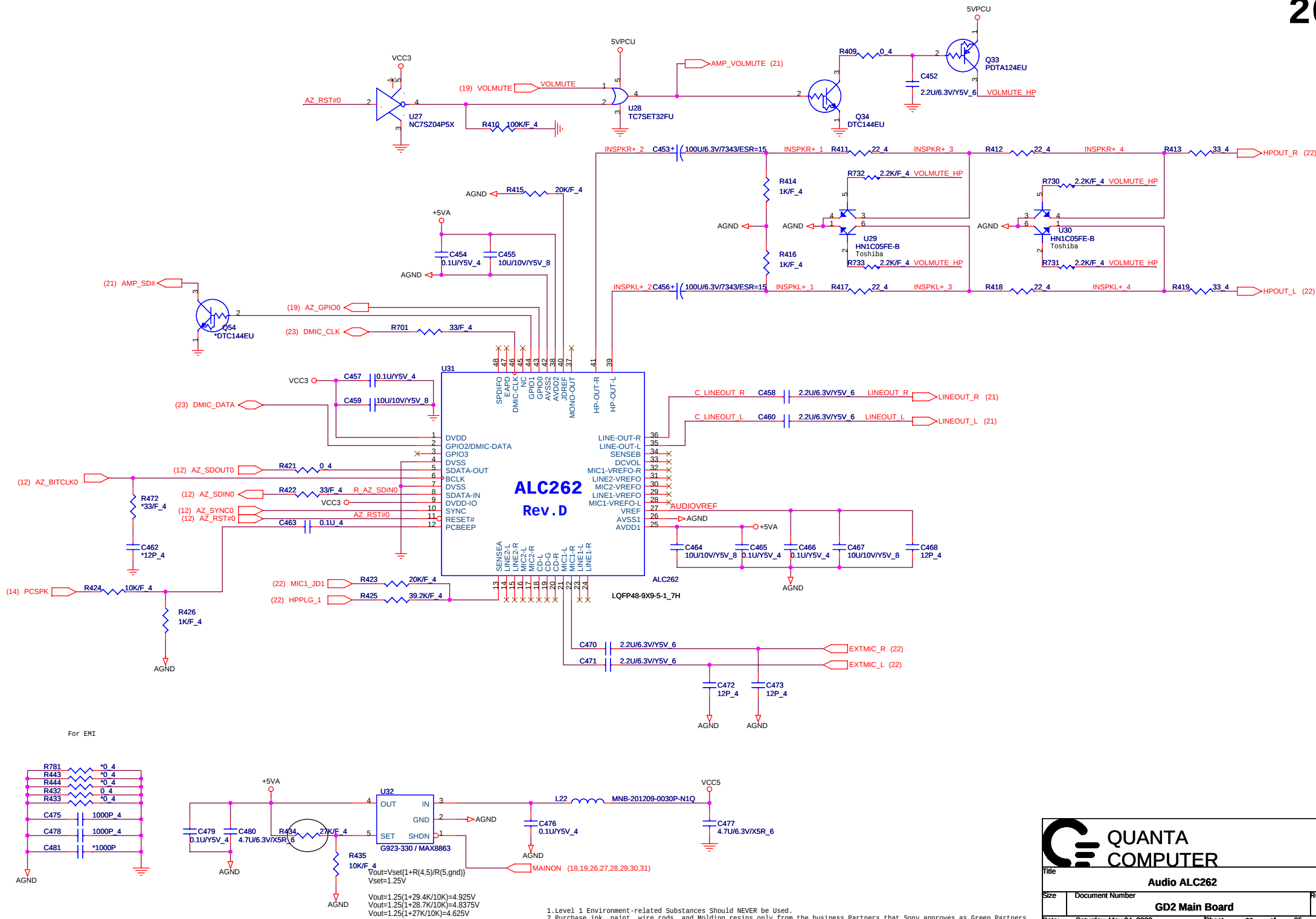
WPC8763L & FLASH

GD2 Main Board

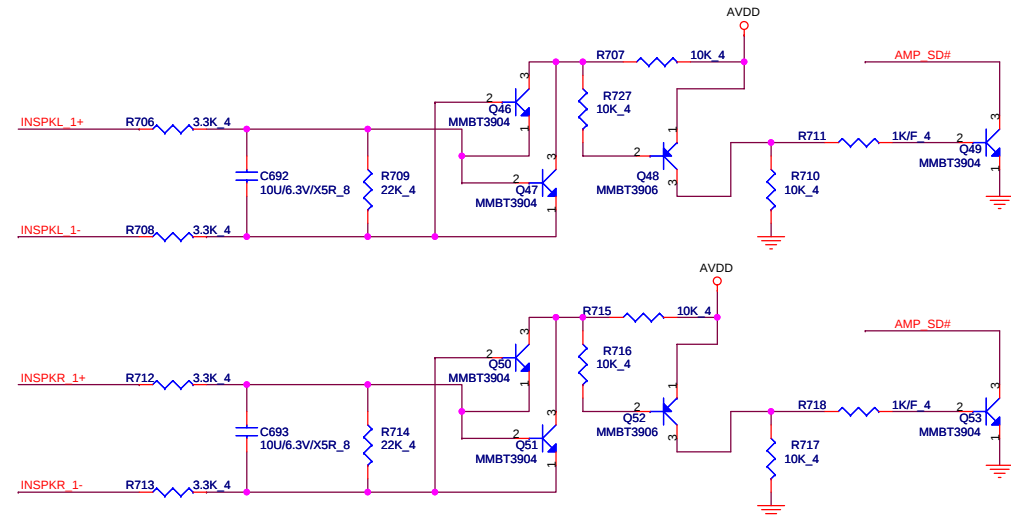
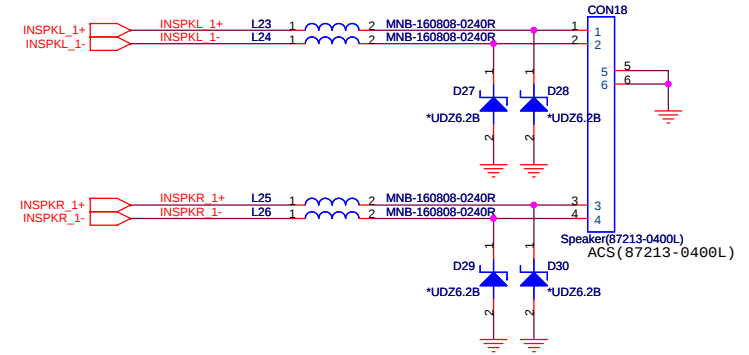
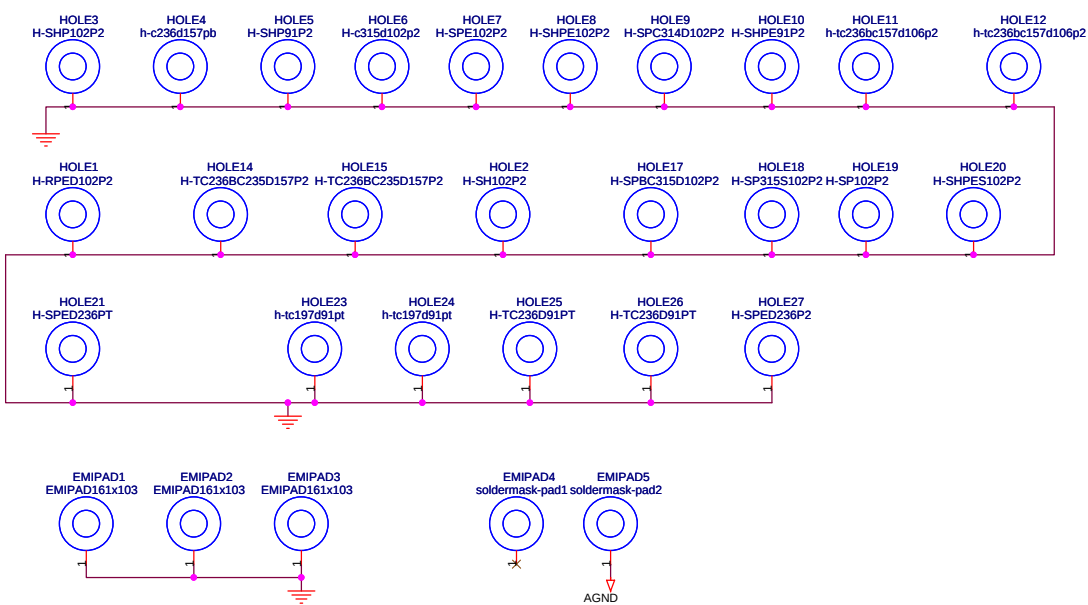
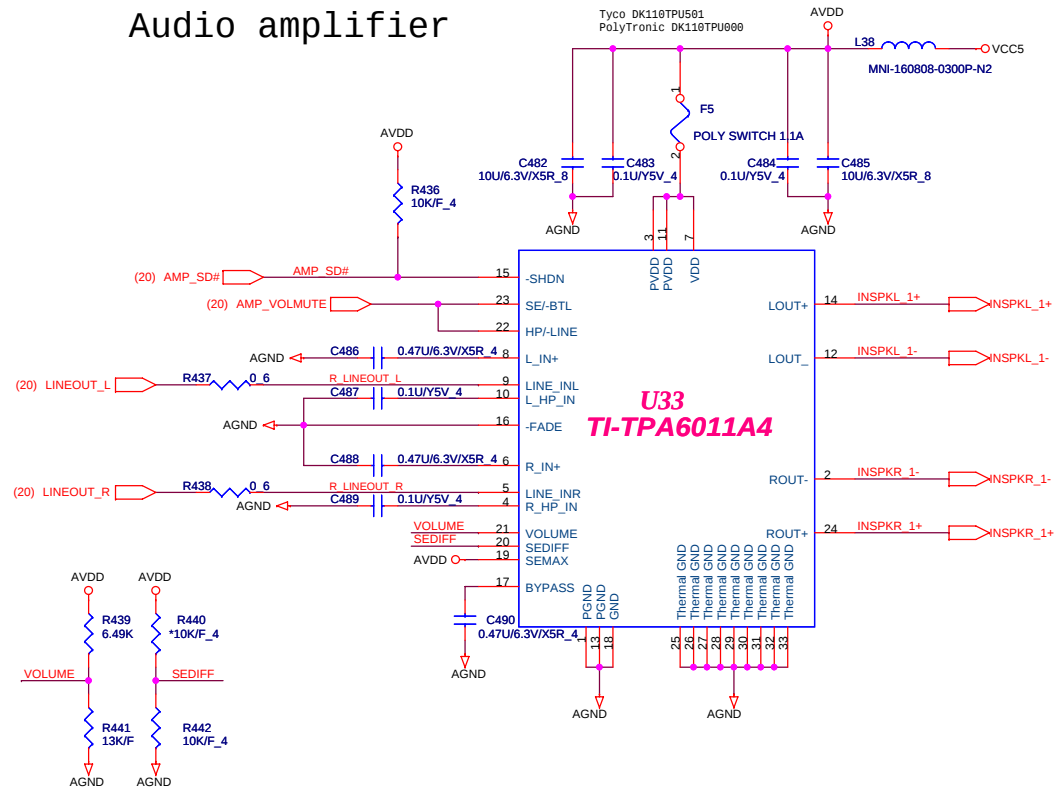
Size: Document Number: Rev 3A

Date: Saturday, May 24, 2008 Sheet 19 of 35

1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

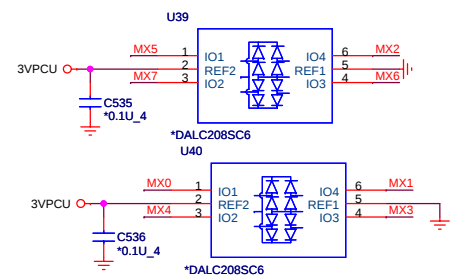
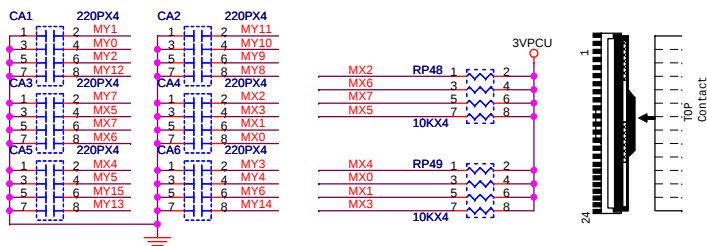
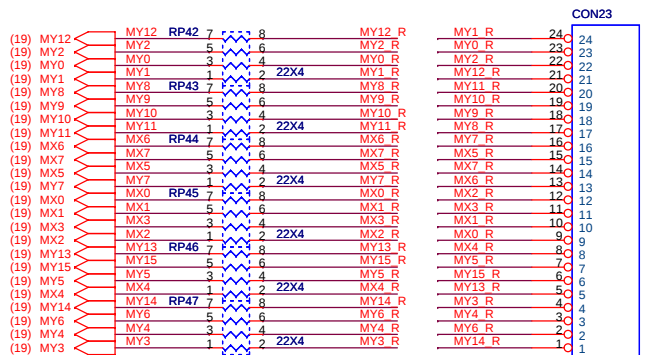


Audio amplifier

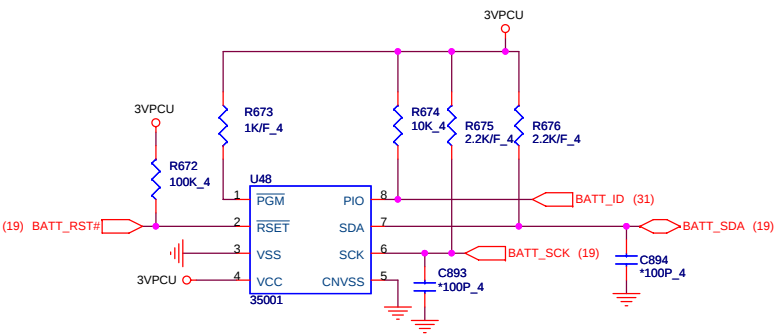
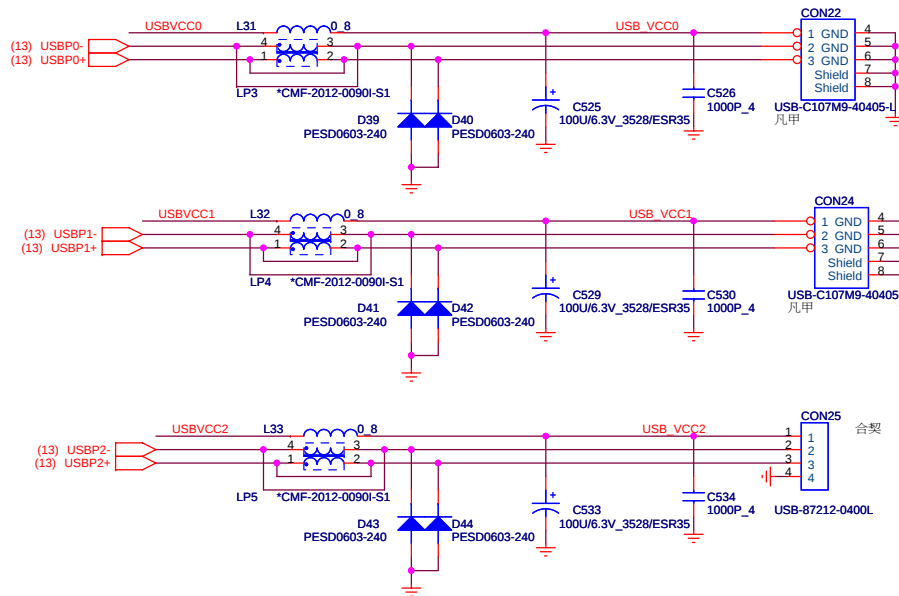
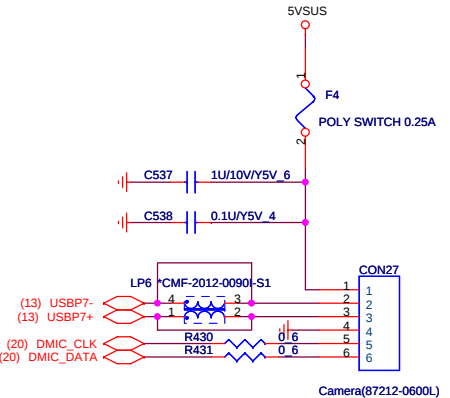


Title			Audio AMP & Int. Speaker
Size			Document Number
Date			Saturday, May 24, 2008
Sheet			21 of 35
Rev			3A

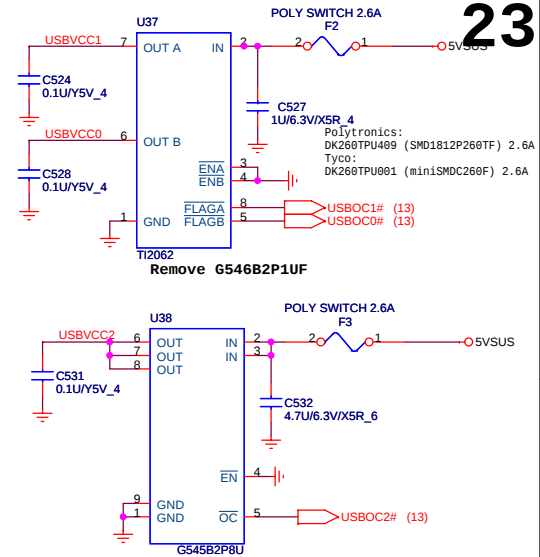
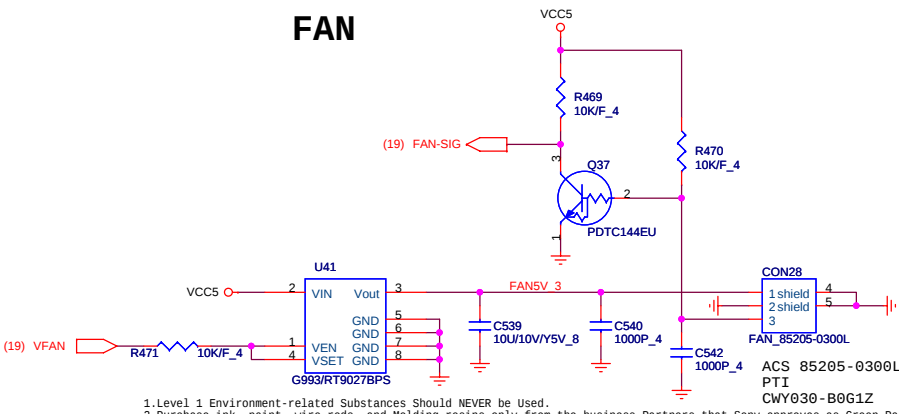
KEYBOARD



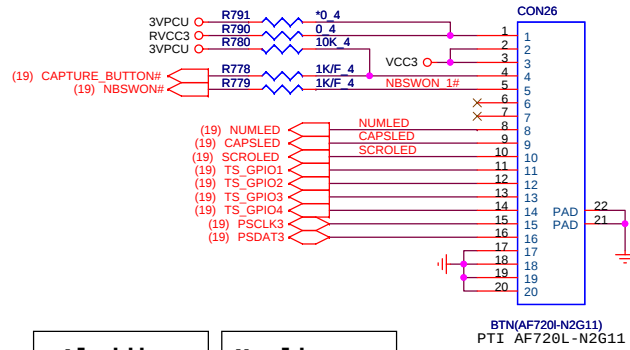
USB Camera



FAN



Power SW BOARD



Aladdin :

VCC3
PSCLK3
PSDAT3
TS_GPIO3
TS_GPIO4
GND

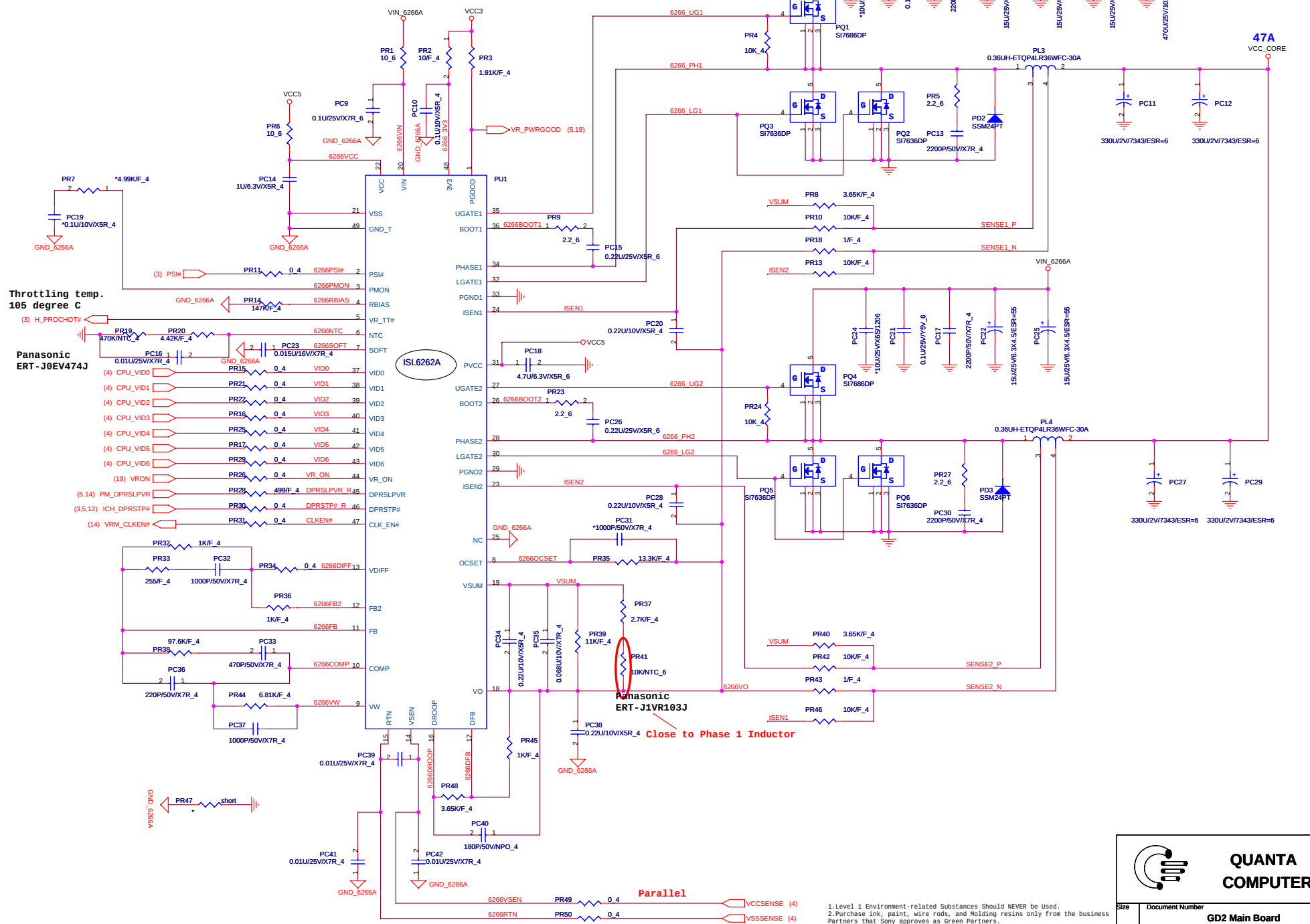
Merlin:

RVCC3
TS_GPIO1
TS_GPIO2
GND

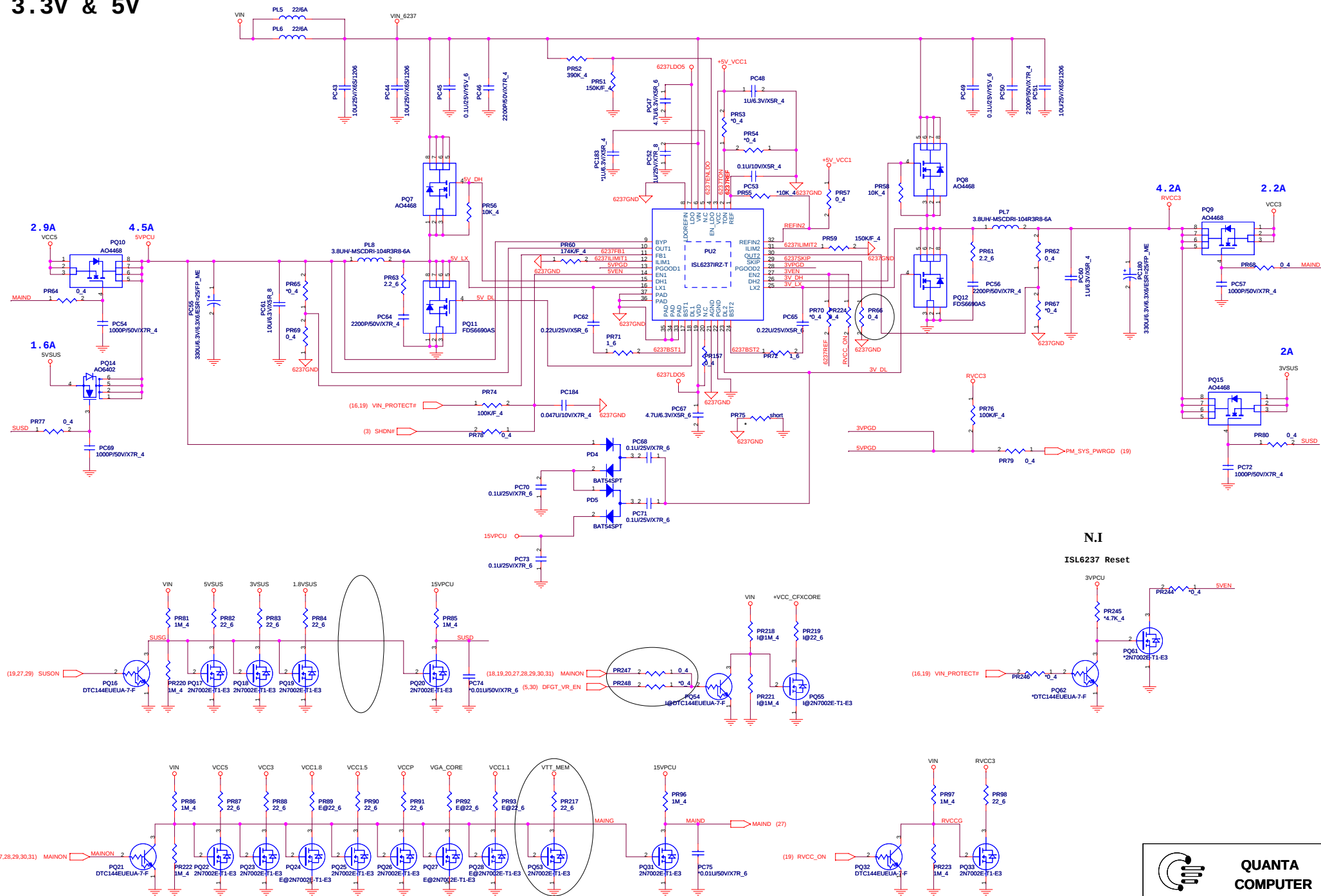


Title		K/B ,USB	
Size	Document Number	Rev 3A	
G02 Main Board			
Date:	Saturday, May 24, 2008	Sheet	23 of 35

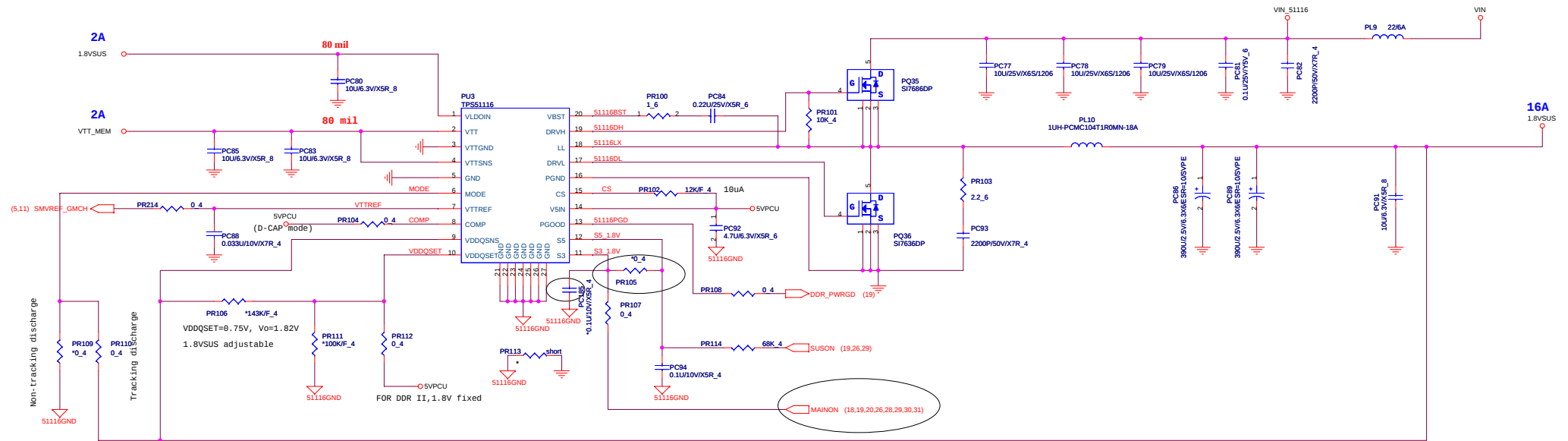
CPU_CORE



3.3V & 5V



1.8VSUS & VTT_MEM

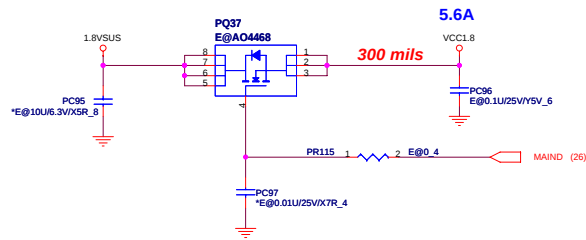


MODE	DISCHARGE MODE
+5V	No discharge
+1.8V	Tracking discharge
GND	Non-tracking discharge

VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	2.5 fixed	VDDQSNS/2	DDR
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

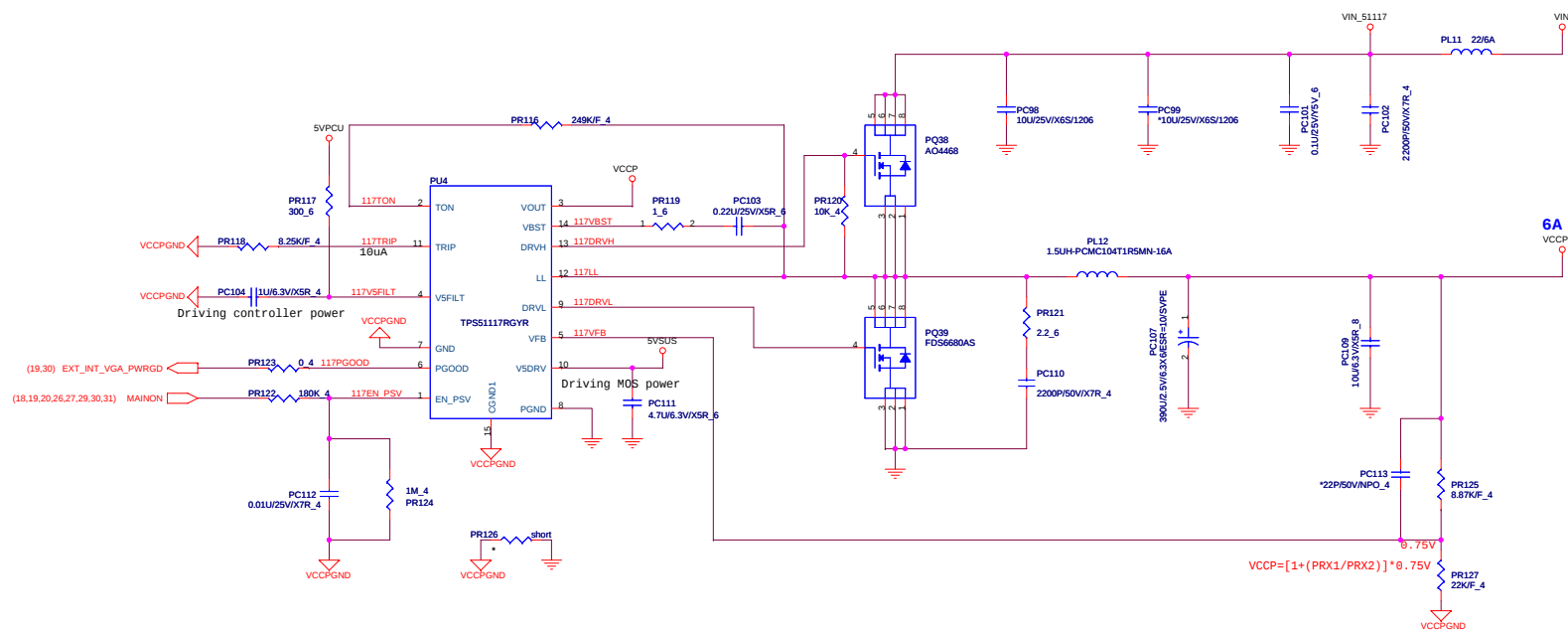
$$V_{TT} = V_{TTREF} = V_{DDQSN}/2 = 0.9V$$

STATE	S3	S5	1.8VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off

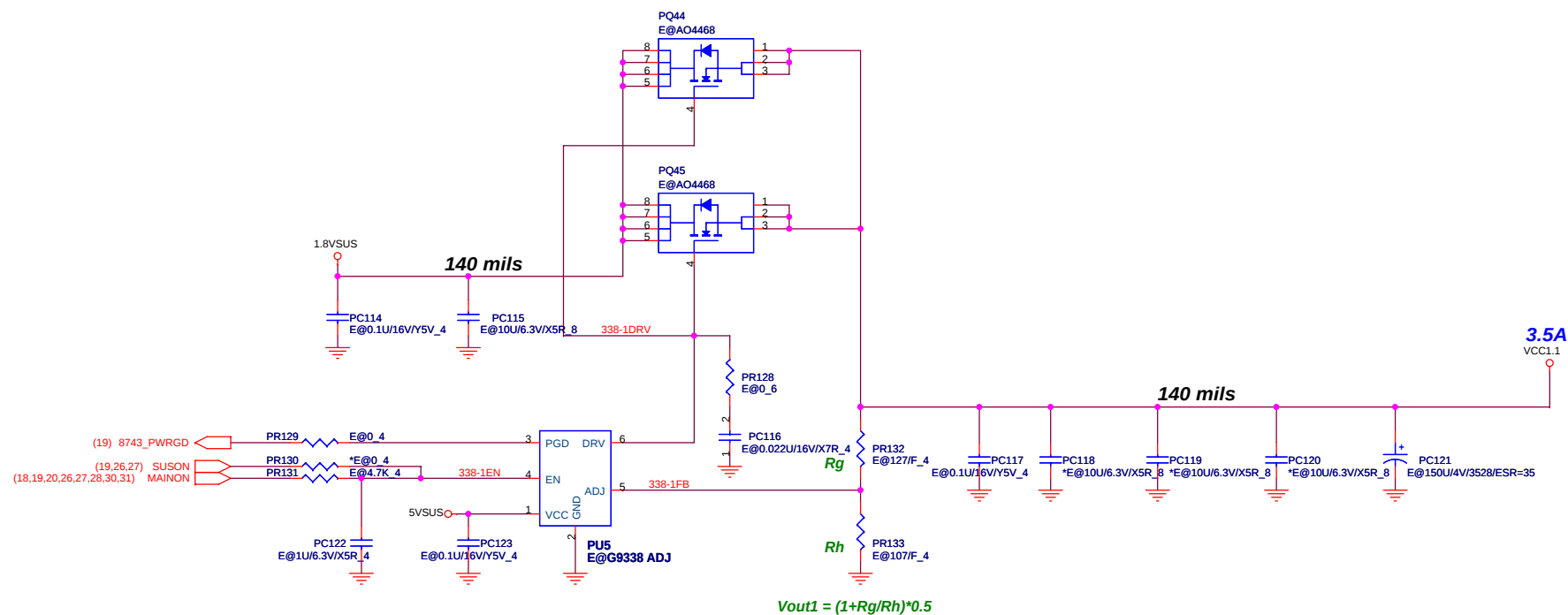


**QUANTA
COMPUTER**

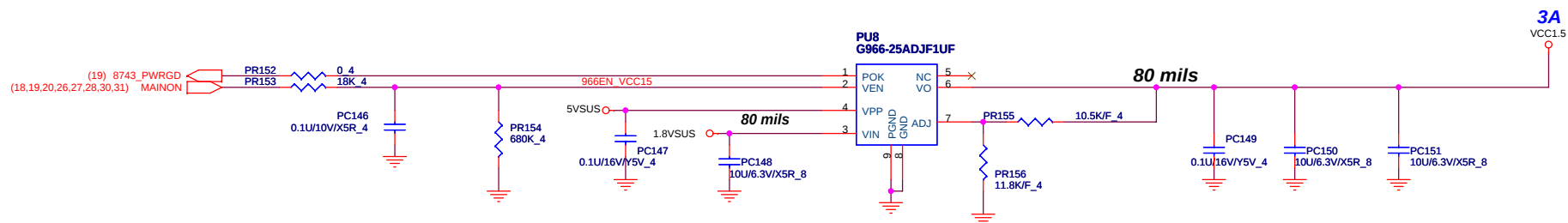
VCCP



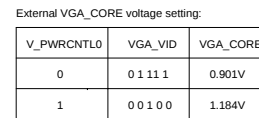
VCC1.1

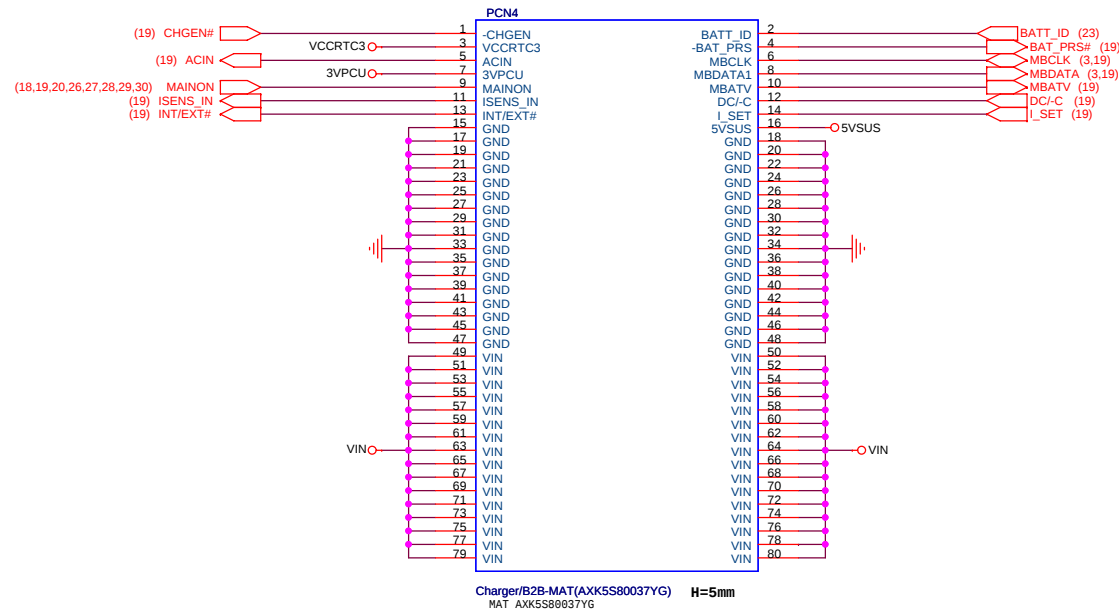


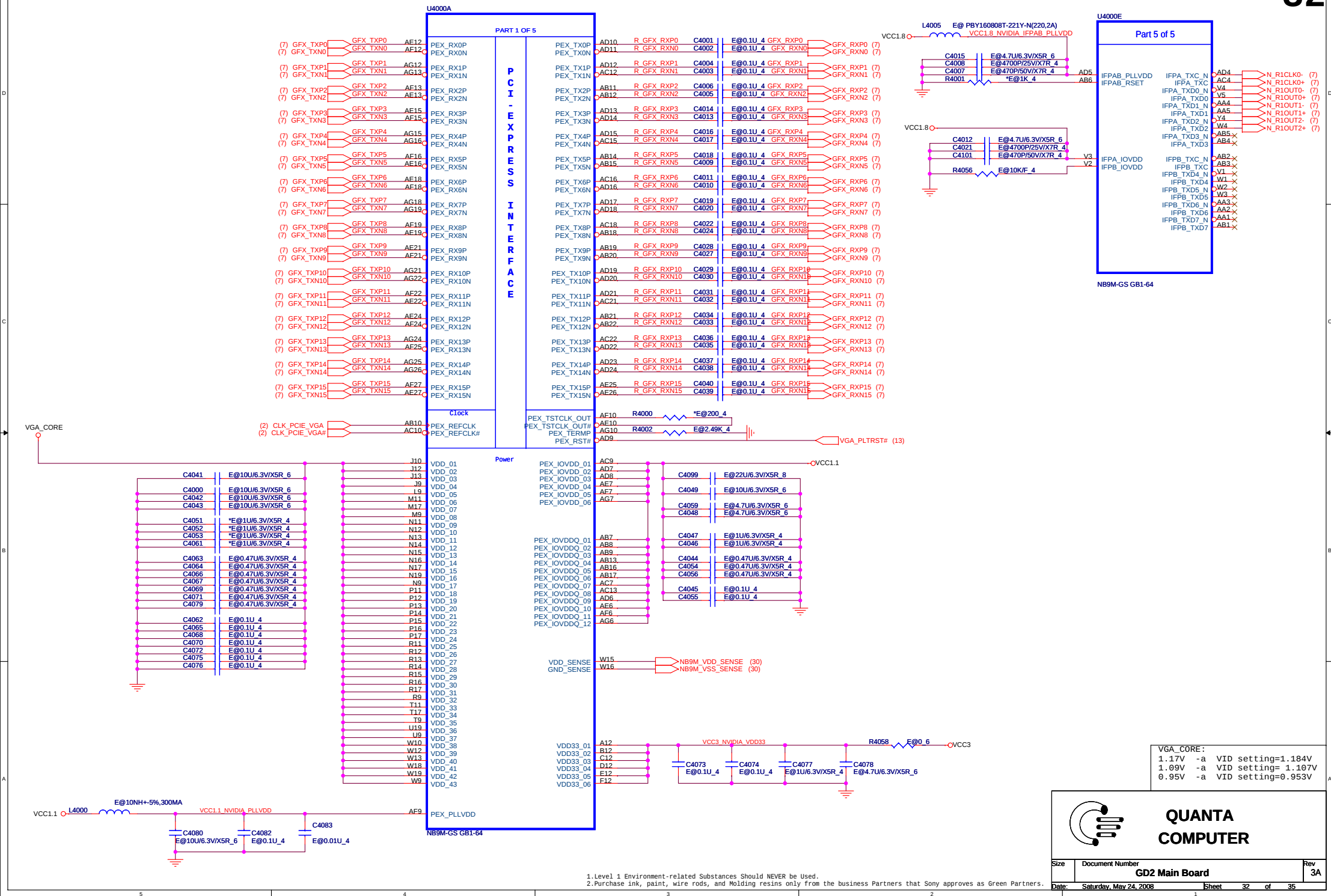
VCC1.5



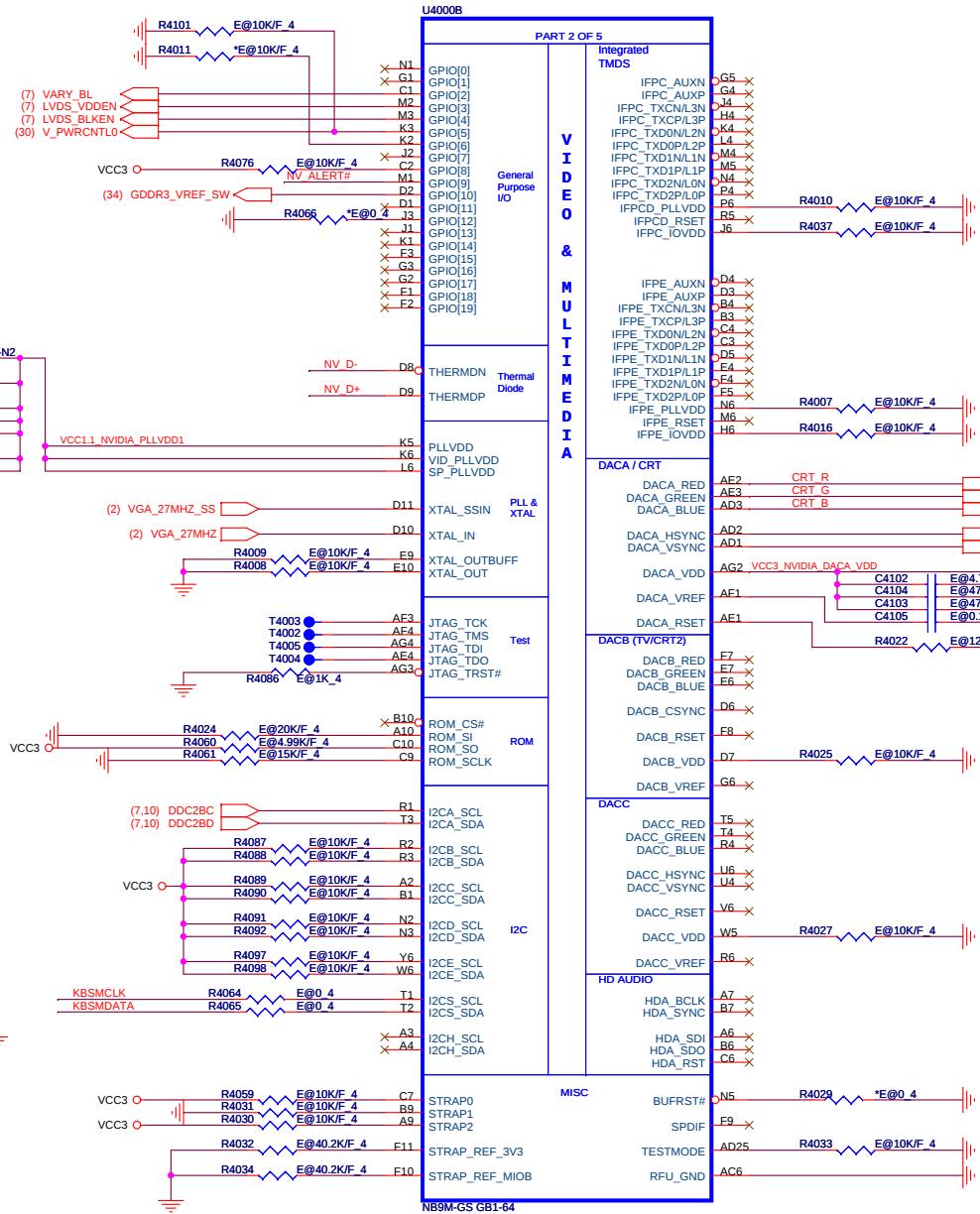
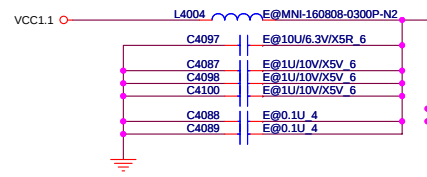
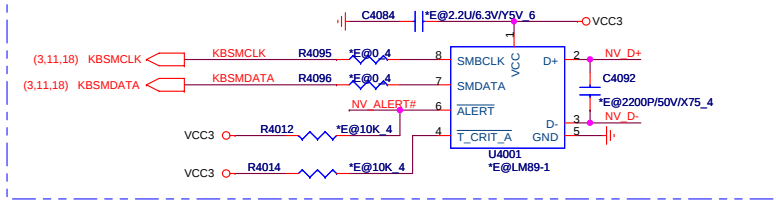
**QUANTA
COMPUTER**







NB9M-GS Thermal Sensor



Logical Strap Bit Mapping

Resistor Value	Pull to VDD	Pull to GND
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Strap Bit Define

Straps	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_S0	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

VRAM Strap:ROM_SI ; RAMCFG[x]

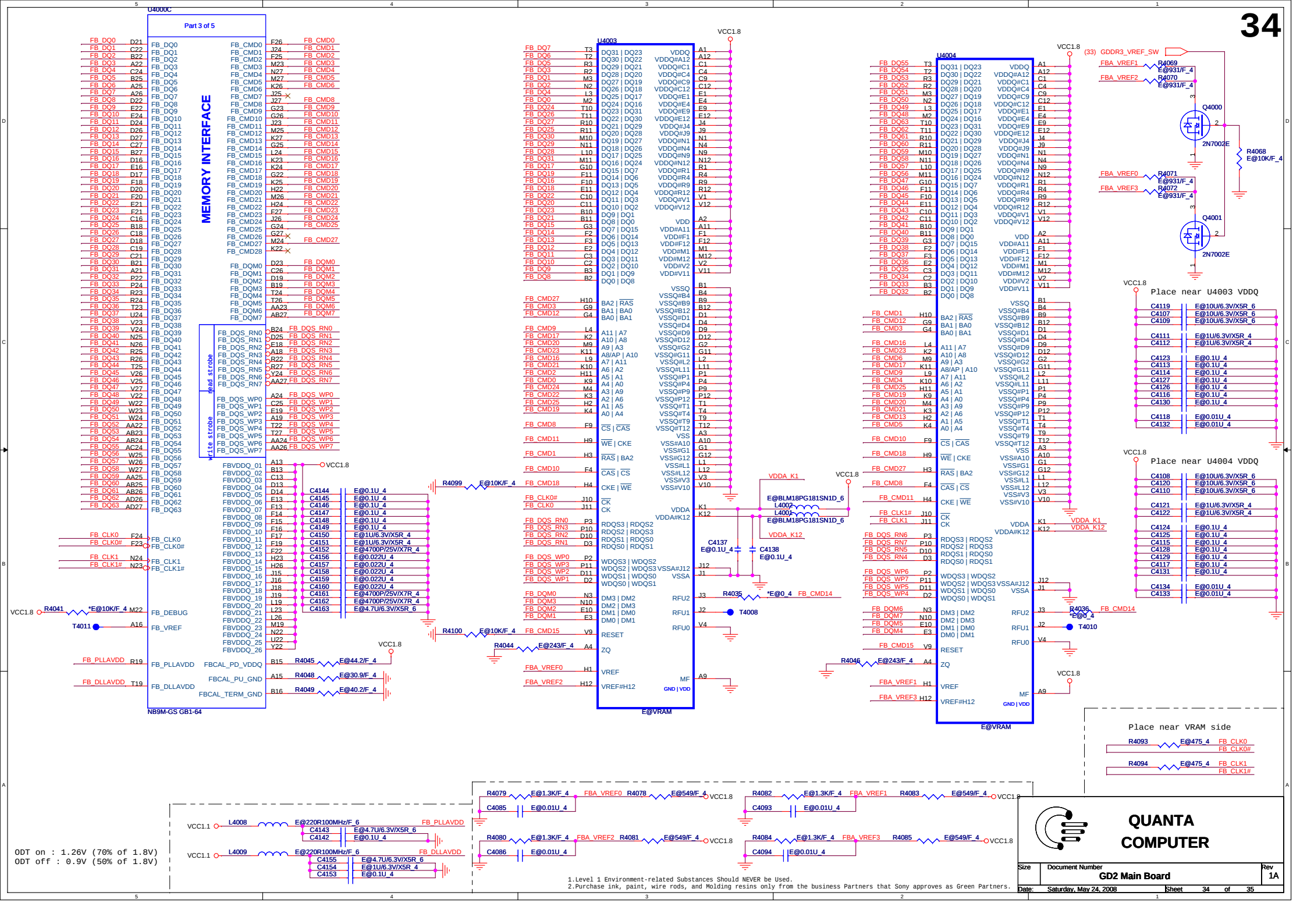
VRAM Vender	ID	R4024
Infineon	0001	PD 10K
Hynix	0010	PD 15K
Samsung	0011	PD 20K

1.Level 1 Environment-related Substances should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



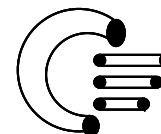
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* Delete RP1, RP2, RP3, RP6, RP7, RP9, RP10, RP11. (P2)
* Delete R56(P3)
* Delete R69(P4)
* Delete R726, R725(P7)

* R789 change value to E@40.2F/I@42.2F.(P10)
* R788 change value to 42.2F.(P10)
* Delete R516, R517(P17)
* U20 pin 7 pull low.(P17)
* C731, C732 change from 0805 to 1206(P18)
* CON14 change to BtB connector.(easy for ASSY)(P18)
* Add D11(P18)
* Change net BSW to BSW# (P18)
* Change net BSW to BSW# (P19)
* R434 change value from 28.7K/F to 27K/F.(P20)
* Add PR66 to enable "Skip" mode for 3V/5V. (P26)
* Change P053 pin2 from SUSG to MAING. (P26)
* Change PR107 connection to MAINON / reserve PR105, PC185. (P27)



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