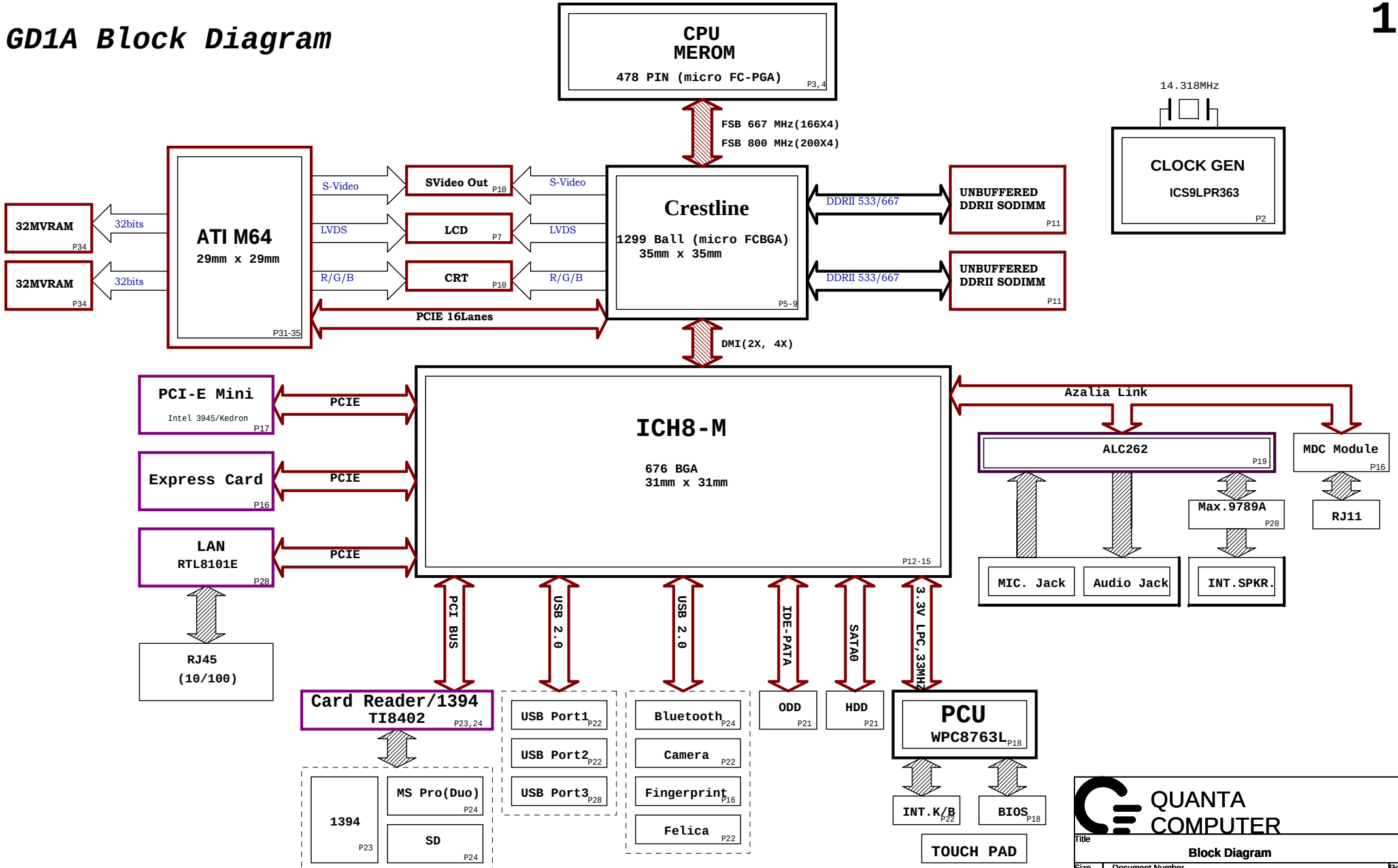
GD1A Block Diagram



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: Block Diagram		
Size: B	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007	Sheet 1 of 35	

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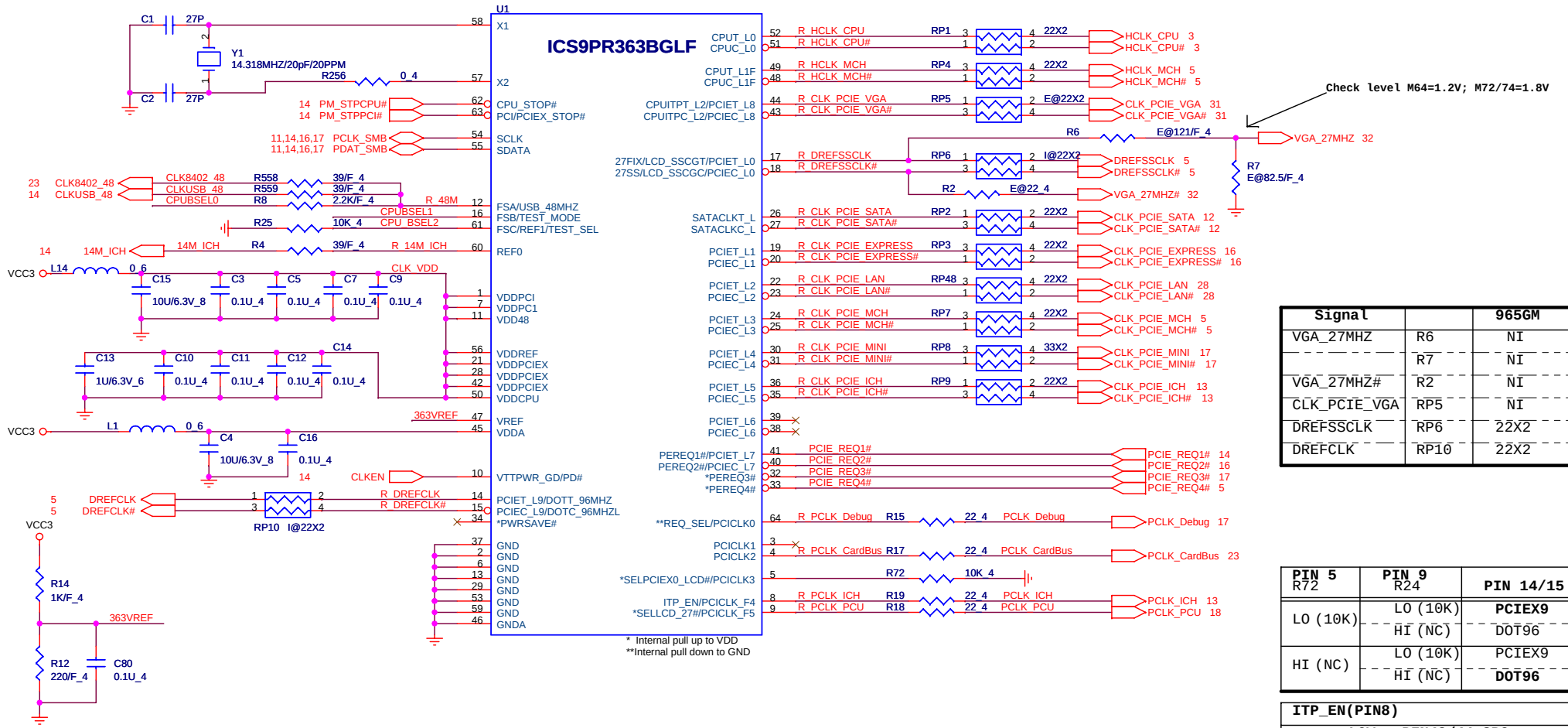

Signal		965GM	965PM
VGA_27MHZ	R6	NI	121
	R7	NI	71.5
VGA_27MHZ#	R2	NI	22
CLK_PCIE_VGA	RP5	NI	22X2
DREFSSCLK	RP6	22X2	NI
DREFCLK	RP10	22X2	NI

PIN 5 R72	PIN 9 R24	PIN 14/15	PIN 17/18
LO (10K)	LO (10K)	PCIEX9	27MHZ
	HI (NC)	DOT96	LCD
HI (NC)	LO (10K)	PCIEX9	PCIEX0
	HI (NC)	DOT96	PCIEX0

ITP_EN(PIN8)
LOW : PIN43/44 SRC
HIGH : PIN43,44 CPUITP

PCIE_REQ1#	PCIE_L0	PCIE_L6	
PCIE_REQ2#	PCIE_L1	PCIE_L8	
PCIE_REQ3#	PCIE_L2	PCIE_L4	
PCIE_REQ4#	PCIE_L3	PCIE_L5	PCIE_L7

FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
* 0	1	0	**200.00**	100	33.33	14.318	48	96	0.5 Down
0	1	1	166.66	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	200.00	100	33.33	14.318	48	96	0.5 Down

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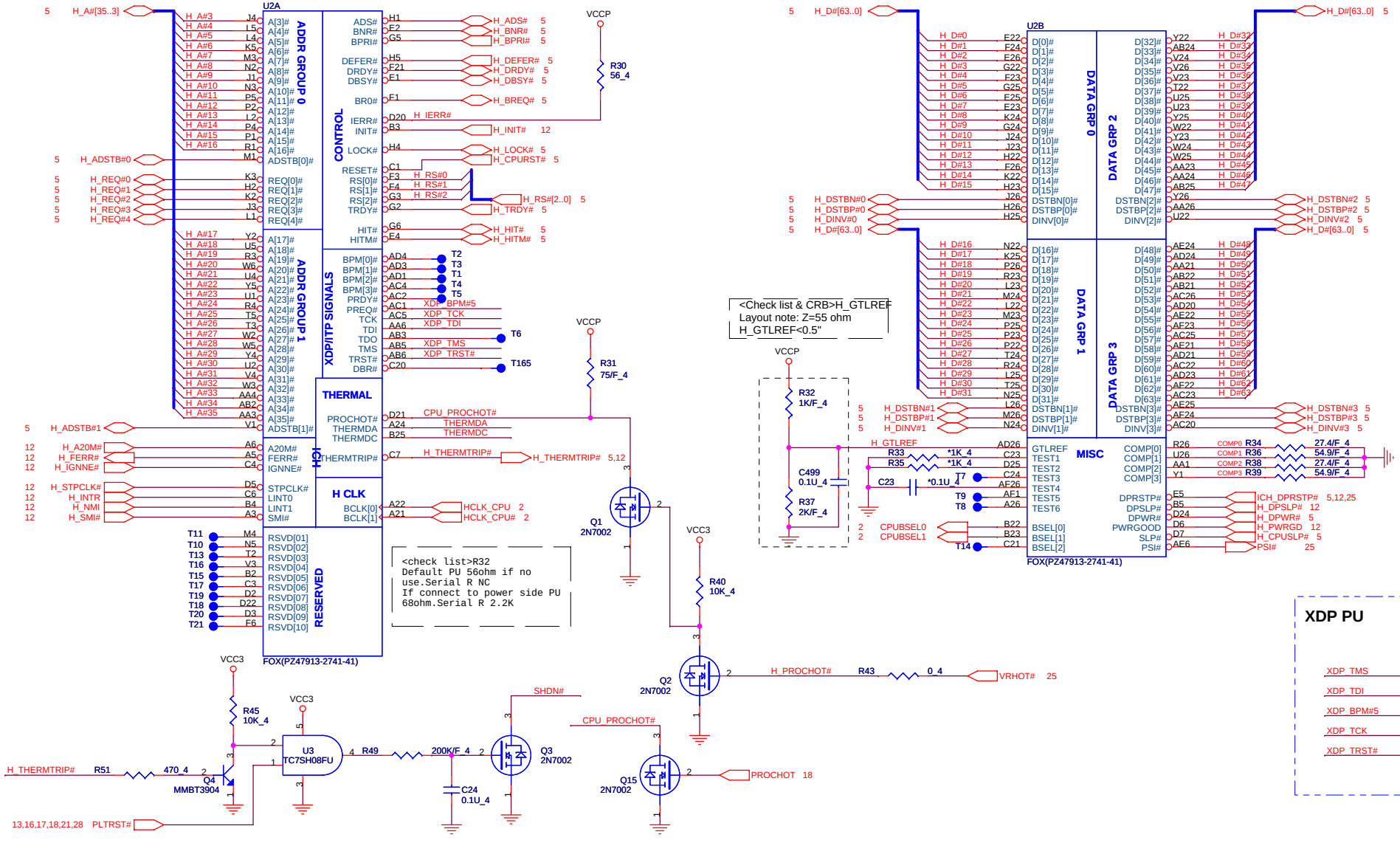
QUANTA COMPUTER

Title	CLOCK GENERATOR	
Size B	Document Number GD1A Main Board	Rev 2A
Date: Monday, July 23, 2007	Sheet 2 of 35	



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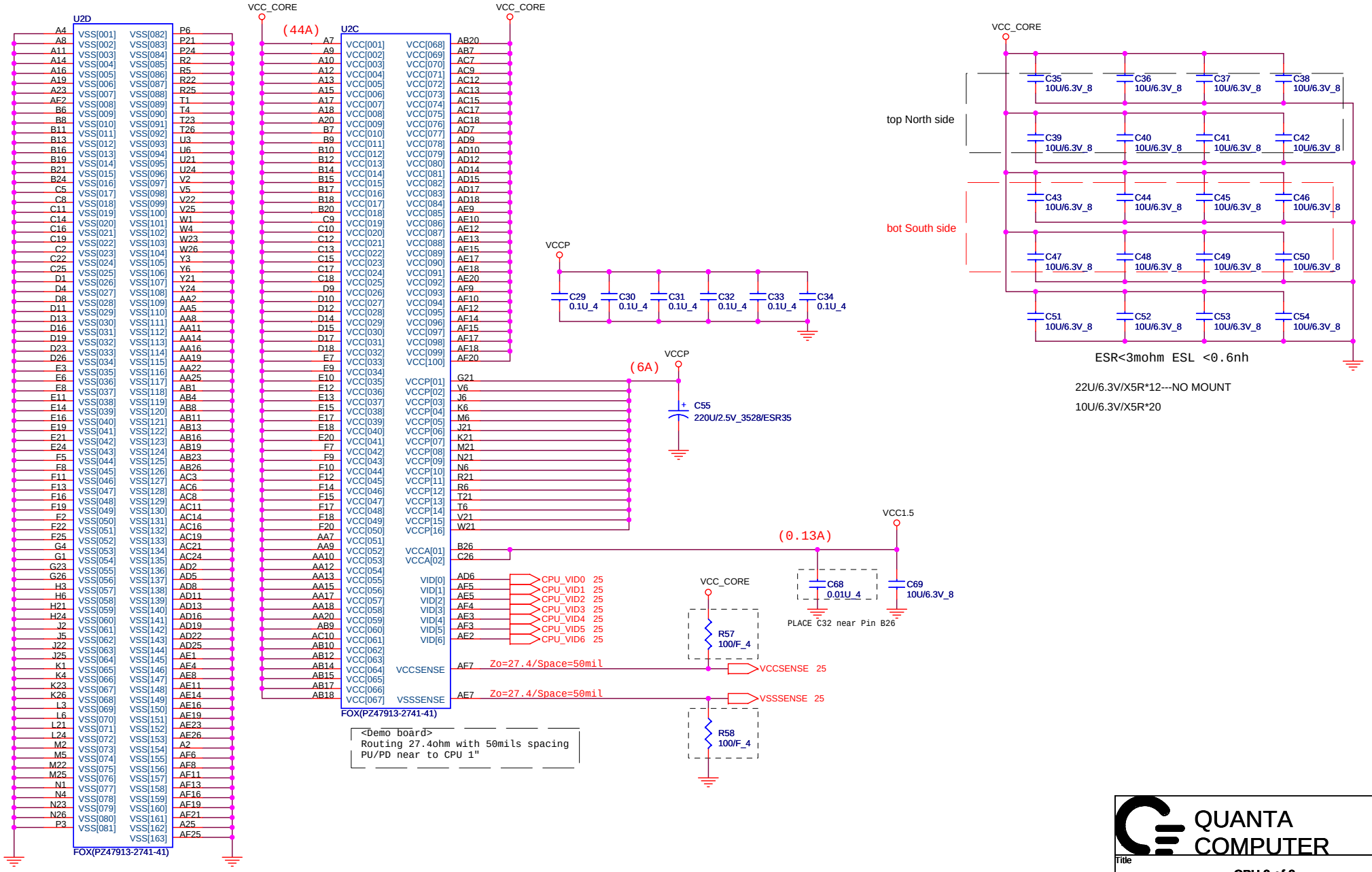
QUANTA COMPUTER

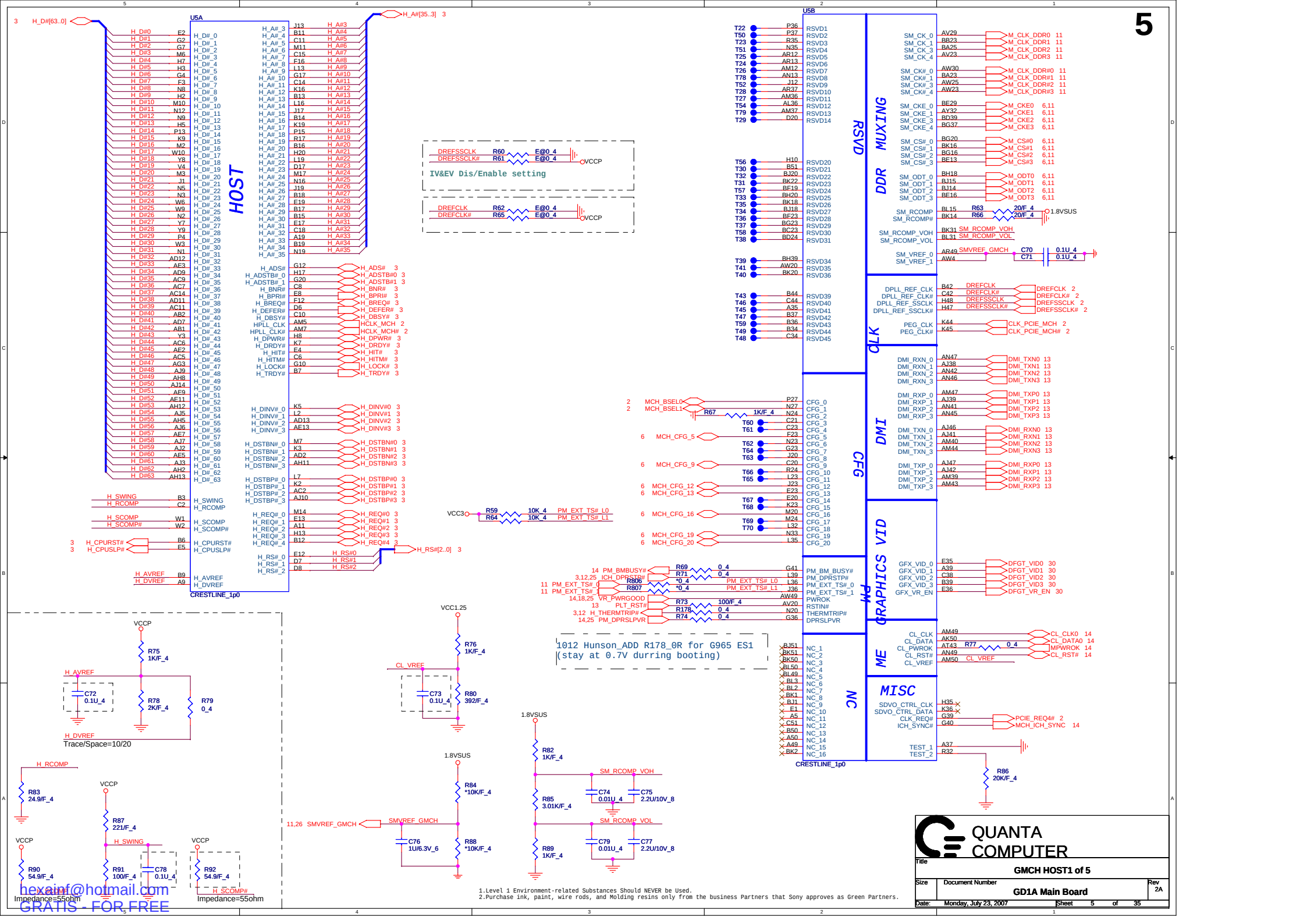
Title	CPU1 of 2	
Size	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007	Sheet 3 of 35	



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: CPU 2 of 2		
Size: B	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007	Sheet 4 of 35	



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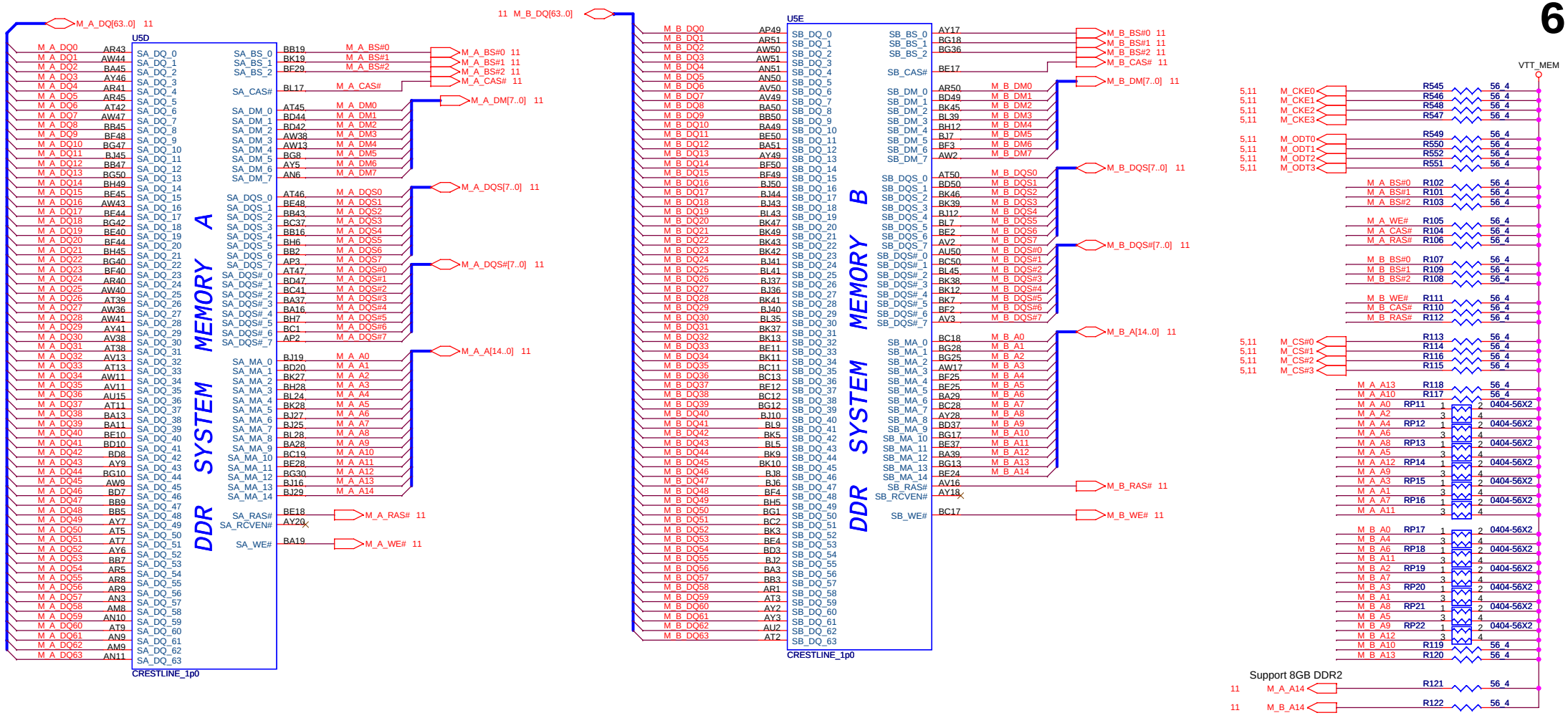


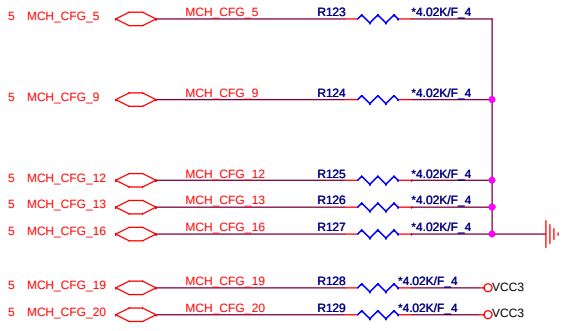
GMCH Strap pin description

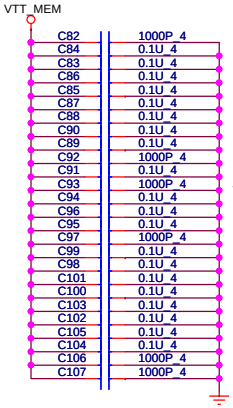
	Low	High
CGF5	DMIx2	* DMIx4
CGF6	RSVD for 945GMS	
CGF7	RSVD	* CPU type: Mobile CPU
CGF9	PCIE Graphics lan : Reverse Lane	* PCIE Graphics lan : Normal operation
CGF10	reserved	
CGF11	reserved	
CGF16	FSB Dynamic ODT Disabled	* FSB Dynamic ODT Enabled
CGF18 *	GMCH core: 1.05V	GMCH core: 1.5V
CGF19 *	DMI LANE Normal	DMI LANE Reversed
CGF20 *	only SDVO or PCIE x1 is operational	SDVO and PCIE x1 are operation simultaneously via the PEG port

CGF[13:12]

00 = Partial clock gating disable
01 = XOR mode enabled
10 = All-Z mode enabled
* 11 = Normal Operation(Default)

int.Pull-down : CFG 18,19,20
Int.Pull-high : CFG CFG 3~17





Place one cap close to every 2 pull-up resistors terminated to VccSus0_9(Total 0.1u x 26)

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2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	GMCH DDR II 2 of 5	
Size	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007	Sheet 6 of 35	

E@: PM965(EXT) should mount
I@: GM965(INT) should mount
@:please refer to form nearly

Signal		GM965	PM965
NB_VSYNC	R158	NI	0_4
	R168	30.1_4	NI
NB_HSYNC	R159	NI	0_4
	R166	30.1_4	NI
GFX	C112, C114~C129, C130~C145	NI	0.1UF_4

Signal		965GM	965PM
NB_B	R160	0_4	NI
	R155	150_4	0_4
NB_G	R161	0_4	NI
	R157	150_4	0_4
NB_R	R162	0_4	NI
	R156	150_4	0_4
L_IBG	R147	2.4K_4	NI
LVDS	RP38 RP41~RP43	0X2	NI
L_BKLT_EN	R170	0_4	NI
L_CTRL_CLK	R130	10K	NI
	RP46	NI	0X4
L_CTRL_DATA	R145	10K	NI
	RP46	NI	0X4
LVDS_VDDEN	R146	0_4	NI
DDC2BC	R163	0_4	NI
	R553	NI	0_4
DDC2BD	R164	0_4	NI
	R554	NI	0_4
CRT_TVO_IREF	R167	1.3K_4	0
L_DDC_CLK	RP46	NI	0X4
L_DDC_DATA	RP46	NI	0X4
BRIGHT	R173	0_4	NI
	R175	NI	0_4

SM Bus PD

CRT_DDC_CLK R553 E@0_4
CRT_DDC_DATA R554 E@0_4
L_CTRL_CLK RP46 E@0X4
L_CTRL_DATA
L_DDC_CLK
L_DDC_DATA

CRT PU/PD

R155 E@0_4 NB_B
R157 E@0_4 NB_G
R156 E@0_4 NB_R
R158 E@0_4 NB_VSYNC
R159 E@0_4 NB_HSYNC

NB LVDS enable

L_VDD_EN R148 I@0_4
31 LVDS_VDDEN
U6 AAT4280IGU-1-T1
R307 100K_4
C108 1U/6.3V_6
C185 0.1U_4
C194 0.1U_4
C184
C182 0.01U_4
4.7U/6.3V_8
0517 Hunson_change from 0.1u to 1u

LVDS

CON1 LVDS-HND(LVC-C30SFYG+)
VIN C802 0.1U/50V_6
L_BKLTCTL R173 I@0_4
31 VARY_BL
DISPON R172 5.6K_4
R174 10K_4

Display On

C770 0.1U_4
32 LVDS_BLKEN
L_BKLT_EN R170 I@0_4
R171 10K_4
14,18 PWROK
U48 TC7SH08FU
18 DISP_ON_EC
C129 0.1U_4
R180 10K_4
U47 TC7SH08FU
R564 *0_4
DISPON

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	GMCH DMI VEDIO 3 of 5	
Size	Document Number: GD1A Main Board	Rev 2A
Date: Monday, July 23, 2007	Sheet 7 of 35	

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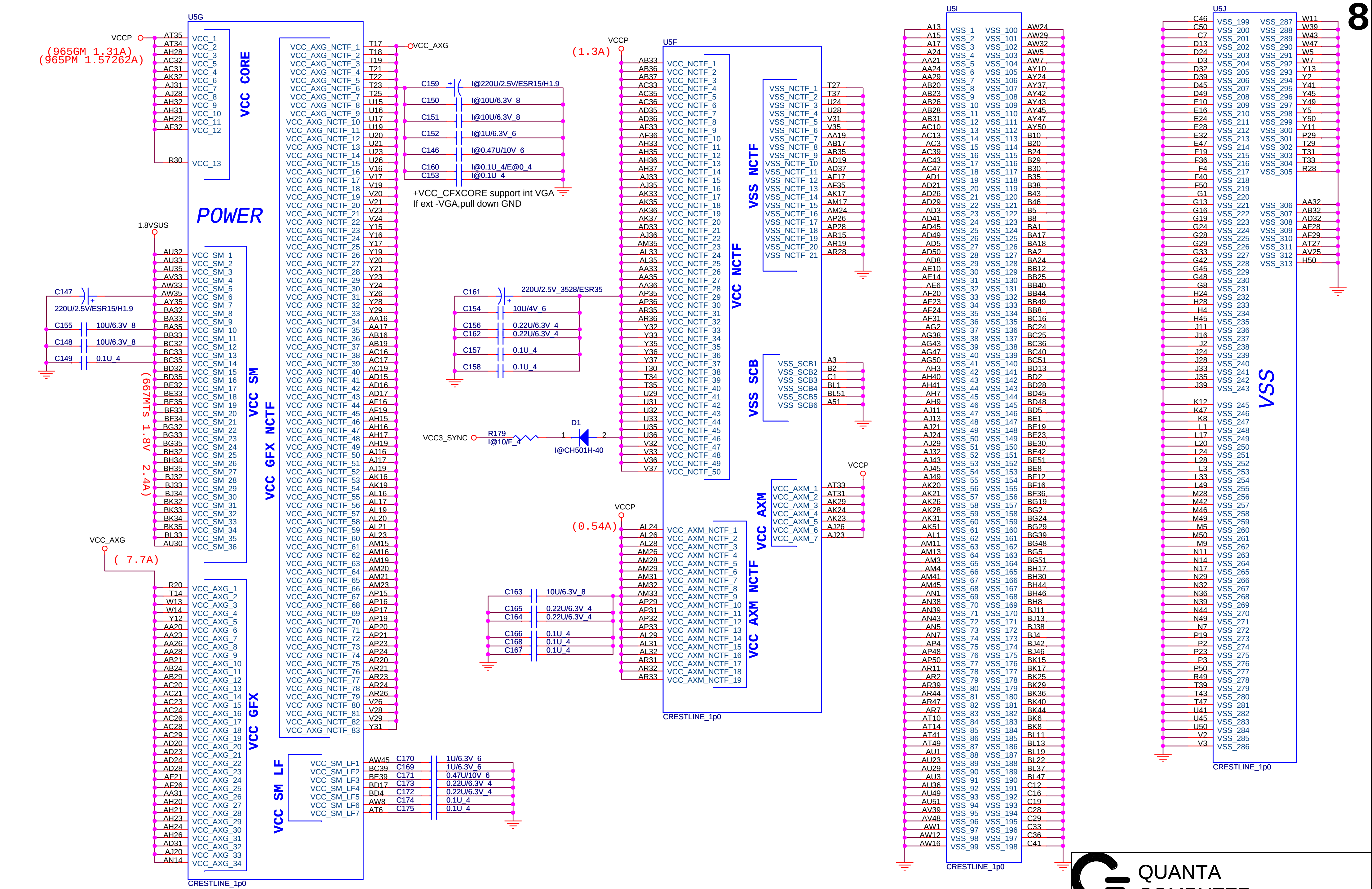

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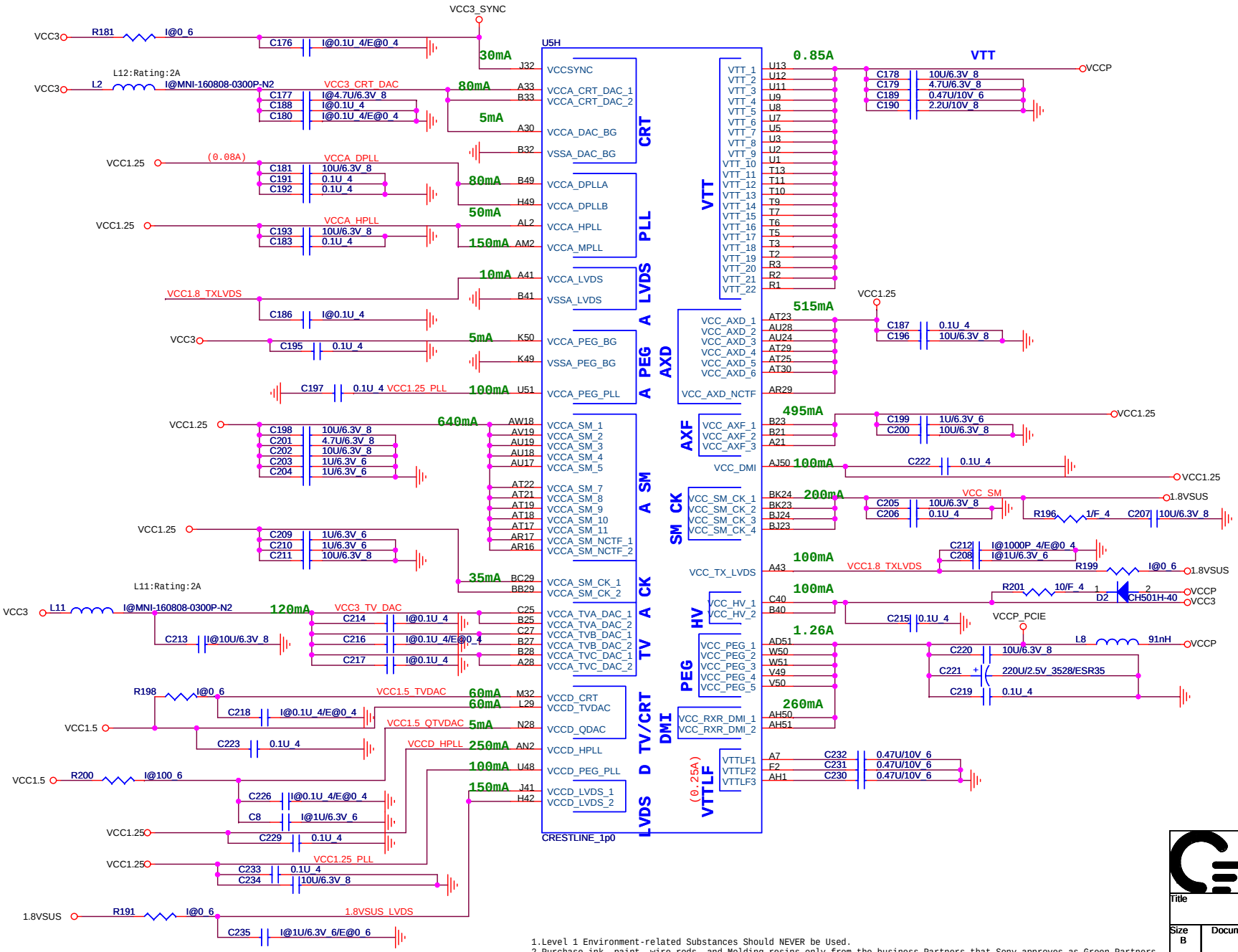
QUANTA COMPUTER

Title	GMCH Power 4 of 5		
Size	Document Number: GD1A Main Board		Rev 2A
Date: Monday, July 23, 2007	Sheet 8 of 35		



Signal		965GM	965PM
VCCA_TV_DAC	L12	V	X
	C244	V	X
	C245	V	X
	C246	V	X
	C248	V	X
	R193	X	V
VCC1.5_TVDAC	L14	V	X
	C250	V	X
	C247	V	X
	R195	X	V
VCC1.5_QTVDAC	L17	V	X
	C257	V	X
	C258	V	X
	R197	X	V

Signal		965GM	965PM
VCCA_DAC_BG	L8	V	X
	C214	V	X
	R181	X	V
VCCSYNC	R177	V	X
	C201	V	X
	C202	V	X
	R178	X	V
VCC3_CRT_DAC	L7	V	X
	C203	V	X
	C211	V	X
	R179	X	V
VCCD_LVDS	R198	V	X
	C265	V	X
	C264	V	X
	R199	X	V
VCCA_LVDS	R183	0_4	NC
	C208	0.01u_4	NC
	C209	0.1u_4	NC
	R184	NC	0_4
VCC_TX_LVDS	R192	V	X
	C240	V	X
	C238	V	X
	R191	X	V

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QUANTA COMPUTER

Title	GMCH Power 2 5 of 5	
Size B	Document Number GD1A Main Board	Rev 2A
Date: Monday, July 23, 2007	Sheet 9 of 35	

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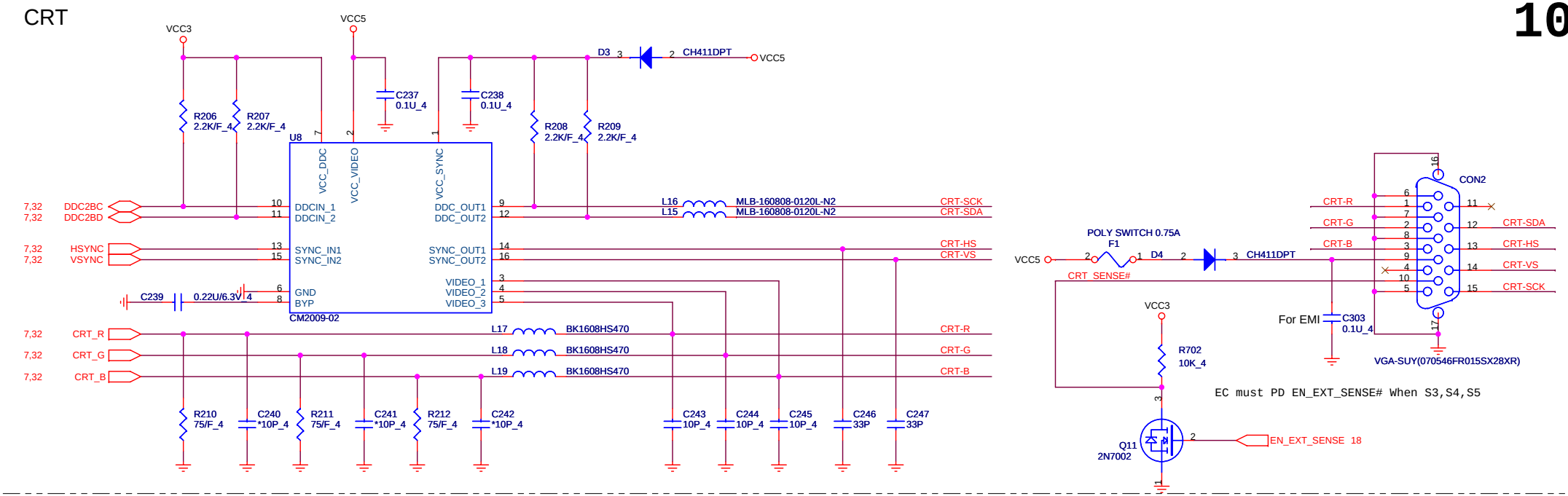
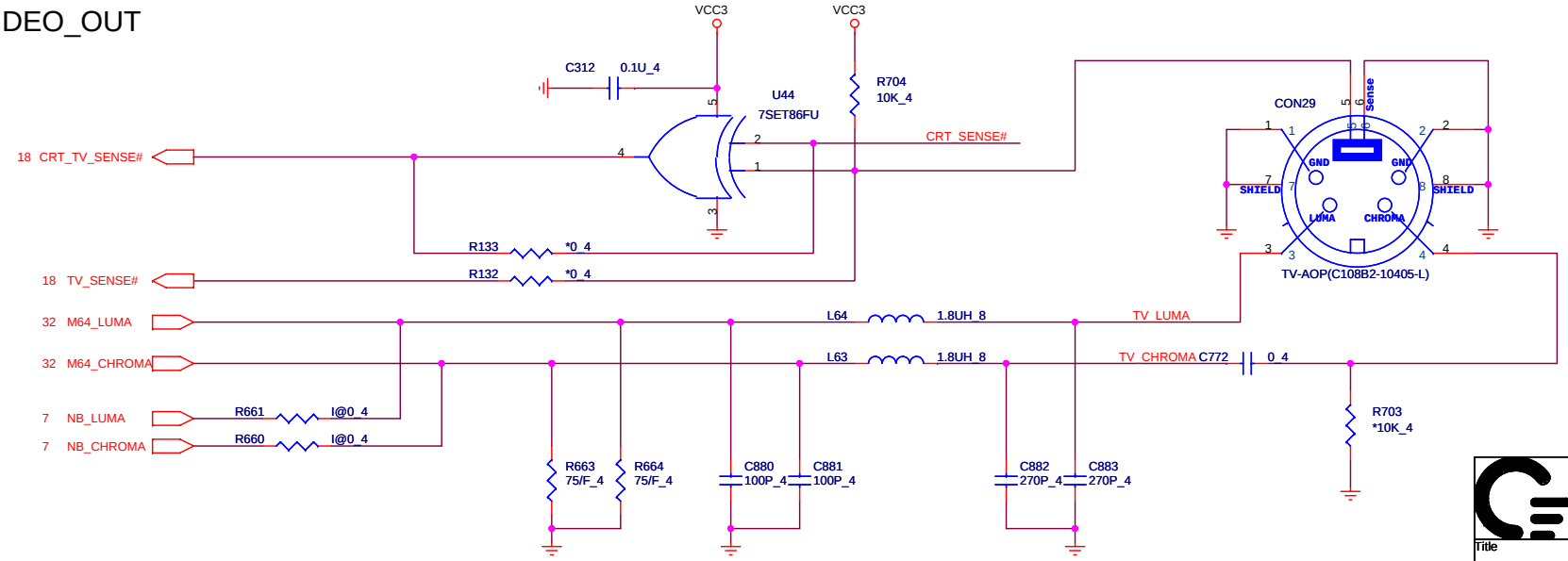
CRT



S-VIDEO_OUT



1.Level 1 Environment-related Substances Should NEVER be Used.
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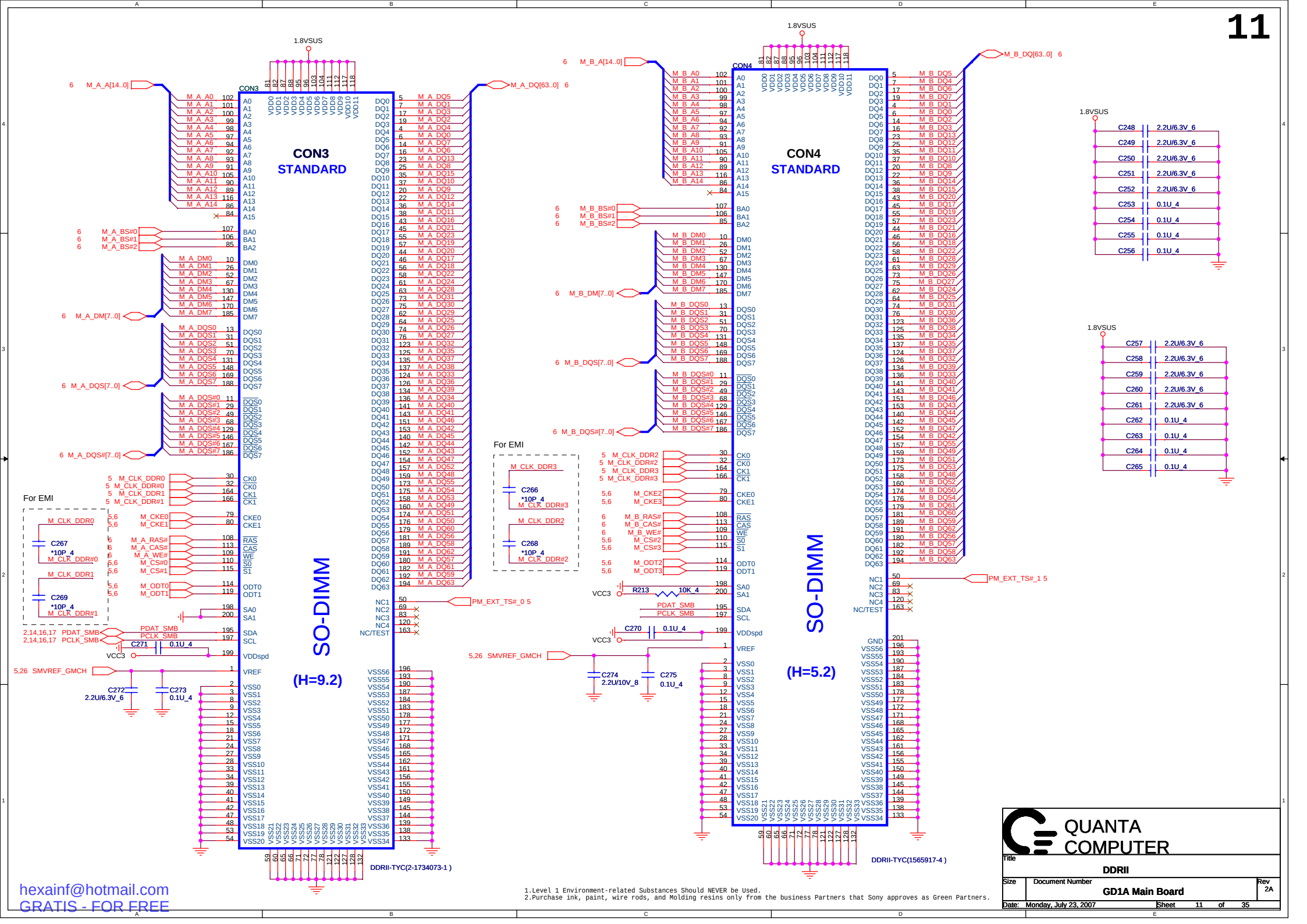
QUANTA COMPUTER

Title: CRT & S-VIDEO		
Size: B	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007	Sheet 10 of 35	



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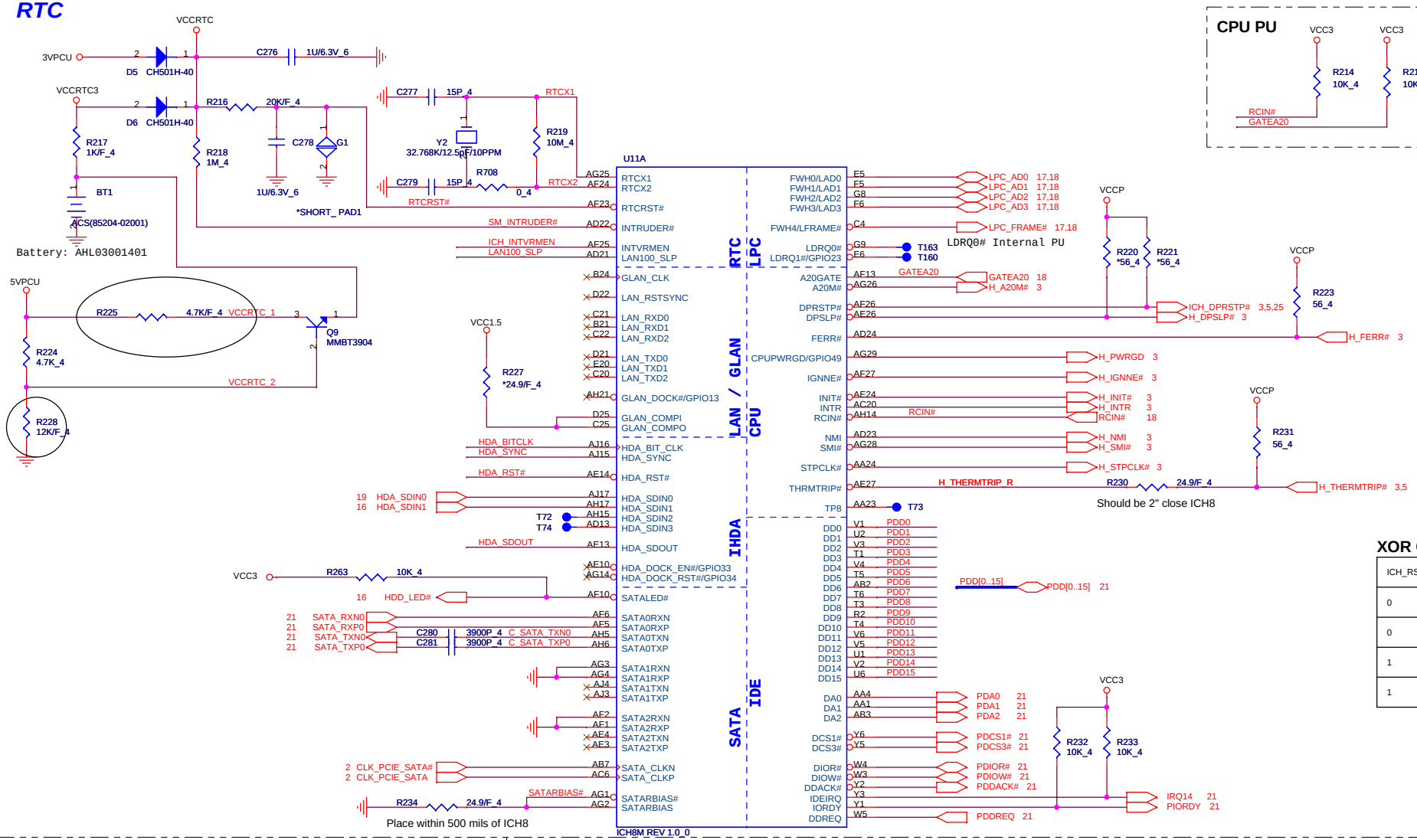
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	DDRII	
Size	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007	Sheet 11 of 35	

RTC



CPU PU

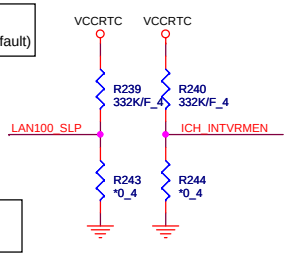
XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

ICH8 strap

ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1.05)

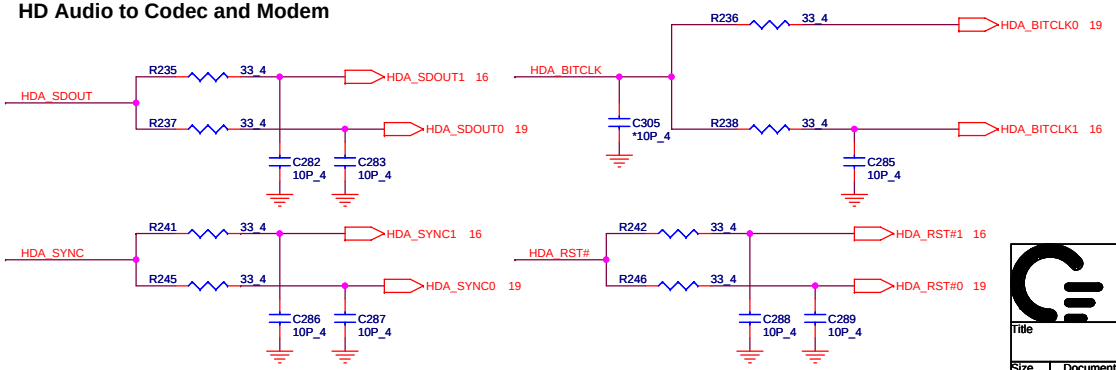
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)



ICH_INTVRMEN	Low = Disable High = Enable(Default)

ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

HD Audio to Codec and Modem



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QUANTA COMPUTER

Title	ICH8-M HOST 1 of 4	
Size	Document Number: GD1A Main Board	Rev: 3A
Date: Monday, July 23, 2007	Sheet 12 of 35	

WireLess Lan

Express card

10/100 Lan

U11D

PCI-Express Direct Media Interface

SPI

USB

ICH8M REV 1.0_0

USB_PORT

USB_PORT

USB_PORT

Express Card

Finger Print

Blue Tooth

Felica

CAMERA

VCC1.5

R247 24.9/F_4

Within 500 mils

DMI_COMP

R250 22.6/F_4

<CRB>
USB_RBIAS_PN<500mils

U11B

PCI

Interrupt I/F

ICH8M REV 1.0_0

ICH8 internal PU PME# 3Vsus

U12 TC7SH08FU

U13 *E@TC7SH08FU

R255 E@0_4

R182 100K/F

C294 0.1U_4

C295 *E@0.1U_4

PLT_RST# 5

PLTRST# 3,16,17,18,21,28

VGA_PLTRST# 31

1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

PCI bus info.

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
TI8402	AD23	REQ0# / GNT0#	PIRQ E/F/G

A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

PCI_GNT3# R248 *1K_4

ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

PCI_GNT0# R251 *1K_4

SPI_CS1# R249 *1K_4

RP23 10KX8

RP24 10KX8

RP26 10KX8

RP25 10KX8

USBOC8# R253 10K_4

USBOC9# R254 10K_4

Title	ICH8-M PCIE 2 of 4
Size B	Document Number GD1A Main Board
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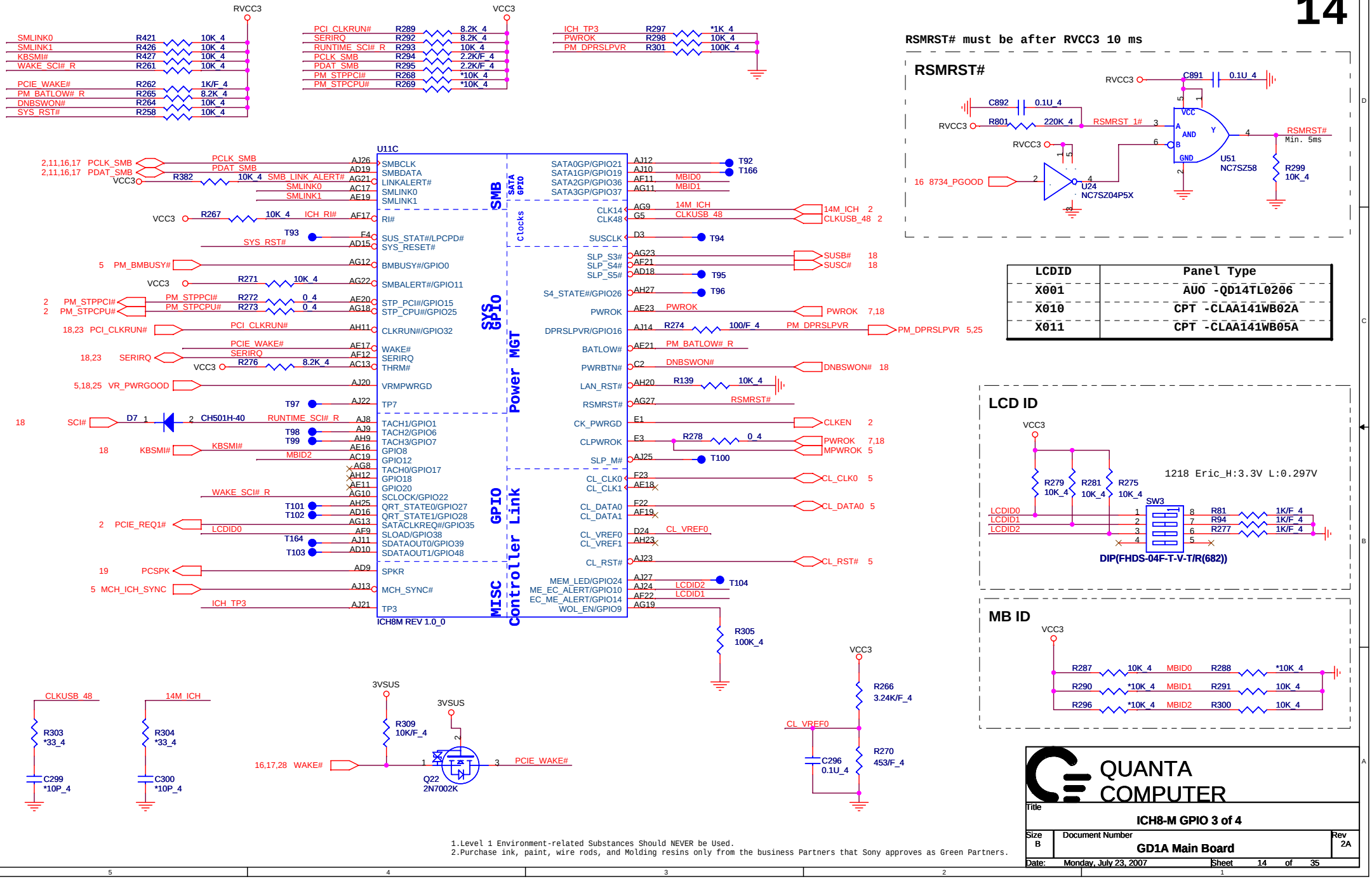

LCDID	Panel Type
X001	AUO -QD14TL0206
X010	CPT -CLAA141WB02A
X011	CPT -CLAA141WB05A

1.Level 1 Environment-related Substances Should NEVER be Used.
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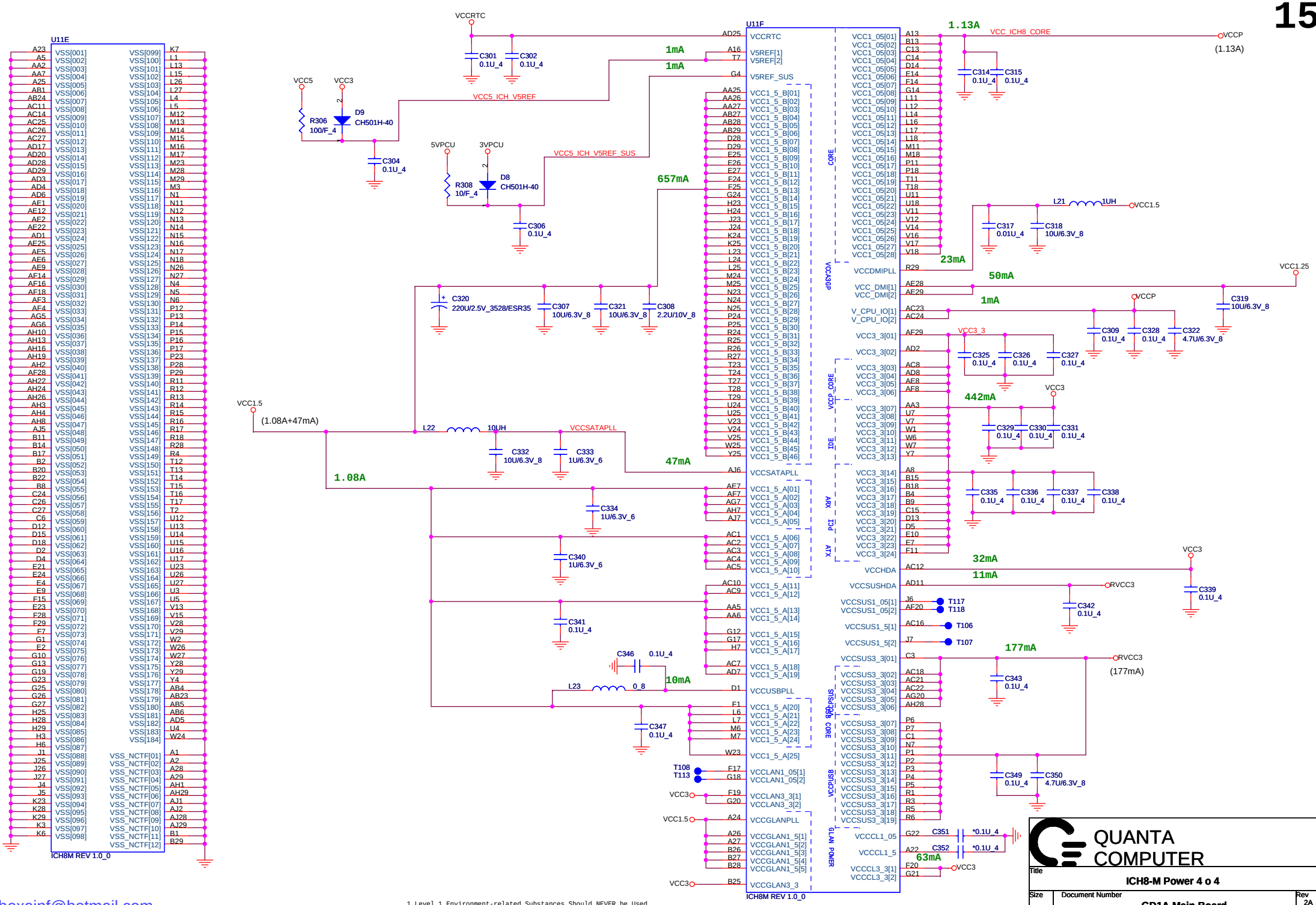
QUANTA COMPUTER

Title	ICH8-M GPIO 3 of 4	
Size B	Document Number GD1A Main Board	Rev 2A
Date: Monday, July 23, 2007	Sheet 14 of 35	



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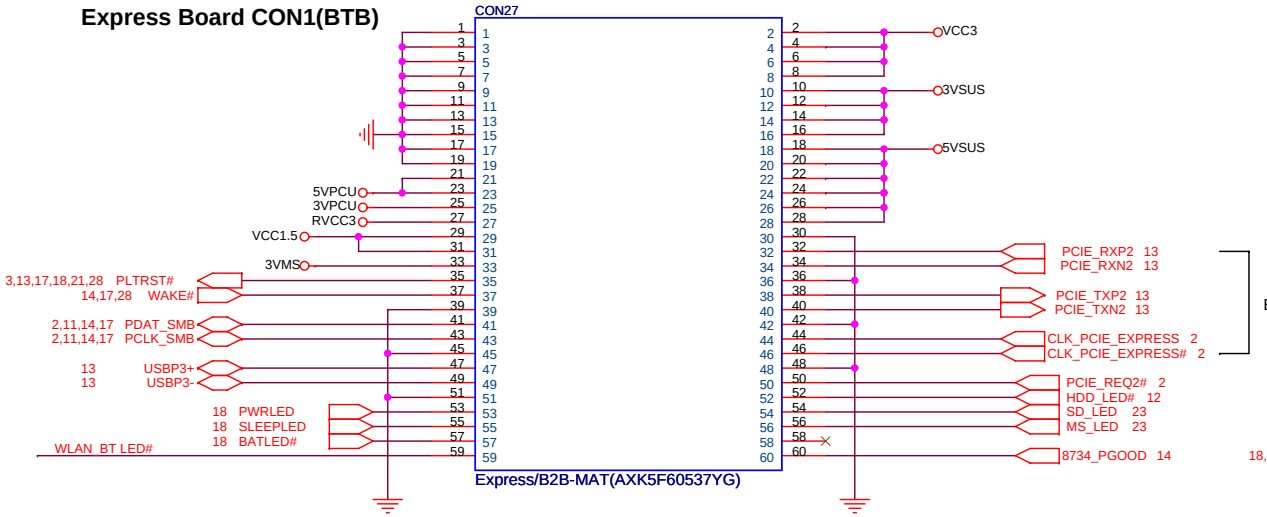
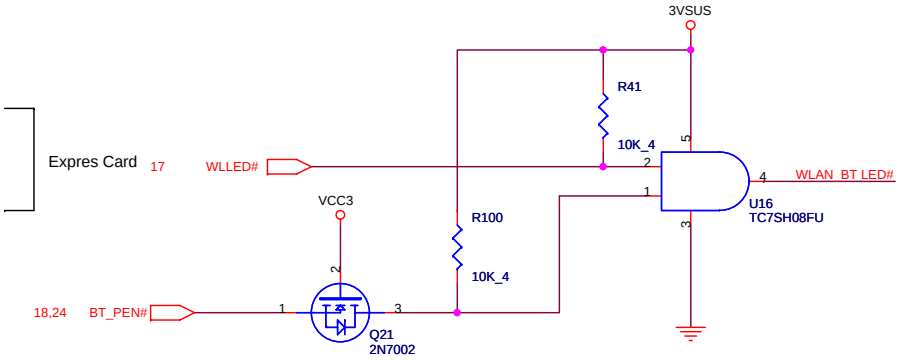
QUANTA COMPUTER

Title	ICH8-M Power 4 o 4	
Size	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007	Sheet 15 of 35	

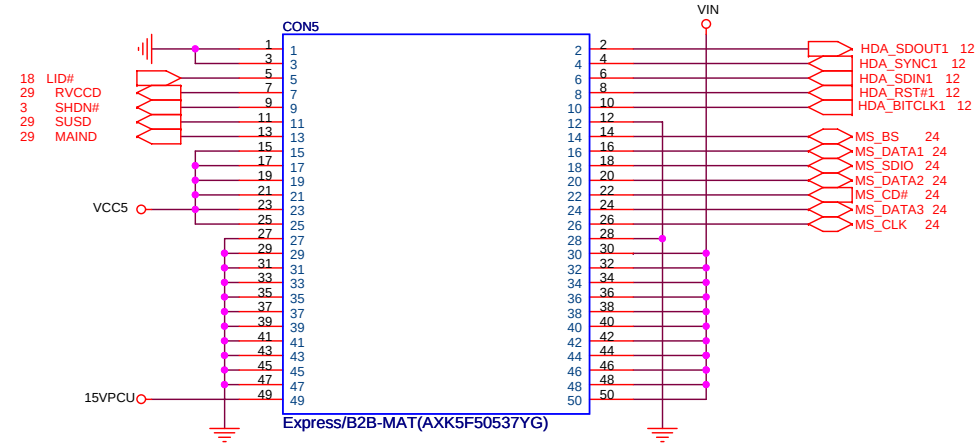
Express Board CON1(BTB)



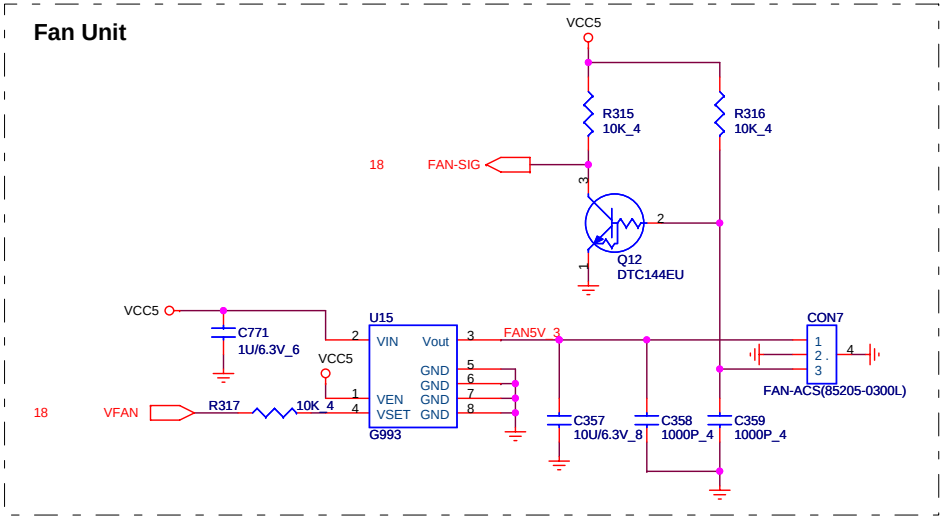
Expres Card 17



Express Board CON2(BTB)



Fan Unit



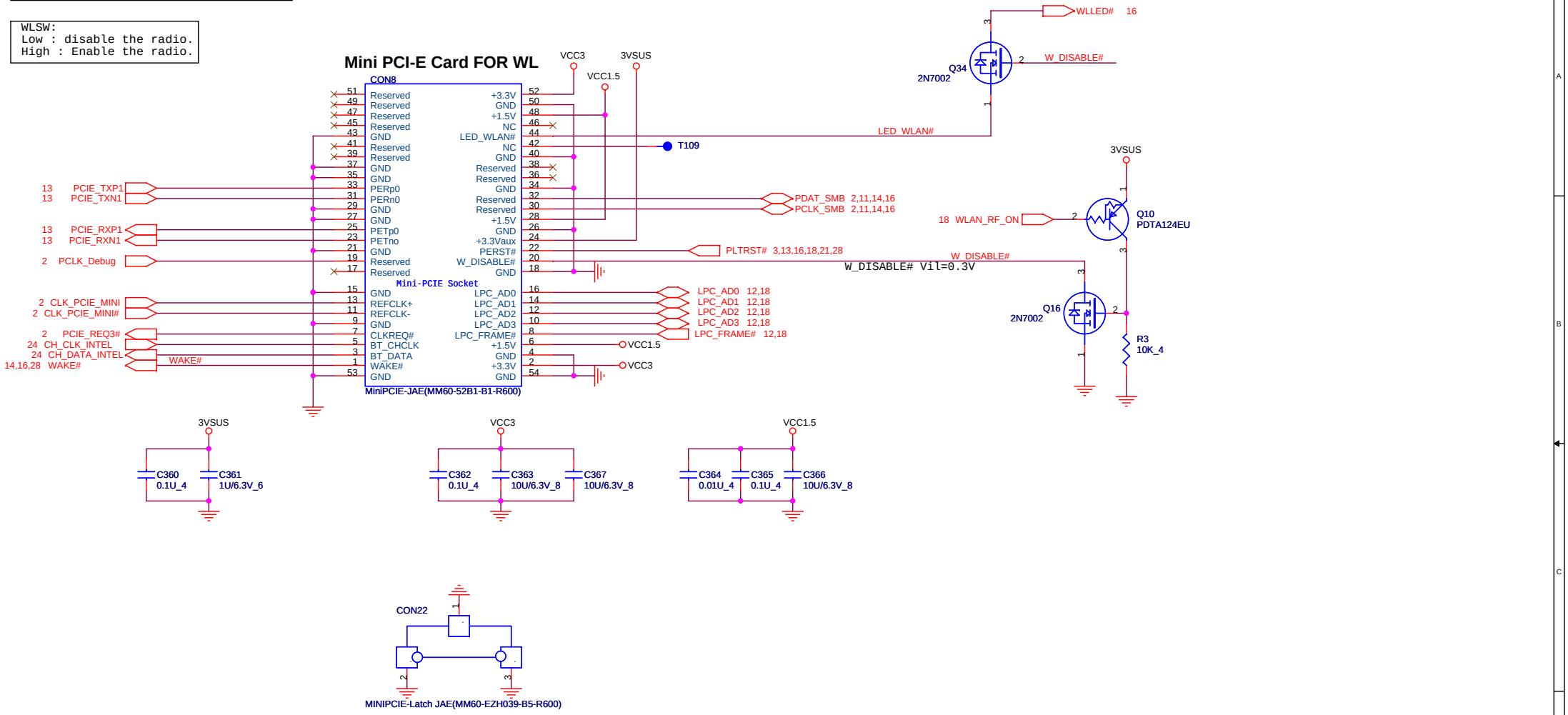
1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: Express Card		
Size: B	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007	Sheet 16 of 35	

LED_GP :LED WLEN LINK
Output Current : 7mA
Blink rate : 1 flash per every 3 sec.

WLSW:
Low : disable the radio.
High : Enable the radio.



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	MINIPCIE / MDC	
Size B	Document Number GD1A Main Board	Rev 2A
Date: Monday, July 23, 2007	Sheet 17 of 35	

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SPI Flash

U19 WND(W25X80VSSIG)

WPC8763L

I/O Address		
BADDR1:0	Index	Data
1 0	2E	2F
1 1	4E	4F
0 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
0 1	XOR-TREE TEST	

DOCK_RST# : BADDR0
DK_BAY_PWEN: BADDR1

BT_PEN# : SHBM(If = 0 Enable share host BIOS memory)

PWROK must be after HWPG at least 10ms
VRON must be after PGOOD at least 99ms

MAINON <-- 3ms --> MAION1
MAINON <-- 3.5ms --> MAION2

MAINON
MAINON1
MAINON2
3ms
3.5ms

100ms
VRON
PGOOD
11ms
PWROK
HWPG

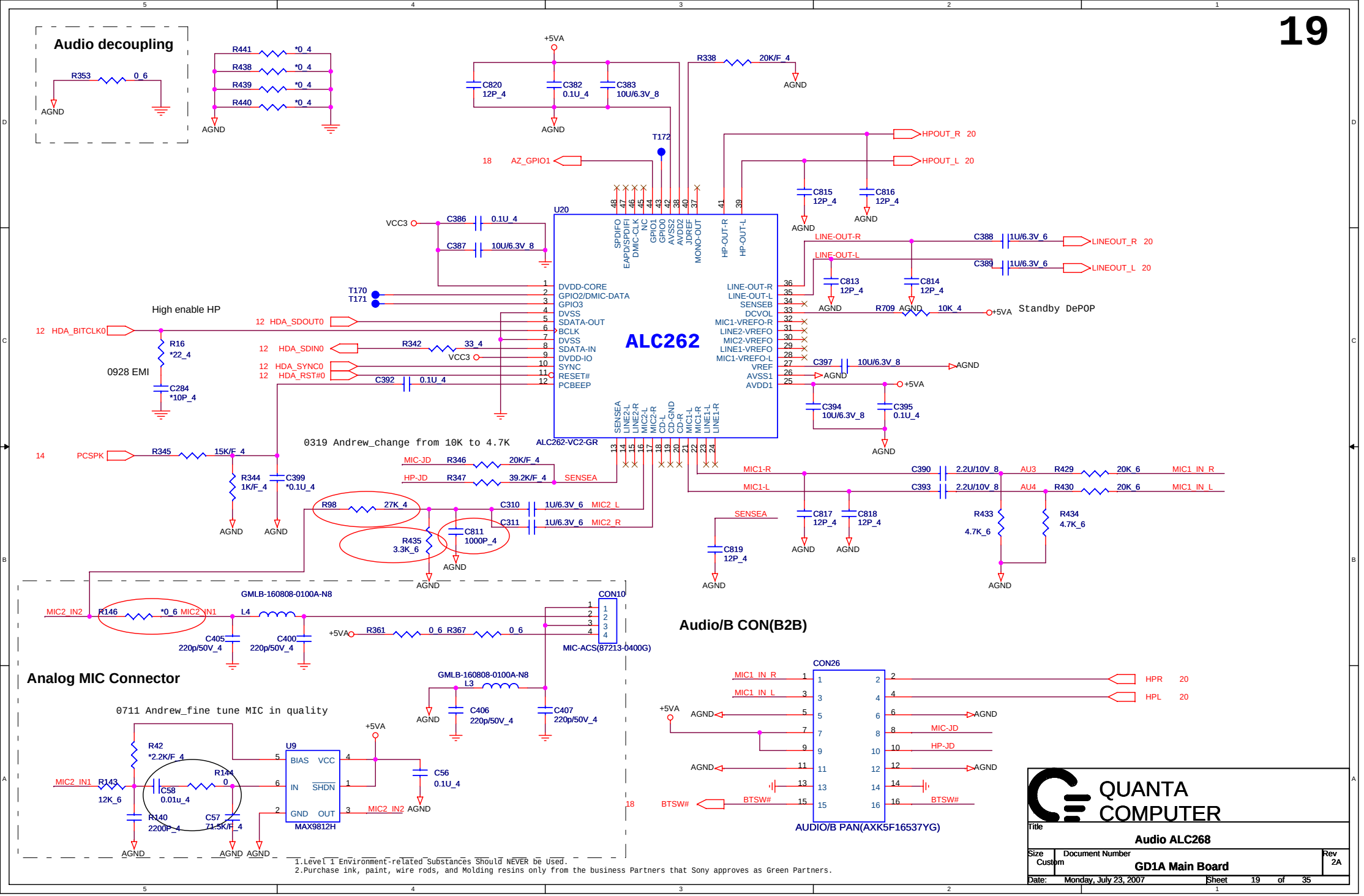
JTAG SELECT CONFIGURATION

JEN0(PIN24)	JENK(PIN53)	Functionality of PINs (17,20,21,23,25,27)	Functionality of PINs (47,48,50,51,52)
NC	NC	GPIO	KEYBOARD OUTPUT
10K PD	NC	JTAG Signal	KEYBOARD OUTPUT
NC	10K PD	GPIO	JTAG Signal
10K PD	10K PD	Illegal Strap combination	

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	WPC8763L & SPI FLASH	
Size	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007	Sheet 18 of 35	



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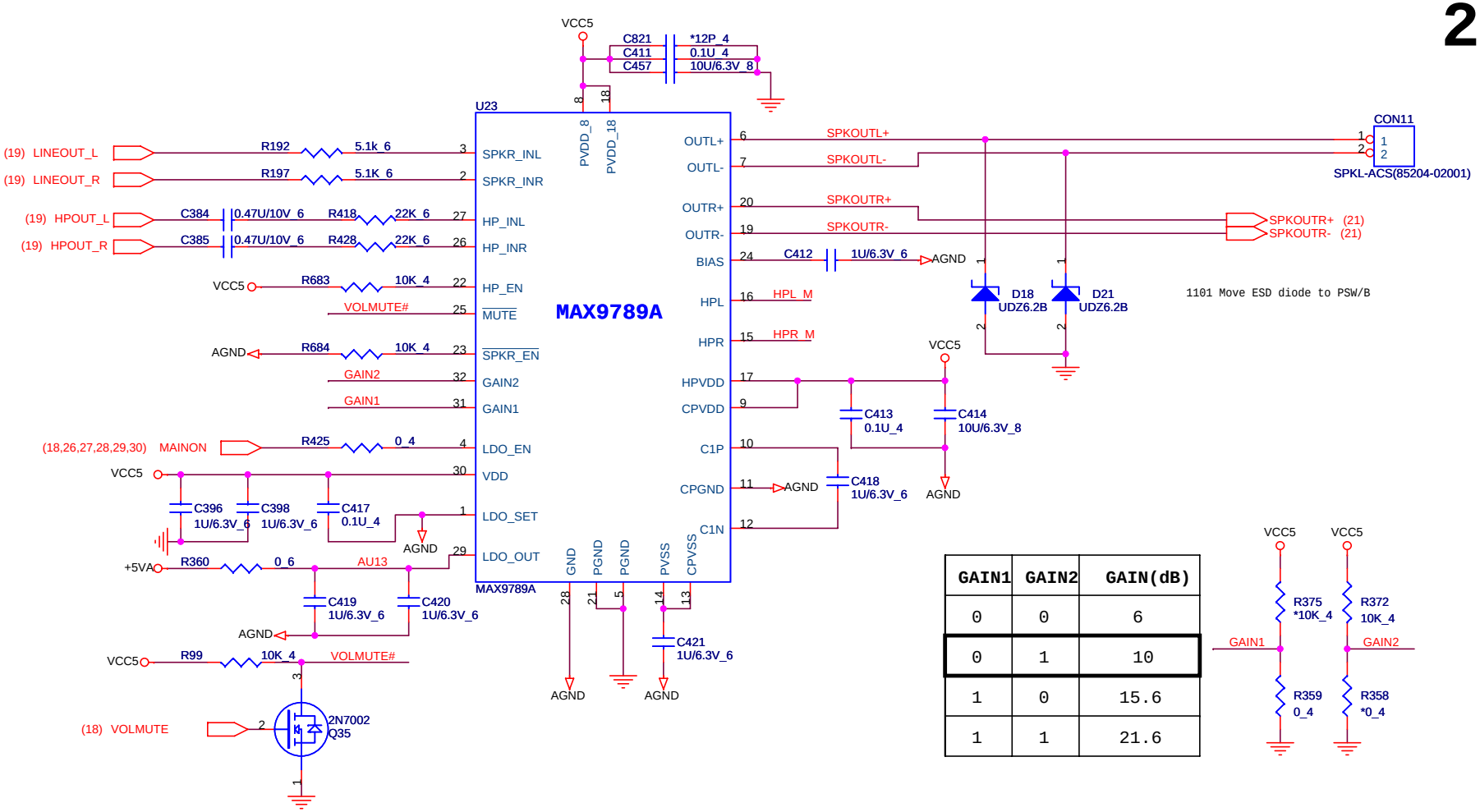
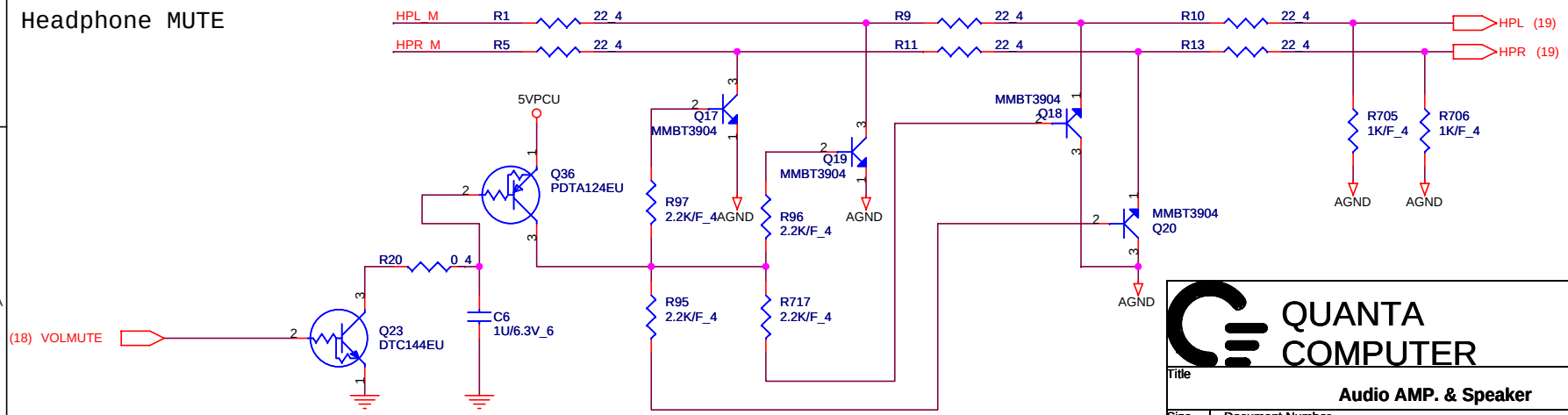


GAIN1	GAIN2	GAIN(dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6

Headphone MUTE

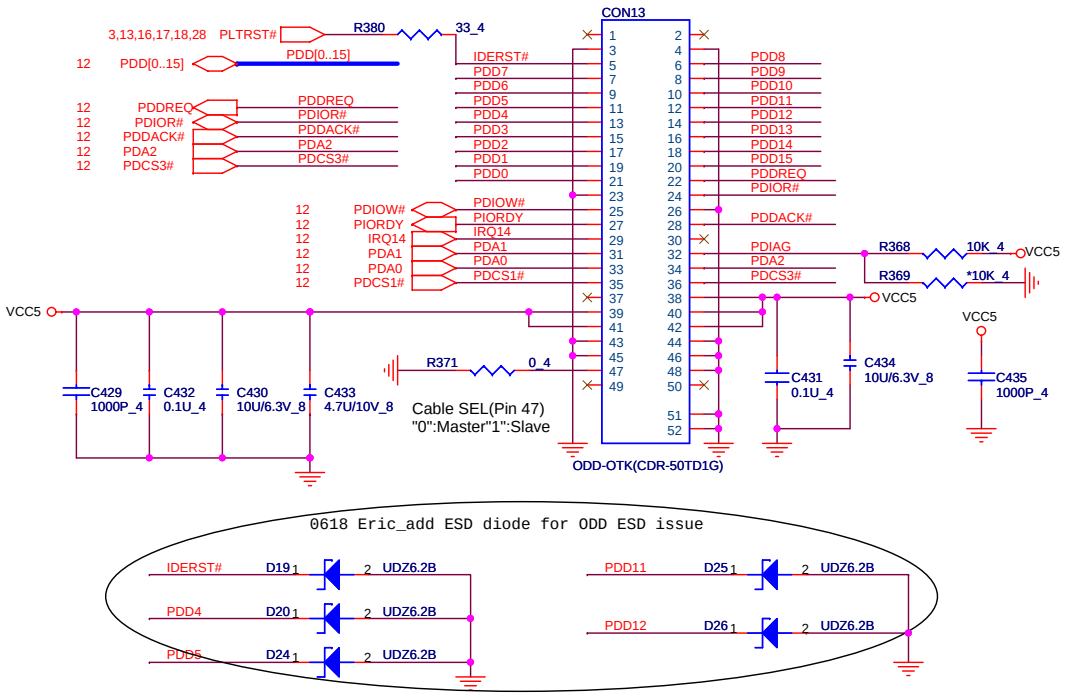


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

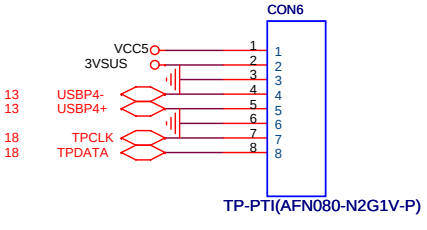
Title	Audio AMP. & Speaker	
Size: Custom	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007	Sheet 20 of 35	

ODD CONNECTOR

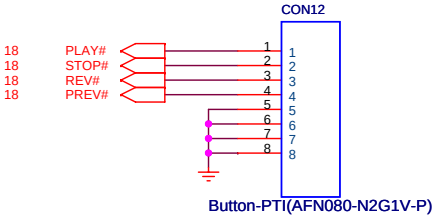


0618 Eric_add ESD diode for ODD ESD issue

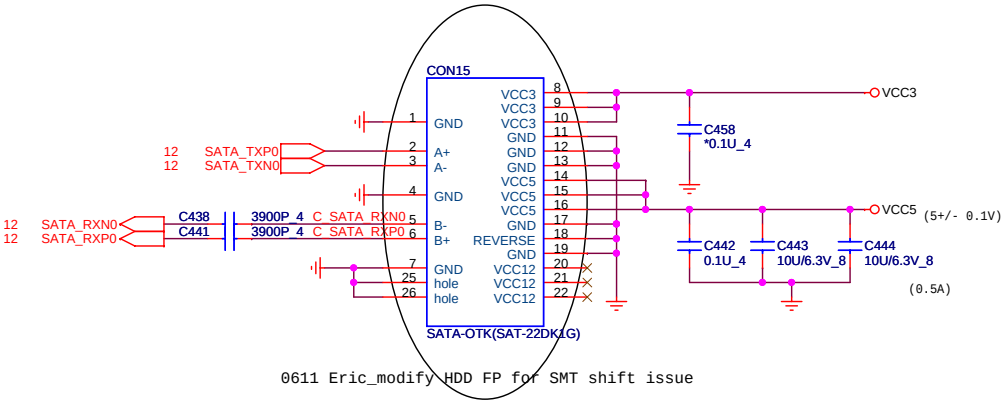
TouchPAD Board CON(FPC)



Button CON(FFC)

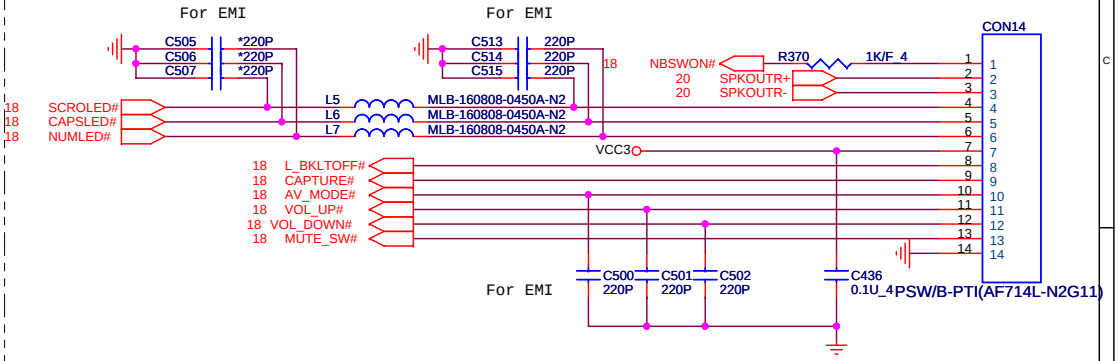


HDD CONNECTOR



0611 Eric_modify HDD FP for SMT shift issue

PSW Board CON(Inverse FFC)



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	HDD/ODD/PSW/BUT/TP	
Size B	Document Number GD1A Main Board	Rev 3A
Date: Monday, July 23, 2007	Sheet 21 of 35	

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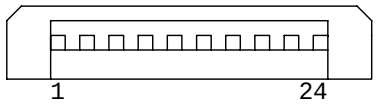
Keyboard



MY12 MY2 MY0 MY1 MY8 MY9 MY10 MY11 MX6 MX7 MX5 MX7 MX0 MX1 MX3 MX2 MY13 MY15 MY5 MX4 MY14 MY6 MY4 MY3

RP29 RP30 RP31 RP32 RP33 RP34 22X4

MY12_R MY2_R MY0_R MY1_R MY8_R MY9_R MY10_R MY11_R MX6_R MX7_R MX5_R MX7_R MX0_R MX1_R MX3_R MX2_R MY13_R MY15_R MY5_R MX4_R MY14_R MY6_R MY4_R MY3_R

CON16

MY1_R MY0_R MY2_R MY12_R MY11_R MY10_R MY9_R MY8_R MY7_R MX5_R MX7_R MX6_R MX2_R MX3_R MX1_R MX0_R MX4_R MY5_R MY15_R MY13_R MY3_R MY4_R MY6_R MY4_R MY14_R

KB-PTI(AFN240-N2G1V-P)

0711 Eric_modify FP for 2nd IR

3VPCU

U29

MX0 MX2 IO1 REF2 IO2 IO4 REF1 IO3 MX1 MX3

C454 *0.1U_4

*DALC208SC6

U30

MX5 MX6 IO1 REF2 IO2 IO4 REF1 IO3 MX7 MX4

C460 *0.1U_4

*DALC208SC6

3VPCU

RP35 MX0 MX1 MX3 MX2 10KX4

RP36 MX7 MX6 MX5 MX4 10KX4

CA1 CA2 CA3 CA4 CA5 CA6 220PX4

MY1 MY0 MY2 MY12 MY11 MY10 MY9 MY8 MX2 MX3 MX1 MX0 MX4 MY5 MY15 MY13 MY14 MY6 MY4 MY3 MX6 MX7 MY7 MX5

USB Port x 2

USBVCC0 13 USBP0- 13 USBP0+ LP1 *CMF-2012-0160I-S1 L32 0_8 C445 100U/6.3V_3528/ESR35 C447 1000P_4 D22 *NSAD500S CON17 USB-FOX(UB1112C-RA212-7F)

USBVCC1 13 USBP1- 13 USBP1+ LP2 *CMF-2012-0160I-S1 L33 0_8 C451 100U/6.3V_3528/ESR35 C452 *22U/10V/X5R C453 1000P_4 D23 *NSAD500S CON18 USB-FOX(UB1112C-RA212-7F)

U27 TPS2062 OUT A IN OUT B GND ENA ENB FLAGA FLAGB

5VSUS C449 1U/6.3V_6

USBVCC1 C448 0.1U_4

USBVCC0 C450 0.1U_4

USBOC1# 13 USBOC0# 13

Felica

5VSUS C466 1U/6.3V_6 13 USBP7- 13 USBP7+ CON20 FeliCa-PTI(AF706L-N2G11)

ODD

5VSUS VCC5 C901 1000P_4

5VSUS VIN C902 1000P_4

VCC3 VIN C903 1000P_4

VCC3 VCC1.5 C904 1000P_4

5VSUS VCC1.5 C905 1000P_4

VCC5 VCC3 C906 1000P_4

VCC5 VIN C907 1000P_4

PCI Bus

5VSUS VCC5 C911 1000P_4

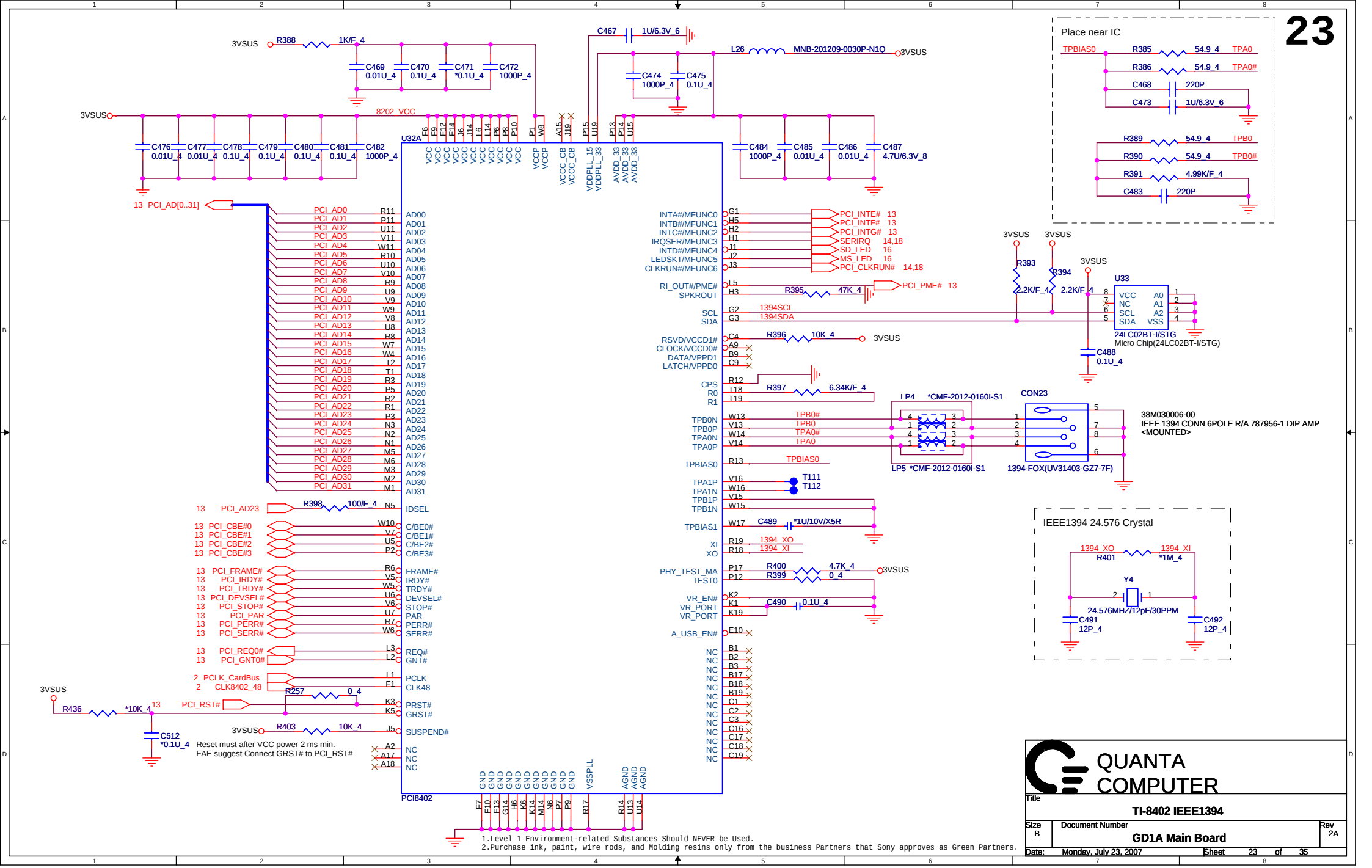
5VSUS VIN C912 1000P_4

VCC5 VCC3 C913 1000P_4

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	K/B ,USB Device	
Size B	Document Number GD1A Main Board	Rev 3A
Date: Monday, July 23, 2007	Sheet 22 of 35	



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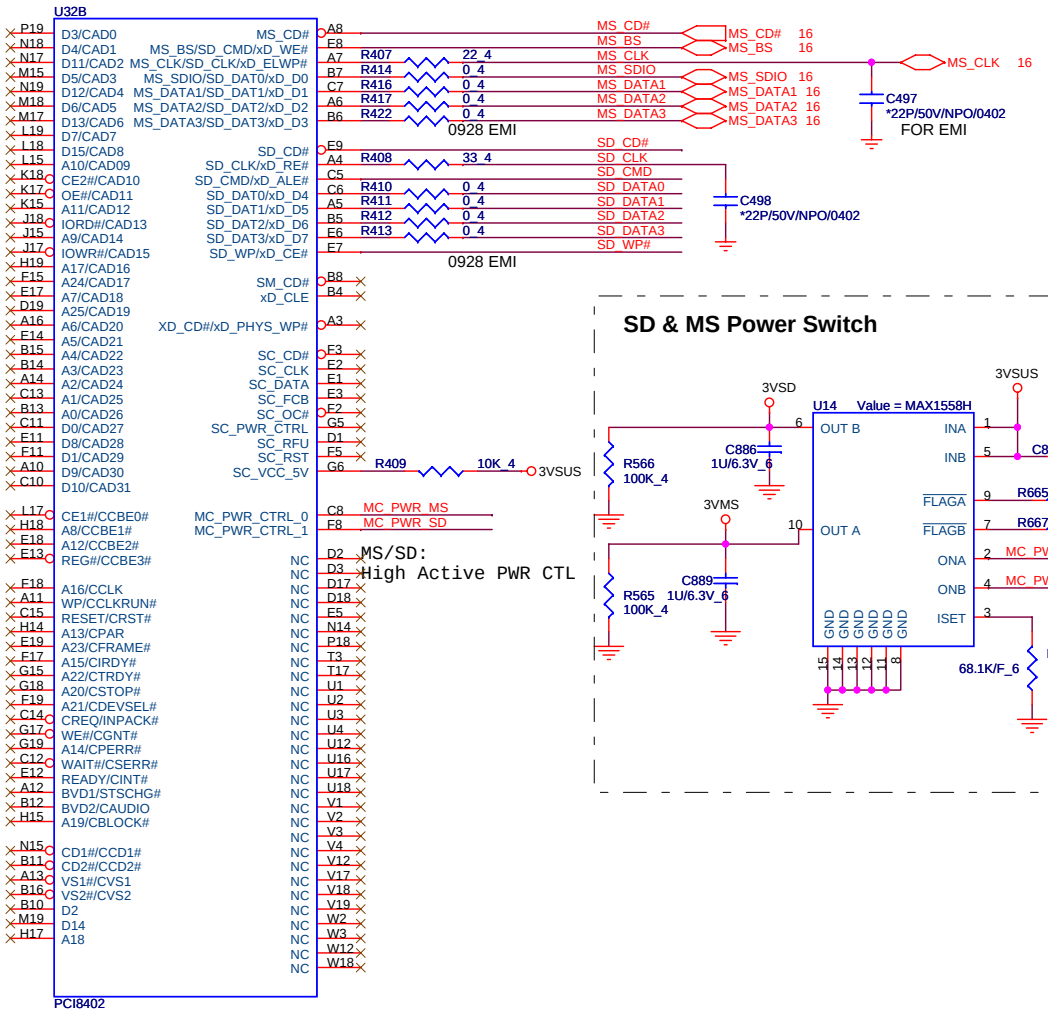
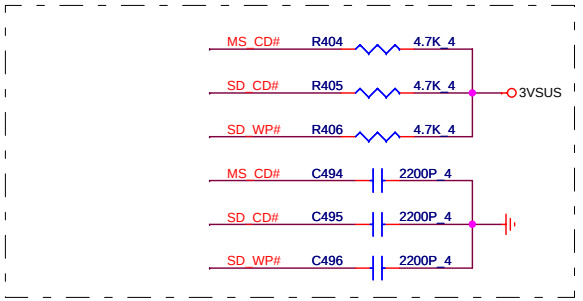
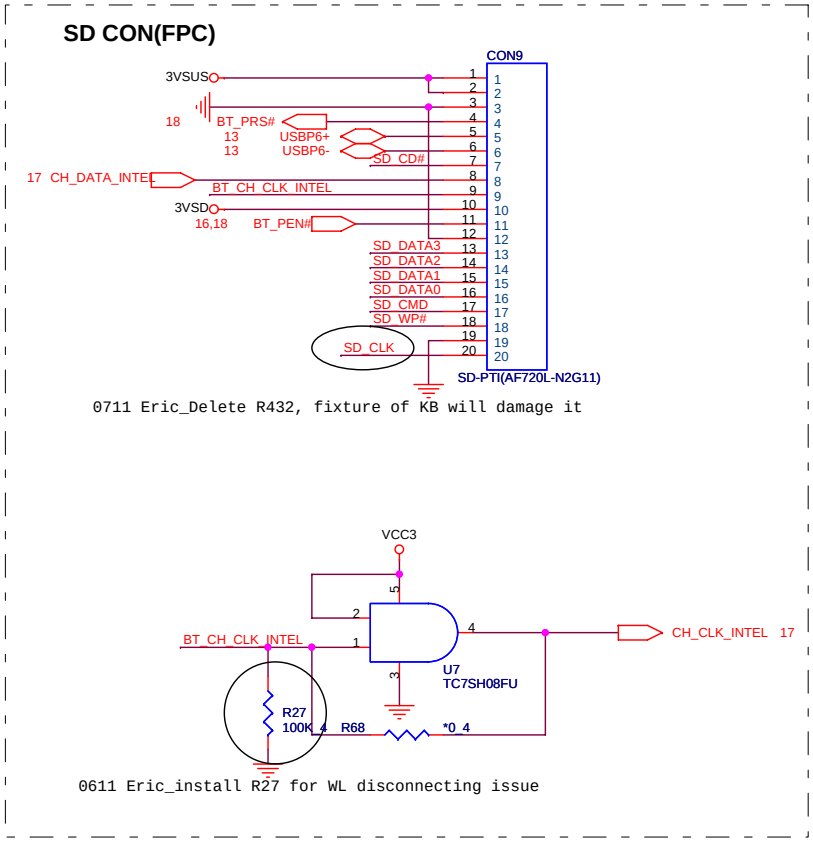


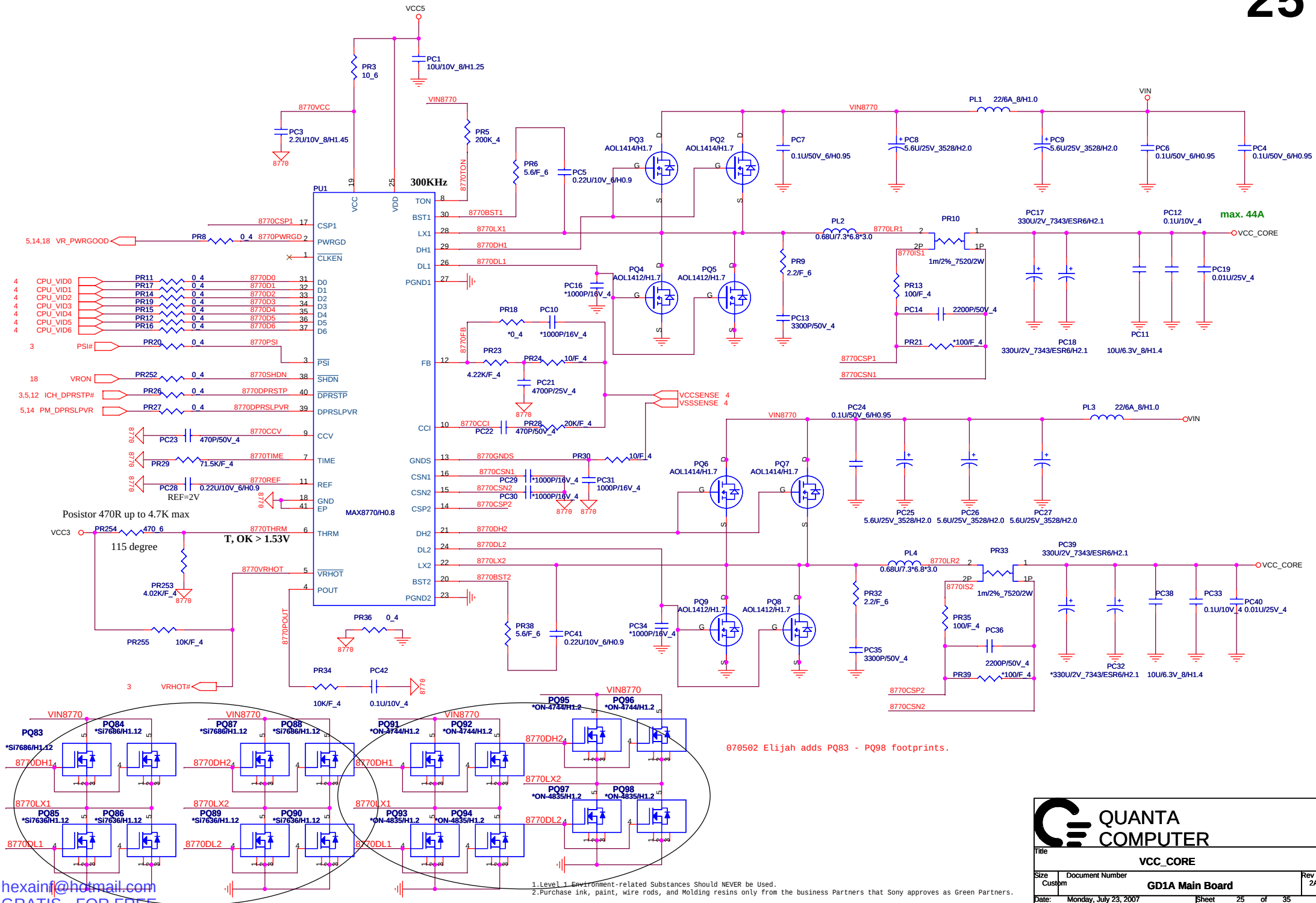




1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	TI-8402 MS & SD	
Size B	Document Number GD1A Main Board	Rev 3A
Date: Monday, July 23, 2007	Sheet 24 of 35	



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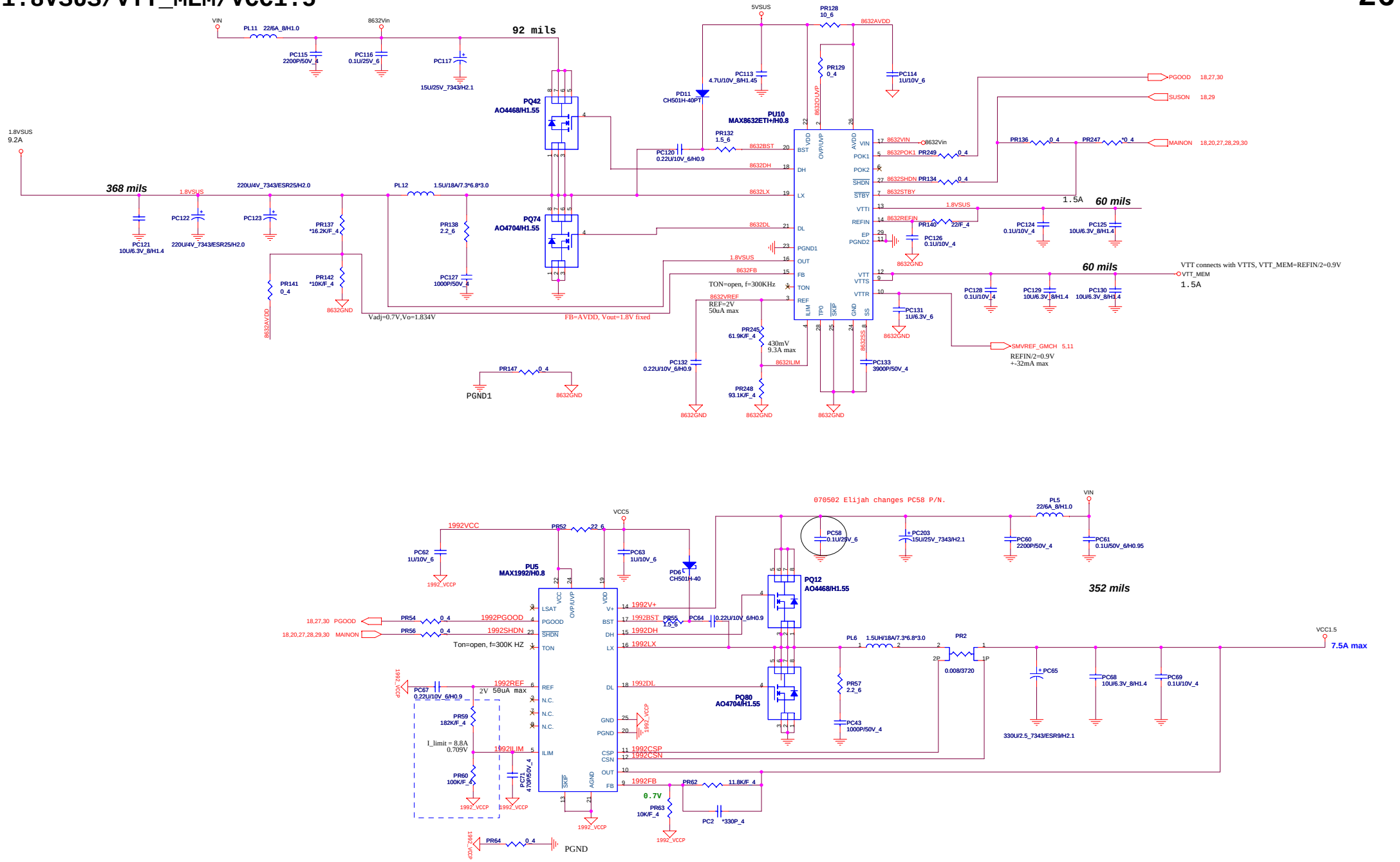
1.8VSUS/VTT_MEM/VCC1.5

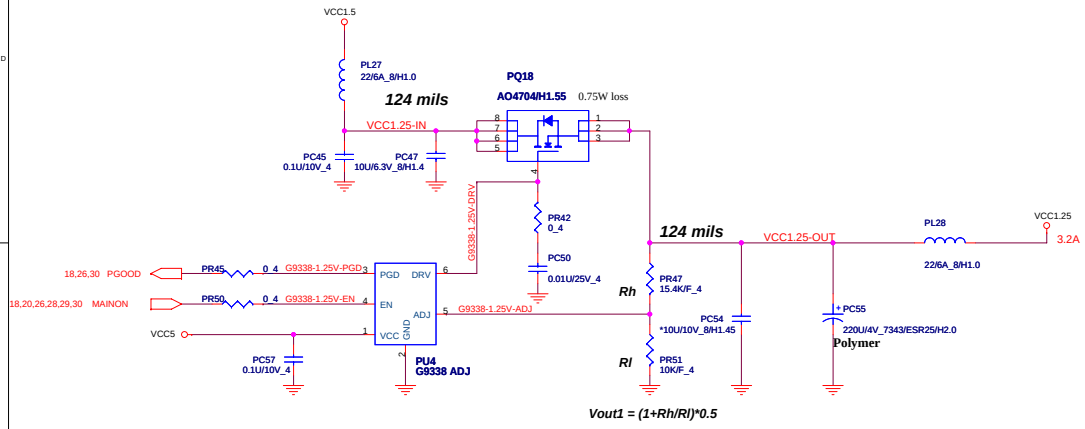


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

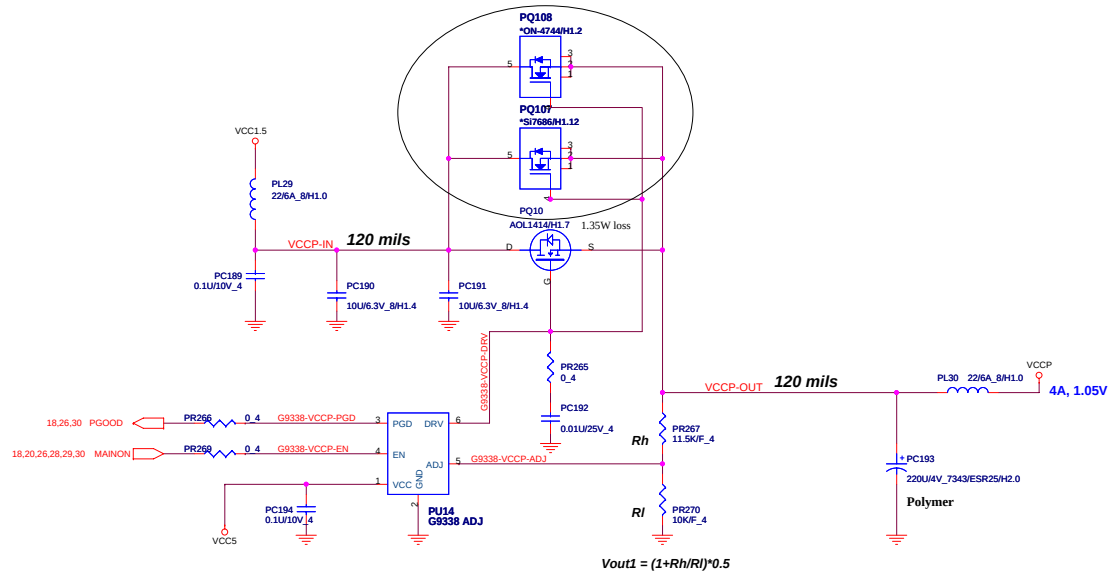
QUANTA COMPUTER

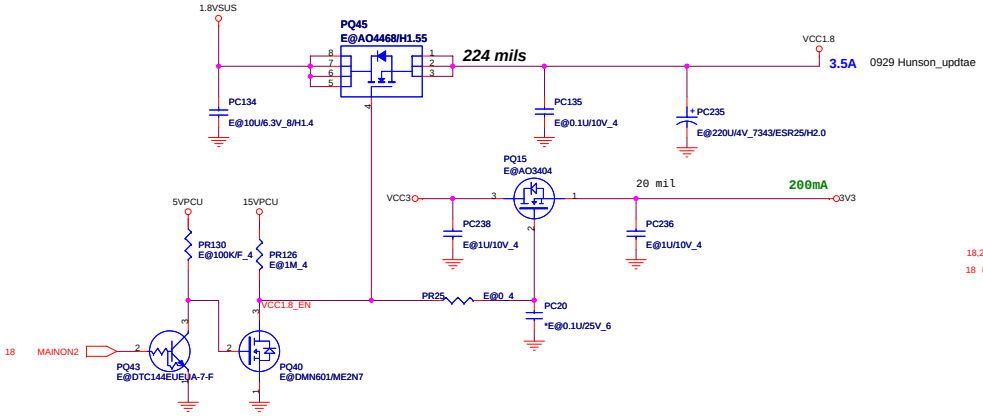
Title	1.8VSUS, VTT_MEM, VCC1.5	
Size	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007	Sheet 26 of 35	

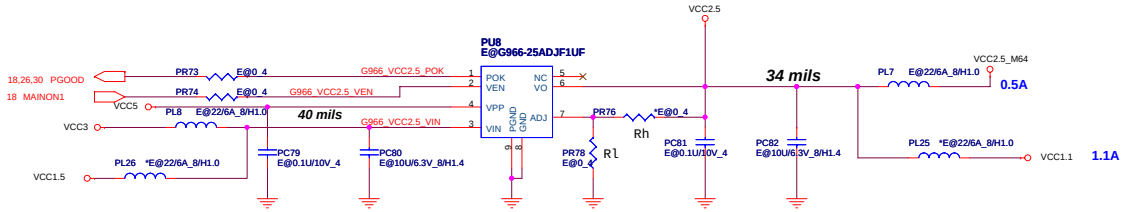
VCC2.5/VCC1.25/VCC1.8/VCCP



070502 Elijah adds two footprints.







Vo=(0.8*(Rh+Rl))/Rl
ADJ=GND, Vo= Fix 2.5V

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	VCC1.25, VCCP, VCC2.5, VCC1.8 & 3V3	
Size	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007	Sheet 27 of 35	

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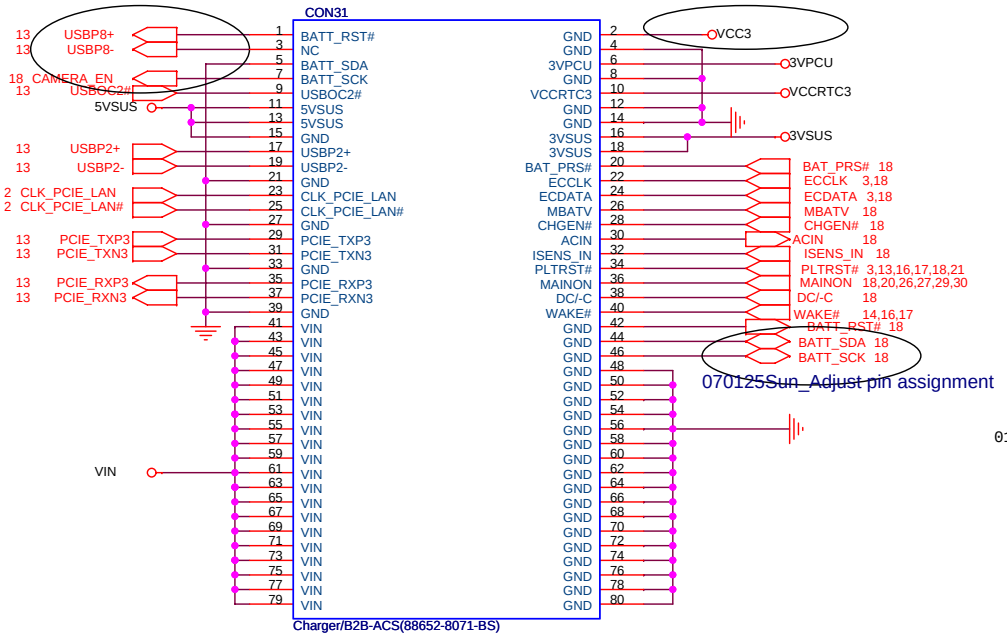
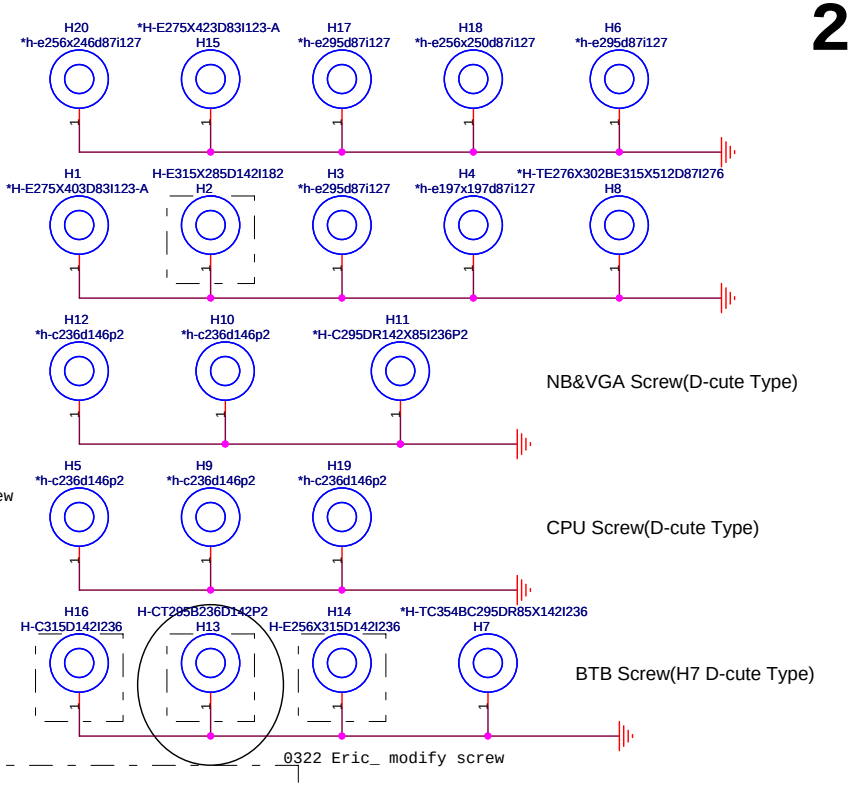
070125Sun_Adjust pin assignment

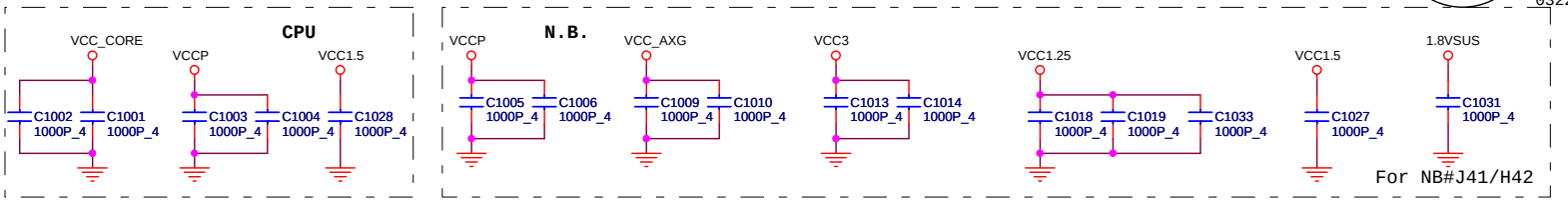


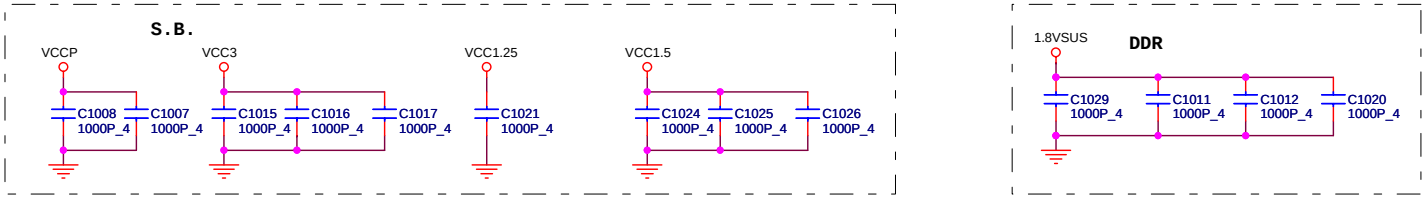
070125Sun_Adjust pin assignment

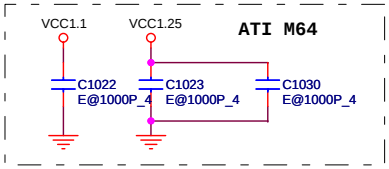
070125Sun_Adjust pin assignment

0109 Eric_modify Screw





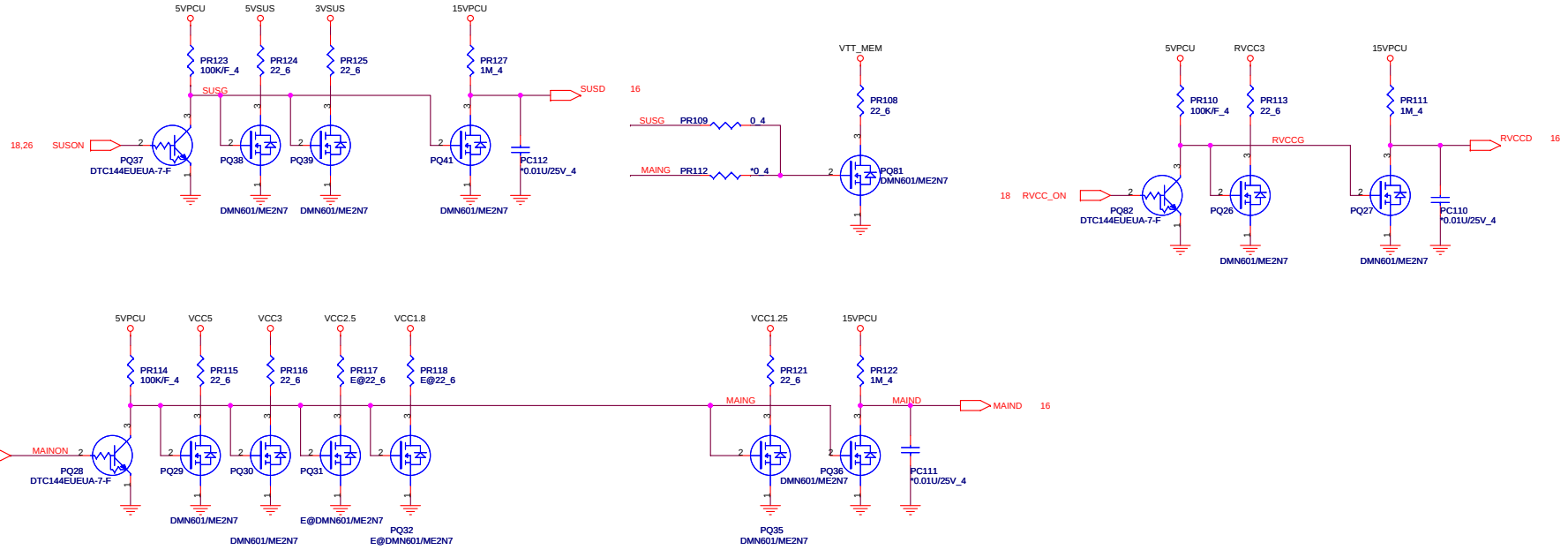




1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	Power Charger & LAN CON	
Size B	Document Number GD1A Main Board	Rev 2A
Date: Monday, July 23, 2007	Sheet 28 of 35	



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	Discharge, SUSD, RVCCD, MAIND	
Size: Custom	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007	Sheet 29 of 35	

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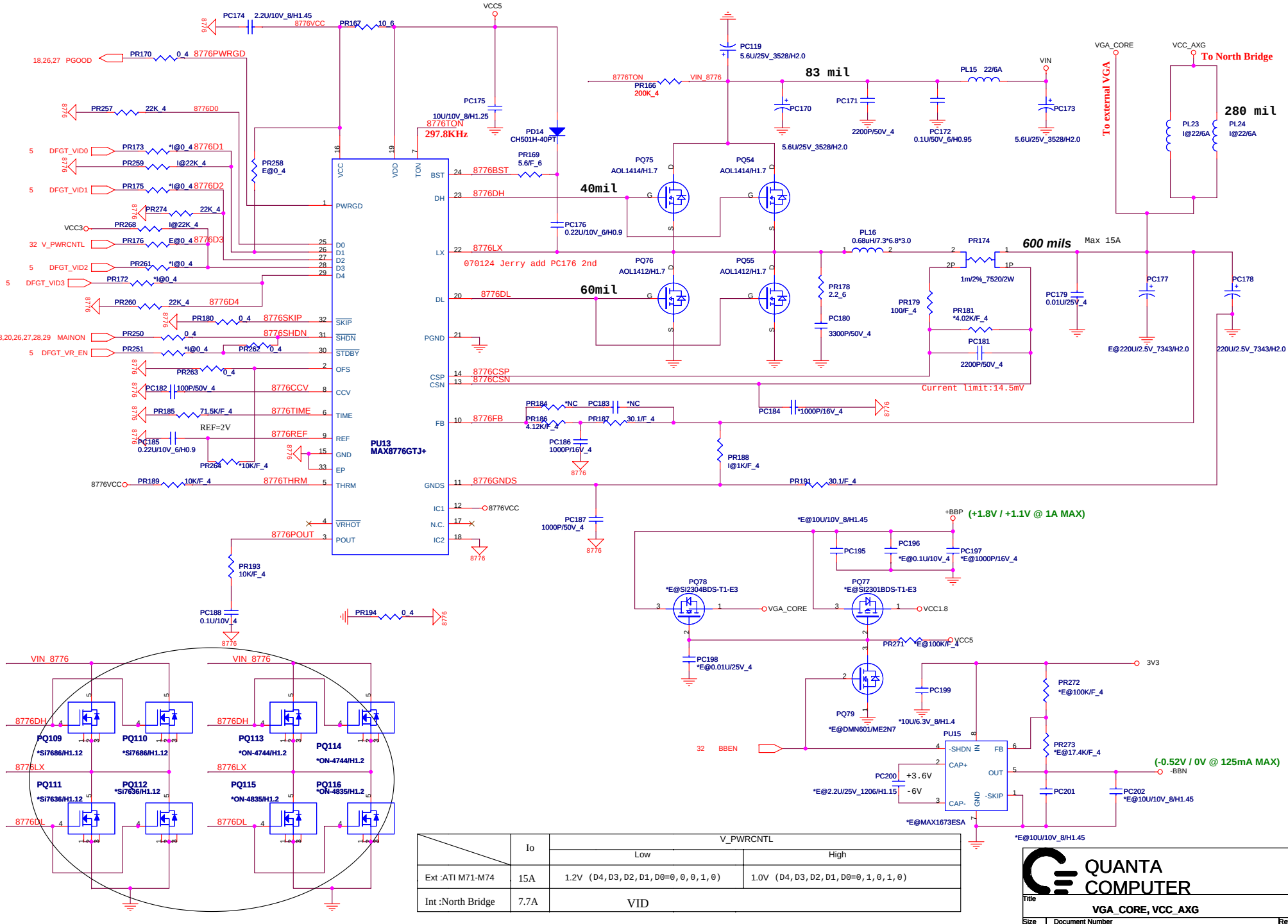


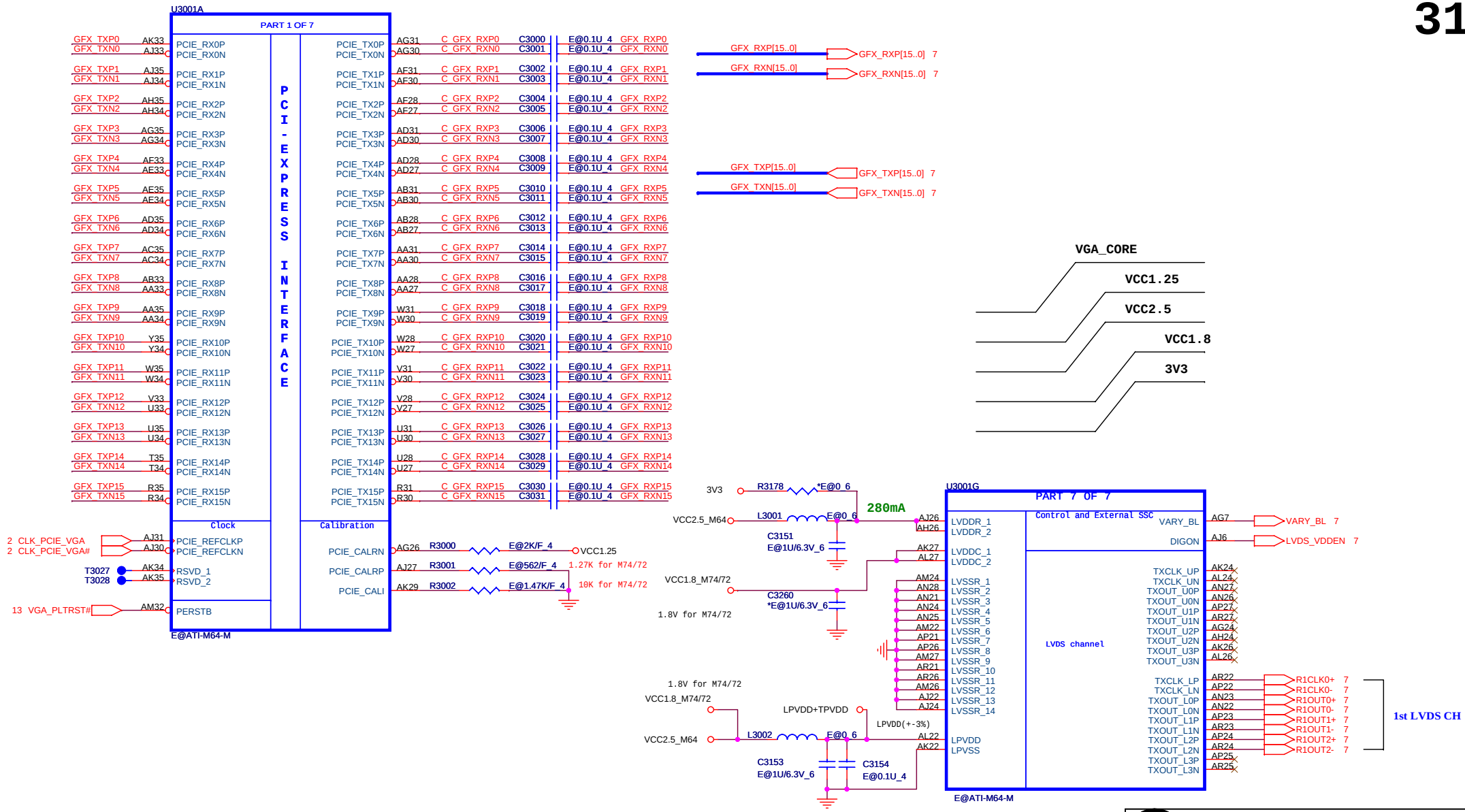
	Io	V_PWRCNTL	
		Low	High
Ext :ATI M71-M74	15A	1.2V (D4,D3,D2,D1,D0=0,0,0,1,0)	1.0V (D4,D3,D2,D1,D0=0,1,0,1,0)
Int :North Bridge	7.7A	VID	

070502 Elijah adds PQ109 - PQ116 footprints.

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	VGA_CORE, VCC_AXG	
Size	Document Number: GD1A Main Board	Rev: 2A
Date: Monday, July 23, 2007	Sheet 30 of 35	



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	ATI M64M PCIE	
Size B	Document Number GD1A Main Board	Rev 2A
Date: Monday, July 23, 2007	Sheet 31 of 35	

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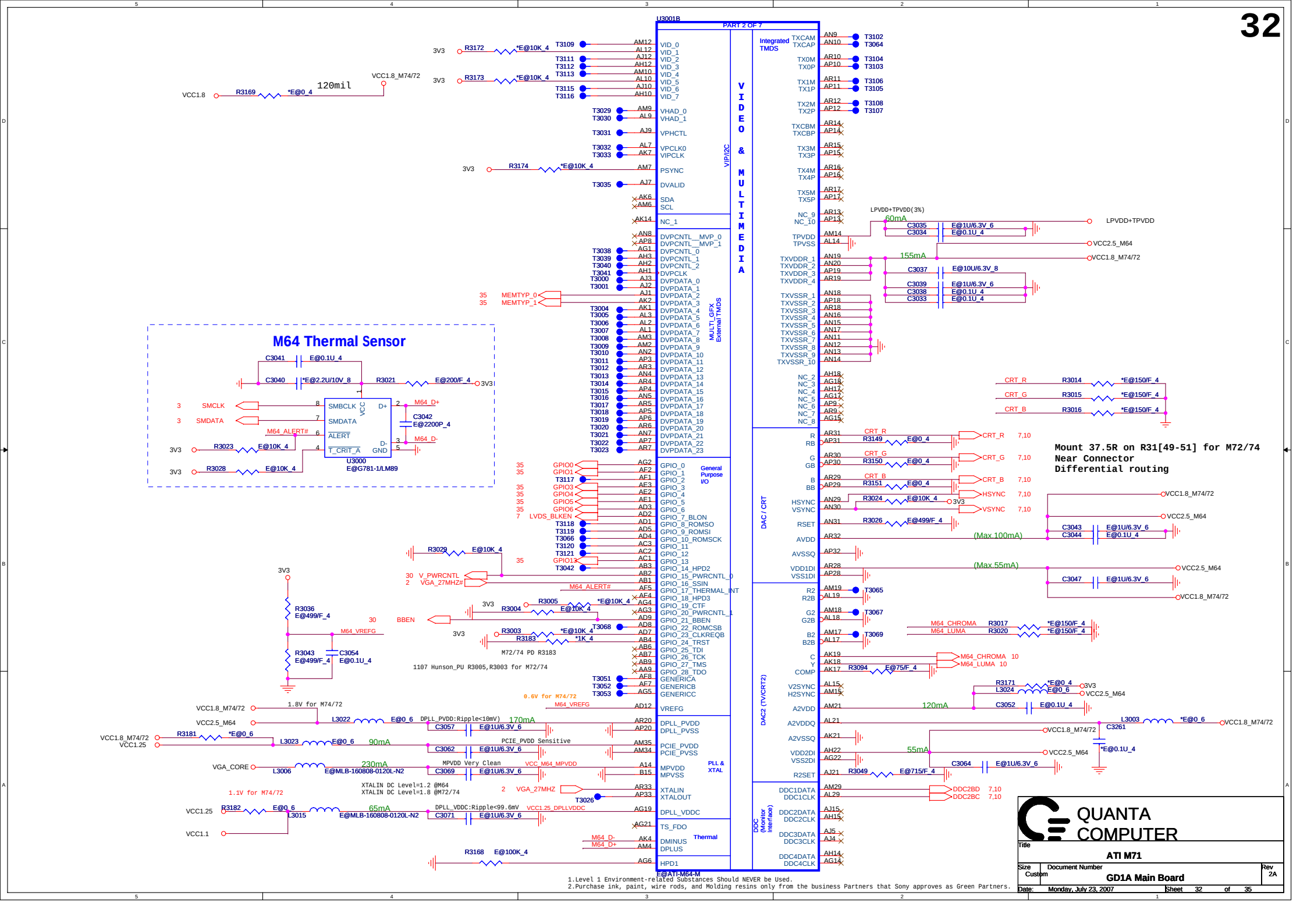
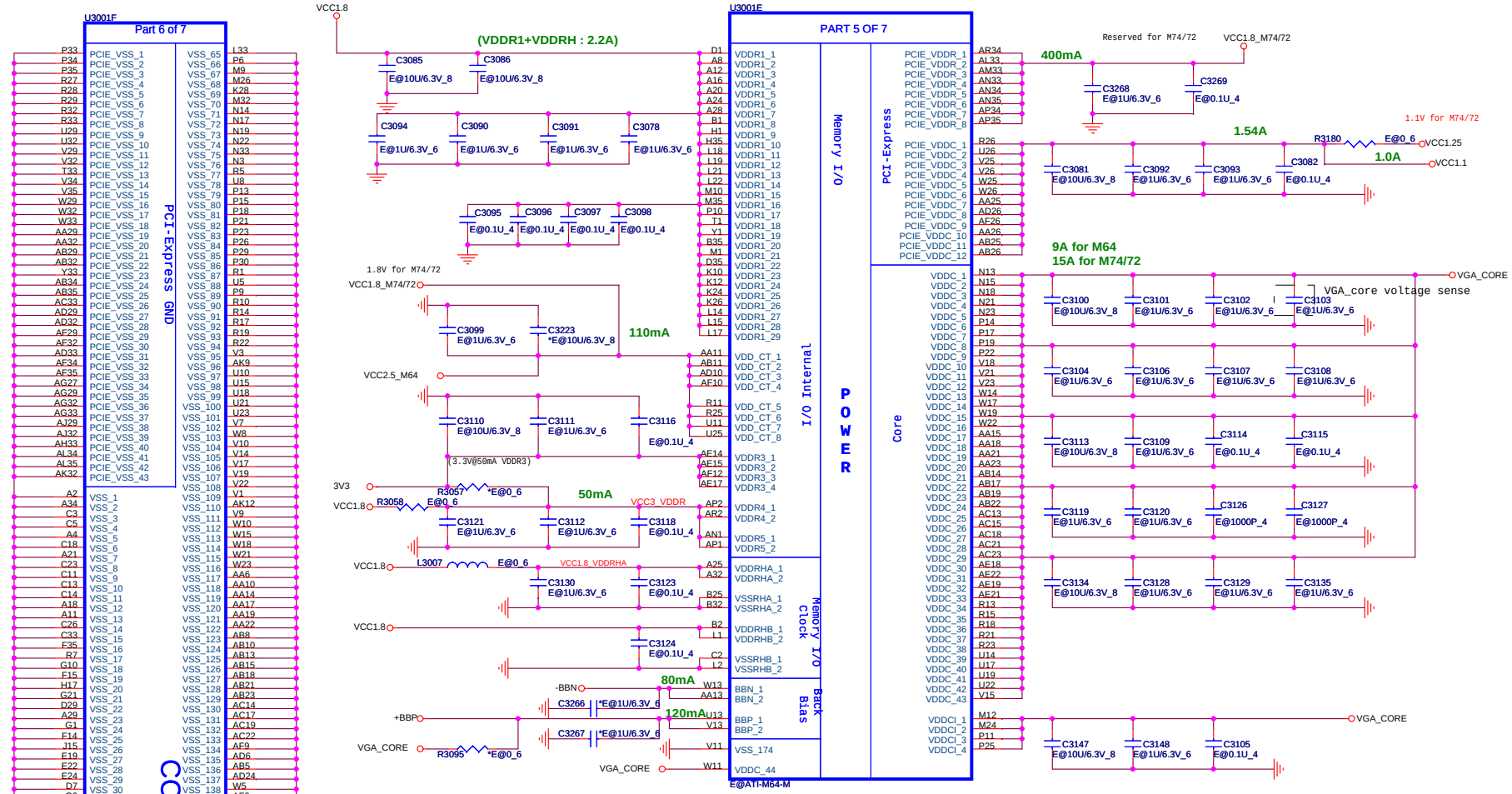

U3001B
PART 2 OF 7
VIDEO & MULTIMEDIA
VID_0
VID_1
VID_2
VID_3
VID_4
VID_5
VID_6
VID_7
VHAD_0
VHAD_1
VPHCTL
VPCLK0
VIPCLK
PSYNC
DVALID
SDA
SCL
NC_1
VIP/I2C
DVPCNTL_MVP_0
DVPCNTL_MVP_1
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCLK
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
MULTI_GFX External TMDS
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15_PWRCNTL_0
GPIO_16_SSIN
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21_BBEN
GPIO_22_ROMCSB
GPIO_23_CLKREQB
GPIO_24_TRST
GPIO_25_TDI
GPIO_26_TCK
GPIO_27_TMS
GPIO_28_TDO
GENERICA
GENERICB
GENERICC
General Purpose I/O
VREFG
DPLL_PVDD
DPLL_PVSS
PCIE_PVDD
PCIE_PVSS
MPVDD
MPVSS
XTALIN
XTALOUT
DPLL_VDDC
PLL & XTAL
TS_FDO
DMINUS
DPLUS
HPD1
Thermal
E@ATI-M64-M
Integrated TMDS
TXCAM
TXCAP
TX0M
TX0P
TX1M
TX1P
TX2M
TX2P
TXCBM
TXCBP
TX3M
TX3P
TX4M
TX4P
TX5M
TX5P
NC_9
NC_10
TPVDD
TPVSS
TXVDDR_1
TXVDDR_2
TXVDDR_3
TXVDDR_4
TXVSSR_1
TXVSSR_2
TXVSSR_3
TXVSSR_4
TXVSSR_5
TXVSSR_6
TXVSSR_7
TXVSSR_8
TXVSSR_9
TXVSSR_10
NC_2
NC_3
NC_4
NC_5
NC_6
NC_7
NC_8
DAC / CRT
R
RB
G
GB
B
BB
HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1DI
VSS1DI
R2
R2B
G2
G2B
B2
B2B
C
Y
COMP
DAC2 (TV/CRT2)
V2SYNC
H2SYNC
A2VDD
A2VDDQ
A2VSSQ
VDD2DI
VSS2DI
R2SET
DDC (Monitor Interface)
DDC1DATA
DDC1CLK
DDC2DATA
DDC2CLK
DDC3DATA
DDC3CLK
DDC4DATA
DDC4CLK
LPVDD+TPVDD(3%)
60mA
LPVDD+TPVDD
155mA
VCC2.5_M64
VCC1.8_M74/72
(Max.100mA)
(Max.55mA)
120mA
55mA
Mount 37.5R on R31[49-51] for M72/74
Near Connector
Differential routing
M64 Thermal Sensor
U3000
E@G781-1/LM89
SMCLK
SMDATA
M64_ALERT#
M64_D+
M64_D-
M64_VREFG
M64_CHROMA
M64_LUMA
CRT_R
CRT_G
CRT_B
HSYNC
VSYNC
V_PWRCNTL
VGA_27MHZ#
BBEN
LVDS_BLKEN
MEMTYP_0
MEMTYP_1
DDC2BD
DDC2BC
VGA_27MHZ
VCC_M64_MPVDD
M72/74 PD R3183
1107 Hunson_PU R3005,R3003 for M72/74
1.8V for M74/72
0.6V for M74/72
1.1V for M74/72
XTALIN DC Level=1.2 @M64
XTALIN DC Level=1.8 @M72/74
DPLL_PVDD:Ripple<10mV)
PCIE_PVDD Sensitive
MPVDD Very Clean
DPLL_VDDC:Ripple<99.6mV
VCC1.25_DPLLVDDC
VGA_CORE
VCC1.25
VCC1.1
VCC1.8
VCC1.8_M74/72
VCC2.5_M64
3V3
120mil
90mA
230mA
65mA
170mA
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.
QUANTA COMPUTER
Title
ATI M71
Size
Custom
Document Number
GD1A Main Board
Rev
2A
Date:
Monday, July 23, 2007
Sheet
32
of
35



POWER Regulator	M64/M71	Rail	M72/M74	Rail
VDDC+VDDCI	1.0~1.2V	VGA_CORE	0.95~1.1V	VGA_CORE
PCIE_PVDD	1.25	VCC1.25	1.8	VCC1.8_M74/72
PCIE_VDDR	NC	x	1.8	VCC1.8_M74/72
PCIE_VDDC	1.25	VCC1.25	1.1	VCC1.1
MPVDD	VDDC	VGA_CORE	VDDC	VGA_CORE
DPLL_PVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
DPLL_VDDC	1.25	VCC1.25	1.1	VCC1.1
VDDR1+VDDRH	1.8	VCC1.8	1.8	VCC1.8
VDDR4+VDDR5	1.8	VCC1.8	1.8	VCC1.8
VDDR3	3.3	3V3	3.3	3V3
VDD_CT	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
LPVDD+TPVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
LVDDR	2.5	VCC2.5_M64	3.3	3V3_M74/72
LVDDC	NC	x	1.8	VCC1.8_M74/72
TXVDDR	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
AVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
VDD1DI+VDD2DI	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
A2VDD	2.5	VCC2.5_M64	3.3	3V3_M74/72
A2VDDQ	NC	x	1.8	VCC1.8_M74/72

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

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Channel A

U3001C — Part 3 of 7 — MEMORY INTERFACE A — E@ATI-M64-M

Signal		DDR1,2	DDR3
MVREF to 1.8V		100R	40.2R
MVREF to GND		100R	100R

close to M64

U3002 / U3003 — E@VRAM_256Mb

SAM PN#AKD5JWFT508
SNI PN#AKD5JW-T^05

Use for DDR2 only, keep NC for others

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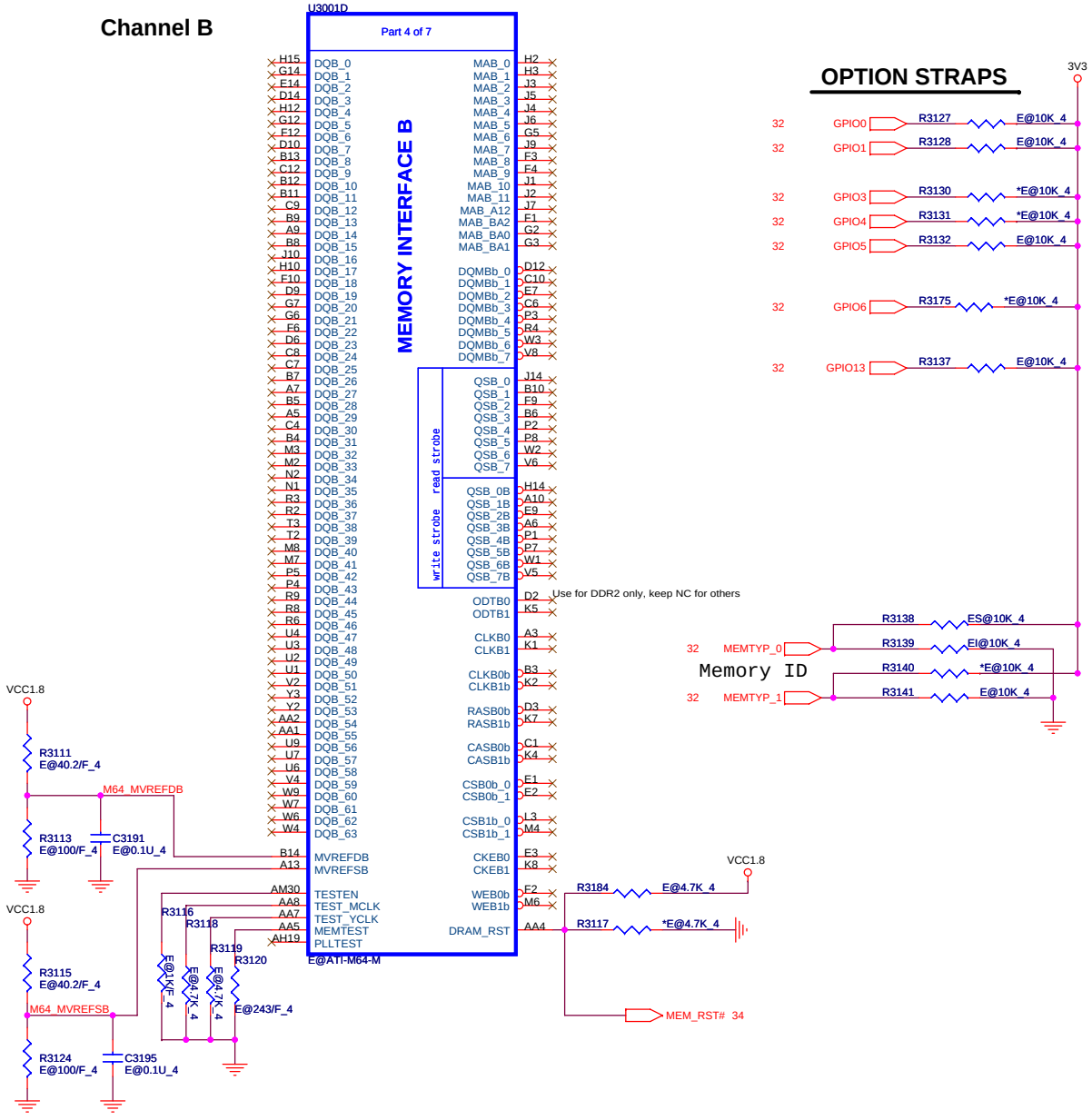
Channel B



OPTION STRAPS

M64-M Strap

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: full Tx output swing (recommended)	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled (recommended)	0 (internal pull-down)
Reserved	GPIO(3:2)	ATI internal use only. Other logic must not affect this signal during RESET.(GPIO2=VDD_VCL)	00
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0 (internal pull-down)
PLL_IBIAS_RD	GPIO[6:5]	Bias Current for the PCI Express PHY PLL	01
Reserved	GPIO8	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128MB 001x - No ROM,MEM_AP_SIZE=01 256MB 010x - No ROM, MEM_AP_SIZE=10 64MB(Default) 011x - No ROM,MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	GPIO[9,13,12,11] 0000 (internal pull-down)
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port deviced present. 1-No slave VIP port devices reporting presence during reset	0 (internal pull-down)
Reserved	PCIE_TEST	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
Reserved	HSYNC	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0

VRAM Straps REV. 0.1

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE[1:0]	GPIO 27,26	Memory identification for BIOS 00 - Infineon GDDR3 : 2M x 32 bits x 4 banks(Default) 01 - SAMSUNG GDDR3 : 2M x 32 bits x 4 banks 10 - RESERVED 11 - RESERVED	00

MEMTYPE1	MEMTYPE0	R3140	R3141	R3138	R3139	
0	0	NC	10K	NC	10K	00 - Infineon GDDR3 : 2M x 32 bits x 4 banks
0	1	NC	10K	10K	NC	01 - SAMSUNG GDDR3(G) : 2M x 32 bits x 4 banks
1	0	10K	NC	NC	10K	10 - Hynix GDDR3: 2M x 32 bits x 4 banks
1	1	10K	NC	10K	NC	11 - SAMSUNG GDDR3(I) : 2M x 32 bits x 4 banks

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QUANTA COMPUTER

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