JM31-CP Block Diagram

Project code: 91.4HL01.001
PCB P/N : 48.4HL01.031
REVISION : 09921-3

Clock Generator
ICS9LRS3197AKLFT 3

DDRIII Slot 0
800/1066/1333 20

DDRIII Slot 1
800/1066/1333 21

DDRII Channel A

DDR II Channel B

Intel CPU
Arrandale
4,5,..,9,10

FDIx8

DMIx4

PCI EXPRESS GRAPHIC
X16

Madison
ATI
22

Digital Display

HDMI 25

INTEL
PCH

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
6 SATA ports
8 PCIE ports
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE

11,12,...,18,19

RGB CRT

CRT 24

LVDS ICH

LCD
WXGA+ 23

Mini-Card
3G 37

PCIE+USB 2.0

Mini-Card
WLAN 38

PCIE+USB 2.0

WEBCAM 23

BLUETOOTH 29

USB 2.0

USB x 2 30

RJ45
CONN 32

Giga LAN
Atheros AR8151
31

PCIE

LAN Small Card
Project code: 91.4HL01.001
PCB P/N:09733

Card Reader
AU 6433 37

SD/MMC
MS/MS Pro/xD 37

Cardreader Small Card
Project code: 91.4HL01.001
PCB P/N : 09732

MIC IN

Digital MIC

HD AUDIO
CODEC
ALC271X 33

AZALIA

SATA

SATA HDD 26

LINE OUT

2CH SPEAKER

SPI

LPC Bus

LPC debug 41

Flash ROM
4MB 41

KBC
NPCE781B
40

SPI

Flash ROM
128KB 41

Thermal
Sensor 39
G787

Touch
PAD 43

Int.
KB 40

Power Board
37

Cardreader Small Card
Project code: 91.4HL01.001
PCB P/N : 09734

CPU FAN 2

CPU FAN 1

SYSTEM DC/DC RT8223BGQW	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 49

SYSTEM DC/DC RT8209EGQW	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 50

SYSTEM DC/DC RT8209EGQW	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 50

SYSTEM DC/DC RT8209EGQW	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 51

CPU DC/DC ISL62882HRTZ-T	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 47,48

MAXIM CHARGER ISL62881HRTZ-T	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 53

PCB STACKUP

TOP
GND
S
S
GND
BOTTOM

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Title: Block Diagram

Size	Document Number	Rev
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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ – 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default – Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved – Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** – Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE1	**LAN**
LANE2	**MiniCard1**
LANE3	**MiniCard2**

USB Table

Pair	*Device*
0	*USB1*
1	*USB2*
2	*USB4*
3	*MINICARD2*
4	*WECAM*
5	*Blue Tooth*
6	*MINIC1*
7	*Cardreader*
8	*NC*
9	*NC*
10	*NC*
11	*NC*
12	*NC*
13	*NC*

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Title: **Table of Content**

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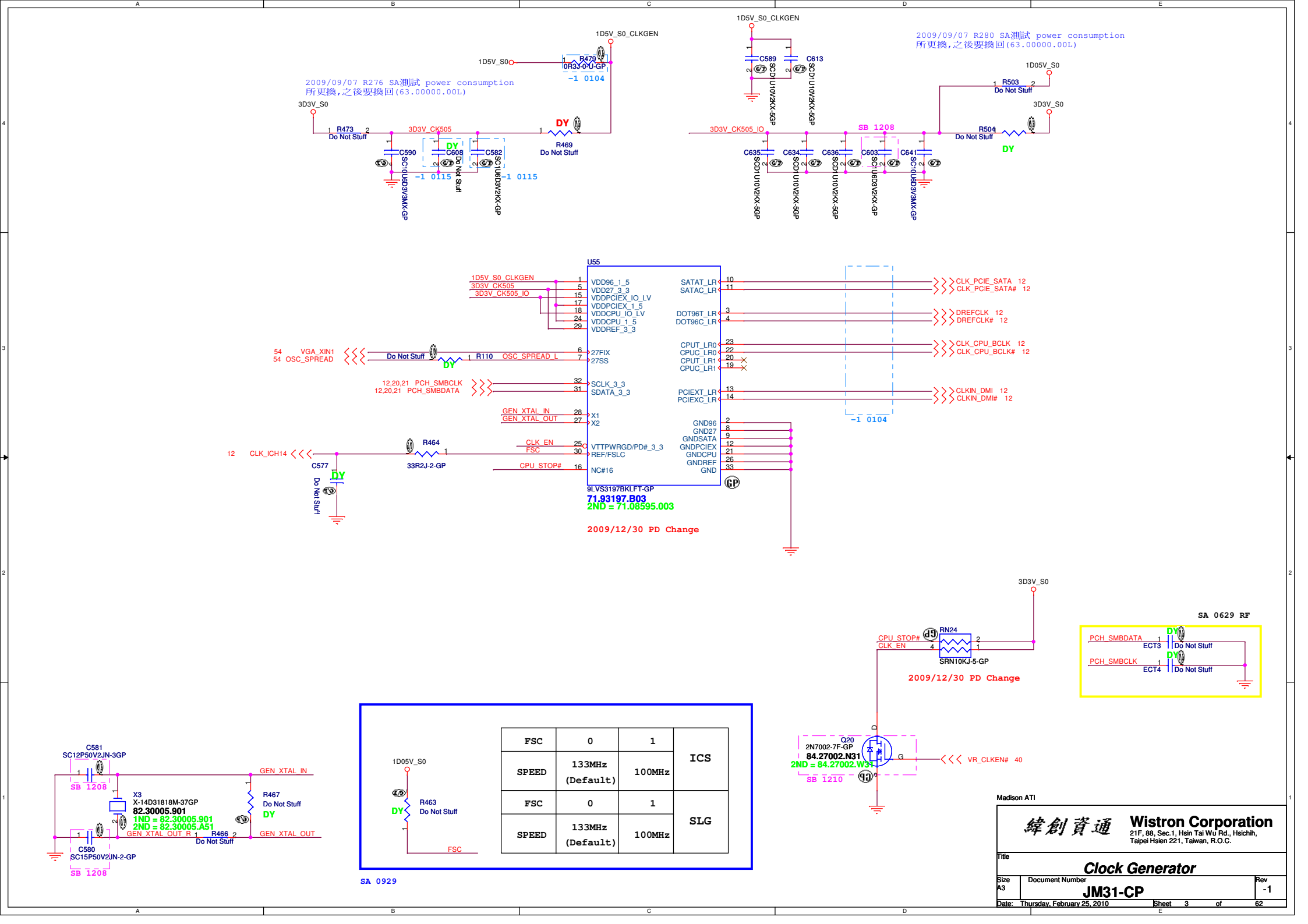
1D5V_S0_CLKGEN
1D5V_S0
R479
0R3J-0-U-GP
-1 0104
2009/09/07 R276 SA測試 power consumption
所更換,之後要換回(63.00000.00L)
3D3V_S0
R473
Do Not Stuff
3D3V_CK505
DY
R469
Do Not Stuff
C590
SC10U6D3V3MX-GP
C608
Do Not Stuff
C582
SC1U6D3V2KX-GP
-1 0115
-1 0115
C589
SCD1U10V2KX-5GP
C613
SCD1U10V2KX-5GP
2009/09/07 R280 SA測試 power consumption
所更換,之後要換回(63.00000.00L)
1D05V_S0
R503
Do Not Stuff
3D3V_S0
3D3V_CK505_IO
SB 1208
R504
Do Not Stuff
DY
C635
SCD1U10V2KX-5GP
C634
SCD1U10V2KX-5GP
C636
SCD1U10V2KX-5GP
C603
SC1U6D3V2KX-GP
C641
SC10U6D3V3MX-GP
U55
1D5V_S0_CLKGEN
3D3V_CK505
3D3V_CK505_IO
VDD96_1_5
VDD27_3_3
VDDPCIEX_IO_LV
VDDPCIEX_1_5
VDDCPU_IO_LV
VDDCPU_1_5
VDDREF_3_3
SATAT_LR
SATAC_LR
DOT96T_LR
DOT96C_LR
CPUT_LR0
CPUC_LR0
CPUT_LR1
CPUC_LR1
PCIEXT_LR
PCIEXC_LR
CLK_PCIE_SATA 12
CLK_PCIE_SATA# 12
DREFCLK 12
DREFCLK# 12
CLK_CPU_BCLK 12
CLK_CPU_BCLK# 12
CLKIN_DMI 12
CLKIN_DMI# 12
-1 0104
54 VGA_XIN1
54 OSC_SPREAD
Do Not Stuff
R110
OSC_SPREAD_L
27FIX
27SS
12,20,21 PCH_SMBCLK
12,20,21 PCH_SMBDATA
SCLK_3_3
SDATA_3_3
GEN_XTAL_IN
GEN_XTAL_OUT
X1
X2
CLK_EN
FSC
CPU_STOP#
VTTPWRGD/PD#_3_3
REF/FSLC
NC#16
GND96
GND27
GNDSATA
GNDPCIEX
GNDCPU
GNDREF
GND
9LVS3197BKLFT-GP
71.93197.B03
2ND = 71.08595.003
2009/12/30 PD Change
12 CLK_ICH14
R464
33R2J-2-GP
C577
DY
Do Not Stuff
3D3V_S0
CPU_STOP#
CLK_EN
RN24
SRN10KJ-5-GP
2009/12/30 PD Change
SA 0629 RF
PCH_SMBDATA
ECT3
PCH_SMBCLK
ECT4
Do Not Stuff
Q20
2N7002-7F-GP
84.27002.N31
2ND = 84.27002.W31
SB 1210
VR_CLKEN# 40
C581
SC12P50V2JN-3GP
SB 1208
X3
X-14D31818M-37GP
82.30005.901
1ND = 82.30005.901
2ND = 82.30005.A51
GEN_XTAL_IN
R467
Do Not Stuff
DY
GEN_XTAL_OUT_R
R466
Do Not Stuff
GEN_XTAL_OUT
C580
SC15P50V2JN-2-GP
SB 1208
1D05V_S0
R463
DY
Do Not Stuff
FSC
FSC 0 1 ICS
SPEED 133MHz (Default) 100MHz
FSC 0 1 SLG
SPEED 133MHz (Default) 100MHz
SA 0929
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Title
Clock Generator
Size A3
Document Number JM31-CP
Rev -1
Date: Thursday, February 25, 2010
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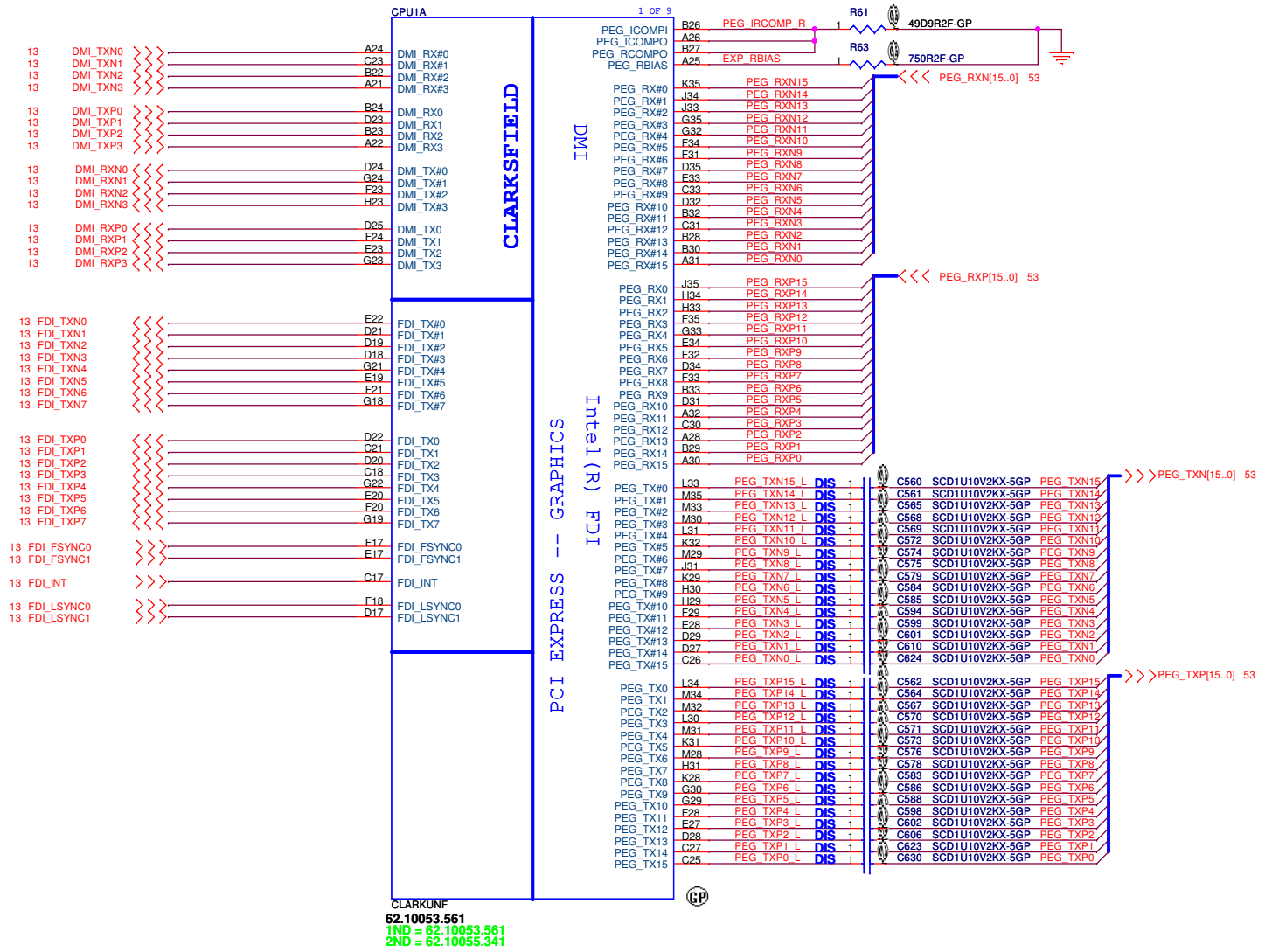

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Title: CPU (1/7)

Size	Document Number	Rev
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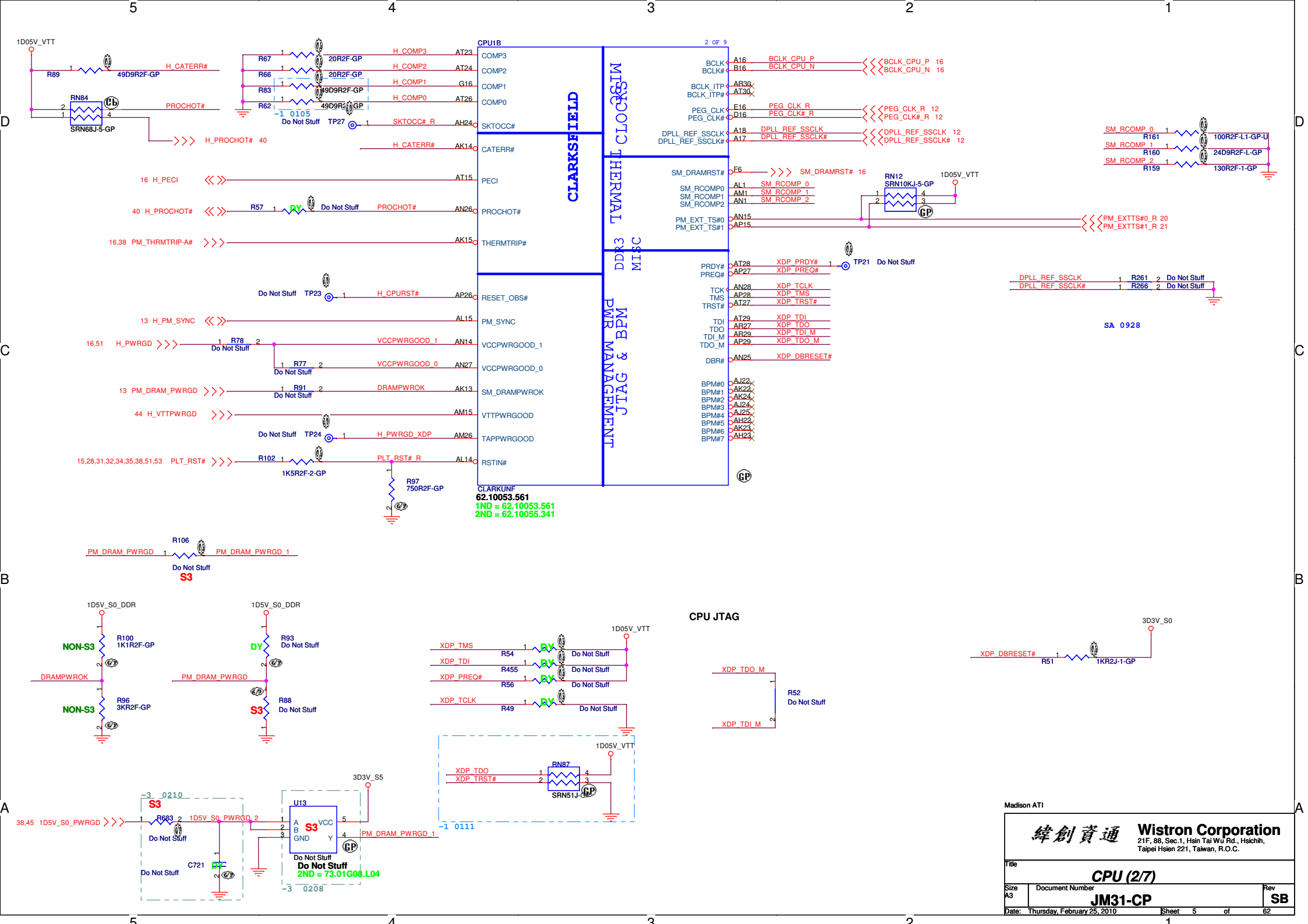
CPU1B
CLARKSFIELD
MISC THERMAL DDR3 MISC
JTAG & BPM PWR MANAGEMENT
CLARKUNF
62.10053.561
1ND = 62.10053.561
2ND = 62.10055.341
SA 0928
CPU JTAG
Madison ATI
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Title
CPU (2/7)
Size A3
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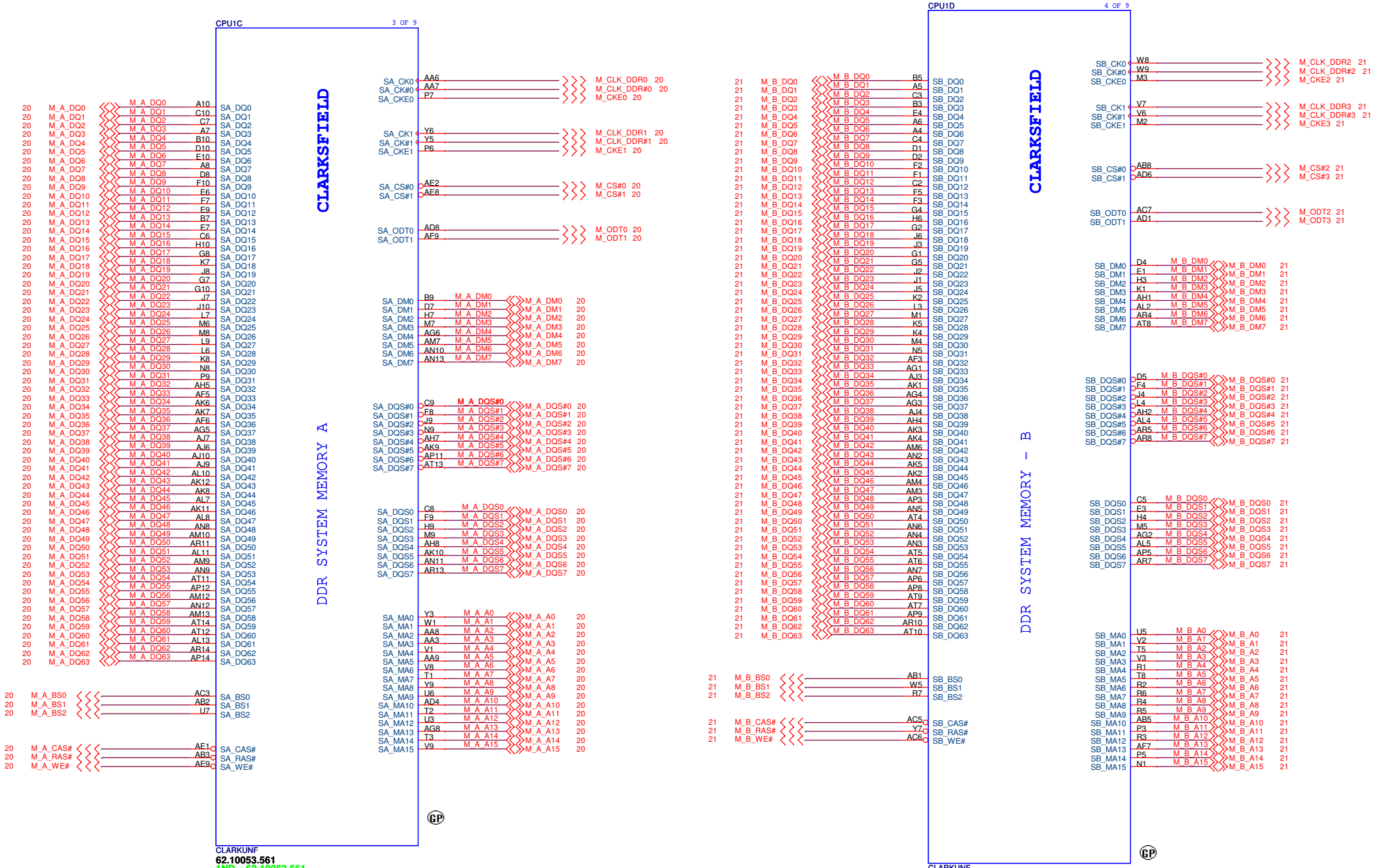

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Title: **CPU (3/7)**

Size	Document Number	Rev
A3	JM31-CP	SA

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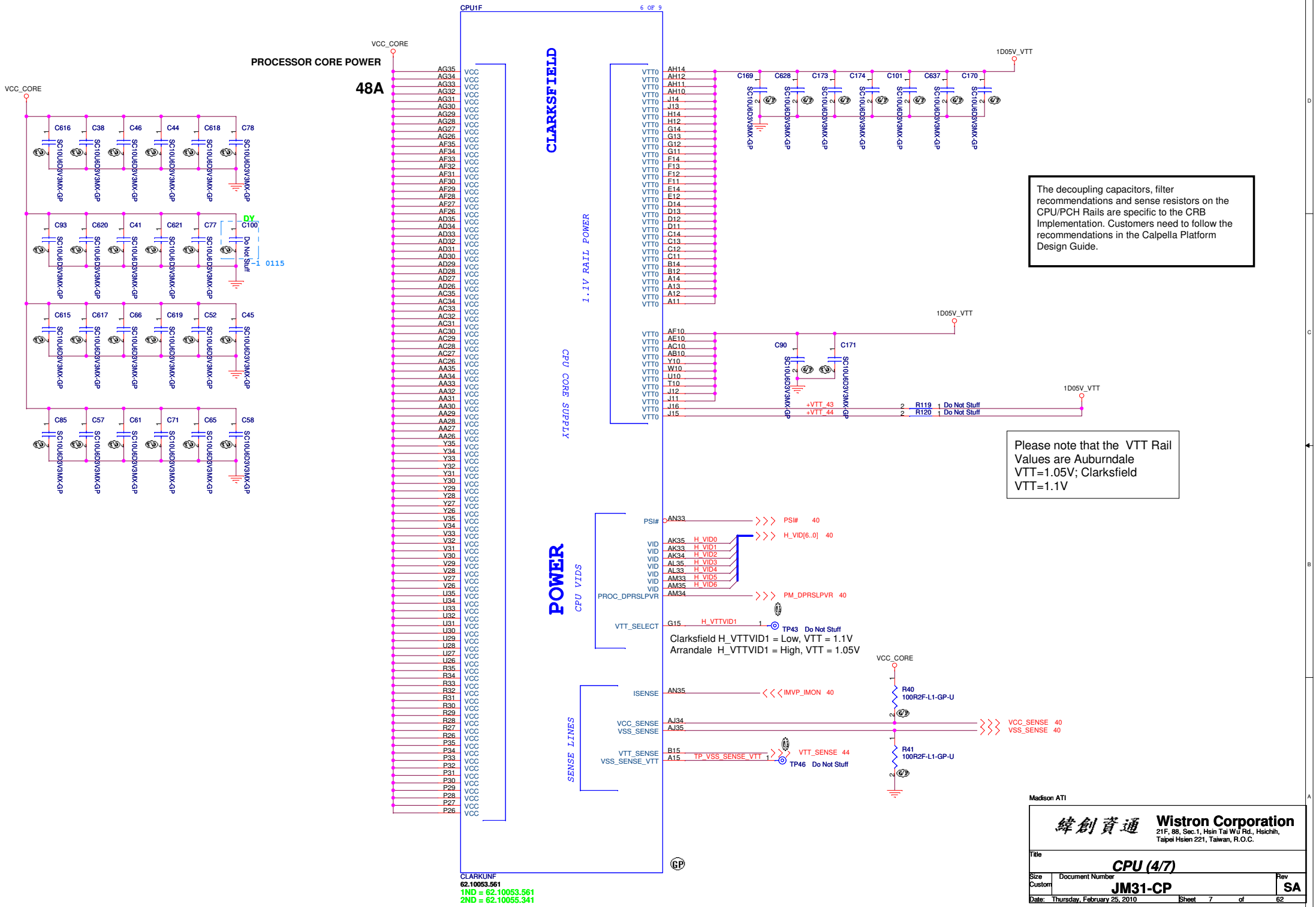
PROCESSOR CORE POWER
48A
VCC_CORE
CPU1F
6 OF 9
CLARKSFIELD
1.1V RAIL POWER
CPU CORE SUPPLY
POWER
CPU VIDS
SENSE LINES
1D05V_VTT
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V
CLARKUNF
62.10053.561
1ND = 62.10053.561
2ND = 62.10055.341
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Title
CPU (4/7)
Size
Custom
Document Number
JM31-CP
Rev
SA
Date: Thursday, February 25, 2010
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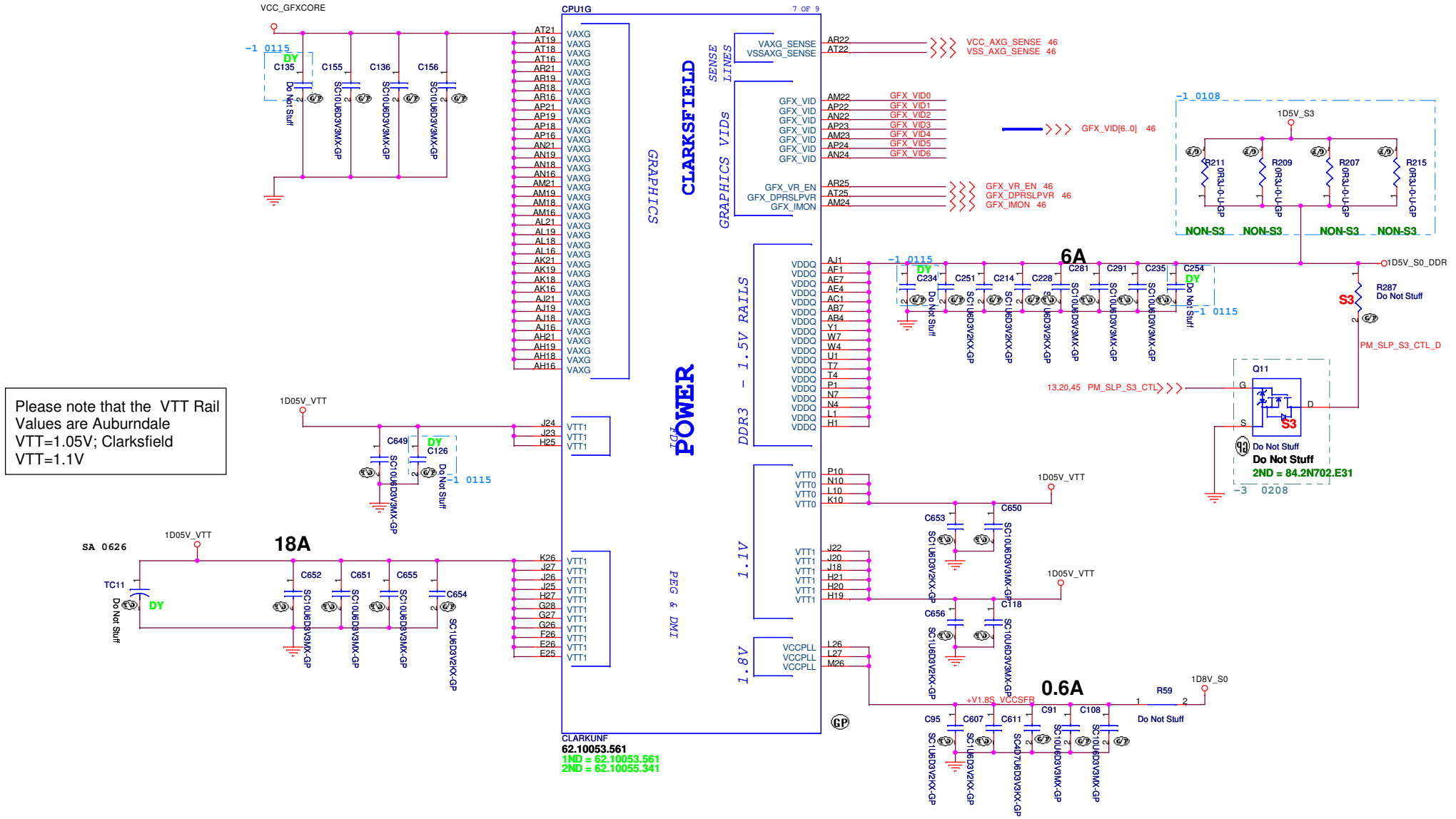
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
CPU1G
7 OF 9
CLARKSFIELD
POWER
GRAPHICS
SENSE LINES
GRAPHICS VIDs
DDR3 - 1.5V RAILS
1.1V
1.8V
PEG & DMI
VCC_GFXCORE
1D05V_VTT
1D5V_S3
1D5V_S0_DDR
1D8V_S0
VCC_AXG_SENSE 46
VSS_AXG_SENSE 46
GFX_VID[6..0] 46
GFX_VR_EN 46
GFX_DPRSLPVR 46
GFX_IMON 46
13,20,45 PM_SLP_S3_CTL
PM_SLP_S3_CTL_D
NON-S3
Do Not Stuff
Do Not Stuff
2ND = 84.2N702.E31
6A
18A
0.6A
SA 0626
CLARKUNF
62.10053.561
1ND = 62.10053.561
2ND = 62.10055.341
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Title
CPU (5/7)
Size A3
Document Number
JM31-CP
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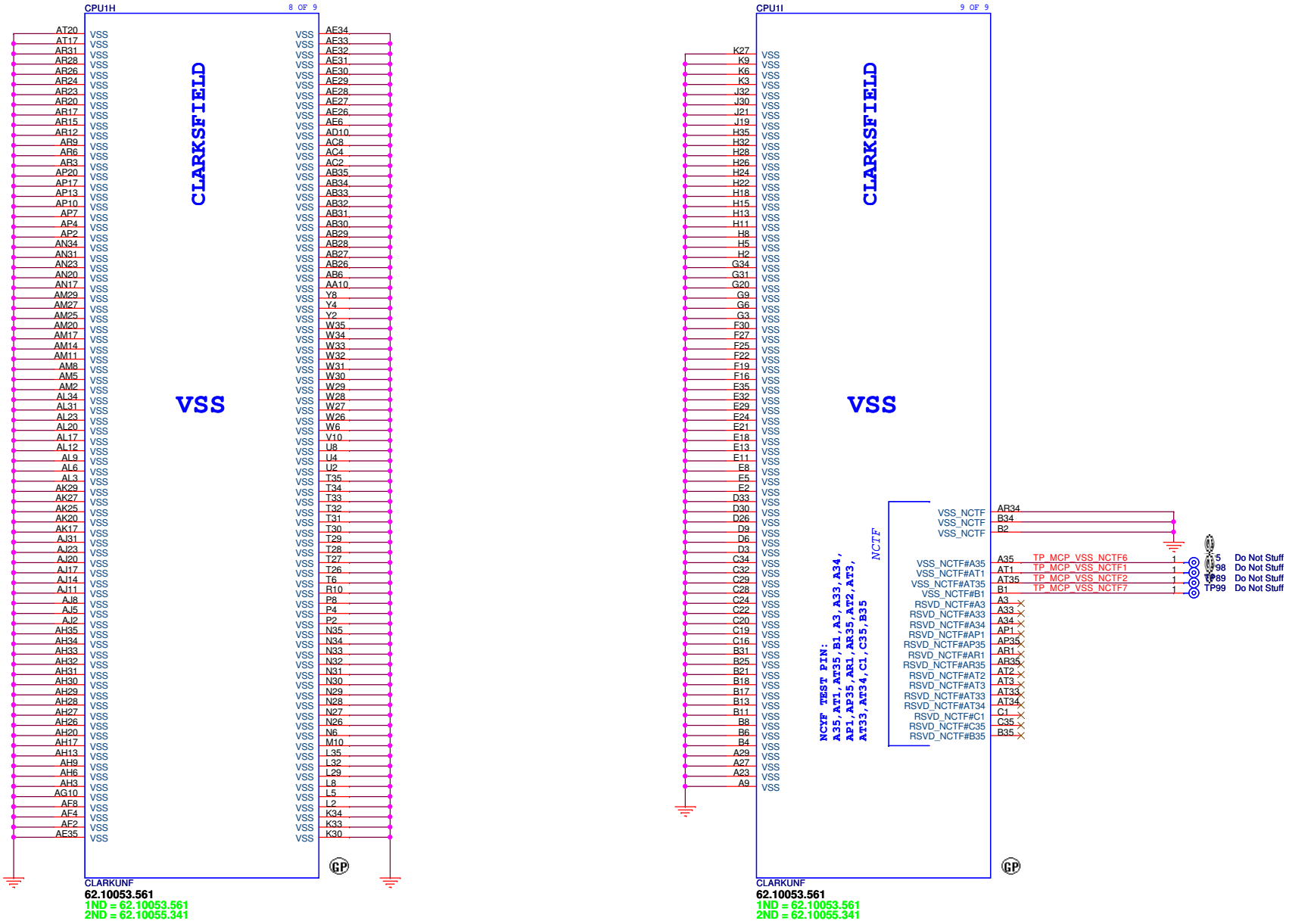

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Title: ***CPU (6/7)***

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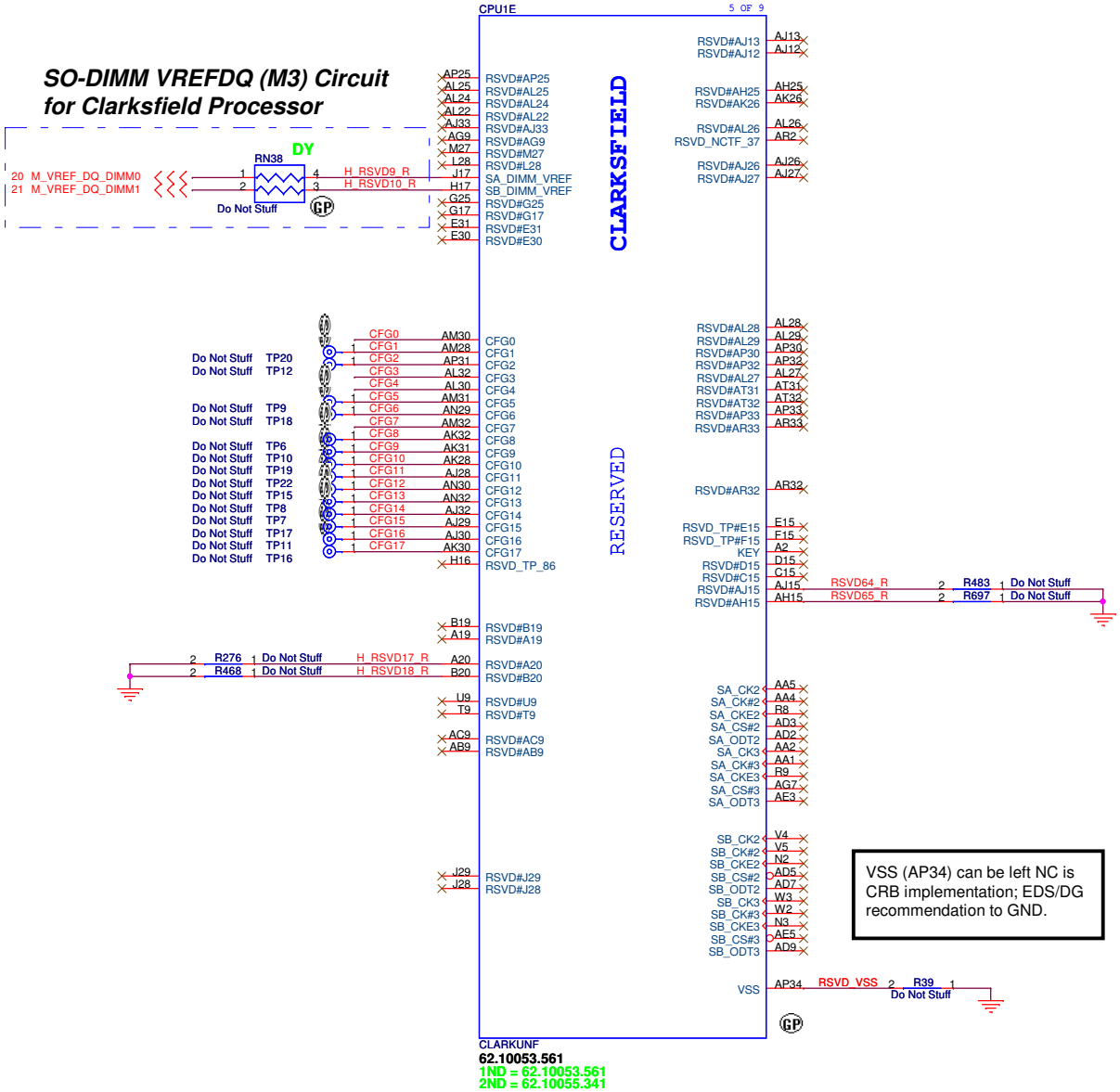
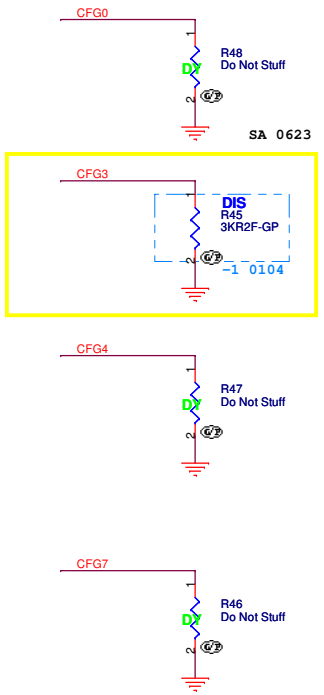
SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

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integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

SA 0709

When unused all JTAG pins may be NC

SA 0629 RF

SA 1012

SB 1105

SB 1202

SB 1208

SA 0930

SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required

SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"

PCH1A — 1 OF 10

IBEXPEAK-M-GP-NF
71.0IBEX.A0U
1ND = KI.G5501.002

HDD

BAS40CW-GP
83.00040.E81
1ND = 83.00040.E81
2nd = 83.00040.M81

BAT-CON2-1-GP-U
62.70001.011

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Title: **PCH (1/9)**

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LAN

MINICARD1

MINICARD2

PCH1B

2 OF 10

PCI-E*

SMBus

Controller Link

PEG

From CLK BUFFER

Clock Flex

IBEXPEAK-M-GP-NF

71.0IBEX.A0U

1ND = KI.G5501.002

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).

SA 0929

SA 1013

DIS

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Title: PCH (2/9)

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PCH1C

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DMI

4 DMI_RXN0	BC24	DMI0RXN	
4 DMI_RXN1	BJ22	DMI1RXN	
4 DMI_RXN2	AW20	DMI2RXN	
4 DMI_RXN3	BJ20	DMI3RXN	
4 DMI_RXP0	BD24	DMI0RXP	
4 DMI_RXP1	BG22	DMI1RXP	
4 DMI_RXP2	BA20	DMI2RXP	
4 DMI_RXP3	BG20	DMI3RXP	
4 DMI_TXN0	BE22	DMI0TXN	
4 DMI_TXN1	BF21	DMI1TXN	
4 DMI_TXN2	BD20	DMI2TXN	
4 DMI_TXN3	BE18	DMI3TXN	
4 DMI_TXP0	BD22	DMI0TXP	
4 DMI_TXP1	BH21	DMI1TXP	
4 DMI_TXP2	BC20	DMI2TXP	
4 DMI_TXP3	BD18	DMI3TXP	

1D05V_S0

R622 1 — 2 49D9R2F-GP

DMI_IRCOMP_R — BH25 DMI_ZCOMP — BF25 DMI_IRCOMP

FDI

FDI_RXN0	BA18	FDI_TXN0 4
FDI_RXN1	BH17	FDI_TXN1 4
FDI_RXN2	BD16	FDI_TXN2 4
FDI_RXN3	BJ16	FDI_TXN3 4
FDI_RXN4	BA16	FDI_TXN4 4
FDI_RXN5	BE14	FDI_TXN5 4
FDI_RXN6	BA14	FDI_TXN6 4
FDI_RXN7	BC12	FDI_TXN7 4
FDI_RXP0	BB18	FDI_TXP0 4
FDI_RXP1	BF17	FDI_TXP1 4
FDI_RXP2	BC16	FDI_TXP2 4
FDI_RXP3	BG16	FDI_TXP3 4
FDI_RXP4	AW16	FDI_TXP4 4
FDI_RXP5	BD14	FDI_TXP5 4
FDI_RXP6	BB14	FDI_TXP6 4
FDI_RXP7	BD12	FDI_TXP7 4
FDI_INT	BJ14	FDI_INT 4
FDI_FSYNC0	BF13	FDI_FSYNC0 4
FDI_FSYNC1	BH13	FDI_FSYNC1 4
FDI_LSYNC0	BJ12	FDI_LSYNC0 4
FDI_LSYNC1	BG14	FDI_LSYNC1 4

12 SUS_PWR_DN_ACK_R >>> SUS_PWR_DN_ACK_R

System Power Management

16 PM_SYSRST#_R <<< PM_SYSRST#_R — T6 SYS_RESET#

38 PM_PWROK >>> R64 1 — DY — 2 Do Not Stuff — M6 SYS_PWROK

38,40 CORE_PWRGD >>> R65 1 — 2 Do Not Stuff — PM_PWROK_1 — B17 PWROK

R522 1 — 2 10KR2J-3-GP

38,40,43,44 ALL_PWRGD >>> ALL_PWRGD — R517 1 — DY — 2 Do Not Stuff — ME_PWROK — K5 MEPWROK

R523 1 — 2 Do Not Stuff

R492 1 — 2 10KR2J-3-GP — LAN_RST#1 — A10 LAN_RST#

5 PM_DRAM_PWRGD <<< PM_DRAM_PWRGD — D9 DRAMPWROK

PM_RSMRST# — C16 RSMRST#

34 SUS_PWR_DN_ACK <<< R194 1 — 2 Do Not Stuff — SUS_PWR_DN_ACK_R — M1 SUS_PWR_DN_ACK/GPIO30

34,51 PM_PWRBTN# >>> R587 1 — 2 Do Not Stuff — PM_PWRBTN#_R — P5 PWRBTN#

34 AC_PRESENT >>> R579 1 — 2 Do Not Stuff — AC_PRESENT_R — P7 ACPRESENT/GPIO31

12 PCH_GPIO72 >>> A6 BATLOW#/GPIO72

PM_RI# >>> PM_RI# — F14 RI#

WAKE#	J12	PCIE_WAKE# >>> PCIE_WAKE# 31,32
CLKRUN#/GPIO32	Y1	PM_CLKRUN# <<< PM_CLKRUN# 15,34
SUS_STAT#/GPIO61	P8	PM_SUS_STAT# 1 — TP71 Do Not Stuff
SUSCLK/GPIO62	F3	PM_SUS_CLK >>> PM_SUS_CLK 34 — SA 1003
SLP_S5#/GPIO63	E4	PM_SLP_S5# 1 — TP54 Do Not Stuff
SLP_S4#	H7	PM_SLP_S4#_R — R99 1 — 2 Do Not Stuff >>> PM_SLP_S4# 34,43,45
SLP_S3#	P12	PM_SLP_S3#_R — R525 1 — 2 Do Not Stuff >>> PM_SLP_S3# 34,38,43,44,45,46
SLP_M#	K8	PM_SLP_M#_R — R94 1 — 2 Do Not Stuff >>> PM_SLP_M# 34
TP23	N2	PM_SLP_DSW# 1 — TP93 Do Not Stuff
PMSYNCH	BJ10	H_PM_SYNC <<< H_PM_SYNC 5
SLP_LAN#/GPIO29	F6	PM_SLP_LAN# 1 — TP64 Do Not Stuff

IBEXPEAK-M-GP-NF

71.0IBEX.A0U

1ND = KI.G5501.002

3D3V_S5

R681 1 — 1KR2F-3-GP — 16

R680 1 — DY — 2 Do Not Stuff

SA1016

DY D21 — Do Not Stuff

34 RSMRST#_KBC >>> 3

PM_RSMRST# — PM_RSMRST# 16

SB 1202

R480 1 — 2 100KR2J-1-GP

Do Not Stuff

1ND = 83.00054.T81

2ND = 83.BAT54.D81

SA0922

3D3V_AUX_S5

R675 1 — 10KR2J-3-GP

R679 1 — 100KR2J-1-GP

Q51

PM_RSMRST# — 3

51123_PGOOD — 2

51123_PGOOD 42

2N7002KDW-GP

84.2N702.A3F

2ND = 84.DM601.03F

SB 1117

12 PCIE_CLK_RQ0# <<< PCIE_CLK_RQ0# — 1

AC_PRESENT_R — 2

PM_PWRBTN#_R — 3

16 PCH_GPIO28 <<< PCH_GPIO28 — 4

RN16 — 8 7 6 5

SRN10KJ-GP

SA 0929

3D3V_S5

PCIE_WAKE# — R518 1 — 2 1KR2J-1-GP

3D3V_S5

R547 1 — 2 Do Not Stuff

PM_SLP_S3# — Q25 G — S3 — D — S

PM_SLP_S3_CTL 8,20,45

Do Not Stuff

Do Not Stuff

2ND = 84.2N702.E31

-3 0208

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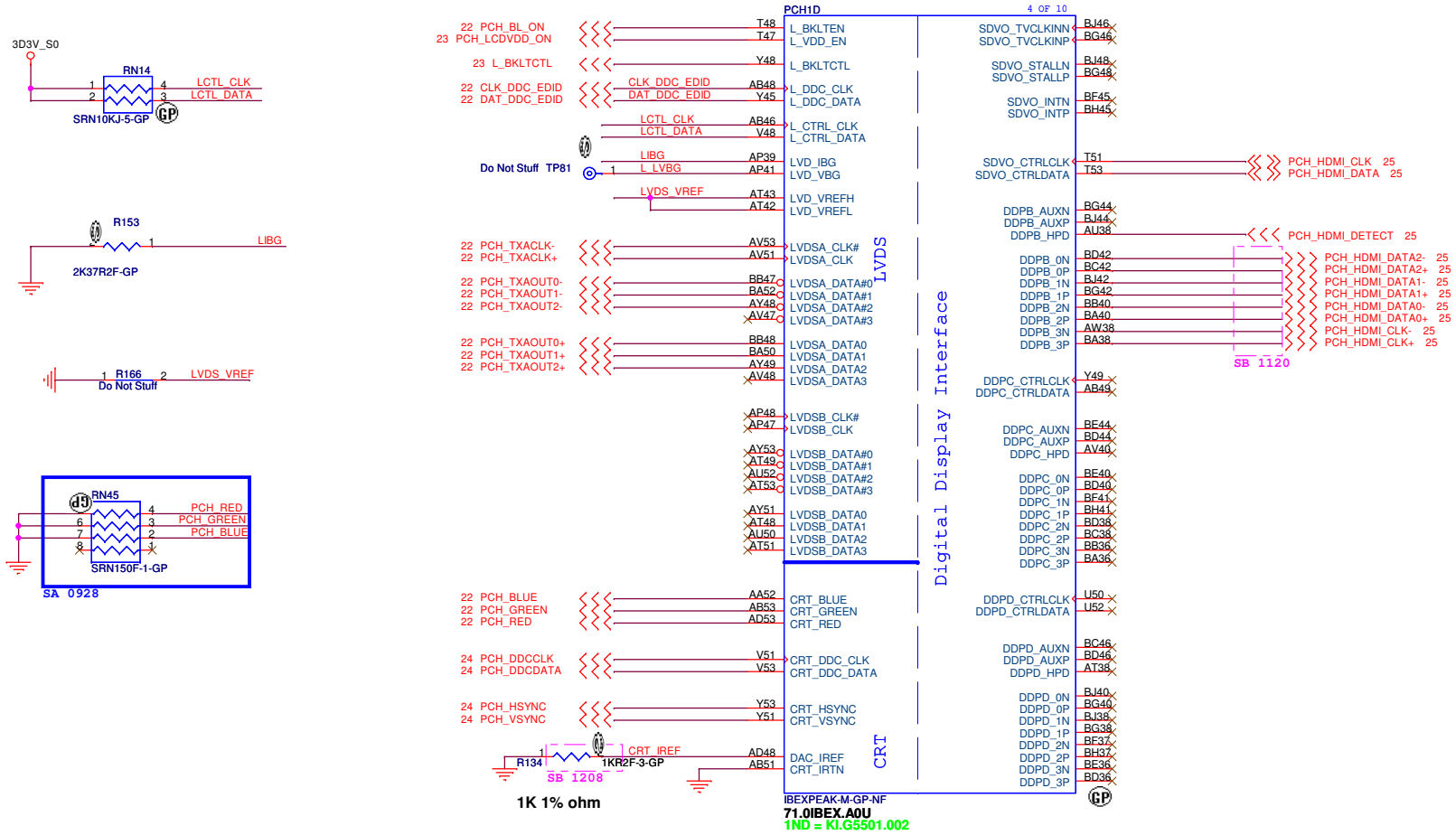
Title	PCH (3/9)	
Size A3	Document Number JM31-CP	Rev -3
Date: Thursday, February 25, 2010	Sheet 13 of 62	



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Title: ***PCH (4/9)***

Size	Document Number	Rev
A3	JM31-CP	SB

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These pins are left as NC, because the function is disable.

These pins are left as NC, because the function is disable.

PCH1E

5 OF 10

NVRAM

PCI

USB

IBEXPEAK-M-GP-NF

71.0IBEX.A0U

1ND = KI.G5501.002

SA 0929

RN10

SRN8K2J-2-GP

SA 0929

RN42

SRN8K2J-2-GP

SA 0929

RN35

SRN8K2J-4-GP

DIS

R487

2K2R2J-2-GP

SA1006

USE SPI

R519 Do Not Stuff

R98 Do Not Stuff

R163 Do Not Stuff

R165 Do Not Stuff

R167 Do Not Stuff

R74 22D6R2F-L1-GP

SA1005

RN7

SRN10KJ-6-GP

R529 22R2J-2-GP

R531 22R2J-2-GP

R108 33R2J-2-GP

SB 1125

Do Not Stuff TP65

Do Not Stuff TP95

Do Not Stuff TP67

R521 Do Not Stuff

C625 Do Not Stuff

U57

R515 Do Not Stuff

R512 Do Not Stuff

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:
Disabled when Low.
Enable when High.

USB

Pair	Device
0	EXT USB1
1	USB1(on board)
2	EXT USB2
3	MINICARD1
4	WECAM
5	SIM Card
6	NC
7	NC
8	NC
9	NC
10	NC
11	Blue Tooth
12	MINIC2
13	Cardreader

BOOT BIOS Strap

PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

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Title: PCH (5/9)

Size: A3 | Document Number: JM31-CP | Rev: SB

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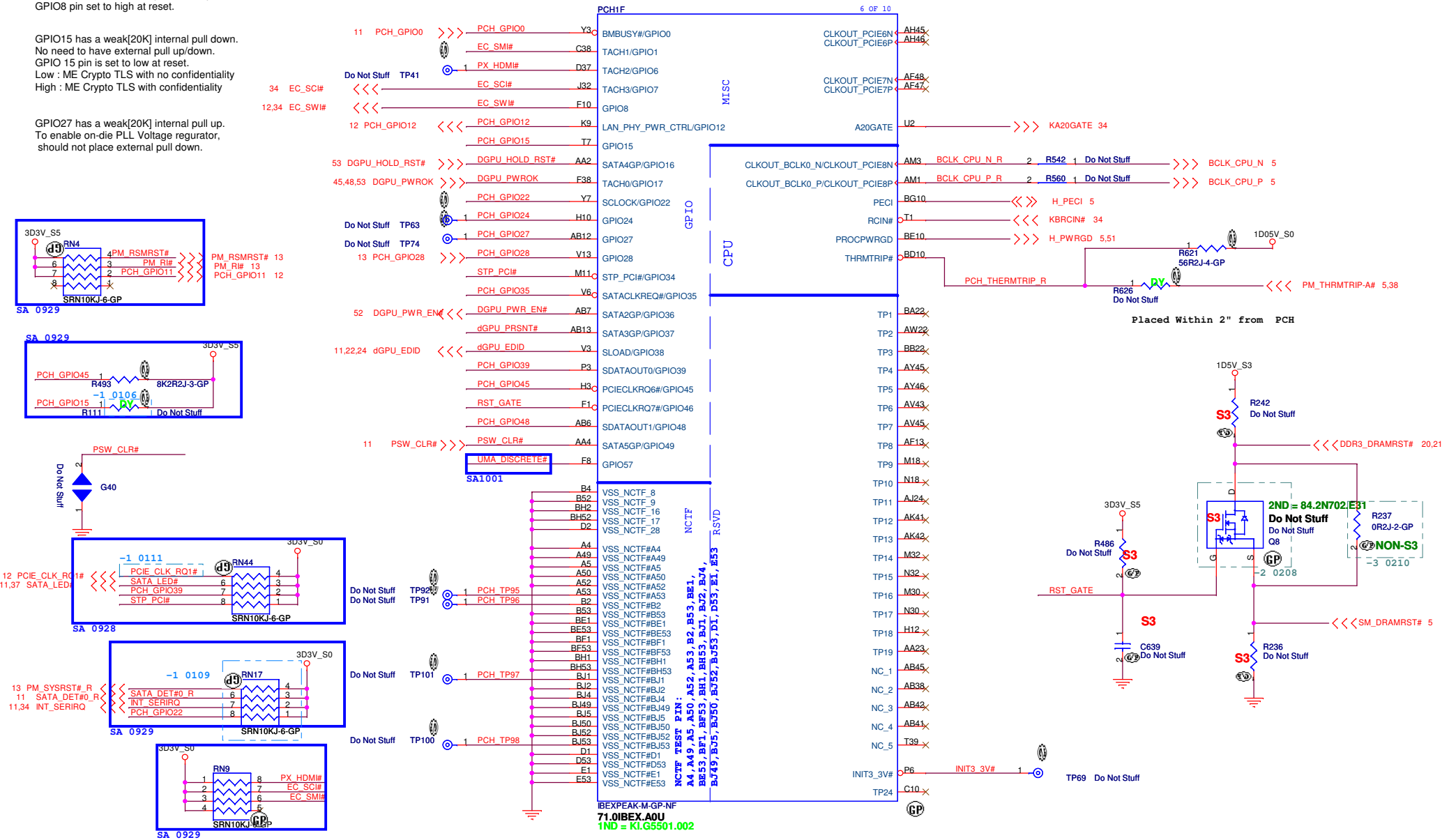
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.



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Title: PCH (6/9)

Size	Document Number	Rev
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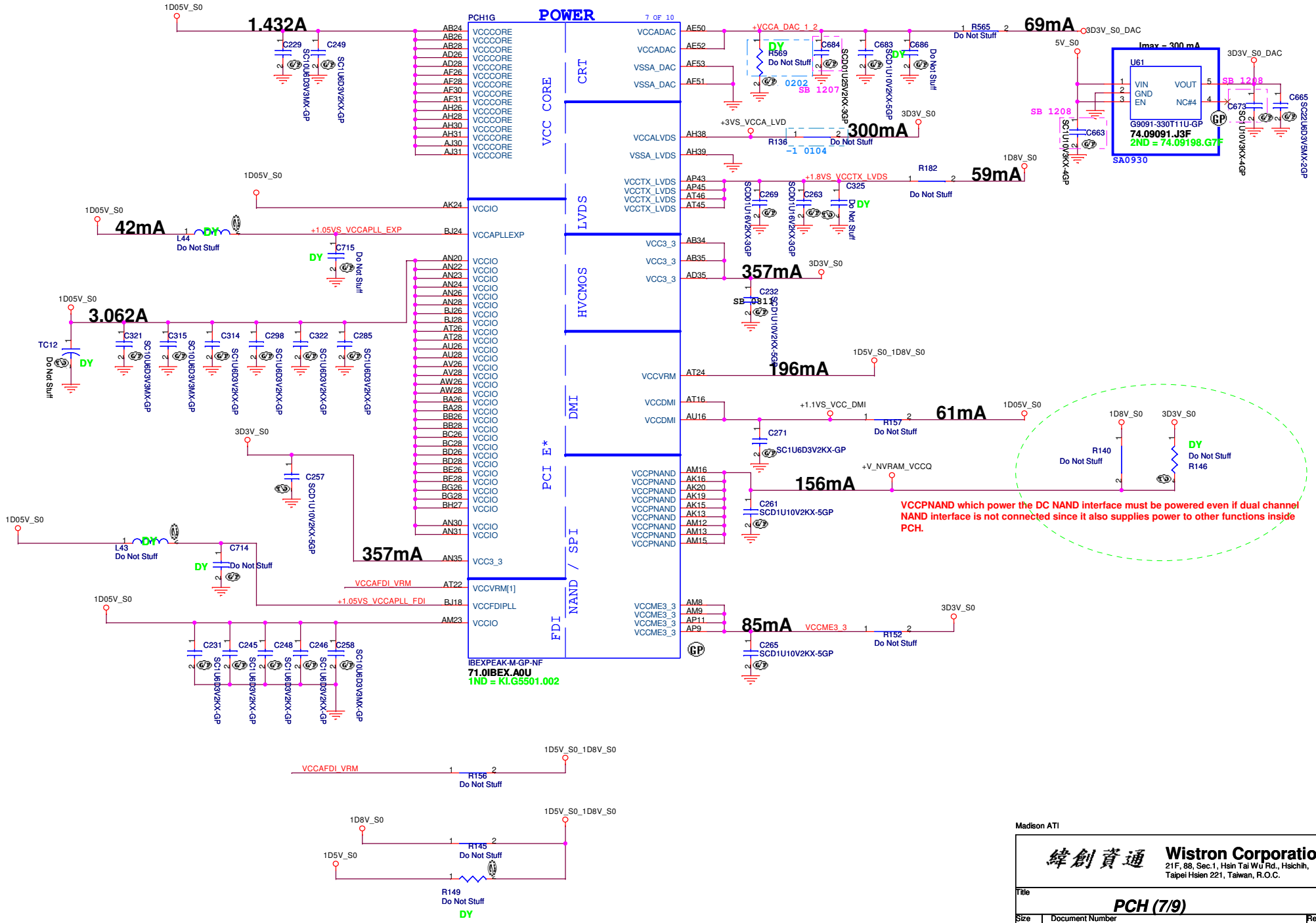

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Title	PCH (7/9)	
Size A3	Document Number JM31-CP	Rev -1
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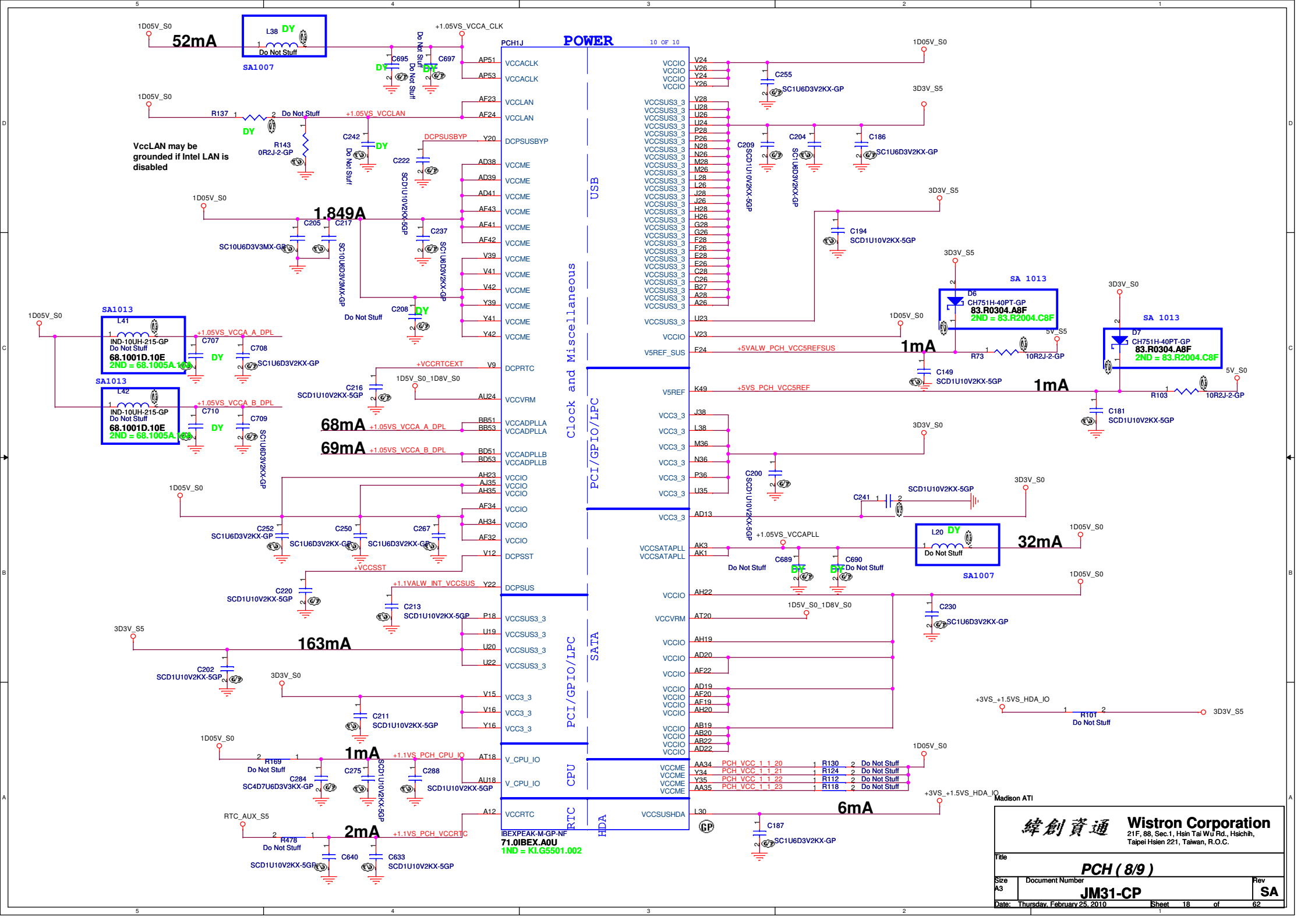
POWER
10 OF 10
PCH1J
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
52mA
1.849A
68mA
69mA
163mA
1mA
2mA
32mA
6mA
SA1007
SA1013
VccLAN may be grounded if Intel LAN is disabled
IBEXPEAK-M-GP-NF
71.0IBEX.A0U
1ND = KI.G5501.002
Madison ATI
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (8/9)
Size A3
Document Number
JM31-CP
Rev SA
Date: Thursday, February 25, 2010
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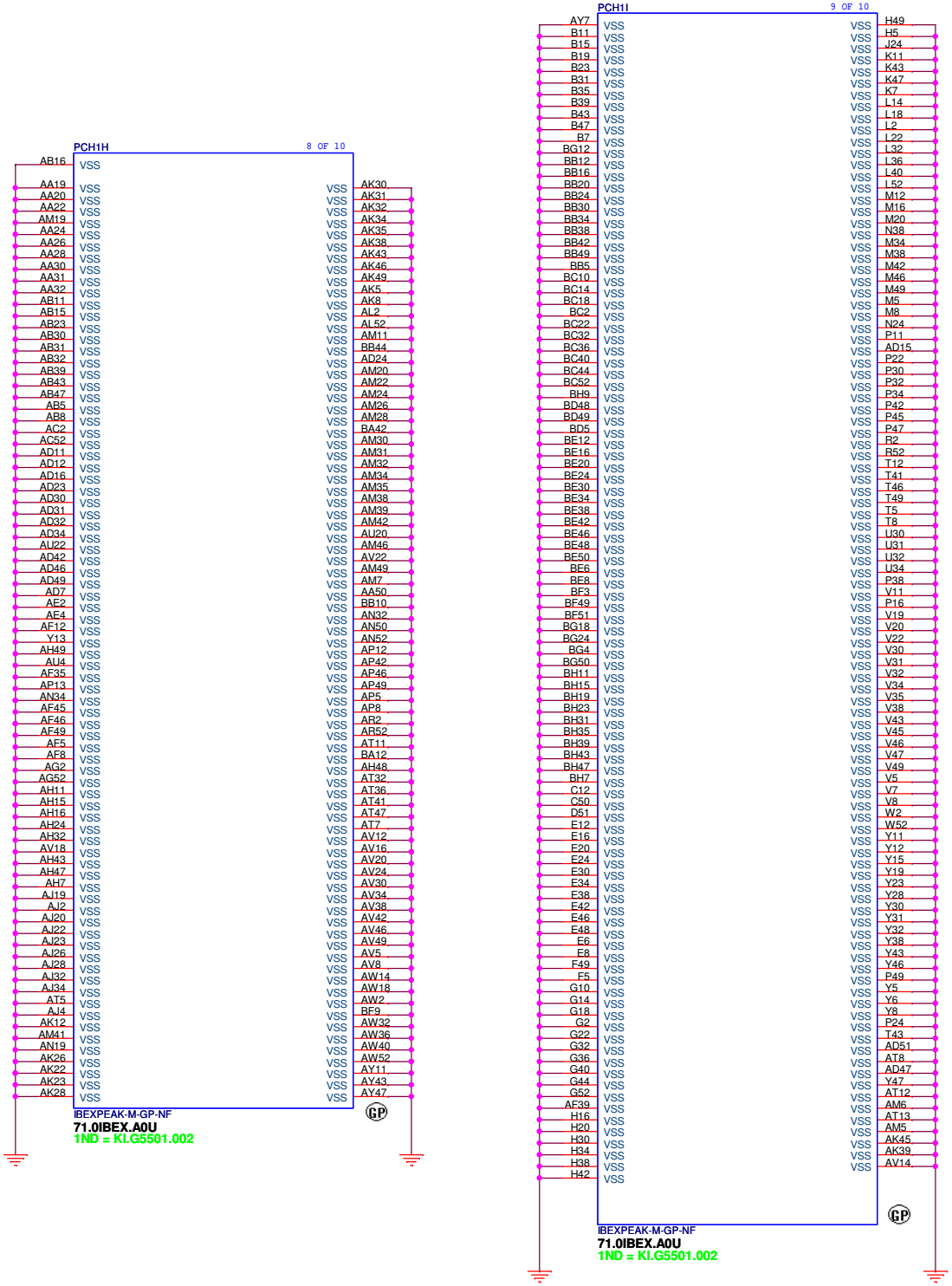

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Title: ***PCH (9/9)***

Size	Document Number	Rev
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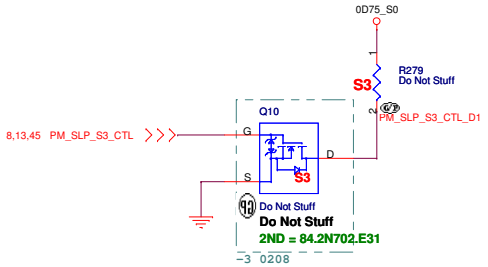
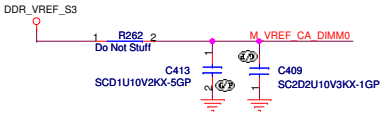
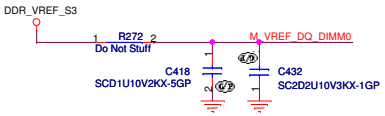
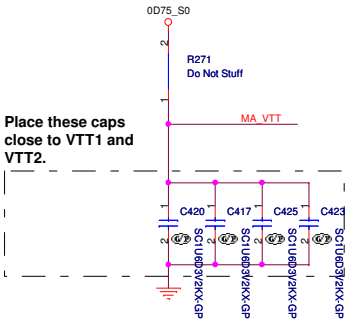


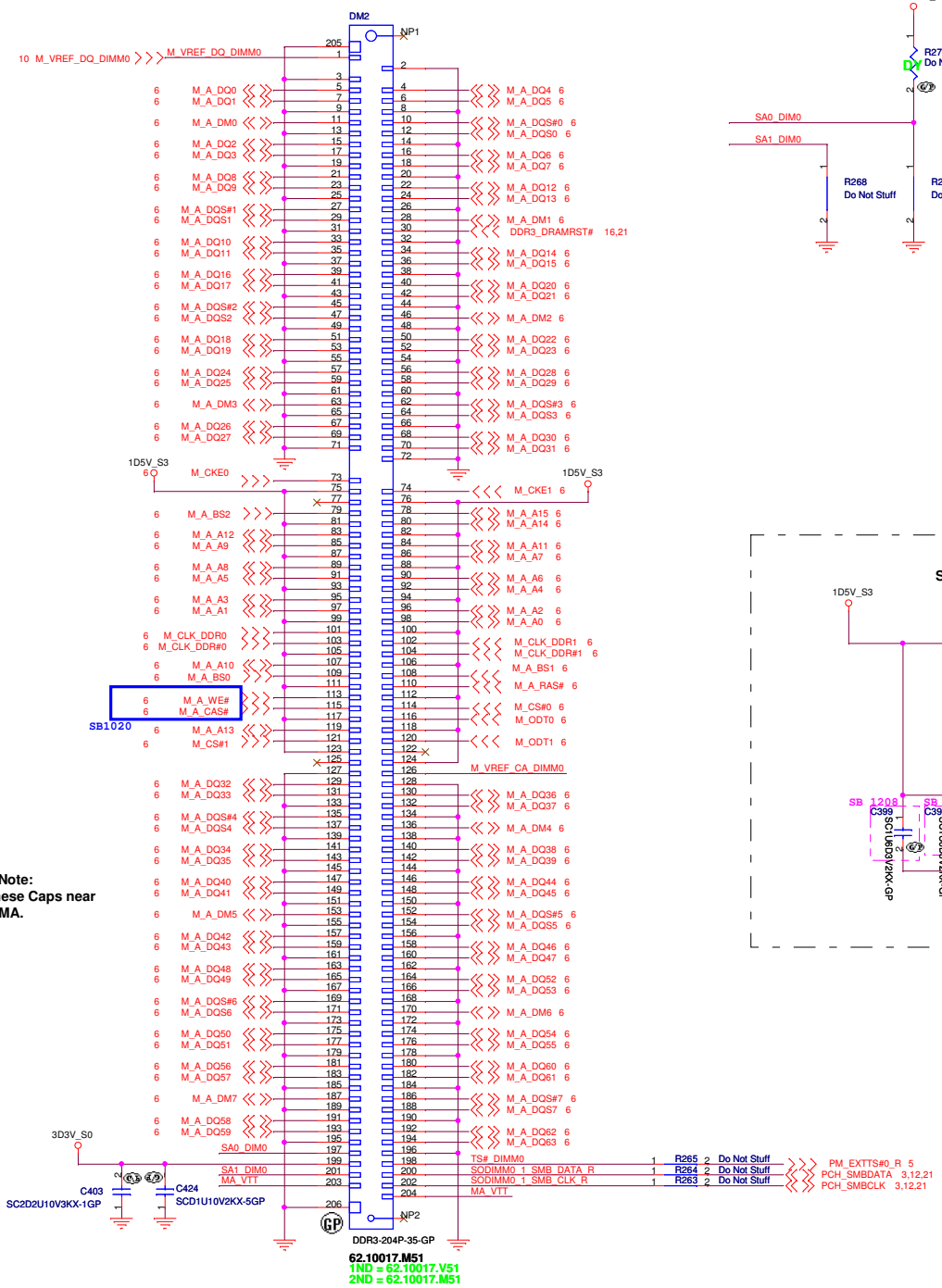


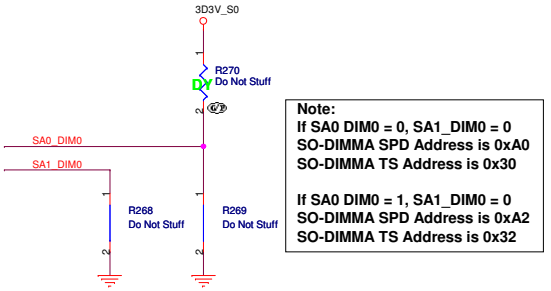




Place these caps close to VTT1 and VTT2.

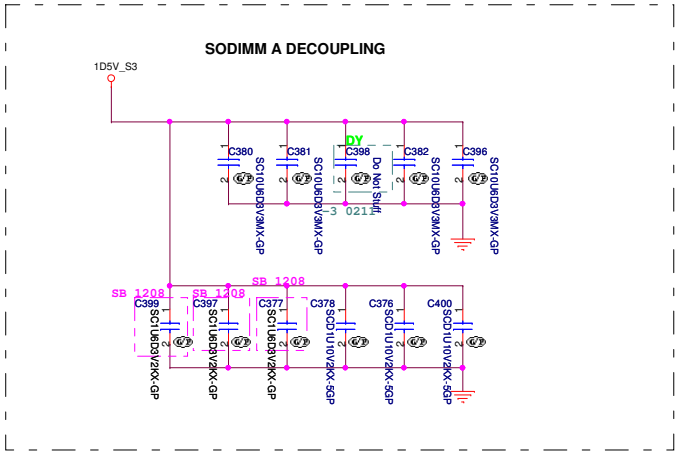
Layout Note: Place these Caps near SO-DIMMA.





Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



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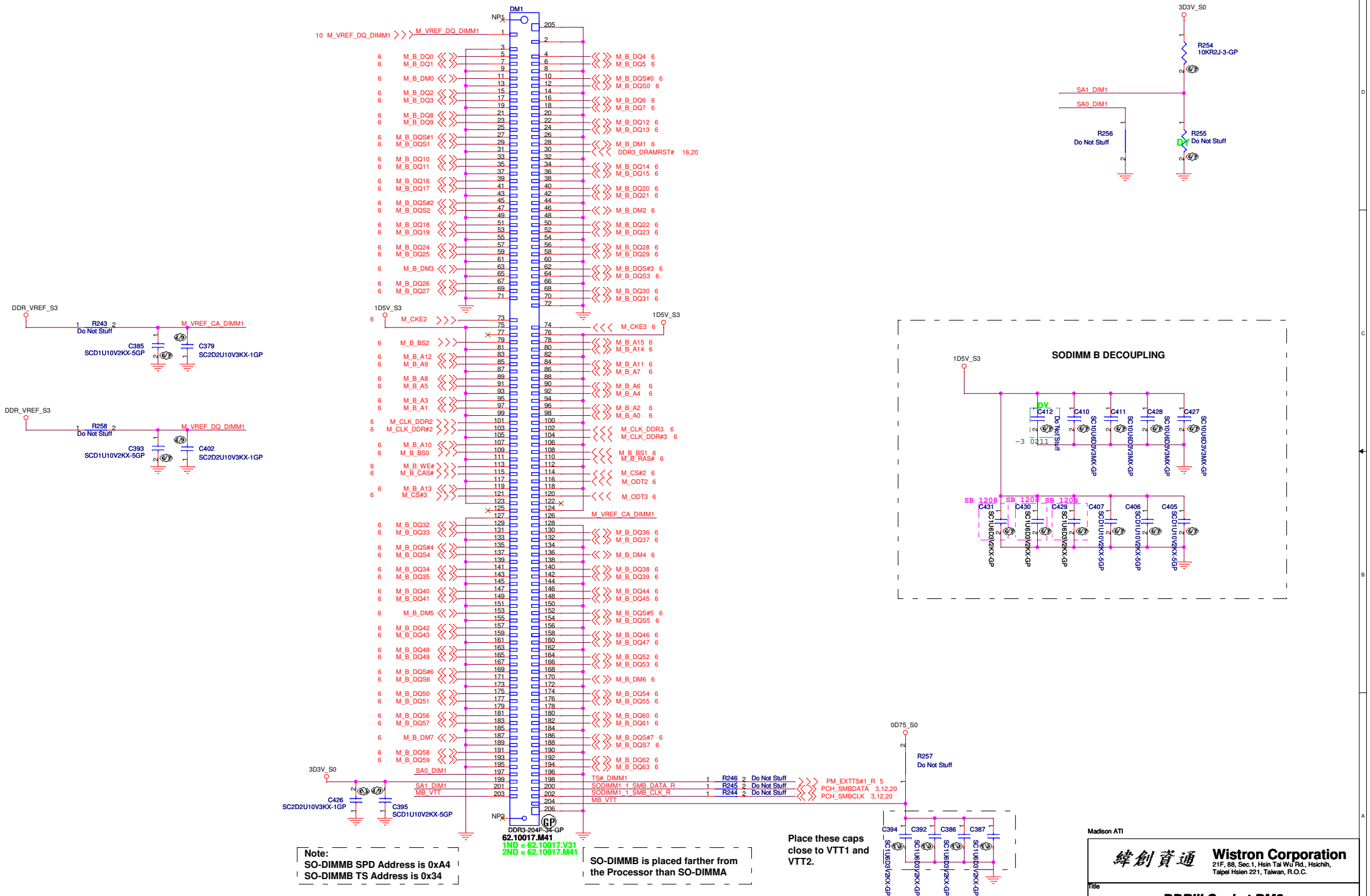
Title: DDRIII Socket DM1

Size	Document Number	Rev
Custom	JM31-CP	-3

Date: Thursday, February 25, 2010 Sheet 20 of 62



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Title: **DDRIII Socket DM2**

Size	Document Number	Rev
Custom	JM31-CP	SA

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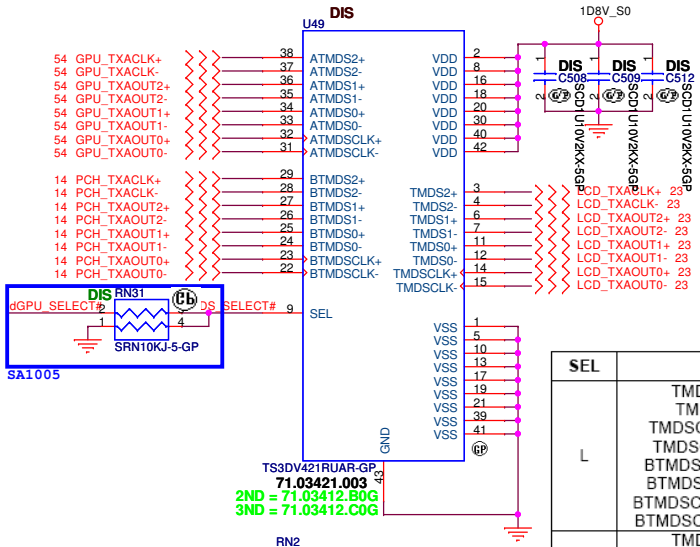


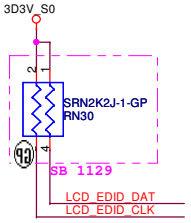
FUNCTION TABLE

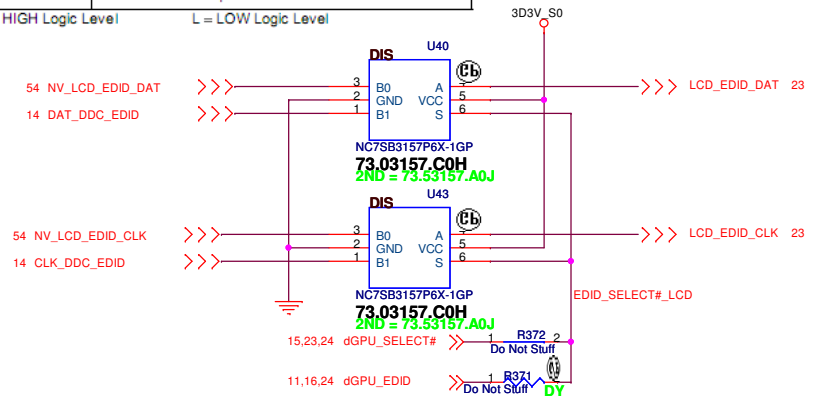
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level

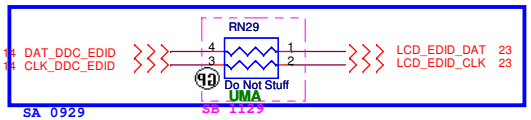


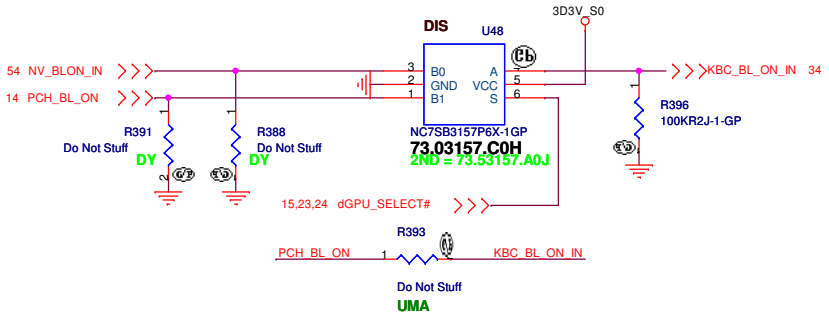


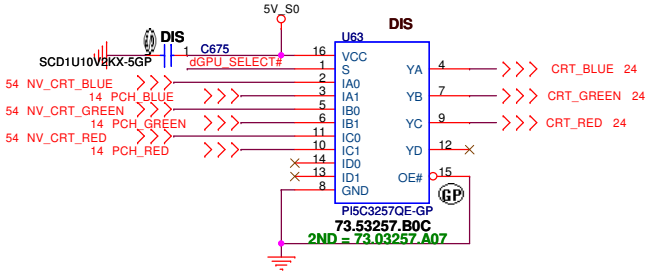
Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

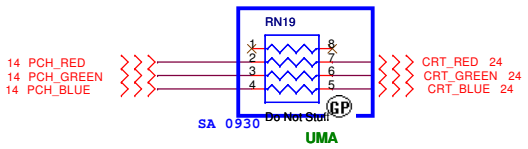
H = HIGH Logic Level L = LOW Logic Level







$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1



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Title: PX SWITCH

Size	Document Number	Rev
A3	JM31-CP	SB

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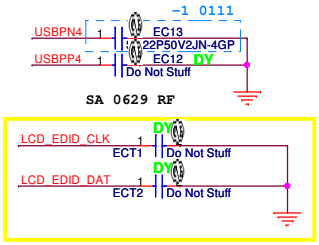
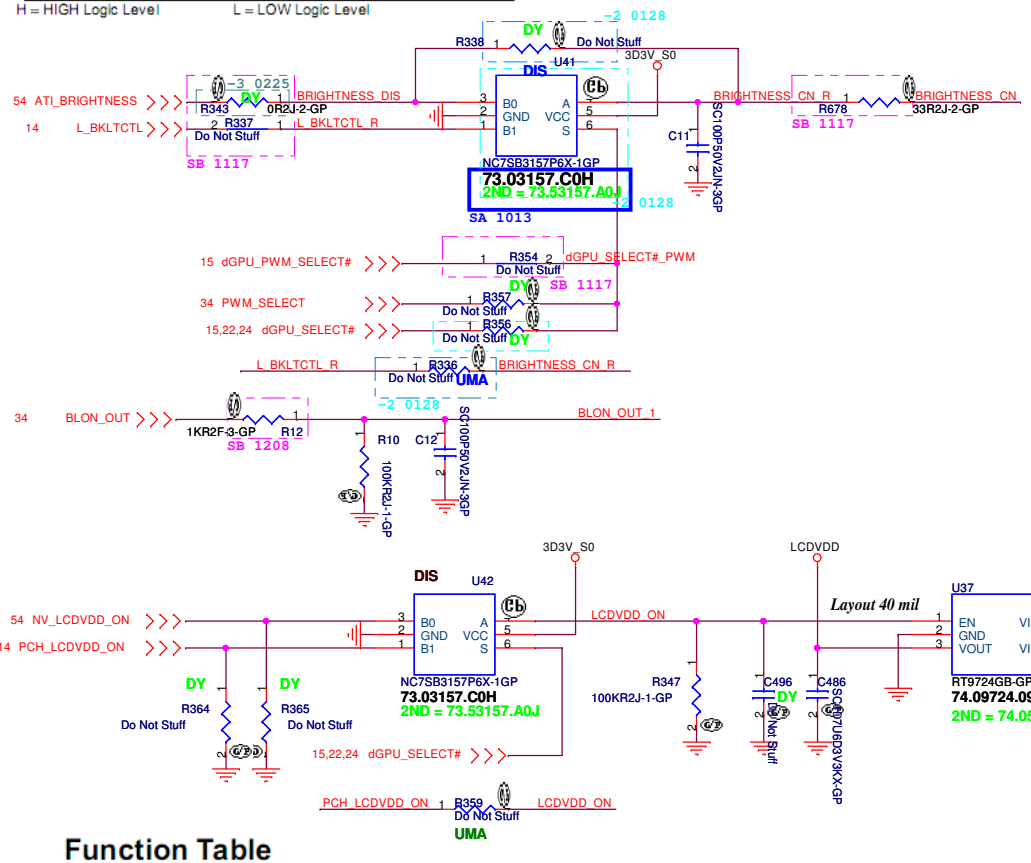
LCD/INVERTER/CCD CONN



Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

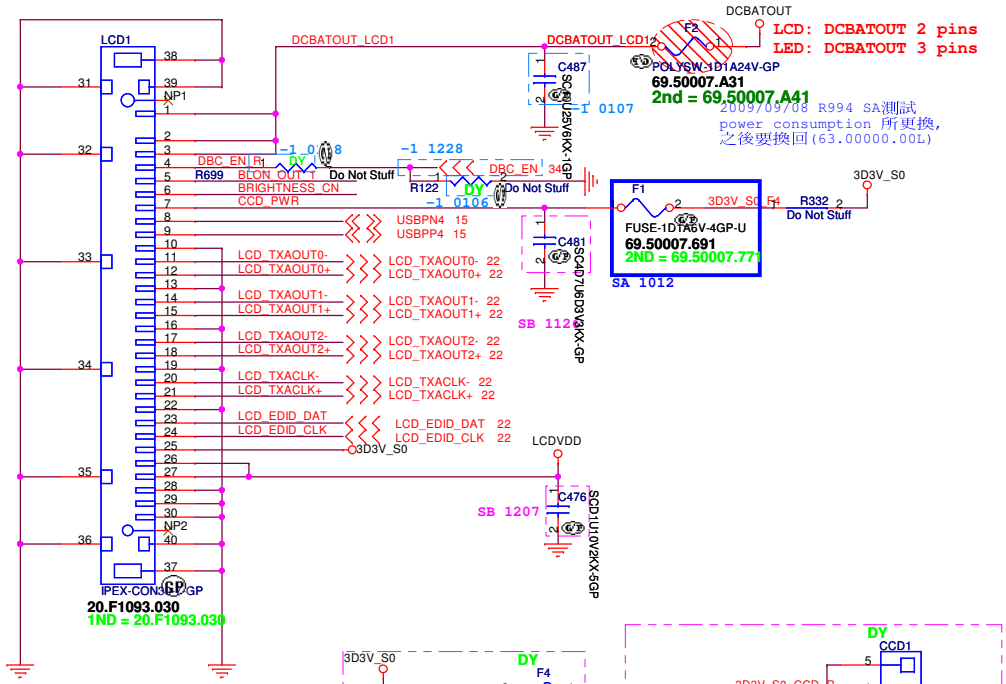
H = HIGH Logic Level L = LOW Logic Level



Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level



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Title: **LCD CONN**

Size	Document Number	Rev
A3	JM31-CP	-1

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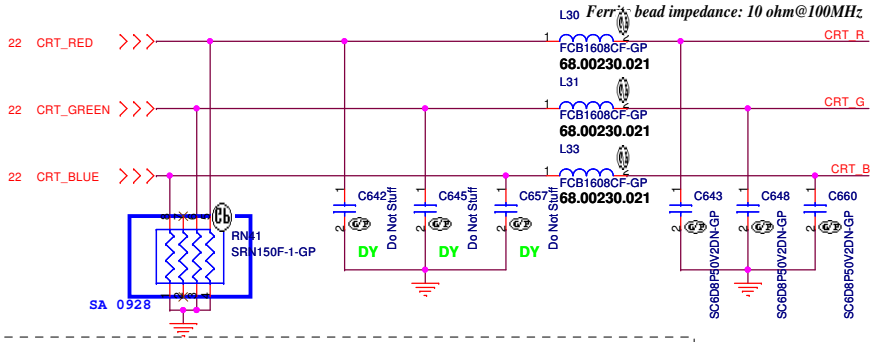
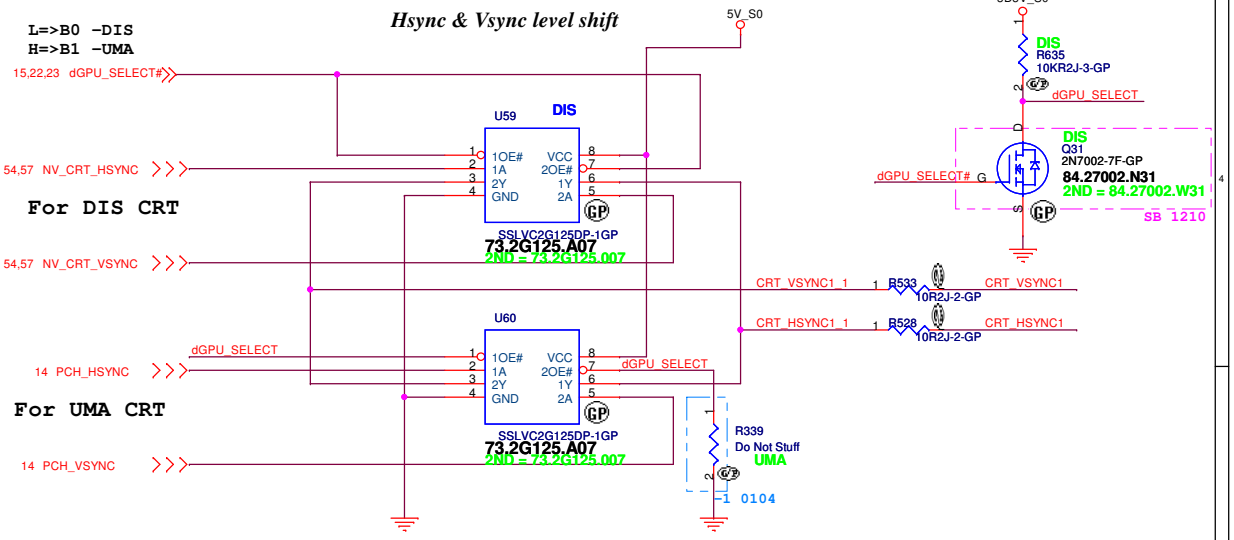
Layout Note:
Place these resistors close to the CRT-out connector

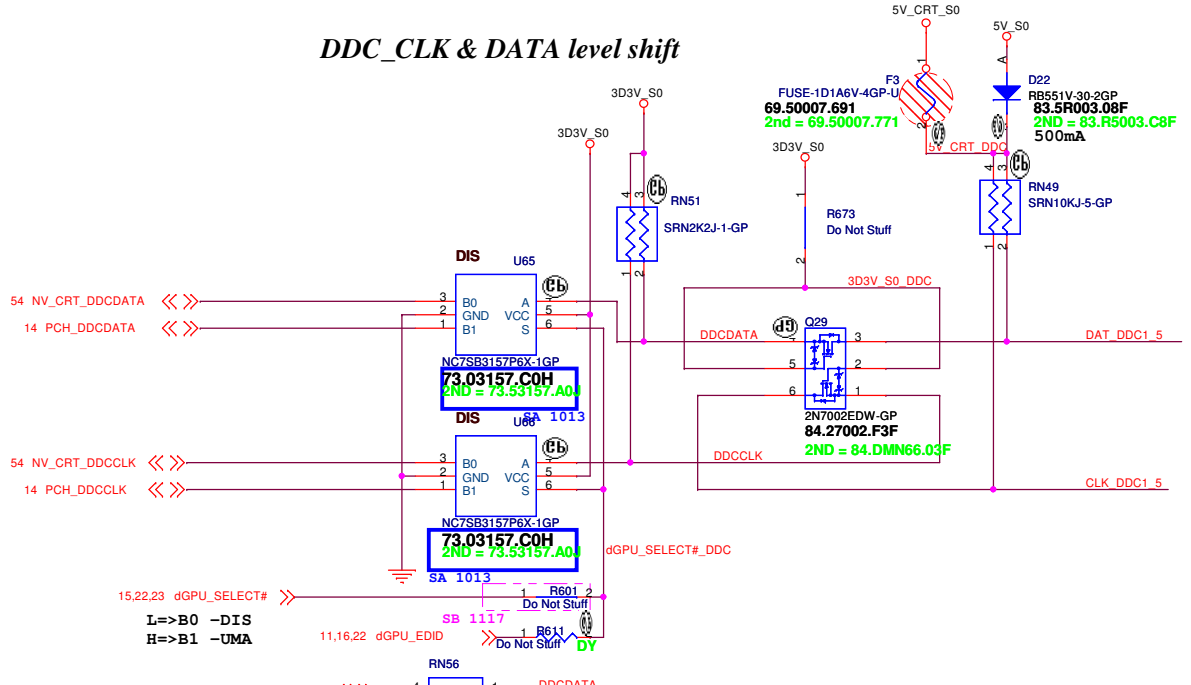


Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

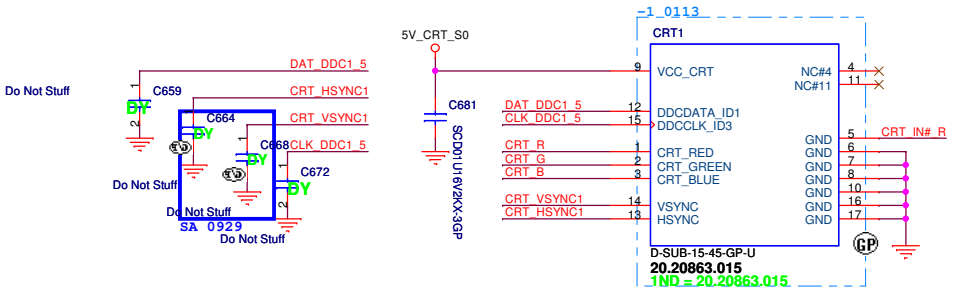
Hsync & Vsync level shift

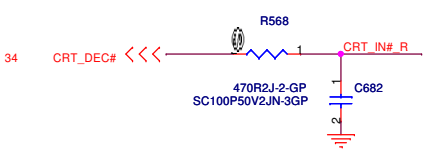


DDC_CLK & DATA level shift



CRT I/F & CONNECTOR





6 1 7 2 8 3 9 4 10 5

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Title: CRT CONN

Size	Document Number	Rev
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Close HDMI1

SB 1209

HDMI1
SKT-HDMI23-1-GP
22.10296.181
1ND = 22.10296.181
2ND = 22.10296.211
-1 0111

HDMI_TX2+
HDMI_TX2-
HDMI_TX1+
HDMI_TX1-
HDMI_TX0+
HDMI_TX0-
HDMI_TXC+
HDMI_TXC-
HDMI_A_CEC
TP83 Do Not Stuff
TDMS_A_CLK
TDMS_A_DAT
5V_HDMI
-2 0127
HDMI_A_HPD_CN
R637 10KR2J-3-GP
-1 0105
R629 100KR2J-1-GP
NV_HDMI_DETECT

5V_S0
D26
DY
HDMI_A_HPD_CN
Do Not Stuff

3D3V_S0
RN57
Do Not Stuff
UMA
Do Not Stuff
14 PCH_HDMI_CLK
14 PCH_HDMI_DATA

RN61
SRN2K2J-1-GP
66.22236.04L
TDMS_A_CLK_R
TDMS_A_DAT_R
D25
BAW56-5-GP
83.00056.Q11
2ND = 83.00056.G11
EC84 DY
EC85 DY
Do Not Stuff

5V_HDMI
-3 0210
FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771
R703 DY Do Not Stuff
-2 0127
-3 0210

3D3V_VGA
RN25
DY
Do Not Stuff
54 NV_HDMI_CLK
54 NV_HDMI_DATA
PCH_HDMI_DATA
PCH_HDMI_CLK
RN71
-1 0105
Do Not Stuff
UMA
U20 DY
1OE# VCC
1A 2OE#
1B 2B
GND 2A
Do Not Stuff
Do Not Stuff
2ND = 73.03306.D0B
TDMS_A_CLK
TDMS_A_DAT
5V_S0

SA1001
3D3V_HDMI
SB 1125
Q7 UMA
54 NV_HDMI_CLK
54 NV_HDMI_DATA
TDMS_A_CLK
TDMS_A_DAT
Do Not Stuff
Do Not Stuff
2ND = 84.DMN66.03F
SA1001

54 NV_HDMI_DATA0-
54 NV_HDMI_DATA0+
54 NV_HDMI_DATA1-
54 NV_HDMI_DATA1+
54 NV_HDMI_DATA2-
54 NV_HDMI_DATA2+
54 NV_HDMI_CLK-
54 NV_HDMI_CLK+
From VGA on board
DIS C342 SCD1U10V2KX-5GP HDMI_TX0-
DIS C340 SCD1U10V2KX-5GP HDMI_TX0+
DIS C328 SCD1U10V2KX-5GP HDMI_TX1-
DIS C324 SCD1U10V2KX-5GP HDMI_TX1+
DIS C317 SCD1U10V2KX-5GP HDMI_TX2-
DIS C313 SCD1U10V2KX-5GP HDMI_TX2+
DIS C335 SCD1U10V2KX-5GP HDMI_TXC-
DIS C332 SCD1U10V2KX-5GP HDMI_TXC+
SB 1207

3D3V_S0
C717 DY
C713 DY
C705 DY
C711 DY
Do Not Stuff
SB 1130
R634 DY
R633 DY
NC#35
NC#34

SA 1002
14 PCH_HDMI_DATA0-
14 PCH_HDMI_DATA0+
14 PCH_HDMI_CLK-
14 PCH_HDMI_CLK+
14 PCH_HDMI_DATA1-
14 PCH_HDMI_DATA1+
14 PCH_HDMI_DATA2-
14 PCH_HDMI_DATA2+
From PCH

U67
VCC GND
IN_D1- IN_D1+
IN_D2- IN_D2+
IN_D3- IN_D3+
IN_D4- IN_D4+
OUT_D1- OUT_D1+
OUT_D2- OUT_D2+
OUT_D3- OUT_D3+
OUT_D4- OUT_D4+
NC#35 NC#34
PC0 PC1
REXT RT_EN# OE# DDC_EN
SDA SCL HPD
HPD_SINK SDA_SINK SCL_SINK
Do Not Stuff
DY
Do Not Stuff

SA 1002
HDMI_TX0- HDMI_TX0+
HDMI_TXC- HDMI_TXC+
HDMI_TX1- HDMI_TX1+
HDMI_TX2- HDMI_TX2+
PCH_HDMI_DATA
PCH_HDMI_CLK
PCH_HDMI_DETECT

Recommended Equalization: [PC1,PC0]=01, 4dB
SB 1130
3D3V_S0
R607 DY Do Not Stuff PC0
R606 DY Do Not Stuff PC1
R605 DY Do Not Stuff
REXT_HDMI
PS8101_RT_EN#
OE# PS8101
DDC_EN_PS8101

HDMI_TX0- HDMI_TX0+ R627 R625
HDMI_TX1- HDMI_TX1+ R619 R617
HDMI_TX2- HDMI_TX2+ R615 R613
HDMI_TXC- HDMI_TXC+ R624 R620
562R2F-GP
DIS 64.49905.6DL/ UMA:64.56205.6DL
SB 1202

HDMI_A_HPD_CN
TDMS_A_DAT
TDMS_A_CLK
RN23
SRN0J-6-GP
DIS
SB 1119
NV_HDMI_DATA 54
NV_HDMI_CLK 54
R603 Do Not Stuff DY
PCH_HDMI_DETECT 14

3D3V_S0
R628 Do Not Stuff DY
OE# PS8101
Q36 Do Not Stuff
Do Not Stuff
2ND = 84.27002.W31
DY
R631 DY Do Not Stuff
HDMI_A_HPD_CN
SB 1210
SB 1207

SB 1125
3D3V_S0 3D3V_VGA
R180 0R2J-2-GP
R179 Do Not Stuff DY
3D3V_HDMI
SB 1210
Q22 2N7002-7F-GP
84.27002.N31
2ND = 84.27002.W31
NV_HDMI_DETECT
34,54 HPD1
PCH_HDMI_DETECT
R178 UMA Do Not Stuff
SB 1125
R524 10KR2J-3-GP
-1 0105

Q5 2N7002-7F-GP
84.27002.N31
2ND = 84.27002.W31
SB 1210
3D3V_S0
DY R201 Do Not Stuff
SA 0929

REXT_HDMI
PS8101_RT_EN#
R604 Do Not Stuff DY
R602 Do Not Stuff DY
SB 1202

3D3V_S0
SB 1202
R632 Do Not Stuff DY
DDC_EN_PS8101

PCH_HDMI_CLK- UMA C339 Do Not Stuff HDMI_TXC-
PCH_HDMI_CLK+ UMA C334 Do Not Stuff HDMI_TXC+
PCH_HDMI_DATA0- UMA C344 Do Not Stuff HDMI_TX0-
PCH_HDMI_DATA0+ UMA C341 Do Not Stuff HDMI_TX0+
PCH_HDMI_DATA1- UMA C327 Do Not Stuff HDMI_TX1-
PCH_HDMI_DATA1+ UMA C323 Do Not Stuff HDMI_TX1+
PCH_HDMI_DATA2- UMA C316 Do Not Stuff HDMI_TX2-
PCH_HDMI_DATA2+ UMA C312 Do Not Stuff HDMI_TX2+
SA1001
SB 1207

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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI CONNECTOR
Size: A3
Document Number: JM31-CP
Rev: -1
Date: Thursday, February 25, 2010
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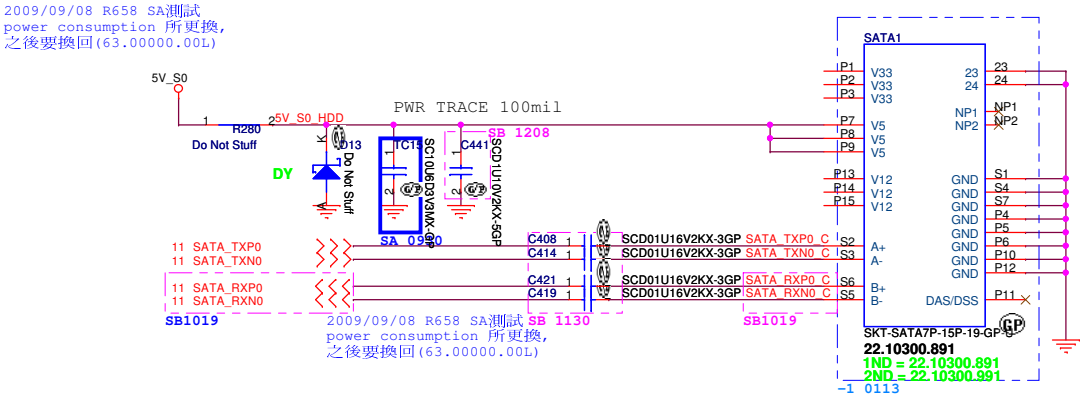
SATA Connector



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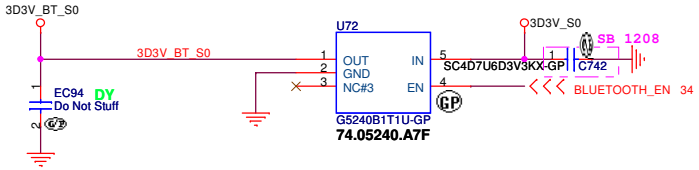
Title: ***HDD CONN***

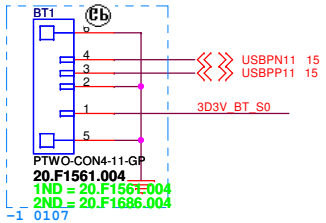
Size	Document Number	Rev
A3	JM31-CP	-1

Date: Thursday, February 25, 2010 Sheet 26 of 62

BLUETOOTH MODULE



EC20 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request



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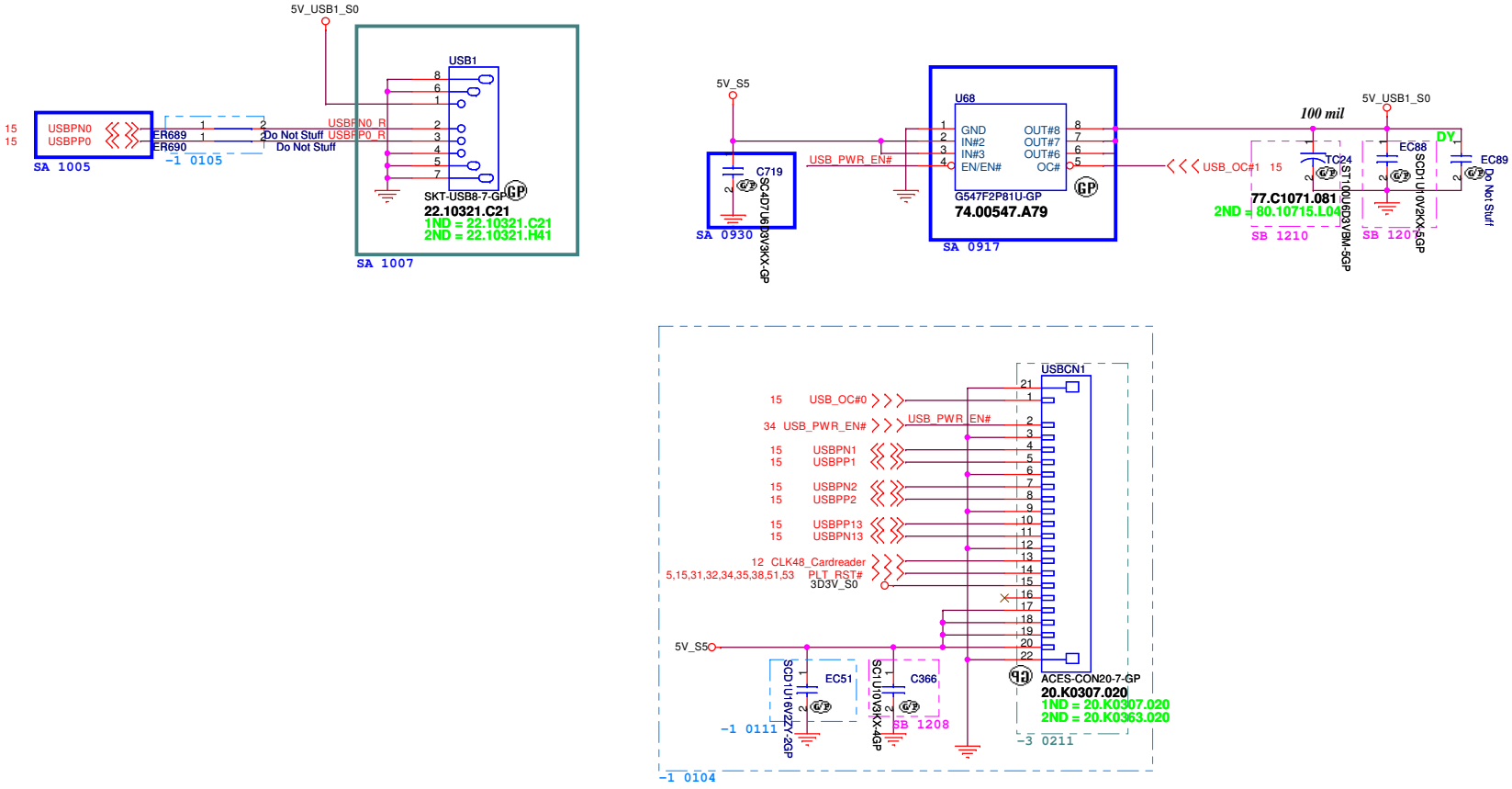
Title: ***BLUETOOTH***		
Size: A3	Document Number: **JM31-CP**	Rev: -1
Date: Thursday, February 25, 2010	Sheet 27 of 62	



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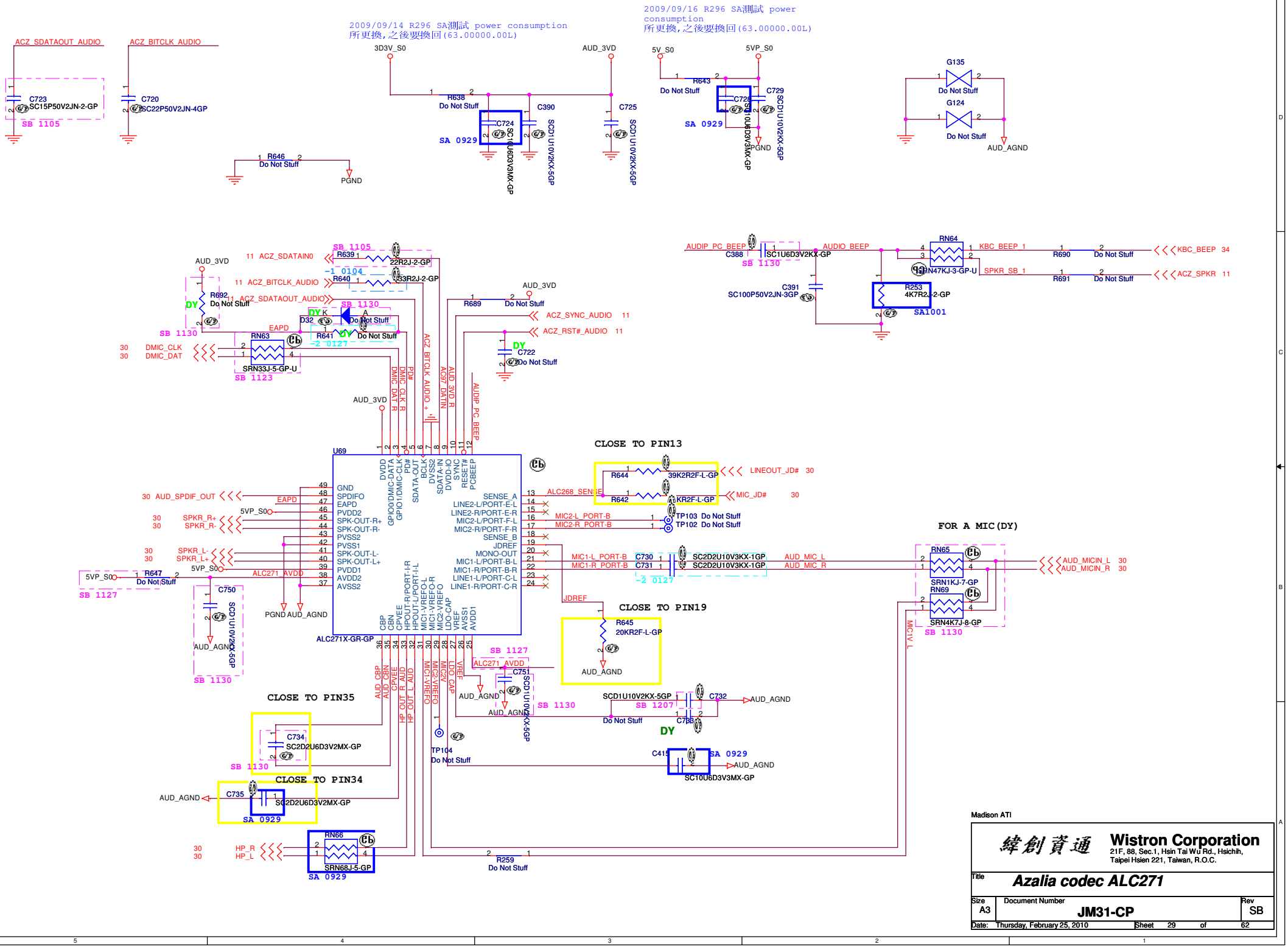
Title	*USB CONN*	
Size A3	Document Number JM31-CP	Rev -3
Date: Thursday, February 25, 2010	Sheet 28 of 62	


2009/09/14 R296 SA測試 power consumption
所更換,之後要換回(63.00000.00L)
2009/09/16 R296 SA測試 power consumption
所更換,之後要換回(63.00000.00L)
ACZ_SDATAOUT_AUDIO
ACZ_BITCLK_AUDIO
C723 SC15P50V2JN-2-GP
SB 1105
C720 SC22P50V2JN-4GP
3D3V_S0
AUD_3VD
R638 Do Not Stuff
C724 SC10U6D3V3MX-GP
SA 0929
C390 SCD1U10V2KX-5GP
C725 SCD1U10V2KX-5GP
R646 Do Not Stuff
PGND
5V_S0
5VP_S0
R643 Do Not Stuff
C728 SC10U6D3V3MX-GP
SA 0929
C729 SCD1U10V2KX-5GP
G135 Do Not Stuff
G124 Do Not Stuff
AUD_AGND
AUDIP_PC_BEEP
C388 SC1U6D3V2KX-GP
SB 1130
AUDIO_BEEP
RN64 RN47KJ-3-GP-U
KBC_BEEP_1
R690 Do Not Stuff
KBC_BEEP 34
SPKR_SB_1
R691 Do Not Stuff
ACZ_SPKR 11
C391 SC100P50V2JN-3GP
R253 4K7R2J-2-GP
SA1001
11 ACZ_SDATAIN0
SB 1105
R639 22R2J-2-GP
-1 0104
11 ACZ_BITCLK_AUDIO
R640 33R2J-2-GP
11 ACZ_SDATAOUT_AUDIO
SB 1130
R692 Do Not Stuff
DY
D32 Do Not Stuff
R641 Do Not Stuff
-2 0127
EAPD
SB 1130
RN63 SRN33J-5-GP-U
SB 1123
30 DMIC_CLK
30 DMIC_DAT
AUD_3VD
R689 Do Not Stuff
ACZ_SYNC_AUDIO 11
ACZ_RST#_AUDIO 11
C722 Do Not Stuff
ACZ_BITCLK_AUDIO
ACZ_SDATAIN
AUDIP_PC_BEEP
U69
ALC271X-GR-GP
CLOSE TO PIN13
R644 39K2R2F-L-GP
R642 2K2F-L-GP
LINEOUT_JD# 30
MIC_JD# 30
TP103 Do Not Stuff
TP102 Do Not Stuff
MIC2-L_PORT-B
MIC2-R_PORT-B
FOR A MIC (DY)
RN65 SRN1KJ-7-GP
RN69 SRN4K7J-8-GP
SB 1130
AUD_MICIN_L 30
AUD_MICIN_R 30
MIC1-L_PORT-B
MIC1-R_PORT-B
C730 SC2D2U10V3KX-1GP
C731 SC2D2U10V3KX-1GP
AUD_MIC_L
AUD_MIC_R
-2 0127
30 AUD_SPDIF_OUT
30 SPKR_R+
30 SPKR_R-
30 SPKR_L-
30 SPKR_L+
5VP_S0
R647 Do Not Stuff
SB 1127
ALC271_AVDD
C750 SCD1U10V2KX-5GP
SB 1130
PGND AUD_AGND
JDREF
CLOSE TO PIN19
R645 20KR2F-L-GP
SB 1127
C751 SCD1U10V2KX-5GP
SB 1130
SCD1U10V2KX-5GP
C732
SB 1207
Do Not Stuff
C733
DY
TP104 Do Not Stuff
C415 SC10U6D3V3MX-GP
SA 0929
CLOSE TO PIN35
C734 SC2D2U6D3V2MX-GP
SB 1130
CLOSE TO PIN34
C735 SC2D2U6D3V2MX-GP
SA 0929
RN66 SRN68J-5-GP
SA 0929
30 HP_R
30 HP_L
R259 Do Not Stuff
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Wistron Corporation
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Title
Azalia codec ALC271
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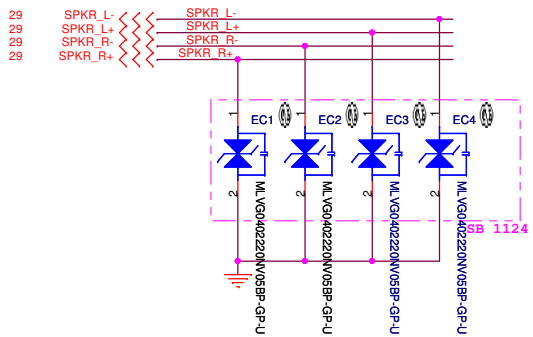
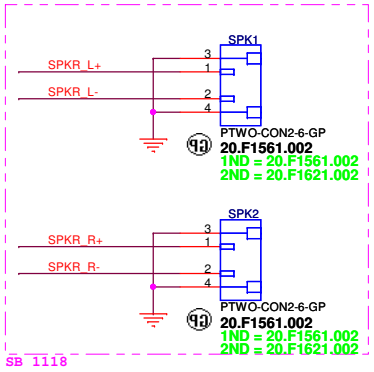
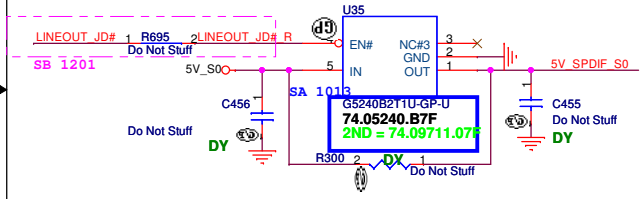
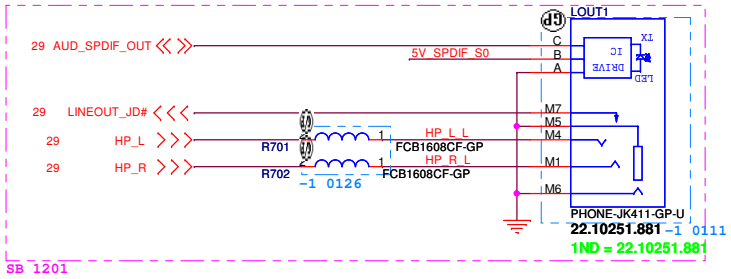
Internal Speaker

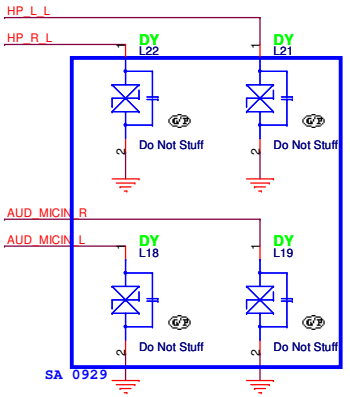




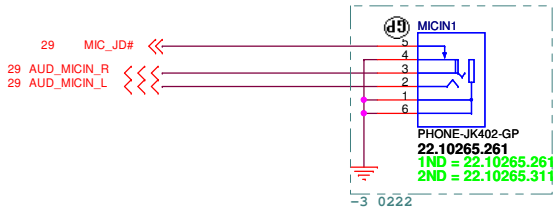
LINE OUT

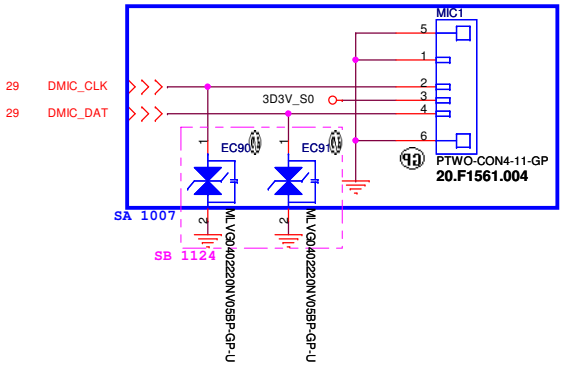






MIC IN





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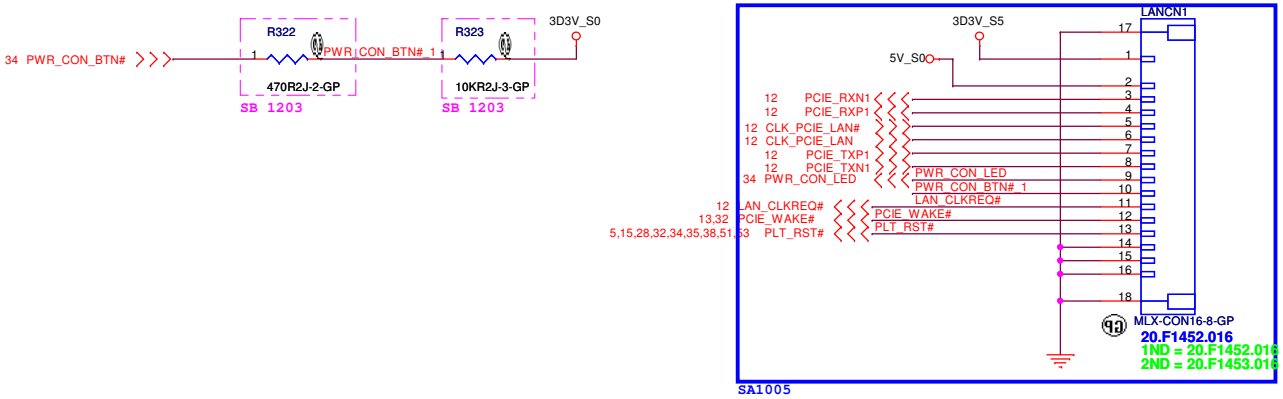
Title	*AUDIO jack*	
Size A3	Document Number JM31-CP	Rev -1
Date: Thursday, February 25, 2010	Sheet 30 of 62	



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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN CONN***

Size	Document Number	Rev
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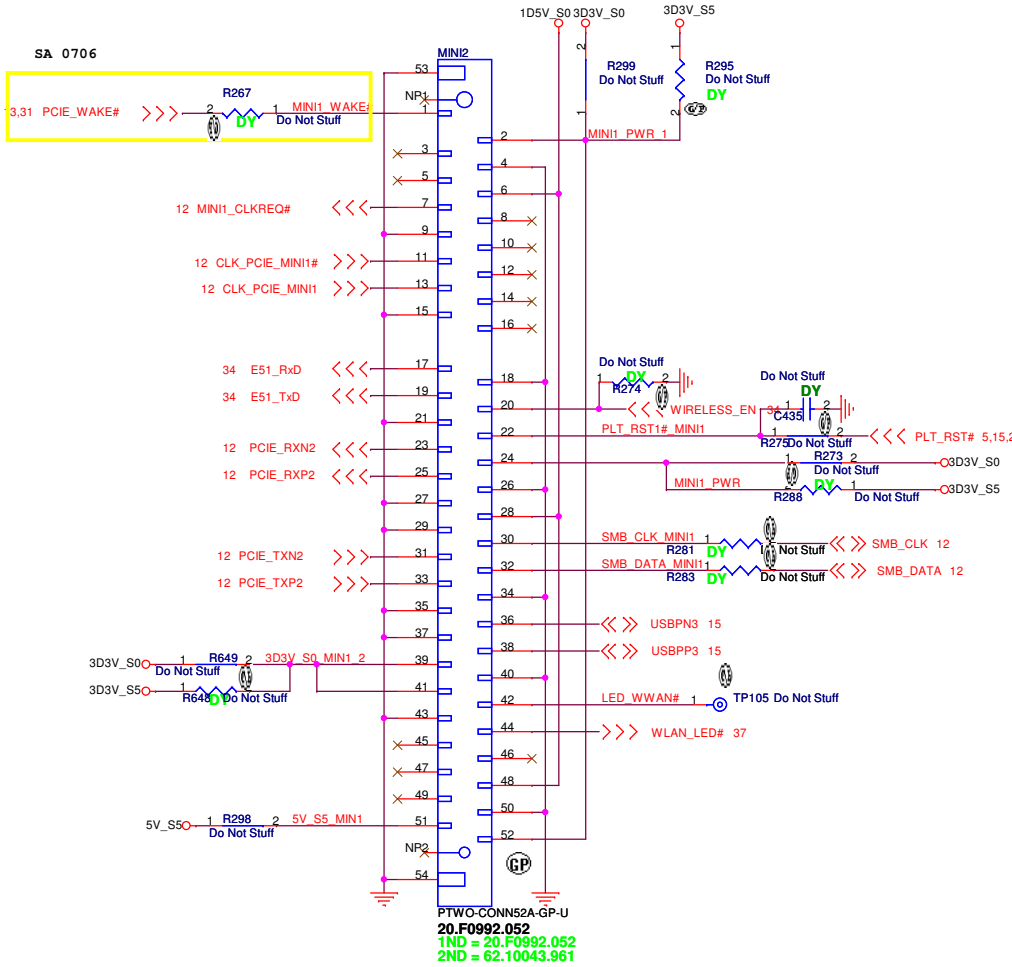
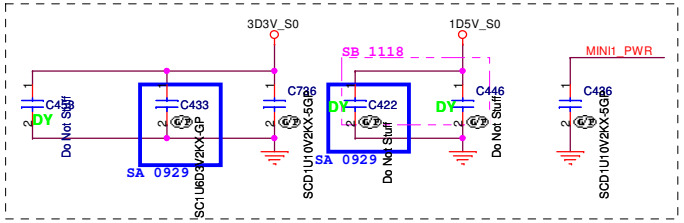
Date: Thursday, February 25, 2010 Sheet 31 of 62

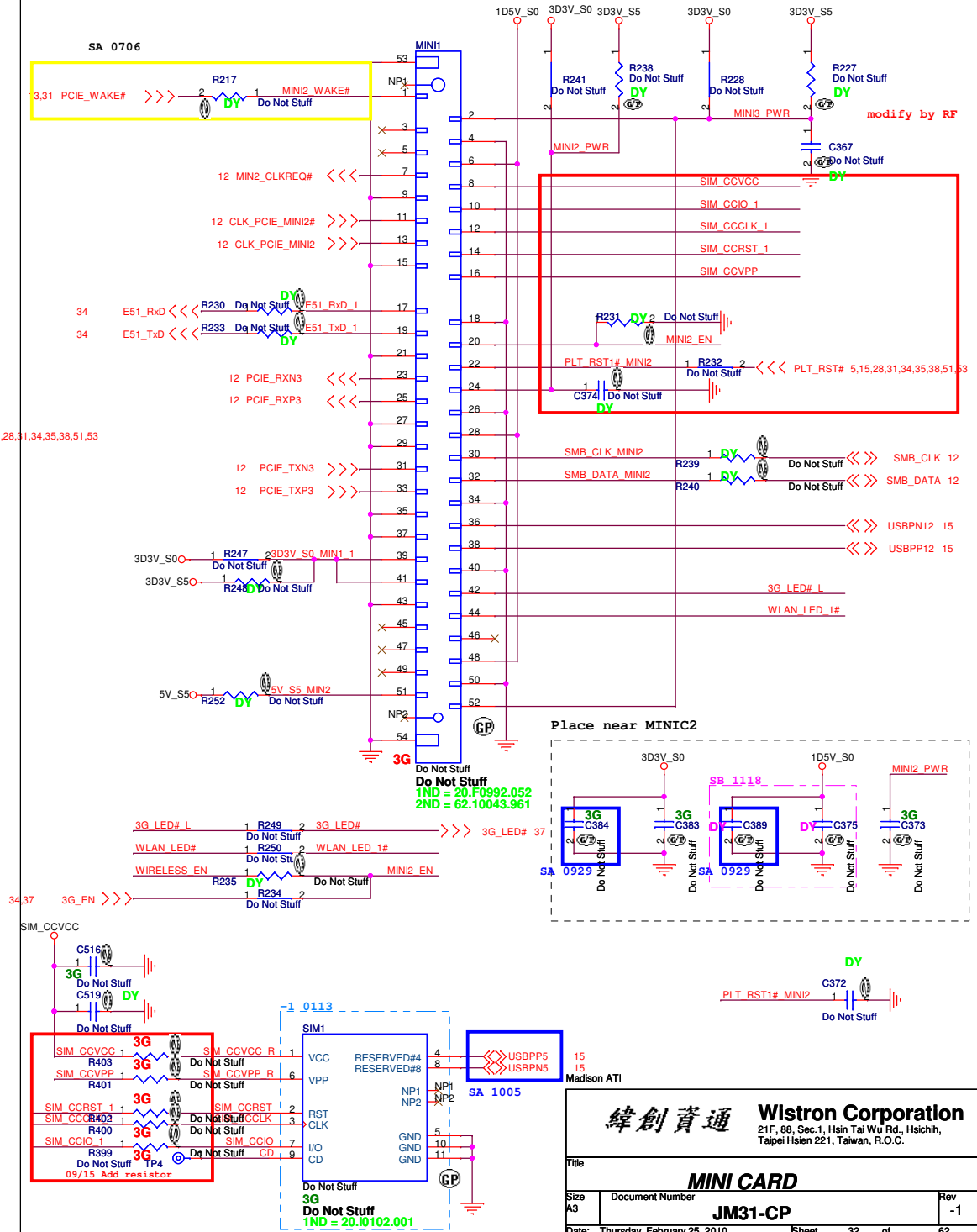
Mini Card Connector(WLAN)
Support debug-card



Place near MINI1



Mini Card Connector(Robson2 and 3G)



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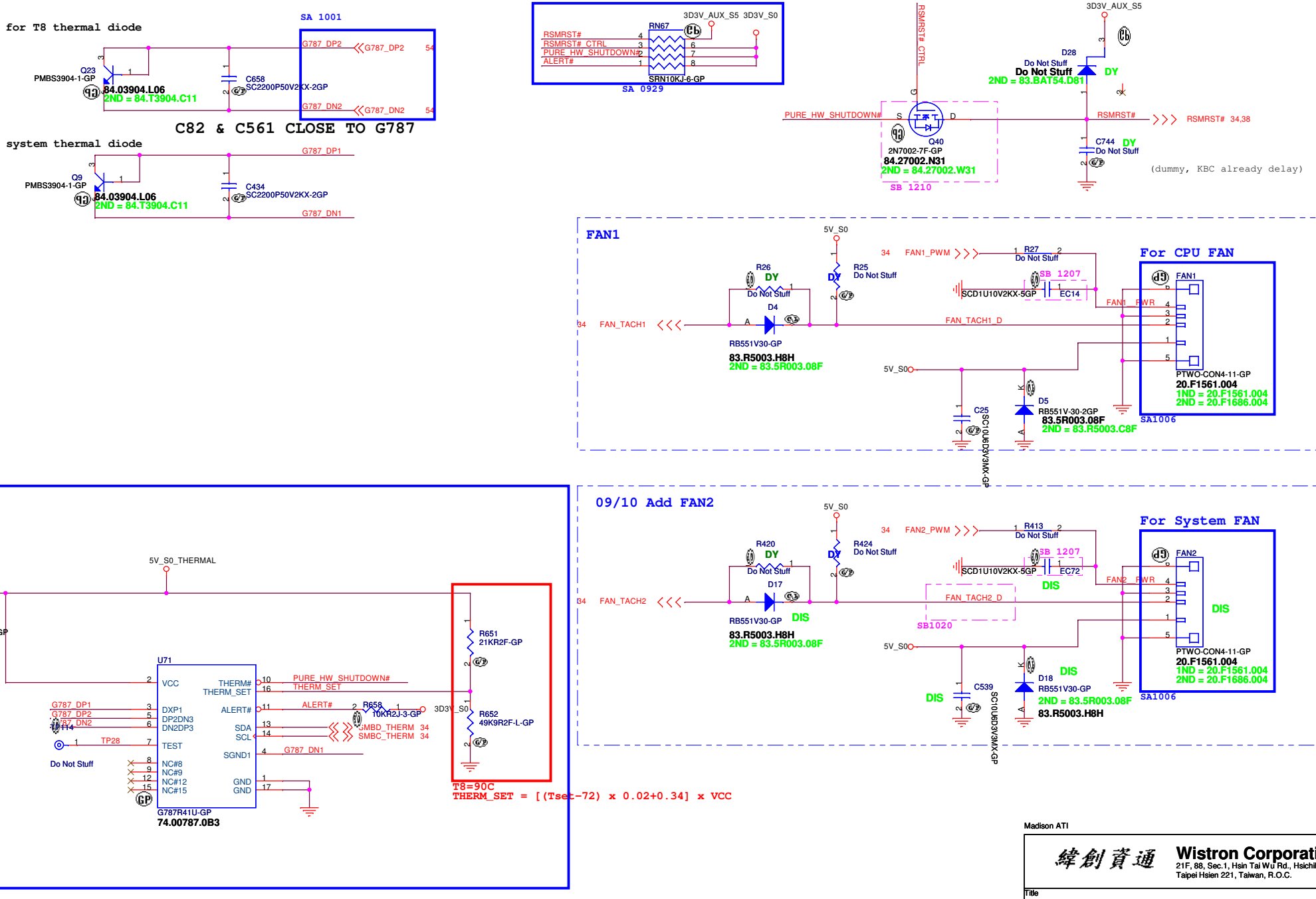
Title: **MINI CARD**		
Size: A3	Document Number: JM31-CP	Rev: -1
Date: Thursday, February 25, 2010	Sheet 32 of 62	



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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Connector***

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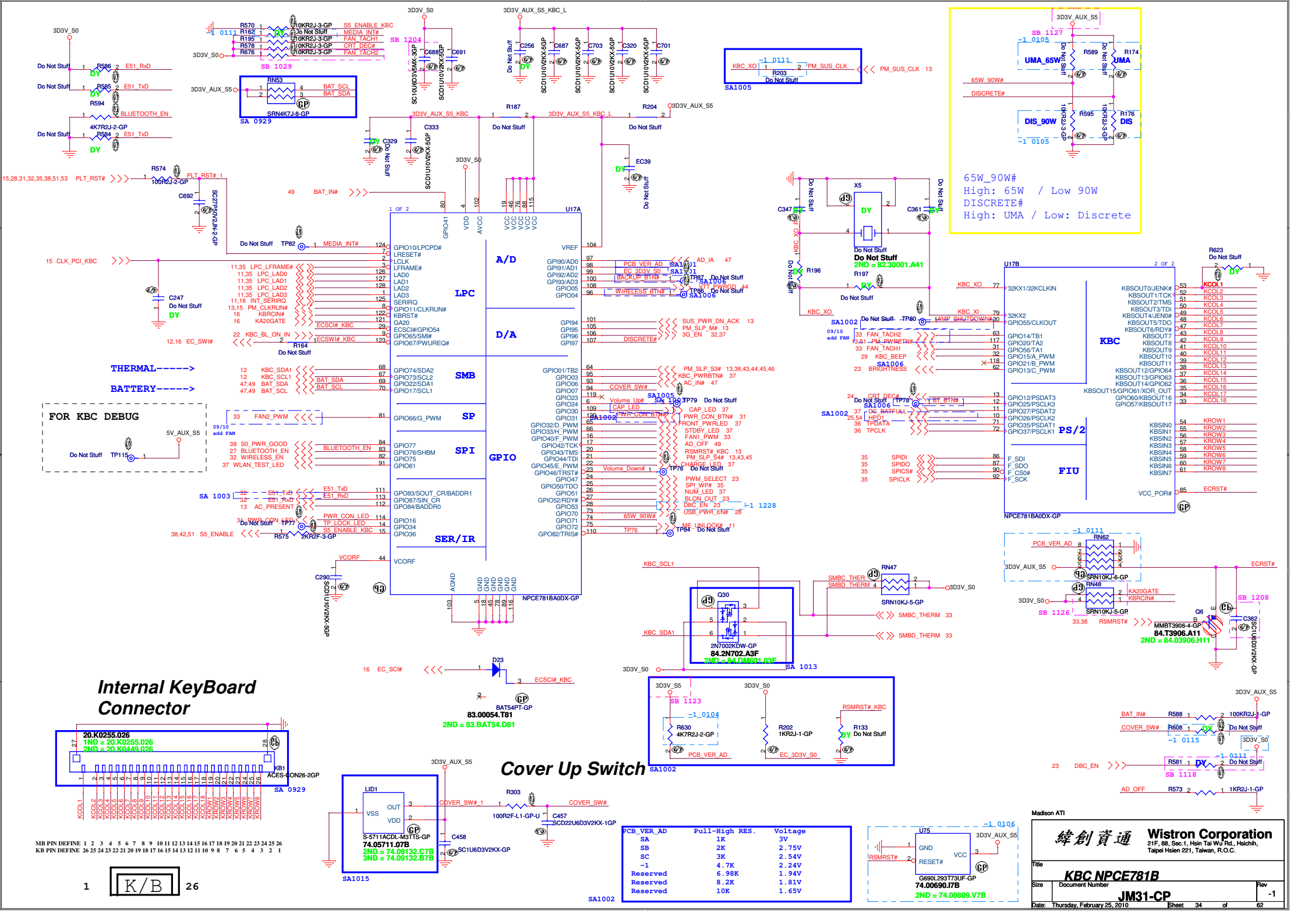
65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete
FOR KBC DEBUG
THERMAL----->
BATTERY----->
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IRQ
KBC
PS/2
FIU
Internal KeyBoard Connector
Cover Up Switch
20.K0255.026
1ND = 20.K0255.026
2ND = 20.K0449.026
83.00054.T81
2ND = 83.BAT54.D81
74.05711.07B
2ND = 74.09132.C7B
3ND = 74.09132.B7B
2N7002KDW-GP
84.2N702.A3F
MMBT3906-4-GP
84.T3906.A11
2ND = 84.03906.H11
G690L293T3UF-GP
74.00690.I7B
2ND = 74.00809.V7B
NPCE781BA0DX-GP
MB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
KB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
PCB_VER_AD Pull-High RES. Voltage
SA 1K 3V
SB 2K 2.75V
SC 3K 2.54V
-1 4.7K 2.24V
Reserved 6.98K 1.94V
Reserved 8.2K 1.81V
Reserved 10K 1.65V
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緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC NPCE781B
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Date: Thursday, February 25, 2010
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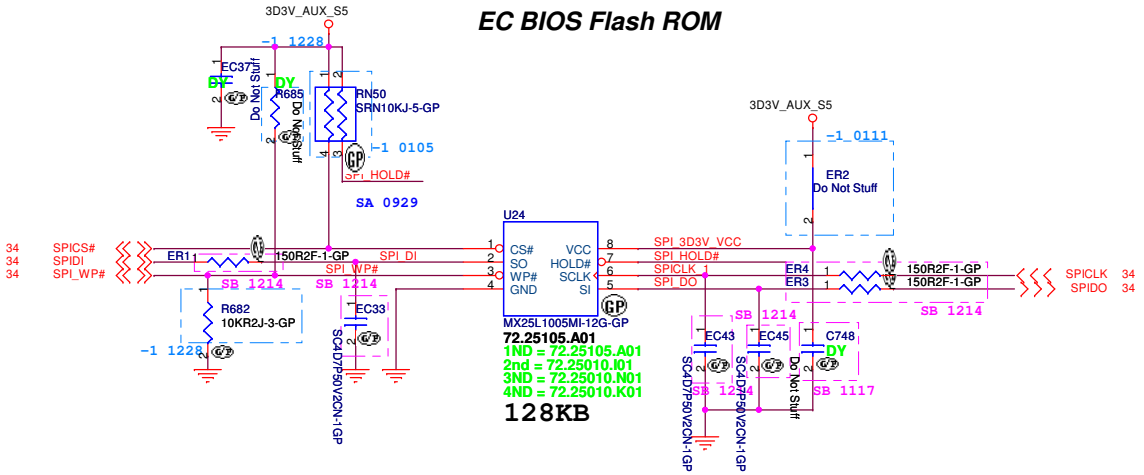
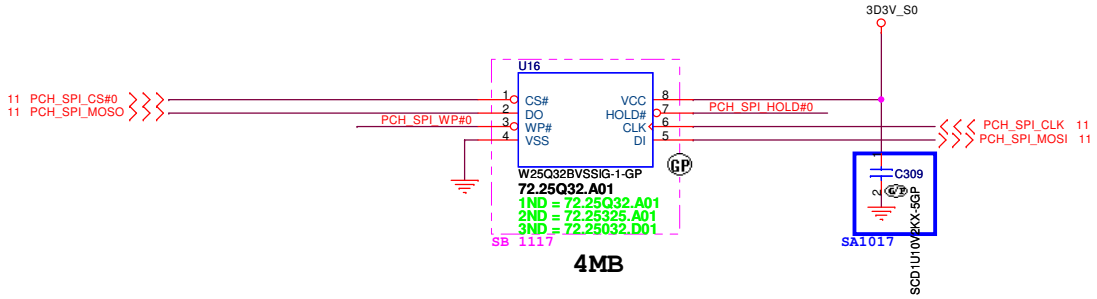
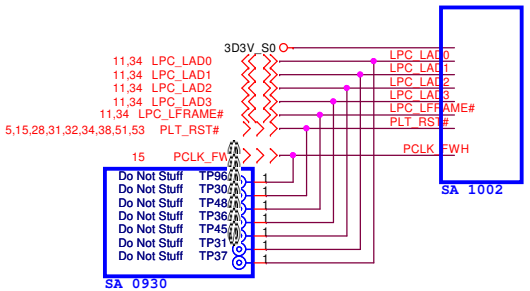
EC BIOS Flash ROM

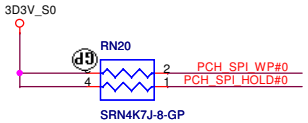


System BIOS Flash ROM



GOLDEN FINGER FOR DEBUG BOARD





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Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS**

Size	Document Number	Rev
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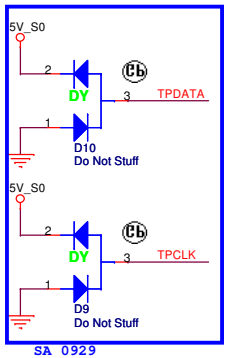
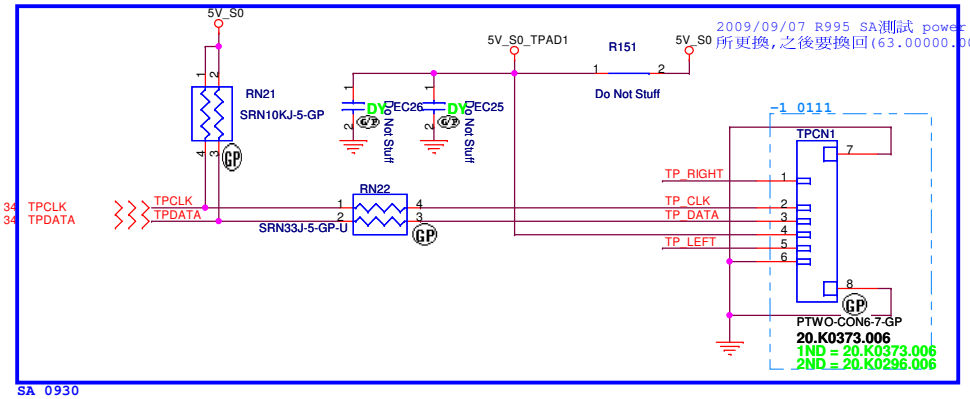
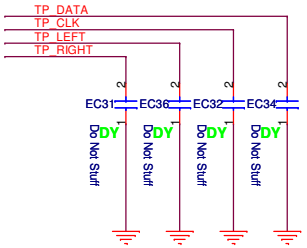
TOUCH PAD

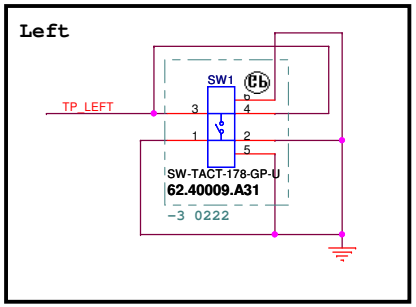


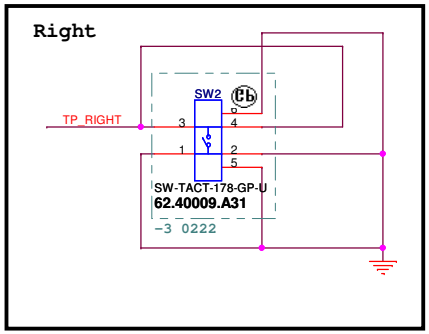


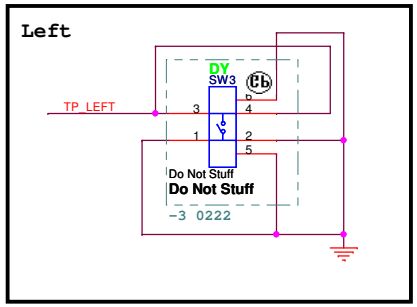


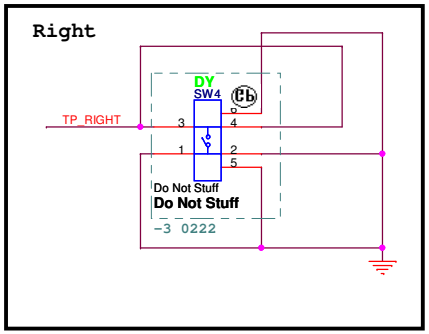
1 12

T/P









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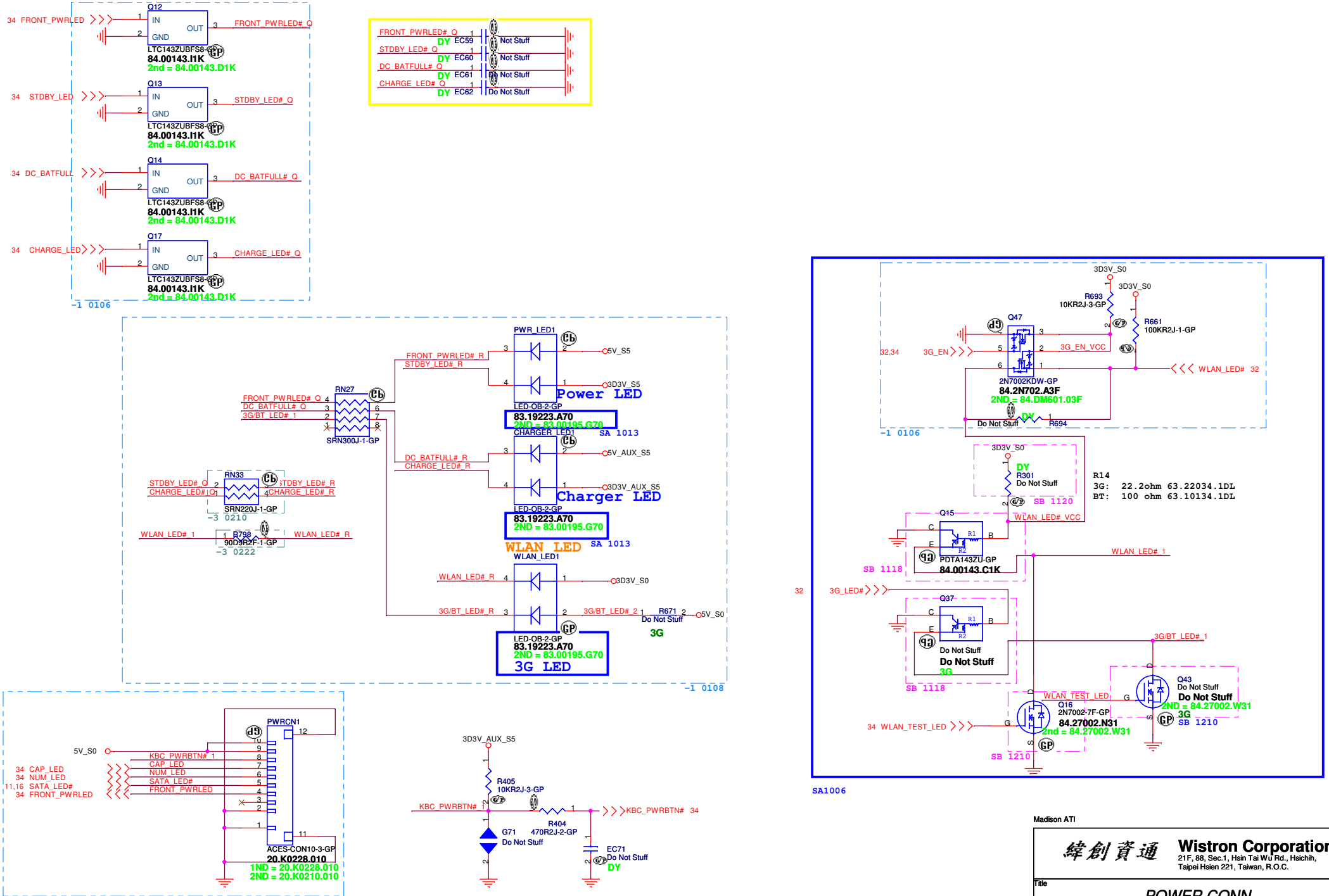
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Touch PAD*		
Size: A3	Document Number: JM31-CP	Rev: -1
Date: Thursday, February 25, 2010	Sheet 36 of 62	



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Title	POWER CONN	
Size A3	Document Number JM31-CP	Rev -3
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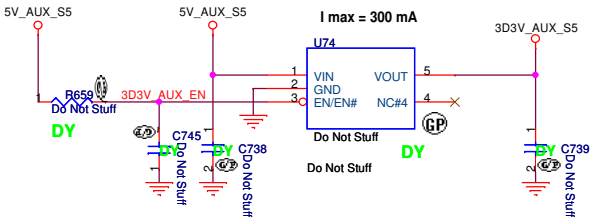
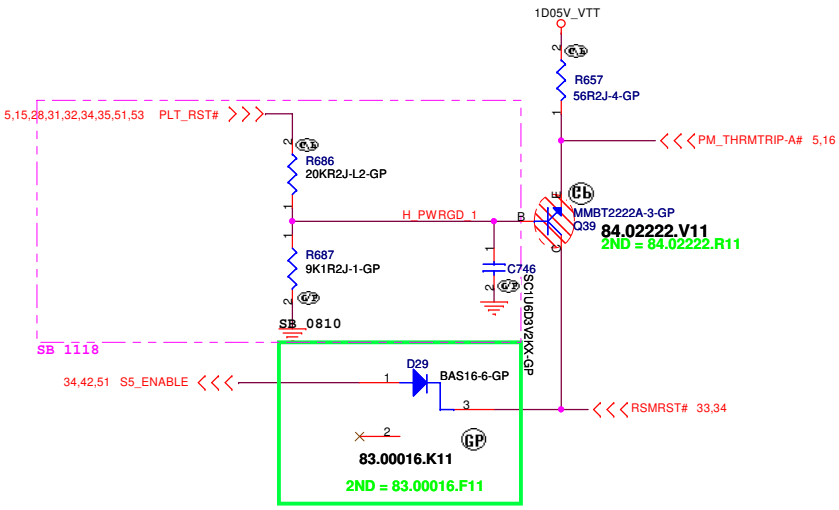
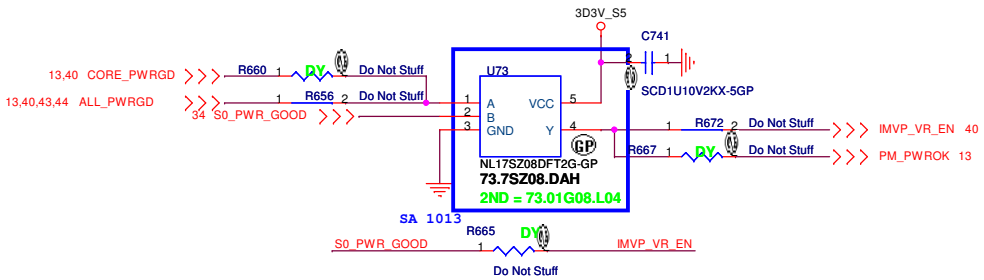
Run Power

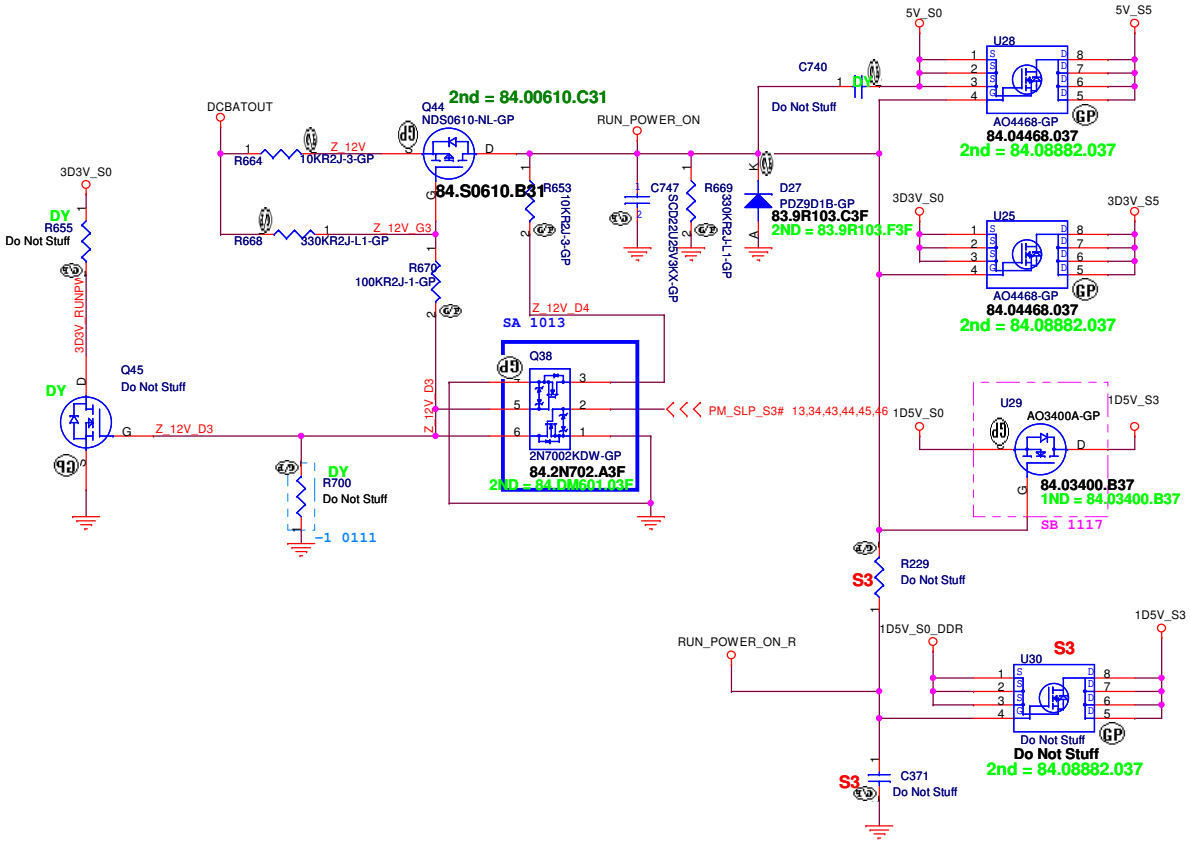
Aux Power

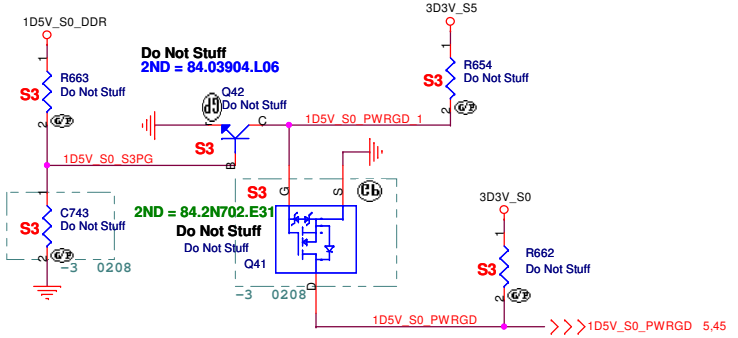
3D3V_AUX_S5











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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER and 3D3V_AUX_S5**

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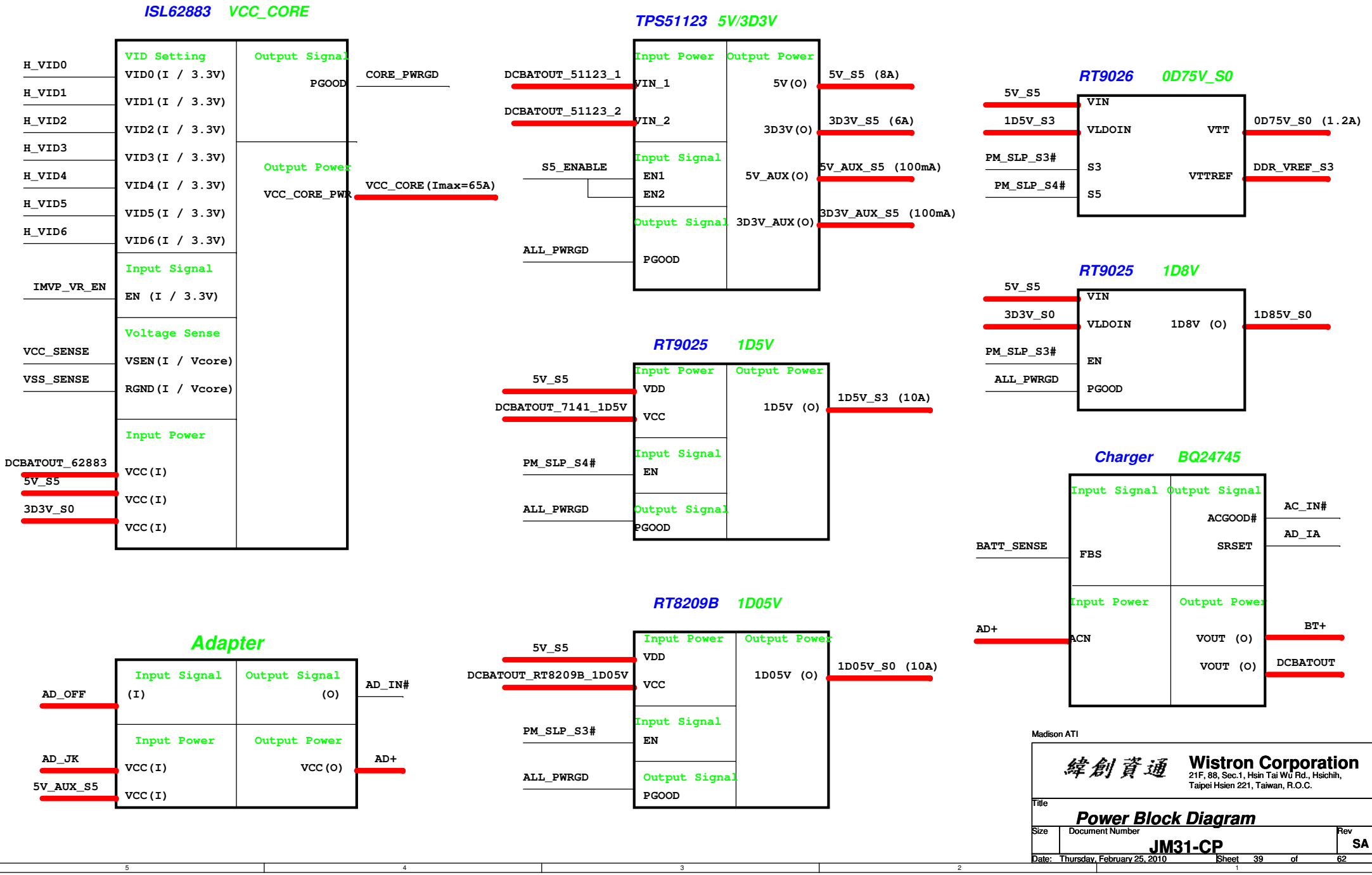

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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	JM31-CP	SA

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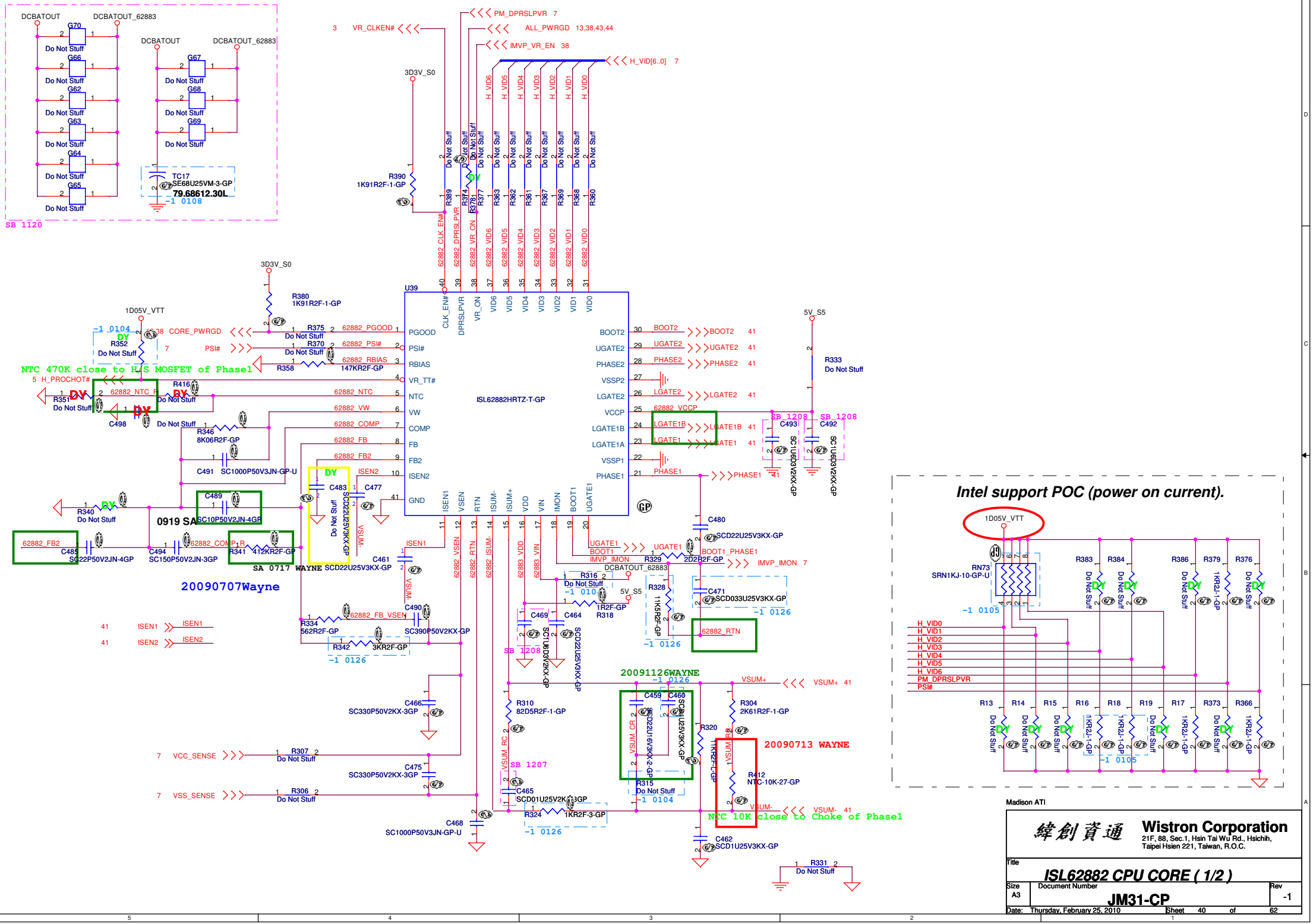
DCBATOUT
DCBATOUT_62883
G70
G66
G62
G63
G64
G65
G67
G68
G69
Do Not Stuff
TC17
SE68U25VM-3-GP
79.68612.30L
-1 0108
SB 1120
3D3V_S0
R390
1K91R2F-1-GP
PM_DPRSLPVR 7
ALL_PWRGD 13,38,43,44
IMVP_VR_EN 38
H_VID[6..0] 7
VR_CLKEN# 3
62882_CLK_EN#
62882_DPRSLPVR
62882_VR_ON
62882_VID6
62882_VID5
62882_VID4
62882_VID3
62882_VID2
62882_VID1
62882_VID0
U39
ISL62882HRTZ-T-GP
PGOOD
PSI#
RBIAS
VR_TT#
NTC
VW
COMP
FB
FB2
ISEN2
GND
ISEN1
VSEN
RTN
ISUM-
ISUM+
VDD
VIN
IMON
BOOT1
UGATE1
BOOT2
UGATE2
PHASE2
VSSP2
LGATE2
VCCP
LGATE1B
LGATE1A
VSSP1
PHASE1
1D05V_VTT
5V_S5
CORE_PWRGD
PSI#
H_PROCHOT#
NTC 470K close to H/S MOSFET of Phase1
R352
R351
R416
R358
147KR2F-GP
C498
R346
8K06R2F-GP
C491
SC1000P50V3JN-GP-U
C489
SC10P50V2JN-4GP
0919 SA
R340
C485
SC22P50V2JN-4GP
C494
SC150P50V2JN-3GP
R341
412KR2F-GP
SA 0717 WAYNE SCD22U25V3KX-GP
20090707Wayne
C483
C477
C461
R334
562R2F-GP
C490
SC390P50V2KX-GP
R342
3KR2F-GP
-1 0126
C466
SC330P50V2KX-3GP
R307
Do Not Stuff
C475
SC330P50V2KX-3GP
R306
C468
SC1000P50V3JN-GP-U
R380
1K91R2F-1-GP
R375
R370
C480
SCD22U25V3KX-GP
R329
2D2R2F-GP
IMVP_IMON 7
DCBATOUT_62883
R316
1R2F-GP
R318
R328
11K5R2F-GP
C471
SCD033U25V3KX-GP
62882_RTN
C469
C464
SCD22U25V3KX-GP
SB 1208
SC1U6D3V2KX-GP
20091126WAYNE
R310
82D5R2F-1-GP
C459
C460
SCD22U16V3KX-2-GP
SCD22U25V3KX-GP
R315
R320
1KR2F-GP
R304
2K61R2F-1-GP
VSUM+ 41
VSUM- 41
20090713 WAYNE
R312
NTC-10K-27-GP
NTC 10K close to Choke of Phase1
C465
SCD01U25V2KX-3GP
R324
1KR2F-3-GP
SB 1207
C462
SCD1U25V3KX-GP
R331
C493
C492
R333
SB 1208
Intel support POC (power on current).
RN73
SRN1KJ-10-GP-U
R383
R384
R386
R379
R376
R13
R14
R15
R16
R18
R19
R17
R373
R366
1KR2J-1-GP
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
PM_DPRSLPVR
PSI#
Madison ATI
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62882 CPU CORE (1/2)
Size
A3
Document Number
JM31-CP
Rev
-1
Date: Thursday, February 25, 2010
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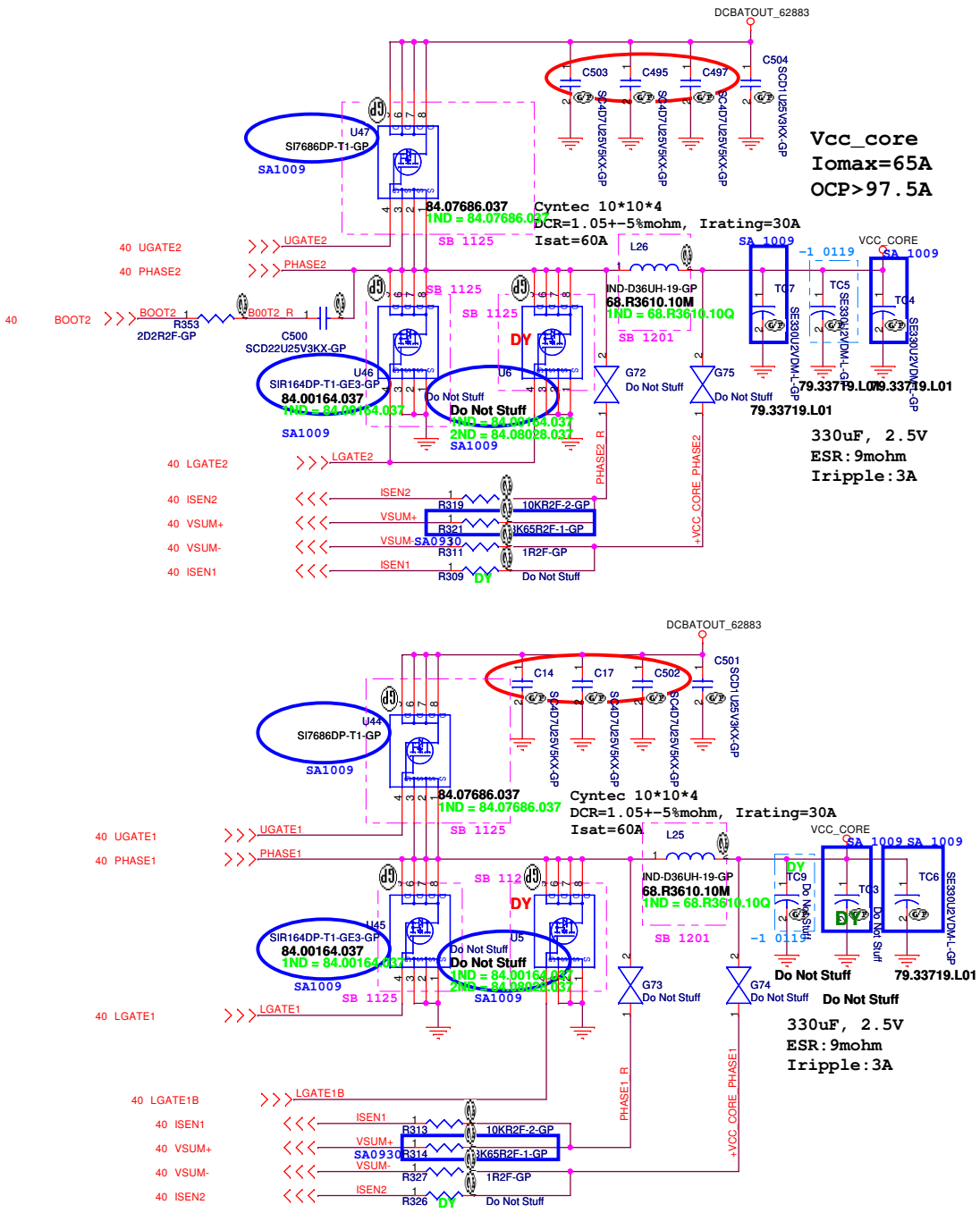

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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *ISL62882 CPU CORE (2/2)*

Size	Document Number	Rev
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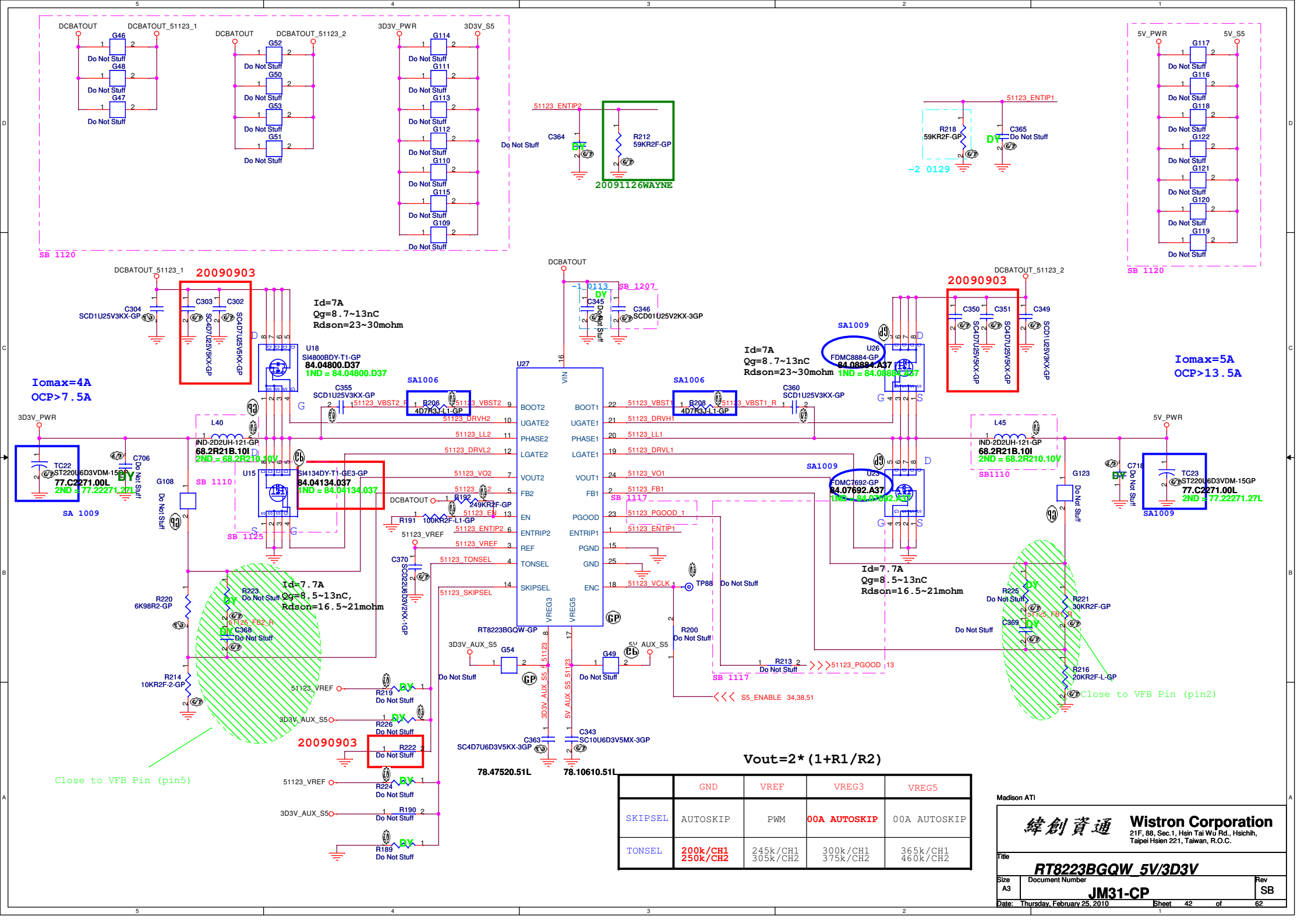

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

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Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223BGQW_5V/3D3V

Size: A3 | Document Number: JM31-CP | Rev: SB

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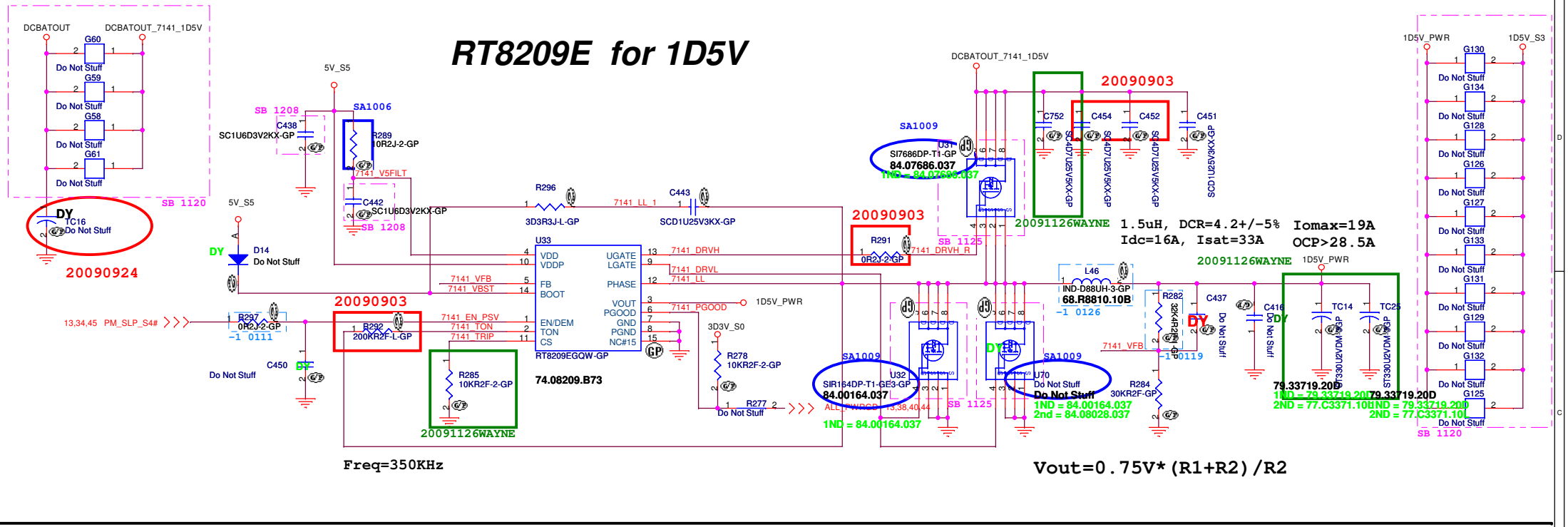
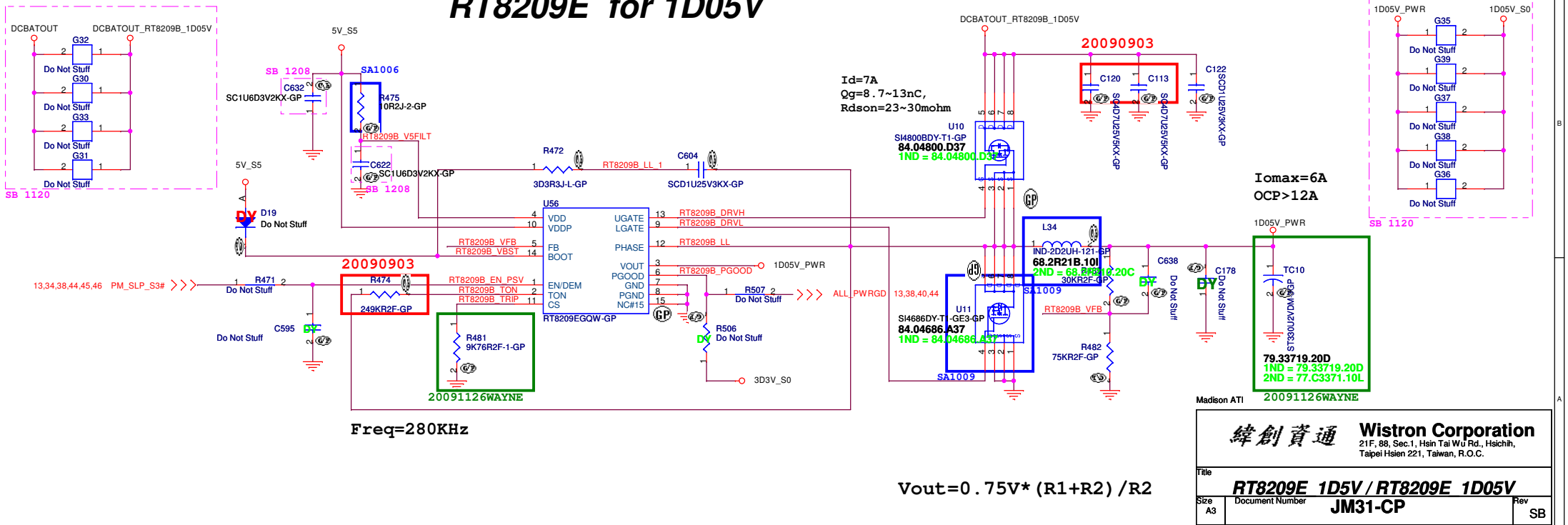
RT8209E for 1D5V



RT8209E for 1D05V



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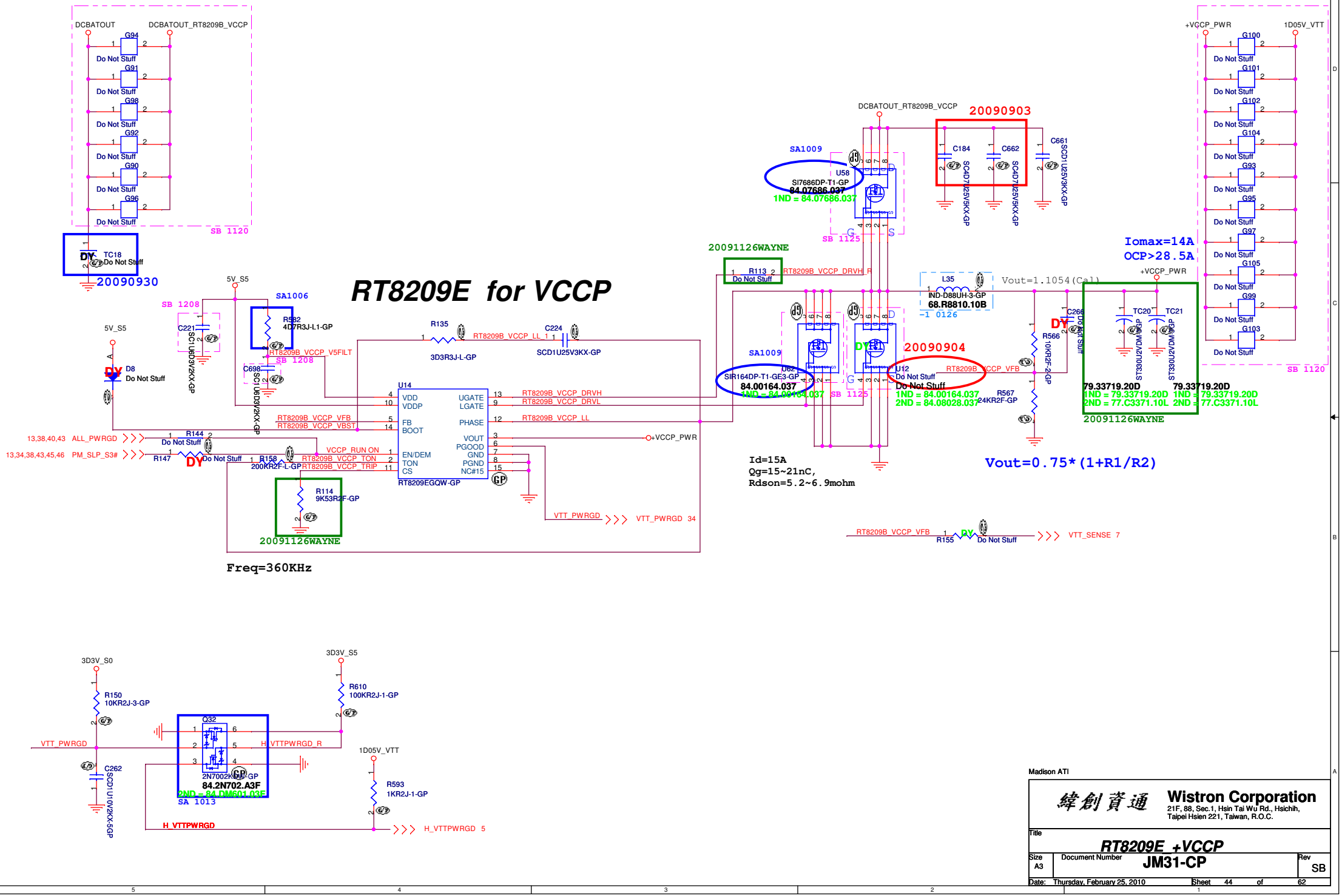
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8209E 1D5V / RT8209E 1D05V	
Size A3	Document Number JM31-CP	Rev SB
Date: Thursday, February 25, 2010	Sheet 43 of 62	



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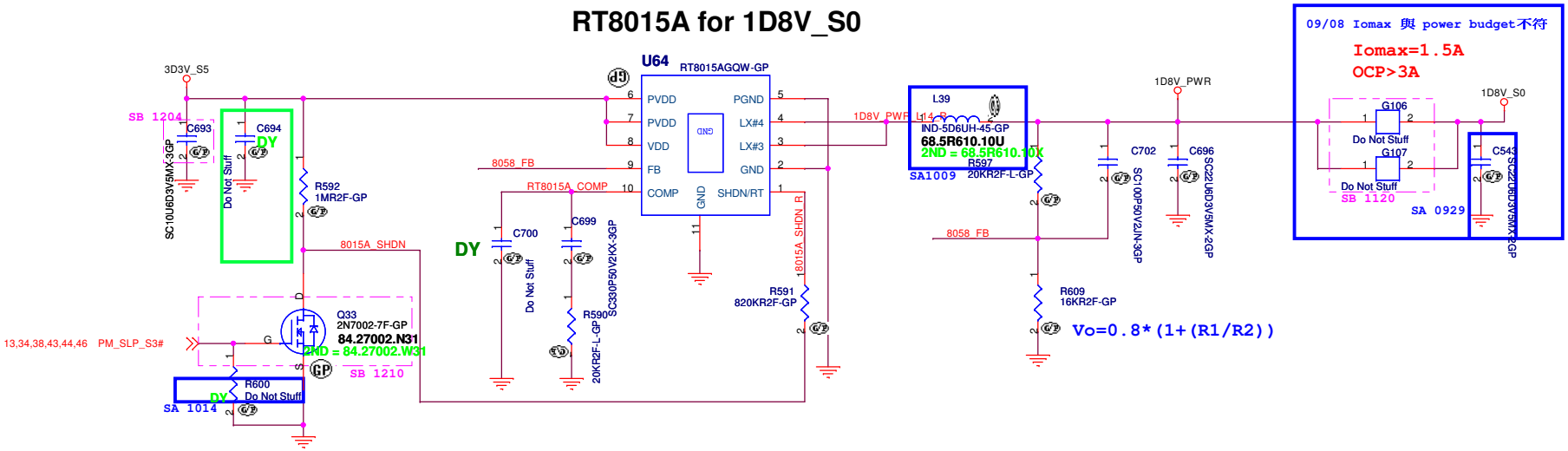
Taipei Hsien 221, Taiwan, R.O.C.

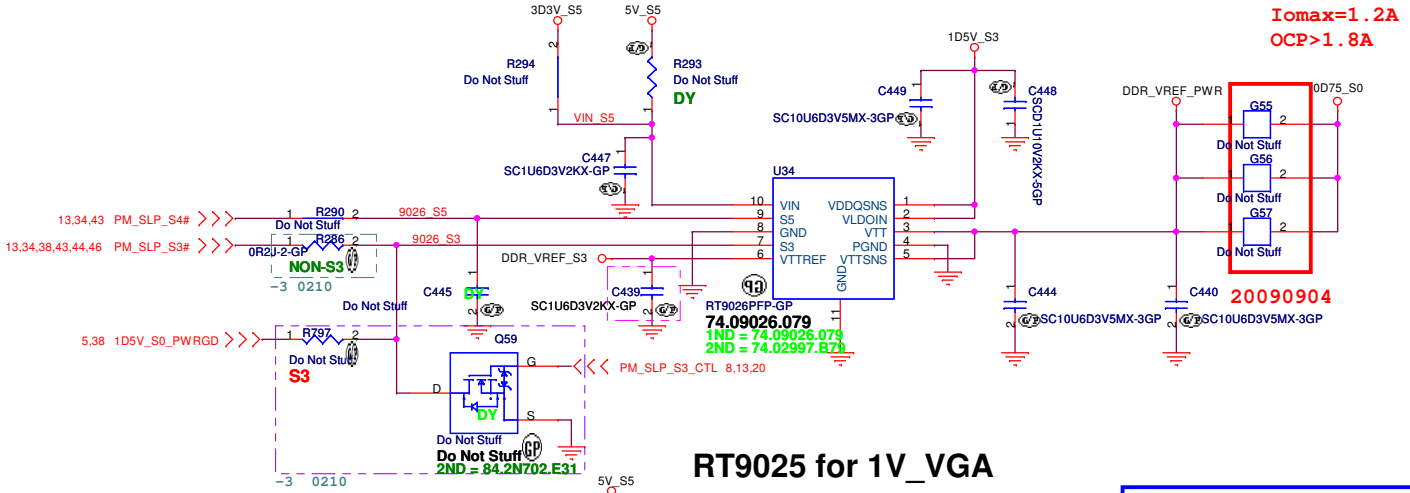
Title	RT8209E +VCCP	
Size A3	Document Number JM31-CP	Rev SB
Date: Thursday, February 25, 2010	Sheet 44 of 62	

RT8015A for 1D8V_S0

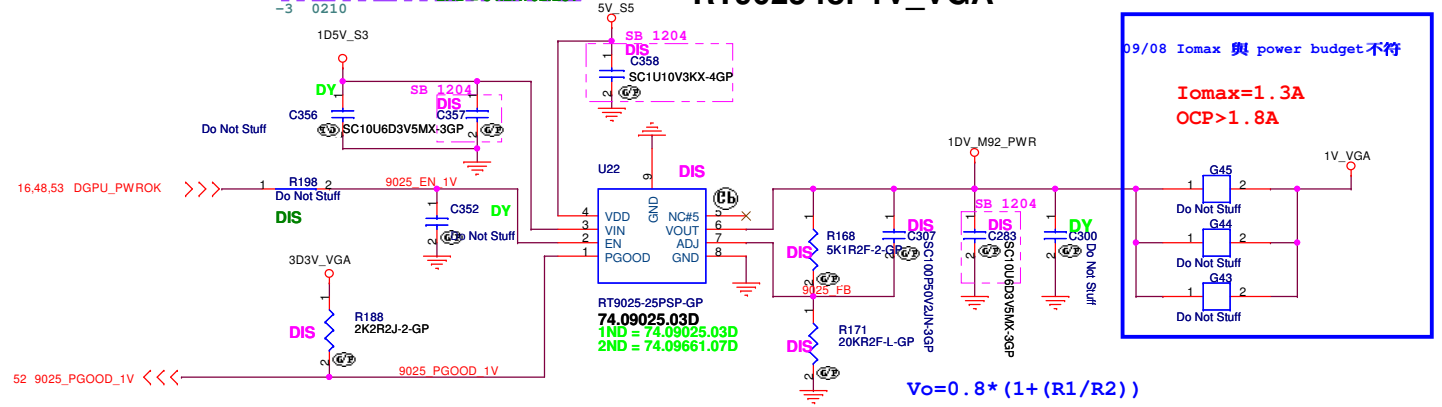


09/08 add 3D3V_S5,R837,R836

RT9026 for 0D75V_S3



RT9025 for 1V_VGA



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Taipei Hsien 221, Taiwan, R.O.C.

Title: RT9025_1D8V_1V/RT9026_0D75

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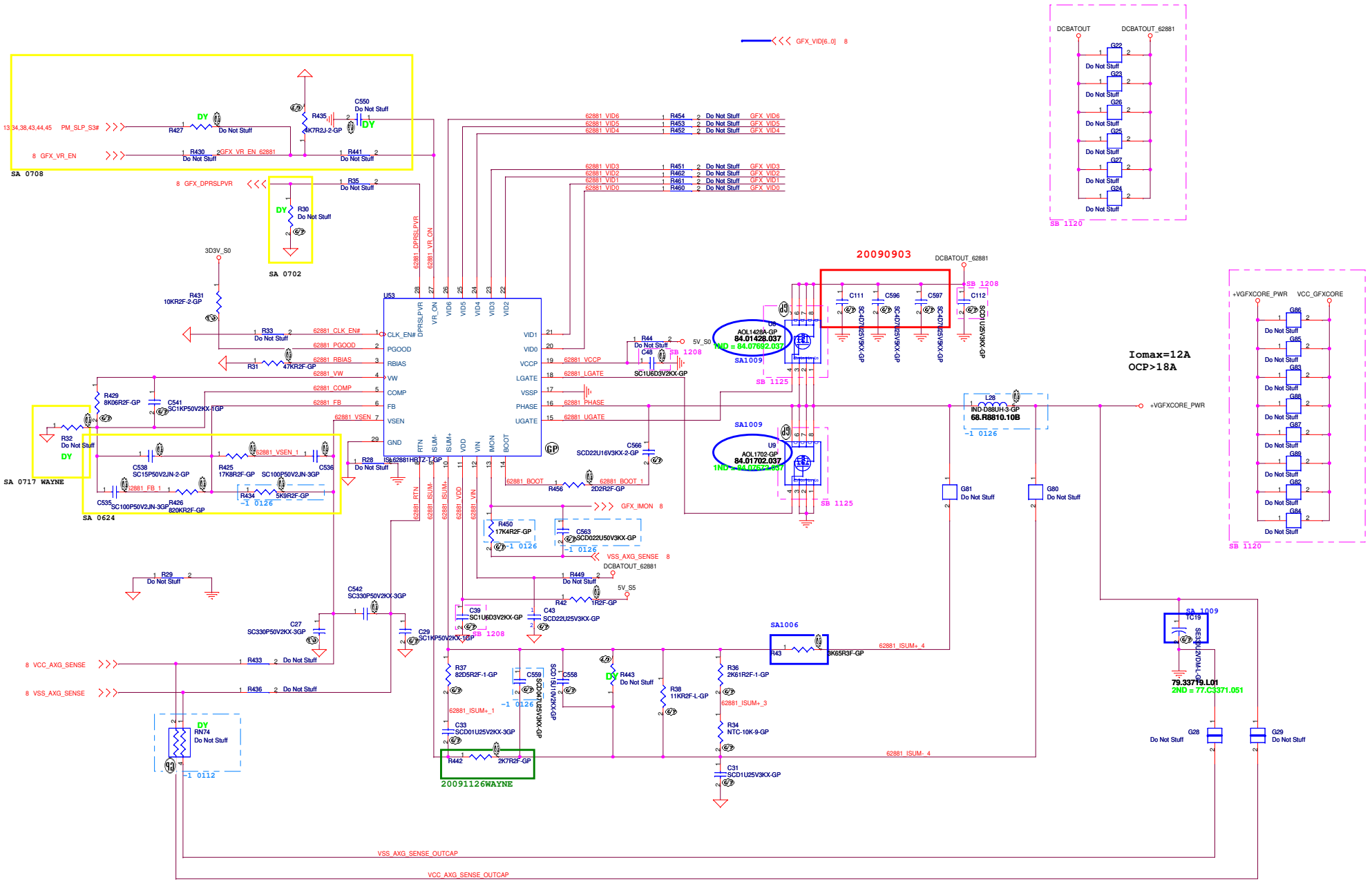

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62881 +VCC_GFXCORE

Size	Document Number	Rev
C	JM31-CP	SB

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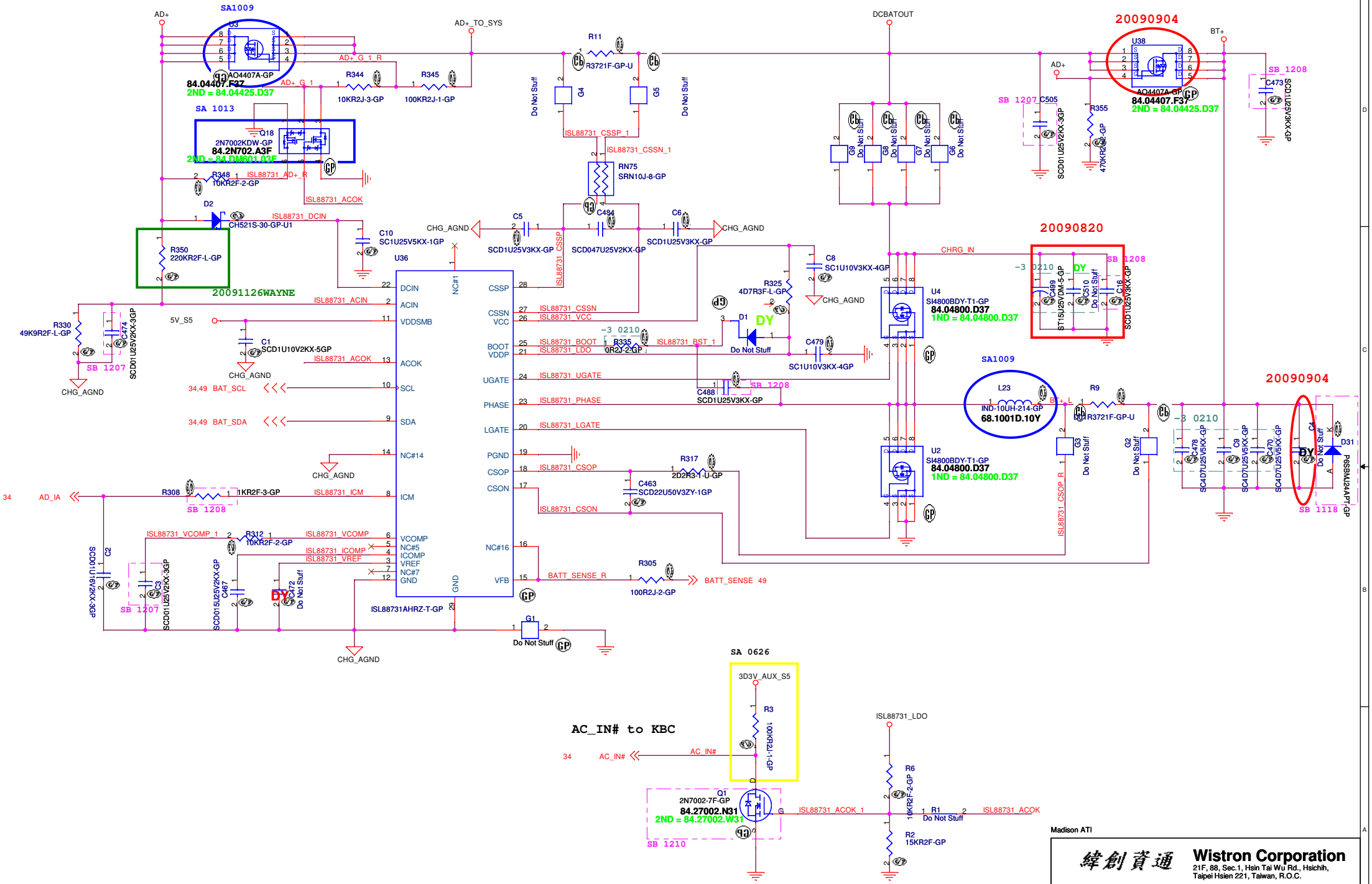
SA1009
AD+
Q3
AO4407A-GP
84.04407.F37
2ND = 84.04425.D37
AD+_G_1_R
AD+_G_1
R344
10KR2J-3-GP
R345
100KR2J-1-GP
AD+_TO_SYS
R11
R3721F-GP-U
Do Not Stuff
G4
G5
SA 1013
Q18
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
R348
10KR2F-2-GP
ISL88731_AD+_R
ISL88731_ACOK
D2
CH521S-30-GP-U1
ISL88731_DCIN
R350
220KR2F-L-GP
20091126WAYNE
C10
SC1U25V5KX-1GP
U36
ISL88731_ACIN
5V_S5
C1
SCD1U10V2KX-5GP
CHG_AGND
R330
49K9R2F-L-GP
C474
SCD01U25V2KX-3GP
SB 1207
34,49 BAT_SCL
34,49 BAT_SDA
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
NC#1
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
ISL88731AHRZ-T-GP
ISL88731_CSSP_1
ISL88731_CSSN_1
RN75
SRN10J-8-GP
C484
SCD047U25V2KX-GP
C5
SCD1U25V3KX-GP
C6
SCD1U25V3KX-GP
CHG_AGND
ISL88731_CSSP
ISL88731_CSSN
ISL88731_VCC
ISL88731_BOOT
ISL88731_LDO
ISL88731_BST_1
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
ISL88731_CSOP
ISL88731_CSON
ISL88731_ICM
ISL88731_VCOMP
ISL88731_ICOMP
ISL88731_VREF
BATT_SENSE_R
BATT_SENSE 49
R335
0R2J-2-GP
-3 0210
R325
4D7R3F-L-GP
D1
Do Not Stuff
DY
C479
SC1U10V3KX-4GP
C8
SC1U10V3KX-4GP
C488
SCD1U25V3KX-GP
SB 1208
R317
2D2R3-1-U-GP
C463
SCD22U50V3ZY-1GP
R308
1KR2F-3-GP
AD_IA
34
R312
10KR2F-2-GP
C2
C3
C467
C472
R305
100R2J-2-GP
G1
SA 0626
3D3V_AUX_S5
R3
100KR2J-1-GP
AC_IN#
AC_IN# to KBC
Q1
2N7002-7F-GP
84.27002.N31
2ND = 84.27002.W31
SB 1210
ISL88731_ACOK_1
R6
10KR2F-2-GP
R1
Do Not Stuff
R2
15KR2F-GP
ISL88731_ACOK
DCBATOUT
CHRG_IN
U4
SI4800BDY-T1-GP
84.04800.D37
1ND = 84.04800.D37
U2
SI4800BDY-T1-GP
84.04800.D37
1ND = 84.04800.D37
20090820
20090904
U38
AO4407A-GP
84.04407.F37
2ND = 84.04425.D37
SB 1207 C505
SCD01U25V2KX-3GP
R355
470KR2J-GP
BT+
SB 1208
C473
SCD1U25V5KX-GP
SA1009
L23
IND-10UH-214-GP
68.1001D.10Y
R9
R3721F-GP-U
BT+_L
G3
G2
C478
SC4D7U25V5KX-GP
C9
SC4D7U25V5KX-GP
C470
SC4D7U25V5KX-GP
C4
D31
P6SBMJ24APT-GP
SB 1118
ISL88731_CSOP_R
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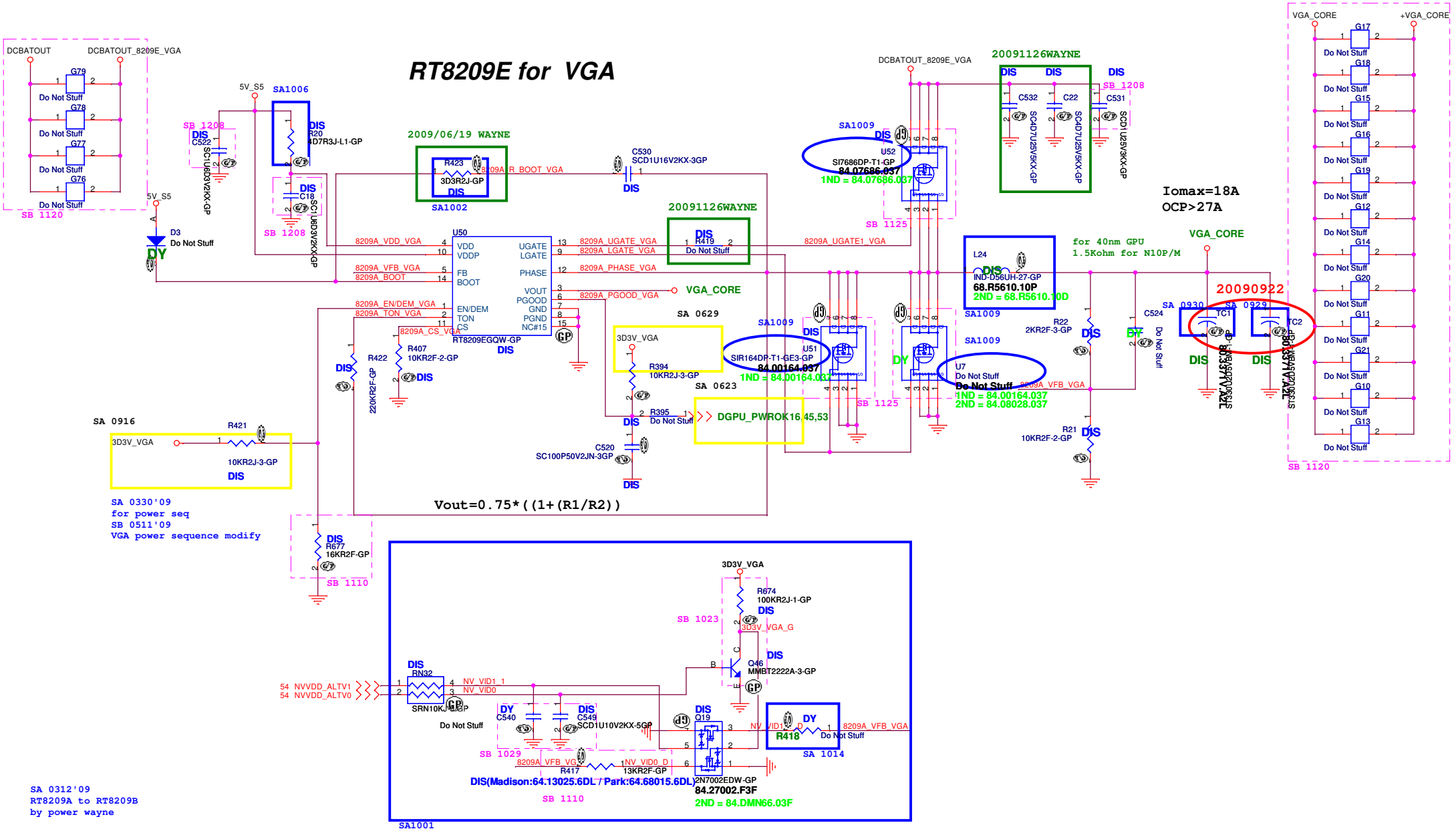
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A_CHARGER
Size
A3
Document Number
JM31-CP
Rev
-3
Date: Thursday, February 25, 2010
Sheet 47 of 62

RT8209E for VGA



PARK (6.8K)

GPIO15/VID0	VGA_CORE
0	0.90V
1	1.12V

MADISON (13K)

GPIO15/VID0	VGA_CORE
0	0.90V
1	1.02V

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *RT8209E_VGA_CORE*

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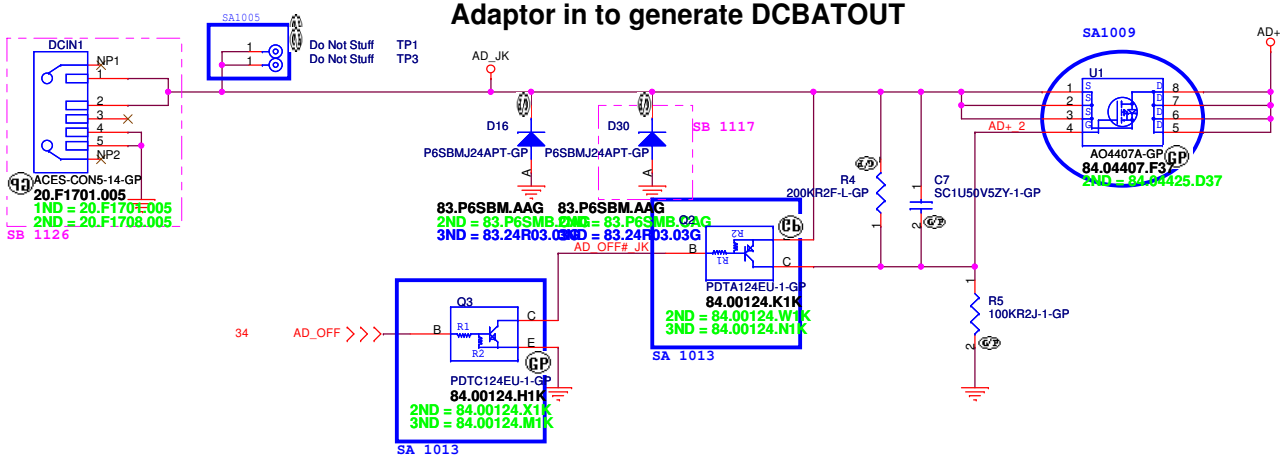
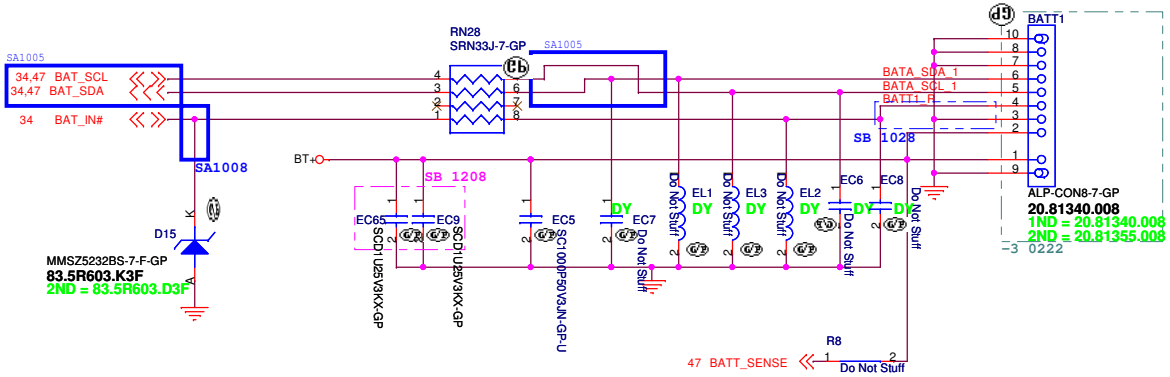
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

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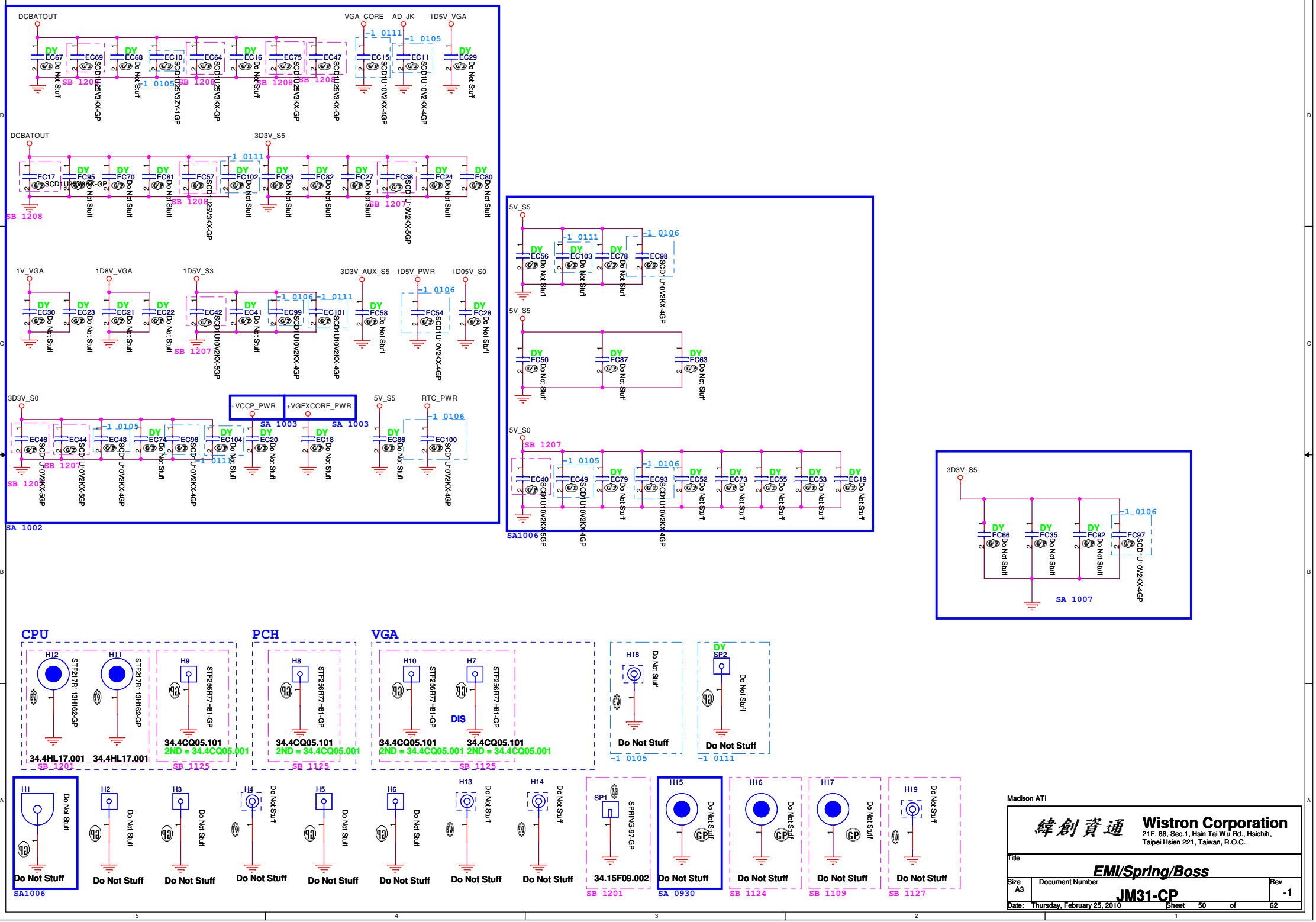

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

Size	Document Number	Rev
A3	JM31-CP	-1

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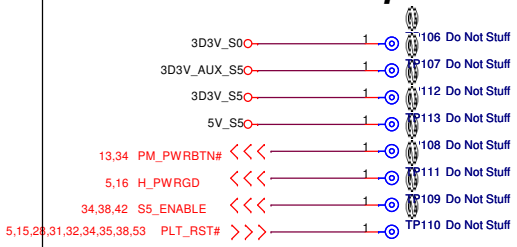
Check test point



Test Point放在Dimm Door打開可量測處

Madison ATI

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Title: ***AFTE_TP***

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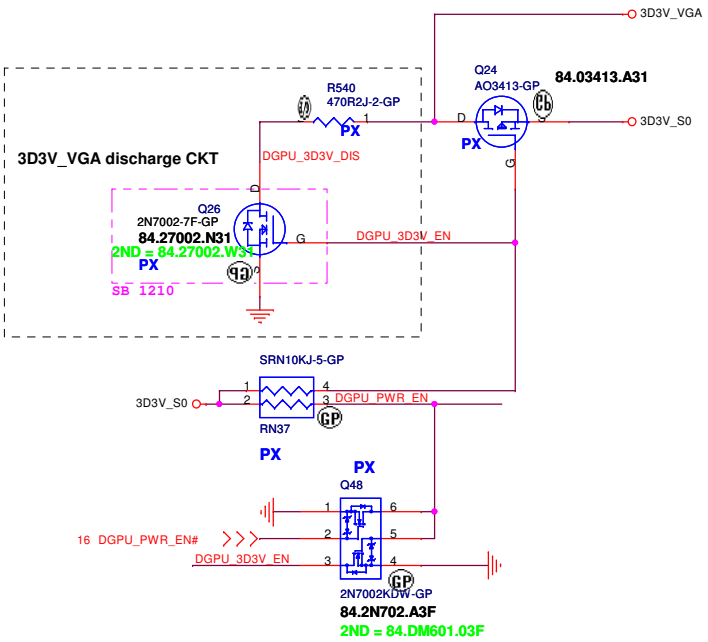
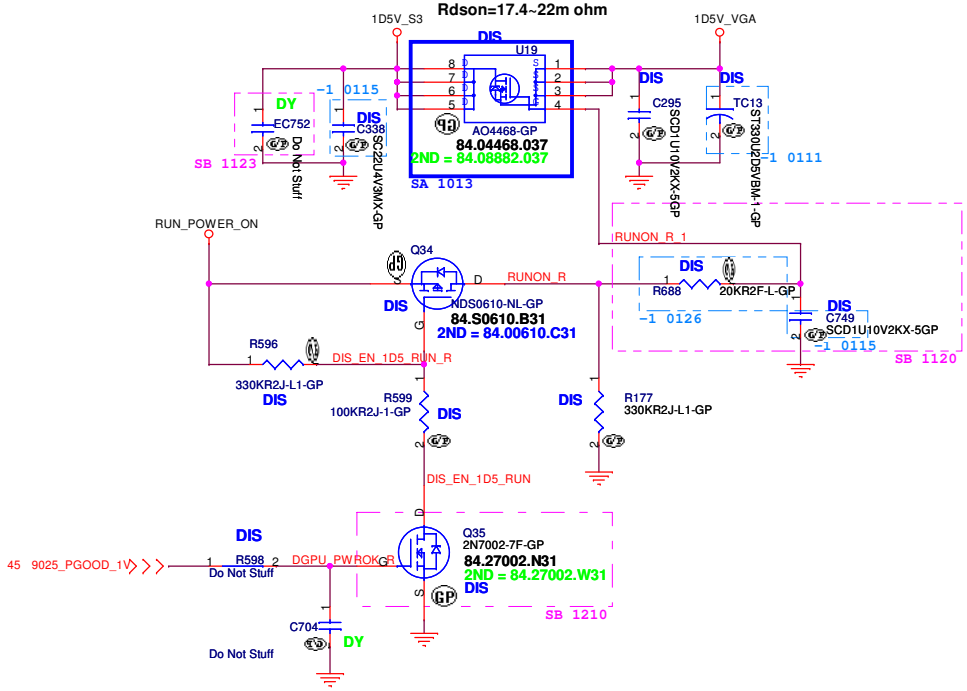
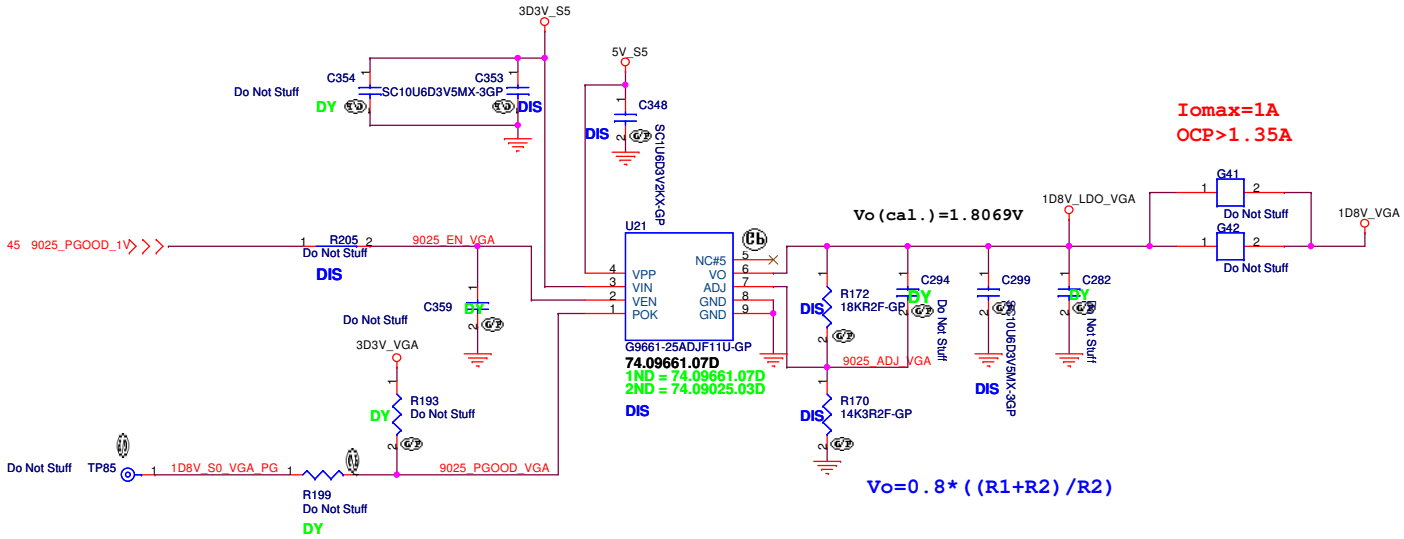
+3VS to 3.3V_DELAY Transfer



AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm



G9661 for 1D8V_VGA



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Title		
ATI_POWER		
Size: A3	Document Number: JM31-CP	Rev: -1
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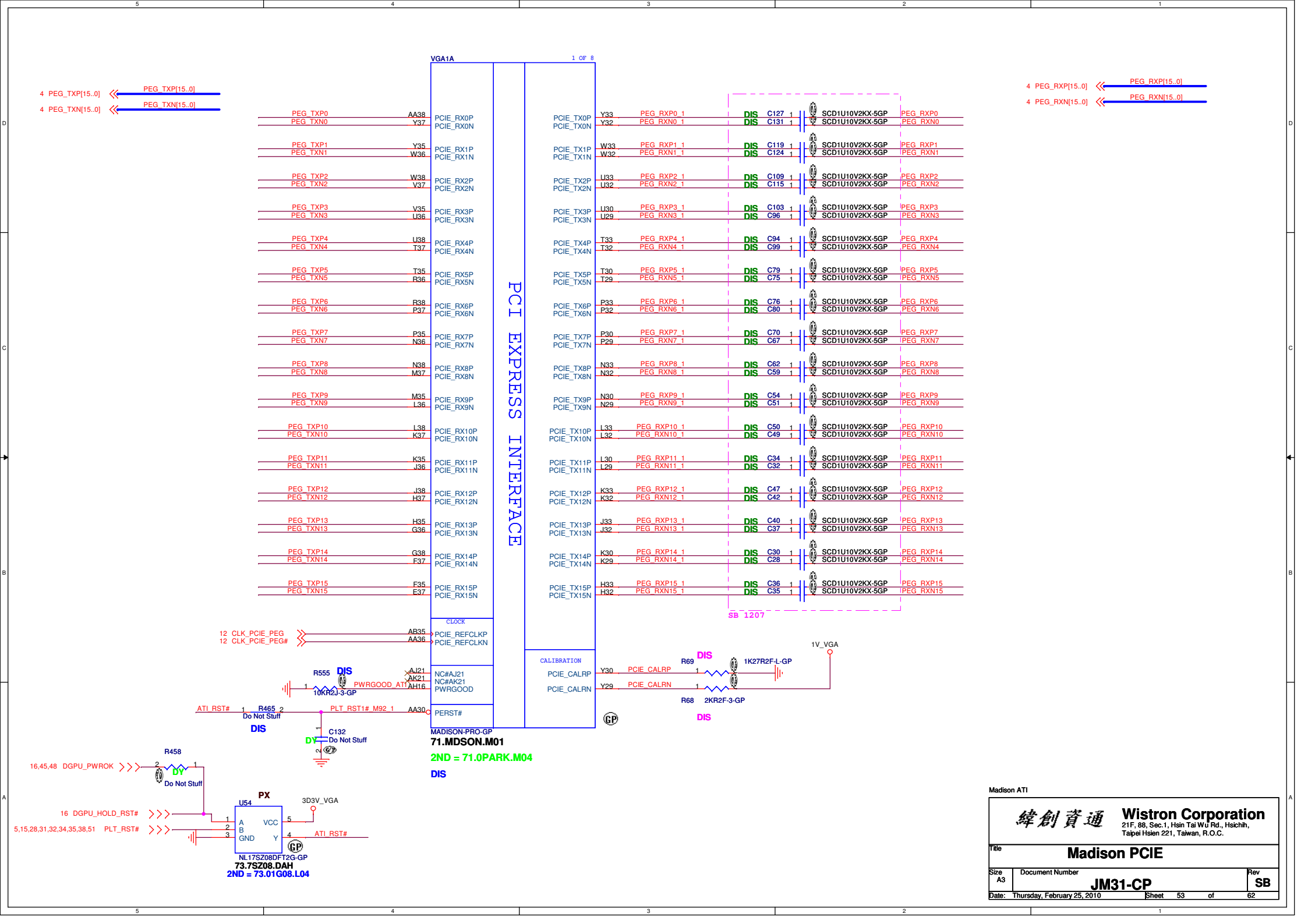

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Title	Madison PCIE	
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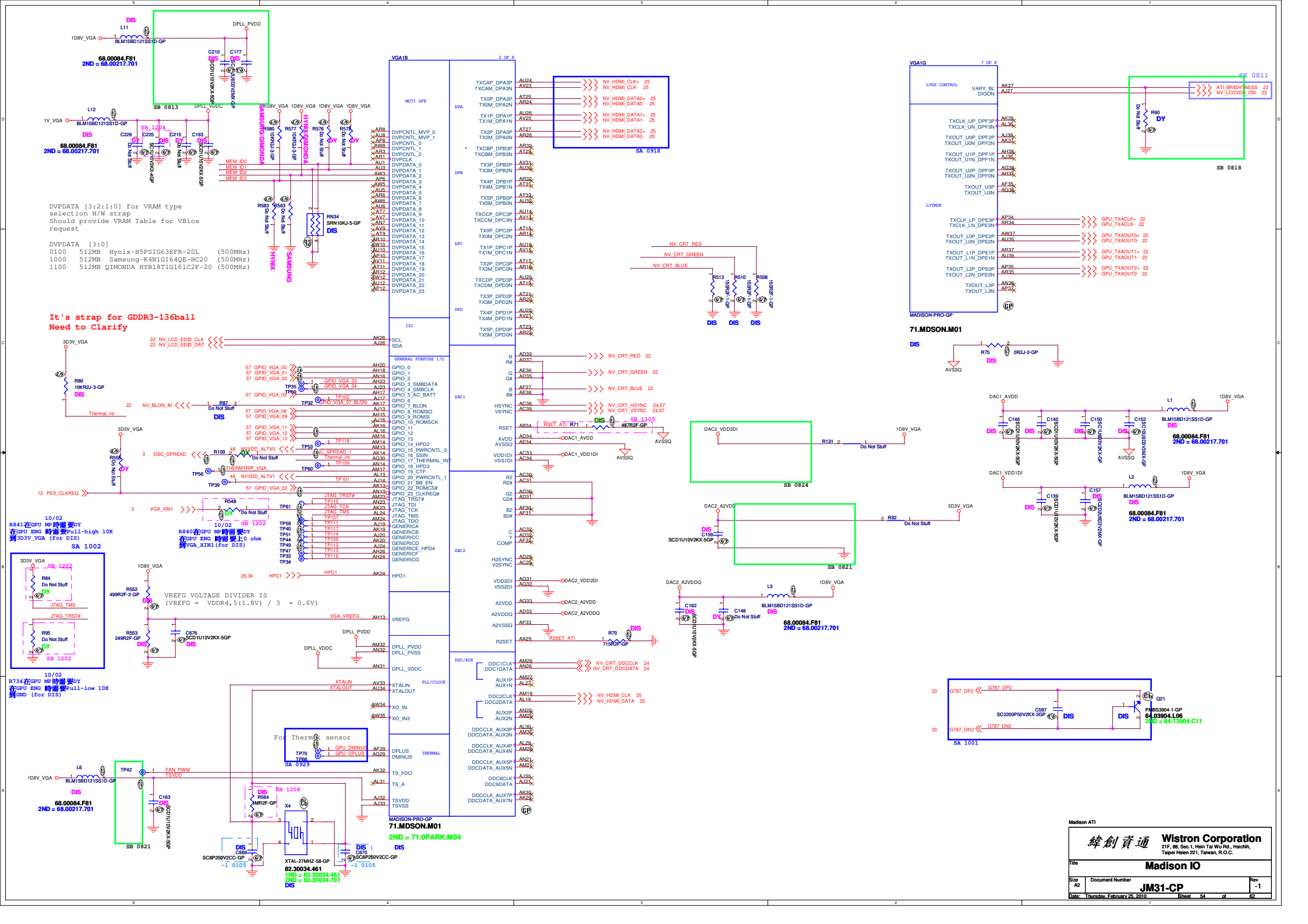
DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request
DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)
It's strap for GDDR3-136ball
Need to Clarify
VREFG VOLTAGE DIVIDER IS (VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
For Thermal sensor
VGA1B
VGA1G
MADISON-PRO-GP
71.MDSON.M01
2ND = 71.0PARK.M04
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Madison IO
JM31-CP
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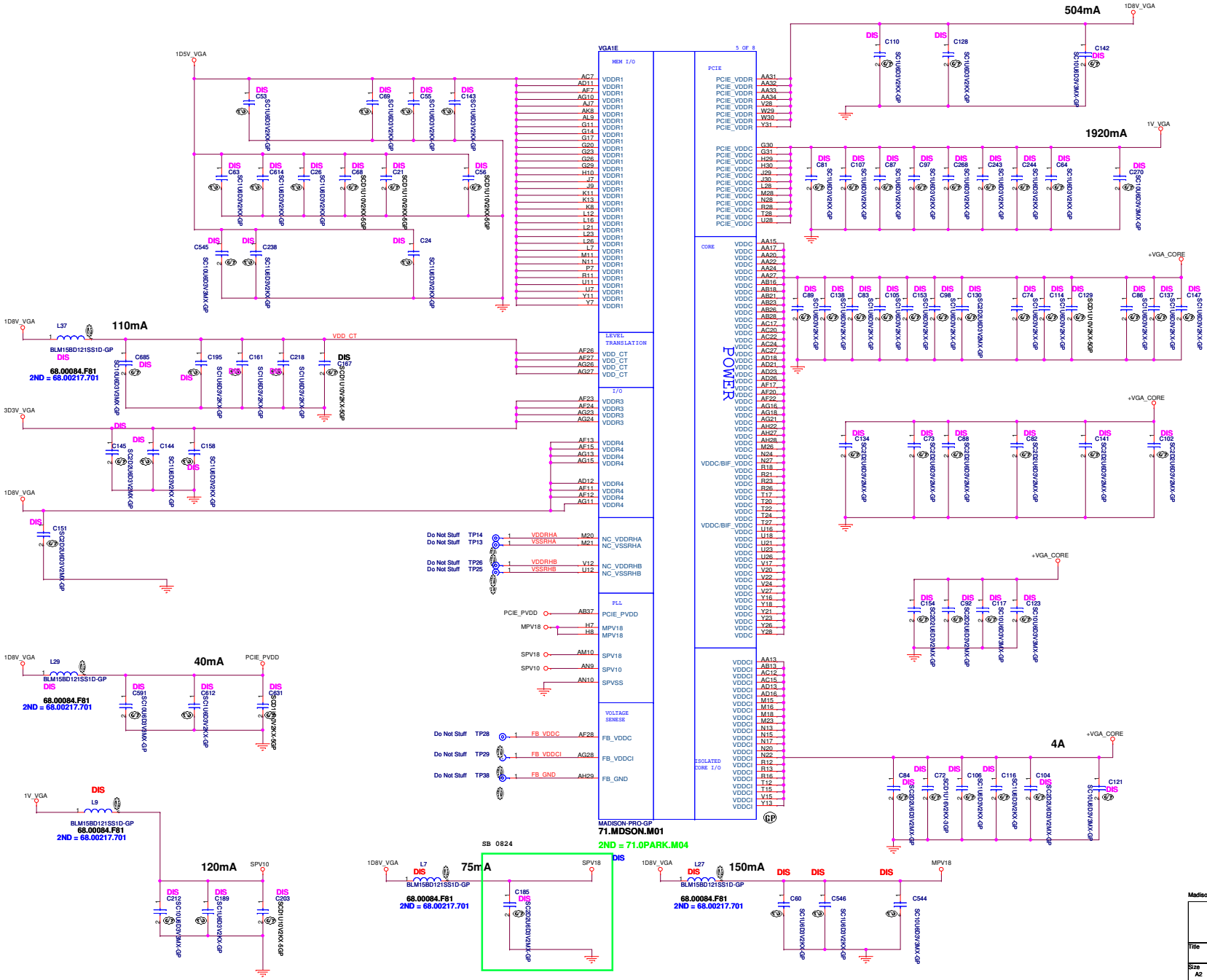
504mA
1920mA
+VGA_CORE
4A
110mA
40mA
120mA
75mA
150mA
1D5V_VGA
1D8V_VGA
3D3V_VGA
1V_VGA
VGA1E
MADISON-PRO-GP
71.MDSON.M01
2ND = 71.0PARK.M04
SB 0824
Madison ATI
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Taipei Hsien 221, Taiwan, R.O.C.
Madison POWER
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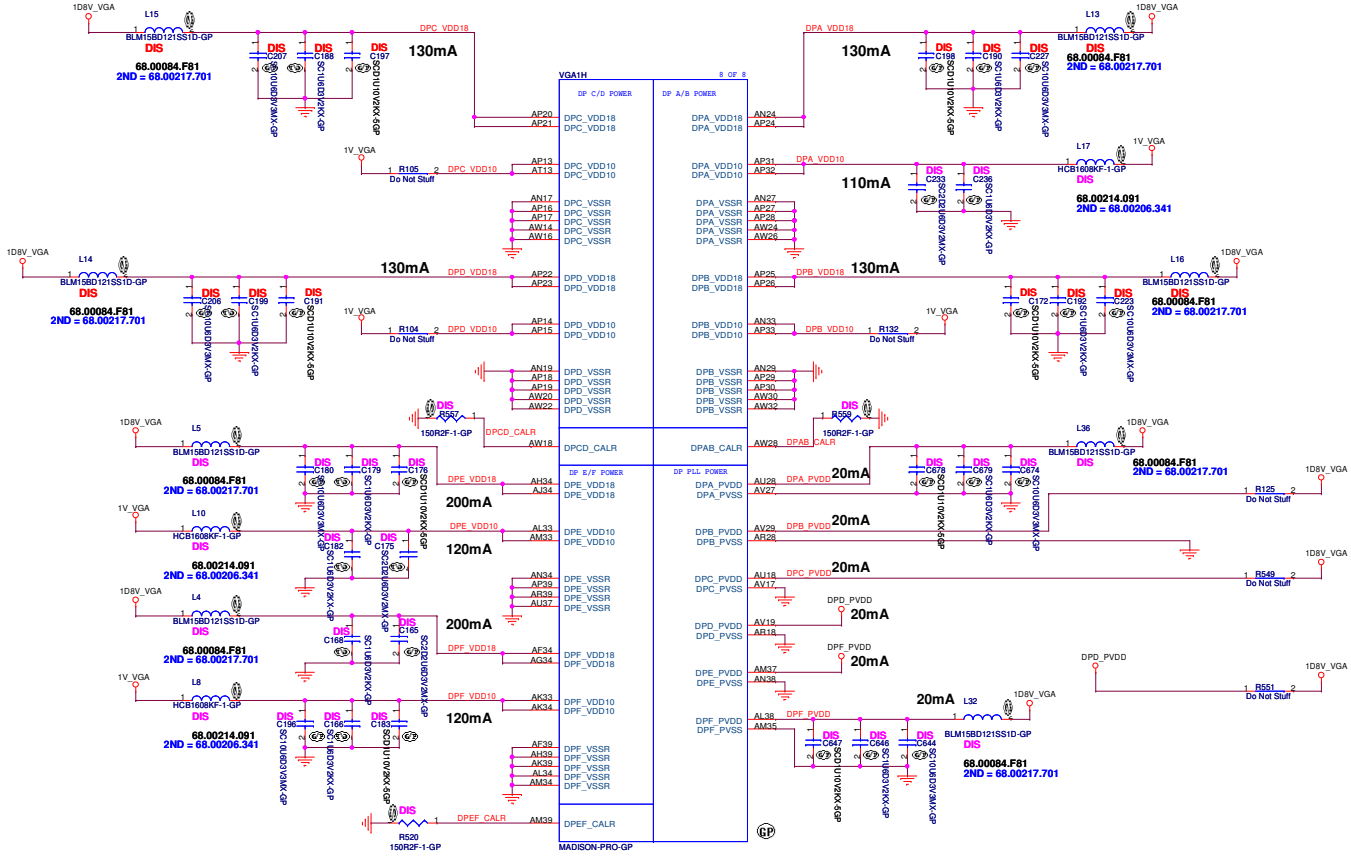

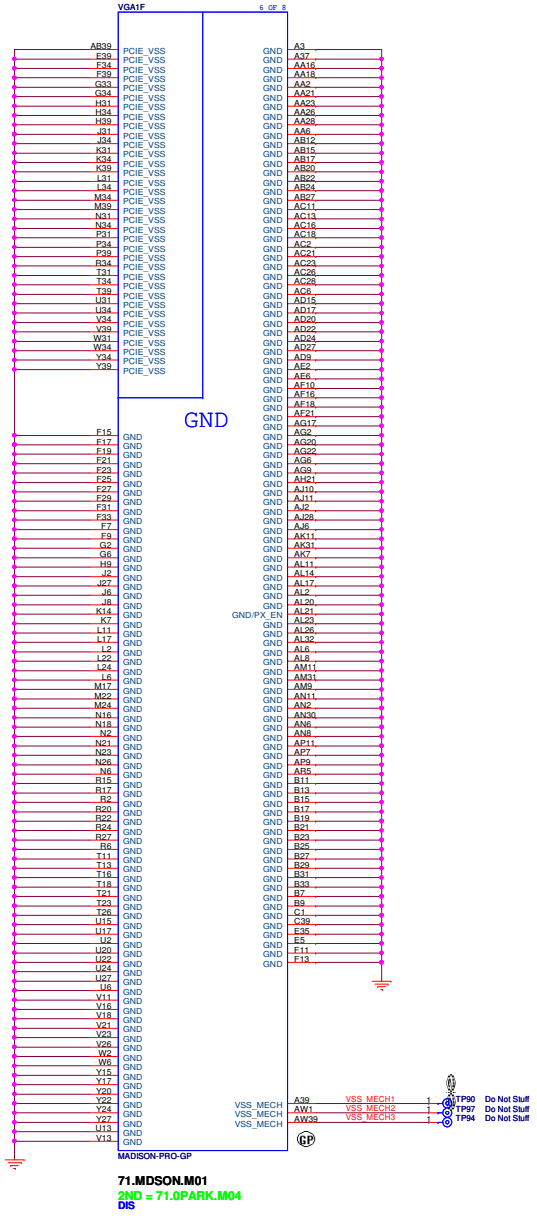

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Title	DP POWER_GND	
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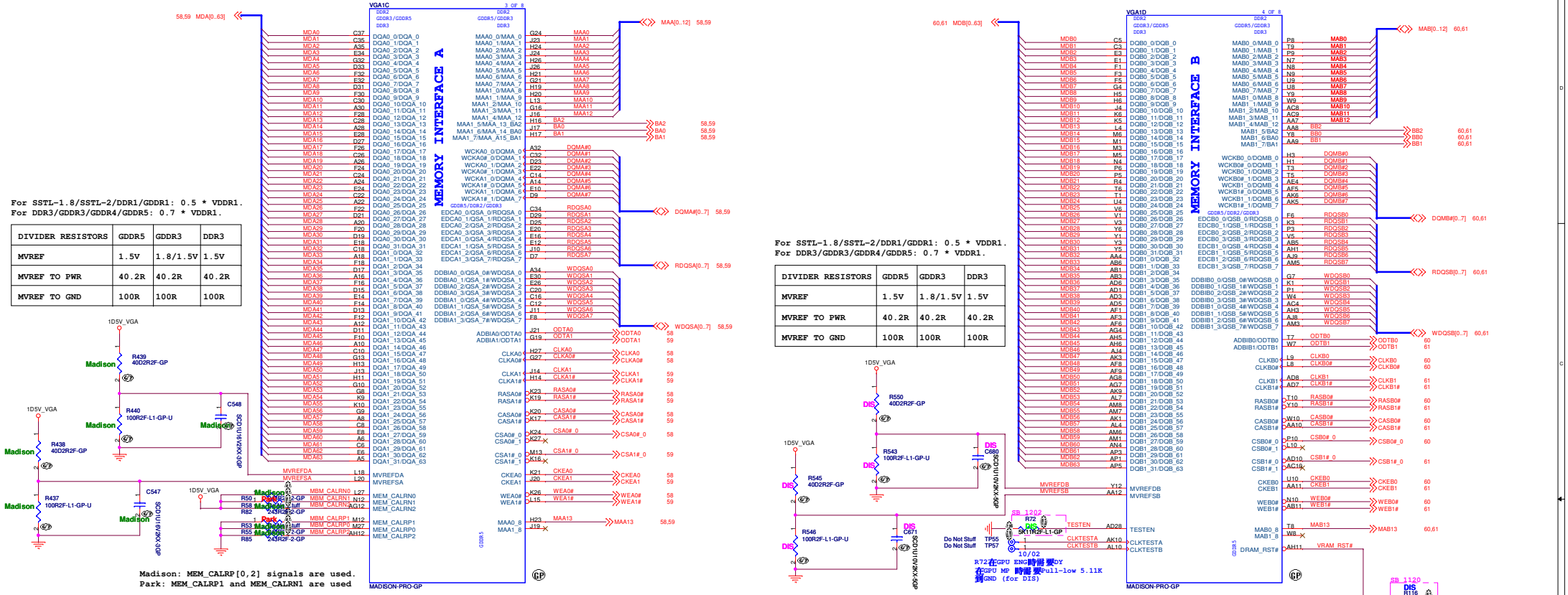

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

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Title: Madison Memory / Straps

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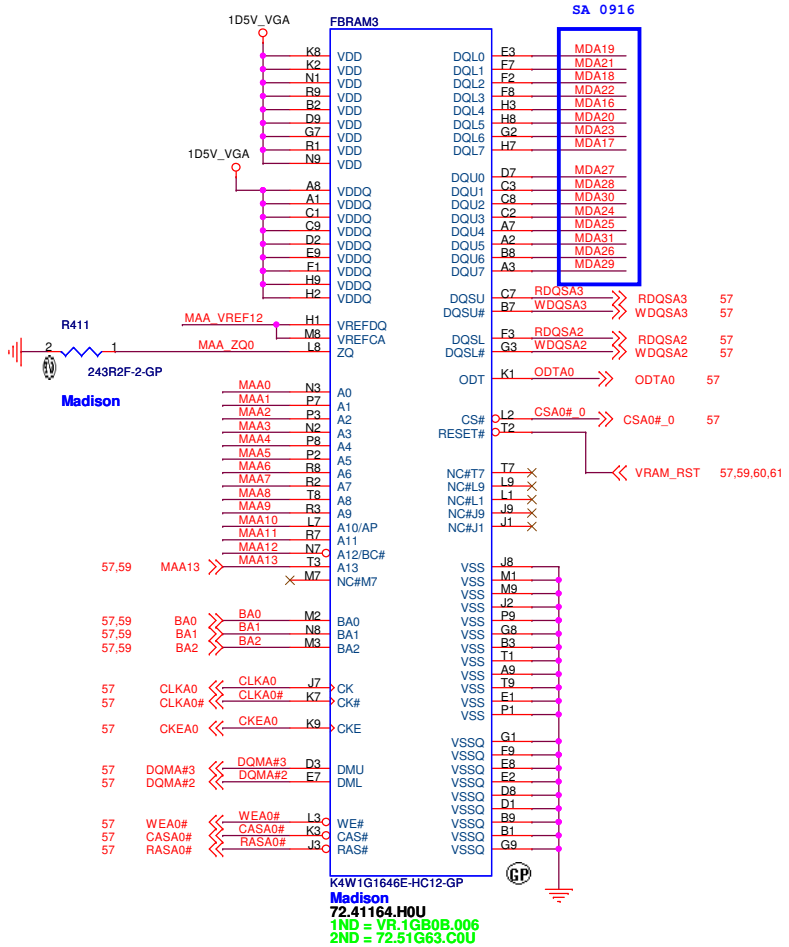
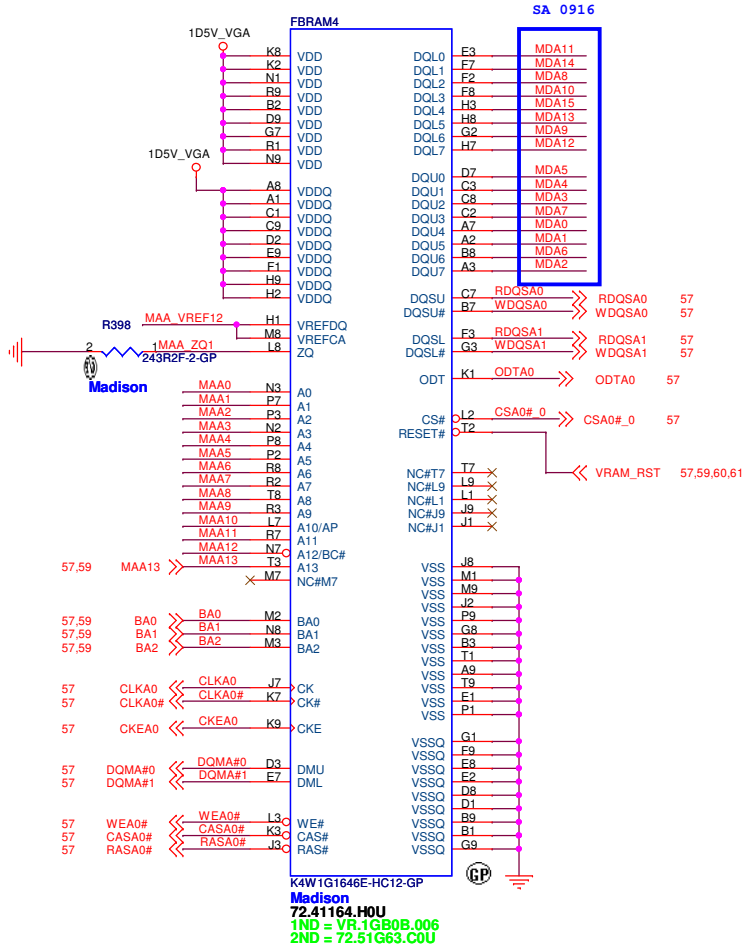
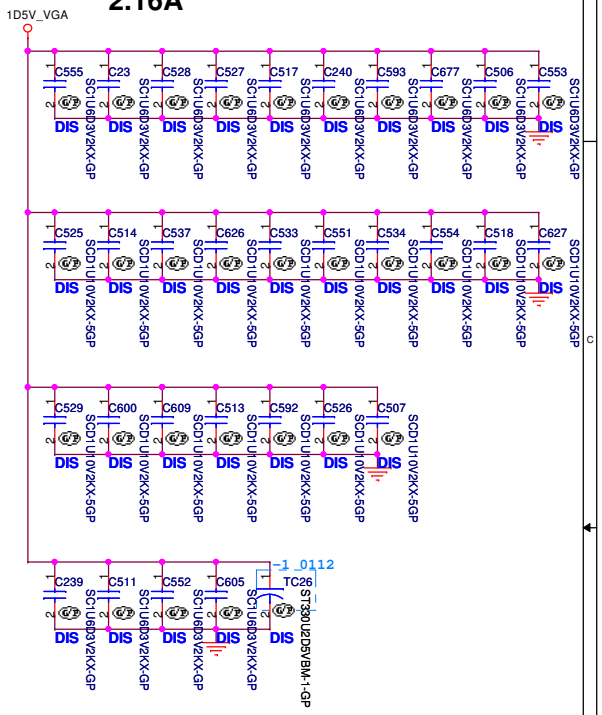
DDR3







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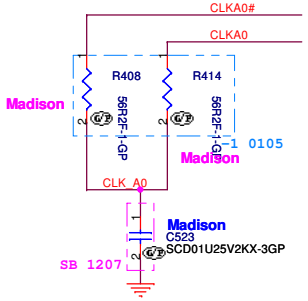
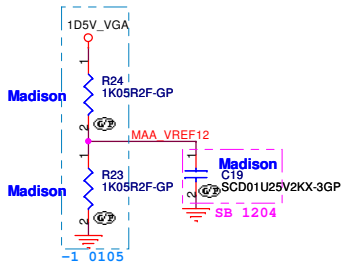
HYNIX: 72.51G63.C0U(VR.1GB0G.004)





57,59 DQMA#[0..7]

57,59 RDQSA[0..7]

57,59 WDQSA[0..7]

57,59 MAA[0..12] MAA[0..12]

57,59 MDA[0..63] MDA[0..63]

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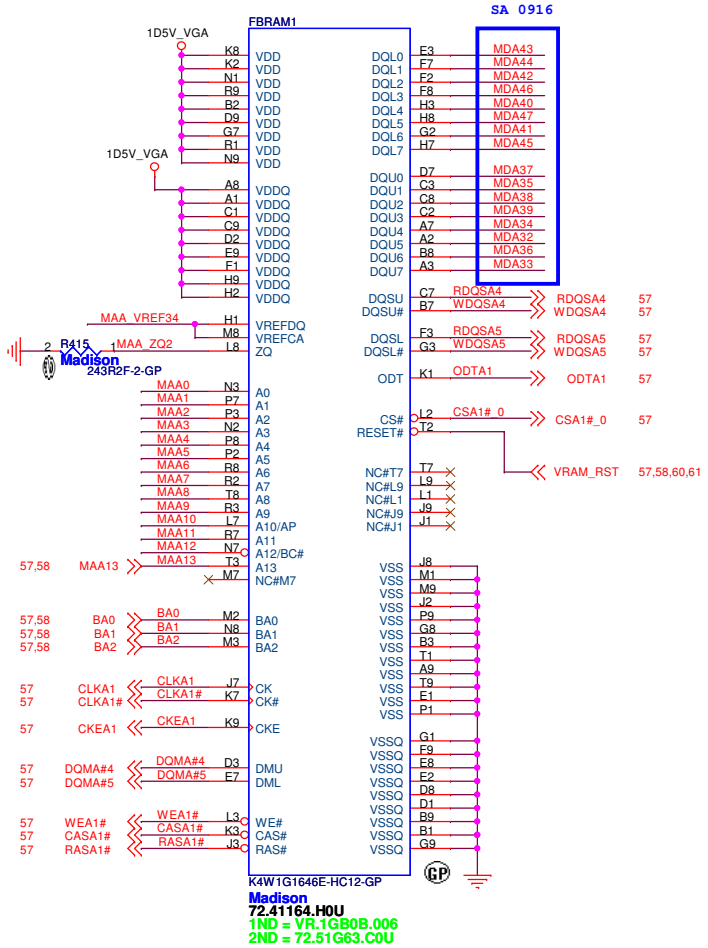
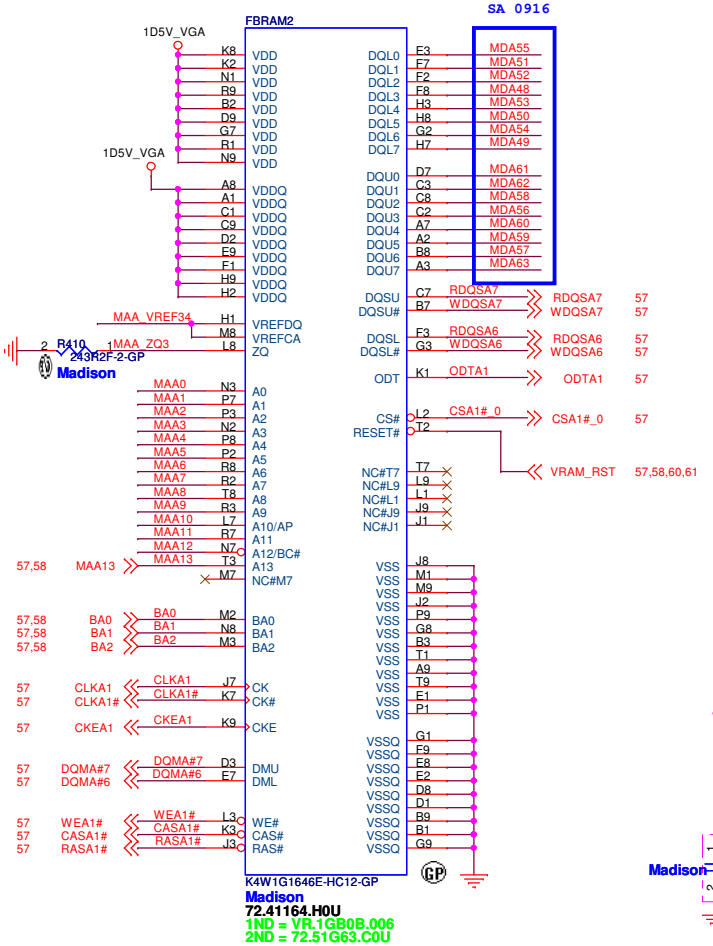
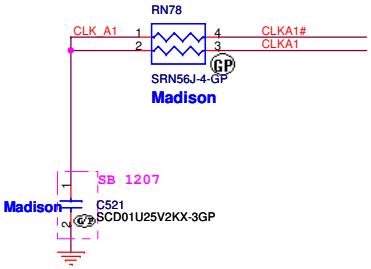
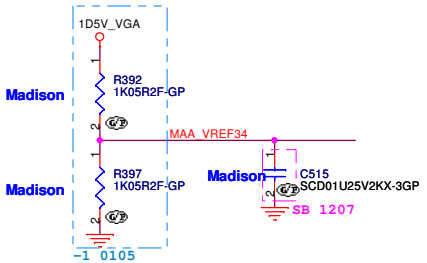
DDR3









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HYNIX: 72.51G63.C0U(VR.1GB0G.004)

57,58 DQMA#[0..7]
57,58 RDQSA[0..7]
57,58 WDQSA[0..7]
57,58 MAA[0..12] MAA[0..12]
57,58 MDA[0..63] MDA[0..63]

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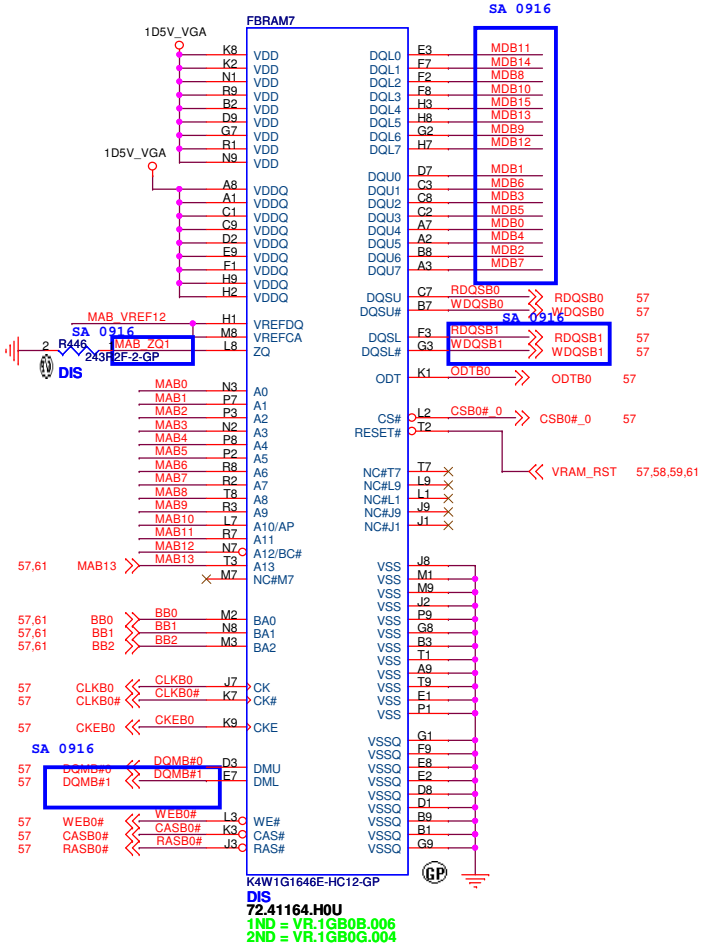
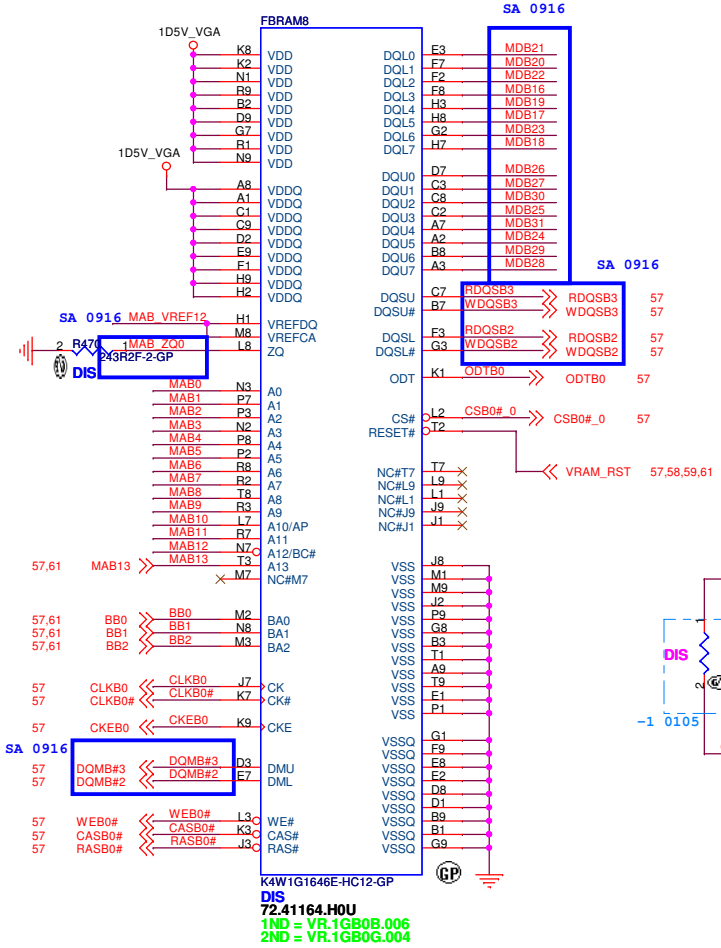
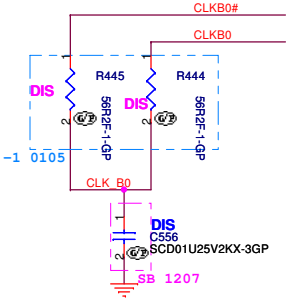
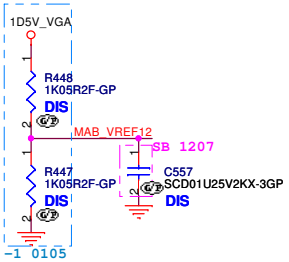
DDR3









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HYNIX: 72.51G63.C0U(VR.1GB0G.004)

57,61 DQMB#[0..7]
57,61 RDQSB[0..7]
57,61 WDQSB[0..7]
57,61 MAB[0..12] MAB[0..12]
57,61 MDB[0..63] MDB[0..63]

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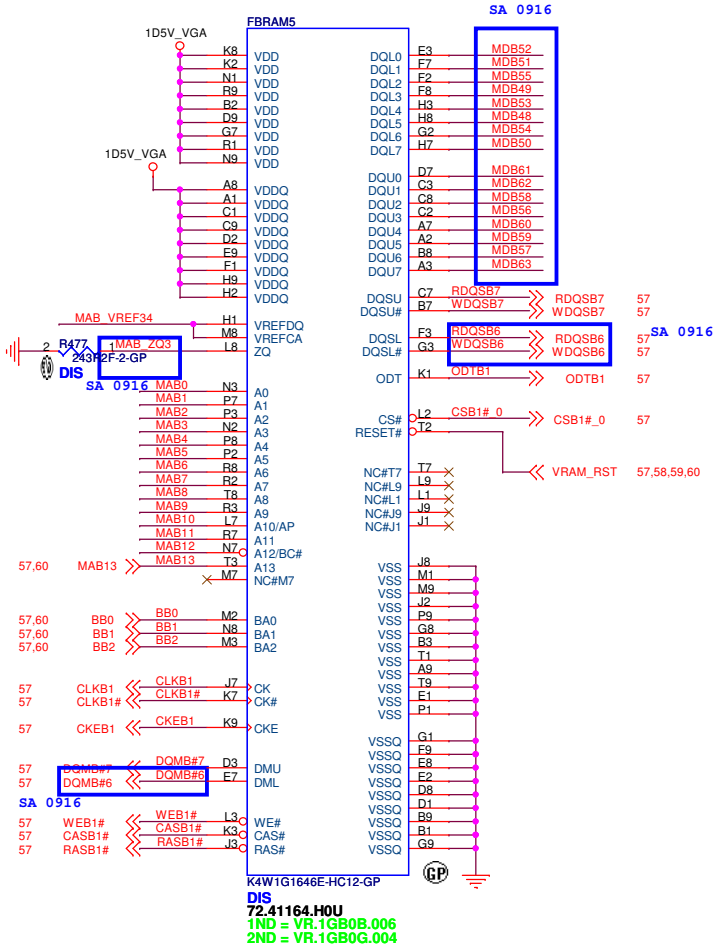
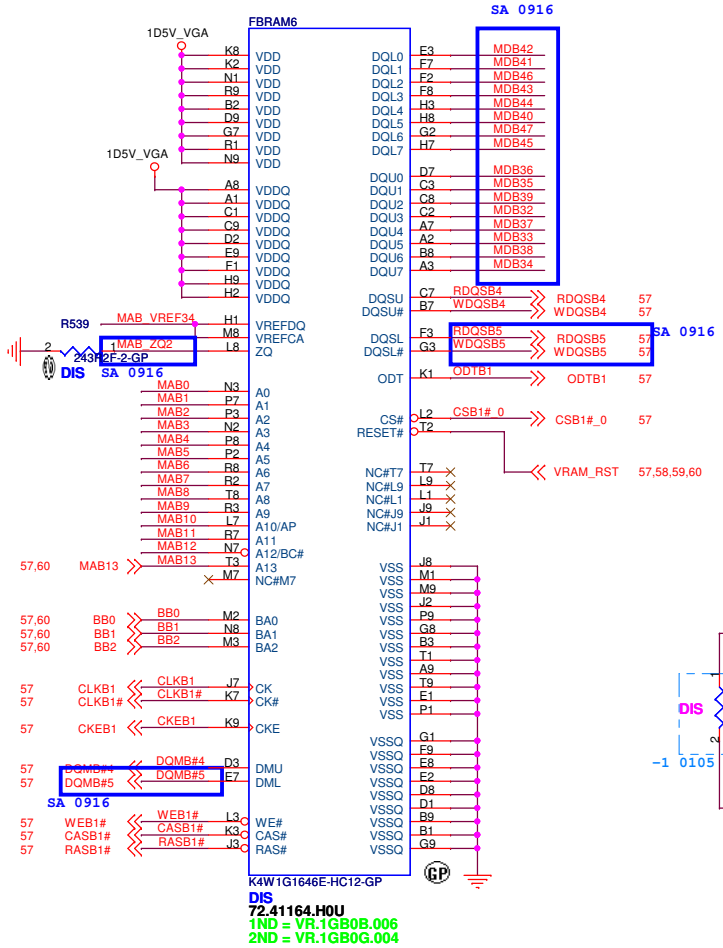
DDR3





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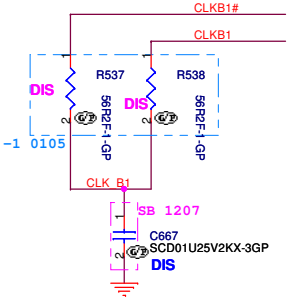

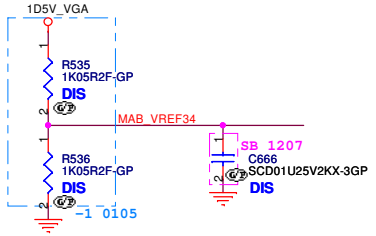

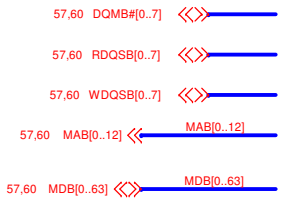

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Title

Modify History

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