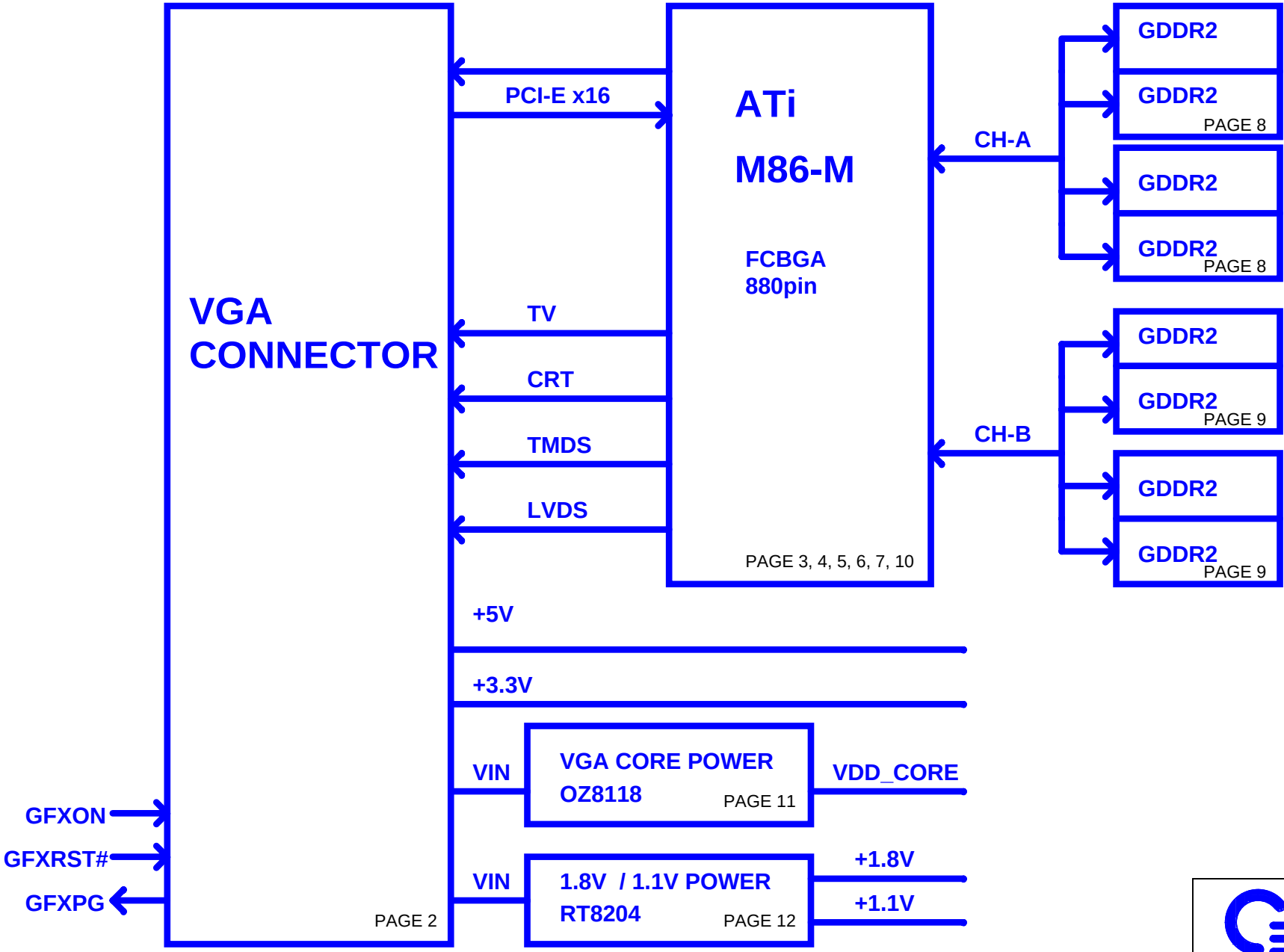
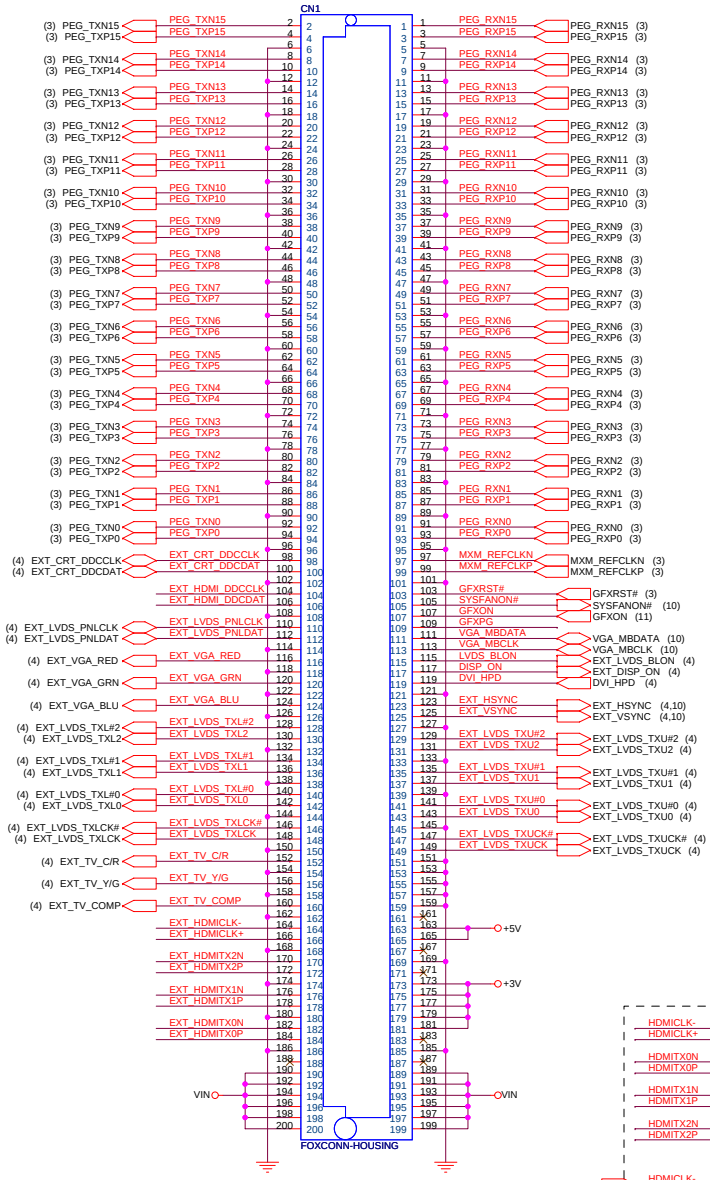
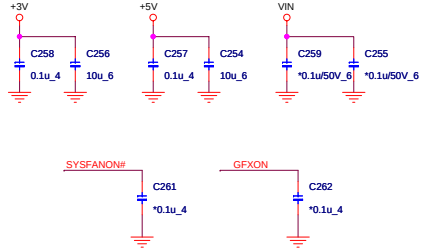


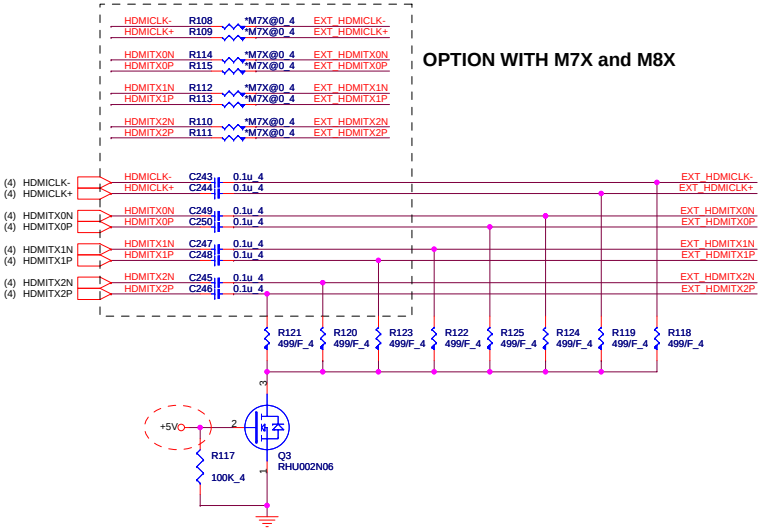
PROJECT :BD3
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Wednesday, November 07, 2007 Sheet 1 of 13



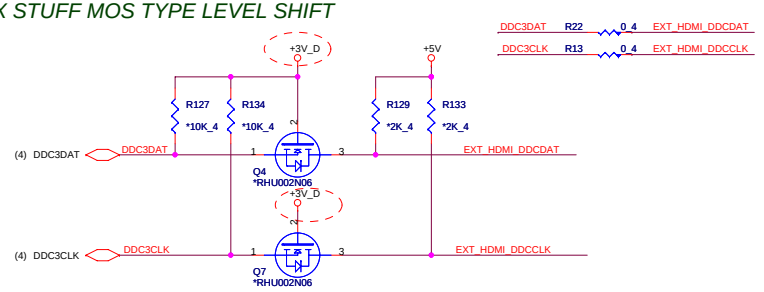




OPTION WITH M7X and M8X

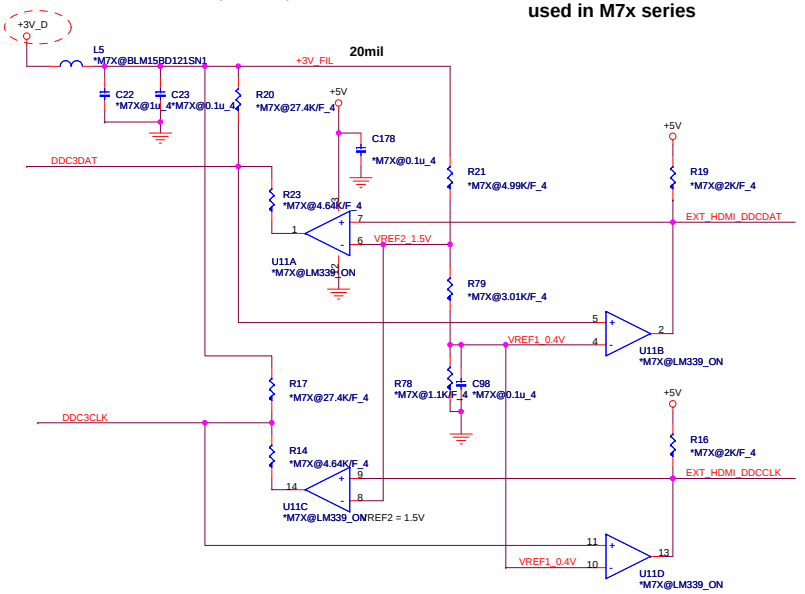
COMPARATOR LEVEL SHIFT LOGIC

M8X STUFF MOS TYPE LEVEL SHIFT

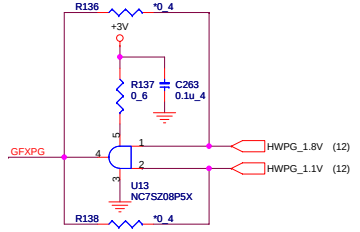


M7X STUFF OP-AMP (LM339) TYPE LEVEL SHIFT

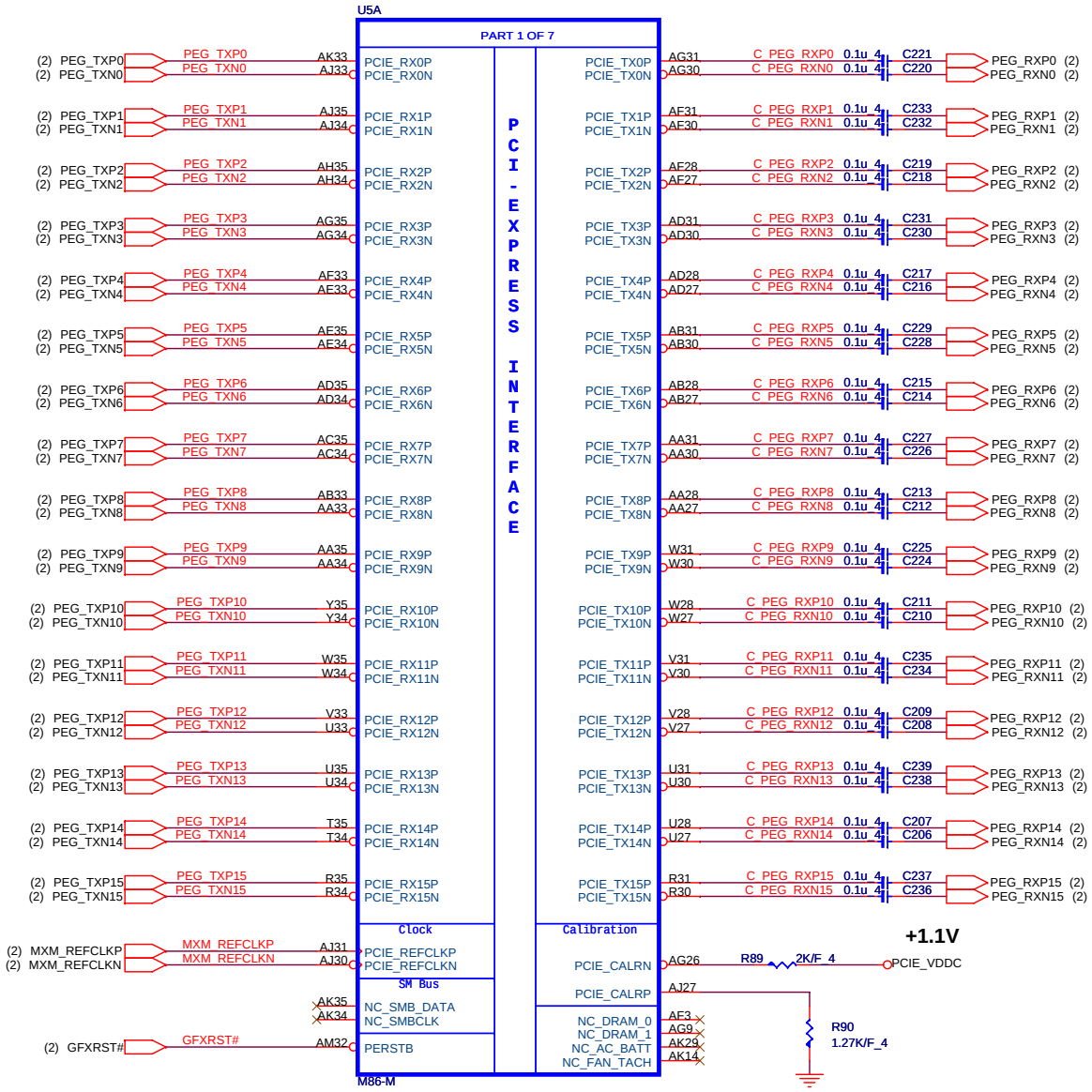
used in M7x series



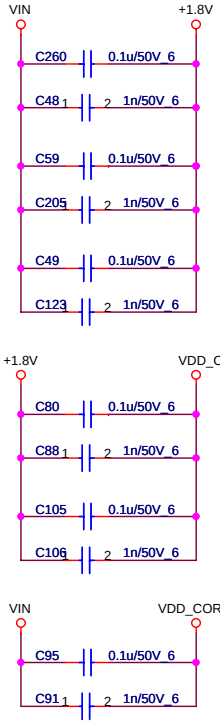
Fine-tune Power-on sequence



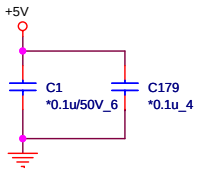
PROJECT :BD3		
Quanta Computer Inc.		
Size	Document Number: VGA CONNECTOR	Rev: 1A
Date: Monday, November 12, 2007	Sheet 2 of 13	



STITCH CAPACITORS

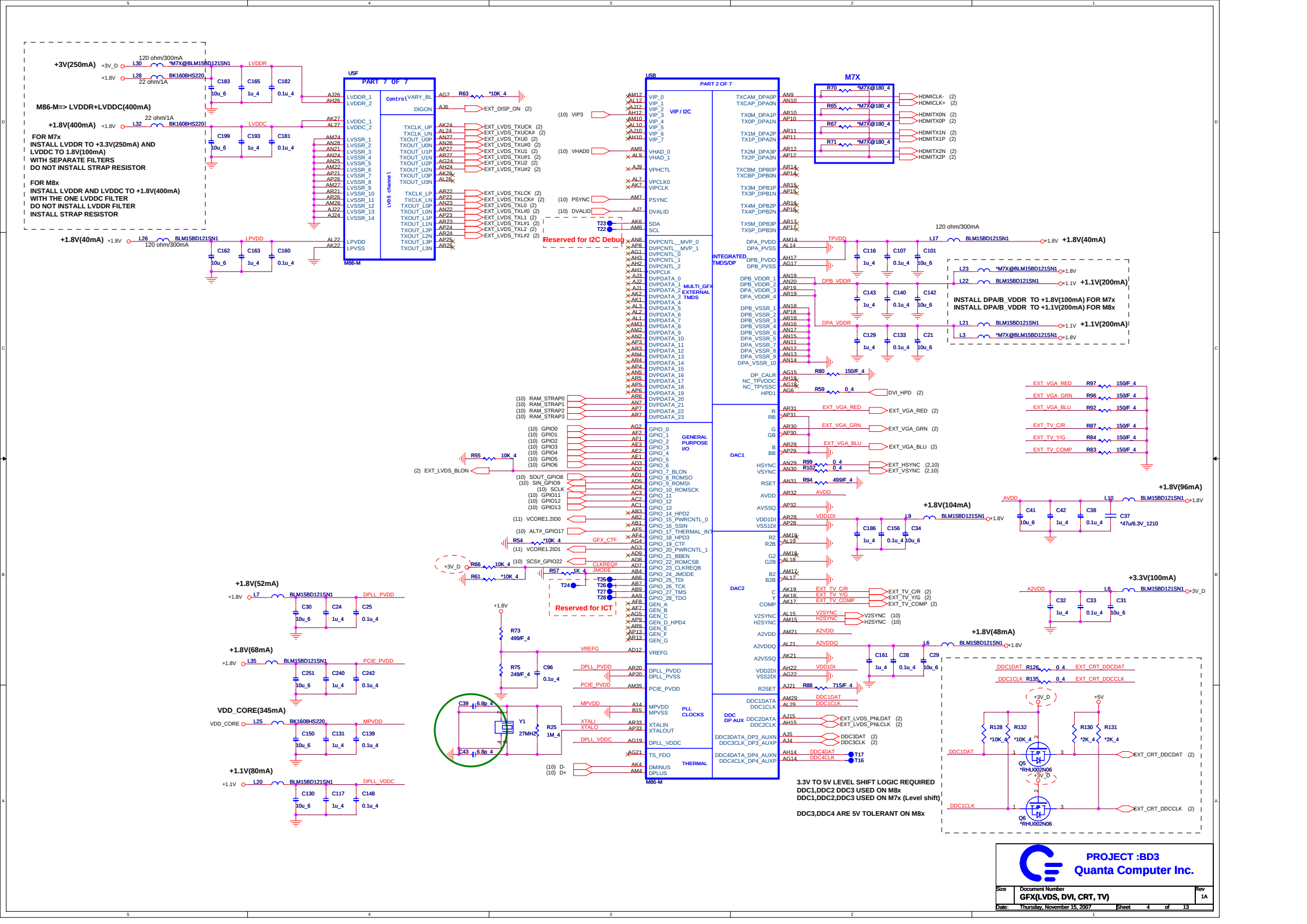


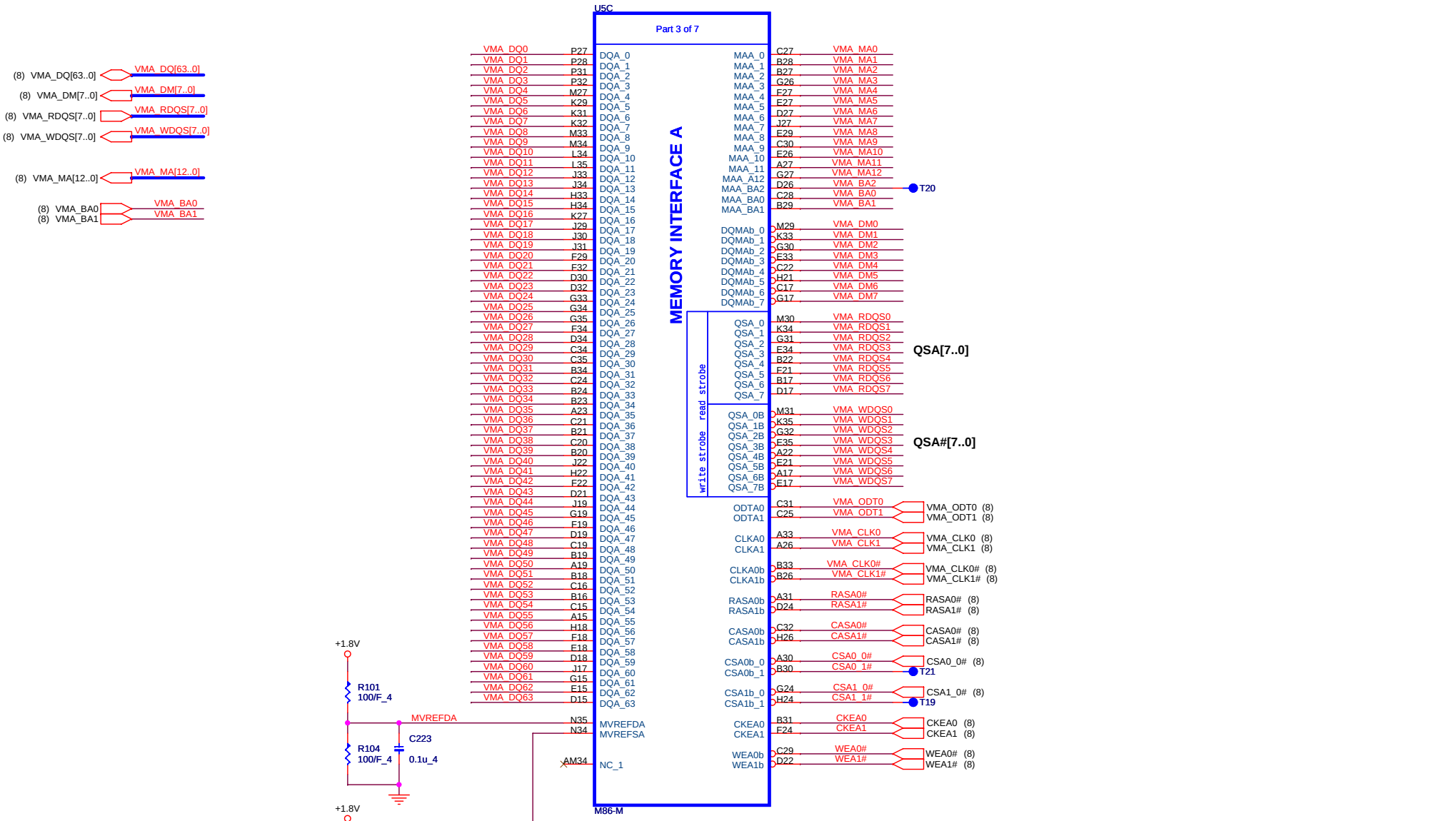
EMI CAP.



PROJECT :BD3
Quanta Computer Inc.

Size	Document Number	Rev
	GFX(PCIE I/F)	1A
Date: Thursday, November 08, 2007	Sheet 3 of 13	

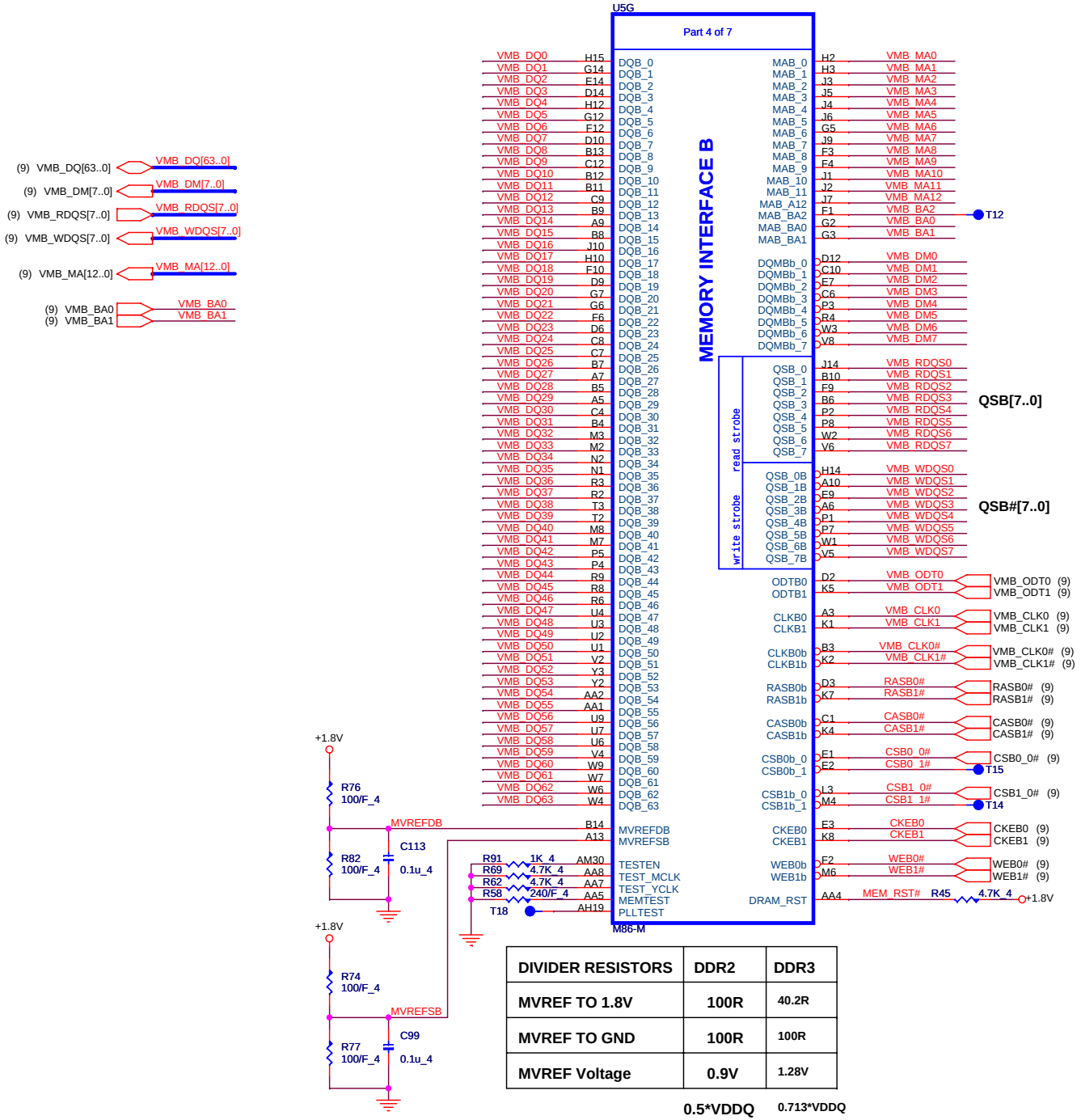

+3V(250mA)
120 ohm/300mA
*M7X@BLM15BD121SN1
22 ohm/1A
BK1608HS220
M86-M=> LVDDR+LVDDC(400mA)
+1.8V(400mA)
FOR M7x
INSTALL LVDDR TO +3.3V(250mA) AND
LVDDC TO 1.8V(100mA)
WITH SEPARATE FILTERS
DO NOT INSTALL STRAP RESISTOR
FOR M8x
INSTALL LVDDR AND LVDDC TO +1.8V(400mA)
WITH THE ONE LVDDC FILTER
DO NOT INSTALL LVDDR FILTER
INSTALL STRAP RESISTOR
+1.8V(40mA)
U5F
PART 7 OF 7
M86-M
U5B
PART 2 OF 7
M86-M
M7X
Reserved for I2C Debug
Reserved for ICT
INTEGRATED TMDS/DP
MULTI_GFX EXTERNAL TMDS
GENERAL PURPOSE I/O
PLL CLOCKS
THERMAL
DAC1
DAC2
DDC DP AUX
+1.8V(104mA)
+1.8V(96mA)
+3.3V(100mA)
+1.8V(48mA)
+1.8V(52mA)
+1.8V(68mA)
VDD_CORE(345mA)
+1.1V(80mA)
+1.1V(200mA)
INSTALL DPA/B_VDDR TO +1.8V(100mA) FOR M7x
INSTALL DPA/B_VDDR TO +1.1V(200mA) FOR M8x
3.3V TO 5V LEVEL SHIFT LOGIC REQUIRED
DDC1,DDC2 DDC3 USED ON M8x
DDC1,DDC2,DDC3 USED ON M7x (Level shift)
DDC3,DDC4 ARE 5V TOLERANT ON M8x
PROJECT :BD3
Quanta Computer Inc.
GFX(LVDS, DVI, CRT, TV)
Thursday, November 15, 2007
Sheet 4 of 13



DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R
MVREF Voltage	0.9V	1.28V
	0.5*VDDQ	0.713*VDDQ

PROJECT :BD3
Quanta Computer Inc.

Size	Document Number	Rev
	GFX(MEM I/F 1/2)	1A
Date: Monday, November 12, 2007	Sheet 5 of 13	



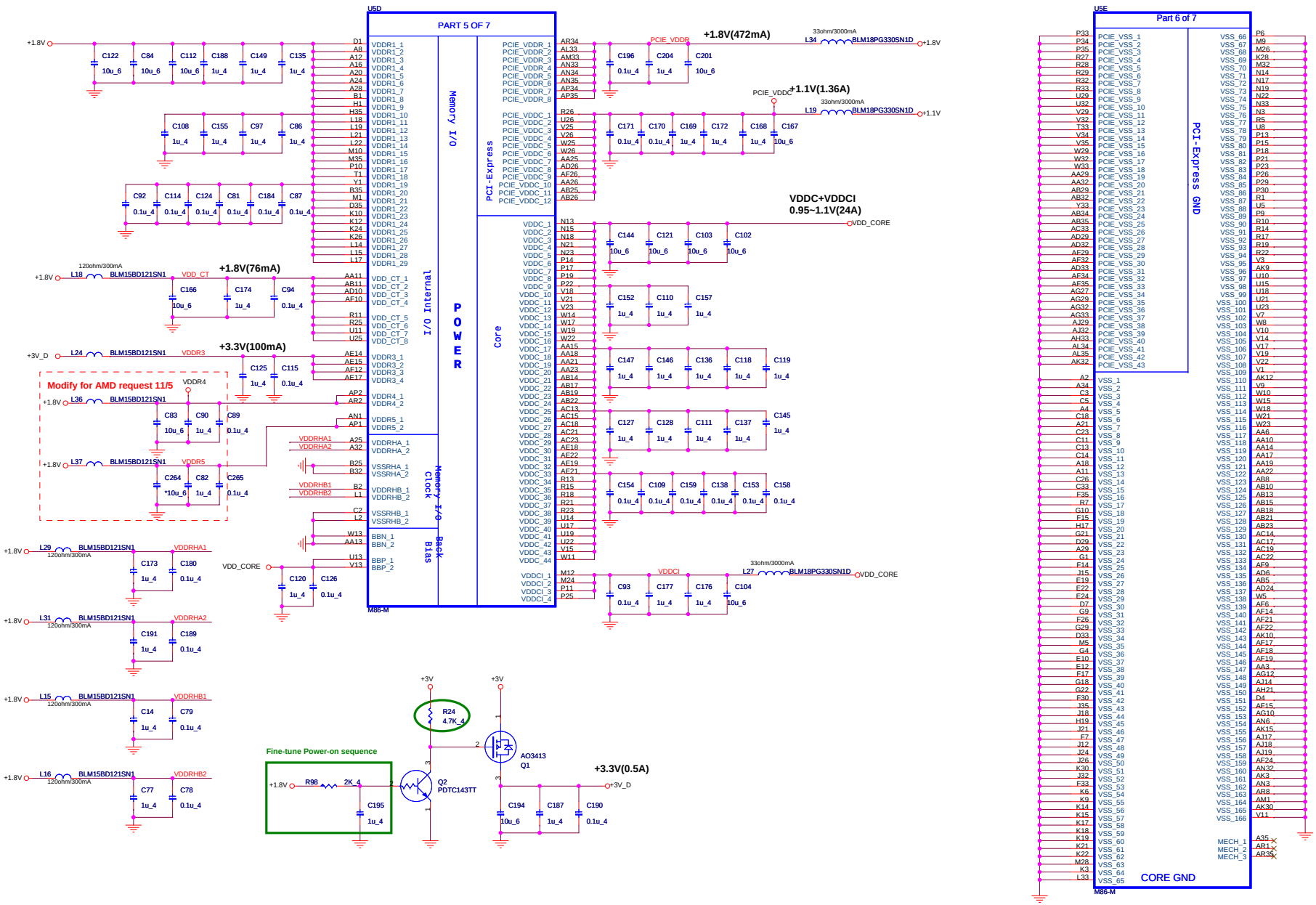
DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R
MVREF Voltage	0.9V	1.28V

0.5*VDDQ 0.713*VDDQ

PROJECT :BD3
Quanta Computer Inc.

Size	Document Number	Rev
	GFX(MEM I/F 2/2)	1A

Date: Thursday, November 08, 2007 Sheet 6 of 13

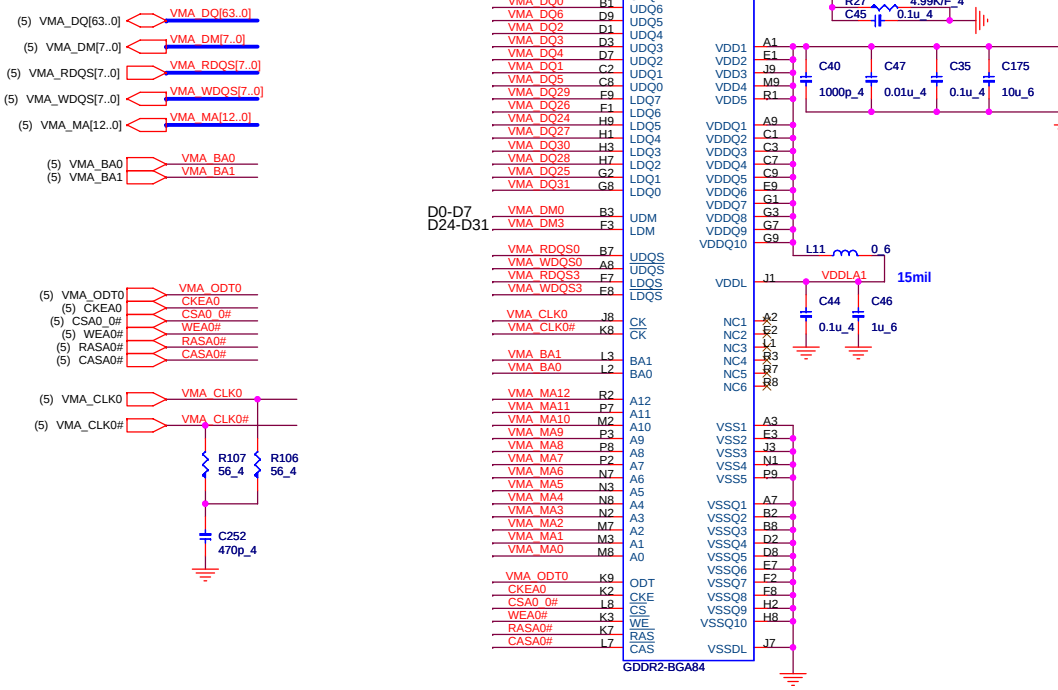


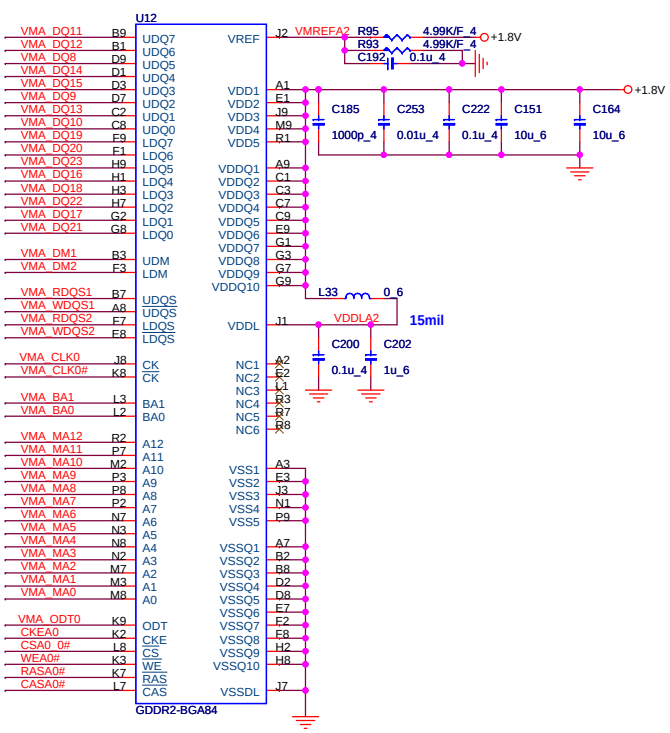
PROJECT :BD3
Quanta Computer Inc.

Size	Document Number	Rev
	GFX(GPIO, STRAP)	1A

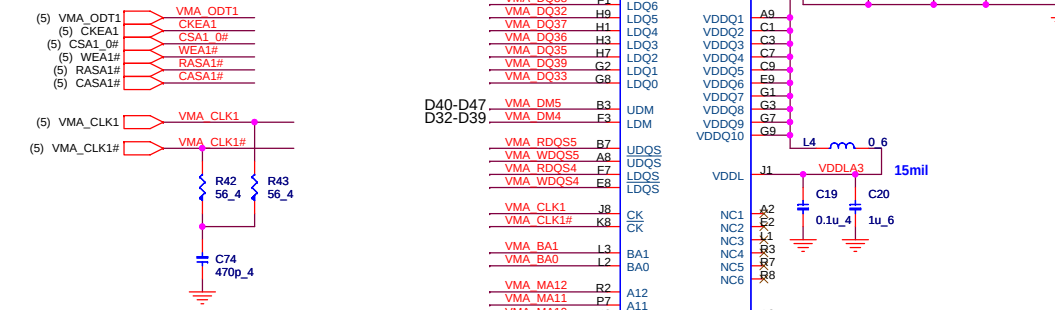
Date: Thursday, November 15, 2007 Sheet 7 of 13

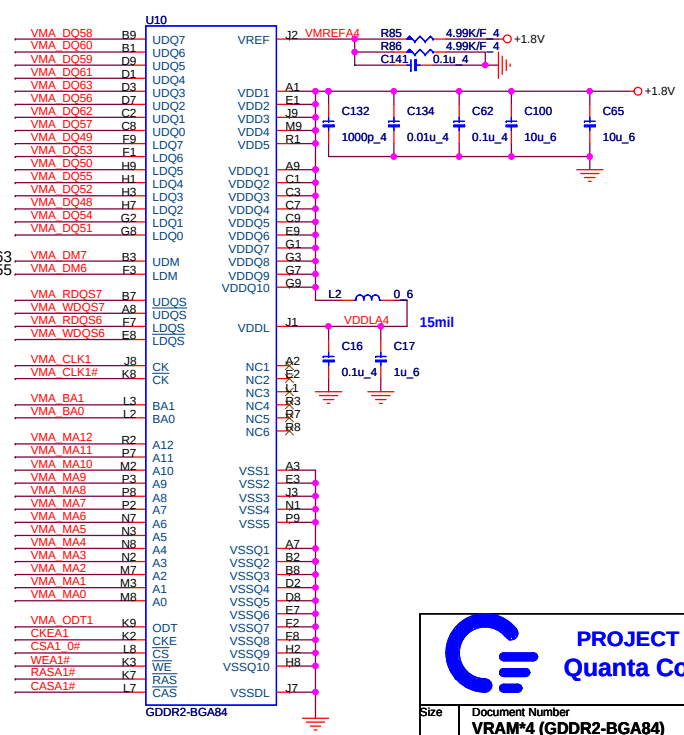
Channel A-1





Channel A-1

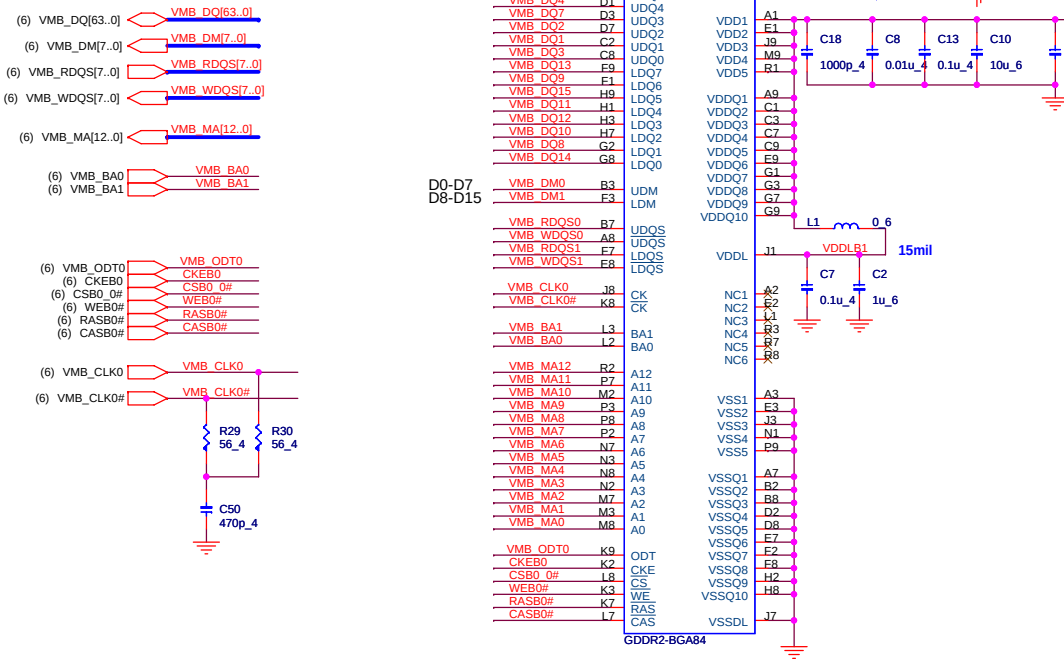




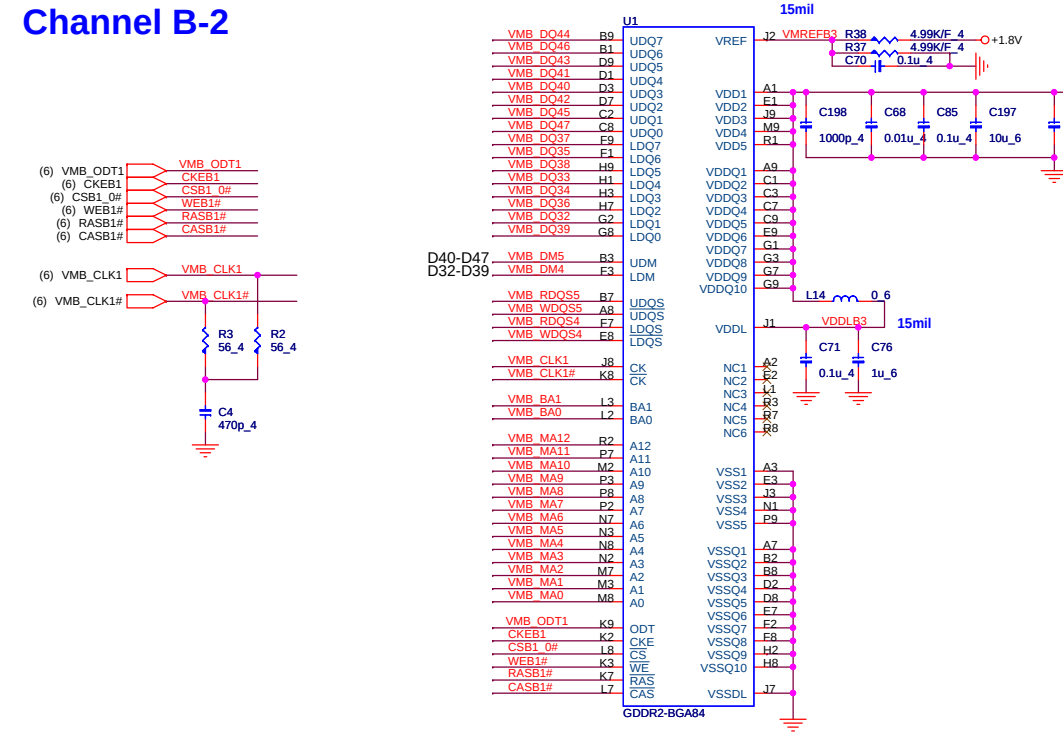
PROJECT :BD3
Quanta Computer Inc.

Size	Document Number	Rev
	VRAM*4 (GDDR2-BGA84)	1A
Date: Thursday, November 08, 2007	Sheet 8 of 13	

Channel B-1



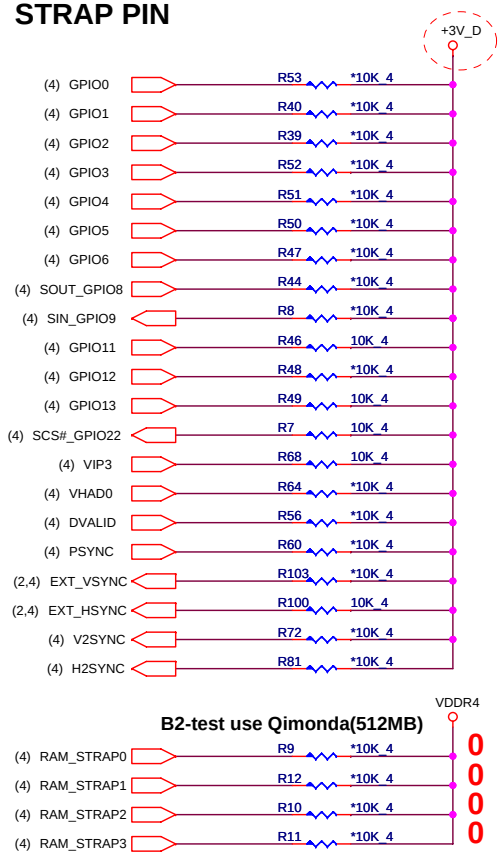
Channel B-2



PROJECT :BD3
Quanta Computer Inc.

Size	Document Number	Rev
	VRAM2*4 (GDDR2-BGA84)	1A
Date: Thursday, November 08, 2007	Sheet 9 of 13	

STRAP PIN



B2-test use Qimonda(512MB)

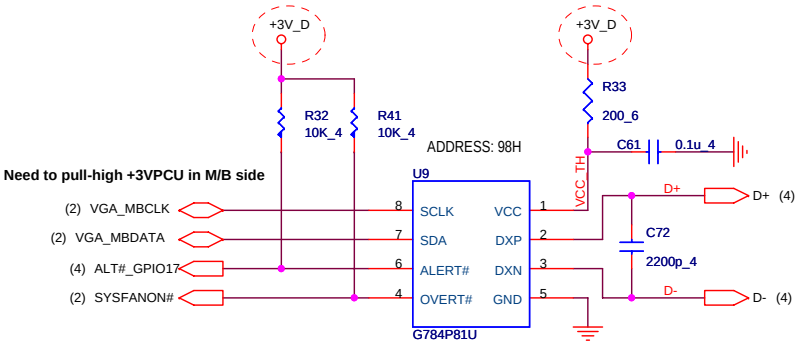
CONFIGURATION STRAPS

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE RSVD = ATI RESERVED (DO NOT INSTALL) M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO (M7x/M8x-M)	NA	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO (M82-S)	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX XX	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	O	O
BIF_VGA DIS	PSYNC	VGA ENABLED	0	O
BIF_HDMI_EN	HSYNC	HDMI ENABLE (SEE NOTE 2)	X	X
DEBUG_I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X

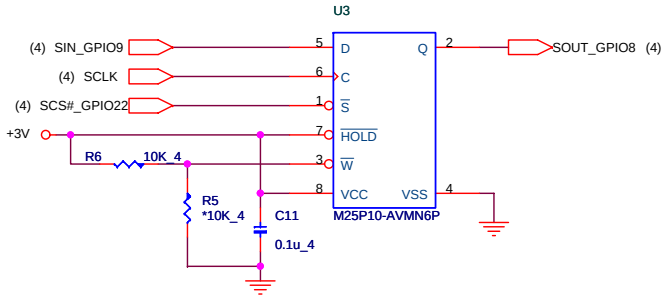
M86-DDR2 Memory Aperture size

Vendor	Size	RAM_STRAP3 DVPDATA_23	RAM_STRAP2 DVPDATA_22	RAM_STRAP1 DVPDATA_21	RAM_STRAP0 DVPDATA_20
Samsung	128M				
	256M				
	512M				
Hynix	128M	0	1	1	0
	256M	0	1	0	1
	512M	0	1	0	0
Qimonda (500MHz)	128M	0	0	1	0
	256M	0	0	0	1
	512M	0	0	0	0

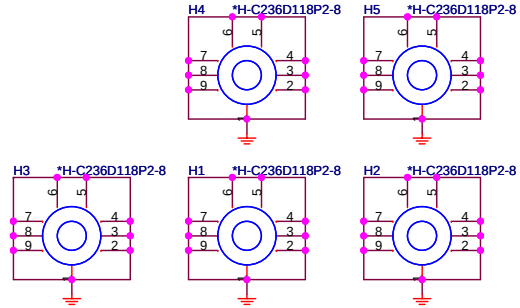
Thermal Sensor



Flash ROM



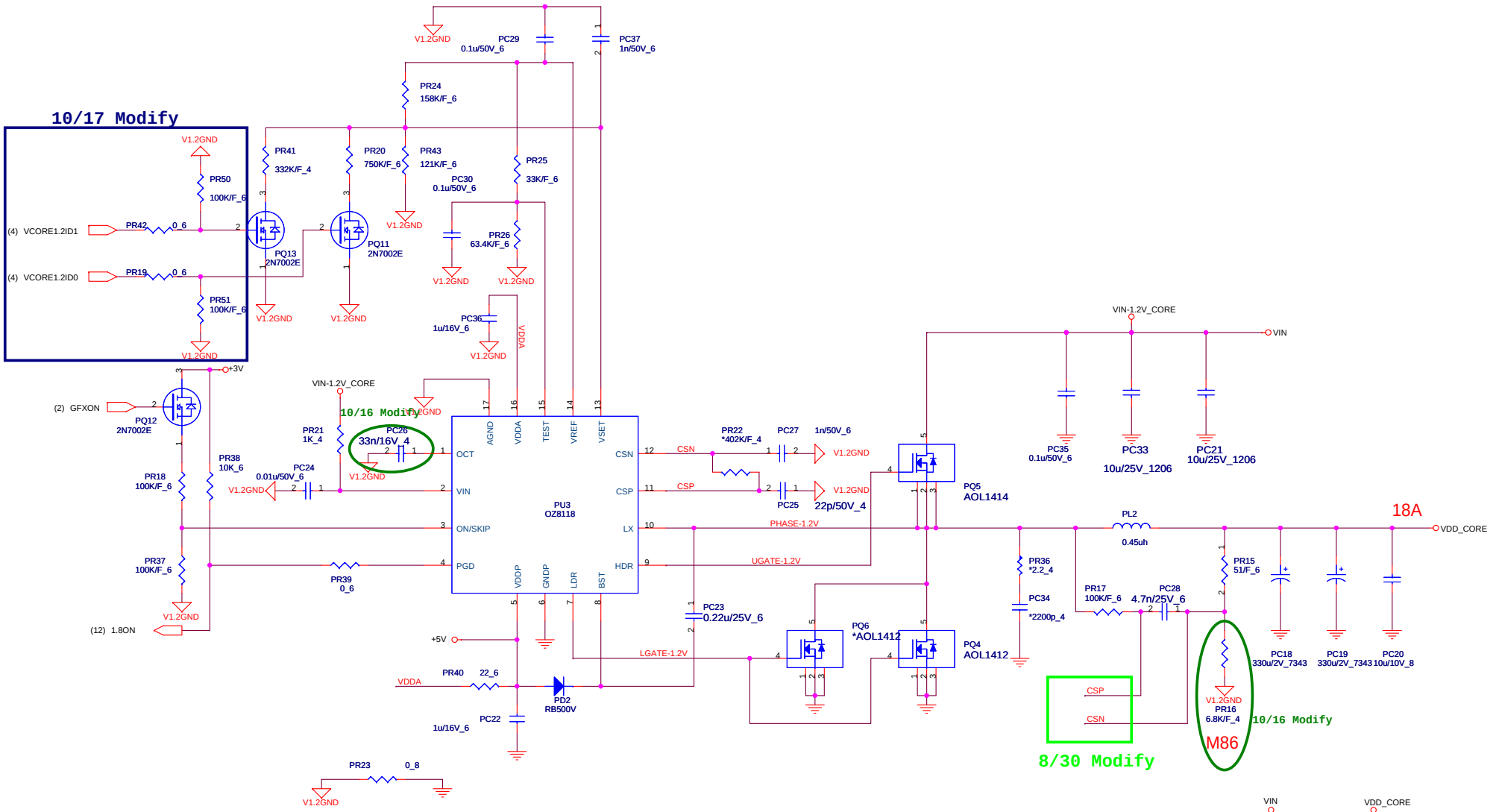
Hole



PROJECT :BD3

Quanta Computer Inc.

Title		
Size B	Document Number STRAP & EEPROM	Rev A
Date: Thursday, November 15, 2007	Sheet 10 of 13	



VID[1:0]		
VID1	VID0	
0	0	1.2V
0	1	1.1V
1	0	1.0V
1	1	0.9V

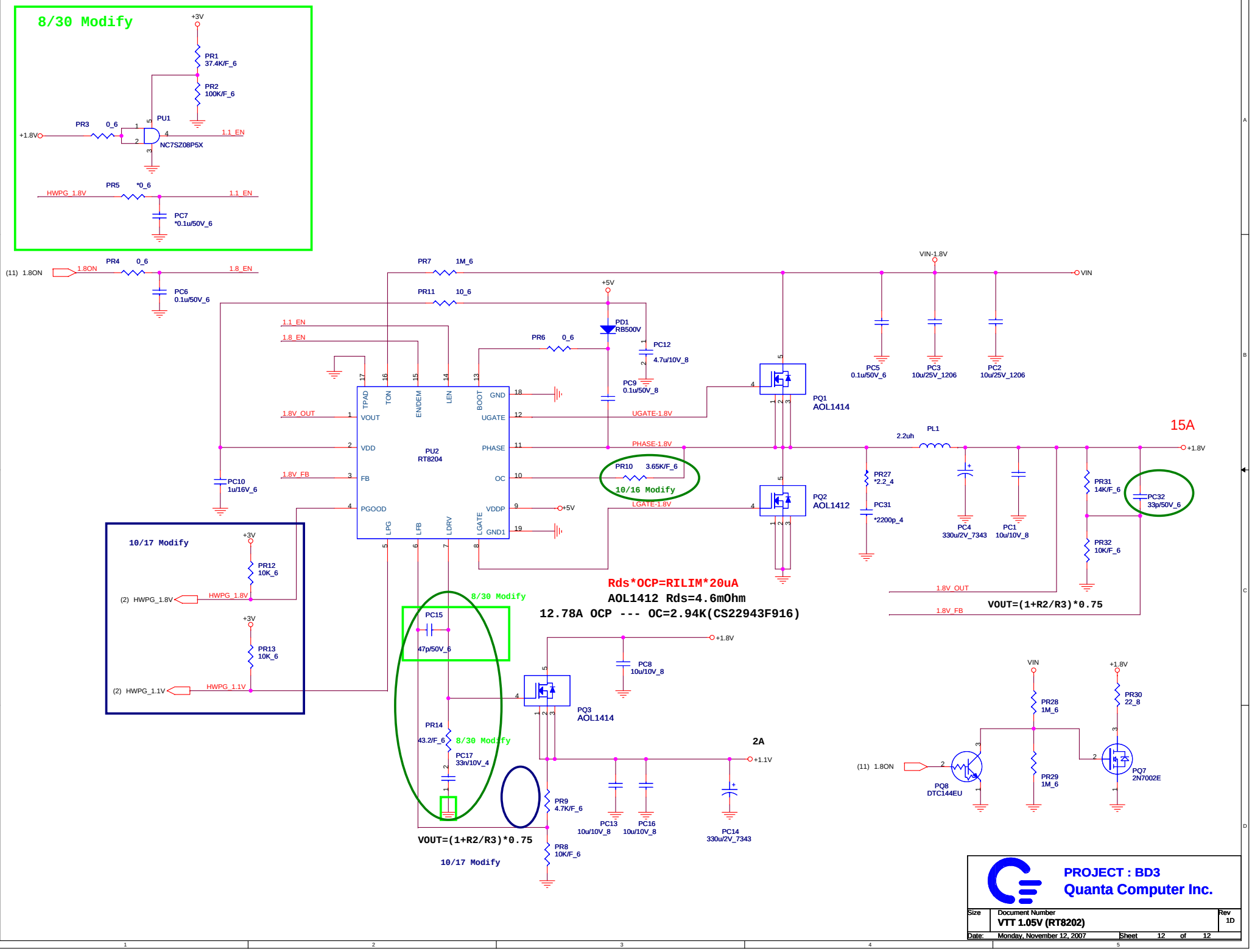
MCP67 TABLE

INPUTS		OUTPUTS			VOUT1
G1	G0	OD1	OD2	OD3	
0	0	0.75x(1+R1/R2+R1/R3+R1/R4)			1.2V
1	0	0.75x(1+R1/R2+R1/R3)			1.1V
0	1	0.75x(1+R1/R2+R1/R4)			1.0V
1	1	0.75x(1+R1/R2)			0.9V

Set

PROJECT : BD3
Quanta Computer Inc.

Size	Document Number	Rev
	1.2V_CORE (OZ8118)	1D
Date: Monday, November 12, 2007	Sheet 11 of 12	


8/30 Modify
+3V
PR1
37.4K/F_6
PR2
100K/F_6
PR3 0_6
PU1
+1.8V
1.1_EN
NC7SZ08P5X
PR5 *0_6
HWPG_1.8V
1.1_EN
PC7
*0.1u/50V_6
(11) 1.8ON
1.8ON
PR4 0_6
1.8_EN
PC6
0.1u/50V_6
PR7 1M_6
PR11 10_6
+5V
PD1
RB500V
PC12
4.7u/10V_8
PC9
0.1u/50V_8
PR6 0_6
1.1_EN
1.8_EN
VIN-1.8V
VIN
PC5
0.1u/50V_6
PC3
10u/25V_1206
PC2
10u/25V_1206
PQ1
AOL1414
15A
PL1
2.2uh
+1.8V
PR27
*2.2_4
PC31
*2200p_4
PC4
330u/2V_7343
PC1
10u/10V_8
PR31
14K/F_6
PC32
33p/50V_6
PR32
10K/F_6
PQ2
AOL1412
1.8V_OUT
1.8V_FB
VOUT=(1+R2/R3)*0.75
PU2
RT8204
TPAD
TON
EN/DEM
LEN
BOOT
GND
VOUT
UGATE
VDD
PHASE
FB
OC
PGOOD
VDDP
LPG
LFB
LDRV
LGATE
GND1
1.8V_OUT
1.8V_FB
UGATE-1.8V
PHASE-1.8V
LGATE-1.8V
+5V
PR10 3.65K/F_6
10/16 Modify
PC10
1u/16V_6
10/17 Modify
+3V
PR12
10K_6
(2) HWPG_1.8V
HWPG_1.8V
+3V
PR13
10K_6
(2) HWPG_1.1V
HWPG_1.1V
Rds*OCP=RILIM*20uA
AOL1412 Rds=4.6mOhm
12.78A OCP --- OC=2.94K(CS22943F916)
8/30 Modify
PC15
47p/50V_6
PR14
43.2/F_6
8/30 Modify
PC17
33n/10V_4
PQ3
AOL1414
+1.8V
PC8
10u/10V_8
2A
+1.1V
PR9
4.7K/F_6
PC13
10u/10V_8
PC16
10u/10V_8
PC14
330u/2V_7343
PR8
10K/F_6
VOUT=(1+R2/R3)*0.75
10/17 Modify
VIN
+1.8V
PR28
1M_6
PR30
22_8
(11) 1.8ON
PR29
1M_6
PQ8
DTC144EU
PQ7
2N7002E
PROJECT : BD3
Quanta Computer Inc.
Size
Document Number
VTT 1.05V (RT8202)
Rev
1D
Date: Monday, November 12, 2007
Sheet 12 of 12

Model	REV	CHANGE LIST
BD3 VGA/B	1A	FIRST RELEASED: E200710-1822 (PCB: DABD3UB18A0)
	2A	2ND RELEASED: E200710-3032 (PCB: DABD3UB18B0) Page02 : Add AND gate circuit (U13/R136/R137/R138/C263) to fine-tune power-good signal Page04 : Because GPIO_19 (temp_fail) output high level, change pull-up to pull-down (reserve) ==>Don't highlight to customer Change C39/C43 from 15pf to 6.8pf (CH-686T0B07) for 27Mhz frequency correction Page07 : Change R98 (2Kohm)/C195(1uf) to fine-tune power-on sequence for +3V_D Power circuit (Page11~12) 1. Change PC26 from original P/N: CH02206JB08 Value: 22p/25V_4 to final P/N: CH33303ZB30 Value: 33n/16V_4. 2. Change PC15 from original P/N: CH5103K9901 Value: 1u/16V_6 to final P/N: CH04706K909 Value: 47p/50V_6. 3. Change PR14 from original P/N: CS11003F953 Value: 100/F_6_4 to final P/N: CS04323F909 Value: 43.2/F_6. 4. Change PC17 from original P/N: CH23306JB16 Value: 3.3n/50V_4 to final P/N: CH33302KB12 Value: 33n/10V_4. 5. Remove PC11 original P/N: CH41006K911 Value: 0.1u/50V_6 6. Add PC14 original P/N: CH733RM8858 Value: 330u/2V_7343 7. Change PR16 from original P/N: CS21912FB13 Value: 1.91K/F_4 to final P/N: CS26802FB19 Value: 6.8K/F_4. 8. Change PR10 from original P/N: CS22943F916 Value: 2.94K/F_6 to final P/N: CS23653F912 Value: 3.65K/F_6. 9. Change PC26 from original P/N: CH3334K1B00 Value: 33n/25V_4 to final P/N: CH33303ZB30 Value: 33n/16V_4. 10.Add PC32 to final P/N: CH03306J905 Value: 33p/50V_6
	2B	3RD RELEASED: E2007??-???? (PCB: DABD3UB18C0) Page02/04/10 : Change +3V to +3V_D (delayed 3.3V) power rail to avoid leakage during power-up for DDC/GPIO Page04 : Add test point (T22/T23) at SDA/SCL for I2C Debug access Add test point (T24/25/26/27/28) for GPU boundary scan test Page07 : Add bead(L36/L37) to separate VDDR4 and VDDR5 power for AMD request Page10 : Change DVPDATA[20..23] pull-up to VDDR4(+1.8V)
	3A	

MODEL	BD3 VGA/B FROM	BD3 VGA/B To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B

PROJECT : BD3
Quanta Computer Inc.

Size	Document Number	Rev
	Change list	2B

Date: Thursday, November 15, 2007 Sheet 13 of 13

DOC NO.	PROJECT MODEL :	BD3 VGA/B	APPROVED BY:		DATE:	2007/11/05
	PART NUMBER:		DRAWING BY:		REVISON:	2B