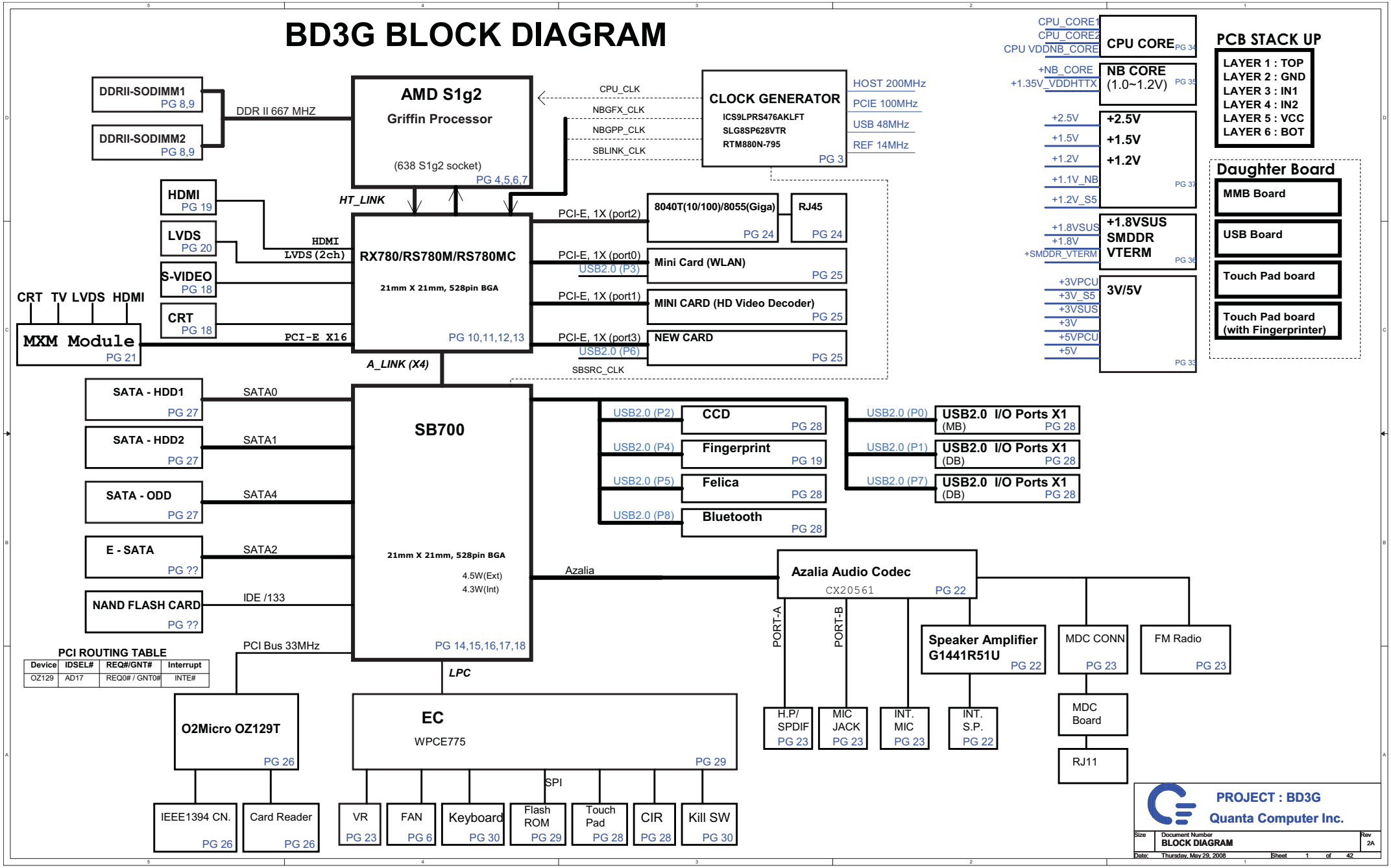
BD3G BLOCK DIAGRAM



PCI ROUTING TABLE

Device	IDSEL#	REQ#/GNT#	Interrupt
OZ129	AD17	REQ0# / GNT0#	INTE#

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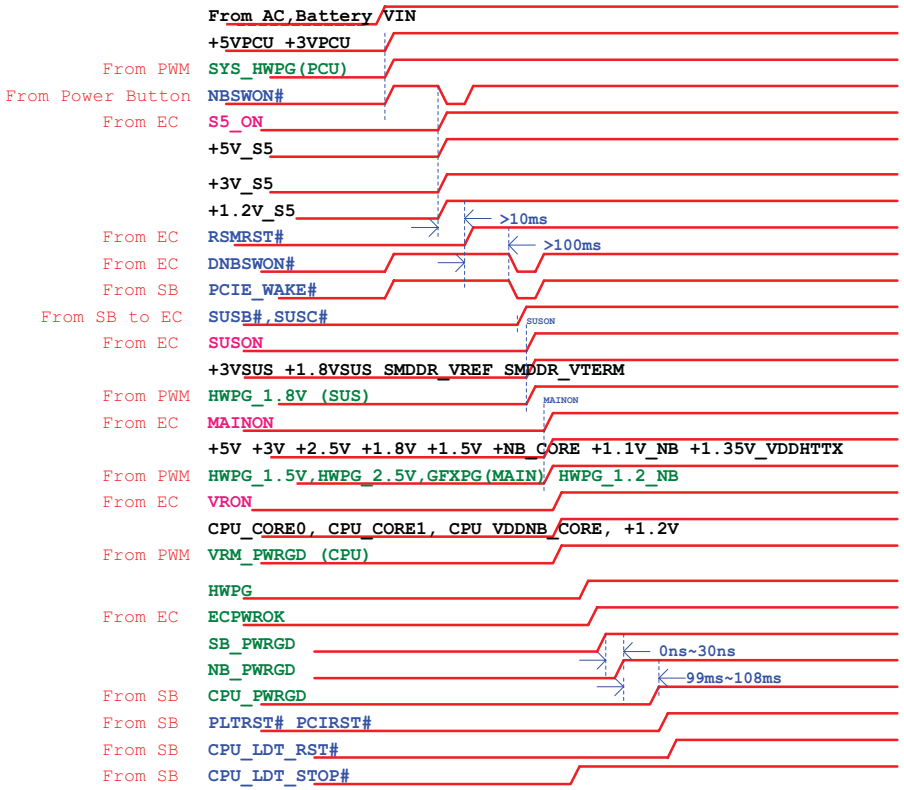
BD3G Power On Sequence



BOM naming rule

Items	Function	BTO	Name	Description
1	CIR	v	CIR@	
2	HDMI port	v	HDM@	
3	HDMI transmitter	v	SI@	Silicon image SiI 1392/1932
4	HDMI-CEC	v	CEC@	Renesas R8C/1B
5	Discrete VGA		EV@	External VGA stuff
6	UMA		IV@	Internal VGA stuff
7	New Card		NEW@	
8	RJ11	v	MD@	Modem
9	RJ45-10/100		40@	Marvell 8040T(10/100)
10	RJ45-1000		55@	Marvell 8055(Giga)
11	Option for RJ45-10/100 and RJ45-1000		40@55@	Option for 8040/8055
12	TV	v	TV@	
13	Cardbus		CB@	
14	FM transmitter	v	FM@	
15	Mainstream ID LED		MID@	
16	Low cost ID LED		LID@	
17	CCD	v	CCD@	
18	INT MIC	v	I_MIC@	
19	AMD Hyper Flash		HF@	Only for AMD platform
20	North bridge(690MC/RS780MC)		MC@	Only for AMD platform
21	North bridge(RX780)		RX@	Only for AMD platform
22	PowerXpress		PX@	Only for AMD platform
23	PowerXpress with UMA SKU		PX@IV@	Only for AMD platform
24	PowerXpress with Discrete VGA SKU		PX@EV@	Only for AMD platform
25	Power player/Power Shift		PP@	Only for AMD platform

*Note: EC will sampling SUSB# &
SUSC# every 5ms.

AMD SB700 SMBUS Table

	CLK GEN	RAM	Mini Card (HD-Decoder)	Mini-card(WL)	New Card	HDMI
SB700 SDATA0/SCLK0(+3V)	V	V	V	V	V	
SB700 SDATA1/SCLK1(+3V_S5)						V
SB700 SDATA2/SCLK2(+3V_S5)						
Power	+3V	+3V	+3V	+3V (Atheros)	+3V	+3V_S5
Reserve MOS ckt	V	V	V	V	V	V

EC SMBUS Table

	Battery	CPU thermal Sensor	EC EEPROM	VGA thermal Sensor	Touch Sensor	HDMI CEC
EC775 SDATA1/SCLK1(+3VPCU)	V					
EC775 SDATA2/SCLK2(+3VPCU)		V	V			
EC775 SDATA3/SCLK3(+3VPCU)				V	V	V
EC775 SDATA4/SCLK4(+3VPCU)						
Power	+3VPCU	+3V	+3VPCU	+3V	+3VPCU	+5VPCU
Reserve MOS ckt	X	V	X	V	X	V

CLK_GEN_SLG8SP628

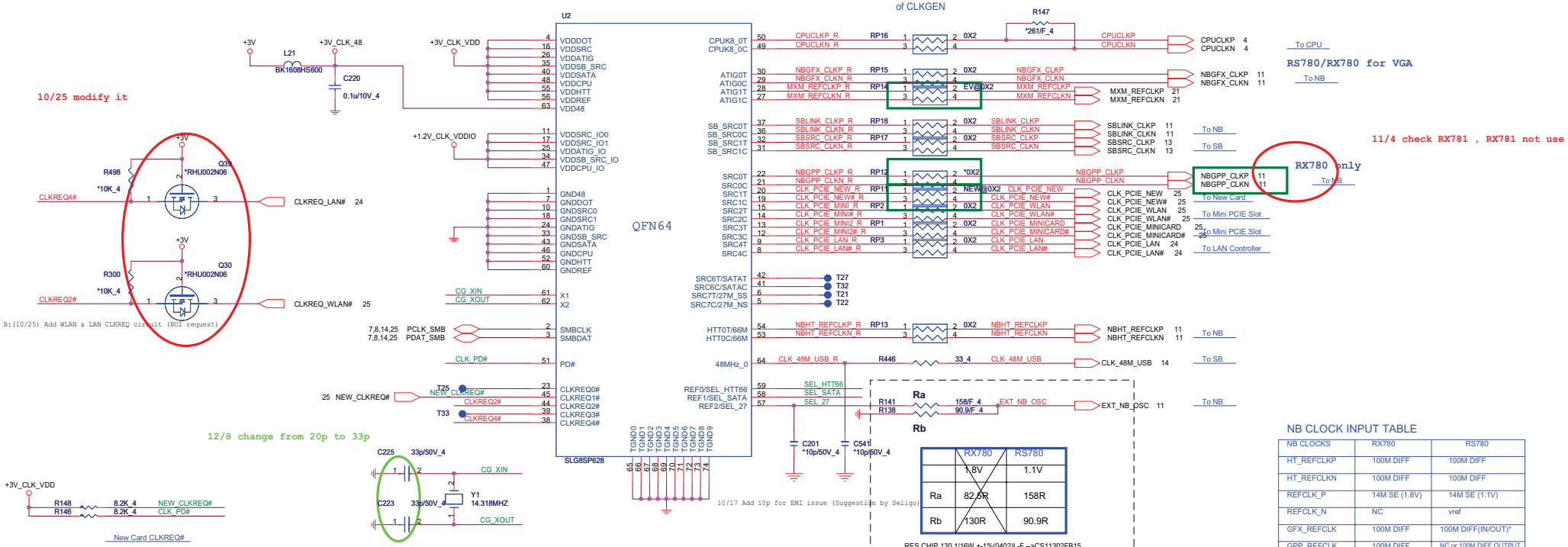
ICS9LPRS480 P/N : ALPRS480000

SLG8SP628 P/N : AL8SP628000

RTM880N-796 P/N : AL000880000

Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

Place within 0.5" of CLKGEN



	RX780	RS780
	1.8V	1.1V
Ra	82.5R	158R
Rb	130R	90.9R

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

CLOCKS name	RX780	RS780	Clock pin function
NBGFX_CLKP NBGFX_CLKN	RP1001 STUFF	RP1001 STUFF	to NB for VGA reference clock
MXM_REFCLKP MXM_REFCLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBGPP_CLKP NBGPP_CLKN	RP1005 STUFF	RP1005 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP1003 STUFF	RP1003 STUFF	to NB for AC-LINK reference clock

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

PROJECT : BD3G

Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR_SLG8SP628	1A

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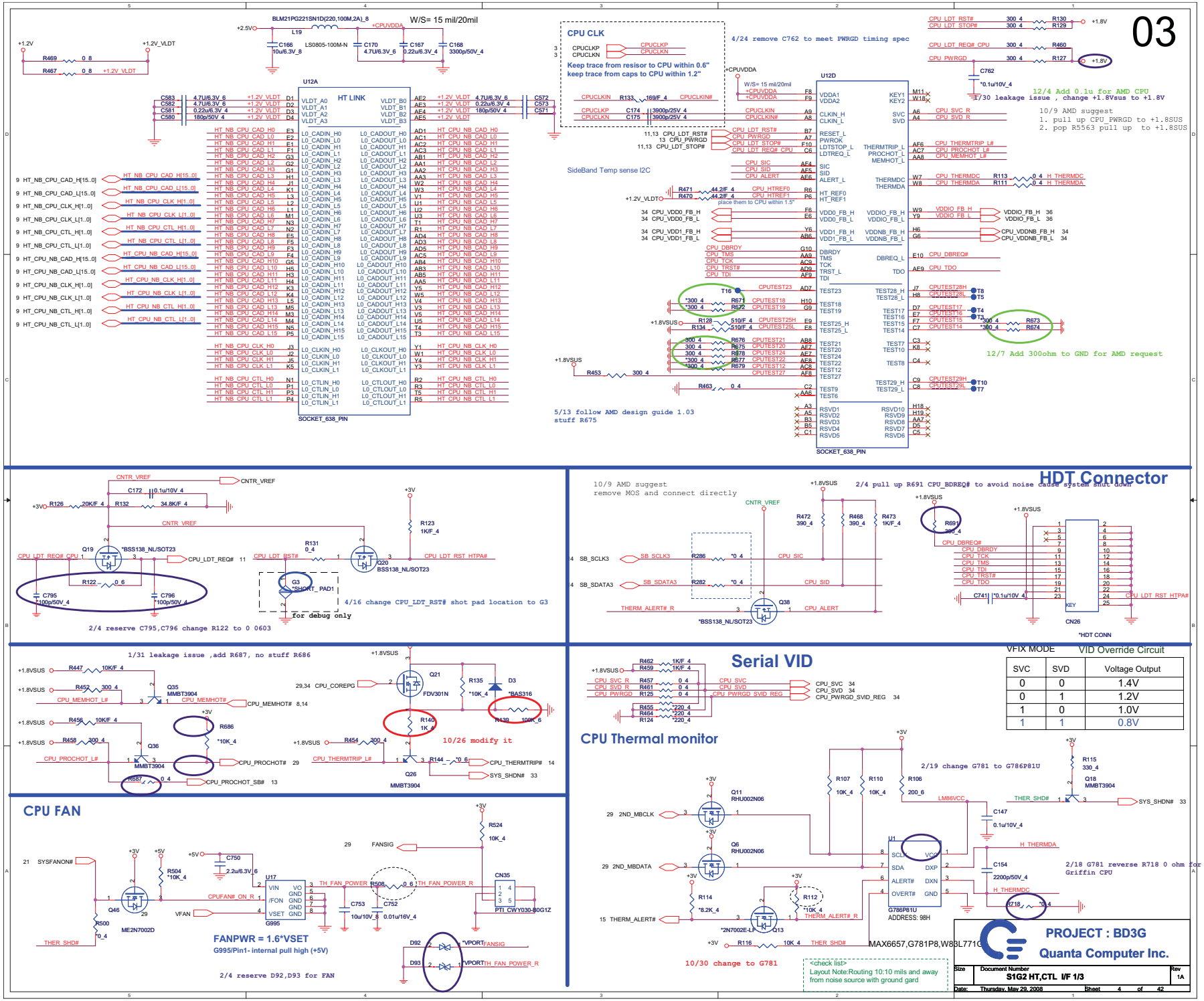
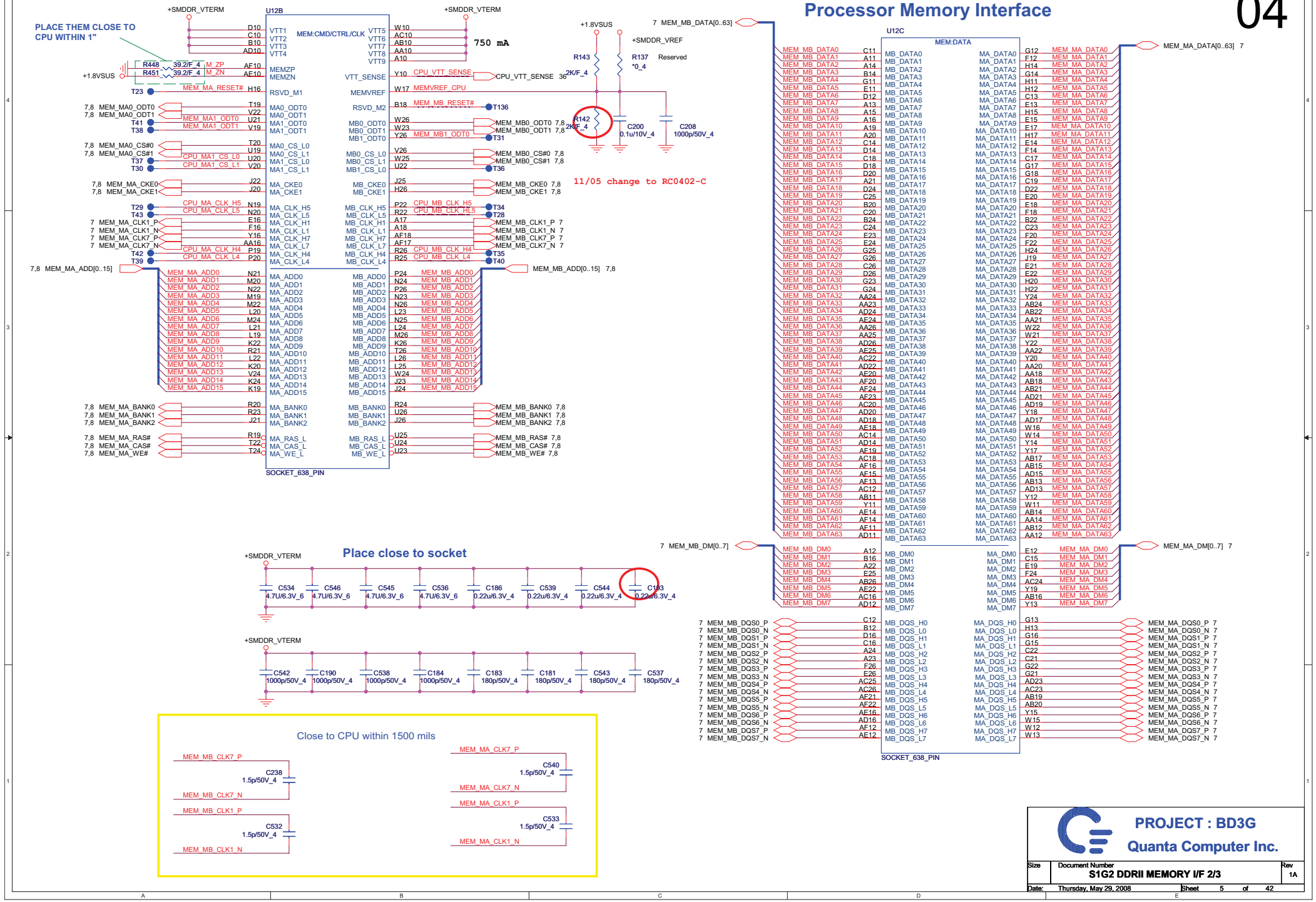

03
U12A
HT LINK
SOCKET_638_PIN
U12D
SOCKET_638_PIN
CPU CLK
Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"
4/24 remove C762 to meet PWRGD timing spec
12/4 Add 0.1u for AMD CPU
1/30 leakage issue , change +1.8Vsus to +1.8V
10/9 AMD suggest
1. pull up CPU_PWRGD to +1.8SUS
2. pop R5563 pull up to +1.8SUS
SideBand Temp sense I2C
place them to CPU within 1.5"
12/7 Add 300ohm to GND for AMD request
5/13 follow AMD design guide 1.03
stuff R675
HDT Connector
10/9 AMD suggest
remove MOS and connect directly
2/4 pull up R691 CPU_BDREQ# to avoid noise cause system shut down
CN26
*HDT CONN
CNTR_VREF
2/4 reserve C795,C796 change R122 to 0 0603
4/16 change CPU_LDT_RST# shot pad location to G3
for debug only
1/31 leakage issue ,add R687, no stuff R686
10/26 modify it
Serial VID
VFIX MODE
VID Override Circuit
SVC SVD Voltage Output
0 0 1.4V
0 1 1.2V
1 0 1.0V
1 1 0.8V
CPU Thermal monitor
2/19 change G781 to G786P81U
2/18 G781 reverse R718 0 ohm for Griffin CPU
10/30 change to G781
MAX6657,G781P8,W83L771G
CPU FAN
FANPWR = 1.6*VSET
G995/Pin1- internal pull high (+5V)
2/4 reserve D92,D93 for FAN
PROJECT : BD3G
Quanta Computer Inc.
S1G2 HT,CTL I/F 1/3
Thursday, May 29, 2008
Sheet 4 of 42

Processor Memory Interface

04



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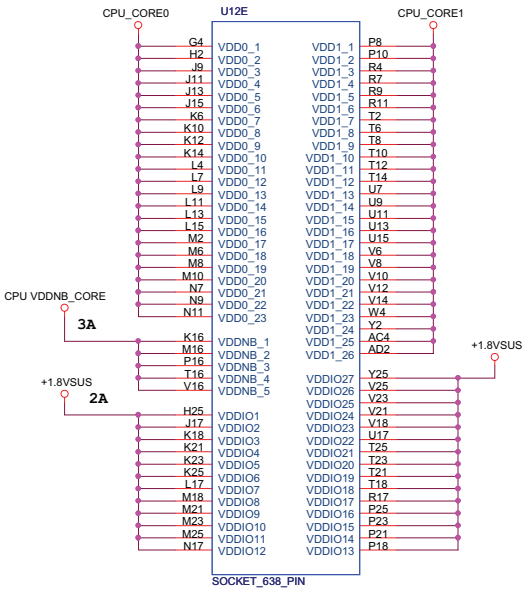
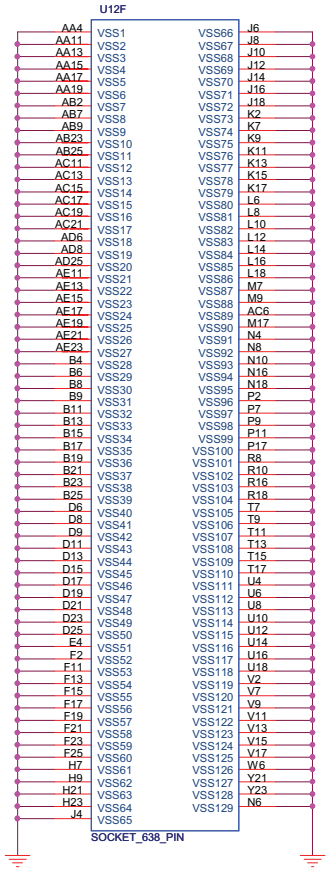
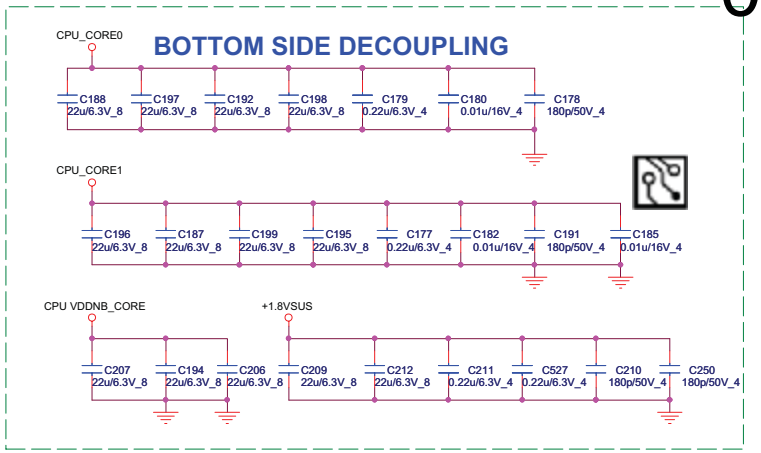
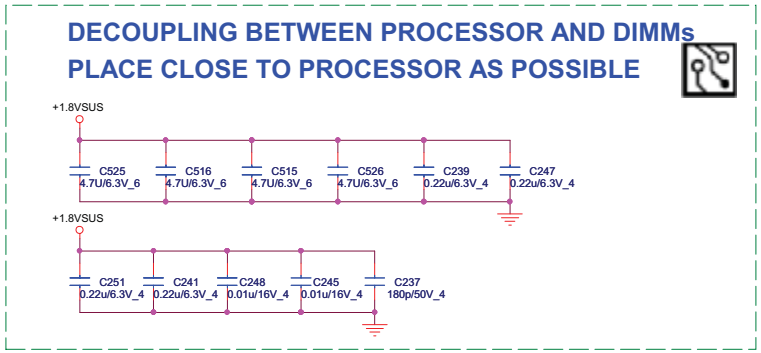


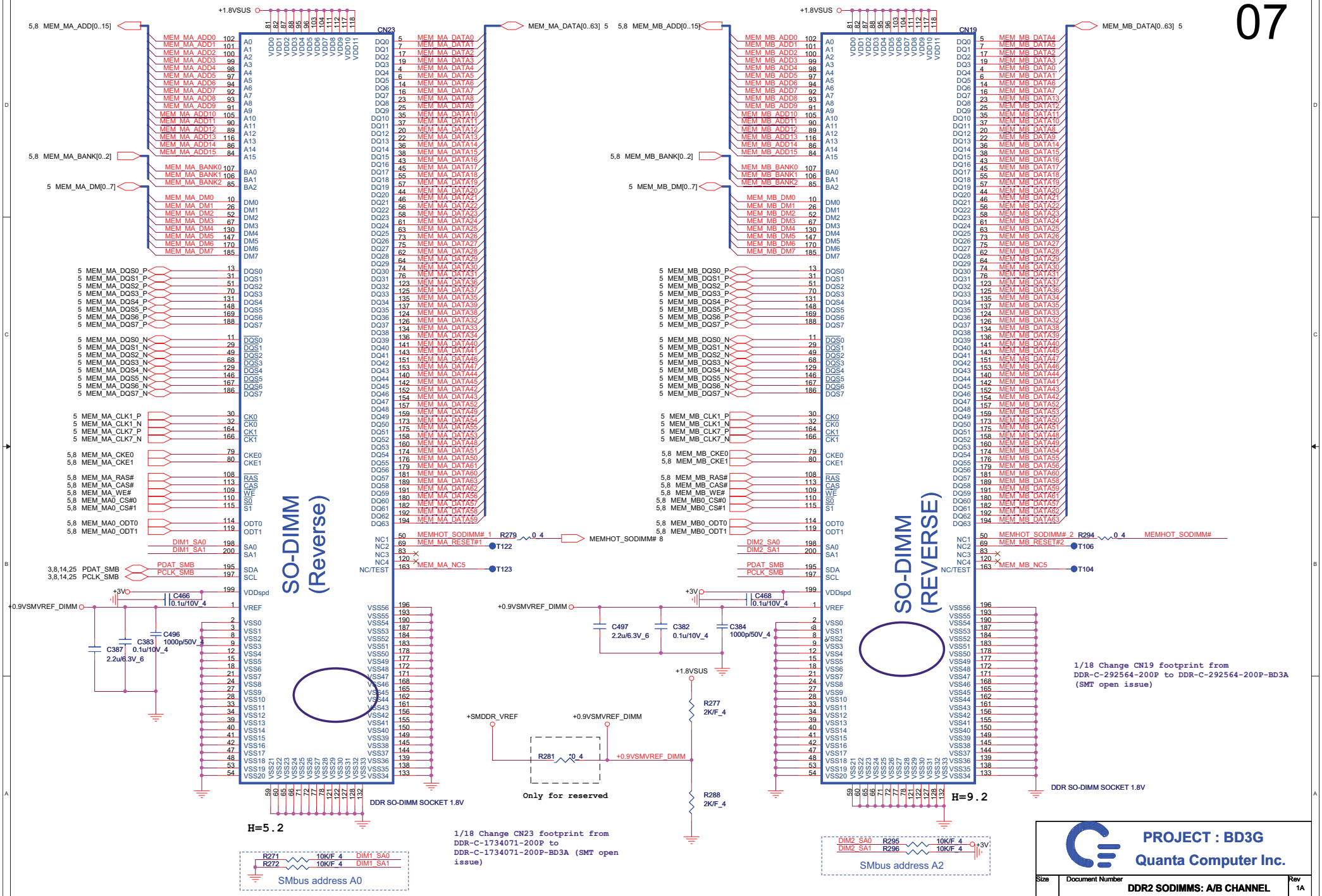






PROCESSOR POWER AND GROUND

PROJECT : BD3G Quanta Computer Inc.		
Size	Document Number S1G2 PWR & GND 3/3	Rev 1A
Date: Thursday, May 29, 2008	Sheet 6 of 42	



PROJECT : BD3G

Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 SODIMMS: A/B CHANNEL	1A

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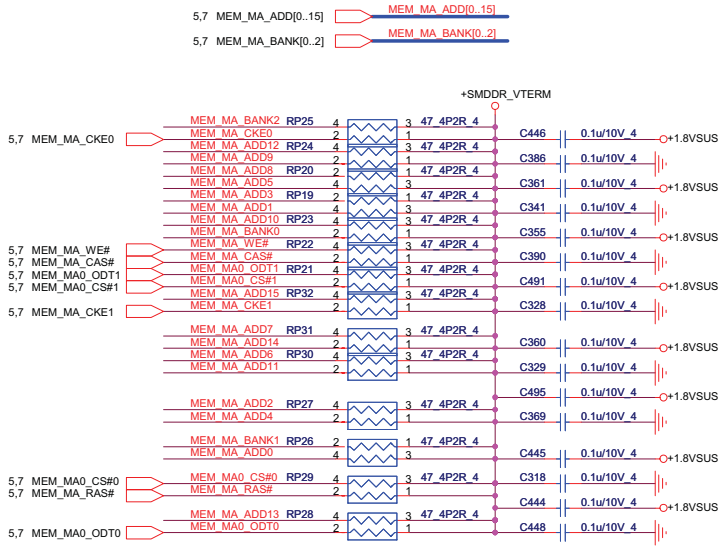
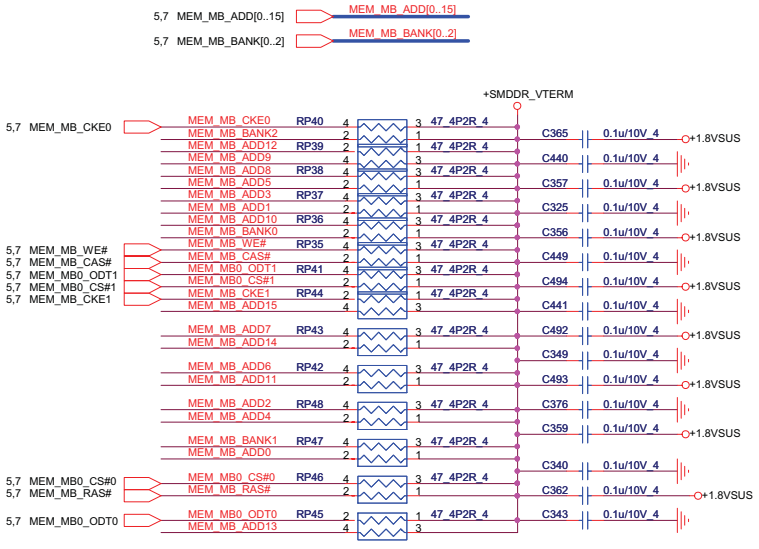
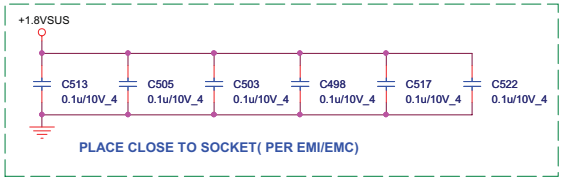
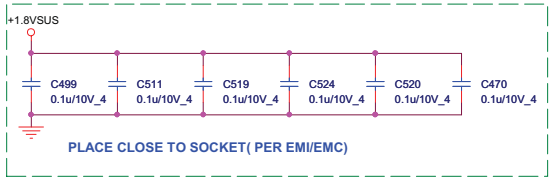


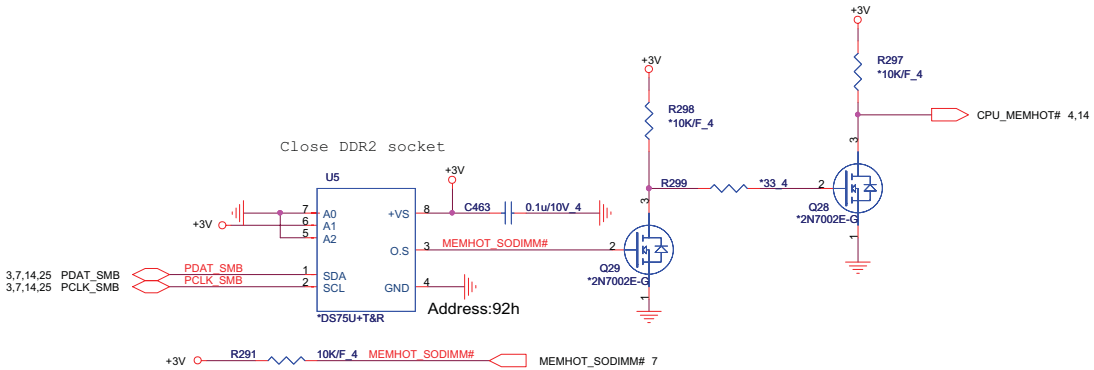


PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH





PROJECT : BD3G

Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 SODIMMS TERMINATIONS	1A

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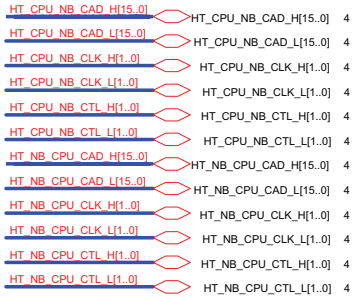


11/4 modify

signals	RS780	RX780
HT_TXCALP	R641 300 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 300 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

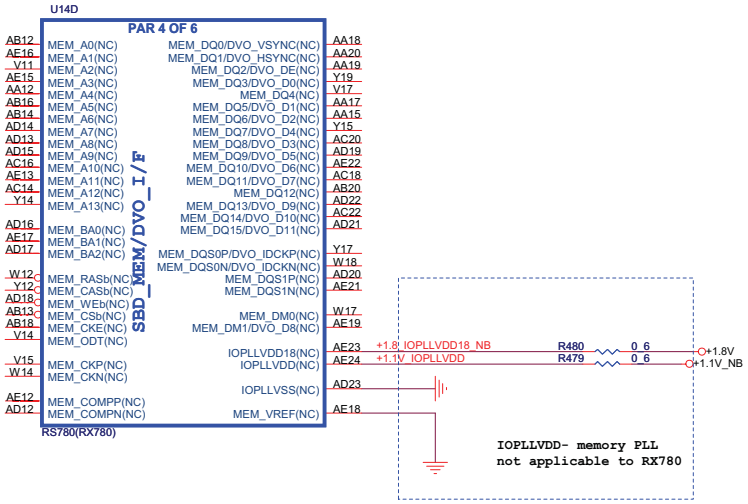
RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 300 1/16W +-1%(0402)
P/N : CS13002FB00

A12 version
RS780M AJ067400T05 100-CK2612(216-0674008-00)
RS780MC AJ067400T06 100-CK2613(216-0674010-00)
RX781 AJ067400T10 100-CK2642(215-0674024)
SB700 AJA12FG0T18 100-CK2614(218S7EALA12FG)

A13 version
RS780M AJ067400T18 100-CK2699(216-0674022)
RS780MC AJ067400T20 100-CK2704(216-0674024)
RX781 AJ067400T21 100-CK2706(215-0674034)
A12 version
SB700 AJA12FG0T18

This block is for UMA RS780 only , RX780 can remove all component



2/1 R480,R479 no stuff when RS780M without side port / RX781

4/24 stuff R480,R479

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	RS740/RS780-HT LINK I/F 1/5	1A

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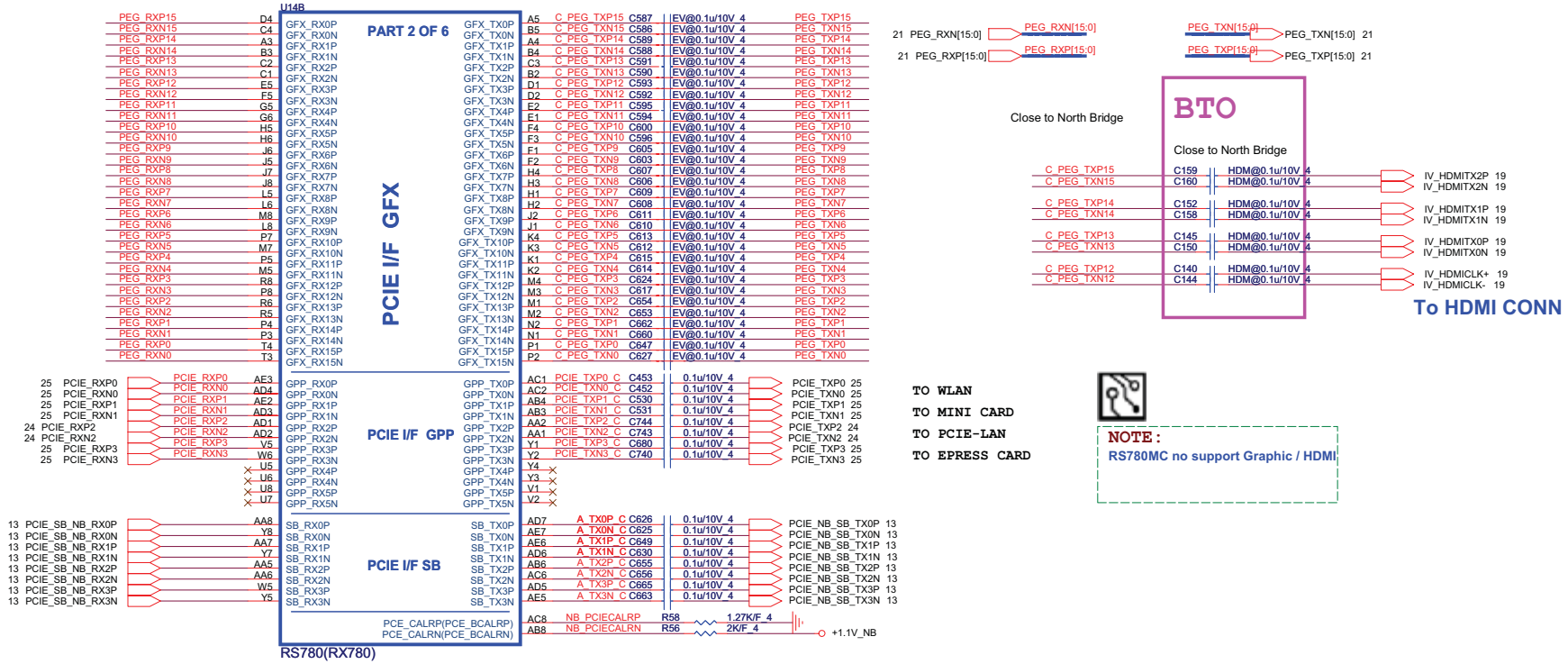

NOTE :
RS780MC no support Graphic / HDMI

11/4 modify

RX780/RS740/RS780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	RS740/RS780-PCIE I/F 2/5	1A

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RX780: Powered from the 1.8-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.
RS780: Powered from the 3.3-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.

10/26 change to 4 pin S-video conn , no need TV_comp

2/1 follow A13 request change
R103 from 150 to 140 CS11402FB19

RX780
4,13 CPU_LDT_RST# — R30 *0_4 — NB_RST# IN
RS780
13 NB_PLTRST# — R31 0_4
North Bridge RESET

11/4 stuff R5160 for RS780M/MC/RX781

RX780
+1.1V_NB — R47 *2K/F_4 — INT_CRT_DDCDAT
R46 *2K/F_4 — INT_CRT_DDCCLK
10/9 add 2K pull up to DDCDAT /DDCCLK for RX780

11/4 no stuff for RS780M/MC/RX781

12/22 stuff R48 2.2K for power play

+NB_CORE_ON — R44 *10K/F_4 — +3V
R48 2.2K_4

U14C — PART 3 OF 6 — RS780(RX780)

CRT/TVOUT: AVDD1(NC), AVDD2(NC), AVDDDI(NC), AVSSDI(NC), AVDDQ(NC), AVSSQ(NC), C_Pr(DFT_GPIO5), Y(DFT_GPIO2), COMP_Pb(DFT_GPIO4), RED(DFT_GPIO0), REDb(NC), GREEN(DFT_GPIO1), GREENb(NC), BLUE(DFT_GPIO3), BLUEb(NC), DAC_HSYNC(PWM_GPIO4), DAC_VSYNC(PWM_GPIO6), DAC_SDA(PCE_TCALRN), DAC_SCL(PCE_RCALRN), DAC_RSET(PWM_GPIO1)

LVTM: TXOUT_L0P(NC), TXOUT_L0N(NC), TXOUT_L1P(NC), TXOUT_L1N(NC), TXOUT_L2P(NC), TXOUT_L2N(DBG_GPIO0), TXOUT_L3P(NC), TXOUT_L3N(DBG_GPIO2), TXOUT_U0P(NC), TXOUT_U0N(NC), TXOUT_U1P(PCIE_RESET_GPIO3), TXOUT_U1N(PCIE_RESET_GPIO2), TXOUT_U2P(NC), TXOUT_U2N(NC), TXOUT_U3P(PCIE_RESET_GPIO5), TXOUT_U3N(NC), TXCLK_LP(DBG_GPIO1), TXCLK_LN(DBG_GPIO3), TXCLK_UP(PCIE_RESET_GPIO4), TXCLK_UN(PCIE_RESET_GPIO1)

PLL PWR: PLLVDD(NC), PLLVDD18(NC), PLLVSS(NC), VDDA18HTPLL, VDDA18PCIEPLL1, VDDA18PCIEPLL2

PM: SYSRESETb, POWERGOOD, LDTSTOPb, ALLOW_LDTSTOP

CLOCKs: HT_REFCLKP, HT_REFCLKN, REFCLK_P/OSCIN(OSCIN), REFCLK_N(PWM_GPIO3), GFX_REFCLKP, GFX_REFCLKN, GPP_REFCLKP, GPP_REFCLKN, GPPSB_REFCLKP(SB_REFCLKP), GPPSB_REFCLKN(SB_REFCLKN)

MIS.: I2C_DATA, I2C_CLK, DDC_DATA/AUX0N(NC), DDC_CLK/AUX0P(NC), AUX1P(NC), AUX1N(NC), STRP_DATA, RSVD, AUX_CAL(NC), VDDLTP18(NC), VSSLTP18(NC), VDDLT18_1(NC), VDDLT18_2(NC), VDDLT33_1(NC), VDDLT33_2(NC), VSSLT1(VSS), VSSLT2(VSS), VSSLT3(VSS), VSSLT4(VSS), VSSLT5(VSS), VSSLT6(VSS), VSSLT7(VSS), LVDS_DIGON(PCE_TCALRP), LVDS_BLON(PCE_RCALRP), LVDS_ENA_BL(PWM_GPIO2), TMDS_HPD(NC), HPD(NC), TVCLKIN(PWM_GPIO5), THERMALDIODE_P, THERMALDIODE_N, TESTMODE

+3V AVDD_NB — F12, F12
+1.8V AVDDDI_NB — F14
+1.8V AVDDQ_NB — G15, H15, H14
18 INT_TV_C/R — INT_TV_C/R — F17
18 INT_TV_Y/G — INT_TV_Y/G — F17
INT_TV_COMP — F15
18 INT_CRT_RED — R95 IV@150/F_4, R89 IV@150/F_4, R84 *150/F_4 — INT_CRT_RED — G18
18 INT_CRT_GRN — R103 IV@140/F_4 — INT_CRT_GRN — G17, E18
18 INT_CRT_BLU — R99 IV@150/F_4 — INT_CRT_BLU — F18, E19, F19
R102 IV@150/F_4
18 INT_HSYNC — INT_HSYNC — A11
18 INT_VSYNC — INT_VSYNC — B11
18 INT_CRT_DDCDAT — INT_CRT_DDCDAT — E8
18 INT_CRT_DDCCLK — INT_CRT_DDCCLK — F8
R79 IV@715/F_6 — DAC_RSET_NB — G14
+1.1V_PLLVDD — A12
+1.8V_PLLVDD18 — D14, B12
+1.8V_VDDA18HTPLL — H17
+1.8V_VDDA18PCIEPLL — D7, E7
17 NB_PWRGD_IN — NB_RST# IN — D8
NB_PWRGD_IN — A10
NB_LDT_STOP# — C10
NB_ALLOW_LDTSTOP — C12
3 NBHT_REFCLKP — NBHT_REFCLKP — C25
3 NBHT_REFCLKN — NBHT_REFCLKN — C24
3 EXT_NB_OSC — R485 0_4 — NB_REFCLK_P — E11
R53 0_4 — NB_REFCLK_N — F11
+1.1V_NB — R50 4.7K_4 — RS780 — R51 4.7K_4
3 NBGFX_CLKP — NBGFX_CLKP — T2
3 NBGFX_CLKN — NBGFX_CLKN — T1
3 NBGPP_CLKP — NBGPP_CLKP — U1
3 NBGPP_CLKN — NBGPP_CLKN — U2
3 SBLINK_CLKP — SBLINK_CLKP — V4
3 SBLINK_CLKN — SBLINK_CLKN — V3
20 INT_LVDS_EDIDDATA — INT_LVDS_EDIDDATA — A9
20 INT_LVDS_EDIDCLK — INT_LVDS_EDIDCLK — B9
19 IV_HDMI_DDCDATA — IV_HDMI_DDCDATA — B8
19 IV_HDMI_DDCCLK — IV_HDMI_DDCCLK — A8
T145 — RS740_DFT_GPIO1 — B7
T144 — A7
35 +NB_CORE_ON — R49 0_4 — STRP_DATA — B10
RSVD — G11
T143 — RS780_AUX_CAL — AUX_CAL(NC) — C8

A13 — +1.8V_VDDLTP18_NB
B13
A15 — +1.8V_VDDLT_18_NB
B15
A14 — +3V_VDLT33_NB
B14
C14, D15, C16, C18, C20, E20, C22

11/01 exchange LVDS_PWM /LVDS_BLON

E9 — INT_LVDS_DIGON — 20
F7 — INT_LVDS_PWM — 20
G12 — INT_LVDS_BLON — 20
R25 *1.97K/F_4
R11 *1.27K/F_4
For RX780 only

D9 — TMDS_HPD0 — R26 IV@0_4 — IV_HDMI_HPD — 19
D10 — TMDS_HPD1 — T2
D12 — SUS_STAT# NB — R71 0_4 — SUS_STAT# — 14
AE8 — R_NB_THRMDA — T142
AD8 — R_NB_THRMDC — T141
D13 — TEST_EN — R75 1.82K/F_4

selects Loading of straps from EPROM
1 : use default vaule , default
0 : I2C Master can load strap values from EEPROM
if connected, or use default values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT

RX780
RS780_AUX_CAL — R491 *3K_4

Enables Debug Bus acess through memory T/O pads and GPIO.
1 : Enable RX780 , Default
0 : Disable RX780

RX780
INT_TV_C/R — R96 *3K_4

Reserved only

12/22 stuff R65

Enables Debug Bus acess through memory T/O pads and GPIO.
1 : Enable RS780 , Default
0 : Disable RS780
(RS780 use VSYNC#)

RS780
INT_VSYNC — R65 3K_4 — +3V
R66 *3K_4

Indicates if memory Side port is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)

RS780
INT_HSYNC — R489 3K_4 — +3V
R490 *3K_4

10/19 RS780M Databook rev 1.01 define High disable

+3V — BLM18PG221SN1D(220,1.4A)_6 — L2 — +3V_AVDD_NB
C104 2.2u/6.3V_6
AVDD-DAC Analog
not applicable to RX780

+1.1V_NB — BLM18PG221SN1D(220,1.4A)_6 — L53 — +1.1V_PLLVDD
C646 2.2u/6.3V_6
PLLVDD - Graphics PLL
not applicable to RX780

1/17 RX781 connect to GND
C104,C110,C646,C98,C136,C103,C118 change to CS00003J951

+1.8V — BLM18PG221SN1D(220,1.4A)_6 — L51 — +1.8V_VDDLTP18_NB
C103 2.2u/6.3V_6
VDDLTP18 - LVDS or DVI/HDMI PLL
not applicable to RX780

+1.8V — L12 — BLM18PG221SN1D(220,1.4A)_6 — +1.8V_PLLVDD18
C124 10u/6.3V_8
C110 2.2u/6.3V_6
PLLVDD18 - Graphics PLL
not applicable to RX780

+1.8V — R76 0_6 — +1.8V_AVDDDI_NB
C98 2.2u/6.3V_6
AVDDI-DAC Digital
not applicable to RX780

BLM18PG221SN1D(220,1.4A)_6 — L17 — +1.8V_AVDDQ_NB
C136 2.2u/6.3V_6
AVDDQ-DAC Bandgap Reference
not applicable to RX780

BLM21PG221SN1D(220,100M,2A)_8 — L10 — +1.8V_VDDLT_18_NB
C118 4.7u/6.3V_6
C115 0.1u/10V_4
1/17 RX781 no stuff them
L2,L12,C124,L52,R76,L17,L51,L10,C115
VDDLT18 - LVDS or DVI/HDMI digital
not applicable to RX780

+1.8V — VDDA18PCIEPLL -PCIE PLL
L1 — 20mils width — +1.8V_VDDA18PCIEPLL — BLM18PG221SN1D(220,1.4A)_6
C79 2.2u/6.3V_6

VDDA18HTPLL -HT LINK PLL
L13 — 20mils width — +1.8V_VDDA18HTPLL — BLM18PG221SN1D(220,1.4A)_6
C131 2.2u/6.3V_6

1/31 voltage leakage issue
remove Q5,Q3,R83,R80,R97
stuff R88,R77

+1.8V — +VDDQ_NB
Q5 *BSS138_NL/SOT23
R83 *4.7K_4
4,13 CPU_LDT_STOP# — NB_LDT_STOP#
R88 0_4
RS780

+1.8V — +VDDQ_NB
Q3 *BSS138_NL/SOT23
R80 *4.7K_4
4 CPU_LDT_REQ# — R74 0_4 — NB_ALLOW_LDTSTOP
13 ALLOW_LDTSTOP — R77 0_4
RS780

RX780 — R108 *0_6 — +1.8V — +VDDQ_NB
RS780 — R97 *0_6 — +3V

+3V — L9 — +3V_VDLT33_NB
*BLM21PG221SN1D(220,100M,2A)_8
C108 *2.2u/6.3V_6
VDDLT33 - LVDS or DVI/HDMI ANALOG
RS740 only

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	RS740/RS780-SYSTEM I/F 3/5	1A

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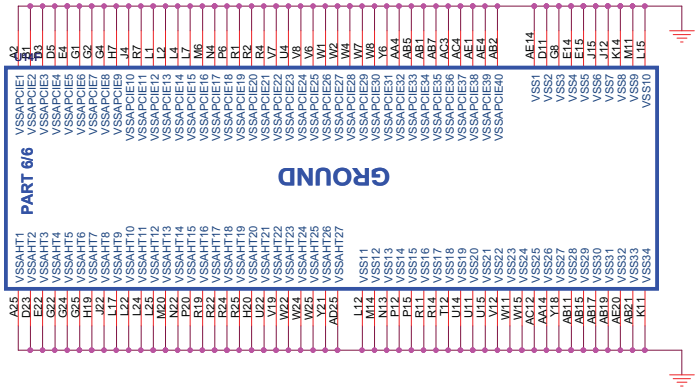
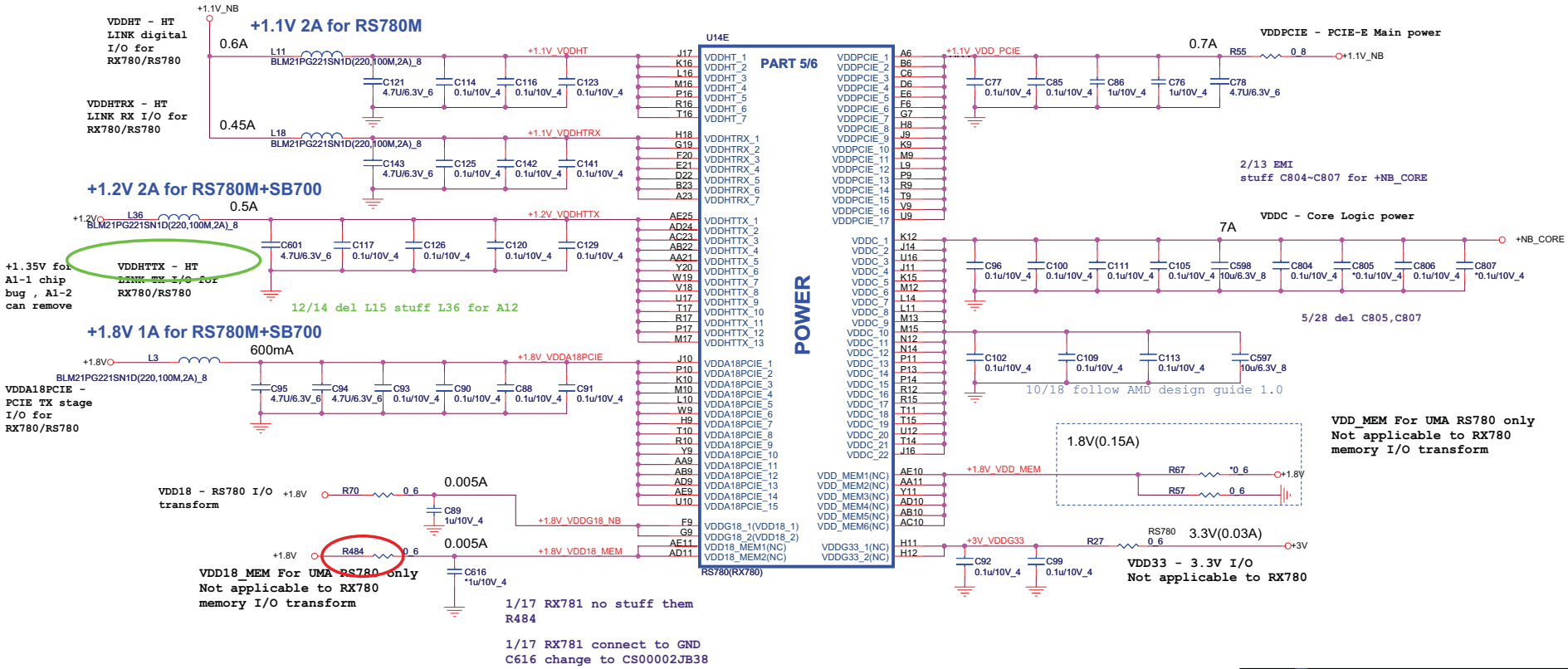


RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC



PROJECT : BD3G

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Size	Document Number	Rev
	RS740/RS780-POWER5/5	1A

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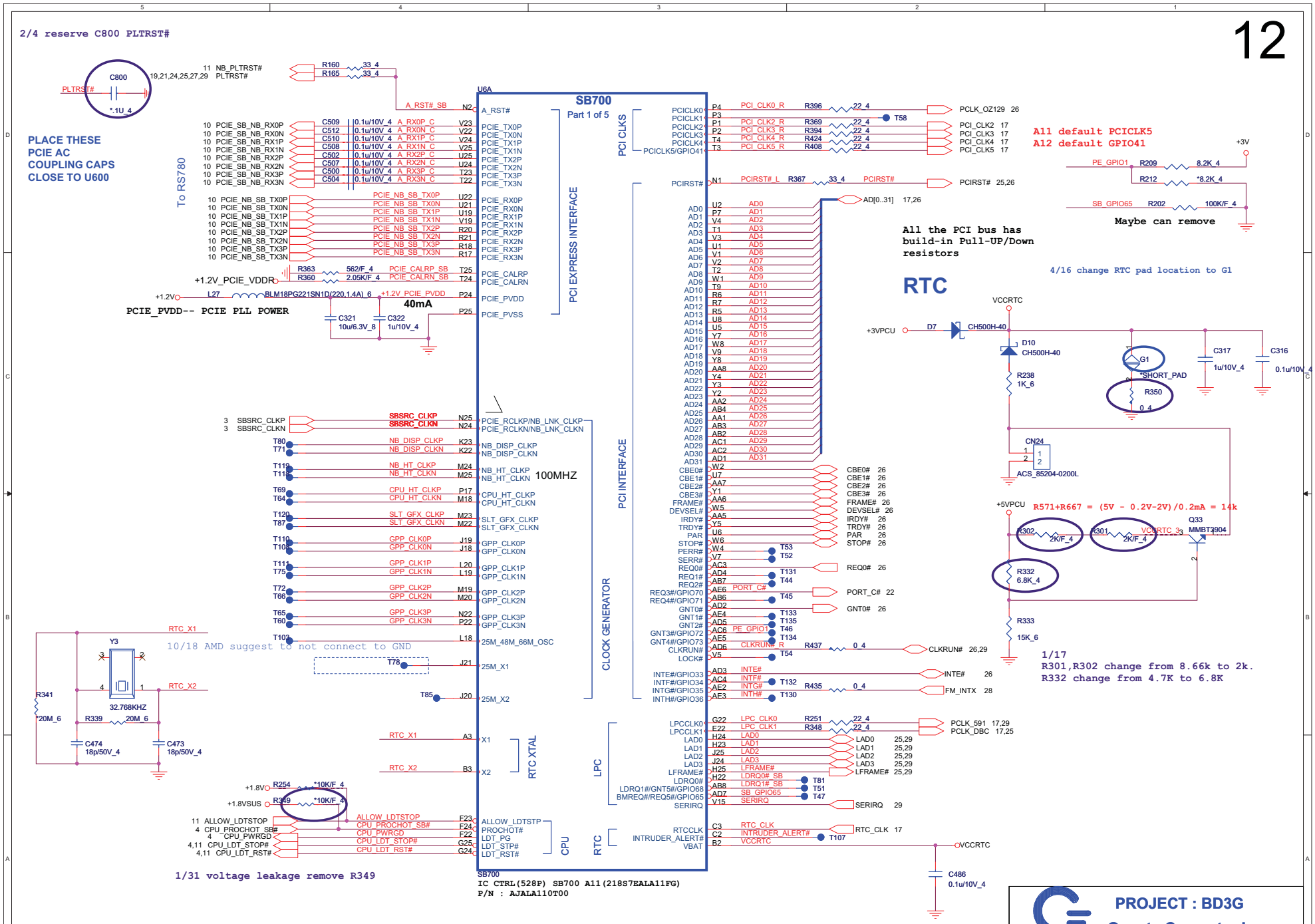
2/4 reserve C800 PLTRST#



PROJECT : BD3G

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Size	Document Number	Rev
	SB700-PCIE/PCI/CPU/LPC 1/4	1A

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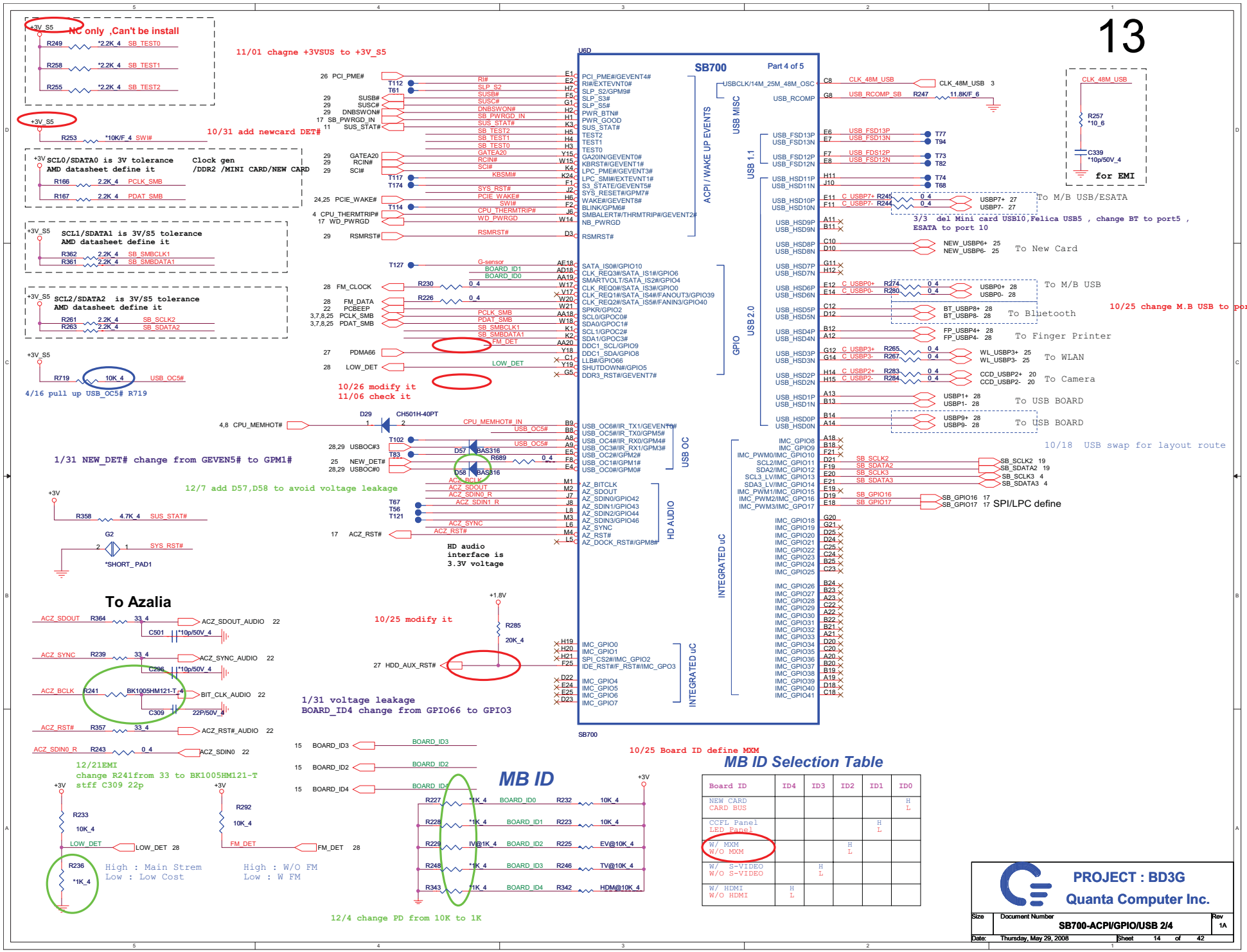

MB ID Selection Table

Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD CARD BUS					H L
CCFL Panel LED Panel				H L	
W/ MXM W/O MXM			H L		
W/ S-VIDEO W/O S-VIDEO		H L			
W/ HDMI W/O HDMI	H L				

PROJECT : BD3G

Quanta Computer Inc.

Size	Document Number	Rev
	SB700-ACPI/GPIO/USB 2/4	1A

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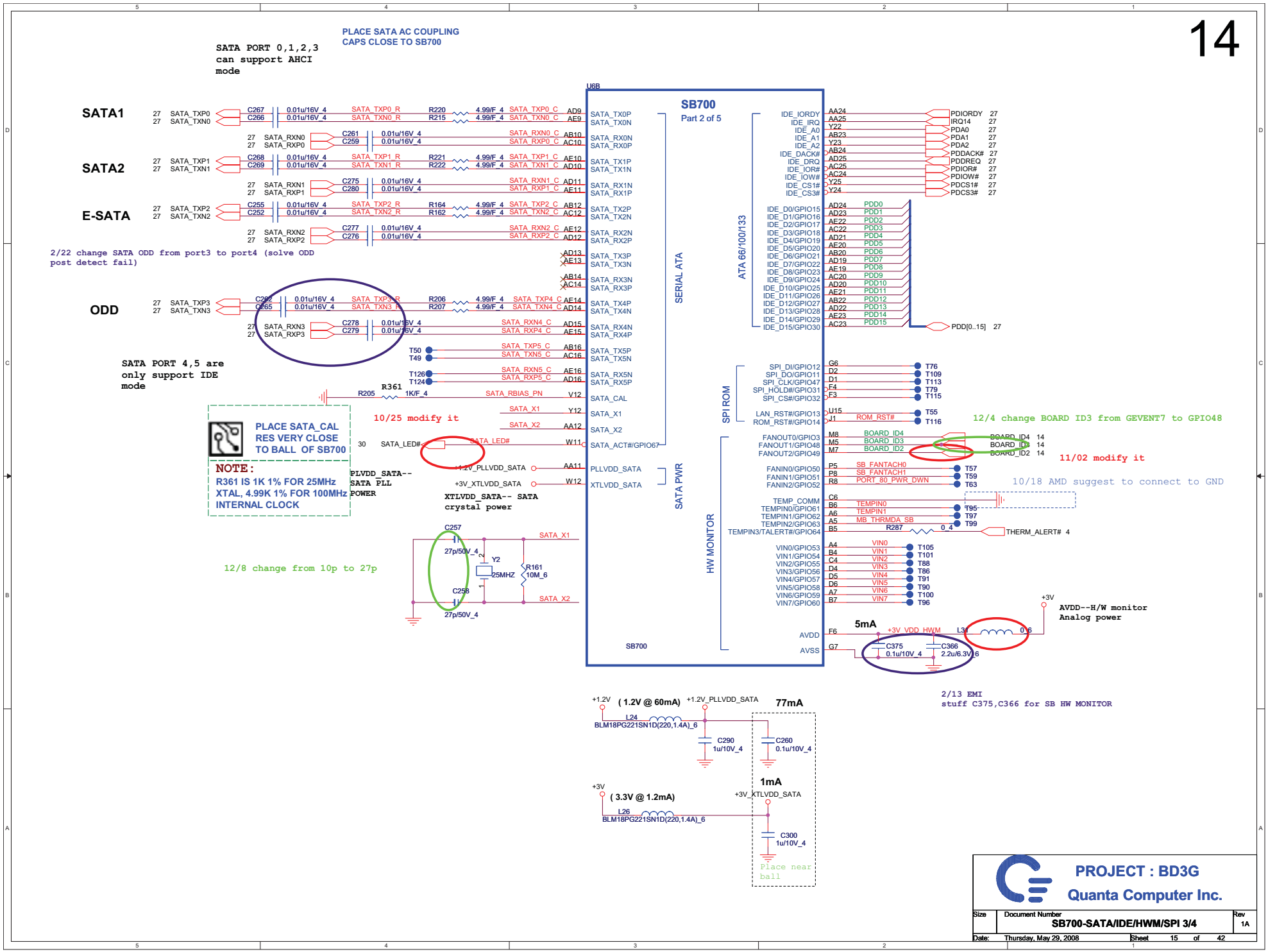

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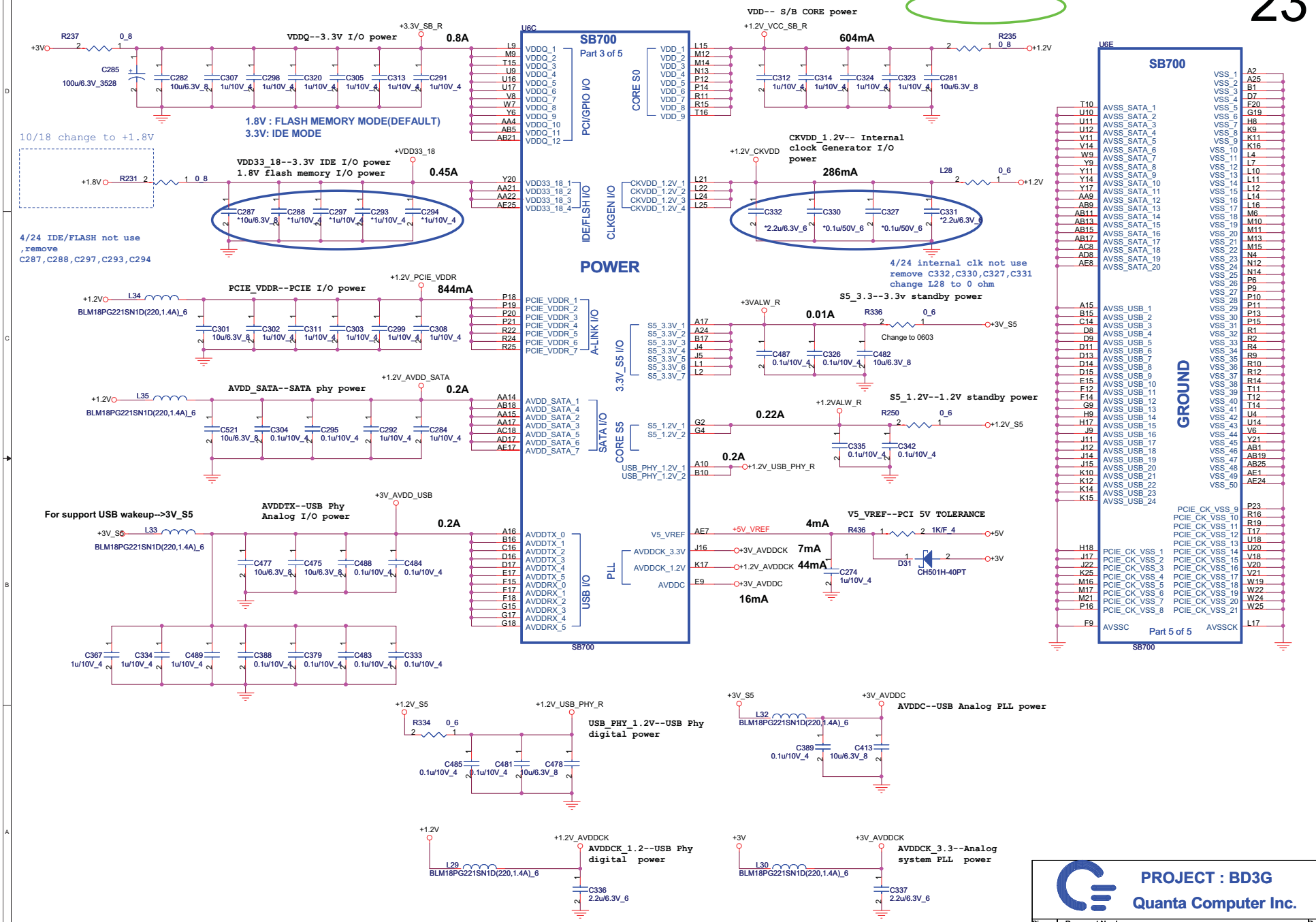
PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

12/14 del R234 stuff R235 for A2



PROJECT : BD3G

Quanta Computer Inc.

Size	Document Number	Rev
	SB700-PWR/DECOUPLING 4/4	1A

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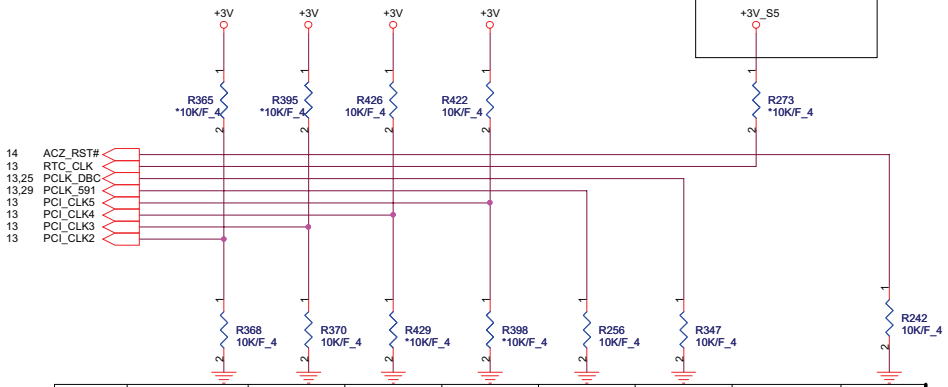
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready refore RSMRST#



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT

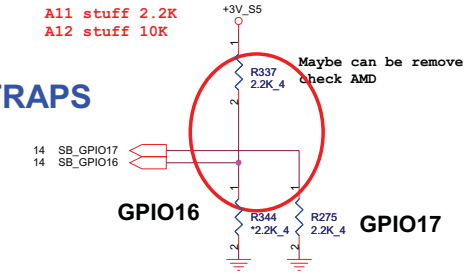
EC ENABLED

ENABLE PCI MEM BOOT

REQUIRED STRAPS

A11 stuff 2.2K
A12 stuff 10K

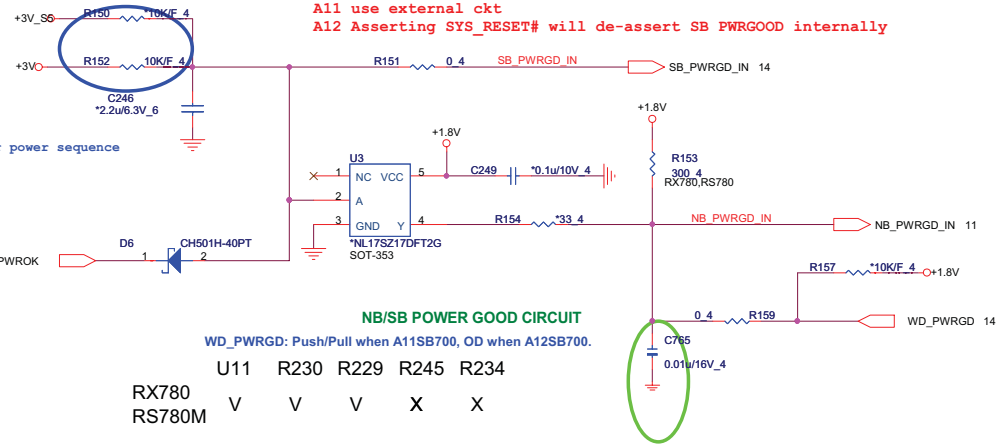
Maybe can be remove -- internla pull up check AMD



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

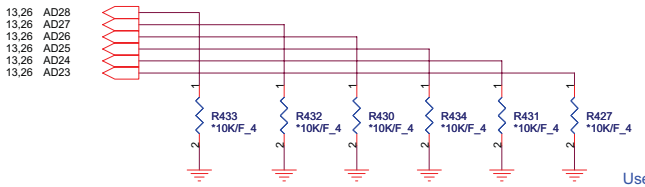
SB_PWRGD
A11 use external ckt
A12 Asserting SYS_RESET# will de-assert SB PWRGOOD internally



4/10 change R150 to R152 for power sequence

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB/SB POWER GOOD CIRCUIT

WD_PWRGD: Push/Pull when A11SB700, OD when A12SB700.

	U11	R230	R229	R245	R234
RX780 RS780M	V	V	V	X	X

12/18 add cap for NB_PWRGD signal

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

4/24 stuff C765 10nf to meet power sequence

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	SB700-STRAPS	1A

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TVOUT

BTO

5/8 stuff D9,D11 for S-VIDEO

TVOUT

close to NB & VGA connector

12/21 EMI
add 27p for TV_Y/G , TV_C/R

21 EXT_TV_Y/G — R497 EV@0_4 — SYS_TV_Y/G
21 EXT_TV_C/R — R496 EV@0_4 — SYS_TV_C/R
C790 EV@27p/50V_4 — C791 EV@27p/50V_4
11 INT_TV_Y/G — R189 IV@0_4
11 INT_TV_C/R — R190 IV@0_4
C792 IV@27p/50V_4 — C793 IV@27p/50V_4

BTO

+3V — D9 — TV-CHROMA — TV@DA204U
+3V — D11 — TV-LUMA — TV@DA204U

SYS_TV_C/R — L14 TV@BLM18PG181SN1D — TV-CHROMA — CN22 — TV-LUMA — L20 TV@BLM18PG181SN1D — SYS_TV_Y/G
R105 TV@150/F_4 — C149 TV@6p/50V_4 — C148 TV@6p/50V_4
C214 TV@6p/50V_4 — C215 TV@6p/50V_4 — R158 TV@150/F_4
TV@SUYIN_030018FR004S100FR

A:(10/24) change CN22 from 7PIN to 4PIN CONN

10/24 modify it to 4 pin BOI request
10/30 modify footprint to SV-030018FR004S100FR-RVS-4P-H
12/12 update p/n to DFMD04FR006
4/16 update footprint to sv-030018fr004s100fr-4p-h-b15m

CRT PORT

10/12 fix CRT connect error

2/10 DEL D4,D5 footprint and DEL CRT_SENSE# net

10/25 no use sense

2/1
RS780M A13 R8 ---> 140 CS11402FB19
MXM R8 ---> 150 CS11502FB21

1/31 EMI Change L4,L5,L6 from CX0HM121008 to CX8BA470003

close to NB & VGA connector

21 EXT_VGA_RED — R196 EV@0_4 — CRT_R
21 EXT_VGA_GRN — R195 EV@0_4 — CRT_G
21 EXT_VGA_BLU — R194 EV@0_4 — CRT_B
21 EXT_HSYNC — R198 EV@0_4 — HSYNC
21 EXT_VSYNC — R197 EV@0_4 — VSYNC
21 EXT_CRT_DDCCLK — R193 EV@0_4 — DDCCLK
21 EXT_CRT_DDCDAT — R192 EV@0_4 — DDCDAT

11 INT_CRT_RED — R184 IV@0_4
11 INT_CRT_GRN — R183 IV@0_4
11 INT_CRT_BLU — R182 IV@0_4
11 INT_HSYNC — R187 IV@0_4
11 INT_VSYNC — R186 IV@0_4
11 INT_CRT_DDCCLK — R181 IV@0_4
11 INT_CRT_DDCDAT — R180 IV@0_4

+5V — D30 SSM14 — F4 — FUSE/1A6V_POLY-1A-6V — 25 MIL — C433 0.1u/10V_4 — 5V_CRT2

CRT_R — L6 BLM18BA470SN1_6 — CRT_R1
CRT_G — L5 BLM18BA470SN1_6 — CRT_G1
CRT_B — L4 BLM18BA470SN1_6 — CRT_B1
R8 150/F — C11 6.8p_4 — R6 150/F_4 — C8 6.8p_4 — R4 150/F_4 — C5 6.8p_4 — C4 6.8p_4 — C7 6.8p_4 — C10 6.8p_4

A:(8/20) change from 39 to 0 ohm
Because MXM side already be stuff 30ohm

2/13 EMI
C4,C7,C10,C5,C8,C11 change from 10p to 6.8p

CN18 — DSUB-070549FR015SX03CX-15P-V — T17

A:(8/20) Reserve Diode for ESD solution

U4 CM2009
VCC_SYNC, SYNC_OUT2, SYNC_OUT1, VCC_DDC, BYP, VCC_VIDEO, SYNC_IN2, SYNC_IN1, VIDEO_1, VIDEO_2, VIDEO_3, DDC_IN1, DDC_IN2, DDC_OUT1, DDC_OUT2, GND
VSYNC1 — R14 0_4 — VSYNC1_CRT
HSYNC1 — R13 0_4 — HSYNC1_CRT
L8 — BLM18BA220SN1D_6 — CRTVSYNC
L7 — BLM18BA220SN1D_6 — CRTHSYNC
+5V — 5V_CRT2 — C25 0.22u/10V_6
+3V
CRT_R1 — CRT_G1 — CRT_B1
VSYNC — HSYNC — DDCCLK — DDCDAT
CRTDCLK — CRTDDAT
H=1.75mm

LCD_ON
C14 *10p/50V_4 — C13 *10p/50V_4
A:(8/27) default no stuff
5V_CRT2 — R9 6.8K_4 — R7 6.8K_4
A:(8/28) change from 2.7k to 6.8k
Follow AMD check list
C8 *10p/50V_4 — C9 *10p/50V_4
A:(8/27) default no stuff

DDCCLK — R22 4.7K_4 — +3V
DDCDAT — R21 4.7K_4
A:(8/28) change from 2.2k to 4.7k
Follow AMD check list

+5V — C24 0.1u/10V_4
+3V — C18 0.1u/10V_4

PROJECT : BD3G
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Size	Document Number	Rev
	SB600 STRAPS/TV/CRT	2A

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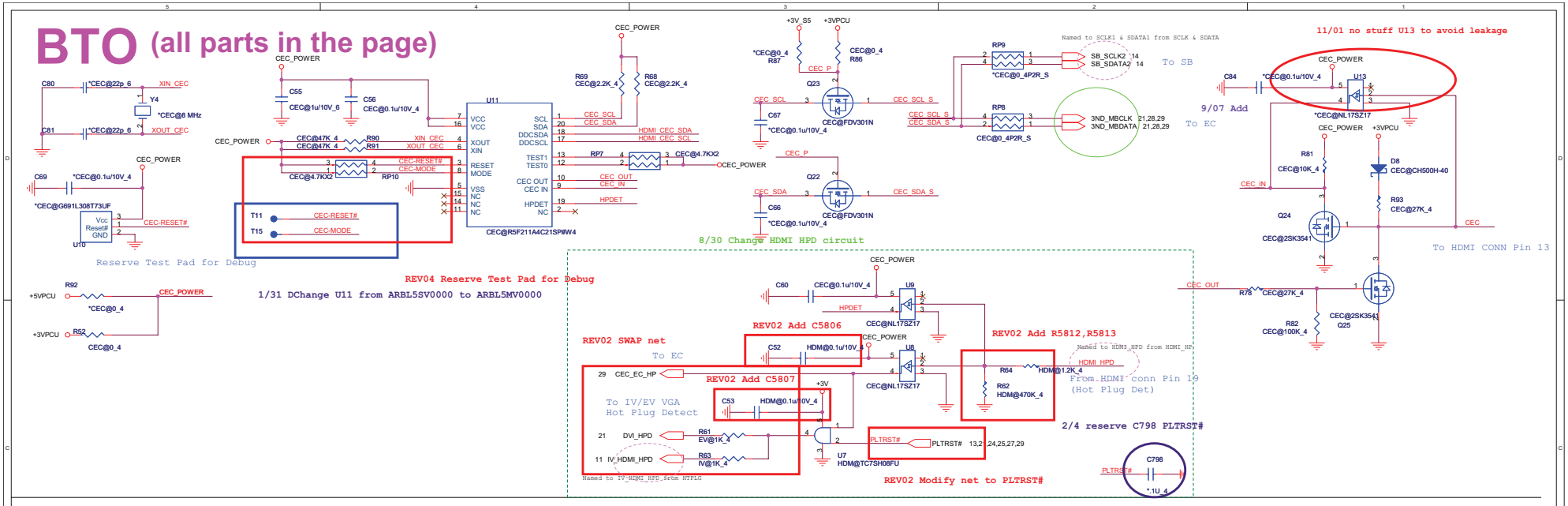
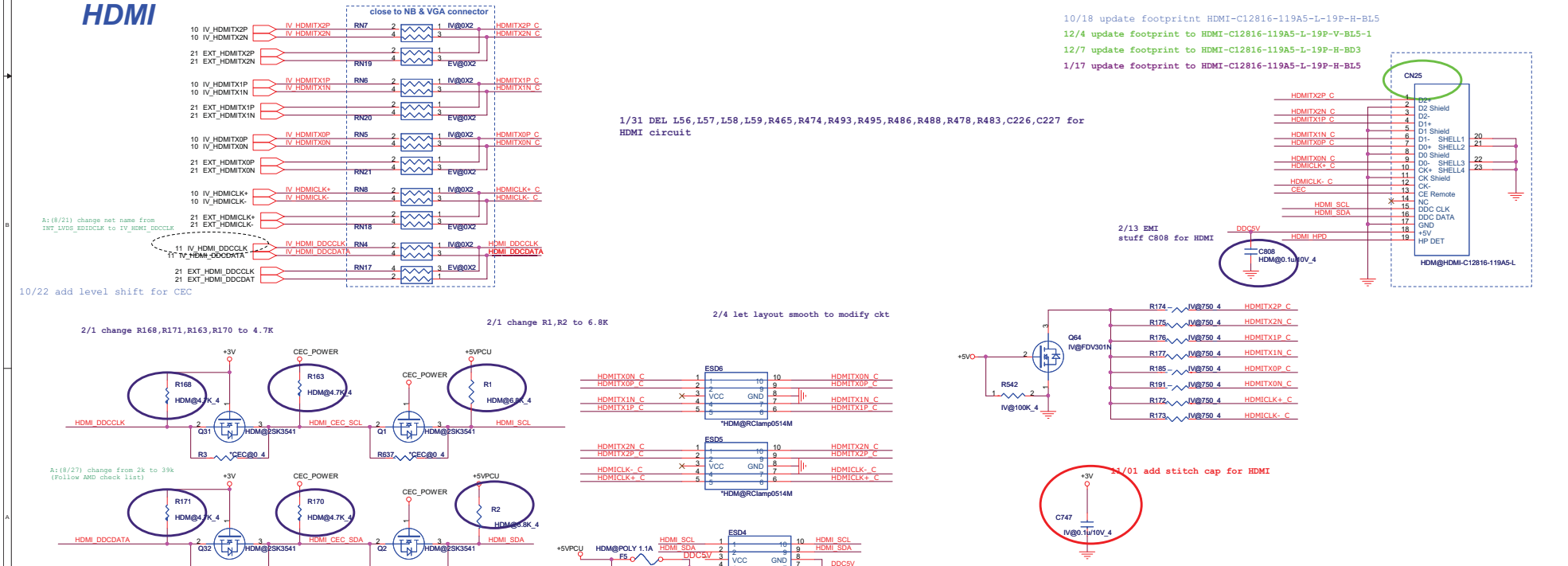
BTO (all parts in the page)



HDMI



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Size	Document Number	Rev
	HDMI + CEC	2A

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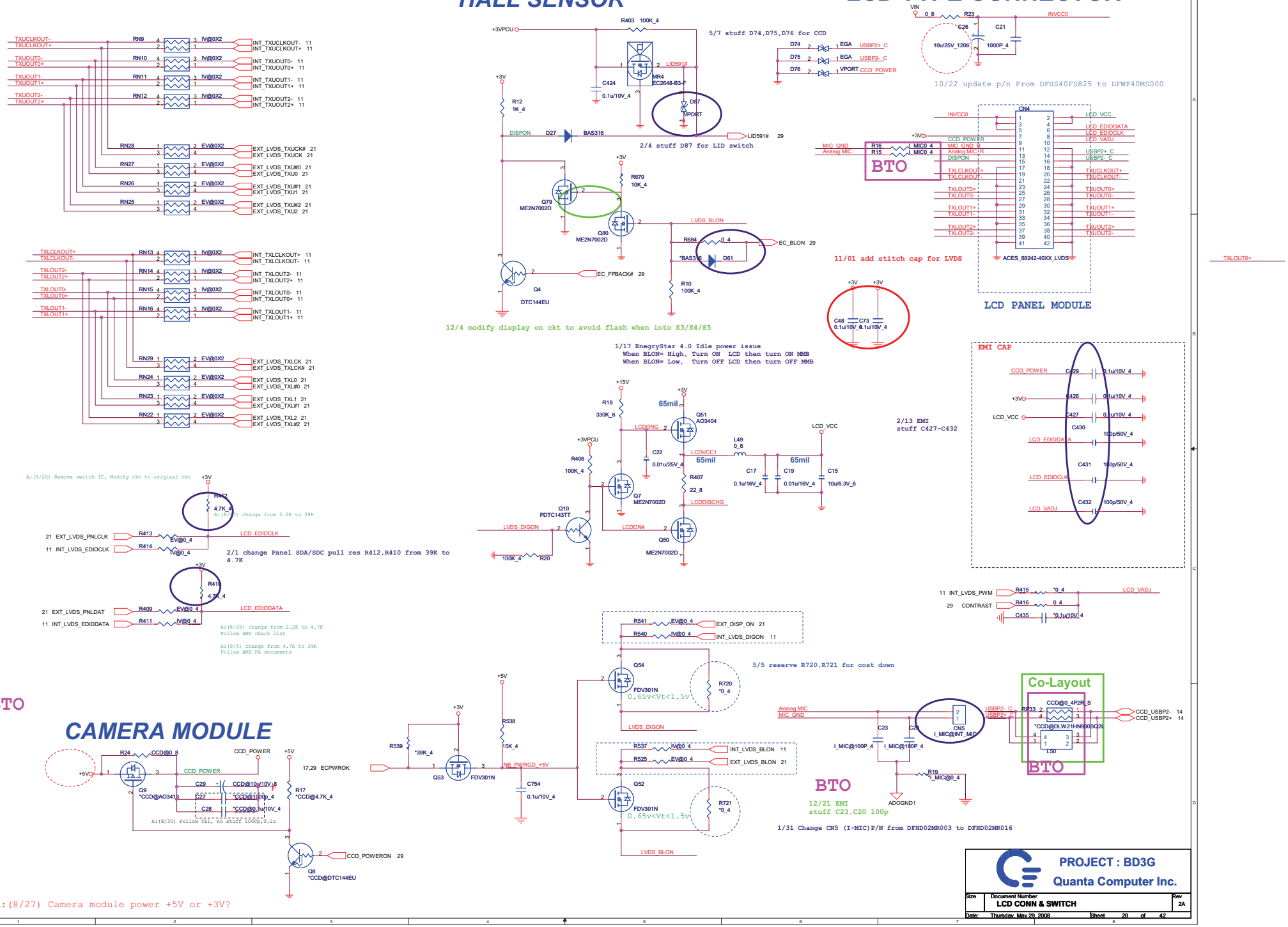
HALL SENSOR

LCD TYPE CONNECTOR



PROJECT : BD3G

Quanta Computer Inc.

Size	Document Number	Rev
	LCD CONN & SWITCH	2A

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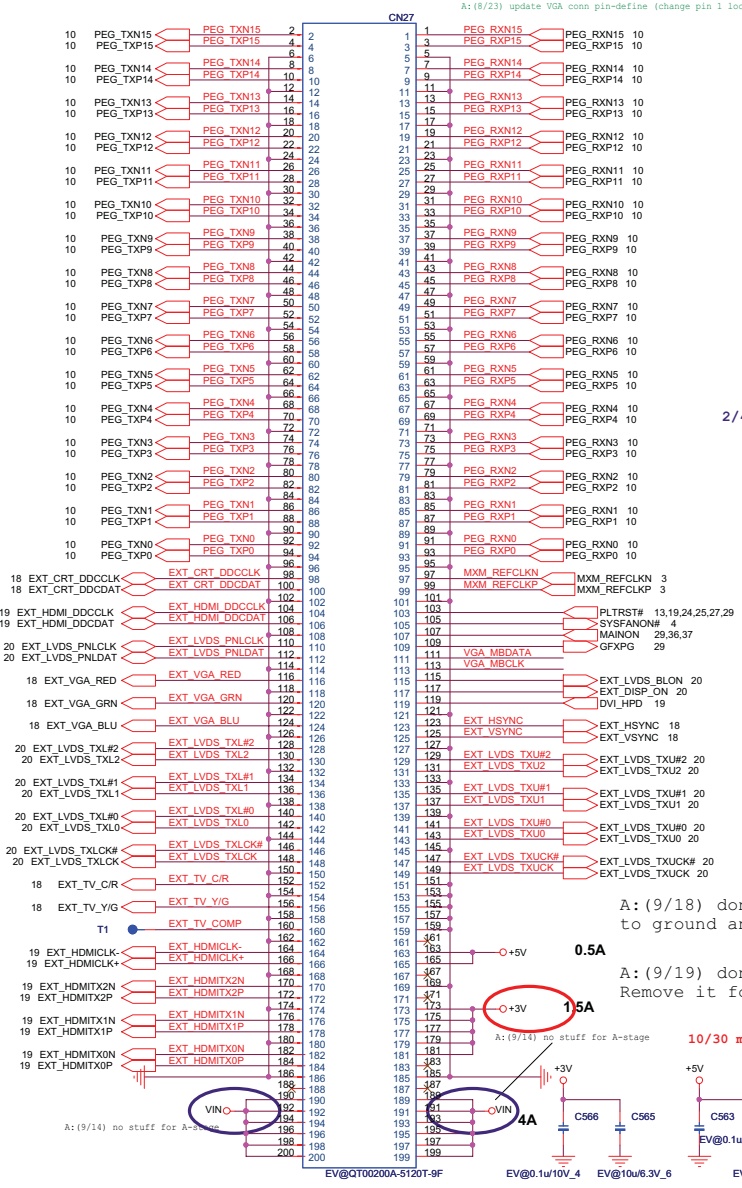
A:(8/18) update VGA conn footprint base on Allan information
A:(8/23) update VGA conn pin-define (change pin 1 location)

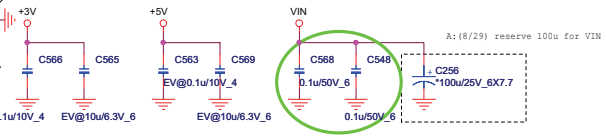


2/4 reserve C797 PLTRST#

A:(9/18) don˜t connect pin 161, 167, 171, 183, 187,188 to ground and reserve test point for A build.

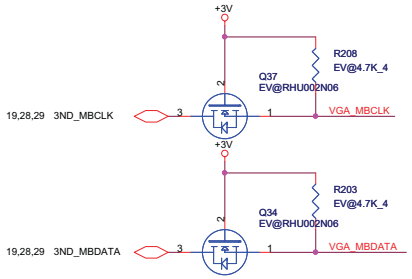
A:(9/19) don˜t have enough space to put the test point, Remove it for A-test

10/30 modify to +3V



1/17 Remove R492,R517, Short CN27/Pin189,190 to VIN directly.

12/21 EMI
stuff C568,C548



PROJECT : BD3G
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Size	Document Number	Rev
	MXM CONNECTOR / TV	2A

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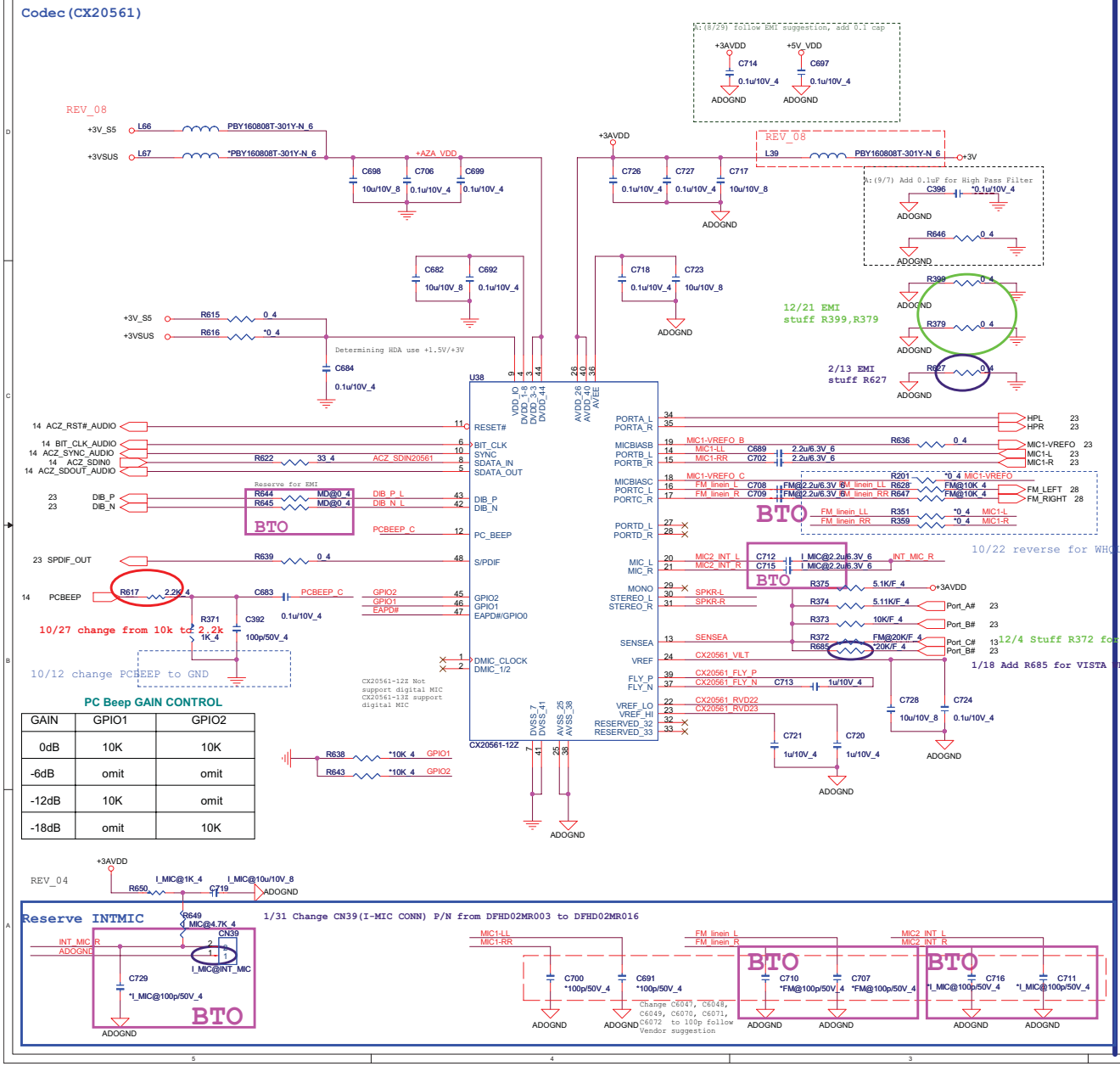
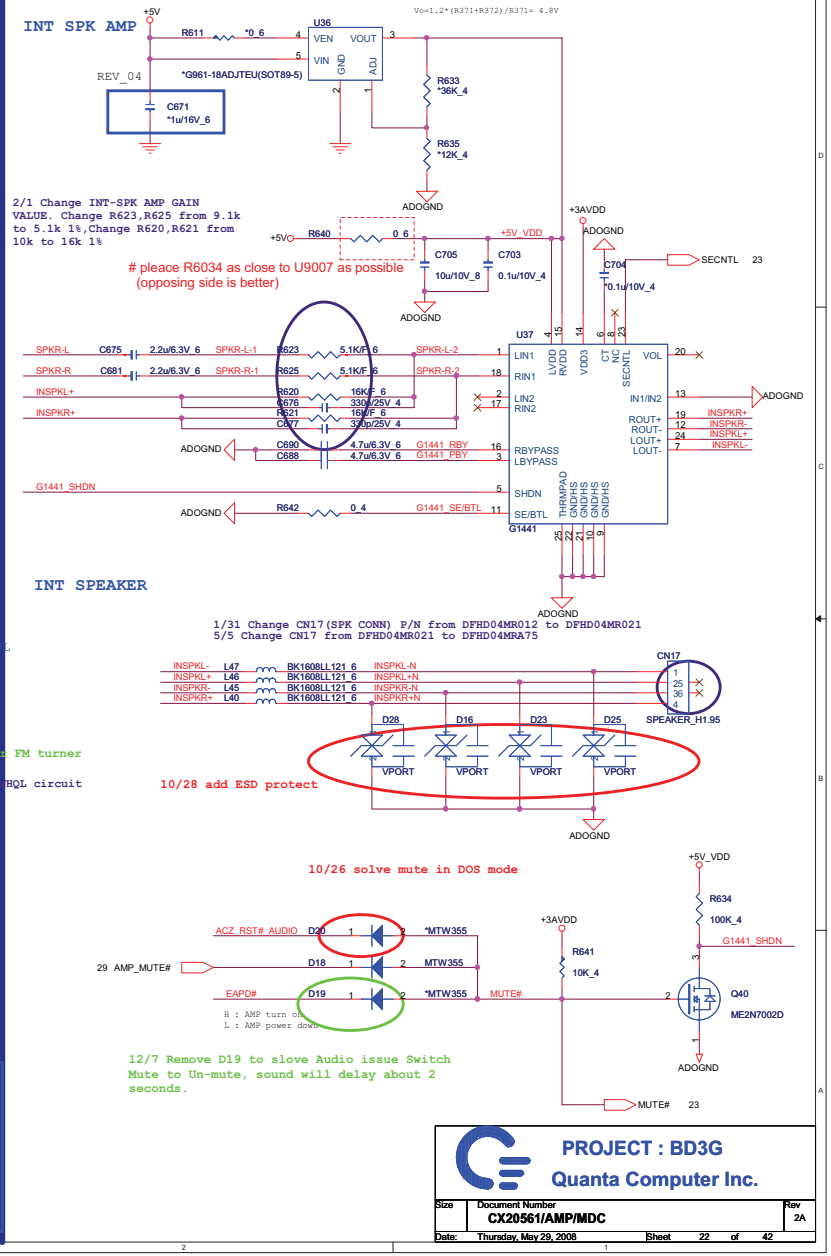
Codec (CX20561)



PC Beep GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K



PROJECT : BD3G

Quanta Computer Inc.

Size	Document Number	Rev
	CX20561/AMP/MDC	2A

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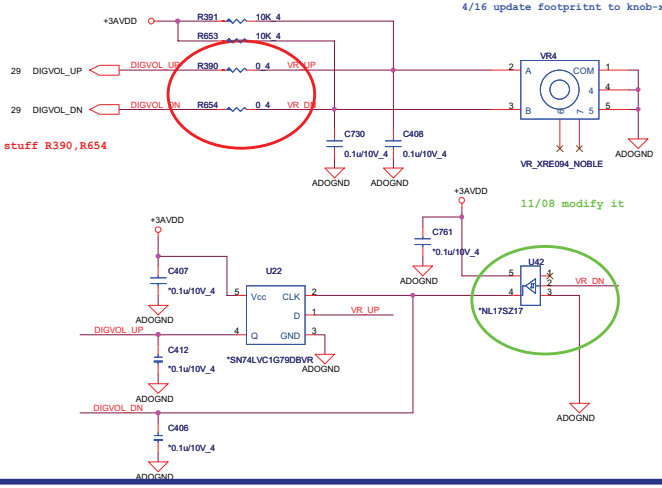
VR

4/16 update footpritnt to knob-xre094-3p-b15m

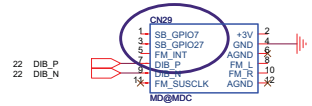


MDC

REV_04

1/18 Change CN43 footprint from MDC-1-179373-2-12P-RUV to MDC-1-179373-2-12P-RUV-BD3A (SMT open issue)

BTO



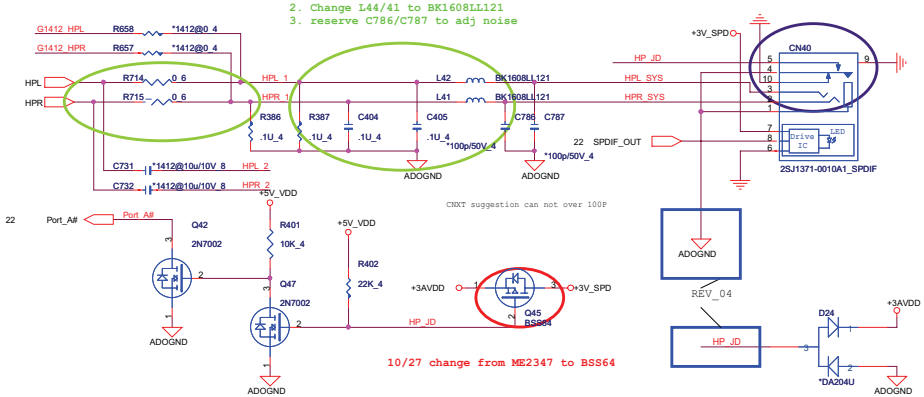
HP

12/07 Slove Audio issue:When plug in-out headphone,headphone has bo sound.
1. Change R652&R651 to C763,C764(10U/6.3V 0603)

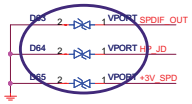
2/5 Change R714,R715 from 10uF to 0 ohm (Audio HP circuit)

12/20 solve GPRS noise
1. stuff R386/R387/C404/C405 to 0.1U
2. Change L44/41 to BK1608LL121
3. reserve C786/C787 to adj noise

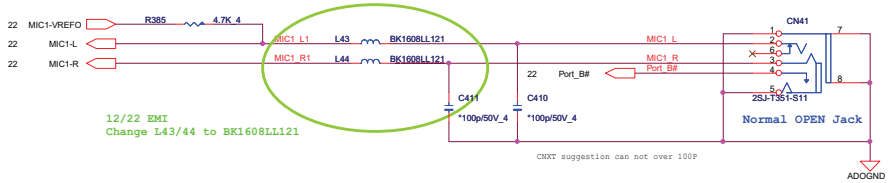
2/4 CN40 pin 9/10 connect to GND

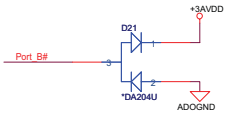


2/4 add Varistor D63,D64,D65 on SPDIF_OUT/HP_JD/+3V_SPD



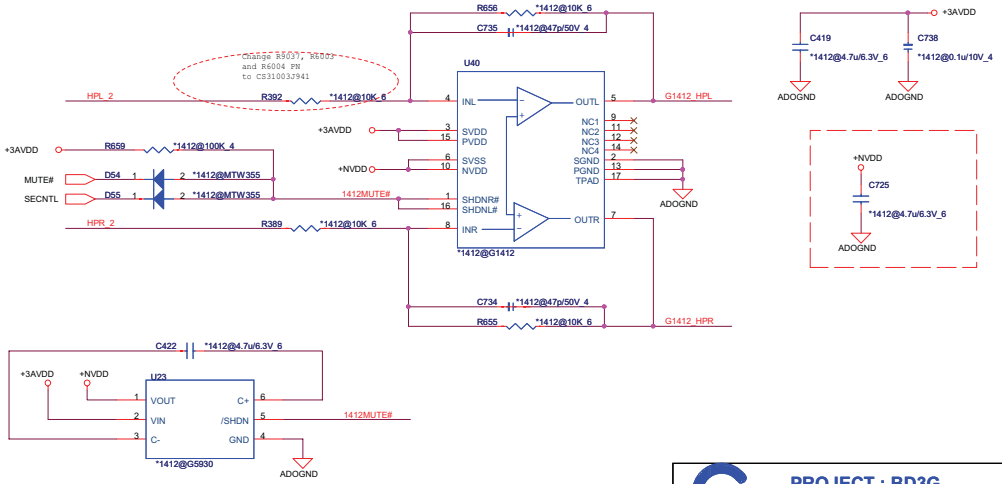
SYSTEM MIC





HP Amplifier

REV_05



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Quanta Computer Inc.		
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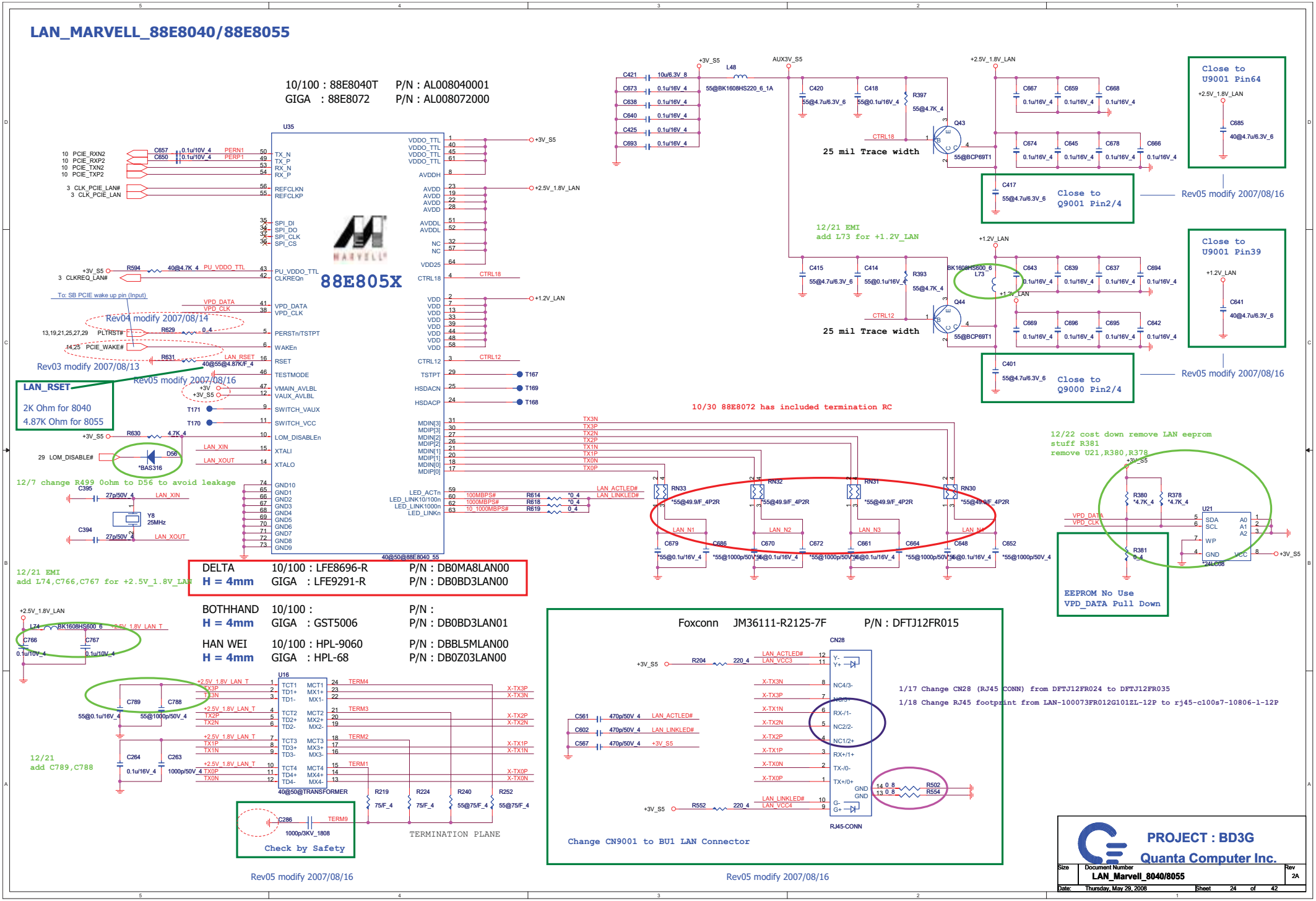
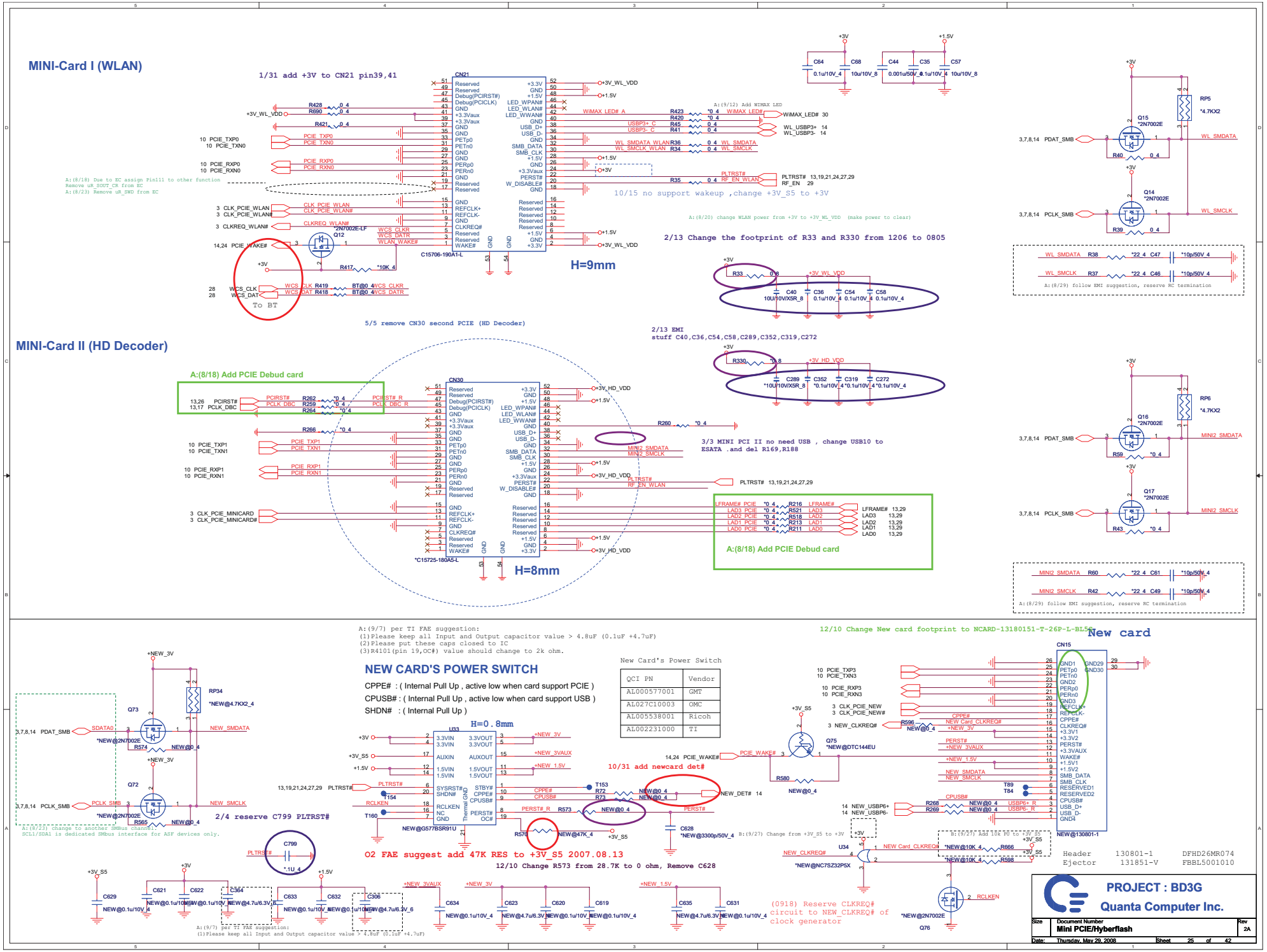
LAN_MARVELL_88E8040/88E8055





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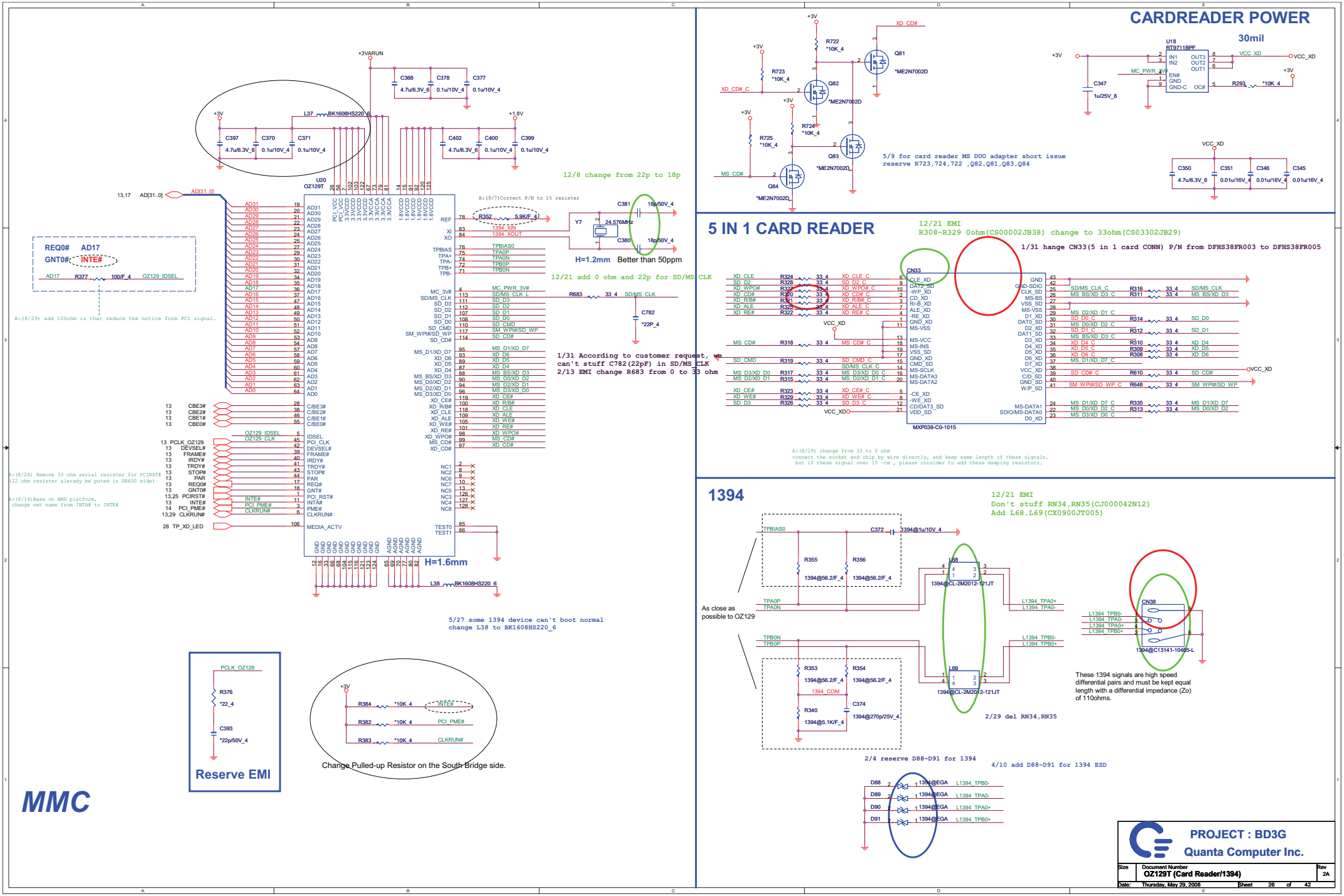
CARDREADER POWER
30mil
U18
RT9711BPF
IN1
IN2
OUT3
OUT2
OUT1
EN#
GND
GND-C
OC#
VCC_XD
MC_PWR_3V
R293
*10K_4
C347
1u/25V_8
C350
4.7u/6.3V_6
C351
0.01u/16V_4
C346
0.01u/16V_4
C345
0.01u/16V_4
R722
*10K_4
R723
*10K_4
R724
*10K_4
R725
*10K_4
Q81
*ME2N7002D
Q82
*ME2N7002D
Q83
*ME2N7002D
Q84
*ME2N7002D
XD_CD#
XD_CD# C
MS_CD#
5/9 for card reader MS DUO adapter short issue
reserve R723,724,722 ,Q82,Q81,Q83,Q84
5 IN 1 CARD READER
12/21 EMI
R308~R329 0ohm(CS00002JB38) change to 33ohm(CS03302JB29)
1/31 hange CN33(5 in 1 card CONN) P/N from DFHS38FR003 to DFHS38FR005
CN33
MXP038-C0-1015
A:(8/29) change from 33 to 0 ohm
connect the socket and chip by wire directly, and keep same length of these signals.
but if these signal over 15 -cm , please consider to add these damping resistors.
1394
12/21 EMI
Don't stuff RN34,RN35(CJ000042N12)
Add L68,L69(CX0900JT005)
TPBIAS0
C372
1394@1u/10V_4
R355
1394@56.2/F_4
R356
1394@56.2/F_4
L68
1394@CL-2M2012-121JT
TPA0P
TPA0N
L1394_TPA0+
L1394_TPA0-
As close as
possible to OZ129
TPB0N
TPB0P
L1394_TPB0-
L1394_TPB0+
R353
1394@56.2/F_4
R354
1394@56.2/F_4
1394_COM
R340
1394@5.1K/F_4
C374
1394@270p/25V_4
L69
1394@CL-2M2012-121JT
CN38
1394@C13141-10405-L
These 1394 signals are high speed
differential pairs and must be kept equal
length with a differential impedance (Zo)
of 110ohms.
2/29 del RN34,RN35
2/4 reserve D88~D91 for 1394
4/10 add D88~D91 for 1394 ESD
D88
D89
D90
D91
1394@EGA
L1394_TPB0-
L1394_TPA0-
L1394_TPA0+
L1394_TPB0+
+3VARUN
C368
4.7u/6.3V_6
C378
0.1u/10V_4
C377
0.1u/10V_4
L37
BK1608HS220_6
C397
4.7u/6.3V_6
C370
0.1u/10V_4
C371
0.1u/10V_4
C402
4.7u/6.3V_6
C400
0.1u/10V_4
C399
0.1u/10V_4
U20
OZ129T
12/8 change from 22p to 18p
A:(9/7)Correct P/N to 1% resister
R352
5.9K/F_4
Y7
24.576MHz
C381
18p/50V_4
C380
18p/50V_4
H=1.2mm
Better than 50ppm
12/21 add 0 ohm and 22p for SD/MS CLK
R683
33_4
SD/MS_CLK
C782
*22P_4
1/31 According to customer request, we
can't stuff C782(22pF) in SD/MS_CLK
2/13 EMI change R683 from 0 to 33 ohm
REQ0#
AD17
GNT0#
INTE#
AD17
R377
100/F_4
OZ129_IDSEL
A:(8/29) add 100ohm is that reduce the notice form PCI signal.
A:(8/24) Remove 33 ohm serial resister for PCIRST#
(22 ohm resister alerady be puted in SB600 side)
A:(8/14)Base on AMD platform,
change net name from INTA# to INTE#
H=1.6mm
L38
BK1608HS220_6
5/27 some 1394 device can't boot normal
change L38 to BK1608HS220_6
PCLK_OZ129
R376
*22_4
C393
*22p/50V_4
Reserve EMI
R384
*10K_4
INTE#
R382
*10K_4
PCI_PME#
R383
*10K_4
CLKRUN#
Change Pulled-up Resistor on the South Bridge side.
MMC
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Quanta Computer Inc.
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Document Number
OZ129T (Card Reader/1394)
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FLASH

4/10 remove Flash card ckt

Flash moduel operate at 1.8V
Pin2, 20 is NC for Flash module

11/01 modify it

10/30 use H:5.2 for A-test

10/29 add four stitch cap

SATA ODD

9/28 change to SATA ODD conn to BD3G use

10/22 update footprint to SATA-C18534-11305-13P-R

Check New ODD CONN Pin Define.

Device Present

ESATA

4/14 change R706 from 0 ohm to 330 , stuff R692,R693,R694

2/13 add ESATA re-driver IC

5/5 update re-driver footprint
to tqfn36-5x6-5-37p-0_75h-telm

Close IC, no stub at high-speed trace on PCB layout.

Option SB to ESATA directly

2/29 del R572,R569

Co-lay ESATA footprint

2/26 change ESATA conn usb-2006109-11p
update p/n to DFHS11FR021

4/10 change ESATA conn usb-2006109-11p
update p/n to DFHS11FR023

4/10 add D67,D49,D50 for ESATA USB ESD

5/29 change ESATA conn p/n to DFHS11FR027

2/20
1.change C801,C82 from 0.01u to 4.7n
2.RX add C811,C812 4.7n

SEL0_X	SEL1_X	Eq	SEL2_X	Swing	SEL3_X	De-Emphasis
0	0	0dB	0	1.0X	0	0dB
0	1	2.5dB	1	1.2X	1	-3.5dB
1	0	4.5dB				
1	1	6.5dB				

2/4 reserve D67 for CN31

4/17 remove D77~D81 for CN34 , change to U44 CM1213-04SO

5/5 add C816 0.01u to U44 +5V for ESD

SATA HDD

A:(8/17) Add Cap for SATA interface

2/4 del R270,R597 , connect to +5V directly

2'nd SATA HDD

A:(9/5) update footprint
A:(9/13) update footprint

1/17 Change CN32(2nd SATA CONN) from DFHS22FR064 to DFHS22FR094

1/17 Change CN32 footprint from SATA-127043FR022XX27ZR-22P-L-H to SATA-127043FR022G285ZR-22P-L

1/31 Change CN34 (1st SATA) P/N from DFHS22FR063 to DFHS22FR082

1/31 Change CN32 (2nd SATA) P/N from DFHS22FR094 to DFHS22FR083

2/4 reserve D82~D86 for CN32(2ND HDD)

4/17 remove D82~D86 for CN32 , change to U45 CM1213-04SO

5/5 add C818 0.01u to U45 +5V for ESD

A:(8/17) Add Cap for SATA interface

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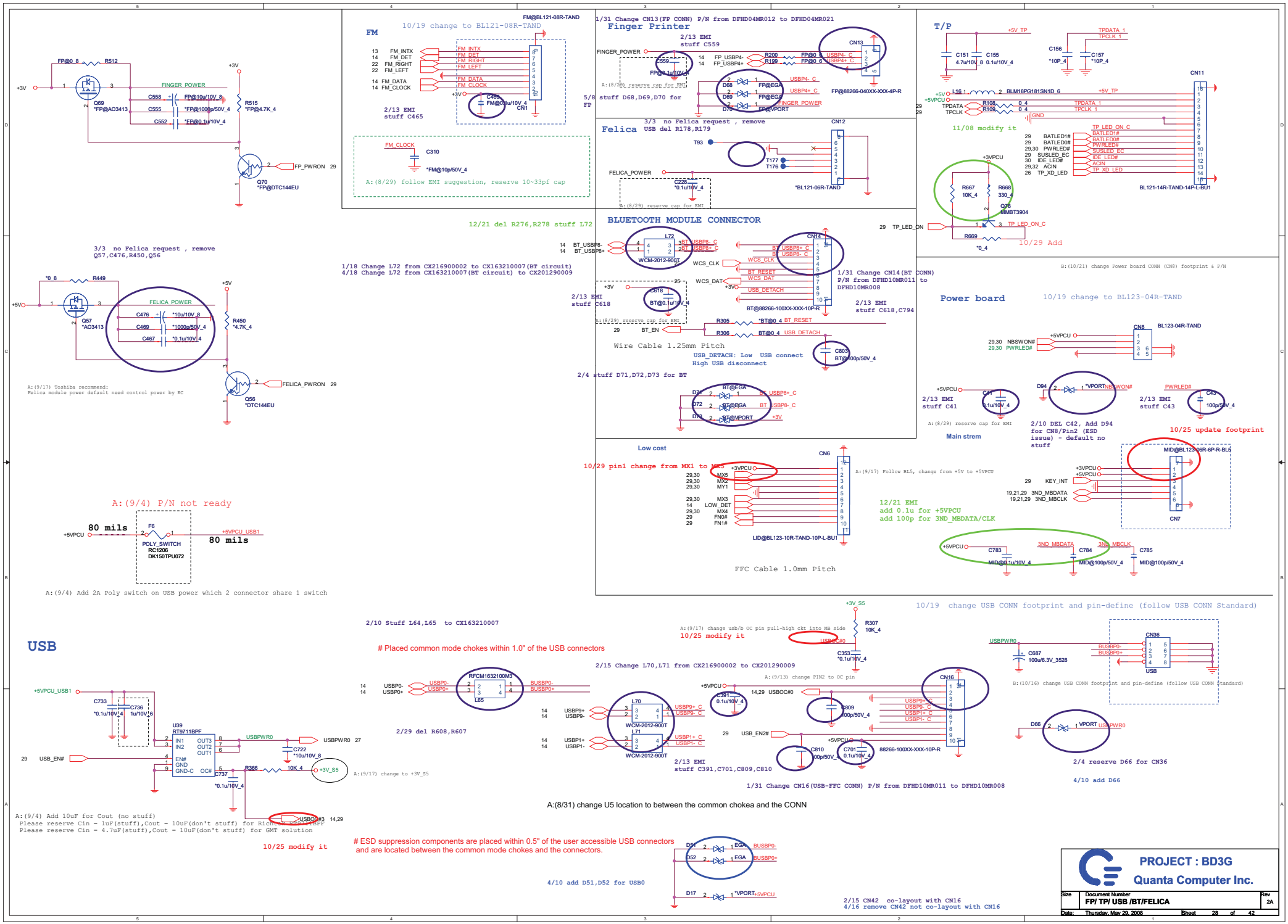
FM
10/19 change to BL121-08R-TAND
FM@BL121-08R-TAND
2/13 EMI stuff C465
A:(8/29) follow EMI suggestion, reserve 10~33pf cap
Finger Printer
1/31 Change CN13(FP CONN) P/N from DFHD04MR012 to DFHD04MR021
2/13 EMI stuff C559
5/8 stuff D68,D69,D70 for FP
FP@88266-040XX-XXX-4P-R
T/P
11/08 modify it
BL121-14R-TAND-14P-L-BU1
10/29 Add
Felica
3/3 no Felica request , remove USB del R178,R179
*BL121-08R-TAND
3/3 no Felica request , remove Q57,C476,R450,Q56
A:(9/17) Toshiba recommend: Felica module power default need control power by EC
12/21 del R276,R278 stuff L72
BLUETOOTH MODULE CONNECTOR
1/18 Change L72 from CX216900002 to CX163210007(BT circuit)
4/18 Change L72 from CX163210007(BT circuit) to CX201290009
WCM-2012-900T
1/31 Change CN14(BT CONN) P/N from DFHD10MR011 to DFHD10MR008
2/13 EMI stuff C618
2/13 EMI stuff C618,C794
BT@88266-100XX-XXX-10P-R
Wire Cable 1.25mm Pitch
USB_DETACH: Low USB connect
High USB disconnect
2/4 stuff D71,D72,D73 for BT
Low cost
10/29 pin1 change from MX1 to MX5
LID@BL123-10R-TAND-10P-L-BU1
FFC Cable 1.0mm Pitch
Power board
10/19 change to BL123-04R-TAND
BL123-04R-TAND
B:(10/21) change Power board CONN (CN8) footprint & P/N
2/13 EMI stuff C41
2/10 DEL C42, Add D94 for CN8/Pin2 (ESD issue) - default no stuff
2/13 EMI stuff C43
10/25 update footprint
Main strem
12/21 EMI add 0.1u for +5VPCU add 100p for 3ND_MBDATA/CLK
MID@BL123-06R-6P-R-BL5
A:(9/4) P/N not ready
80 mils
POLY_SWITCH RC1206 DK150TPU072
A:(9/4) Add 2A Poly switch on USB power which 2 connector share 1 switch
USB
2/10 Stuff L64,L65 to CX163210007
Placed common mode chokes within 1.0" of the USB connectors
2/15 Change L70,L71 from CX216900002 to CX201290009
10/25 modify it
10/19 change USB CONN footprint and pin-define (follow USB CONN Standard)
B:(10/16) change USB CONN footprint and pin-define (follow USB CONN Standard)
2/29 del R608,R607
2/13 EMI stuff C391,C701,C809,C810
1/31 Change CN16(USB-FFC CONN) P/N from DFHD10MR011 to DFHD10MR008
2/4 reserve D66 for CN36
4/10 add D66
A:(9/4) Add 10uF for Cout (no stuff)
Please reserve Cin = 1uF(stuff),Cout = 10uF(don't stuff) for Richtek RT9711BPF
Please reserve Cin = 4.7uF(stuff),Cout = 10uF(don't stuff) for GMT solution
10/25 modify it
A:(8/31) change U5 location to between the common chokea and the CONN
ESD suppression components are placed within 0.5" of the user accessible USB connectors and are located between the common mode chokes and the connectors.
4/10 add D51,D52 for USB0
2/15 CN42 co-layout with CN16
4/16 remove CN42 not co-layout with CN16
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Quanta Computer Inc.
Size
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FP/ TP/ USB /BT/FELICA
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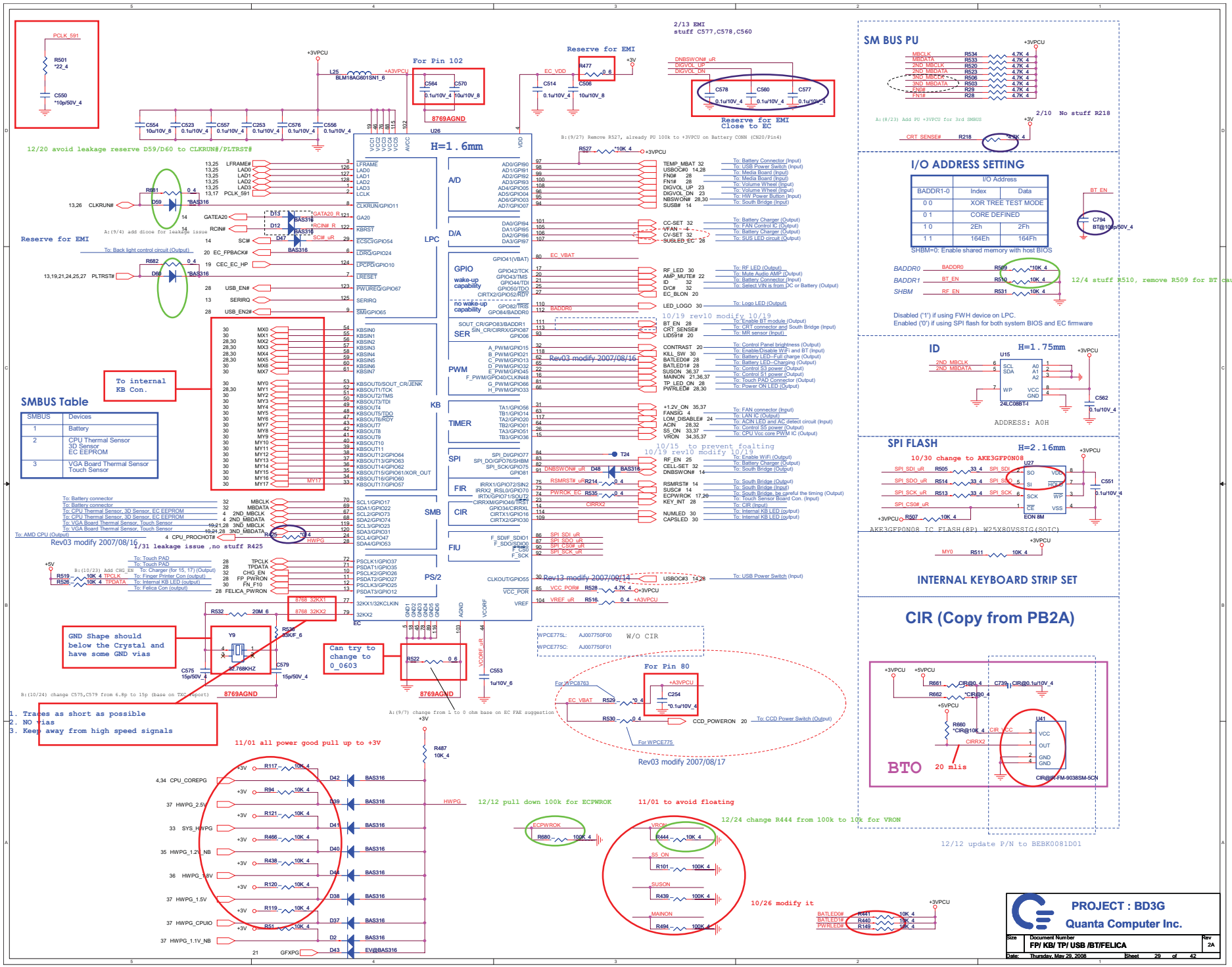

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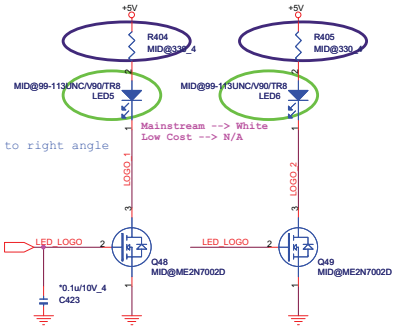
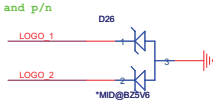
2/1 Change R404,R405 from CS13902JB14 (390 ohm) to CS13302JB21(330 ohm)

LOGO LED



10/16 update LED to right angle

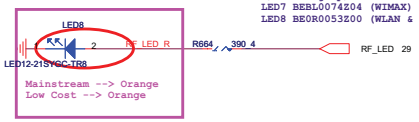
12/7 change LED5,LED6 footprint and p/n



W-LAN&BT

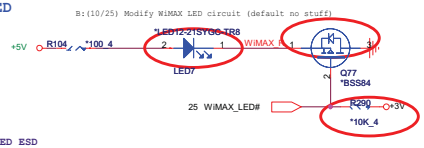
1/18 LED7,8 change footprint from LED12-21SYGC-TR8 to LED27-21-BHC-ZL1M2TY-3C

1/18 change p/n
LED7 BEBL0074Z04 (WIMAX)
LED8 BE0R0053Z00 (WLAN & BT)

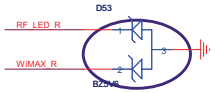


WiMAX LED

B:(10/25) Modify WiMAX LED circuit (default no stuff)

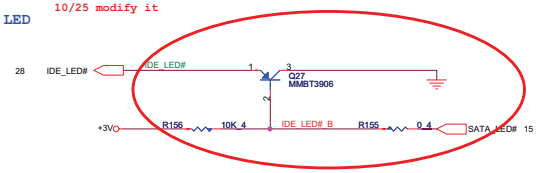


5/8 stuff D53 for RF_LED ESD



IDE LED

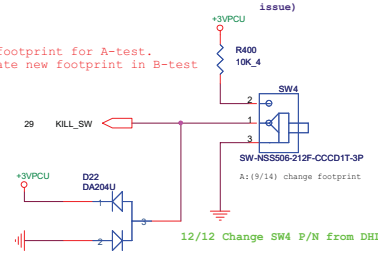
10/25 modify it



Kill SW

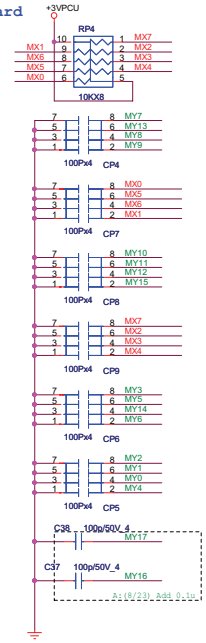
1/18 Change SW4 footprint from SW-NSS506-212F-CCCD1T-3P to SW-NSS506-212F-CCCD1T-3P-BD3A (SMT open issue)

Use old footprint for A-test.
Must update new footprint in B-test



12/12 Change SW4 P/N from DHL00212F05 to DHL00212F07

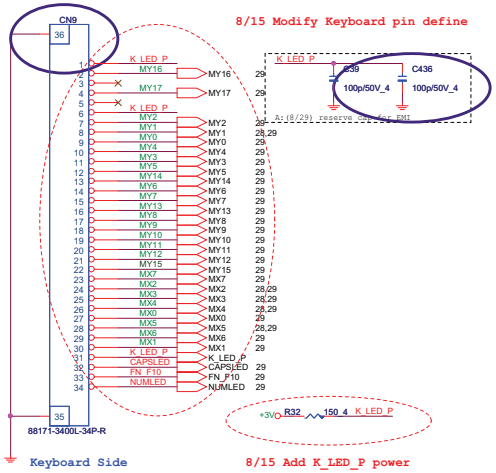
Keyboard



1/18 change footprint from 88171-3400L-34P-L to 91504-340N-34P-L

8/15 Modify Keyboard pin define

2/13 EMI
stuff C39,C436

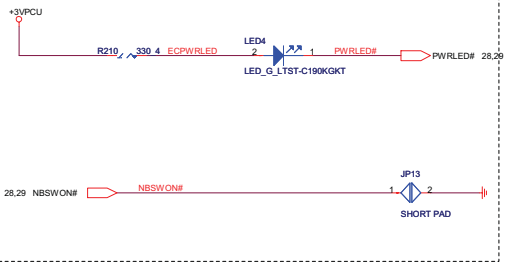


Keyboard Side

8/15 Add K_LED_P power

1/17 Remove CN10 (Keyboard CONN)

Jumper & LED (debug use)



A:(8/27) Confirm with EC FAE,
MY no need External PU resister

	15"	17"
CAPSLED K_LED_P (Pin 31)	V	V
FN_F10 K_LED_P (Pin 6)	V	
NUMLED K_LED_P (Pin 1)	V	V

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	SW/LED/KEYBOARD	2A

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HOLE

Take care NUT P/N base on IV/EV sku

1/18 HOLE 17,18.23 FBBL5004010
change to FBBL5002010

VGA NUT (BOT)

HOLE15 H-TC315BC236D146P2
HOLE24 H-C236D146P2
HOLE25 H-C236D146P2

10/31 EMI request

2/18 HOLE 15,24.25 FBBD3017010
change to FBBD3021010

MDC NUT (BOT)

HOLE32 MD@H-C236D146P2

CPU NUT (BOT)

HOLE17 H-C236D146P2
HOLE18 H-C236D146P2
HOLE23 H-C236D146P2

Mini-PCI-B NUT (BOT)

HOLE13 H-C236D146P2
HOLE14 H-C236D146P2

2/18 HOLE 13,14 FBBL5008010
change to FBBL5051010

4/17 update HOLE13,14 footprint to H-C236D146P2

Mini-PCI-A NUT (BOT)

HOLE28 *H-C236D126P2
HOLE35 *H-C236D126P2

B:(10/17) update footprint

2/18 HOLE 28.35 FBBL5007010
change to FBBL5050010

5/5 remove HOLE28,35 (HD Decoder)

B:(10/17) update footprint

KB NUT (TOP)

HOLE5 H-C236D146P2
HOLE6 H-C236D146P2

E-SATA NUT (BOT)

4/21 remove Hole31,37

HOLE30 *H-C236D91P2
HOLE38 *H-C236D91P2
HOLE8 *H-C216D91P2
HOLE9 *H-C216D91P2
HOLE22 *H-C216D91P2
HOLE34 *H-C216D91P2
HOLE39 *H-C216D91P2
HOLE16 *H-CT315

A:(9/17) Base ON EMI mail(9/13) Item5

HOLE33 *h-sped110p2
HOLE26 *H-C216D91P2
HOLE40 *H-SPED118P2

A:(9/12) Base ON EMI mail(9/13) Item1

10/24 update footprint

B:(10/17) update footprint

HOLE44 *H-TS315BC295D118P2-8
HOLE43 *H-TSBC315D118P2-8

HOLE42 *H-C276D118P2-8
HOLE41 *H-C335D118P2-8
HOLE19 *H-C335D118P2-8
HOLE4 *H-C335D118P2-8
HOLE7 *H-C335D146P2-8
HOLE12 *H-C335D118P2-8
HOLE10 *H-C335D118P2-8
HOLE11 *H-C315D118P2-8

B:(10/17) update footprint

HOLE36 *H-C335D118P2-8
HOLE27 *H-C335I248D118P2-8
HOLE29 *H-C335D118P2-8
HOLE21 *H-C335D118P2-8
HOLE20 *H-C335D118P2-8

R85 0_8

10/31 EMI request

RAMP:(1/16) Follow BL5, update Hole footprint (13pcs)

NUT P/N Control Table

	UMA sku	EV sku
HOLE15	FBBL5002010	FBBD3021010
HOLE24	FBBL5002010	FBBD3021010
HOLE25	FBBL5002010	FBBD3021010

Stitch CAP

CPU_CORE0

C134 0.01u/16V_4
C133 0.01u/16V_4
C130 0.01u/16V_4
C135 0.01u/16V_4

For fix HyperTransport nets across plane splits

VIN

C768 C769 C770 C771 C772 C773 C774 C775 C776 C777 C778 C779 C780 C781
0.1u/10V_4

EMI CAP.

VIN

C746 C63 C87 C137 C106 C97 C119 C169
0.1u/10V_4

VIN

C529 C270 C472 C758 C755 C756 C31 C30 C74
0.1u/10V_4

+3V

C244 C243 C204 C202 C162 C138 C749 C112 C742
0.1u/10V_4

+3V

C12 C65 C2 C416 C451 C1 C71 C72 C50 C62
0.1u/10V_4

+3V

C450 C454 C224 C480 C409 C460 C455
0.1u/10V_4

+3VPCU

C240 C549
0.1u/10V_4

+3VSUS

C229 C518 C128
*0.1u/10V_4

+5VPCU

C83 C161 C132 C165 C760 C205
0.1u/10V_4

3/3 EMI request add C813,C814

+5V

C464 C745 C51 C3 C759 C59
0.1u/10V_4

+1.5V

C813 C814
0.1u/10V_4

+3VPCU

C164 C547 C122 C748 C32 C33 C75 C34 C70
0.1u/10V_4

+1.8V

C273 C213 C574 C107 C146
0.1u/10V_4

+1.2V

C528 C163 C127 C585 C584
0.1u/10V_4

+5V

C139 C271 C462 C442 C171
0.1u/10V_4

+5VPCU

C16 C757 C45
0.1u/10V_4

+1.8V

C599 C385 C283 C203 C189 C176 C173 C153
0.1u/10V_4

PROJECT : BD3G

Quanta Computer Inc.

Size	Document Number	Rev
	HOLE/EMI CAP/ESD PAD	2A

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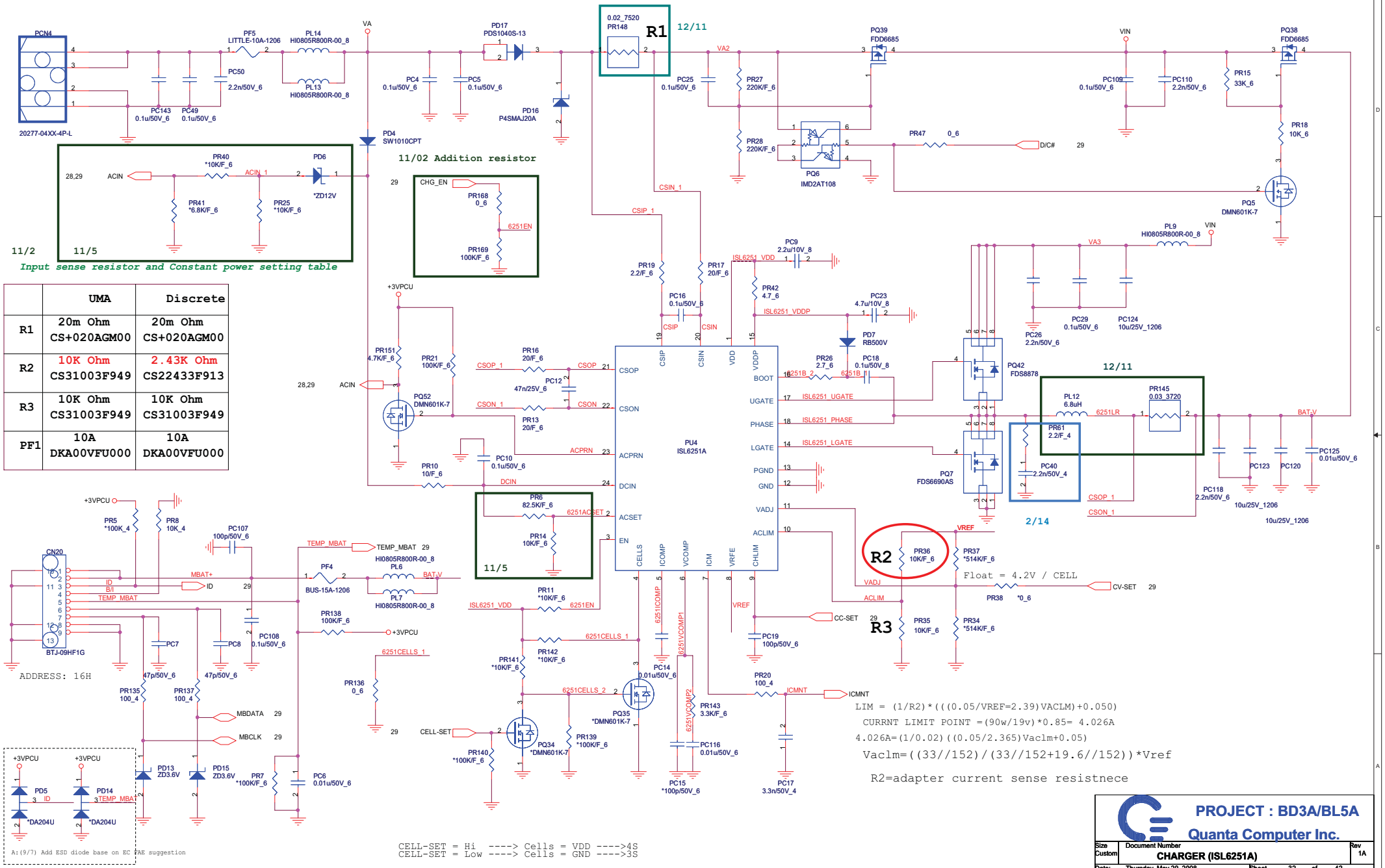
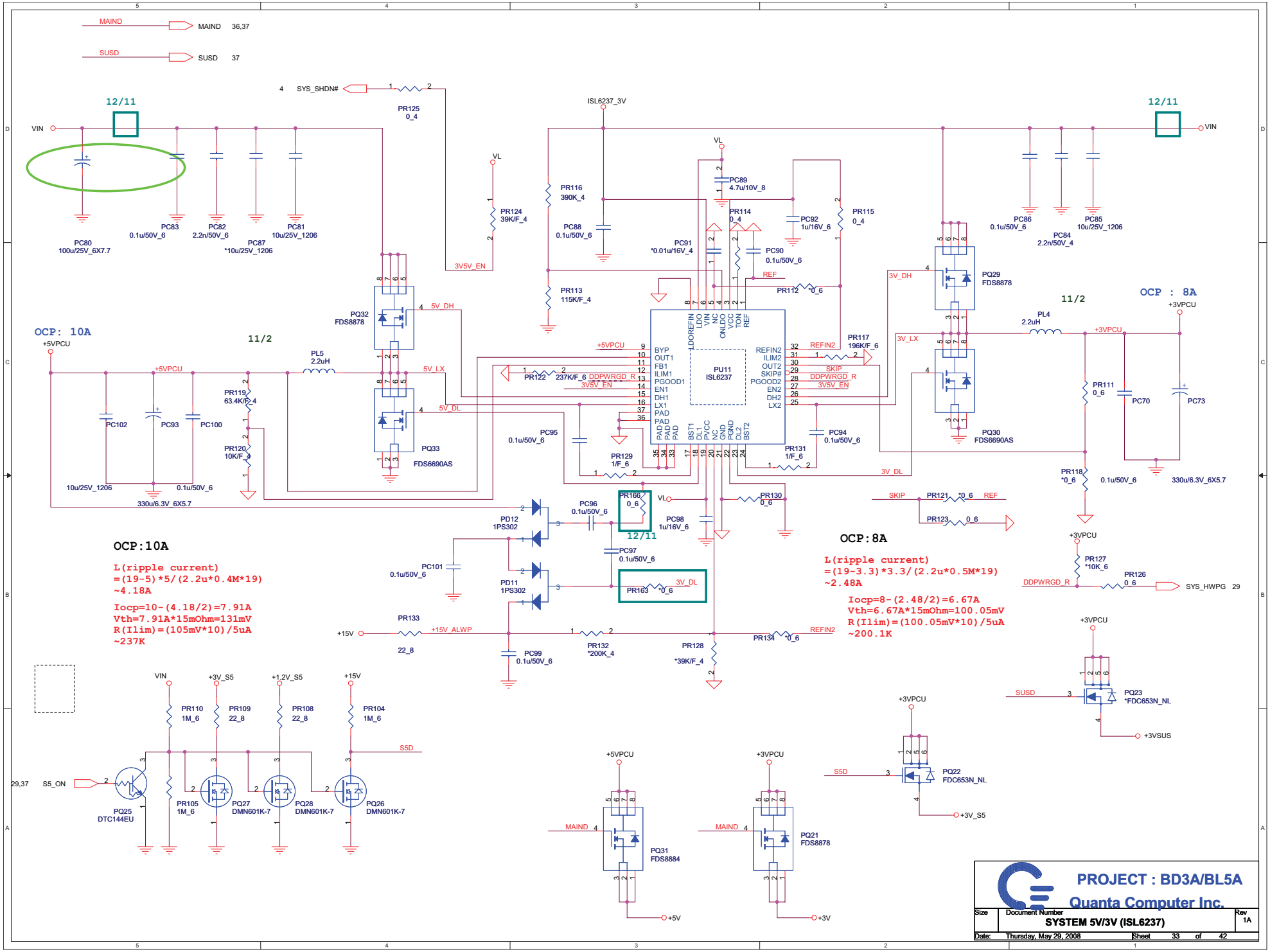


	UMA	Discrete
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	10K Ohm CS31003F949	2.43K Ohm CS22433F913
R3	10K Ohm CS31003F949	10K Ohm CS31003F949
PF1	10A DKA00VFU000	10A DKA00VFU000



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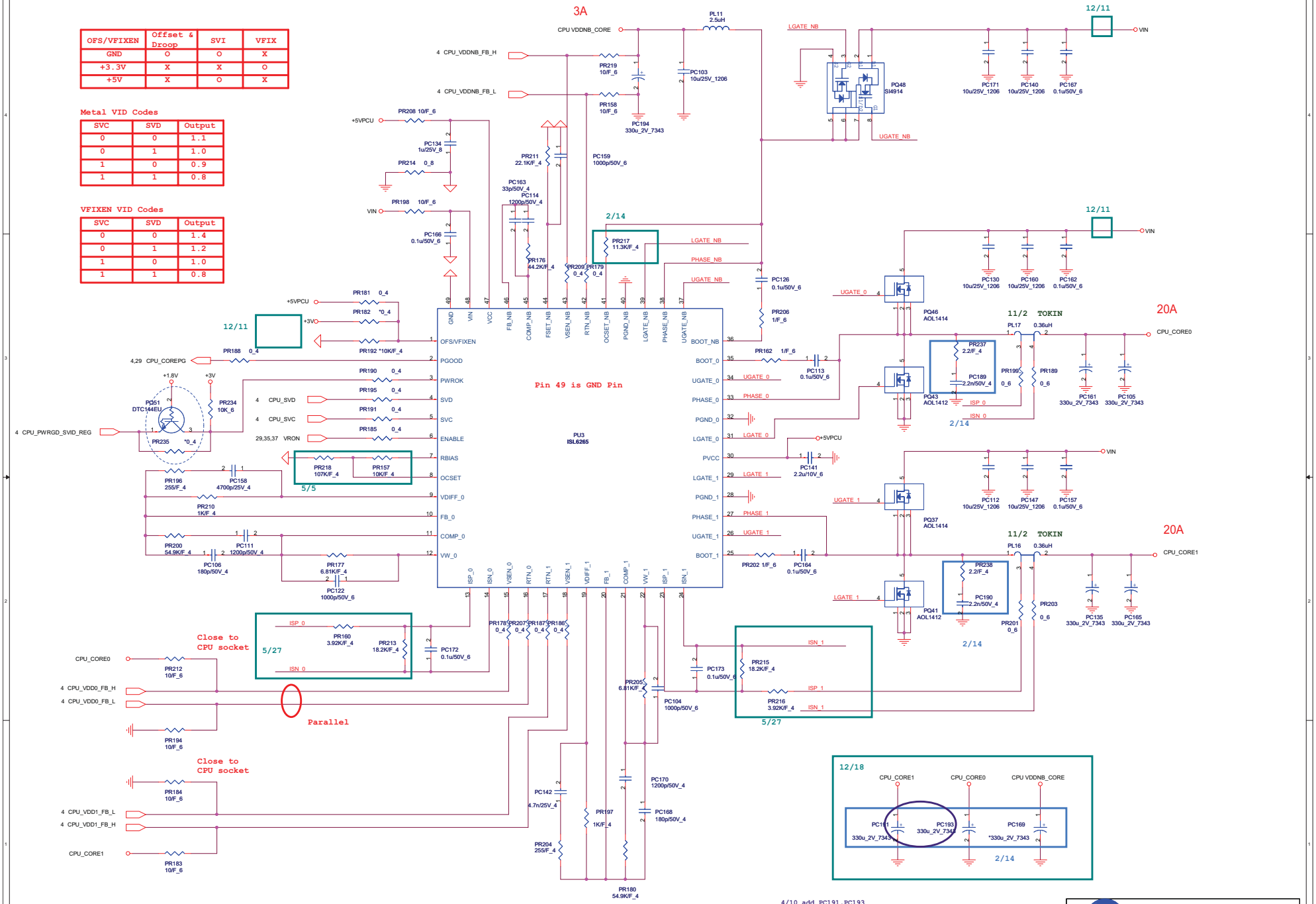
OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



4/10 add PC191,PC193

PROJECT : BD3A/BL5A

Quanta Computer Inc.

Size	Document Number	Rev
C	OZ826 CPU	1A

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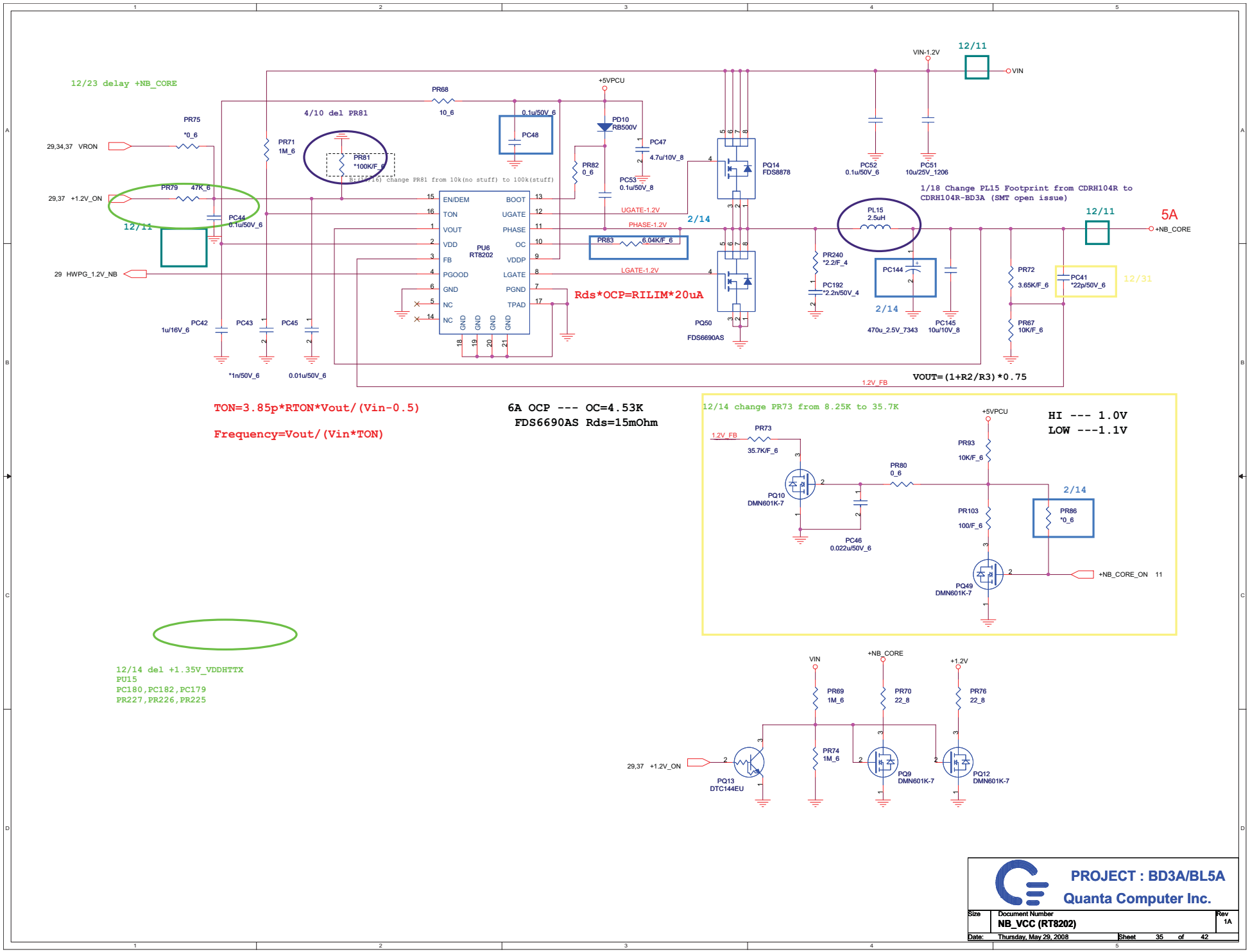

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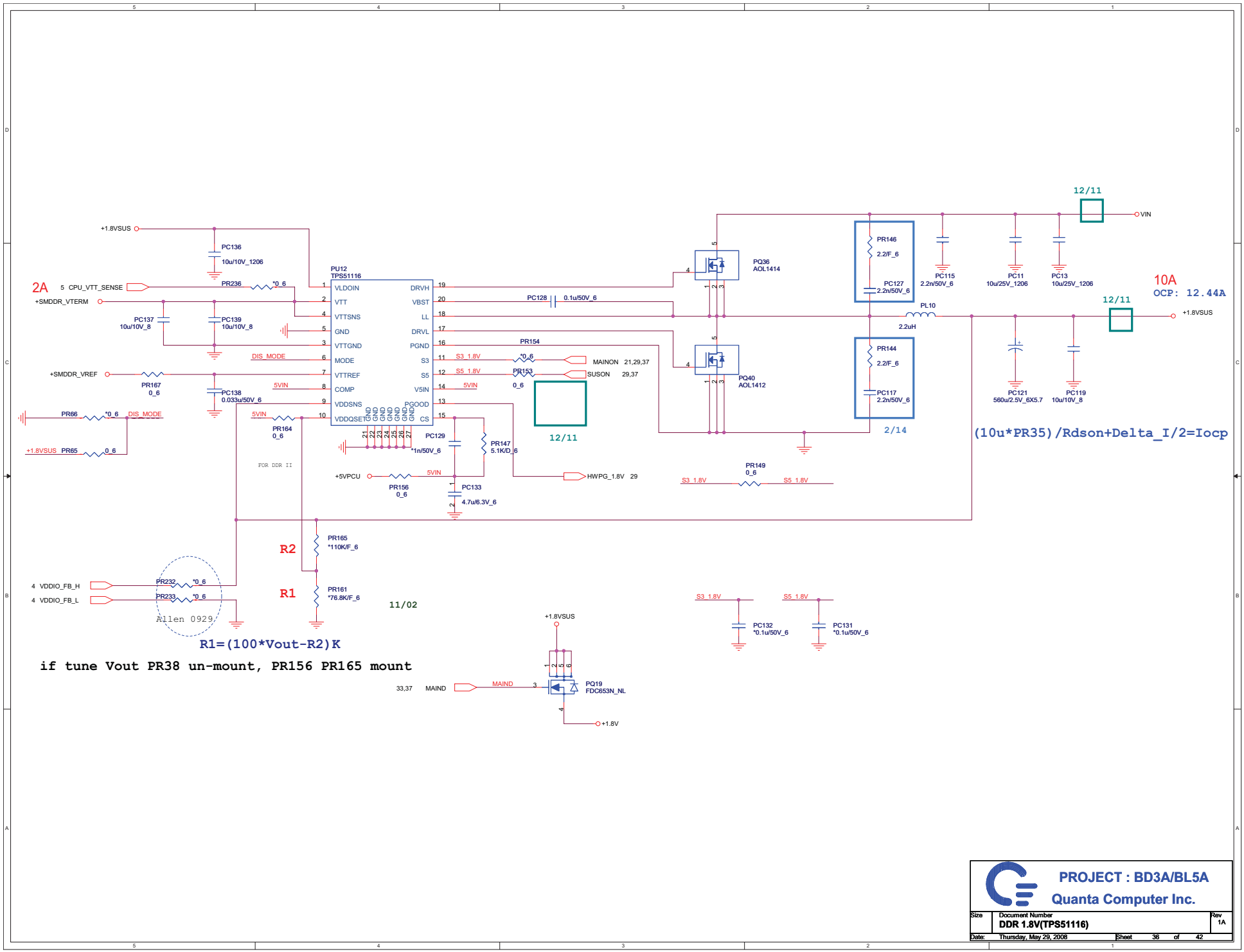

PROJECT : BD3A/BL5A

Quanta Computer Inc.

Size	Document Number	Rev
	DDR 1.8V(TPS51116)	1A

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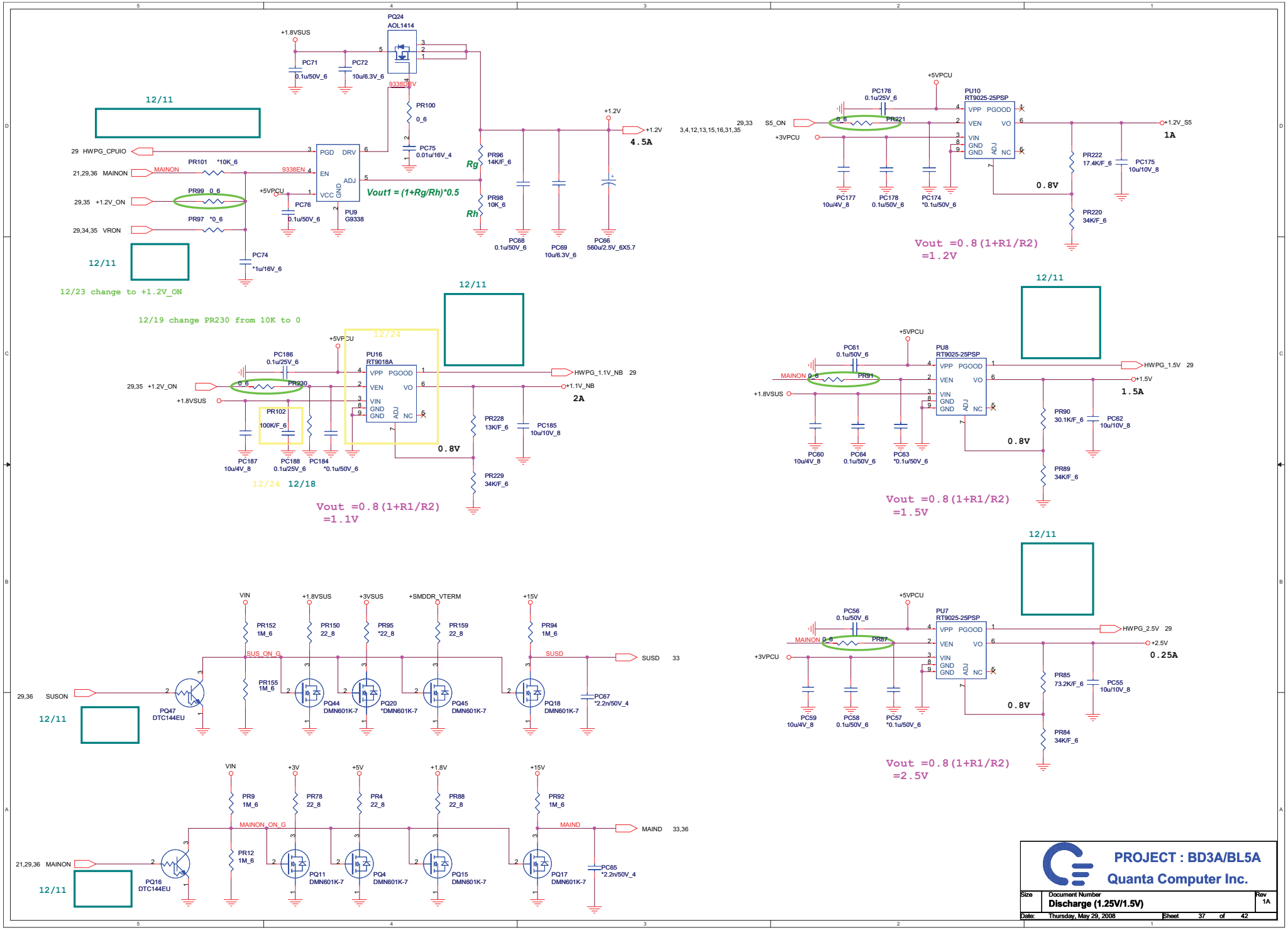

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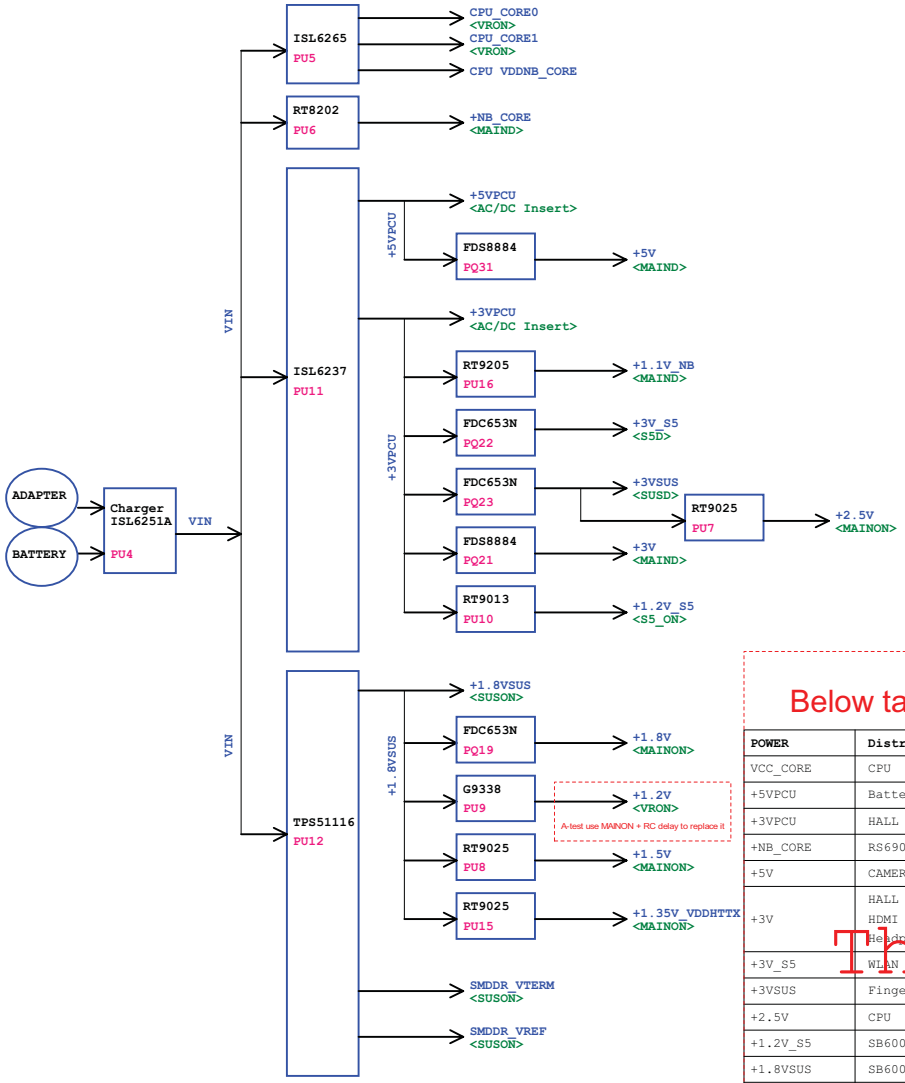

Below table need be modify (waiting other schematic ready)

POWER	Distribution
VCC_CORE	CPU
+5VPCU	Battery LED , Power LED , USB , CIR , RTC
+3VPCU	HALL SENSOR , Battery LED , RF LED , kill SW , Jumper LED , KB , Power Board , EC , ID , SPI Flash , CIR
+NB_CORE	RS690M
+5V	CAMERA , Card Reader LED , ODD/HDD LED , Felica , T/P , T/sensor , CRT , HDMI , SB600 , CPU FAN , MXM , Headphone , EC , INT SPK AMP
+3V	HALL SENSOR , LCD PANEL , LVDS , WLAN , HD Decoder , NEW CARD , KB , KB LED , XD LED , Blue tooth , Touch sensor , Card Reader (OZ129) , ODD/HDD , HDMI , CRT , TVOUT , REQUIRED STRAPS , DEBUG STRAPS , SB600 , RS690M , DDR , CPU Thermal monitor , CPU FAN , CLK , MXM , VR , FM Tuner MDC , Headphone , EC , LAN , Codec(CX 20561)
+3V_S5	WLAN , NEW CARD , SB600 , MXM , LAN
+3VSUS	Finger print , SB600
+2.5V	CPU
+1.2V_S5	SB600
+1.8VSUS	SB600 , DDR , CPU , HDT
+1.8V	SB600 , LCD , LVDS , RS690M
+1.2V	SB600 , RS690M , CPU , WLAN , HD Decoder , NEW CARD
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR
+5V_S5	

The Table NOT READY

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Quanta Computer Inc.

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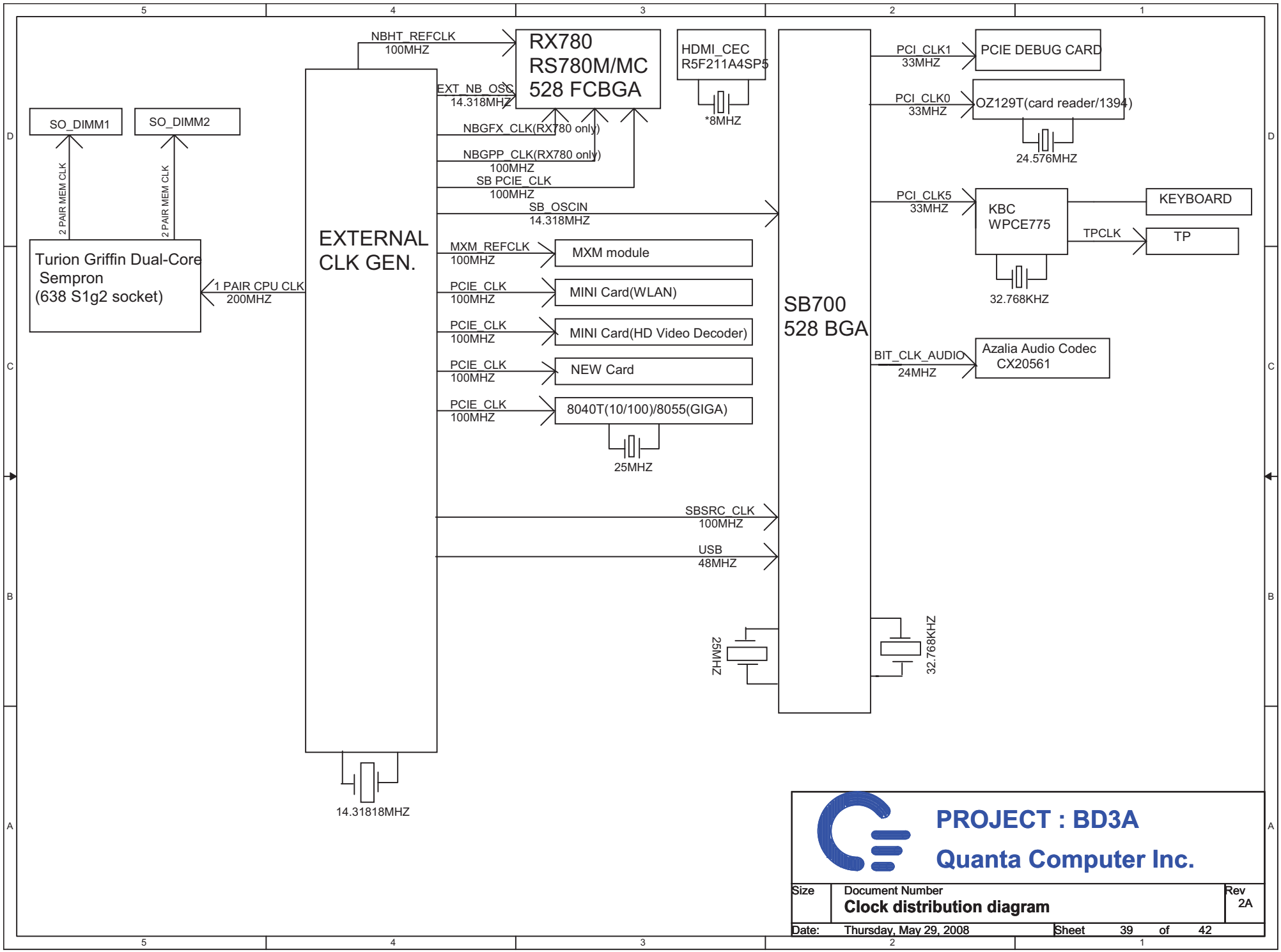

PROJECT : BD3A

Quanta Computer Inc.

Size	Document Number	Rev
	Clock distribution diagram	2A

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Model	REV	DATE	CHANGE LIST	NOTE
BD3G	A1A	2007	FIRST RELEASED : Import BOM ECN	ECN Release
	B2A	20071008	PAGE23:Reverse U42,C761 for VR	Circuit modify
		20071008	PAGE28:Add R667,R668,Q78 for TP_LED	Circuit modify
		20071204	PAGE04:Reverse C762 for AMD engineer CPU use	Circuit modify
		20071204	PAGE19:update CN25 HDMI footprint to HDMI-C12816-119A5-L-19P-V-BL5-1	Circuit modify
		20071204	PAGE15:change BOARD ID3 from GEVENT7 to GPIO48	Circuit modify
		20071204	PAGE14:change BOARD ID PD value from 10K to 1K(R227,R228,R229,R248,R343,R236)	Circuit modify
		20071204	PAGE29:Stuff R510, no-stuff R509 (slove BT module can't bring up issue)	Circuit modify
		20071204	PAGE20: modify display on ckt to avoid flash when into S3/S4/S5 (add Q78,Q80,R670,del Q41,R388)	Circuit modify
		20071207	PAGE19:update CN25 HDMI footprint to HDMI-C12816-119A5-L-19P-H-BD3	Circuit modify
		20071207	PAGE32:update ACIN design	Circuit modify
		20071207	PAGE24:Change R449(0 ohm) to D56(Diode) for leakage issue (3VPCU to 3V_S5)	Circuit modify
		20071207	PAGE23: Slove Audio issue:When plug in-out headphone, headphone has bo sound. 1. Change R652&R651 to C763,C764(10U/6.3V 0603)	Circuit modify Circuit modify Circuit modify
		20071207	PAGE22: Remove D19 to slove Audio issue Switch Mute to Un-mute, sound will delay about 2 seconds.	Circuit modify
		20071207	PAGE14: add D57,D58 to avoid voltage leakage	Circuit modify
		20071207	PAGE30:update LED5,LED6 footprint and PN	Circuit modify
		20071207	PAGE04:add R671~R679 for AMD request	Circuit modify
		20071208	PAGE03:change C223 C225 from 10p to 33p PAGE15:change C257 C258 from 10p to 27p PAGE26:change C380 C381 from 22p to 18p	
		20071210	PAGE25:Change New card footprint to NCARD-13180151-T-26P-L-BL5S	
		20071210	PAGE22:stuff R372 for FM	
		20071211	update power	
		20071212	PAGE29: Change U41(CIR) from BEBK0081D00 to BEBK0081D01	
		20071212	PAGE18: Change CN22(S-Video) from DFMD04FR296(Yellow Color) to DFMD04FR006(Black Color)	
		20071212	PAGE30: Change SW4 P/N from DHL00212F05 to DHL00212F07	
		20071212	PAGE31: Update Hole43 H-TSBC315D118P2, Hole 44 H-TS315BC295D118P2	
		20071212	PAGE29: pull down 100k R680 for ECPWROK	
		20071212	A11 to A12 implemen PAGE12: Del L15 stuff L36 PAGE16: Del R234 stuff R235 PAGE35: Del PU15,PC180,PC182,PC179PR227,PR226,PR225, Change PR73 from 8.25K to 35.7K	
		20071220	PAGE23: Slove GPRS noise 1. stuff R386/R387/C404/C405 to 0.1U 2. Change L44/41 to BK1608LL121	
		20071220	PAGE29: avoid leakage reserve D59/D60 to CLKRUN#/PLTRST#	
		20071221 EMI	PAGE18:add 27p(C790~C793) for TV_Y/G , TV_C/R PAGE21:stuff C568,C548 PAGE22:stuff R399,R379 PAGE23:Change L43/44 to BK1608LL121 PAGE24:add L74,C766,C767,C789,C788 for +2.5V_1.8V_LAN,add L73 for +1.2V_LAN PAGE26:add 0 ohm and 22p for SD/MS CLK , R308~R329 0ohm(CS00002JB38) change to 33ohm(CS03302JB29), remove RN34,RN35, stuff L68,L69 for 1394 PAGE28:del R276,R278 stuff L72 , del R613,R612,R624,R626 stuff L70,L71 , add 0.1u for +5VPCU add 100p for 3ND_MBDATA/CLK PAGE31:stuff all 0.1 cap	
		20071221	update power	
		20071222	PAGE11: stuff R48 2.2K for power play	
		20071222	PAGE24: Per cost down remove LAN eeprom,stuff R381,remove U21,R380,R378	
	C3A	20080102	PAGE14: NEW_DET# change from Geven3# to GPM1#	
		20080117	Update RX781	
		20080117	PAGE13:Modify RTC circuit. R301,R302 change from 8.66k to 2k. R332 change from 4.7K to 6.8K	
		20080117	PAGE13:Change RTC Battery from VARTA (AHL03001441) to MATSUSHITA (AHL03002005)	
		20080117	PAGE19:Change back HDMI connector(CN25) footprint from HDMI-C12816-119A5-L-19P-H-BD3 to HDMI-C12816-119A5-L-19P-H-BL5(SMT open issue)	
		20080117	PAGE20:for engery star add R684 connect to EC pin27	
		20080117	PAGE24:Change CN28 (RJ45 CONN) from DFTJ12FR024 to DFTJ12FR035	
		20080117	PAGE27:Change CN32(2nd SATA CONN) from DFHS22FR064 to DFHS22FR094	
		20080117	PAGE27:Change CN32 footprint from SATA-127043FR022XX27ZR-22P-L-H to SATA-127043FR022G285ZR-22P-L	
		20080117	PAGE30:Remove CN10 (Keyboard CONN)	
		20080117	PAGE21:Remove R492,R517, Short CN27/Pin189,190 to VIN directly.	
		20080118	PAGE28:Change L72 from CX216900002 to CX163210007(BT circuit)	
		20080118	PAGE08:Change CN19 footprint from DDR-C-292564-200P to DDR-C-292564-200P-BD3A (SMT open issue)	
		20080118	PAGE08:Change CN23 footprint from DDR-C-1734071-200P to DDR-C-1734071-200P-BD3A (SMT open issue)	
		20080118	PAGE30:Change SW4 footprint from SW-NSS506-212F-CCCD1T-3P to SW-NSS506-212F-CCCD1T-3P-BD3A (SMT open issue)	
		20080118	PAGE23:Change CN43 footprint from MDC-1-179373-2-12P-RUV to MDC-1-179373-2-12P-RUV-BD3A (SMT open issue)	
		20080118	PAGE35:Change PL15 Footprint from CDRH104R to CDRH104R-BD3A (SMT open issue)	
		20080118	PAGE22:Add R685 for VISTA WHQL circuit	
		20080118	PAGE24: Change RJ45 footprint from LAN-100073FR012G101ZL-12P to rj45-c100s7-10806-l-12P	
		20080118	PAGE31:HOLE 17,18.23 FBBL5004010 change to FBBL5002010	

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Quanta Computer Inc.

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Model	REV	DATE	CHANGE LIST	NOTE
BD3G	C3A	20080118	PAGE30:change footprint from 88171-3400L-34P-L to 91504-340N-34P-L	Circuit modify
		20080118	PAGE30:LED7,8 change footprint from LED12-21SYGC-TR8 to LED27-21-BHC-ZL1M2TY-3C	Circuit modify
		20080118	PAGE30:change p/n LED7 BEBL0074Z04 (WIMAX),LED8 BE0R0053Z00 (WLAN & BT)	Circuit modify
		20080131	PAGE31:update HOLE42,41,19,4,7,12,10,11,36,27,29,21,20,43,44	Circuit modify
		20080131	voltage leakage issue	Circuit modify
			PAGE04:modify CPU_PROCHOT# ckt (add R687, no stuff R686,R425), CPU_LDT_REQ#_CPU ,CPU_PWRGD connect to +1.8V	Circuit modify
			PAGE11:remove Q5,Q3,R83,R80,R97,stuff R88,R77	Circuit modify
			PAGE14:BOARD_ID4 change from GPIO66 to GPIO3	Circuit modify
		20080131	PAGE14:NEW CARD hot plug issue ,NEW_DET# change from GEVEN5# to GPM1# (SB700 A12 Errata)	Circuit modify
		20080131	PAGE19: DEL L56,L57,L58,L59,R465,R474,R493,R495,R486,R488,R478,R483,C226,C227 for HDMI circuit	Circuit modify
		20080131	PAGE25: add +3V to CN21 pin39,41	Circuit modify
		20080131	PAGE18: Change L4,L5,L6 to CX8BA470003 to meet CRT spec	Circuit modify
		20080131	PAGE19: Change U11 from ARBL5SV0000 to ARBL5MV0000	Circuit modify
		20080131	PAGE26:According to customer request, we can't stuff C782 (22pF) in SD/MS_CLK.	Circuit modify
		20080131	PAGE25: Change R573 from 28.7K to 0 ohm, Remove C628 for NEW card some device can't work normal	Circuit modify
		20080131	PAGE14: Change R350 from 1K to 0 ohm (Slove VCCRTC can't reach 0V when clear CMOS.)	Circuit modify
		20080131	PAGE26: Change CN33(5 in 1 card CONN) P/N from DFHS38FR003 to DFHS38FR005	Circuit modify
		20080131	PAGE27: Change CN34 (1st SATA) P/N from DFHS22FR063 to DFHS22FR082	Circuit modify
		20080131	PAGE27: Change CN32 (2nd SATA) P/N from DFHS22FR094 to DFHS22FR083	Circuit modify
		20080131	PAGE20: Change CN5 (I-MIC)P/N from DFHD02MR003 to DFHD02MR016	Circuit modify
		20080131	PAGE22: Change CN39(I-MIC CONN) P/N from DFHD02MR003 to DFHD02MR016	Circuit modify
		20080131	PAGE22: Change CN17(SPK CONN) P/N from DFHD04MR012 to DFHD04MR021	Circuit modify
		20080131	PAGE28: Change CN16(USB-FFC CONN) P/N from DFHD10MR011 to DFHD10MR008	Circuit modify
		20080131	PAGE28: Change CN13(FP CONN) P/N from DFHD04MR012 to DFHD04MR021	Circuit modify
		20080131	PAGE28: Change CN14(BT CONN) P/N from DFHD10MR011 to DFHD10MR008	Circuit modify
		20080201	PAGE22: Change INT-SPK AMP GAIN VALUE. Change R623,R625 from 9.1k to 5.1k 1%,Change R620,R621 from 10k to 16k 1%	Circuit modify
		20080201	PAGE30: Change R404,R405 from CS13902JB14 (390 ohm) to CS13302JB21(330 ohm)	Circuit modify
		20080201	RS780M A13 Errata	Circuit modify
			PAGE11:change R103 from 150 to 140 CS11402FB01	Circuit modify
			PAGE18:RS780M A13 R8 ---> 140 CS11402FB19,MXM R8 ---> 150 CS11502FB21	Circuit modify
		20080201	PAGE19: change HDMI SCL/SDA pull res R168,R171,R163,R170 to 4.7K ,change R1,R2 to 6.8K	Circuit modify
		20080201	PAGE20: change Panel SDA/SDC pull res R412,R410 from 39K to 4.7K	Circuit modify
		20080204	ESD solution	Circuit modify
			PAGE23: add Varistor D63,D64,D65 on SPDIF_OUT/HP_JD/+3V_SPD	Circuit modify
			PAGE28: reserve D66 for CN36 , reserve D68,D69,D70 for FP , stuff D71,D72,D73 for BT	Circuit modify
			PAGE20:reserve D74,D75,D76 for CCD ,stuff D87 for LID switch	Circuit modify
			PAGE27:del R270,R597 , connect to +5V directly ,reserve D77~D81 for CN34(1ND HDD) ,reserve D82~D86 for CN32(2ND HDD) ,reserve D67 for CN31	Circuit modify
			PAGE26:reserve D88~D91 for 1394	Circuit modify
			PAGE04:reserve D92,D93 for FAN , reserve C795,C796 change R122 to 0 0603	Circuit modify
			PAGE13,19,21,25:reserve C797~800 for PLTRST#	Circuit modify
		20080204	PAGE04: pull up R691 CPU_BDREQ# to avoid noise cause system shut down	Circuit modify
		20080205	PAGE23:Change R714,R715 from 10uF to 0 ohm (Audio HP circuit)	Circuit modify
		20080210	PAGE18,29: DEL D4,D5 footprint and DEL CRT_SENSE# net, No stuff R218	Circuit modify
		20080210	PAGE28: DEL C42, Add D94 for CN8/Pin2 (ESD issue) - default no stuff	Circuit modify
		20080210	PAGE28: Change L70,L71 from CX216900002 to CX163210007	Circuit modify
		20080210	PAGE28: Stuff L64,L65 to CX163210007	Circuit modify
		20080213	PAGE27: Add ESATA re-driver IC	Circuit modify
		20080213	PAGE25: Change the footprint of R33 and R330 from 1206 to 0805	Circuit modify
		20080213	EMI solution	Circuit modify
			PAGE18: C4,C7,C10,C5,C8,C11 change from 10p to 6.8p	Circuit modify
			PAGE28: stuff C391,C701, C559 ,C228,C465,C618,C41,C43, C618,C794,C809,C810	Circuit modify
			PAGE20: stuff C427~C432	Circuit modify
			PAGE30: stuff C39,C346	Circuit modify
			PAGE29: stuff C577,C578,C560	Circuit modify
			PAGE12: stuff C804~C807 for +NB_CORE	Circuit modify
			PAGE25: stuff C40,C36,C54,C58,C289,C352,C319,C272 for WL	Circuit modify
			PAGE19: stuff C808 for HDMI	Circuit modify
			PAGE15: stuff C375,C366 for SB HW MONITOR	Circuit modify
			PAGE22: stuff R627	Circuit modify
			PAGE26: change R683 from 0 to 33 ohm	Circuit modify
		20080214	UPDATE POWER	Circuit modify
		20080215	PAGE28: CN42 co-layout with CN16	Circuit modify
		20080215	PAGE31: Remove R98,R145,R118 Hole15,17,18	Circuit modify
		20080215	PAGE28: Change L70,L71 from CX216900002 to CX201290009	Circuit modify
		20080218	PAGE31: HOLE 15,24.25 FBBD3017010 change to FBBD3021010	Circuit modify
		20080218	PAGE31: HOLE 28.35 FBBL5007010 change to FBBL5050010 , HOLE 13,14 FBBL5008010 change to FBBL5051010	

PROJECT : BD3G

Quanta Computer Inc.

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	Change List02	3C

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Model	REV	DATE	CHANGE LIST	NOTE
BD3G	C3A	20080218	PAGE04: G781 reverse R718 0 ohm for Griffin CPU	Circuit modify
		20080219	PAGE04: change G781 to G786P81U	Circuit modify
		20080220	PAGE27:1.change C801,C82 from 0.01u to 4.7n, 2.RX add C811,C812 4.7n	Circuit modify
		20080222	PAGE15:change SATA ODD from port3 to port4 (solve ODD post detect fail)	Circuit modify
		20080226	PAGE27:change ESATA conn usb-2006109-11p,update p/n to DFHS11FR021	Circuit modify
		20080227	update power include EMI	Circuit modify
		20080229	del co-layout parts	Circuit modify
			RN34,RN35,R608,R607,R572,R569	Circuit modify
		20080303	PAGE14: del Mini card USB10,Felica USB5 , change BT to port5 , ESATA to port 10	Circuit modify
		20080303	PAGE25: MINI PCI II no need USB , change USB10 to ESATA .and del R169,R188	Circuit modify
		20080303	PAGE28: no Felica request , remove USB del R178,R179,remove Q57,C476,R450,Q56	Circuit modify
		20080303	PAGE31: EMI request add C813,C814	Circuit modify
		20080410	PAGE17: change R150 to R152 for power sequence	Circuit modify
		20080410	PAGE26: add D88~D91 for 1394 ESD	Circuit modify
		20080410	PAGE27: change ESATA conn usb-2006109-11p update p/n to DFHS11FR023	Circuit modify
		20080410	PAGE27: add D67,D49,D50 for ESATA USB ESD	Circuit modify
		20080410	PAGE28: add D51,D52, D66 for USB0	Circuit modify
		20080410	PAGE34: add PC191,PC193 for CPU core	Circuit modify
		20080410	PAGE35: del PR81	Circuit modify
		20080410	PAGE27: remove Flash card ckt	Circuit modify
		20080416	PAGE13: change RTC pad location to G1	Circuit modify
		20080416	PAGE14: pull up USB_OC5# R719	Circuit modify
		20080416	PAGE18: update footprint to sv-030018fr004s100fr-4p-h-bl5m	Circuit modify
		20080416	PAGE23: update footpritnt to knob-xre094-3p-bl5m	Circuit modify
		20080416	PAGE28: remove CN42 not co-layout with CN16	Circuit modify
		20080416	PAGE31: update HOLE13,14 footprint to H-C236D146P2	Circuit modify
		20080417	PAGE27: remove D77~D81 for CN34 , change to U44 CM1213-04SO(AL001213001) ,remove D82~D86 for CN32 , change to U45 CM1213-04SO	Circuit modify
		20080418	PAGE28: Change L72 from CX163210007(BT circuit) to CX201290009	Circuit modify
		20080421	PAGE31: remove Hole31,37	Circuit modify
		20080421	no stuff +3VSUS component	Circuit modify
			PAGE31: no stuff C229,C518,C128	Circuit modify
			PAGE33: no stuff PQ23	Circuit modify
			PAGE37: no stuff PR95,PQ20	Circuit modify
		20080424	PAGE16: IDE/FLASH not use ,remove C287,C288,C297,C293,C294	Circuit modify
		20080424	PAGE16: internal clk not use ,remove C332,C330,C327,C331, change L28 to 0 ohm	Circuit modify
		20080424	To meet ESATA SI	Circuit modify
			PAGE27: change R706 from 0 ohm to 330 , stuff R692,R693,R694	Circuit modify
				Circuit modify
		20080424	PAGE16: remove C762 to meet PWRGD timing spec	Circuit modify
		20080424	PAGE9: stuff R480,R479 to meet AMD spec	Circuit modify
		20080424	PAGE17: stuff C765 10nf to meet power sequence	Circuit modify
		20080505	PAGE34: intersil recommand to set OCP to 30A	Circuit modify
			Change PR218 from CS32052FB21 to CS41072FB11,Change PR157 from CS41002FB28 to CS31002FB26,Change PR160 PR216 from	Circuit modify
			CS31622FB27 to CS23652FB08	Circuit modify
		20080505	PAGE22: Change CN17 from DFHD04MR021 to DFHD04MRA75	Circuit modify
		20080505	PAGE27: update re-driver footprint to tqfn36-5x6-5-37p-0_75h-te1m	Circuit modify
		20080505	PAGE20: reserve R720,R721 for cost down	Circuit modify
		20080505	PAGE27: add C816 0.1u to U44 +5V for ESD , add C818 0.1u to U45 +5V for ESD	Circuit modify
		20080505	PAGE25: remove CN30 second PCIE (HD Decoder)	Circuit modify
		20080505	PAGE31: remove HOLE28,35 (HD Decoder)	Circuit modify
		20080507	PAGE20: stuff D74,D75,D76 for CCD	Circuit modify
		20080508	PAGE20: reserve CM1293 U46,C819 for CCD ESD protect	Circuit modify
		20080508	PAGE28: stuff D68,D69,D70 for FP	Circuit modify
		20080508	PAGE30: stuff D53 for RF_LED ESD	Circuit modify
		20080509	PAGE26: 5/9 for card reader MS DUO adapter short issue	Circuit modify
			reserve R723,724,722 ,Q82,Q81,Q83,Q84	Circuit modify
		20080513	PAGE4: follow AMD design guide 1.03 stuff R675	Circuit modify
		20080527	PAGE26: some 1394 device can't boot normal	Circuit modify
			change L38 to BK1608HS220_6	Circuit modify
		20080527	PAGE34: CPU core adj	Circuit modify
			1.PR160,PR216 change to 3.92K/F_4	Circuit modify
			2.PR213,PR215 change to 18.2K/F_4	Circuit modify
		20080527	PAGE33: solve system hang up , when plug adp quickly	Circuit modify
			change PR113 from 150K_4 to 115K/F_4	Circuit modify
		20080527	PAGE33: avoid right side USB voltage drop	Circuit modify
			change PR119 to 63.4K , PR120 to 10K	Circuit modify
		20080528	PAGE12: del C805,C807	
		20080529	PAGE27: change ESATA conn p/n to DFHS11FR027	

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