BU3 Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND1
- LAYER 3 : IN1
- LAYER 4 : GND
- LAYER 5 : VCC
- LAYER 6 : IN2
- LAYER 7 : GND2
- LAYER 8 : BOT

PENRYN-SFF
Micro-FCBGA956/10W
FSB P3,4

FSB(667/800/1066MHZ)

CANTIGA-SFF
NB
P5,6,7,8,9,10,11
FSB
DMI
PCI-E
DDR SYSTEM MEMORY
Graphics Interfaces

DDRIII-SODIMM1
DDRIII-SODIMM2
P16
Dual Channel DDR III
800/1066 MHZ

INT_LVDS → USB-3 → LCD/CCD Con. P17
INT_CRT → CRT Con. P17
PCI-Ex16 → USB-5 → HDMI/USB Con. P18

DMI(x2/x4)

Intel I/O Controller Hub 9
(ICH9M-SFF)
SB
P12, 13, 14, 15
SATA
DMI
PCI-E
SATA
USB
RTC
IHDA
LPC

Main SATA - HDD P22 — SATA 0
11.6" SATA HDD P22
SATA - ODD P22 — SATA 1
Bluetooth Con. P21 — USB-2 — USB 2.0 (Port0~9)
USB SW P18 — USB-9

PCI-Express
PCIE-3 → USB-6 → 3G P20 → USB-7 → Sim Con. P20
PCIE-6 → USB-10 → WiFi or WiMAX P20

Atheros
10/100 Lan
P23
PCIE-5
Azalia

BATTERY
P12

LPC

LAN CON.&Audio&Card Reader&USB*2/B P26
- LAN Con.
- USB-0 / USB-1 → USB*2 Con.
- Audio Codec (Port-B, Port-A) → MIC JACK, HP/SPDIF, SPK Con.
- Card Reader → USB-4

EC P22
- FAN P3
- K/B Con. P21
- SPI Flash P22
- TP/LED/Hall Sensor Con. P19
- G-Sensor P19
- P21
- Kill SW P21
- Power /B Con. P21

CK505 P2

POWER SYSTEM
- ISL88731 P24
- ISL6237 P25
- RT8152B P26
- TPS51116REGR P27
- UP6111AQDD P28
- RT9205 P29
- ISL6263A P30

VCC_CORE

+1.8V

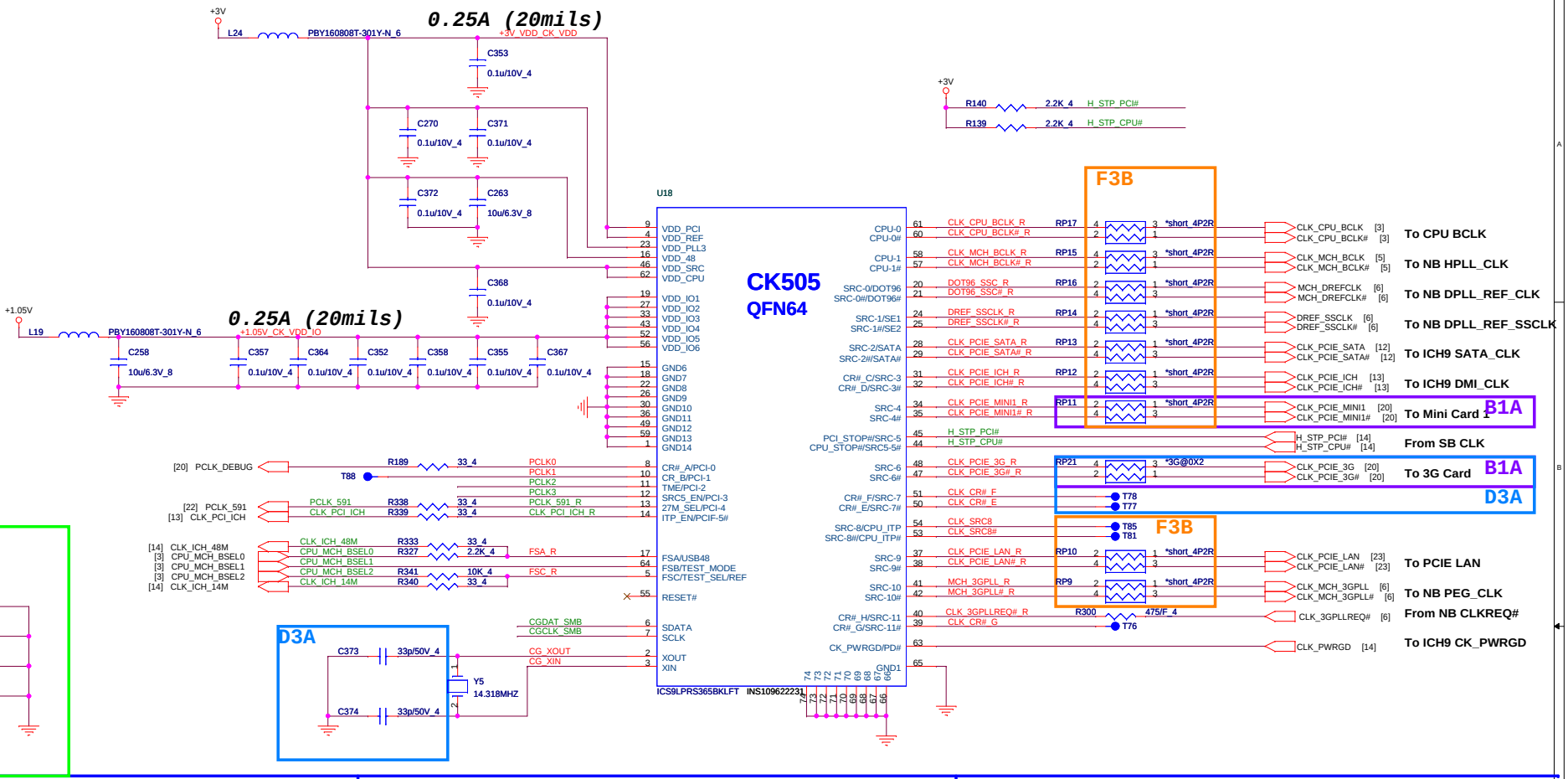
+1.05V

+1.5VSUS
+1.5V

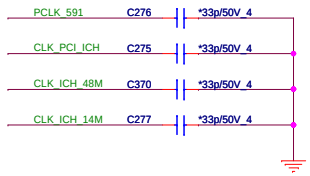
+3VPCU
+3V_S5
+3VSUS
+3V
+5VPCU
+5V
+SMDDR_VTERM
+SMDDR_VREF

Quanta Computer Inc.
PROJECT : BU3
Size | Document Number: Block Diagram | Rev: D3B
Date: Monday, August 10, 2009 | Sheet 1 of 34

CLOCK GEN

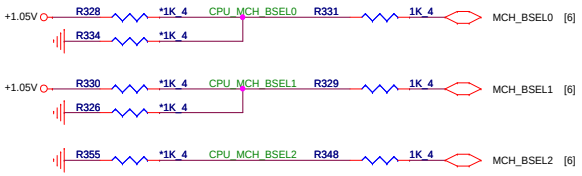


EMI RESERVE



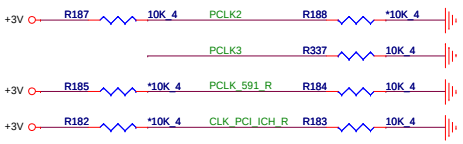
BSEL Frequency Select Table

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

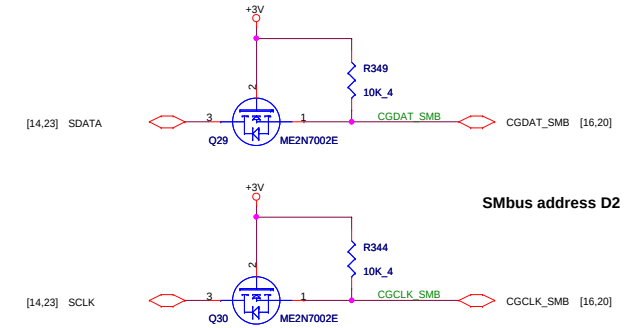


Clock Gen Strap

	SLG8SP513	PULL HIGH	PULL DOWN
PIN11	PCI2/TME	NO OVERCLOCKING (default)	NORMAL RUN
PIN12	PCI-3	PIN44/45 IS SRC5	PIN44/45 IS PCI_STOP/CPU_STOP (default)
PIN13	PCI-4/27M_SEL	PIN 24/25 IS 27MHz	PIN 21/20 IS SRC/DOT (default)
PIN14	PCIF-5/ITP_EN	PIN 53/54 IS CPUITP	PIN 53/54 IS SRC (default)



Clock Gen I2C



PROJECT : BU3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GEN_9LPRS365BKLFT	D3B
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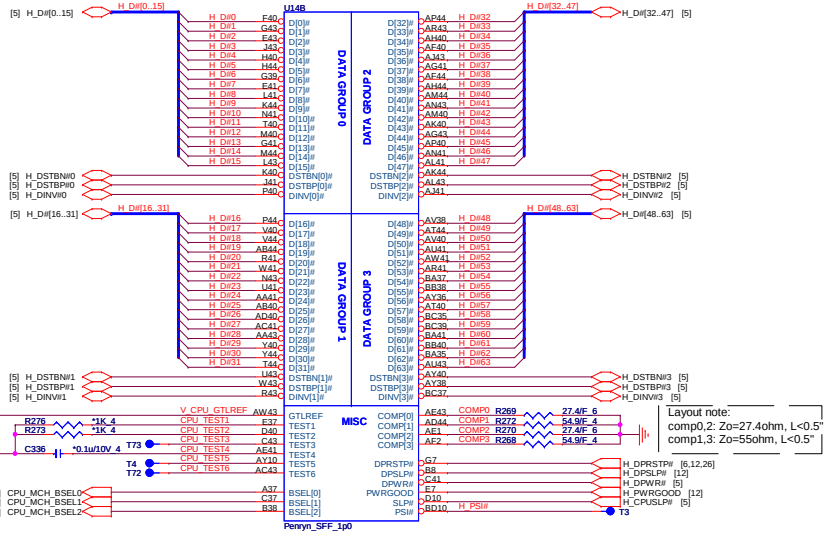
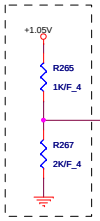
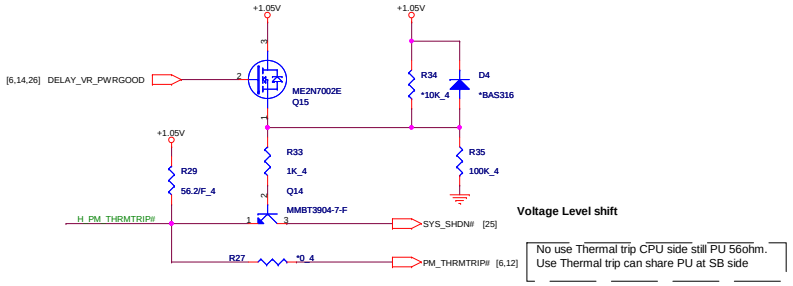
NB7

CPU

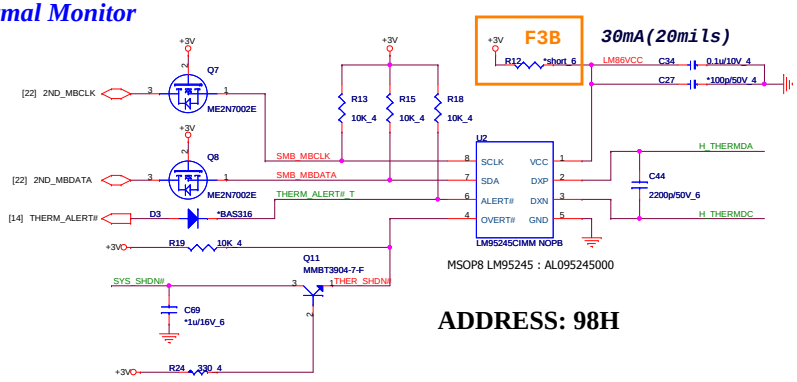




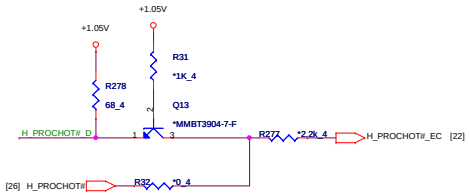
Thermal Trip



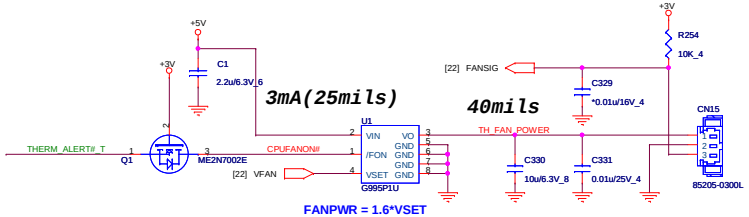
CPU Thermal Monitor



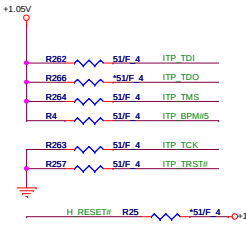
Processor Hot



CPU FAN CTRL



XDP



N87	PROJECT : BU3 Quanta Computer Inc.	
Size: Custom	Document Number: Penryn (HOST BUS)	Rev: D3B
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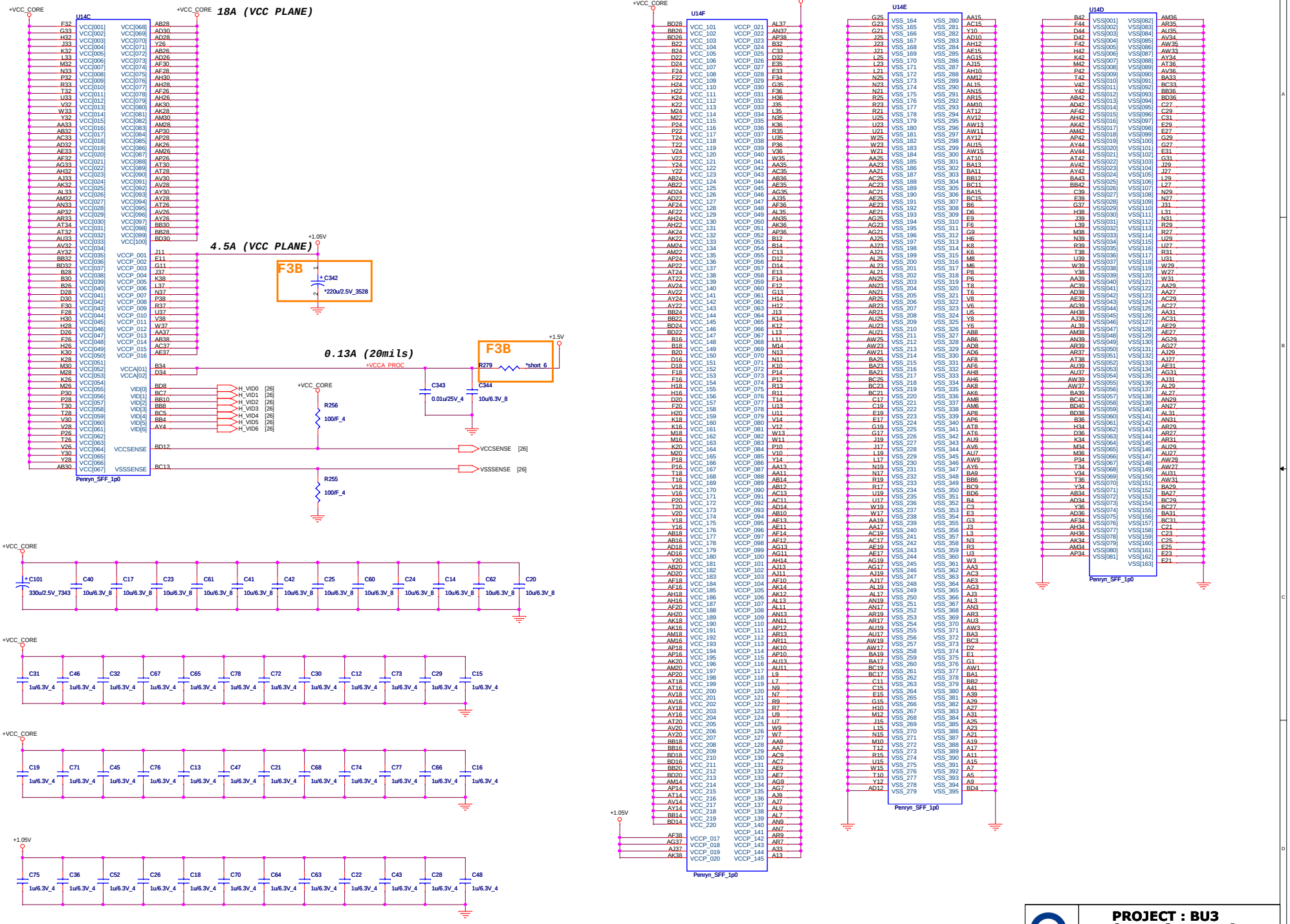
CPU



PROJECT : BU3		
Quanta Computer Inc.		
NB7	Size: Custom	Document Number: Penryn (POWER/NC)
	Rev: D3B	
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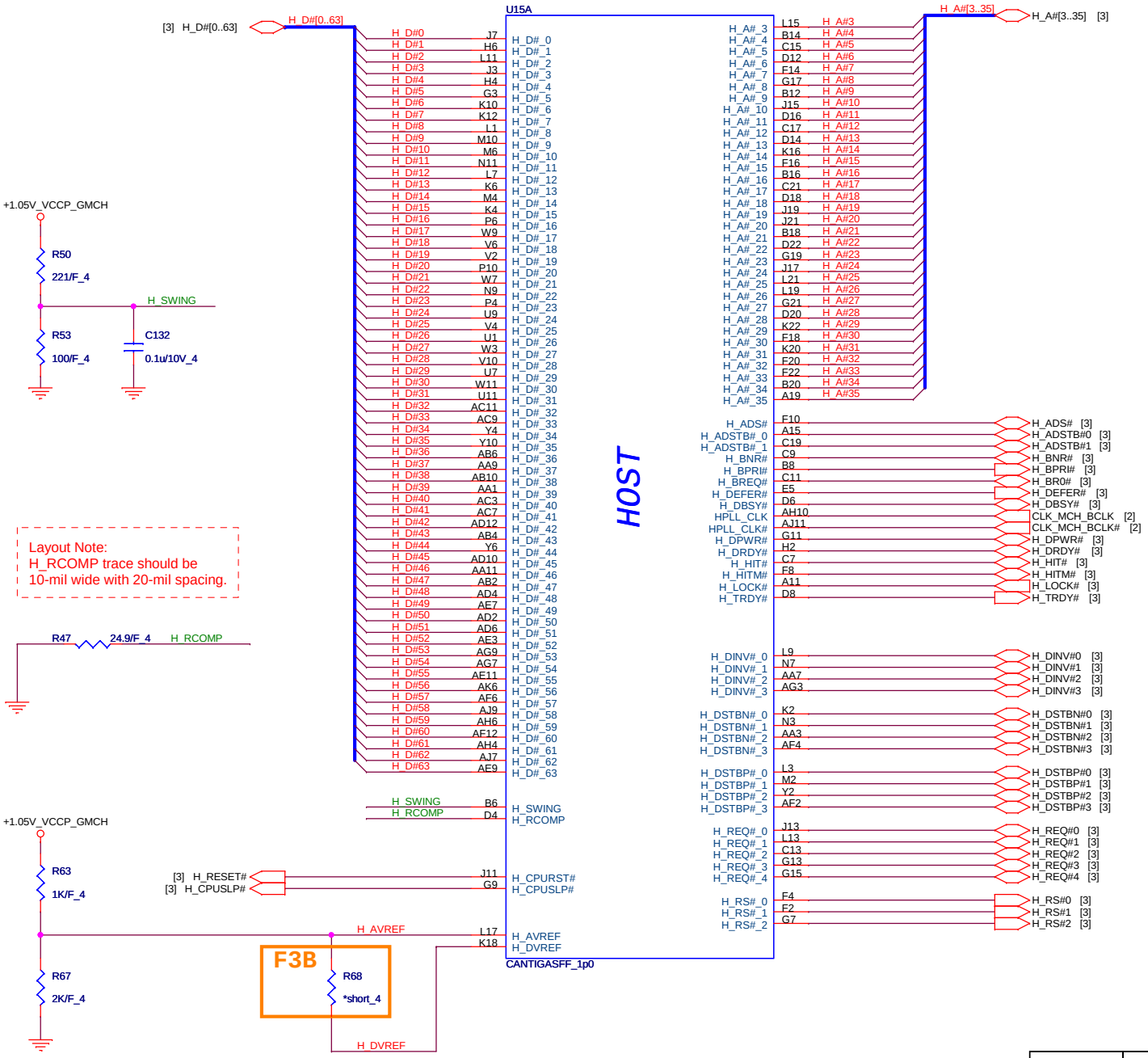
GS45



PROJECT : BU3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	GANTIGA HOST(1/6)	D3B

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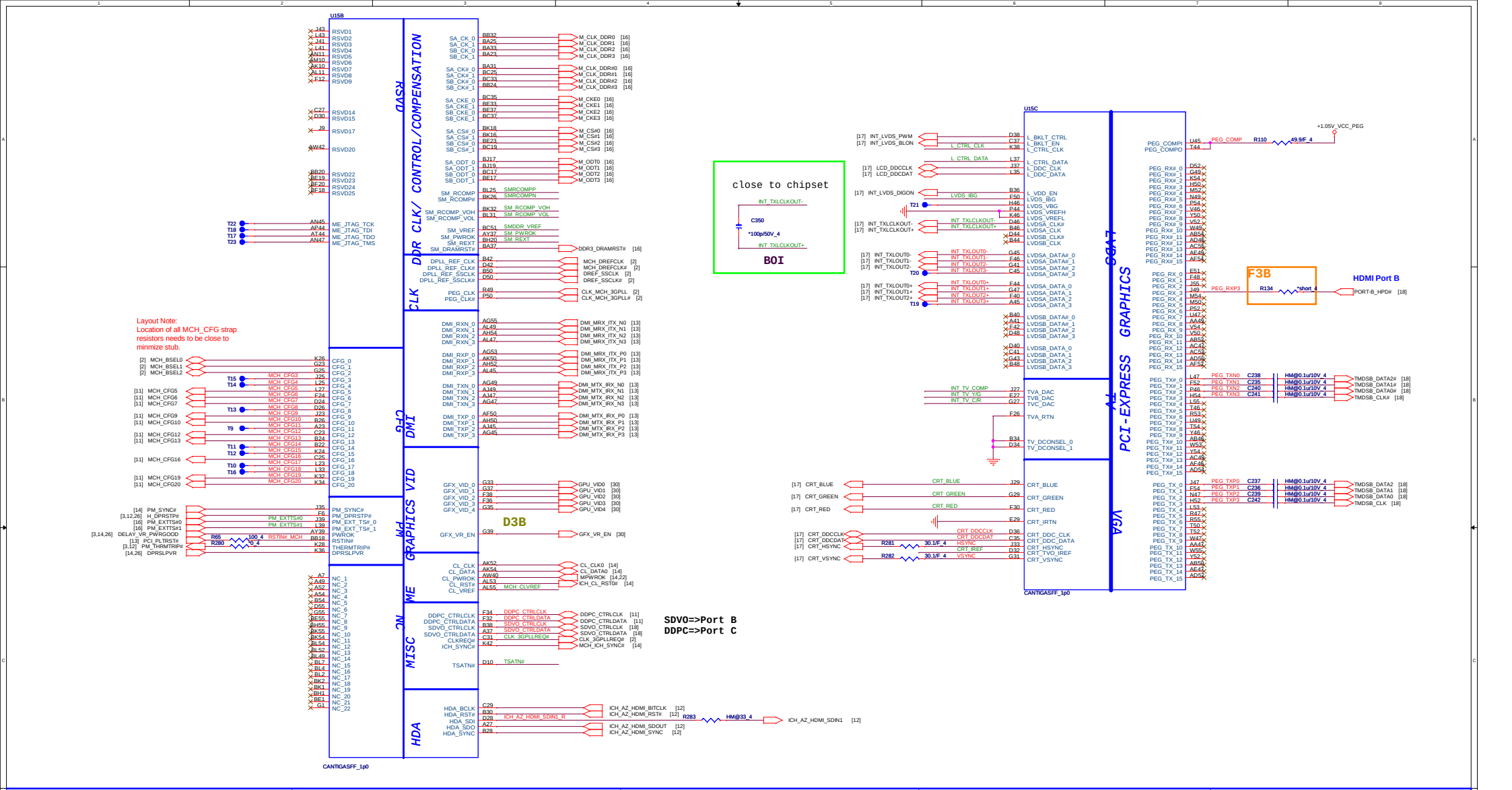
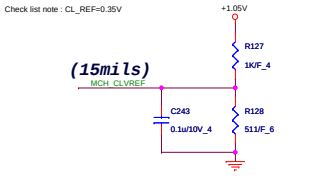
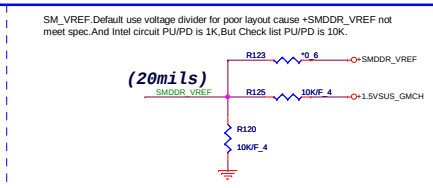
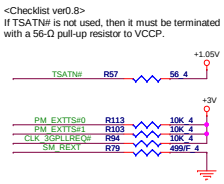
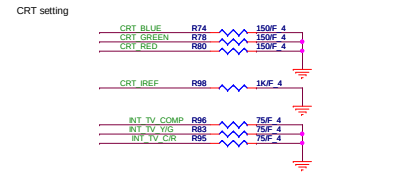
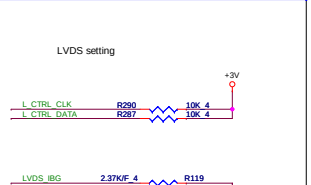

U15B
RSVD
CLK
DDR CLK/ CONTROL/COMPENSATION
CFG
DMI
GRAPHICS VID
PM
ME
MISC
HDA
NC
Layout Note:
Location of all MCH_CFG strap
resistors needs to be close to
minmize stub.
D3B
CANTIGASFF_1p0
U15C
close to chipset
B0I
SDVO=>Port B
DDPC=>Port C
F3B
HDMI Port B
PORT-B_HPD#
PCI-EXPRESS GRAPHICS
TVDC
TV
VGA
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_IRTN
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_TVO_IREF
CRT_VSYNC
CANTIGASFF_1p0

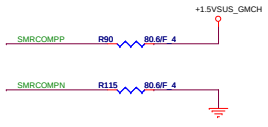

Check list note : CL_REF=0.35V
+1.05V
(15mils)
MCH_CLVREF
R127
1K/F_4
C243
0.1u/10V_4
R128
511/F_6

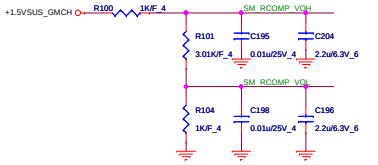

SM_VREF.Default use voltage divider for poor layout cause +SMDDR_VREF not
meet spec.And Intel circuit PU/PD is 1K,But Check list PU/PD is 10K.
(20mils)
SMDDR_VREF
R123
*0_6
+SMDDR_VREF
R125
10K/F_4
+1.5VSUS_GMCH
R120
10K/F_4

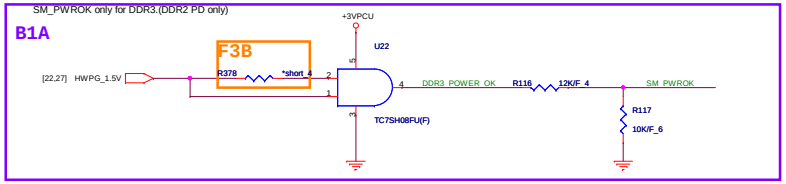

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated
with a 56-Ω pull-up resistor to VCCP.
+1.05V
TSATN#
R57
56_4
+3V
PM_EXTTS#0
PM_EXTTS#1
CLK_3GPLLREQ#
SM_REXT
R113
R103
R94
R79
10K_4
10K_4
10K_4
499/F_4

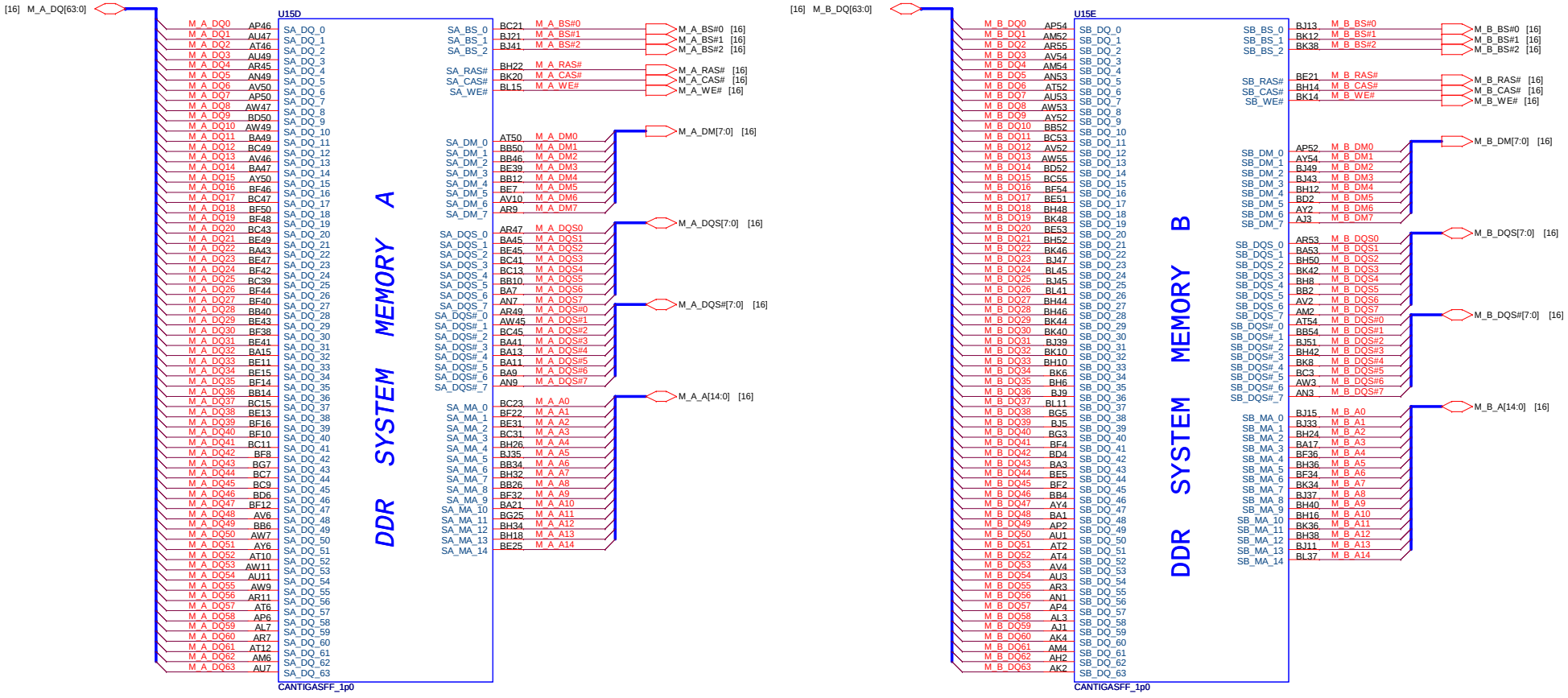

CRT setting
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_IREF
INT_TV_COMP
INT_TV_Y/G
INT_TV_C/R
R74
R78
R80
R98
R96
R83
R95
150/F_4
150/F_4
150/F_4
1K/F_4
75/F_4
75/F_4
75/F_4


LVDS setting
+3V
L_CTRL_CLK
L_CTRL_DATA
R290
R287
10K_4
10K_4
LVDS_IBG
2.37K/F_4
R119


+1.5VSUS_GMCH
SMRCOMPP
R90
80.6/F_4
SMRCOMPN
R115
80.6/F_4


+1.5VSUS_GMCH
R100
1K/F_4
SM_RCOMP_VOH
R101
3.01K/F_4
C195
0.01u/25V_4
C204
2.2u/6.3V_6
SM_RCOMP_VOL
R104
1K/F_4
C198
0.01u/25V_4
C196
2.2u/6.3V_6


SM_PWROK only for DDR3.(DDR2 PD only)
B1A
+3VPCU
U22
F3B
[22,27] HWPG_1.5V
R378
*short_4
DDR3_POWER_OK
R116
12K/F_4
SM_PWROK
R117
10K/F_6
TC7SH08FU(F)



NB7

PROJECT : BU3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	GANTIGA DDRII(3/6)	D3B
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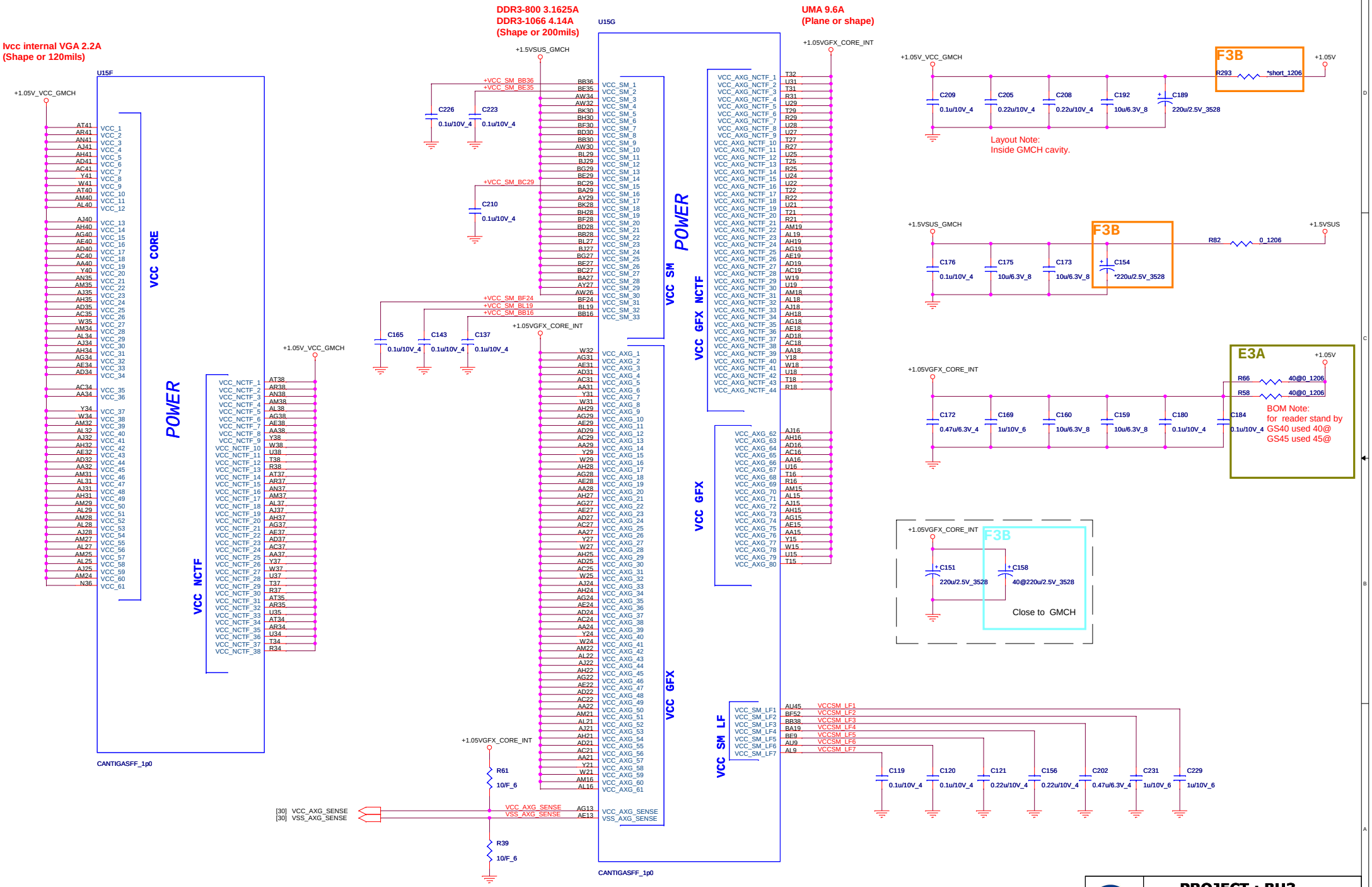
Ivcc internal VGA 2.2A
(Shape or 120mils)

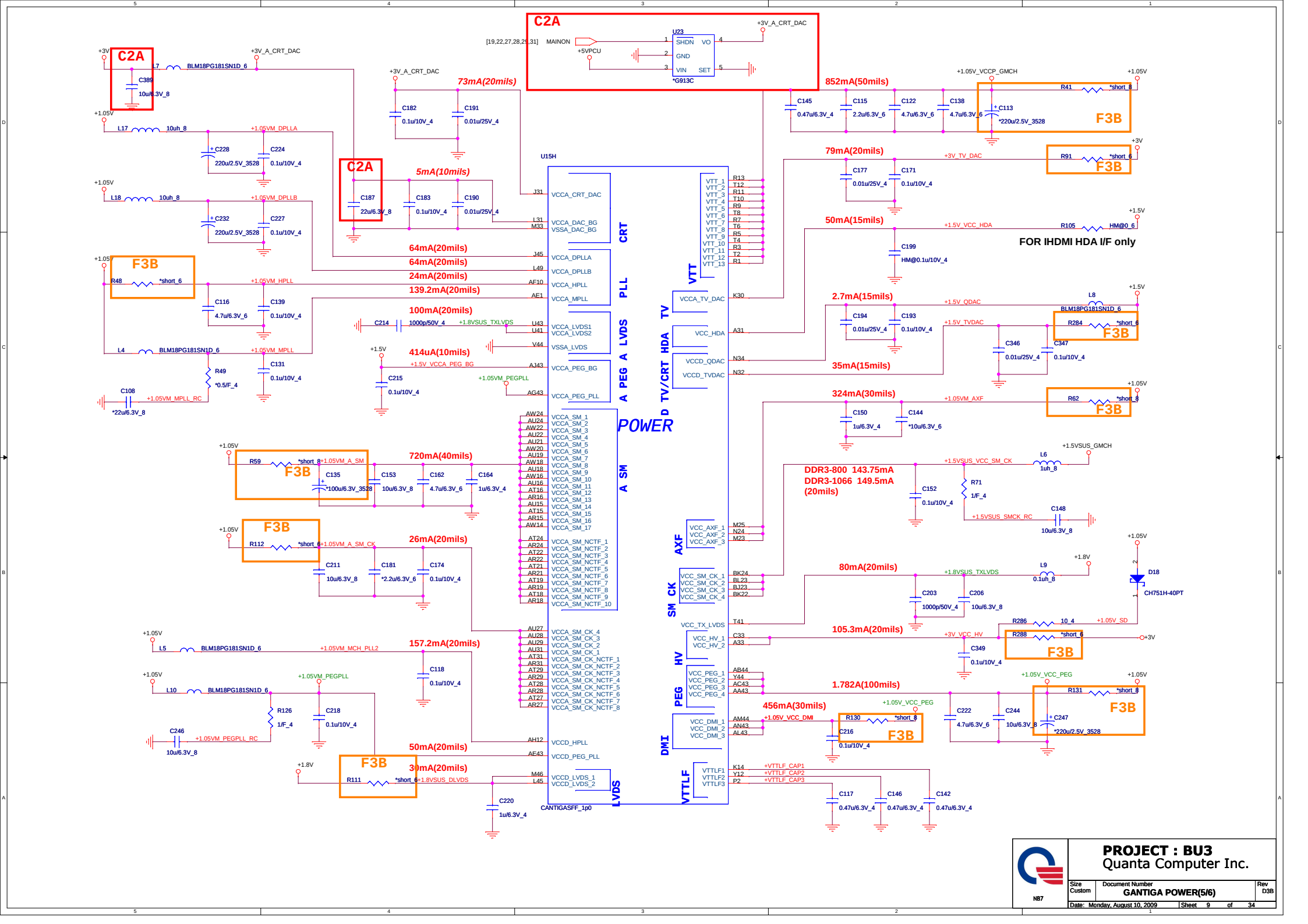
DDR3-800 3.1625A
DDR3-1066 4.14A
(Shape or 200mils)

UMA 9.6A
(Plane or shape)



UMA: Places R721, R726 to 10 ohm.

NB7	PROJECT : BU3 Quanta Computer Inc.		
	Size: Custom	Document Number: GANTIGA VCC/NCTF(4/6)	Rev: D3B
	Date: Monday, August 10, 2009	Sheet 8 of 34	


C2A
U23
SHDN
GND
VIN
VO
SET
*G913C
+3V_A_CRT_DAC
MAINON
+5VPCU
73mA(20mils)
852mA(50mils)
+1.05V_VCCP_GMCH
F3B
79mA(20mils)
+3V_TV_DAC
50mA(15mils)
+1.5V_VCC_HDA
FOR IHDMI HDA I/F only
U15H
5mA(10mils)
64mA(20mils)
64mA(20mils)
24mA(20mils)
139.2mA(20mils)
100mA(20mils)
414uA(10mils)
2.7mA(15mils)
35mA(15mils)
324mA(30mils)
720mA(40mils)
DDR3-800 143.75mA
DDR3-1066 149.5mA
(20mils)
26mA(20mils)
80mA(20mils)
105.3mA(20mils)
157.2mA(20mils)
1.782A(100mils)
456mA(30mils)
50mA(20mils)
30mA(20mils)
CRT
PLL
LVDS
TV
HDA
TV/CRT
PEG
A LVDS
A PEG
A SM
POWER
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
LVDS
CANTIGASFF_1p0
D18
CH751H-40PT
PROJECT : BU3
Quanta Computer Inc.
GANTIGA POWER(5/6)
Size Custom
Document Number
Rev D3B
Date: Monday, August 10, 2009
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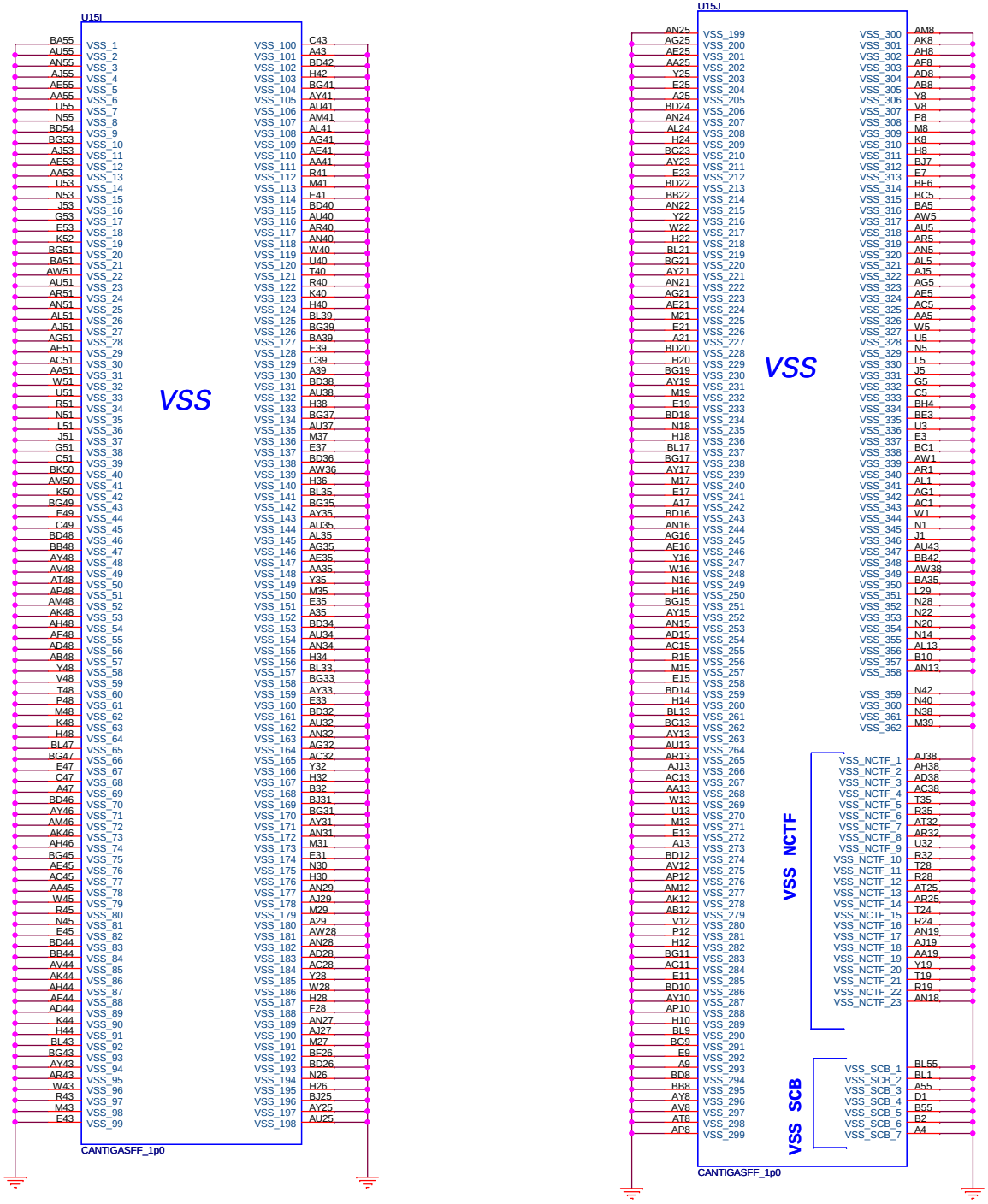

PROJECT : BU3	
Quanta Computer Inc.	
NB7	
Size: Custom	Document Number: GANTIGA VSS(6/6)
Rev: D3B	
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North Bridge Strap Pin Configuration Table

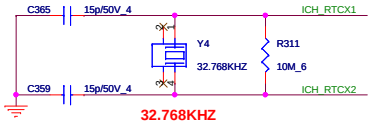
(See DG 2.0 P306 Table 187)
(See NB EDS 1.0 P187 Table 74)

Pin Name	Strap description	Configuration	PU<4.02K> PD <2.21K>	Note
CFG[2:0]	FSB Frequency Select	[000]= FSB 1066MHz [010] = FSB 800MHz [011] = FSB 667MHz	See Page 2 FSB selection table	
CFG[4:3]	Reserved			
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)	[6] MCH_CFG5 R97 *2.2K_4	
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)	[6] MCH_CFG6 R70 *2.2K/F_4	
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)	[6] MCH_CFG7 R72 *2.2K/F_4	
CFG8	Reserved			
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)	[6] MCH_CFG9 R73 *2.2K_4	
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)	[6] MCH_CFG10 R75 *2.2K/F_4	
CFG11	Reserved			
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)	[6] MCH_CFG12 R64 *2.2K/F_4	
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)	[6] MCH_CFG13 R77 *2.2K/F_4	
CFG[15:14]	Reserved			
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)	[6] MCH_CFG16 R81 *2.2K_4	
CFG[18:17]	Reserved			
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed	[6] MCH_CFG19 R93 *4.02K/F_4 +3V	
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port	[6] MCH_CFG20 R92 *4.02K/F_4 +3V	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI/DP Device Present(Default) 1 = SDVO/HDMI/DP Device present	*Strap on P18* *SDVO_CTRLDATA*	
L_DDC_DATA	Local Flat Panel(LFP) Present	0 = LFP Disable(Default) 1 = LFP Card Present;PCIE disable	*Strap on P17* *INT_LVDS_EDIDDATA*	
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present	[6] DDPC_CTRLDATA R109 *1.5K/F_4 +3V [6] DDPC_CTRLCLK R114 *1.5K/F_4 +3V	

Enable iTPM Table

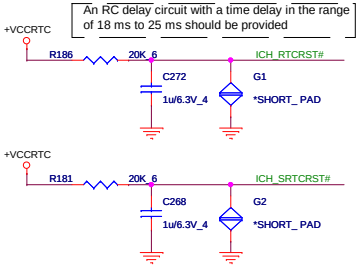
PAGE	Net Name	PU & PD	NOTE
11	MCH_CFG_6	PD 10K to GND	NB Strap pin
13	SPI_MOSI	PU 20K to +3V_S5	SB Strap pin
14	CLGPIO5	PU 10K to +3V_S5	SB Strap pin

RTC CRYSTAL

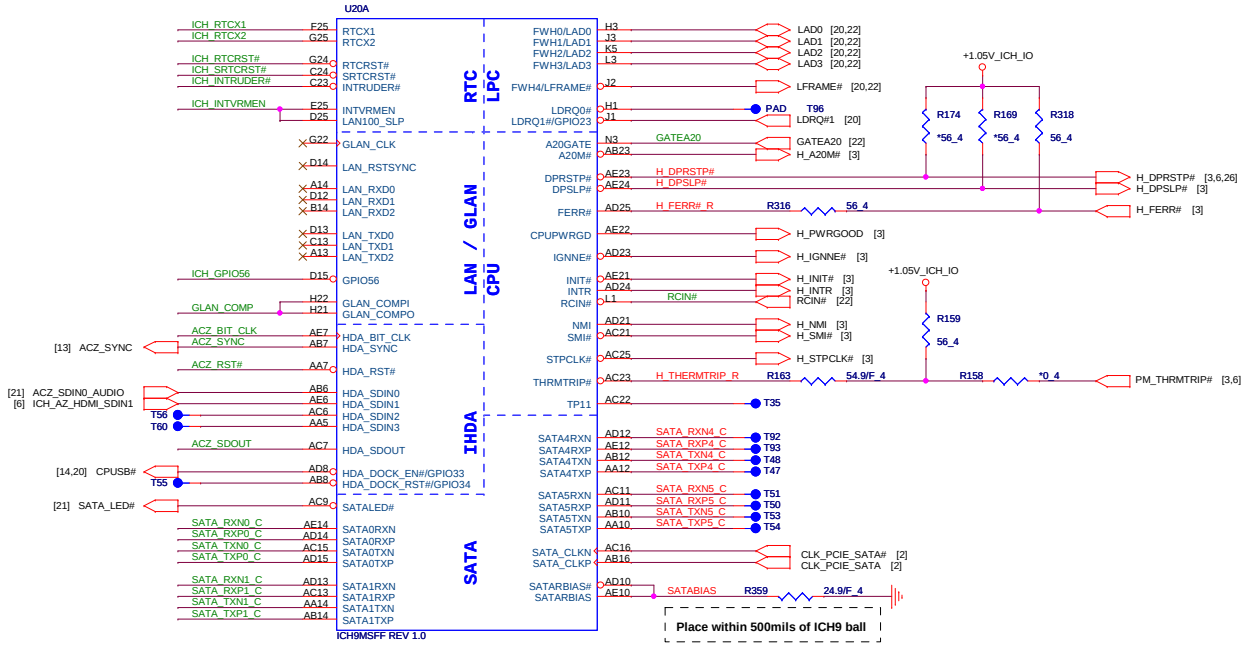


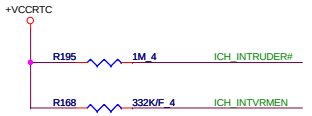
RESET JUMP

An RC delay circuit with a time delay in the range of 18 ms to 25 ms should be provided



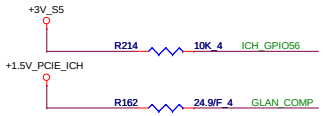
ICH_SATA_LED#	
0	PCIe Lane Reversed
1	PCIe Straight(default)



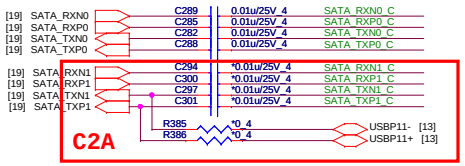


(DG 1.0 Table-292)

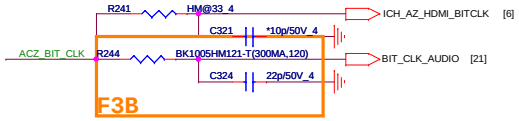
Internal VRM enabled for VccSus1_05, VccSus1_5, VccCL1_5, VccLAN1_05 and VccCL1_05.

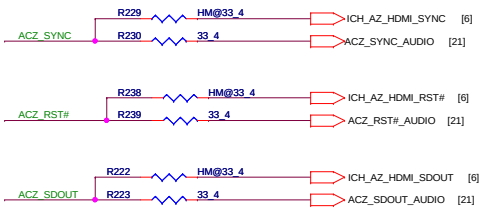


24.9 Ohm pull up to 1.5V for GLAN_COMPI/O is required, no matter intel LAN is used or not.



HD Audio Interface

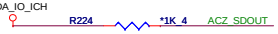




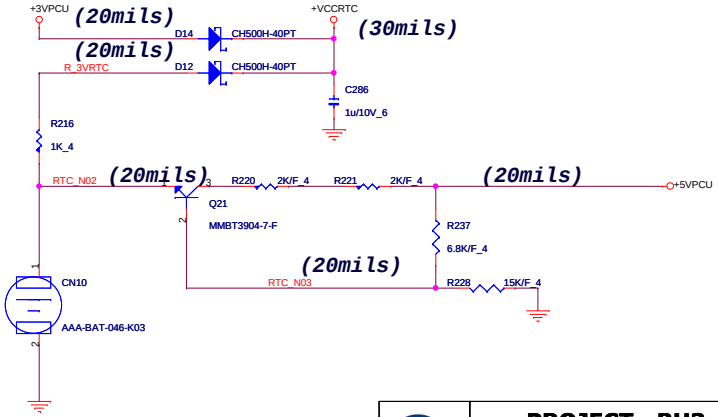
South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
	XOR Chain Entrance	PWROK		
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		

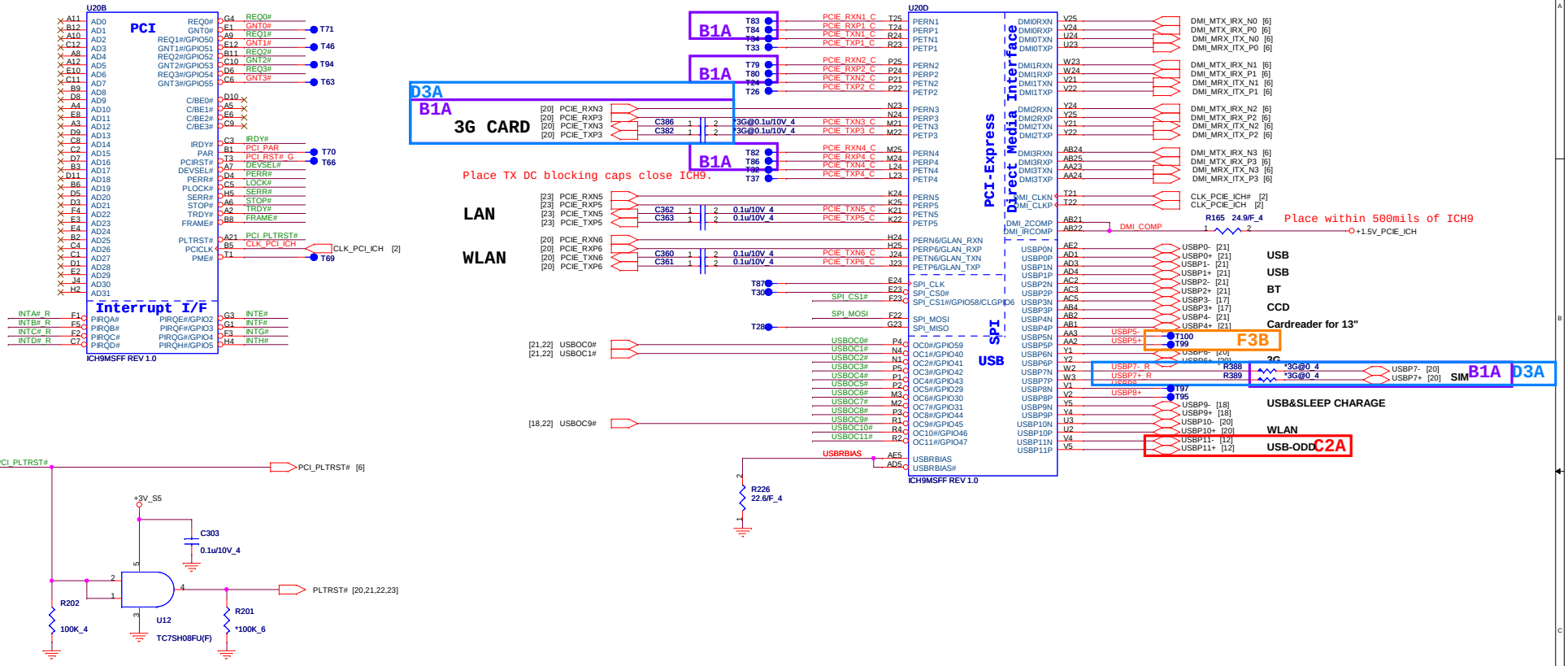
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1



RTC BATTERY



ICH9

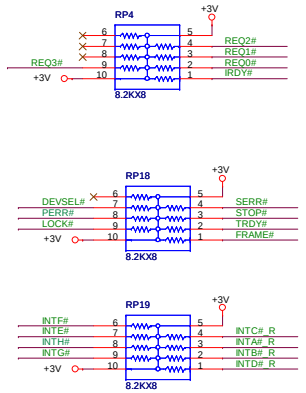


South Bridge Strap Pin (2/3)

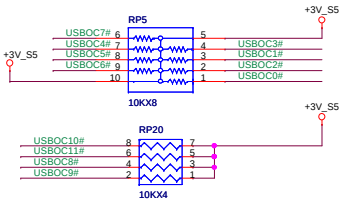
Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	+1.5V_HDA_IO_ICH — R231 *1K_4 — ACZ_SYNC [12]
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	GNT2# — R370 *1K_4
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# — R218 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI — R314 *20K_4
GNT0#	Boot BIOS Selection 0	PWROK		GNT0# — R246 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# — R164 *1K_4

PCI_GNT#0	SPI_CS#1	Boot Location
0	1	SPI(Default)
1	0	PCI

PCI PULL-UP



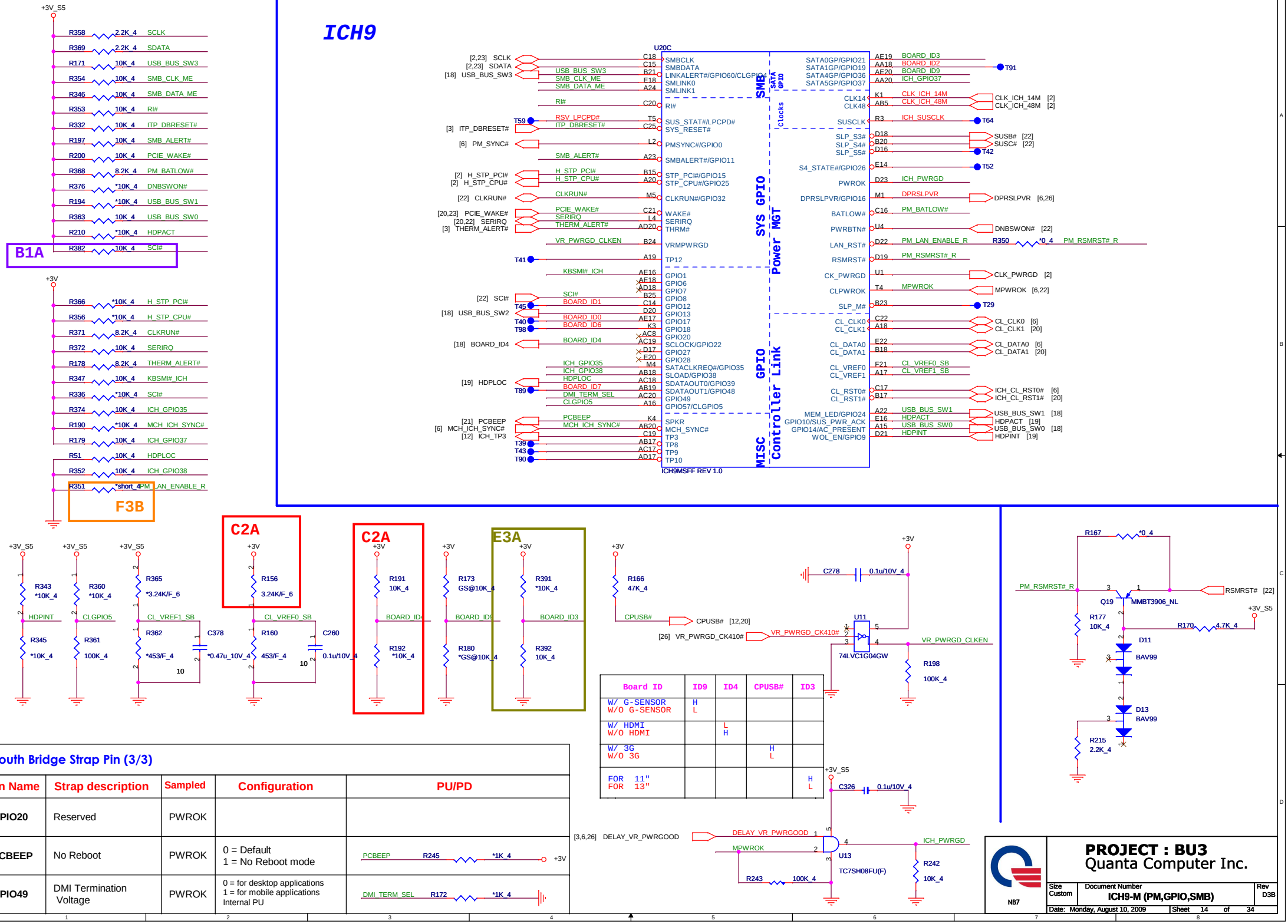
USBOC# PULL-UP



PROJECT : BU3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M (USB/PCIE/DMI)	D3B

Date: Monday, August 10, 2009 | Sheet 13 of 34


ICH9
B1A
F3B
C2A
C2A
E3A
U20C
ICH9MSFF REV 1.0
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
South Bridge Strap Pin (3/3)
Pin Name
Strap description
Sampled
Configuration
PU/PD
GPIO20
Reserved
PWROK
PCBEEP
No Reboot
PWROK
0 = Default
1 = No Reboot mode
GPIO49
DMI Termination Voltage
PWROK
0 = for desktop applications
1 = for mobile applications
Internal PU
Board ID
ID9
ID4
CPUSB#
ID3
W/ G-SENSOR
W/O G-SENSOR
W/ HDMI
W/O HDMI
W/ 3G
W/O 3G
FOR 11"
FOR 13"
74LVC1G04GW
TC7SH08FU(F)
PROJECT : BU3
Quanta Computer Inc.
ICH9-M (PM,GPIO,SMB)
Size Custom
Rev D3B
Date: Monday, August 10, 2009
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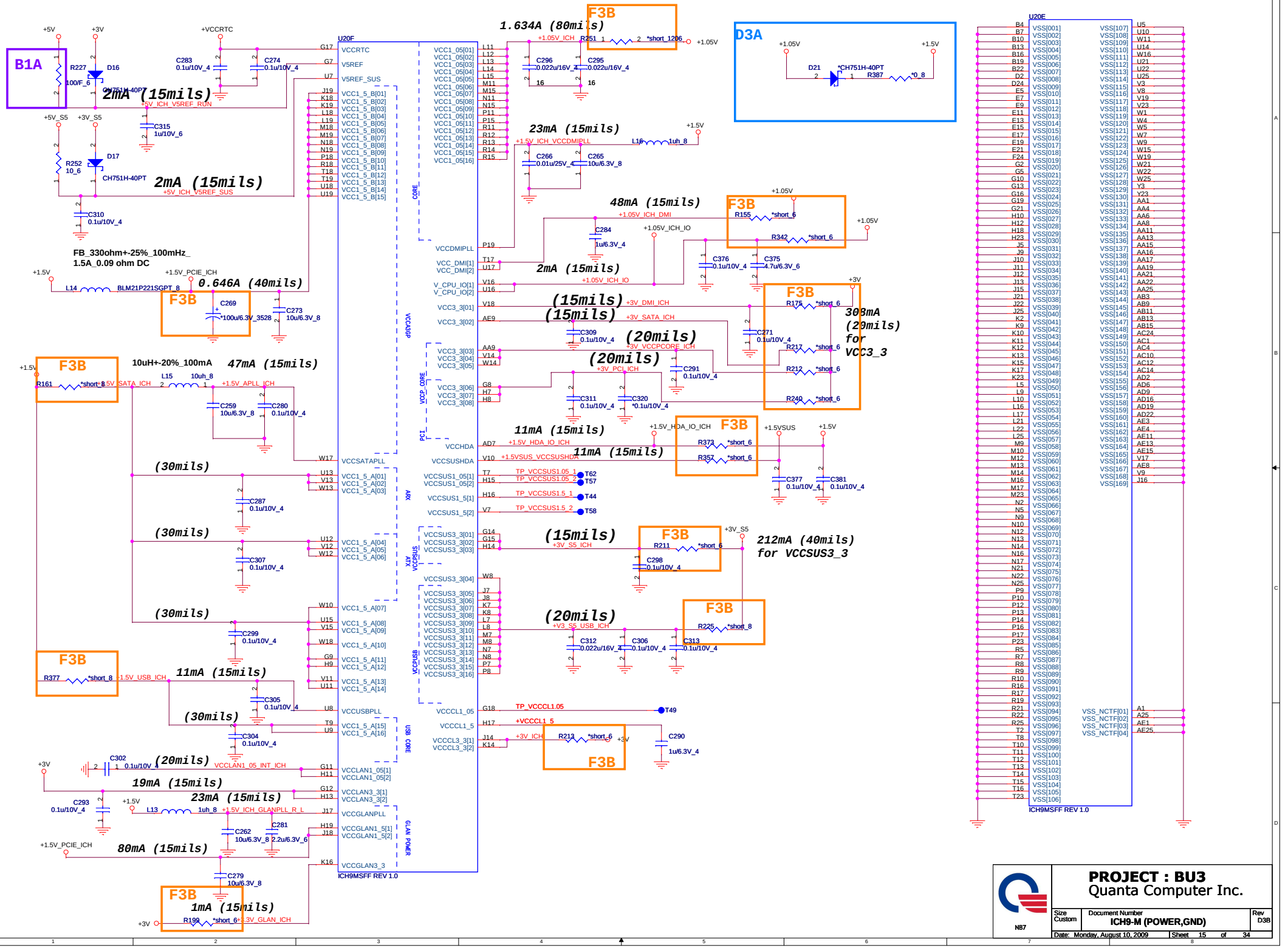
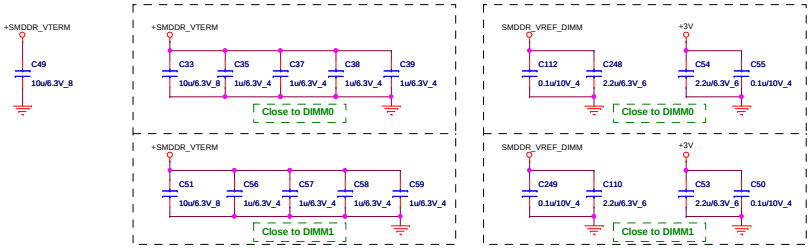
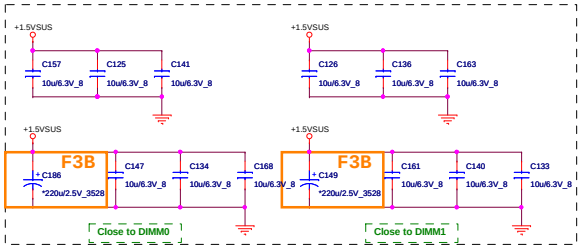

B1A
F3B
D3A
U20F
U20E
2mA (15mils)
1.634A (80mils)
23mA (15mils)
48mA (15mils)
2mA (15mils)
0.646A (40mils)
47mA (15mils)
11mA (15mils)
212mA (40mils) for VCCSUS3_3
308mA (20mils) for VCC3_3
1mA (15mils)
FB_330ohm+-25%_100mHz_ 1.5A_0.09 ohm DC
ICH9MSFF REV 1.0
PROJECT : BU3
Quanta Computer Inc.
ICH9-M (POWER,GND)
Monday, August 10, 2009

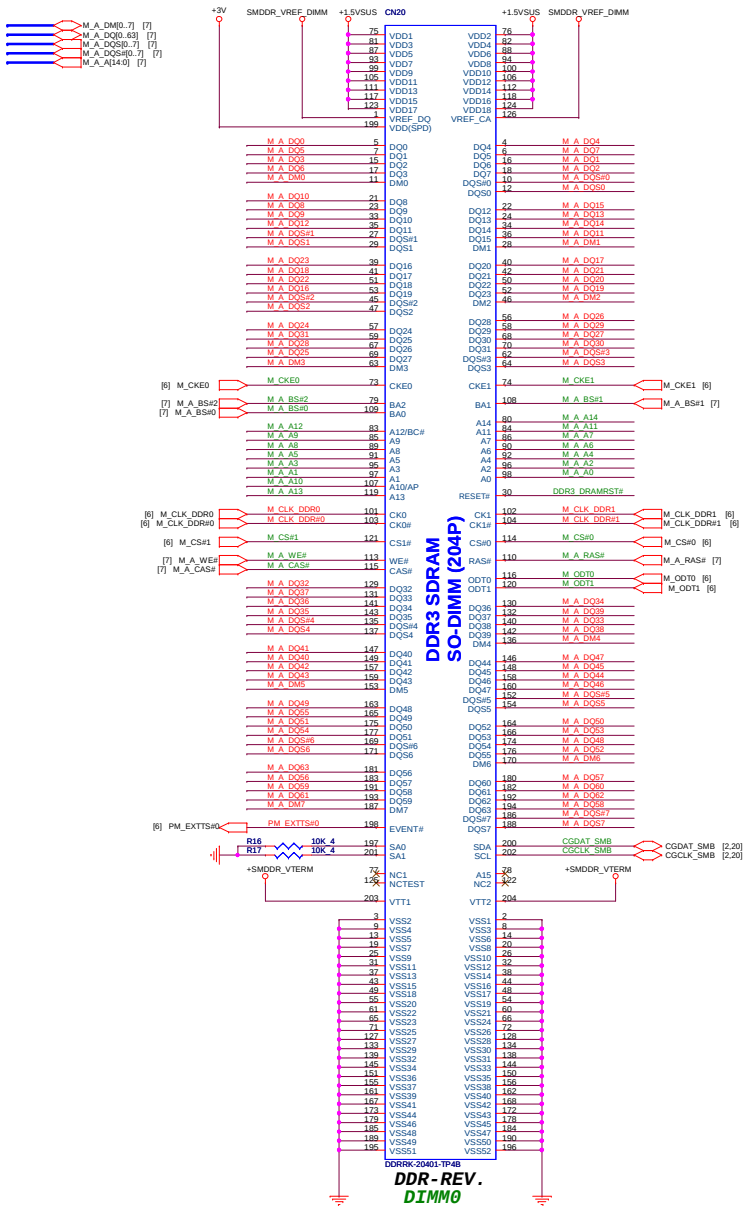
DDRIII

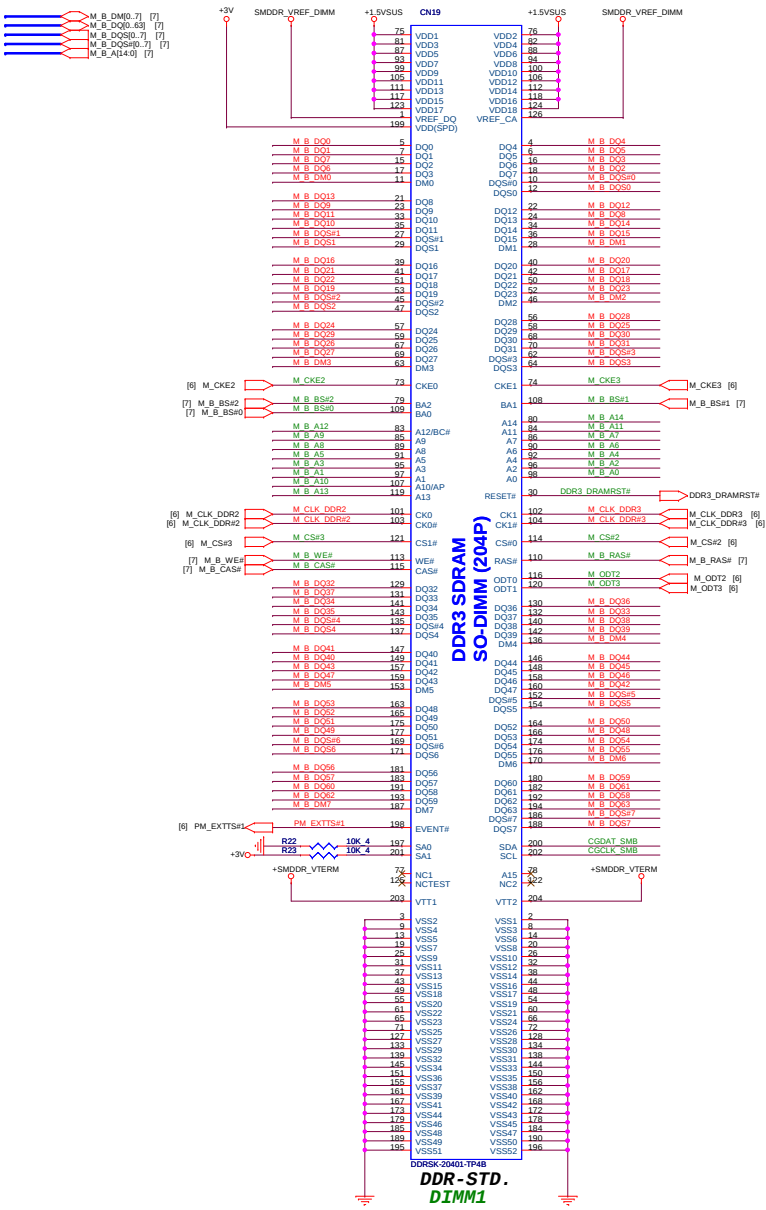
TERMINATOR DECOUPLING CAPACITOR

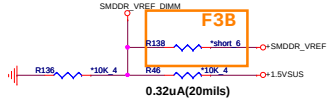


9.12A(VCC plane from source)









PROJECT : BU3 Quanta Computer Inc.			
N87	Size: Custom	Document Number: DDR2 SODIMMS: A/B CHANNEL	Rev: D3B
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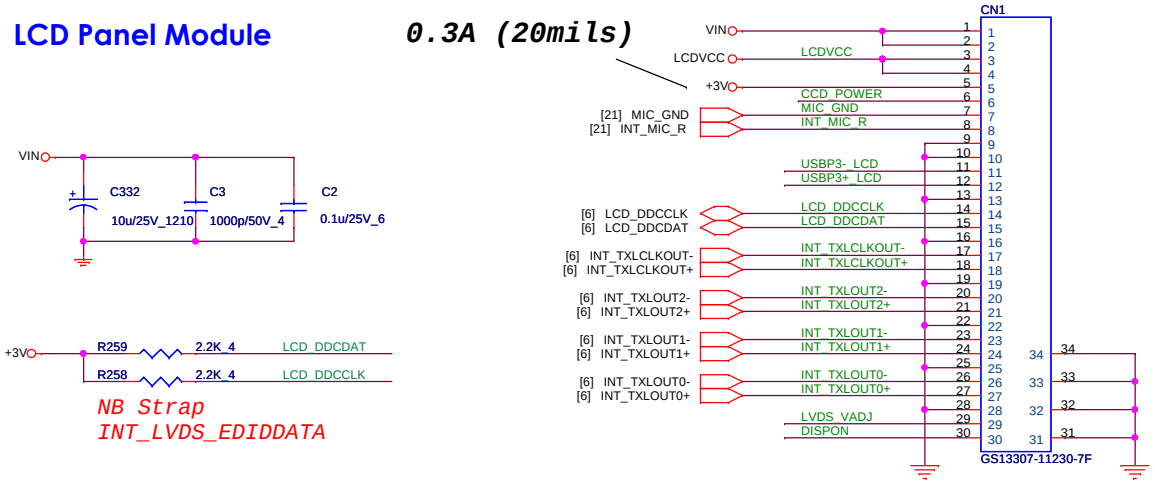
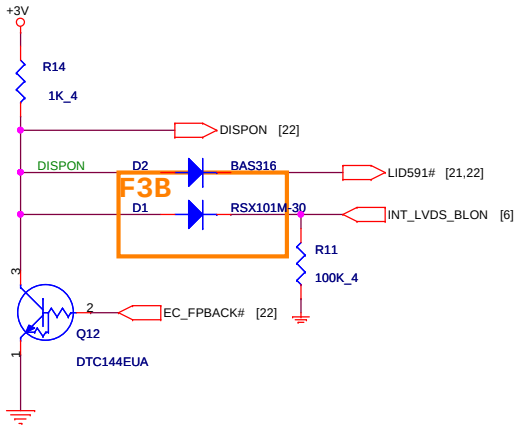
LCD Panel Module

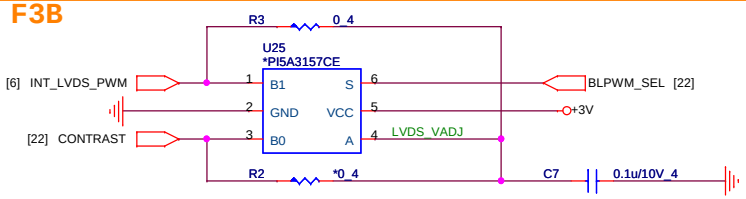
0.3A (20mils)



HALL SENSOR&BACK LIGHT SWITCH

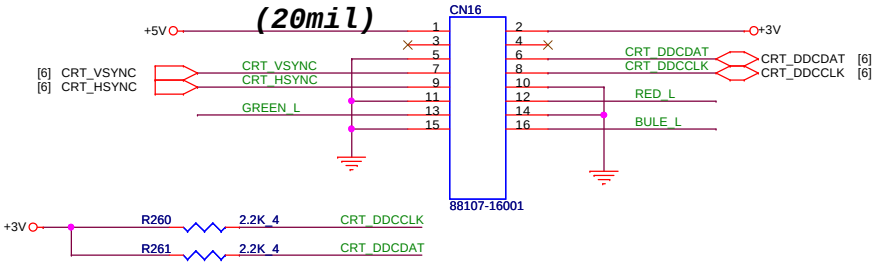


F3B



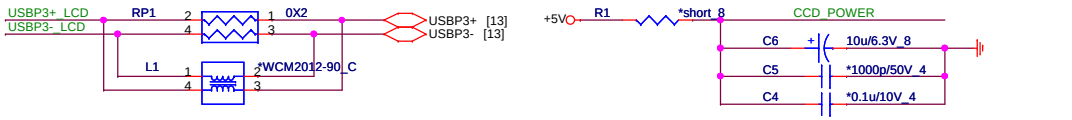
input S	S	S
output A		
INT_LVDS_PWM	H	
CONTRAST		L

CRT CON.

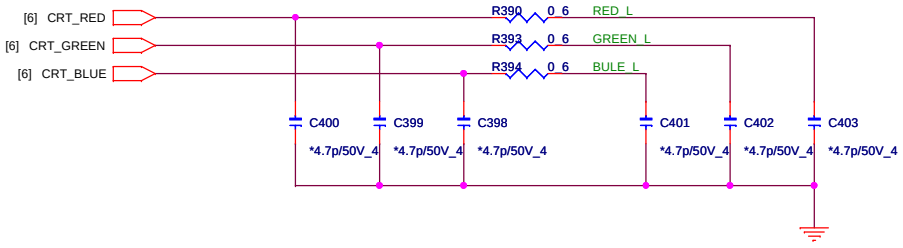


CCD

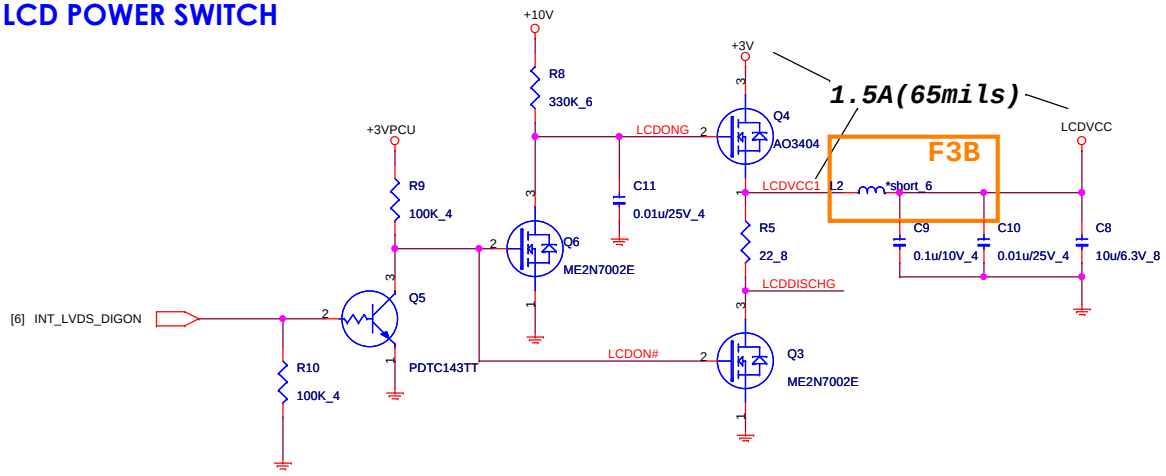
0.2A(20mils)



E3A



LCD POWER SWITCH



CRT CON. co-lay

E3A

Quanta Computer Inc.

PROJECT : BU3

Size	Document Number	Rev
	LCD/LED Panel/CCD	D3B
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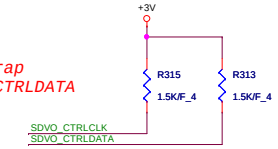
HDMI IC

B1A

NB Strap
SDVO_CTRLDATA



B1A

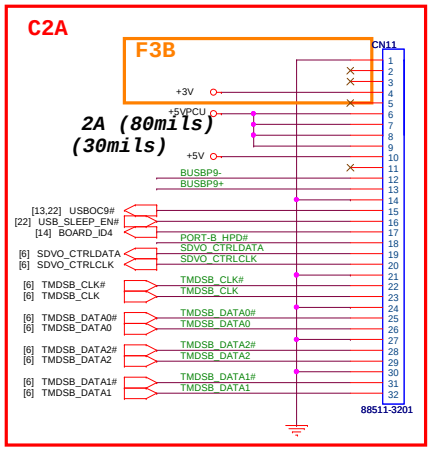
HDMI HPD

HDMI CON.

C2A

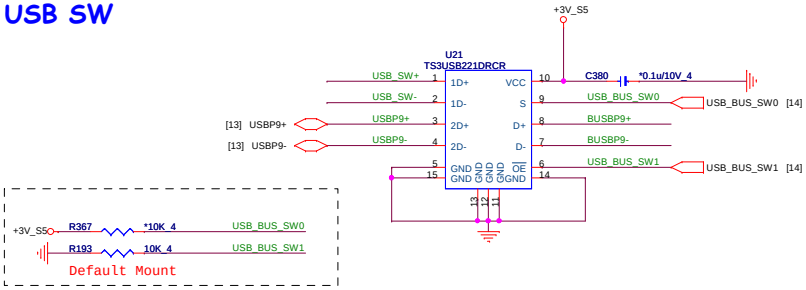
F3B

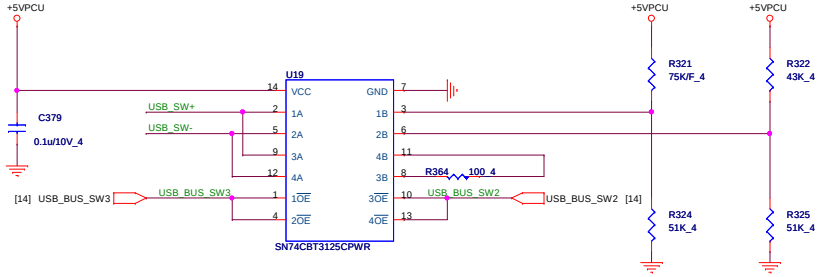
2A (80mils)
(30mils)



EMI

USB SW





S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

OE#	Function
H	Disconnect
L	A port= B port

OE#	1OE#	2OE#	3OE#	4OE#
Mode3	High	High	Low	Low
Mode4	Low	Low	High	High

Quanta Computer Inc.
PROJECT : BU3

Size	Document Number	Rev
	HDMI/USB SW/EMI	D3B

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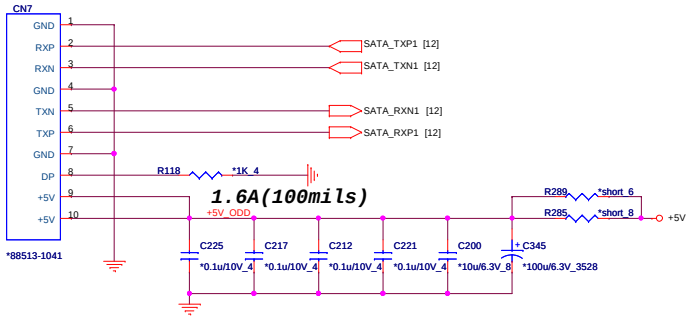
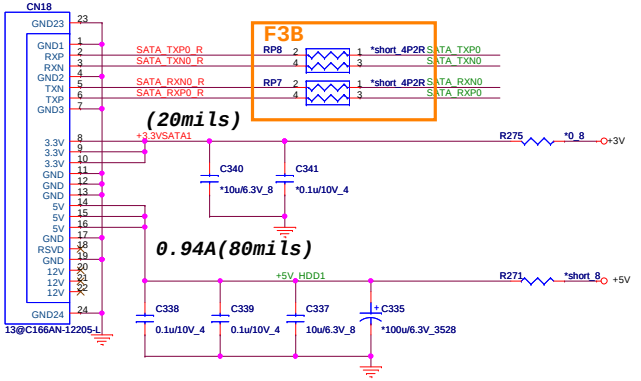
SATA ODD

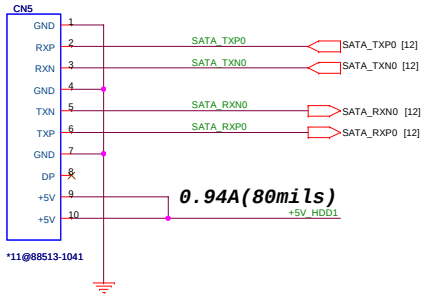
C2A



Main SATA HDD

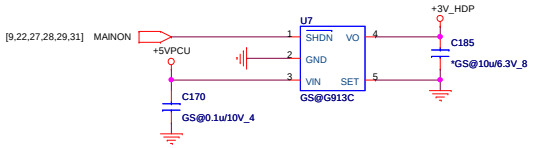


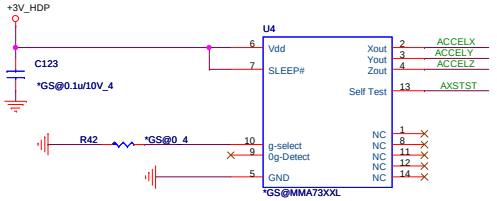
Main SATA HDD (For 11.6")



CO-LAYOUT With MAIN SATA HDD

G-sensor





FS (Full Scale) selection

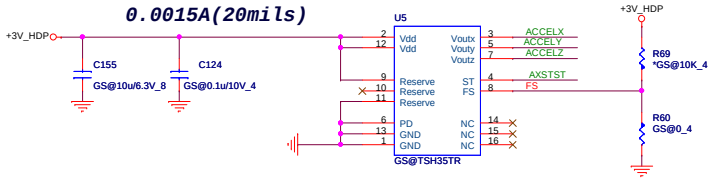
FS	0	1
	2g Full-Scale	6g Full-Scale

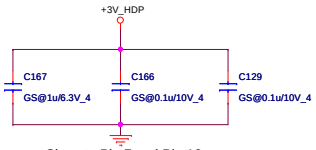
PD (Power Down) selection

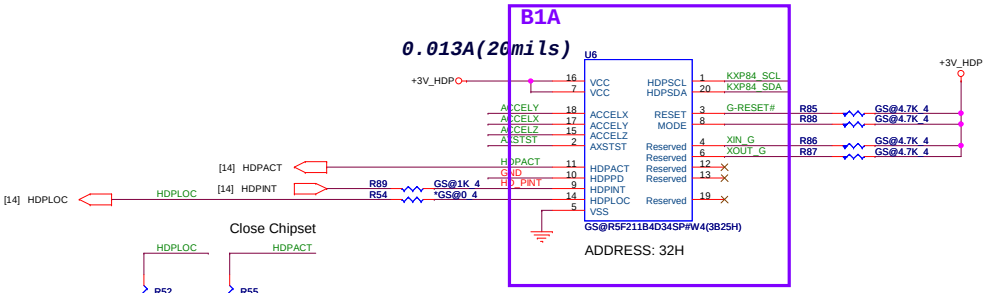
PD	0	1
	Normal Mode	Power-down mode

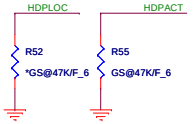
HDPPD selection

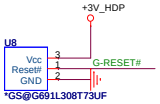
HDPPD	0	1
	Normal Mode	Power-down mode

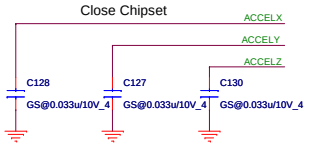


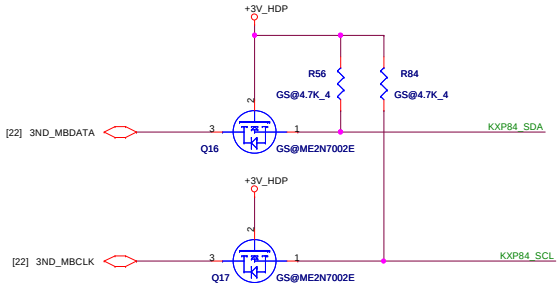


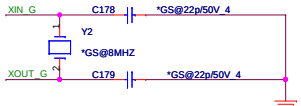












Quanta Computer Inc.
PROJECT : BU3

Size	Document Number	Rev
	HDD/ODD/G-sensor	D3B

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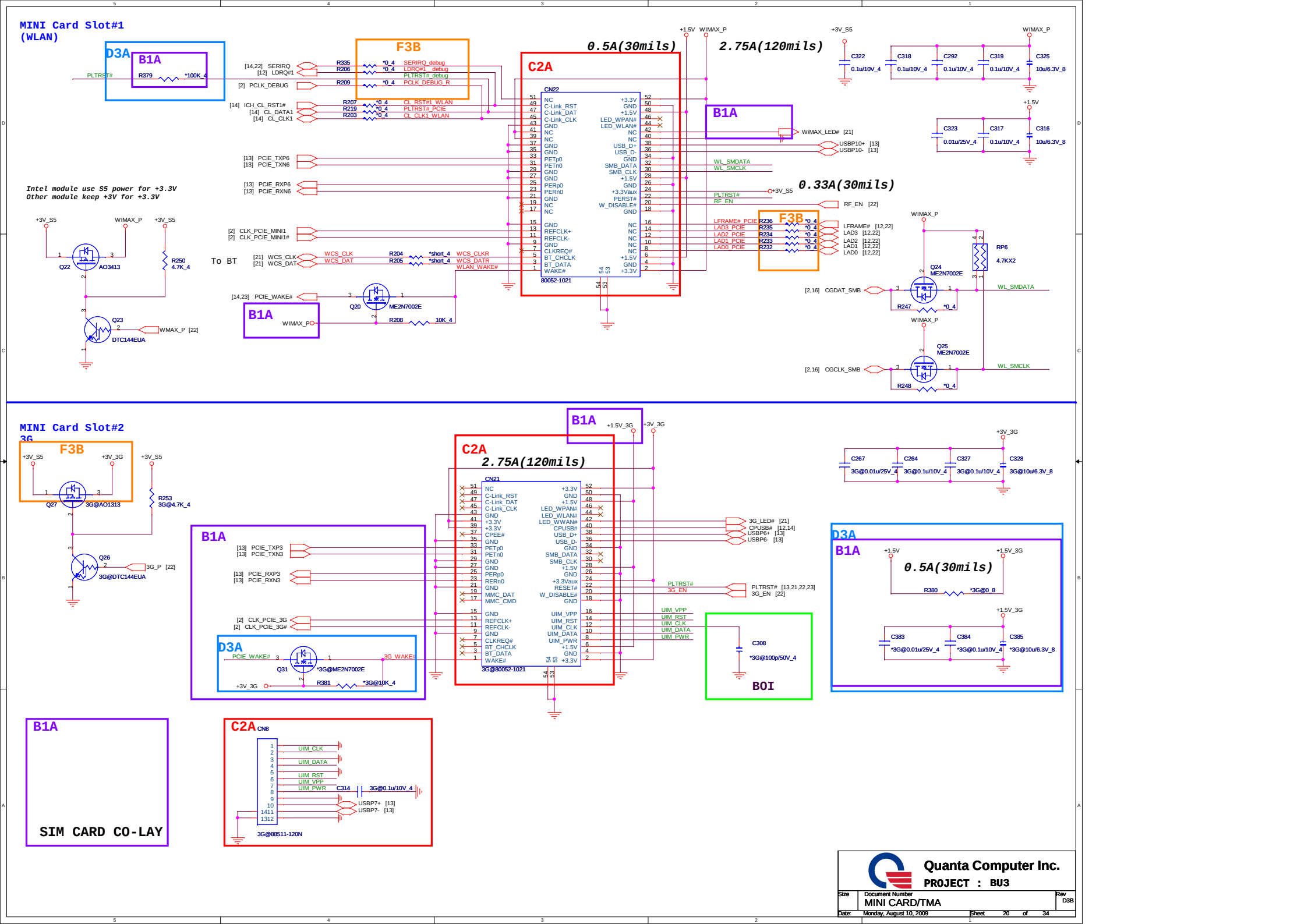
MINI Card Slot#1
(WLAN)
D3A
B1A
F3B
C2A
0.5A(30mils)
2.75A(120mils)
0.33A(30mils)
Intel module use S5 power for +3.3V
Other module keep +3V for +3.3V
To BT
CN22
80052-1021
Q22 AO3413
Q23 DTC144EUA
Q20 ME2N7002E
Q24 ME2N7002E
Q25 ME2N7002E
RP6 4.7KX2
WLAN_WAKE#
WL_SMDATA
WL_SMCLK
MINI Card Slot#2
3G
Q27 3G@AO1313
Q26 3G@DTC144EUA
CN21
3G@80052-1021
Q31 *3G@ME2N7002E
C308 *3G@100p/50V_4
BOI
B1A
SIM CARD CO-LAY
C2A CN8
3G@88511-120N
Quanta Computer Inc.
PROJECT : BU3
Size
Document Number
MINI CARD/TMA
Rev
D3B
Date: Monday, August 10, 2009
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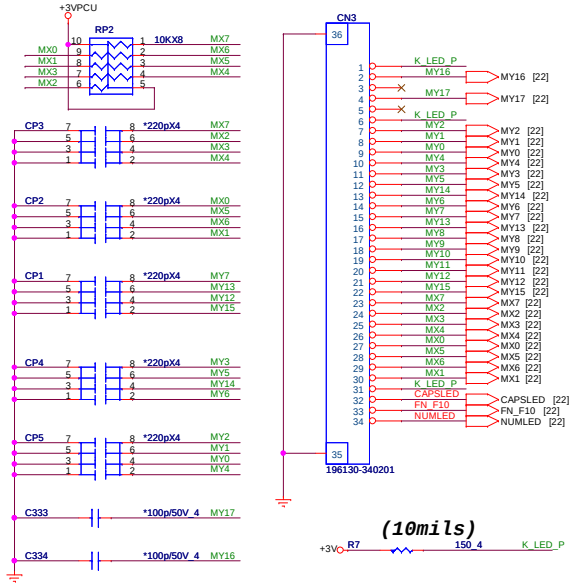
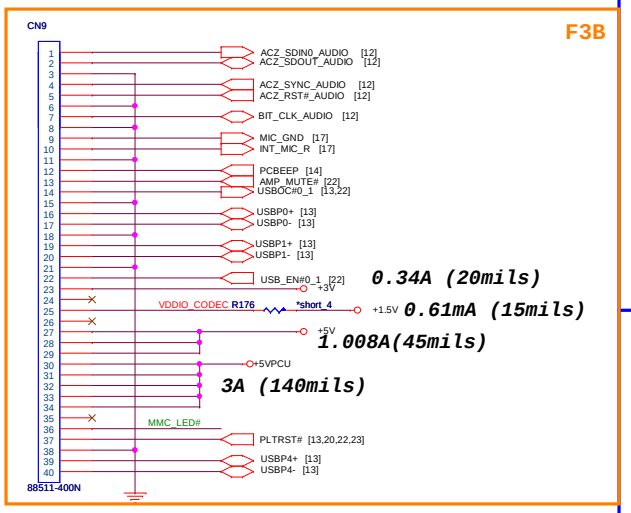
INT KeyBoard



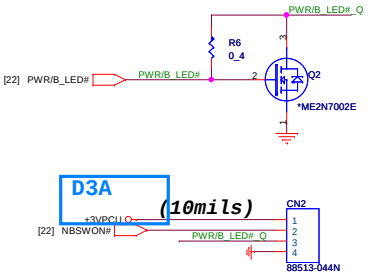
USB&FPC&CARDERAD CONNECTOR

C2A

F3B

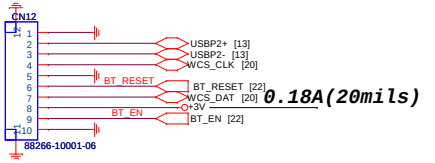


Power board



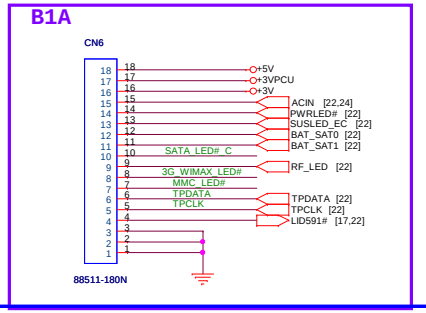
B1A

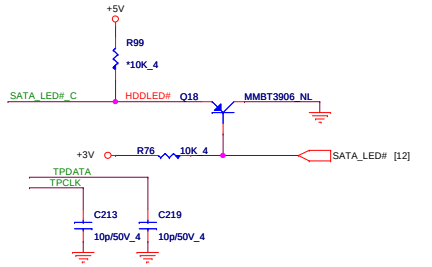
Bluetooth



LED/TP/Hall Sensor Con.

B1A

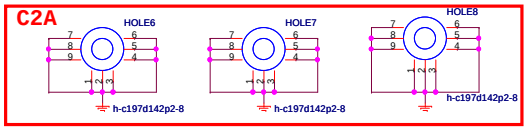


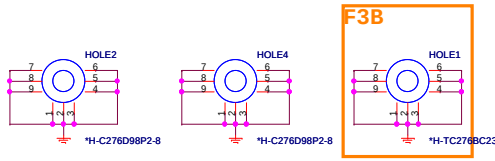


HOLE

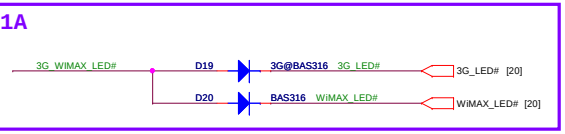
CPU FAN

C2A

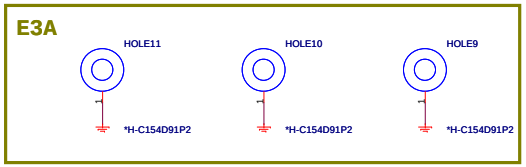




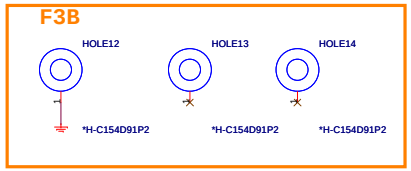
B1A



E3A

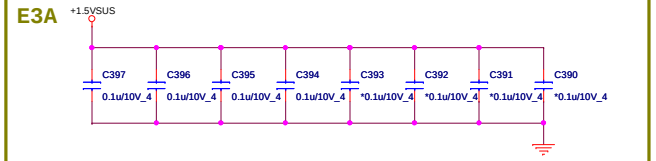


F3B



EMI

E3A



Quanta Computer Inc.

PROJECT : BU3

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EC

D3A

+3VPCU — D22 *VPORT 0603 220K-V05

SM BUS PU

+3VPCU

MBCLK	R148	4.7K_4
MBDATA	R147	4.7K_4
2ND_MBCLK	R146	4.7K_4
2ND_MBDATA	R152	4.7K_4
3ND_MBCLK	R122	4.7K_4
3ND_MBDATA	R121	4.7K_4

I/O Base Address

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0	BADDR0	R124	*10K_4
BADDR1	BT_EN	R129	10K_4
SHBM	RF_EN	R142	10K_4

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

ID

U10 AF24BC08-SI-TE1(DCEF) — SCL, SDA, A0, A1, A2, WP, VCC, GND

+3VPCU — 0.003A(20mils)

2ND_MBCLK, 2ND_MBDATA

C261 0.1u/10V_4

ADDRESS: A0H

SPI FLASH

+3VPCU — 0.025A(20mils)

U16 W25X16AVSSIG — SO, SI, SCK, CE, VDD, HOLD, WP, VSS

SPI_SDI_uR	R294	33_4	SPI_SDI
SPI_SDO_uR	R291	33_4	SPI_SDO
SPI_SCK_uR	R292	33_4	SPI_SCK
SPI_CS0#_uR	R295	10K_4	+3VPCU

C351 0.1u/10V_4

INTERNAL KEYBOARD STRIP SET

+3VPCU — MY0 — R132 10K_4

HWPG

+3V — R107 10K_4

[25] SYS_HWPG	D8	BAS316	HWPG
[28] HWPG_1.05V	D7	BAS316	
[29] HWPG_1.8V	D6	BAS316	
[6,27] HWPG_1.5V	D5	BAS316	

LED

+3VPCU

PWRLED#	R145	10K_4	
	R137	*10K_4	
PWR/B_LED#	R151	10K_4	
	R154	*10K_4	
BAT_SAT0	R141	10K_4	
BAT_SAT1	R106	10K_4	

0.01A(20mils)

+3VPCU — L11 BLM18AG601SN1D_6 — +A3VPCU — C245 0.1u/10V_4 — C251 10u/6.3V_8 — 8769AGND

0.03A(30mils)

C348 10u/6.3V_8; C207 0.1u/10V_4; C234 0.1u/10V_4; C233 0.1u/10V_4; C252 0.1u/10V_4; C253 0.1u/10V_4

+3V_VDD_EC — R102 *short_6 — +3V — C201 0.1u/10V_4 — C188 10u/6.3V_8

R393 must close to C315 and close to EC Pin100/102. Routing 20/10/20

H=1.6mm

U9 WPCE775CA0DG

VCC1 19, VCC2 46, VCC3 78, VCC4 88, VCC5 115, AVCC 102, VDD 4

LPC

[12,20] LFRAME#	3	LFRAME
[12,20] LAD0	126	LAD0
[12,20] LAD1	127	LAD1
[12,20] LAD2	128	LAD2
[12,20] LAD3	1	LAD3
[2] PCLK_591	2	LCLK
[14] CLKRUN#	8	CLKRUN/GPIO11
[12] GATEA20	121	GA20
[12] RCIN#	122	KBRST
[14] SCI#	29	ECSCI/GPIO54
[17] EC_FPBACK#	6	LDRQ/GPIO24
	124	LPCPD/GPIO10
[13,20,21,23] PLTRST#	7	LRESET
[21] USB_EN#0_1	123	PWUREQ/GPIO67
[14,20] SERIRQ	125	SERIRQ
[21] BAT_SAT1	9	SMI/GPIO65

PCLK_591 — R108 *22_4 — C197 *10p/50V_4

D9 BAS316 SCI#_uR

A/D

AD0/GPI90	97	MTEMP [24]
AD1/GPI91	98	ICMNT
AD2/GPI92	99	ACSET_EC
AD3/GPI93	100	ACSET_EC [24]
AD4/GPIO05	108	H_PROCHOT#_EC [3]
AD5/GPIO04	96	USBOC0# [13,18]
AD6/GPIO03	95	NBSWON#
AD7/GPIO07	94	NBSWON# [21]
		SUSB# [14]

D/A

DA0/GPI94	101	
DA1/GPI95	105	
DA2/GPI96	106	VFAN [3]
DA3/GPI97	107	SUSLED_EC [21]

GPIO

GPIO41(VBAT)	80	BAT_SAT0 [21]
GPIO42/TCK	17	RF_LED [21]
GPIO43/TMS	20	AMP_MUTE# [21]
GPIO44/TDI	21	ID [24]
GPIO50/TDO	25	D/C# [24]
CIRTX2/GPIO52/RDY	27	DISPON [17]

wake-up capability

no wake-up capability

GPO82/TRIS	110	
GPO84/BADDR0	112	BADDR0

SER

SOUT_CR/GPO83/BADDR1	111	BT_EN
SIN_CR/CIRRX/GPIO87	113	BT_EN [21]
GPIO06	93	USB_SLEEP_EN# [18]
		LID591# [17,21]

PWM

A_PWM/GPIO15	32	CONTRAST [17]
B_PWM/GPIO21	118	
C_PWM/GPIO13	62	USBOC#0_1
D_PWM/GPIO32	66	USBOC#0_1 [13,21]
E_PWM/GPIO45	22	SUSON [27,31]
F_PWM/GPIO40/CLKIN48	16	MAINON [9,19,27,28,29,31]
G_PWM/GPIO66	81	PWR/B_LED#
H_PWM/GPIO33	66	PWRLED# [21]

TIMER

TA1/GPIO56	31	3G_P [20]
TB1/GPIO14	63	FANSIG [3]
TA2/GPIO20	117	WMAX_P [20]
TB2/GPIO01	64	ACIN [21,24]
TA3/GPIO51	26	S5_ON [25]
TB3/GPIO36	15	VRON [26]

Pin 117 AMD PWM 1.2V INTEL WiMAX_P

SPI

SPI_DI/GPIO77	84	
SPI_DO/GPO76/SHBM	83	RF_EN
SPI_SCK/GPIO75	82	
GPIO81	91	DNBSWON# uR — D10 BAS316 — DNBSWON# [14]

FIR

IRRX1/GPIO72/SIN2	75	RSMRST#
IRRX2_IRSL0/GPIO70	73	RSMRST# [14]
IRTX/GPIO71/SOUT2	74	MPWROK
CIRRXM/GPIO46/TRST	23	SUSC# [14]
		MPWROK [6,14]

CIR

GPIO34/CIRRXL	24	
CIRTX1/GPIO16	114	NUMLED [21]
CIRTX2/GPIO30	109	CAPSLED [21]

FIU

F_SDI/F_SDIO1	86	SPI_SDI_uR
F_SDO/SDIO0	87	SPI_SDO_uR
F_CS0	90	SPI_CS0#_uR
F_SCK	92	SPI_SCK_uR

SMB

SCL1/GPIO17	70	
SDA1/GPIO22	69	
SCL2/GPIO26	67	
SDA2/GPIO74	68	
SCL3/GPIO23	119	
SDA3/GPIO31	120	
SCL4/GPO47	24	
SDA4/GPIO53	28	

[24] MBCLK, [24] MBDATA, [3] 2ND_MBCLK, [3] 2ND_MBDATA, [19] 3ND_MBCLK, [19] 3ND_MBDATA, [20] 3G_EN — HWPG

PS/2

PSCLK1/GPIO37	72	TPCLK
PSDAT1/GPIO35	71	TPDATA
PSCLK2/GPIO26	10	
PSDAT2/GPIO27	11	
PSCLK3/GPIO25	12	
PSDAT3/GPIO12	13	

[21] TPCLK, [21] TPDATA

[21] FN_F10, [17] BLPWM_SEL — F3B

KB

[21] MX0	54	KBSIN0
[21] MX1	55	KBSIN1
[21] MX2	56	KBSIN2
[21] MX3	57	KBSIN3
[21] MX4	58	KBSIN4
[21] MX5	59	KBSIN5
[21] MX6	60	KBSIN6
[21] MX7	61	KBSIN7
[21] MY0	53	KBSOUT0/JENK
[21] MY1	52	KBSOUT1/TCK
[21] MY2	51	KBSOUT2/TMS
[21] MY3	50	KBSOUT3/TDI
[21] MY4	49	KBSOUT4/JEN0
[21] MY5	48	KBSOUT5/TDO
[21] MY6	47	KBSOUT6/RDY
[21] MY7	43	KBSOUT7
[21] MY8	42	KBSOUT8
[21] MY9	41	KBSOUT9
[21] MY10	40	KBSOUT10
[21] MY11	39	KBSOUT11
[21] MY12	38	KBSOUT12/GPIO64
[21] MY13	37	KBSOUT13/GPIO63
[21] MY14	36	KBSOUT14/GPIO62
[21] MY15	35	KBSOUT15/GPIO61/XOR_OUT
[21] MY16	34	KBSOUT16/GPIO60
[21] MY17	33	KBSOUT17/GPIO57

+5V — R150 10K_4 TPCLK — R149 10K_4 TPDATA

C2A

R135 100K/F_4 — +3VPCU

LAN_P [23] — C2A

VCC_POR# — R143 4.7K_4 — +3VPCU

VREF_uR — R133 0_4 — +A3VPCU

F3B

ICMNT, ACSET_EC — F3B

C2A

R144 20M_6 — 8768_32KX1 — 8768_32KX2

Y3 32.768KHZ — C255 15p/50V_4 — C257 15p/50V_4 — R153 33K/F_4 — 8769AGND

8769AGND

L12 0_6 — C230 1u/10V_6 — VCORF_uR

close to u9

ACSET_EC, ICMNT — C254 *10u/6.3V_8 — C256 *10u/6.3V_8 — 8769AGND

DNBSWON# uR — C250 *0.47u/10V_4

NBSWON# — SW1 *SHORT_PAD

[13,21] USBOC0# — USBOC#0_1

[13,21] USBOC1# — USBOC#0_1

[21] USB_EN#0 — USB_EN#0_1

[21] USB_EN#1 — USB_EN#0_1

SMBUS Table

SMBUS	Devices	Address
1	Battery	
2	CPU Thermal Sensor1	98H
	EC EEPROM	A0H
3	3D Sensor	40H

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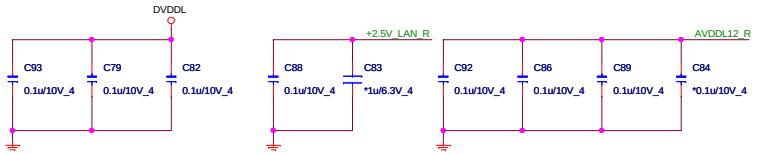
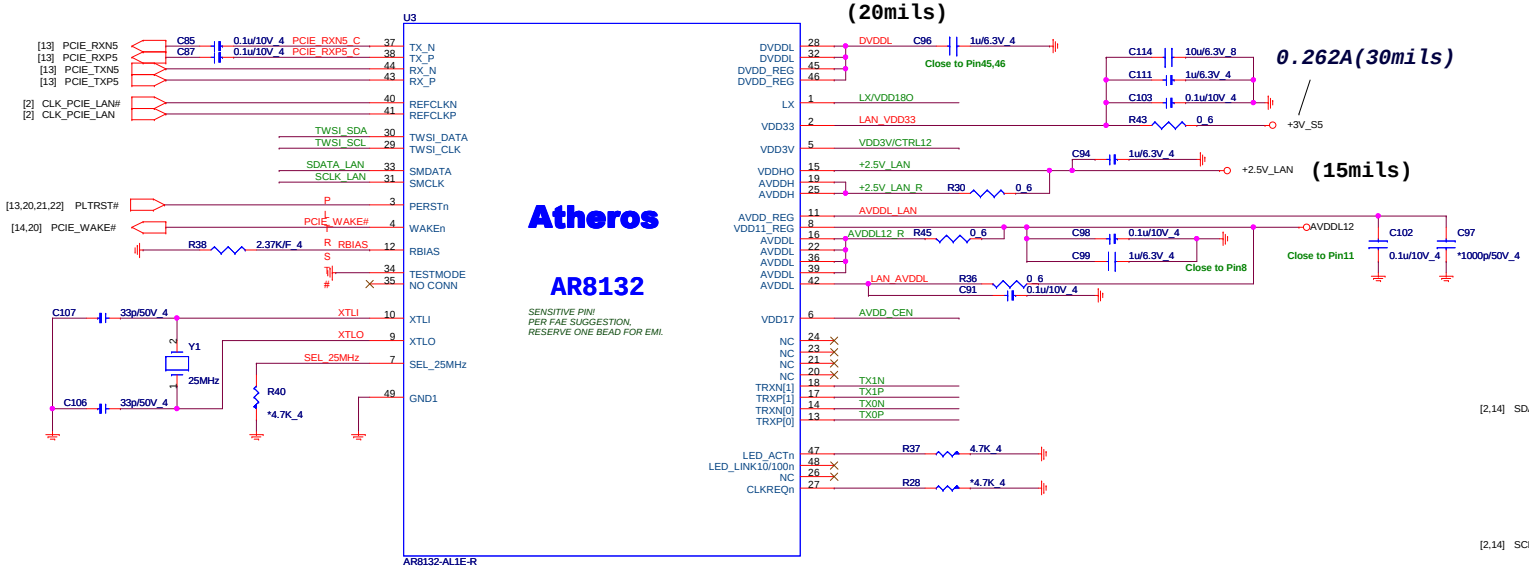
Atheros Lan

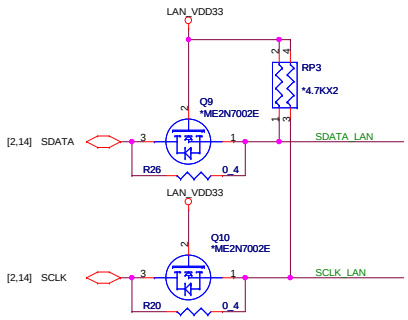
Decoupling CAP

Close to U3



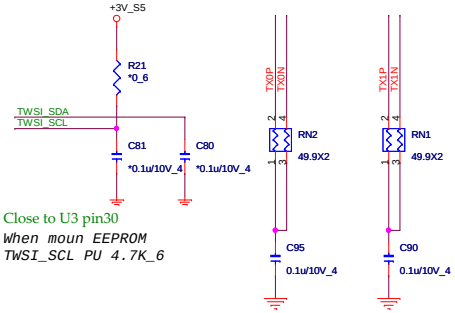
(20mils)





EEPROM

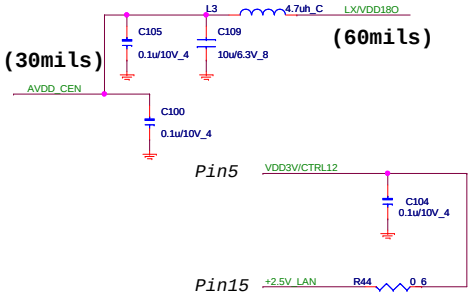
PLACE NEAR LAN IC SIDE



Close to U3 pin30

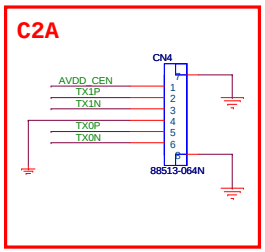
When moun EEPROM
TWSI_SCL PU 4.7K_6

Close to U3

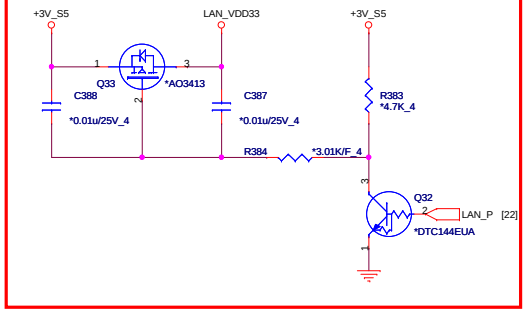


LAN CONNECTOR

C2A



C2A



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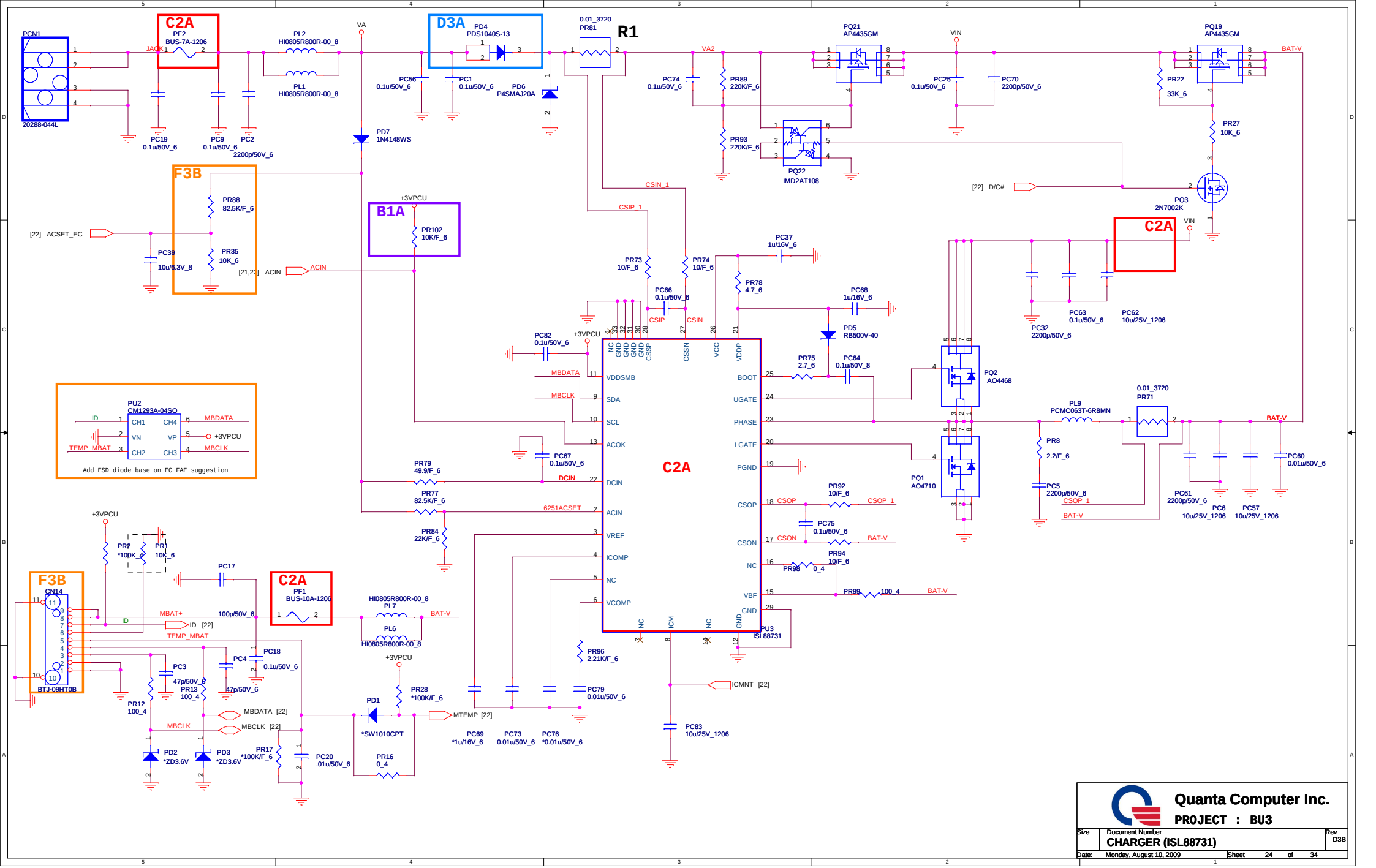
C2A
PF2
BUS-7A-1206
PCN1
20288-044L
PL2
HI0805R800R-00_8
PL1
HI0805R800R-00_8
VA
D3A
PD4
PDS1040S-13
PC56
0.1u/50V_6
PC1
0.1u/50V_6
PD6
P4SMAJ20A
0.01_3720
PR81
R1
VA2
PC74
0.1u/50V_6
PR89
220K/F_6
PR93
220K/F_6
PQ21
AP4435GM
PQ22
IMD2AT108
VIN
PC25
0.1u/50V_6
PC70
2200p/50V_6
PQ19
AP4435GM
BAT-V
PR22
33K_6
PR27
10K_6
PQ3
2N7002K
[22] D/C#
PC19
0.1u/50V_6
PC9
0.1u/50V_6
PC2
2200p/50V_6
PD7
1N4148WS
F3B
PR88
82.5K/F_6
PC39
10u/6.3V_8
PR35
10K_6
[22] ACSET_EC
[21,22] ACIN
ACIN
B1A
+3VPCU
PR102
10K/F_6
CSIN_1
CSIP_1
PR73
10/F_6
PR74
10/F_6
PC37
1u/16V_6
PR78
4.7_6
PC66
0.1u/50V_6
PC68
1u/16V_6
CSIP
CSIN
PD5
RB500V-40
C2A
VIN
PC63
0.1u/50V_6
PC62
10u/25V_1206
PC32
2200p/50V_6
PC82
0.1u/50V_6
+3VPCU
NC
GND
GND
GND
GND
CSSP
CSSN
VCC
VDDP
MBDATA
MBCLK
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
PU3
ISL88731
C2A
PR75
2.7_6
PC64
0.1u/50V_8
PQ2
AO4468
PQ1
AO4710
PL9
PCMC063T-6R8MN
0.01_3720
PR71
PR8
2.2/F_6
PC5
2200p/50V_6
PC61
2200p/50V_6
PC6
10u/25V_1206
PC57
10u/25V_1206
PC60
0.01u/50V_6
CSOP_1
BAT-V
PU2
CM1293A-04SO
ID
TEMP_MBAT
CH1
CH4
VN
VP
CH2
CH3
MBDATA
+3VPCU
MBCLK
Add ESD diode base on EC FAE suggestion
PR79
49.9/F_6
PR77
82.5K/F_6
PR84
22K/F_6
6251ACSET
DCIN
PR92
10/F_6
PC75
0.1u/50V_6
PR94
10/F_6
PR98
0_4
PR99
100_4
PR96
2.21K/F_6
PC79
0.01u/50V_6
ICMNT [22]
PC83
10u/25V_1206
PC69
*1u/16V_6
PC73
0.01u/50V_6
PC76
*0.01u/50V_6
F3B
CN14
BTJ-09HT0B
MBAT+
ID
ID [22]
TEMP_MBAT
PR2
*100K_4
PR1
10K_6
PC17
100p/50V_6
C2A
PF1
BUS-10A-1206
HI0805R800R-00_8
PL7
PL6
HI0805R800R-00_8
BAT-V
PC3
47p/50V_8
PC4
47p/50V_6
PC18
0.1u/50V_6
PR12
100_4
PR13
100_4
MBDATA [22]
MBCLK
MBCLK [22]
PD2
*ZD3.6V
PD3
*ZD3.6V
PR17
*100K/F_6
PC20
.01u/50V_6
PD1
*SW1010CPT
PR28
*100K/F_6
PR16
0_4
MTEMP [22]
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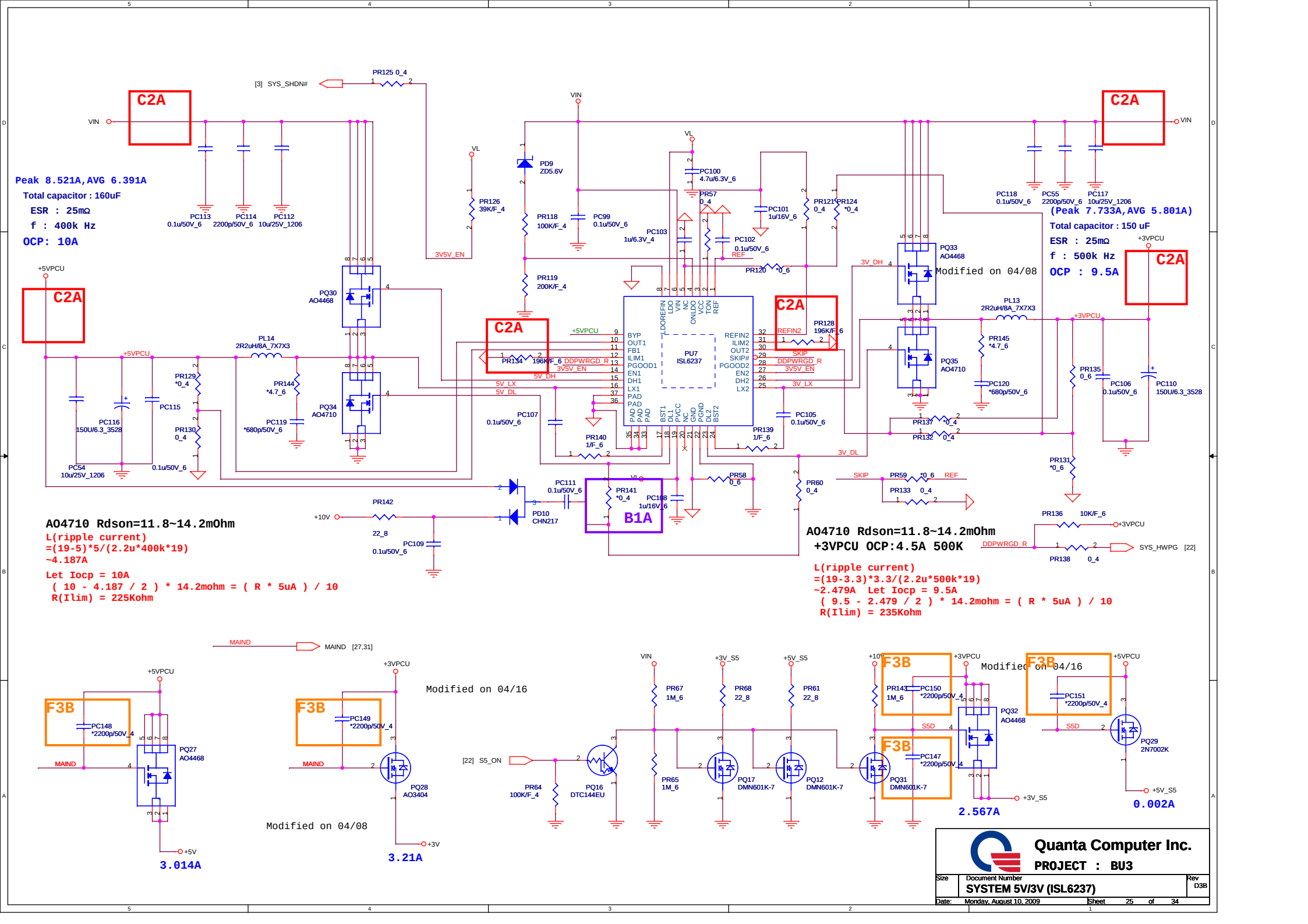
Peak 8.521A,AVG 6.391A
Total capacitor : 160uF
ESR : 25mΩ
f : 400k Hz
OCP: 10A
C2A
VIN
PR125 0_4
[3] SYS_SHDN#
PC113 0.1u/50V_6
PC114 2200p/50V_6
PC112 10u/25V_1206
PR126 39K/F_4
PD9 ZD5.6V
PR118 100K/F_4
PC99 0.1u/50V_6
PR119 200K/F_4
3V5V_EN
PC100 4.7u/6.3V_6
PR57 0_4
PC103 1u/6.3V_4
PC101 1u/16V_6
PC102 0.1u/50V_6
PR121 0_4
PR124 *0_4
PR120 *0_6
REF
PQ30 AO4468
PQ34 AO4710
PL14 2R2uH/8A_7X7X3
PR129 *0_4
PR144 *4.7_6
PC115
PC116 150U/6.3_3528
PR130 0_4
PC119 *680p/50V_6
PC54 10u/25V_1206
0.1u/50V_6
+5VPCU
PU7 ISL6237
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
PR134 196K/F_6
DDPWRGD_R
5V_LX
5V_DL
5V_DH
3V_LX
3V_DL
PC107 0.1u/50V_6
PC105 0.1u/50V_6
PR140 1/F_6
PR139 1/F_6
PC111 0.1u/50V_6
PR141 *0_4
PC108 1u/16V_6
PR58 0_6
PR60 0_4
PD10 CHN217
PR142 22_8
PC109 0.1u/50V_6
+10V
B1A
AO4710 Rdson=11.8~14.2mOhm
L(ripple current)
=(19-5)*5/(2.2u*400k*19)
~4.187A
Let Iocp = 10A
(10 - 4.187 / 2) * 14.2mohm = (R * 5uA) / 10
R(Ilim) = 225Kohm
Modified on 04/08
PQ33 AO4468
PQ35 AO4710
PL13 2R2uH/8A_7X7X3
PR145 *4.7_6
PC120 *680p/50V_6
PR135 0_6
PC106 0.1u/50V_6
PC110 150U/6.3_3528
PR137 *0_4
PR132 0_4
PR131 *0_6
PR128 196K/F_6
REFIN2
SKIP
PR59 *0_6
PR133 0_4
PR136 10K/F_6
PR138 0_4
SYS_HWPG [22]
(Peak 7.733A,AVG 5.801A)
Total capacitor : 150 uF
ESR : 25mΩ
f : 500k Hz
OCP : 9.5A
AO4710 Rdson=11.8~14.2mOhm
+3VPCU OCP:4.5A 500K
L(ripple current)
=(19-3.3)*3.3/(2.2u*500k*19)
~2.479A Let Iocp = 9.5A
(9.5 - 2.479 / 2) * 14.2mohm = (R * 5uA) / 10
R(Ilim) = 235Kohm
MAIND
MAIND [27,31]
F3B
PC148 *2200p/50V_4
PQ27 AO4468
+5V
3.014A
PC149 *2200p/50V_4
PQ28 AO3404
+3V
3.21A
Modified on 04/16
Modified on 04/08
[22] S5_ON
PR67 1M_6
PR68 22_8
PR61 22_8
PR64 100K/F_4
PQ16 DTC144EU
PR65 1M_6
PQ17 DMN601K-7
PQ12 DMN601K-7
PR143 1M_6
PC150 *2200p/50V_4
PC147 *2200p/50V_4
PQ31 DMN601K-7
PQ32 AO4468
+3V_S5
2.567A
PC151 *2200p/50V_4
PQ29 2N7002K
+5V_S5
0.002A
S5D
Quanta Computer Inc.
PROJECT : BU3
Size
Document Number
SYSTEM 5V/3V (ISL6237)
Rev D3B
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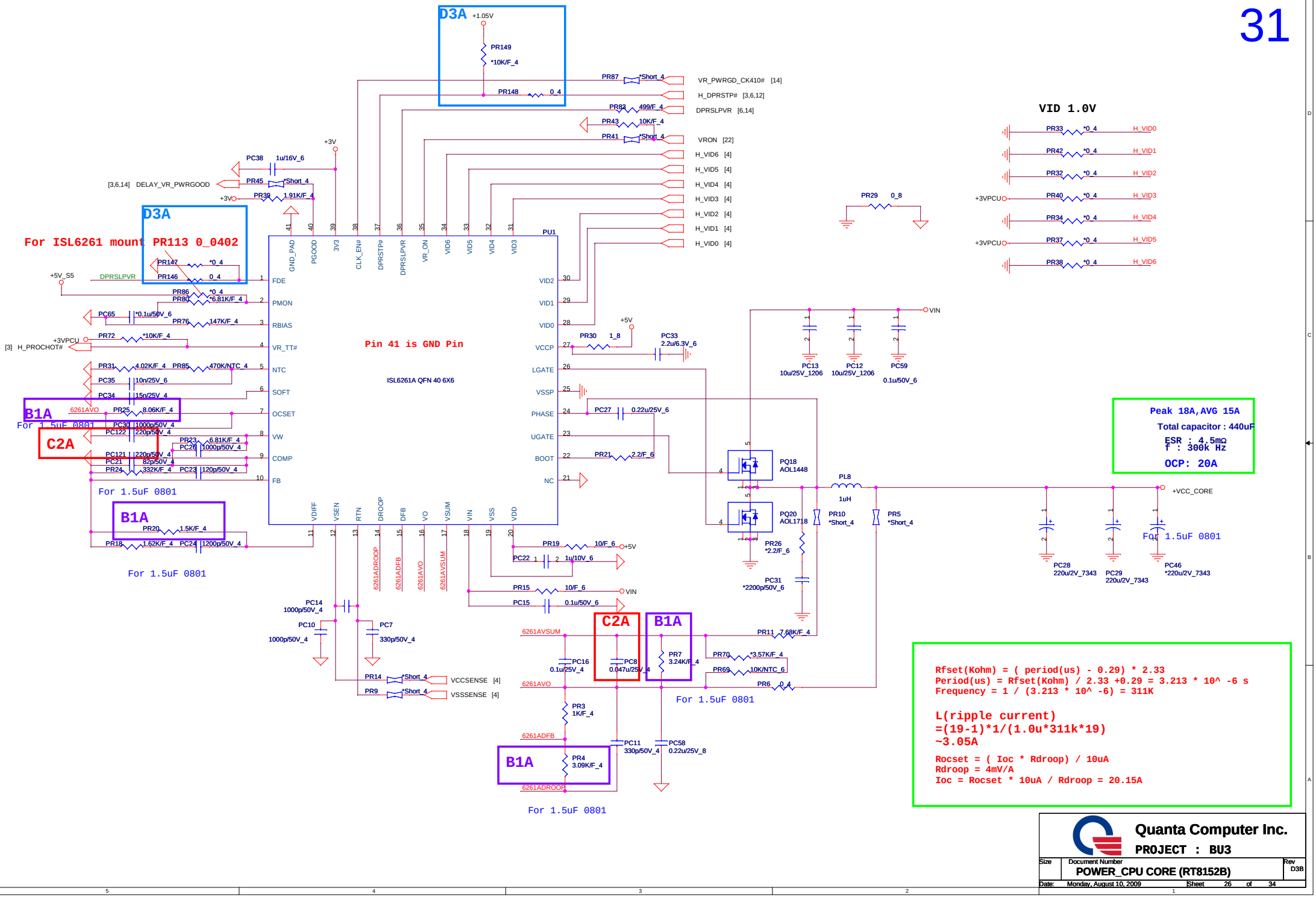
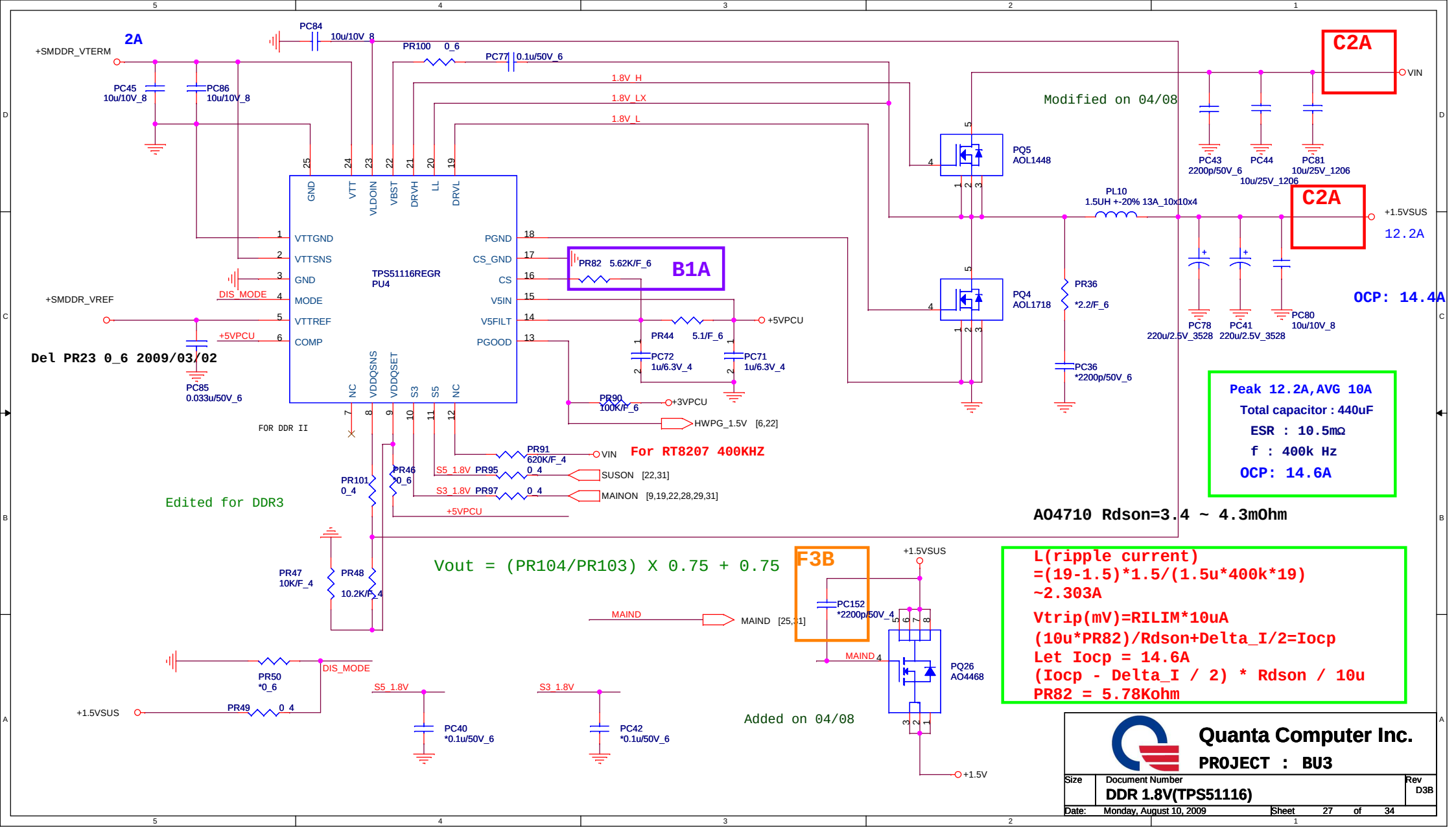


Quanta Computer Inc.			
PROJECT : BU3			
Size	Document Number		Rev
	POWER_CPU CORE (RT8152B)		D3B
Date: Monday, August 10, 2009	Sheet 26 of 34		


2A
+SMDDR_VTERM
PC84
10u/10V_8
PR100 0_6
PC77 0.1u/50V_6
1.8V_H
1.8V_LX
1.8V_L
PC45 10u/10V_8
PC86 10u/10V_8
Modified on 04/08
C2A
VIN
PQ5 AOL1448
PC43 2200p/50V_6
PC44 10u/25V_1206
PC81 10u/25V_1206
PL10 1.5UH +-20% 13A_10x10x4
C2A
+1.5VSUS
12.2A
OCP: 14.4A
PQ4 AOL1718
PR36 *2.2/F_6
PC78 220u/2.5V_3528
PC41 220u/2.5V_3528
PC80 10u/10V_8
PC36 *2200p/50V_6
TPS51116REGR PU4
GND
VTT
VLDOIN
VBST
DRVH
LL
DRVL
VTTGND
VTTSNS
GND
MODE
VTTREF
COMP
PGND
CS_GND
CS
V5IN
V5FILT
PGOOD
NC
VDDQSNS
VDDQSET
S3
S5
NC
DIS_MODE
+SMDDR_VREF
+5VPCU
PR82 5.62K/F_6
B1A
PR44 5.1/F_6
PC72 1u/6.3V_4
PC71 1u/6.3V_4
PR90 100K/F_6
+3VPCU
HWPG_1.5V [6,22]
Del PR23 0_6 2009/03/02
PC85 0.033u/50V_6
FOR DDR II
PR91 620K/F_4
VIN
For RT8207 400KHZ
PR46 0_6
S5_1.8V PR95 0_4
SUSON [22,31]
PR101 0_4
S3_1.8V PR97 0_4
MAINON [9,19,22,28,29,31]
+5VPCU
Edited for DDR3
Peak 12.2A,AVG 10A
Total capacitor : 440uF
ESR : 10.5mΩ
f : 400k Hz
OCP: 14.6A
AO4710 Rdson=3.4 ~ 4.3mOhm
PR47 10K/F_4
PR48 10.2K/F_4
Vout = (PR104/PR103) X 0.75 + 0.75
F3B
+1.5VSUS
PC152 *2200p/50V_4
MAIND
MAIND [25,31]
MAIND
PQ26 AO4468
L(ripple current)
=(19-1.5)*1.5/(1.5u*400k*19)
~2.303A
Vtrip(mV)=RILIM*10uA
(10u*PR82)/Rdson+Delta_I/2=Iocp
Let Iocp = 14.6A
(Iocp - Delta_I / 2) * Rdson / 10u
PR82 = 5.78Kohm
PR50 *0_6
DIS_MODE
PR49 0_4
+1.5VSUS
S5_1.8V
PC40 *0.1u/50V_6
S3_1.8V
PC42 *0.1u/50V_6
Added on 04/08
+1.5V
Quanta Computer Inc.
PROJECT : BU3
Size
Document Number
DDR 1.8V(TPS51116)
Rev D3B
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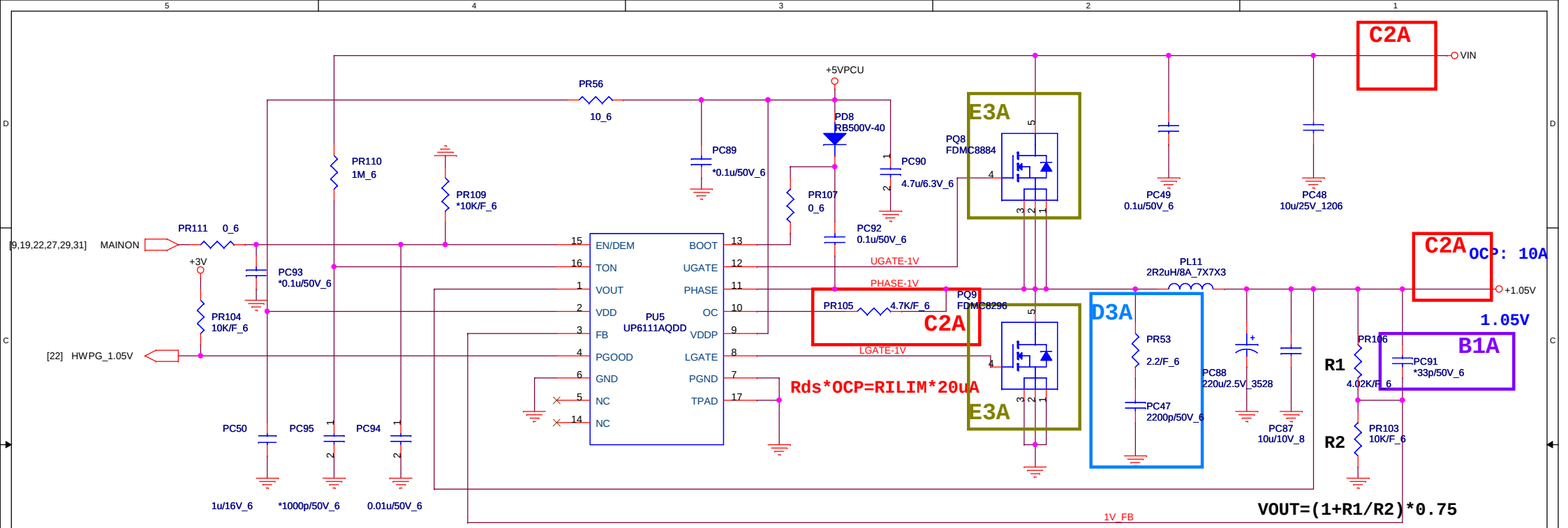

TON=3.85p*RTON*Vout/(Vin-0.5)
TOFF = (Vin / Vout -1)* Ton
TON = 2.185* 10^ -7
TOFF = 3.736 * 10 ^ -6
Frequency = 1 / (Ton + Toff) ~ 253K

FDMC8296 Rdson= 8 mOhm

L(ripple current)
=(19-1.05)*1.05/(2.2u*253k*19)
~1.78A

Let Iocp = 10A
Iocp - Iripple / 2 = RILIM * 20u /Rdson
10 - 1.78 / 2 = RILIM * 20u / 8mohm
RILIM = 3.644Kohm

(Peak 21.199A,AVG 8A)
Total capacitor : 230 uF
ESR : 21mΩ
f : 253k Hz
OCP :10A

Quanta Computer Inc.
PROJECT : BU3

Size	Document Number	Rev
	VCCP 1.05V(UP6111AQDD)	D3B
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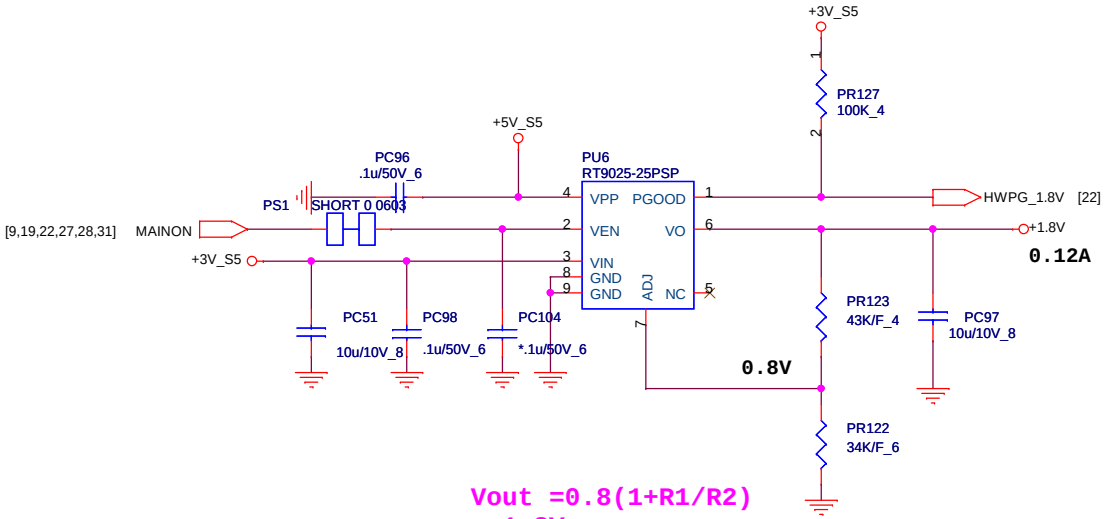

Quanta Computer Inc.		
PROJECT : BU3		
Size	Document Number: VCCP 1.05V(UP6111AQDD)	Rev: D3B
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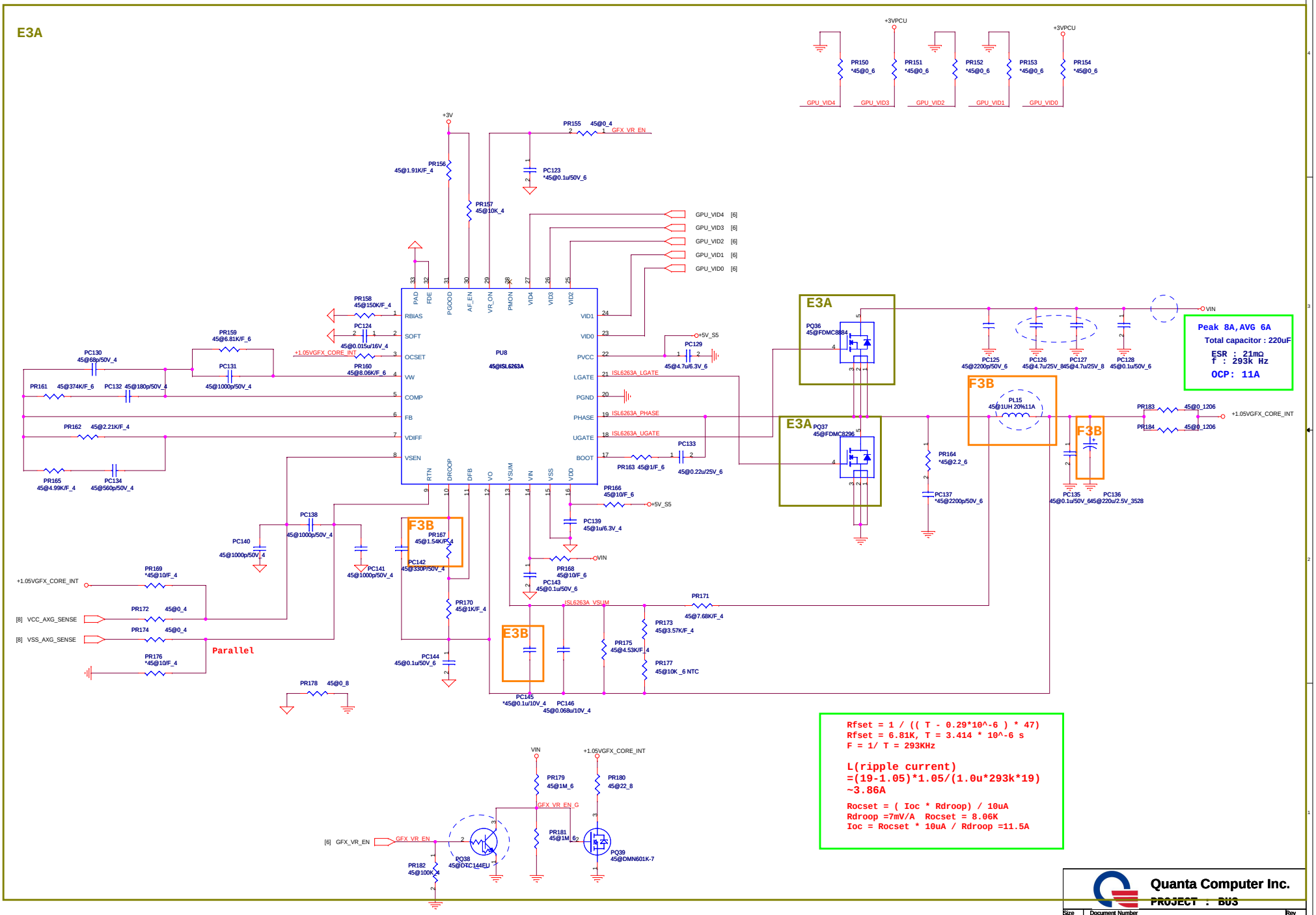
E3A
+3VPCU
PR150 *45@0_6
PR151 *45@0_6
PR152 *45@0_6
PR153 *45@0_6
PR154 *45@0_6
GPU_VID4
GPU_VID3
GPU_VID2
GPU_VID1
GPU_VID0
+3V
PR155 45@0_4
GFX_VR_EN
PR156 45@1.91K/F_4
PC123 *45@0.1u/50V_6
PR157 45@10K_4
GPU_VID4 [6]
GPU_VID3 [6]
GPU_VID2 [6]
GPU_VID1 [6]
GPU_VID0 [6]
PU8
45@ISL6263A
PAD
FDE
PGOOD
AF_EN
VR_ON
PMON
VID4
VID3
VID2
VID1
VID0
PVCC
LGATE
PGND
PHASE
UGATE
BOOT
RBIAS
SOFT
OCSET
VW
COMP
FB
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
VSS
VDD
PR158 45@150K/F_4
PC124 45@0.015u/16V_4
+1.05VGFX_CORE_INT
PR160 45@8.06K/F_6
PR159 45@6.81K/F_6
PC131 45@1000p/50V_4
PC130 45@68p/50V_4
PR161 45@374K/F_6
PC132 45@180p/50V_4
PR162 45@2.21K/F_4
PR165 45@4.99K/F_4
PC134 45@560p/50V_4
+5V_S5
PC129 45@4.7u/6.3V_6
ISL6263A_LGATE
ISL6263A_PHASE
ISL6263A_UGATE
PC133 45@0.22u/25V_6
PR163 45@1/F_6
PR166 45@10/F_6
PC139 45@1u/6.3V_4
PC138 45@1000p/50V_4
PC140 45@1000p/50V_4
PC141 45@1000p/50V_4
F3B
PR167 45@1.54K/F_4
PC142 45@330P/50V_4
PR170 45@1K/F_4
PC144 45@0.1u/50V_6
VIN
PR168 45@10/F_6
PC143 45@0.1u/50V_6
ISL6263A_VSUM
PR171 45@7.68K/F_4
PR173 45@3.57K/F_4
PR175 45@4.53K/F_4
PR177 45@10K_6 NTC
E3B
PC145 *45@0.1u/10V_4
PC146 45@0.068u/10V_4
PR178 45@0_8
+1.05VGFX_CORE_INT
PR169 *45@10/F_4
[8] VCC_AXG_SENSE
PR172 45@0_4
[8] VSS_AXG_SENSE
PR174 45@0_4
PR176 *45@10/F_4
Parallel
E3A
PQ36 45@FDMC8884
E3A
PQ37 45@FDMC8296
PC125 45@2200p/50V_6
PC126 45@4.7u/25V_8
PC127 45@4.7u/25V_8
PC128 45@0.1u/50V_6
VIN
Peak 8A, AVG 6A
Total capacitor : 220uF
ESR : 21mΩ
f : 293k Hz
OCP: 11A
F3B
PL15 45@1UH 20%11A
PR164 *45@2.2_6
PC137 *45@2200p/50V_6
F3B
PC135 45@0.1u/50V_6
PC136 45@220u/2.5V_3528
PR183 45@0_1206
PR184 45@0_1206
+1.05VGFX_CORE_INT
Rfset = 1 / ((T - 0.29*10^-6) * 47)
Rfset = 6.81K, T = 3.414 * 10^-6 s
F = 1/ T = 293KHz
L(ripple current)
=(19-1.05)*1.05/(1.0u*293k*19)
~3.86A
Rocset = (Ioc * Rdroop) / 10uA
Rdroop =7mV/A Rocset = 8.06K
Ioc = Rocset * 10uA / Rdroop =11.5A
VIN
+1.05VGFX_CORE_INT
PR179 45@1M_6
PR180 45@22_8
GFX_VR_EN_G
[6] GFX_VR_EN
GFX_VR_EN
PR181 45@1M_6
PQ38 45@DTC144EU
PQ39 45@DMN601K-7
PR182 45@100K
Quanta Computer Inc.
PROJECT : B03
Size
Document Number
1.05V_GFX (ISL6263A)
Rev D3B
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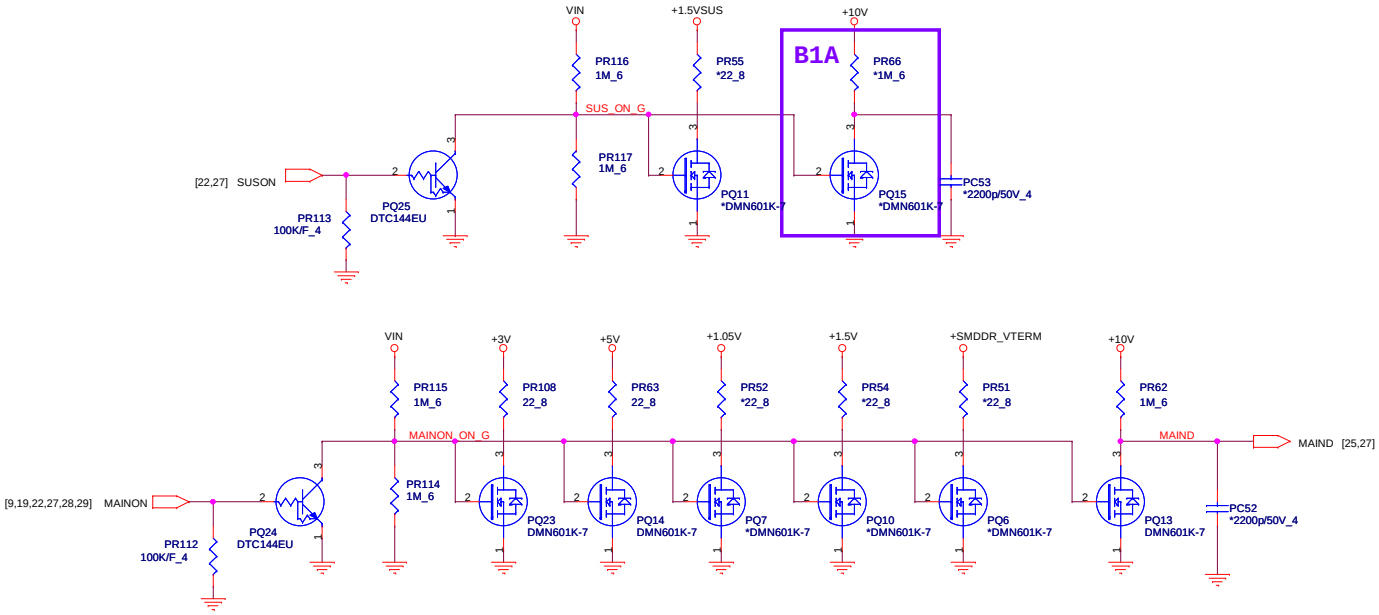

Quanta Computer Inc.

PROJECT : BU3

Size	Document Number	Rev
	Discharge/1.5/2.5V	D3B
Date: Monday, August 10, 2009	Sheet 31 of 34	

Model	REV	CHANGE LIST
BU3 MB	B1B	PAGE 2: add RP21 value 3G@0X2 ,add net name CLK_PCIE_3G to 3G Card pin13 & CLK_PCIE_3G# to 3G Card pin11
		PAGE 13: Add net name PCIE_RXN3,PCIE_RXP3,PCIE_TXN3,PCIE_TXP3 to 3G connector
		PAGE 13: Add C386,C382 both value 3G@0.1u/10V_4
		PAGE 13: del USB5-,USB5+ net
		PAGE 13: add USB7-,USB7+ net to sim connector
		PAGE 18: del HDMI function U17,R298,R299,R303,R305,R307,R309,R320,R323,R308,R306,R304,R310,R319,R317,R302,R297,R296,R312,R157
		PAGE 18: del HDMI function C365,C369,C356,C354,Q28,RN,4,RN5,RNN6,RN3,L20.L21.L22.L23,Q28
		PAGE 20: change Q20 PIN 2 net neme +3V_S5 to WIMAX_P
		PAGE 20: change Q22,Q27 PIN 1 net neme +3V_S5 to +3VPCU
		PAGE 20: Add R380 value 0_8 between net +1.5V and net +1.5V_3G.
		PAGE 20: Add C383 value 0.01V/25_4,C384 value 0.1/10V_4,C385 value 10u/3.6V_8 between net +1.5V_3G and GND
		PAGE 20: change R253,R250 power source +3V_S5 to +3VPCU
		PAGE 20: Connect CN21 PIN 48,PIN 28,PIN 6 to +1.5V_3G
		PAGE 20: Add CN23 value 3G@88266-10001-06 for co-lay SIM card
		PAGE 20: CN21 Connect PIN 33 to PCIE_TXP3,Connect PIN 31 to PCIE_TXN3,Connect PIN 25 to RCIE_RXP3,Connect PIN 23 to PCIE_RXN3
		PAGE 20: Add Q31 value 3G@ME2N7002E,R296 value 3G@10K_4 for PCIE_WAKE to CN21 PIN 1
		PAGE 18: Change CN11 pin define to PORT-B_HPD#
		PAGE 21: Change CN6 footprint and pin define
		PAGE 2: Change CLOCK GEN SRC6 net CLK_PCIE_3G and CLK_PCIE_3G# for 3G card
		PAGE 2: Change CLOCK GEN SRC4 net CLK_PCIE_MINI1 and CLK_PCIE_MINI1# for mini card 1
		PAGE 20: Change D15 to R297 value 0805 ohm
		PAGE 21: Remove CN13
		PAGE 7: Change R116 value to 12.1K ohm, Add U17 for DDR3_POWER_OK
		PAGE 25: Change PR134 value to 169K ohm, change PR128 value to 174K phm . NC PR141
		PAGE 26: Change PR25 value to 8.06k ohm ,change PR20 value to 1.5K ohm ,change PR4 value to 3.09K ohm ,change PR7 value to 3.24k ohm.
		PAGE 27: Change PR82 value to 5.9k ohm
		PAGE 27: Change PR105 value 9.31K ohm , NC PC91
		PAGE 27: NC PR66,PQ15
		PAGE 20: Change CN22 footprint to minipci-80019-1021-52p-ruv-v ,chabge CN23 footprint to minipci-80052-1021-52p-ldv-v
		PAGE 21: Change HOLE 4 module
		PAGE 6: Change R116 value 12.1K/F_4 , add R378 & U22 for DDR3_POWER_OK
		PAGE 6: Change CN6 pin define.
		PAGE 27: Change PR82 value to 5.62K ohm
		PAGE 2: Swap vertical RP11,RP21
		PAGE 15 : Change R227 value to 100/F_6
		PAGE 19 : Change U6 value to GS@R5F211B4D31SP#W4(0217H)
		PAGE 14 : Add R382 to +3V_S5 for ICHP SCI#
		PAGE 17 : Change T79,T80,T82,T84,T83,T86, footprint to TP3050
		PAGE 20 : Add D19,D20 for 3G_LED# & WiMAX_LED# between CN6 PIN 8 3G_WIMAX_LED#
		PAGE 21 : Change CN9 PIN 33 DEFINE for MMC_LED#,change CN6 footprint 18pin
		PAGE 22 : Add R135 for battery state issue.
	C2A	PAGE 23 : Add Q33 Q32 C388 R383 R384 for LAN_P soft start, change CN4 pin define.
		PAGE 20 : change CN21 CN22 footprint
		PAGE 20 : remove CN13 and change CN8 connector module
		PAGE 14 : R191 always pull high for HDMI & USB BOI-FUNCTION
		PAGE 18 : Change CN11 PIN11 net to BOARD_ID4
		PAGE 28 : remove PL5 ,remove JP3, short by trace.
		PAGE 27 : remove PL4 ,remove JP2&JP1 , short by trace.
		PAGE 25 : remove PL12 &PL15,remove JP5 & JP4, short by trace.
		PAGE 24 : remove PL3 ,short by trace.
		PAGE 26 : PC8 change to CH3474K1B04 CAP CHIP 0.047U 25V(+-10% X7R 0402)
		PAGE 21 : Change CN9 PIN 24 net to 1.5V
		PAGE 22 : Add R135 for battery leakage current
		PAGE 26 : Add PU1 PIN8 & PIN9 PC121,PC122 CAP CHIP 220P 50V(+-10%,X7R,0402) to GND SINGAL
		PAGE 9 : Add C389 value 10u/6.3V_8, and change C187 value to 22u/6.3V_8 for CRT power noise issue,(reserve U23)
		PAGE 24 : Change PU3 Part number to AL088731001
		PAGE 22 : Change C255 and C257 value to 15p/50V_4
		PAGE 14 : Change R156 Part Number to CS23243F930
		PAGE 12 : Add R385 ,R386 for USB-ODD CO-LAY.(reserve)
	D3A	PAGE 24 : Change PD4 Footprint to d-5_375-3_975 for OPEN issue
		PAGE 21 : Change CN2 PIN1 NET from +5VPCU to +3VPCU
		PAGE 20 : Change R379 value to 100K_4 for WIFI INTEL module issue
		PAGE 13 : Add R388,R389 for reserve gemalto 3G sim card
		PAGE 18 : Reserve D21 and R387 to keep voltage 0.4 V

MODEL	BU3	
PAGE	FROM	To
1	1A	1B
2	1A	1B
3	1A	1B
4	1A	1B
5	1A	1B
6	1A	1B
7	1A	1B
8	1A	1B
9	1A	1B
10	1A	1B
11	1A	1B
12	1A	1B
13	1A	1B
14	1A	1B
15	1A	1B
16	1A	1B
17	1A	1B
18	1A	1B
19	1A	1B
20	1A	1B
21	1A	1B
22	1A	1B
23	1A	1B
24	1A	1B
25	1A	1B
26	1A	1B
27	1A	1B
28	1A	1B
29	1A	1B
30	1A	1B

DOC NO. 204					
PROJECT MODEL :	BU3	APPROVED BY:	Mosy Li	DATE:	2009/04/27
PART NUMBER:	31BU3MB0000	DRAWING BY:	Mosy Li	REVISON:	1B

Quanta Computer Inc.
PROJECT : BU3
Size | Document Number: Change list | Rev: D3B
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CHANGE LIST

Model	REV	
BU3 MB	D3A	PAGE 26: Add PR146,PR147,PR148 value 0_4 ,PR149 value 10K/F_4 for power suggest
		PAGE 22: Add D22 for ESD/EOS suggestion - Power pin EOS
		PAGE 22: C386,C382,RP21不上件
		PAGE 02: change C373,C374 value to 33p/50V_4 for XTAL report
		PAGE 20: reserve Q31,R381,R380,C383,C384,C385
	E3A	PAGE 17: reserve CRT FILTER R390,R393,R394,C398,C399,C400,C401,C402,C403 for EMI requirement.
		PAGE 21: add C390,C391,C392,C393,C394,C395,C396,C397 for EMI requirement .
		PAGE 30: add 1.05v_GFX SCHEMATIC for reader stand by function (GS45 only)
		PAGE 28: change PQ8 and PQ9 value and footprint .
		PAGE 17: Add R3,R2 BOI-OPTION for GS40.
		PAGE 17: Add R392 ,R391 for Board ID3
		PAGE 21: Add HOLE 9,HOLE 11, HOLE 10.
	F3A	PAGE (12) :Change R244 to bead 120ohm, C324 to 22PF for EMI requirement.
		PAGE (24) : Add PR88, PR35 for Adapter Voltage monitor
		PAGE (17) : Reserve U25 for LVDS_VADJ option (support XP function key).
		PAGE (25) : Reserve PC147,PC148,PC149,PC150,PC151,PC152 for power soft start
		PAGE (21) : Change CN9 connector pin define to 40 pin
		PAGE (17) : Change D1 footprint
		PAGE (18) : Change HDMI CN11 connector PIN DEFINE
		PAGE (22) : R176,RP7,RP8,L2,R138,R161,R377,R199,R251,R351,R213,R225,R211,R373,R357,R240,R212,R217,R175,R342,R155,R48,R59,R112,R111,R130,R131,R288,R284,R62,R91,R41,R134 replace by short pad
		PAGE (22) : R378,R68,R279,R12,RP17,RP15,RP16,RP14,RP13,RP12,RP11,RP10,RP9,R293,R8 replace by short pad
		PAGE (22) : Change CN9 pin define. 40PINS
		PAGE (30) : Change PL15 from 2.2uH to 1uH , PC145 change to unmounted , PR167 change to 1.54K , PC136 should be mounted for 3D hang up issue.
		PAGE (09) : reserve C186,C149,C269,C247,C113,C342,C154,C135 for cost down

MODEL BU3

PAGE	FROM	To
1	1A	1B
2	1A	1B
3	1A	1B
4	1A	1B
5	1A	1B
6	1A	1B
7	1A	1B
8	1A	1B
9	1A	1B
10	1A	1B
11	1A	1B
12	1A	1B
13	1A	1B
14	1A	1B
15	1A	1B
16	1A	1B
17	1A	1B
18	1A	1B
19	1A	1B
20	1A	1B
21	1A	1B
22	1A	1B
23	1A	1B
24	1A	1B
25	1A	1B
26	1A	1B
27	1A	1B
28	1A	1B
29	1A	1B
30	1A	1B

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PROJECT MODEL :	BU3	APPROVED BY:	Mosy Li	DATE:	2009/04/27
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	Change list	D3B

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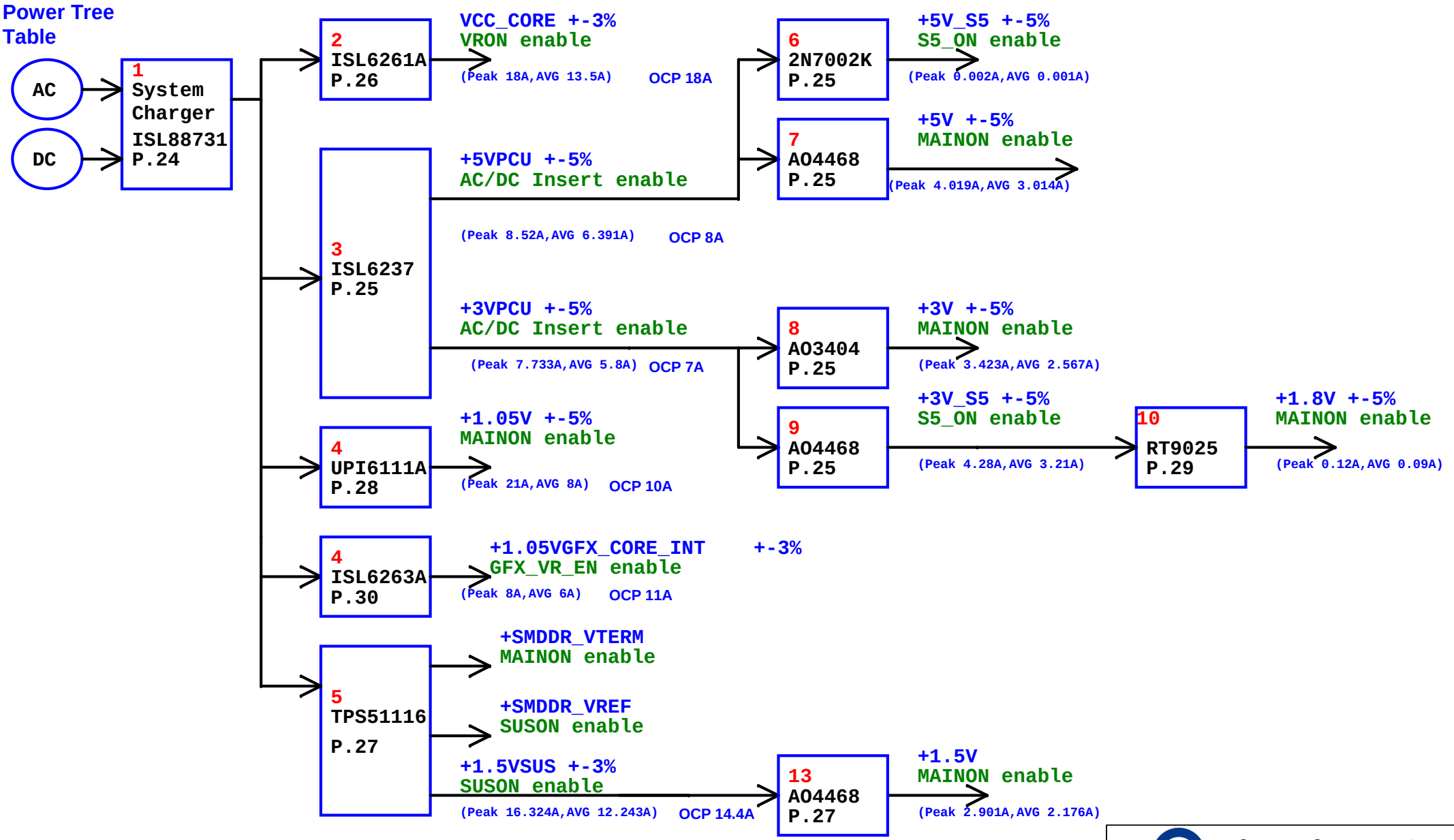
Power Tree Table



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	Power Tree Table	D3B
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